The Future of Analog IC Technology

MP5022A

16V, 12A, 3mΩ R_{DS_ON} Hot-Swap Protection Device With Current Monitoring

DESCRIPTION

The MP5022A is a hot-swap protection device designed to protect circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output.

At start up, in-rush current is limited by the slew rate at the output. The slew rate is controlled by external capacitor at the SS pin.

The maximum load at the output is current limited through a sense FET topology. The magnitude of the current limit is controlled by a low-power resistor from the ISET pin to ground.

An internal charge pump drives the gate of the power device, allowing for a power FET with a very low ON resistance of 3mΩ.

The MP5022A includes an IMON option that produces a voltage proportional to current through the power device set by a resistor from this pin to ground.

The MP5022A includes an optional discharge function that provides a discharge path for the external output capacitor when the part is disabled. Fault protection includes current limit, thermal shutdown and damaged MOSFET detection. The device also features over-voltage protection and under-voltage protection

The MP5022A is available in QFN-22 (3mmx5mm) package.

FEATURES

- 8V to 16V Operating Input Range
- Integrated 3mΩ Power FET
- Adjustable Current Limit
- Output Current Measurement
- +/-3% Current Monitor Accuracy(6A<Io<12A)
- Fast Response (<200ns) for Short Protection
- PG Detector and FLTB Indication
- PG Assert Low at VIN=0
- Damaged MOSFET Detection
- External Soft Start
- Programmable LOADEN Blanking Time
- Under/Over Voltage Lockout
- Thermal Protection
- Small QFN-22 (3mmx5mm) Package

APPLICATIONS

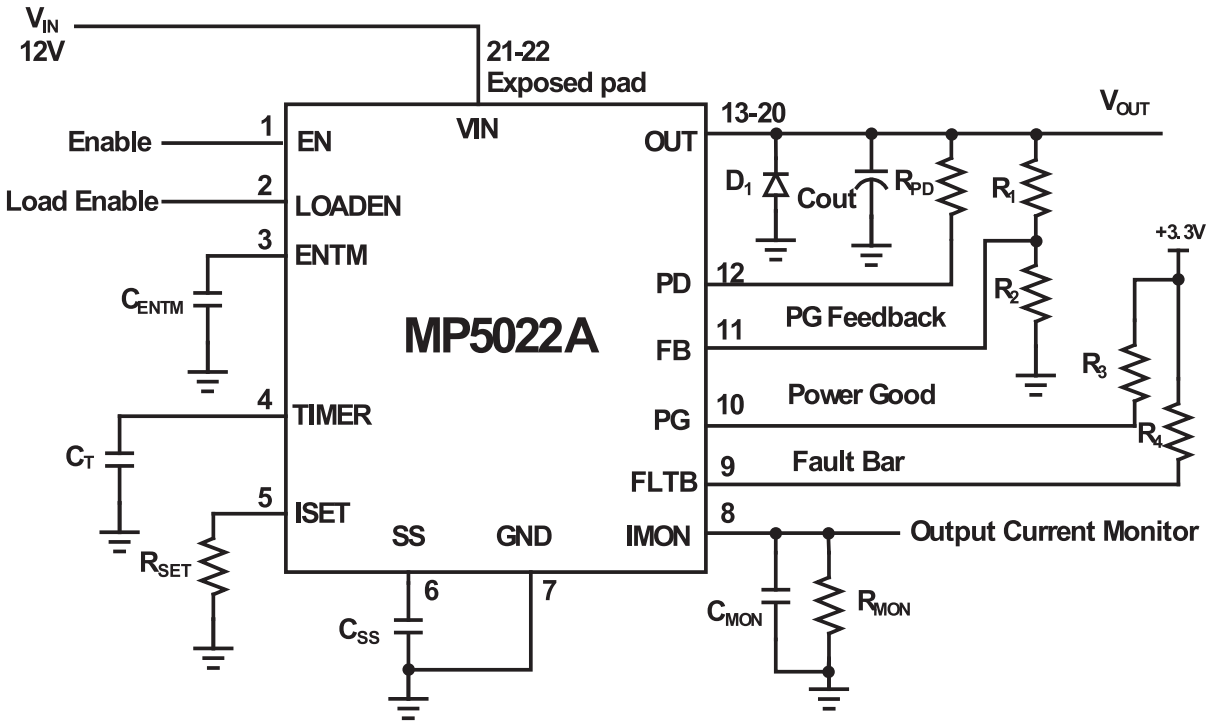
- Hot Swap
- PC Cards
- Disk Drives
- Servers
- Networking
- Laptops

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL APPLICATION



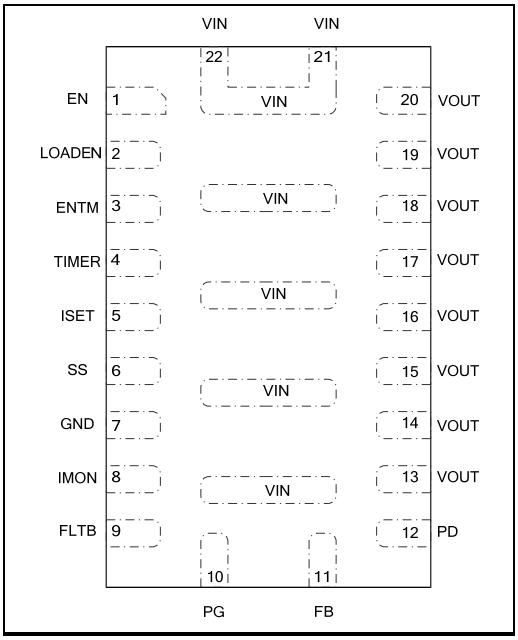
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5022AGQV	QFN-22 (3mmx5mm)	MP5022A

* For Tape & Reel, add suffix-Z (e.g. MP5022AGQV-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 24V
OUT, PD..... -0.3V to 20V
Other Pins ..... -0.3V to 6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 2.17W
Storage Temperature.....-65°C to +155°C
Operating Temperature .....-40°C to +125°C

Recommended Operating Conditions (3)

Input Voltage Operating Range..... 8V to 16V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-22 (3mmx5mm) .....46 ..... 10... °C/W

Notes:

1) Exceeding these ratings may damage the device..
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, R_{SET}=10.2k, C_{OUT}= 470µF, T_J=25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent Current	I_Q	EN=high, No load		1.3	2.0	mA
		Fault latch off		1.3		mA
		EN=0, V_{IN}=16V			500	µA
Power FET						
ON Resistance	R_{DSon}	T_J=25°C		3		mΩ
		T_J=85°C (5)		5		
Off-State Leakage Current	I_{OFF}	V_{IN}=24V, EN=0V			1	µA
Maximum Continuous Current (5)	I_{OUT_MAX}		15			A
Thermal Shutdown						
Shutdown Temperature (5)	t_{STD}			145		°C
Under/Over Voltage Protection						
Under Voltage Lockout Threshold	V_{UVLO}	UVLO Rising Threshold	6.5	7	7.5	V
UVLO Hysteresis	$V_{UVLOHYS}$			2		V
Over Voltage Lockout Threshold	V_{OVLO}	OVLO Rising Threshold	17	17.75	18.5	V
OVLO Hysteresis	$V_{OVLOHYS}$			490		mV
LOADEN Pin						
Low-Level Input Voltage	V_L				0.9	V
High-Level Input Voltage	V_H		2.3			V
Soft Start						
SS Pull-Up Current	I_{SS}	V_{SS}=0V	10	12.5	15	µA
Current Limit						
Current Limit at Normal Operation	I_{Limit_NO}	R_{SET} =10.2k	11.34	12.6	13.86	A
Current Limit Response Time(5)	t_{CL}			20		µs
Secondary Current Limit(5)	I_{LimitH}	Regardless of R_{SET}		36		A
Short Circuit Protection Response Time(5)	t_{SC}			200		ns
Output Current Monitor						
Gain of Current Sense Amplifier	A_{IMON}	6A<I_{OUT}<12A	9.7	10	10.3	µA/A
		3A<I_{OUT}<6A	9.5	10	10.5	µA/A
Max Voltage of IMON Pin	V_{IMON}				3	V
Timer						
Upper Threshold Voltage	V_{TMRH}		1.2	1.24	1.28	V
Insertion Delay Charge Current	I_{INSERT}		34.5	43	51.5	µA
Fault Detection Charge Current	I_{FLTD}		175	215	255	µA
Discharge R_{ON}	R_{FLTE}	I_{OUT} < I_{Limit}		35		Ω
LOADEN Blanking Time (ENTM pin)						
Upper Threshold Voltage	V_{ENTMRH}		1.2	1.24	1.28	V
Charge Current	I_{ENTMCC}		0.8	1.1	1.4	µA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{SET}=10.2k, C_{OUT}= 470µF, T_J=25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable						
Rising Threshold	V_{ENRS}		1.258	1.325	1.391	V
Hysteresis	V_{ENHYS}			170		mV
FB (Power Good Feedback)						
Feedback Rising Threshold	V_{FBH}		1.205	1.245	1.285	V
Hysteresis	V_{FBHYS}			85		mV
Fault Bar/Power Good						
Low-Level Output Voltage	V_{OL}	Sink current 1mA			0.2	V
Fault Bar Off-State Leakage Current	I_{FLT_LKG}	V_{FLTB}=3.3V			1	µA
Fault Bar Propagation Delay	t_{PDE}			14		µs
Power Good Off-State Leakage Current	I_{PG_LKG}	V_{PG}=3.3V			2.5	µA
PG Low-Level Output Voltage	V_{OL_100}	V_{IN}=0V, Pull up to 3.3V through 100kΩ resistor		600	720	mV
	V_{OL_10}	V_{IN}=0V, Pull up to 3.3V through 10kΩ resistor		720	870	mV

Notes:

5) Guaranteed by design.

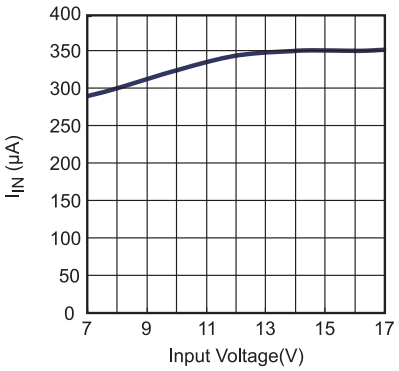
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, C_{OUT}=470uF, C_{ENTM}=1μF, C_T=220nF, C_{SS}=47nF, R_{SET}=6.8kΩ, T_A=+25°C, unless otherwise noted.

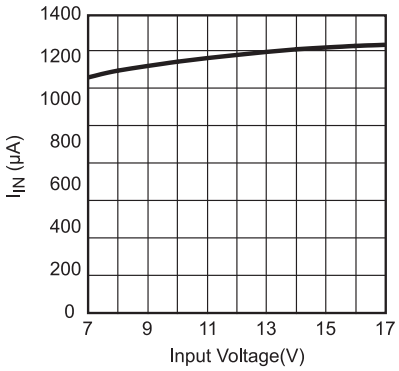
Disable Supply Current vs. Input Voltage

EN=0



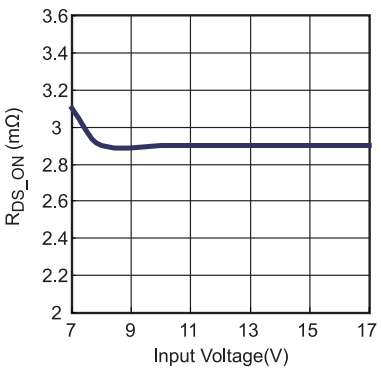
Enable Supply Current vs. Input Voltage

EN=NC, Loaden=3V, No Load



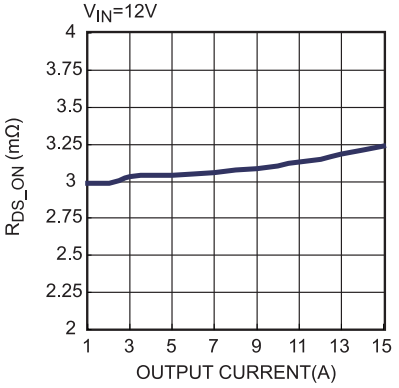
R_{DS_ON} vs. Input Voltage

I_{OUT}=1A

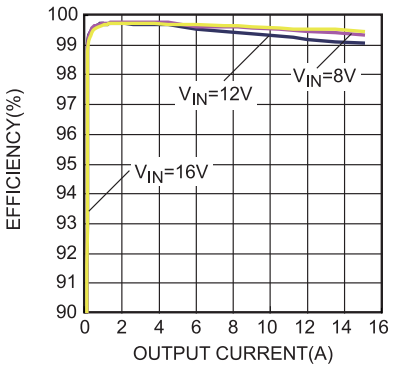


R_{DS_ON} vs. Load Current

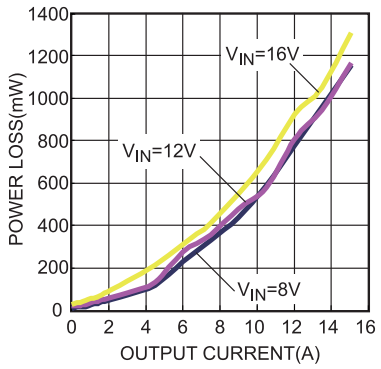
V_{IN}=12V



Efficiency vs. Load Current

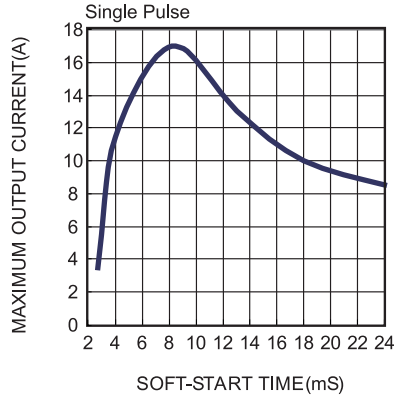


Power Loss vs. Load Current



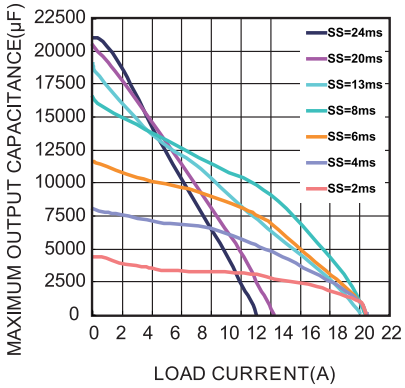
Maximum Output Current vs. Soft Start Time

V_{IN}=12V, C_{OUT}=4700μF, En On, Single Pulse

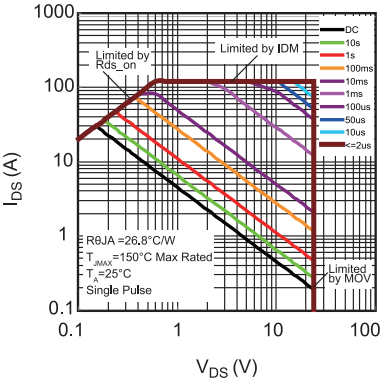


Maximum Output Cap. vs. Load Current

V_{IN}=12V, En On, Single Pulse



Safe Operation Area



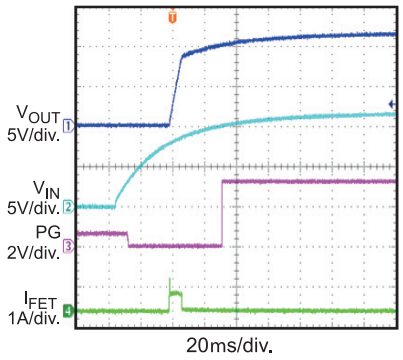
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, C_{OUT}=470uF, C_{ENTM}=1μF, C_T=220nF, C_{SS}=47nF, R_{SET}=6.8kΩ, T_A=+25°C, unless otherwise noted.

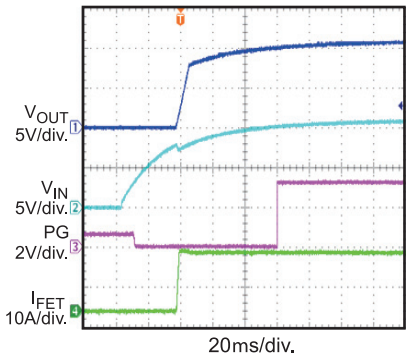
Start Up through V_{IN}

I_{OUT}=0A



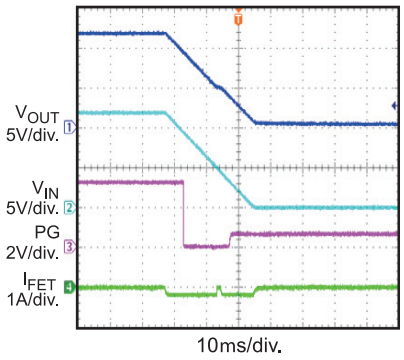
Start Up through V_{IN}

I_{OUT}=15A



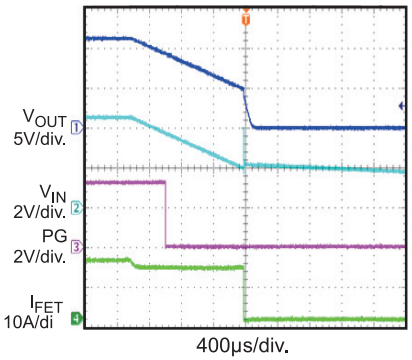
Shut Down through V_{IN}

I_{OUT}=0A



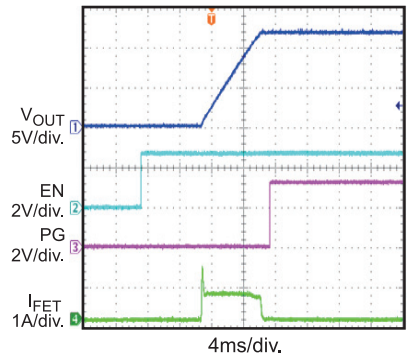
Shut Down through V_{IN}

I_{OUT}=15A



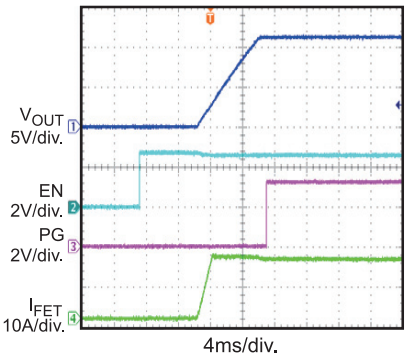
Start Up through EN

I_{OUT}=0A



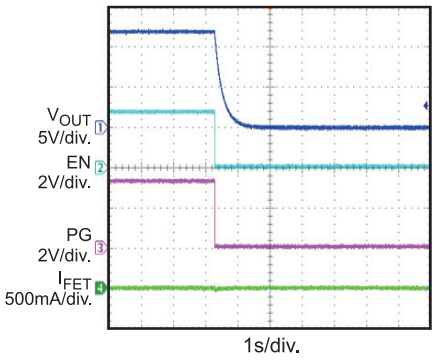
Start Up through EN

I_{OUT}=15A



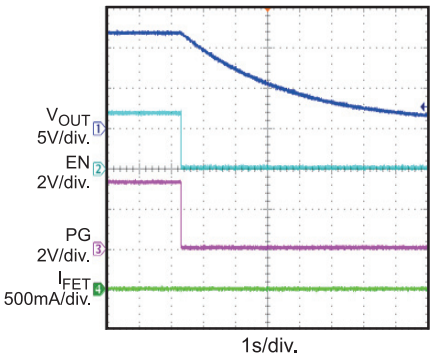
Shut Down through EN

I_{OUT}=0A, with R_{PD}=100Ω



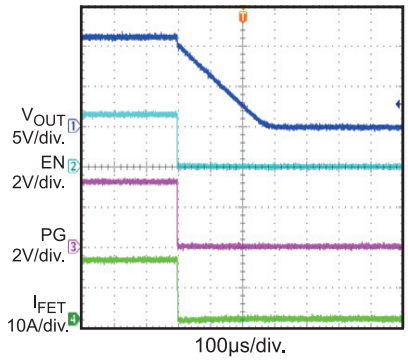
Shut Down through EN

I_{OUT}=0A, PD float



Shut Down through EN

I_{OUT}=15A



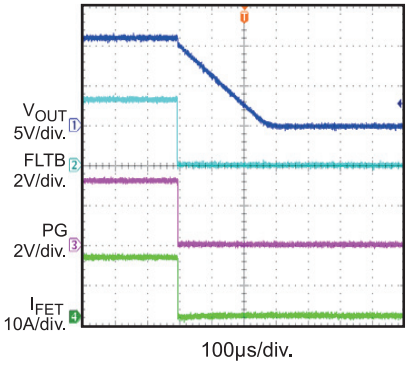
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, C_{OUT}=470uF, C_{ENTM}=1μF, C_T=220nF, C_{SS}=47nF, R_{SET}=6.8kΩ, T_A=+25°C, unless otherwise noted.

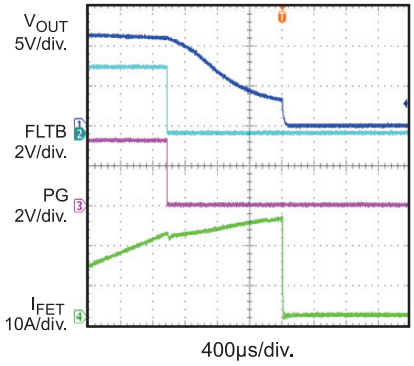
Thermal Shutdown

I_{OUT}=15A



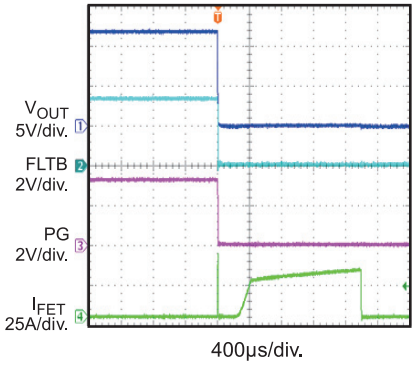
OCP

I_{LIMIT}=19A



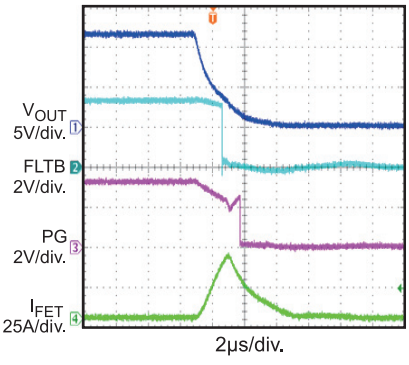
SCP Entry

I_{LIMIT}=19A



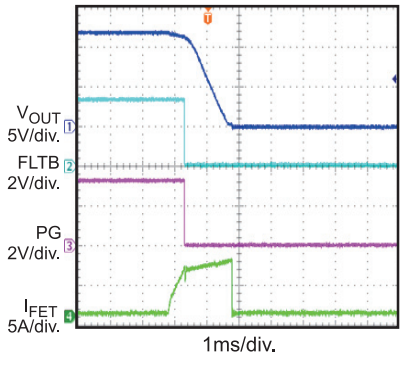
SCP Entry Detail

I_{LIMIT}=19A



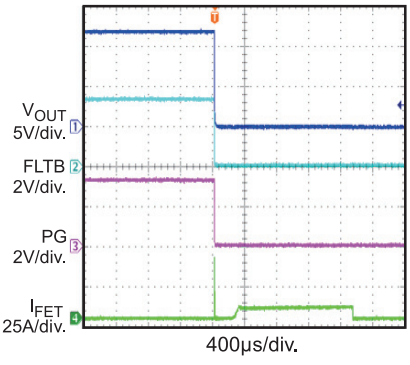
OCP

I_{LIMIT}=5A



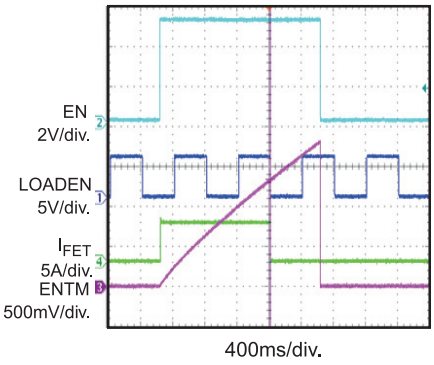
SCP Entry

I_{LIMIT}=5A



EN and LOADEN Logic

I_{OUT}=5A, EN and LOADEN signals are generated by function generator



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PIN FUNCTIONS

<table>
<tr><th>Pin #</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>EN</td><td>Enable Input. EN is used to control the ON/OFF of the MP5022A together with LOADEN pin. EN pin is pulled high internally.</td></tr>
<tr><td>2</td><td>LOADEN</td><td>Load Enable Input. LOADEN is used to control the ON/OFF of the MP5022A together with EN pin as the table shows below. LOADEN is used to shut down the power switch after LOADEN blanking time but can’t turn it on by recycle LOADEN only.
<table>
<tr><th>LOADEN-Blanking–Time is over?</th><th>EN</th><th>LOADEN</th><th>Status</th></tr>
<tr><td>N</td><td>0</td><td>0</td><td>OFF</td></tr>
<tr><td>N</td><td>0</td><td>1</td><td>OFF</td></tr>
<tr><td>N</td><td>1</td><td>0</td><td>ON</td></tr>
<tr><td>N</td><td>1</td><td>1</td><td>ON</td></tr>
<tr><td>Y</td><td>0</td><td>0</td><td>OFF</td></tr>
<tr><td>Y</td><td>0</td><td>1</td><td>OFF</td></tr>
<tr><td>Y</td><td>1</td><td>0</td><td>OFF</td></tr>
<tr><td>Y</td><td>1</td><td>1</td><td>ON</td></tr>
</table></td></tr>
<tr><td>3</td><td>ENTM</td><td>LOADEN-Blanking–Time Set. Connect an external capacitor to set the LOADEN blanking time. Once EN is active, the timer starts and the LOADEN de-assertion is blanked. The switch shuts down in the presence of a fault or EN low, but LOADEN low during blanking time has no effect.</td></tr>
<tr><td>4</td><td>TIMER</td><td>Timer Set. An external capacitor sets the hot-plug insertion time delay, fault timeout period.</td></tr>
<tr><td>5</td><td>ISET</td><td>Current Limit Set. Place a resistor to ground to set the value of the over current limit.</td></tr>
<tr><td>6</td><td>SS</td><td>Soft-Start. An external capacitor connected sets the soft-start time of the output voltage. The internal circuit controls the slew rate of the output voltage at turn-on. Float this pin to set the soft start time at its minimum of 1ms.</td></tr>
<tr><td>7</td><td>GND</td><td>Ground.</td></tr>
<tr><td>8</td><td>IMON</td><td>Output Current Monitor. Provides a voltage proportional to the current flowing through the power device. Placing 10k resistor (R_{MON}) to ground creates a 0V to 1.5V voltage when current ranges from 0A to 15A. Place a more than 10nF capacitor paralleled R_{MON} in application.</td></tr>
<tr><td>9</td><td>FLTB</td><td>Fault Bar. This is an open drain output that drives to ground when an over-current or a thermal shutdown occurs. Pull-up to an external power supply through a 10k-100kΩ resistor.</td></tr>
<tr><td>10</td><td>PG</td><td>Power Good. This is an open drain output. Pull-up to external power supply through a 10k-100kΩ resistor. High means power good. Low indicates output is outside UVLO/OVLO window. PG indication starts to work when pull-up supply is established even the VIN and EN are still disabled.</td></tr>
<tr><td>11</td><td>FB</td><td>Feedback. An external resistor divider from the output sets the output voltage where the PG pin switches. The rising threshold is 1.245V with 85mV hysteresis.</td></tr>
<tr><td>12</td><td>PD</td><td>Output Discharge. Connect to the output through more than 100Ω resistor to discharge the output when the part is disabled by Enable pin. Leave it open disables this function.</td></tr>
<tr><td>13-20</td><td>OUT</td><td>Output. Voltage controlled by the IC. A schottky diode should be placed between the OUT pin and GND pin to absorb the negative voltage spike.</td></tr>
<tr><td>21-22, Exposed Pads</td><td>VIN</td><td>Input Power Supply. Add a RCD clamping circuit close to VIN when the input capacitor is below 10uF. Please refer to Figure 10 in “TYPICAL APPLICATION” part. It is used to hold the line voltage when output short circuit happens.</td></tr>
</table>

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

BLOCK DIAGRAM

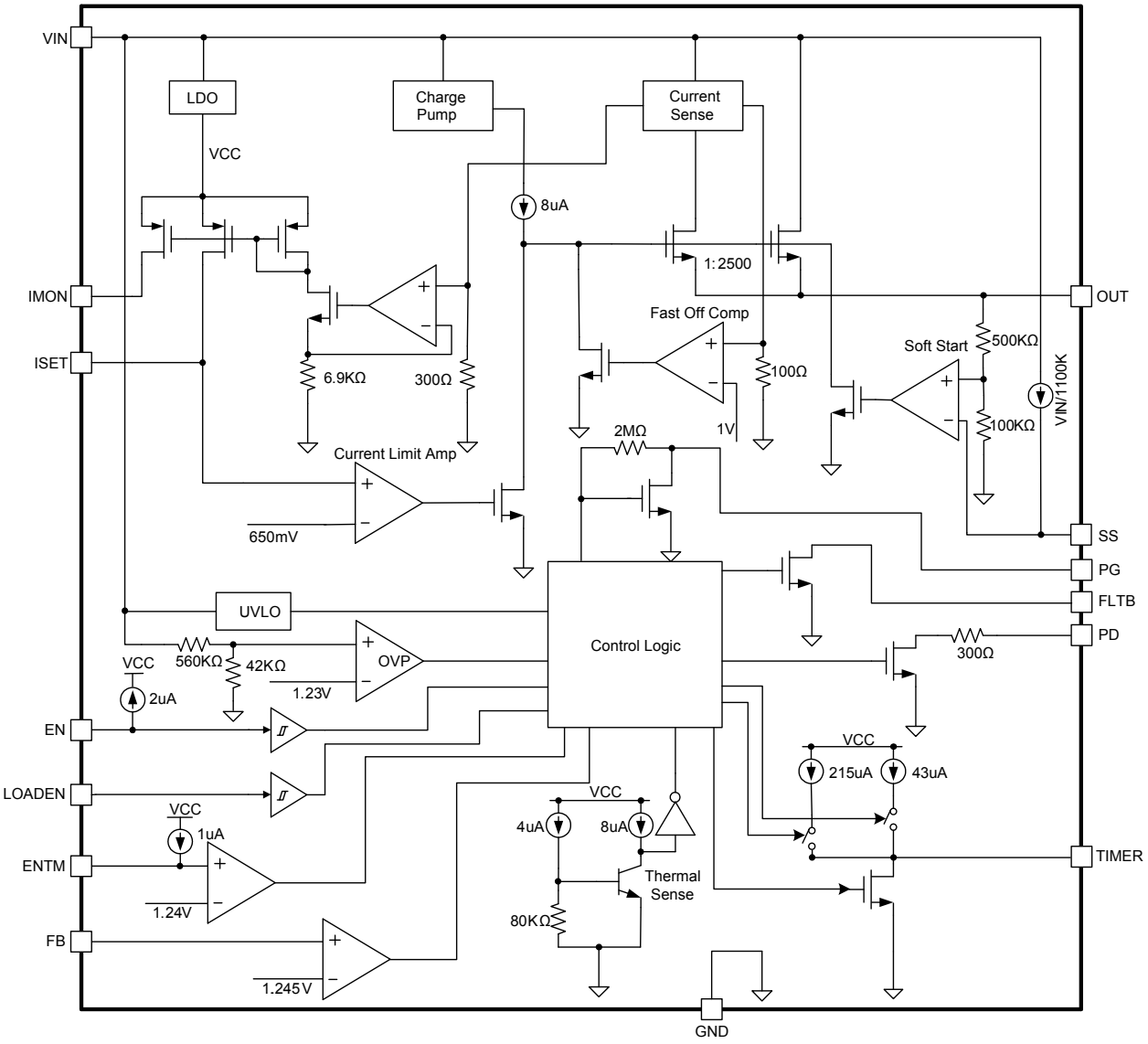


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

OPERATION

The MP5022A is designed to limit the in-rush current to the load when a circuit card is inserted into a live backplane power source; thereby limiting the backplane's voltage drop and the dv/dt of the voltage to the load. It provides an integrated solution to monitor the input voltage, output voltage, output current, and die temperature to eliminate the need for an external current sense power resistor, power MOSFET, and thermal sense device.

Current Limit

The MP5022A provides a constant current limit that can be programmed by an external resistor. Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant. In order to limit the current, the gate to source voltage needs to be regulated from 4V to around 1V. The typical response time is about 20μs and the output current may have a small overshoot during this time period.

When the current limit triggers, the fault timer starts. If the output current falls below the current limit threshold before the end of the fault timeout period, the MP5022A resumes normal operation. Otherwise, if current limit duration exceeds the fault timeout period, the power FET is latched off.

When the device reaches either its current limit or its over-temperature threshold, the FLTB pin is driven low with a 14μs propagation delay to indicate a fault. The desired current limit at normal operation is a function of the external current limit resistor.

Short-Circuit Protection

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold by a lot before the control loop can respond. If the current reaches a 36A secondary current limit level, a fast turn-off circuit activates to turn off the power FET using a 100mA pull-down gate discharge current, as shown in Figure 2. This limits the peak current through the switch to limit the input voltage drop. The total short circuit response time is about 200ns. When the chip triggers short-circuit protection, it will restart once more which used to check whether the over load condition exists or not. If short-circuit is induced by input line transient, the part will work normally, If real short circuit happens, the part will latch off absolutely. Details see Figure 2 and Figure 3.

FLTB switches low once it reaches a 36A current limit, and asserts low until the short circuit is removed.

Fault Timer & Restart

When the current reaches its limit threshold, a 215μA fault timer current source charges the external capacitor C_T at the TIMER pin. If the current limit state ceases before the TIMER pin reaches 1.24V, the MP5022A returns to normal operation mode and it will release timer immediately when current limit remove. If the current limit state lasts beyond the TIMER pin voltage reaches 1.24V, the power FET switches off.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

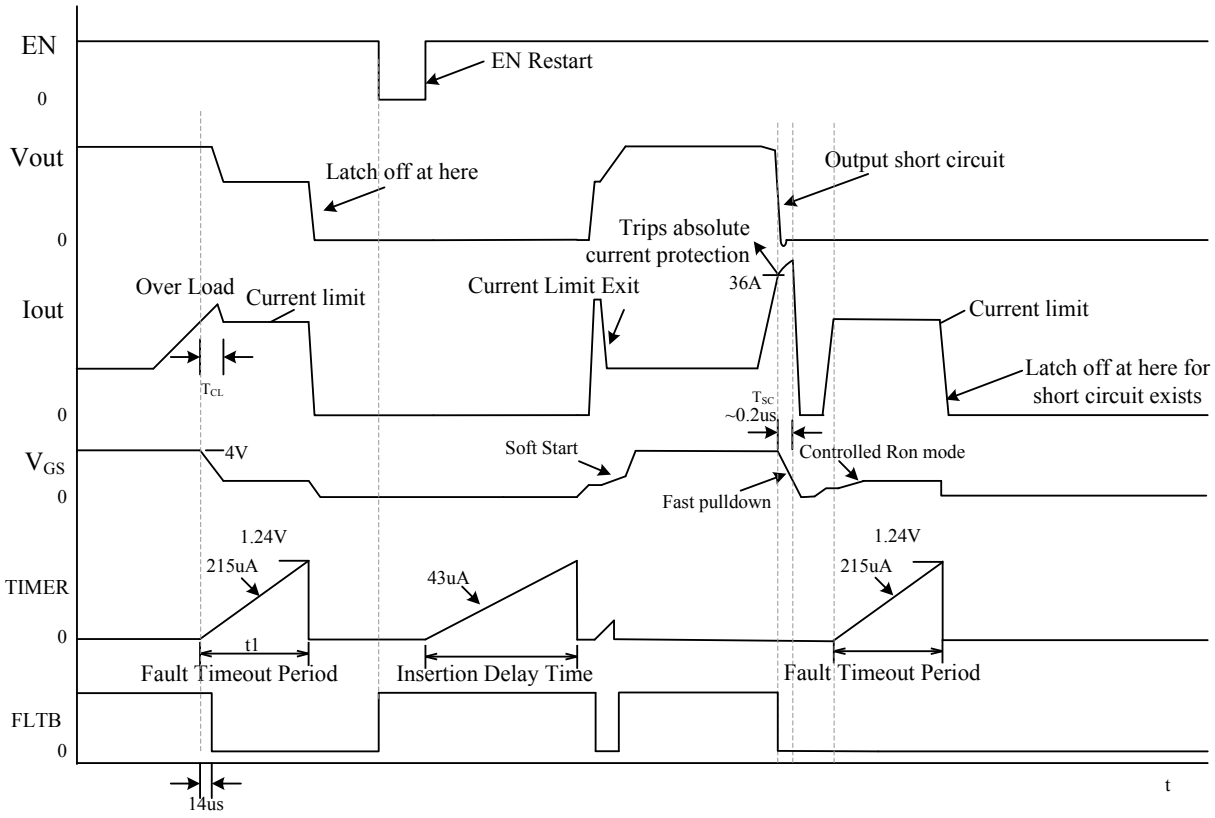


Figure 2: Over-Current Protection

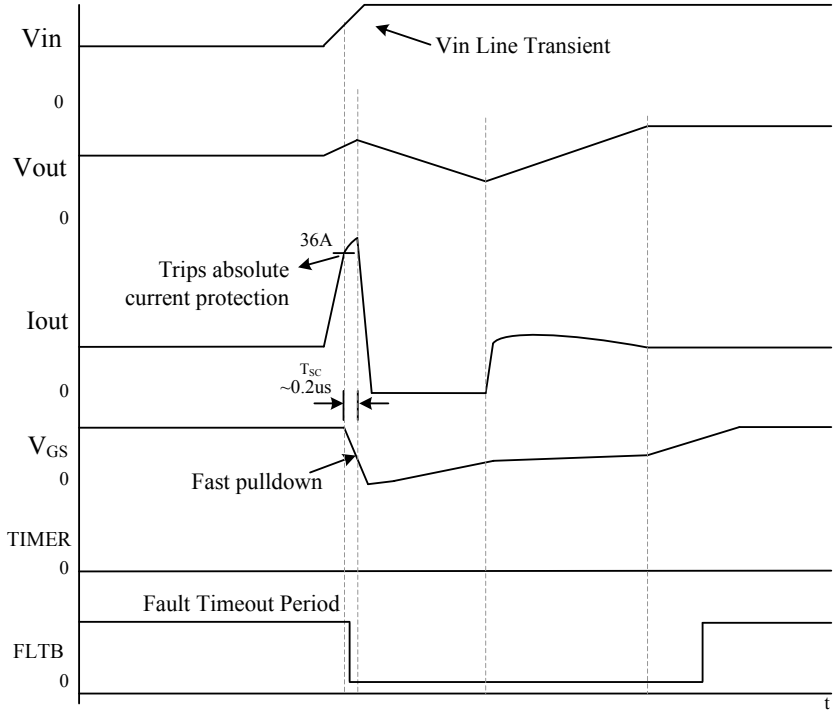


Figure 3: Vin line transient response

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

Power Good

The power good indicates whether the output voltage is in the normal range relative to the input voltage, and is the open drain of a FET. Pull up the PG pin to the external power supply through a 10k-100kΩ resistor. During power-up the power good output will be driven low. This indicates to the system to remain off and minimize the load on OUT to reduce in-rush current and power dissipation at start-up condition.

When the device reaches the following conditions:

A. V_{FB}>1.245V
B. V_{GS}>3V
C. V_{OUT}> V_{IN}-1V

The power good signal is pulled high. The system can now draw full power.

When the FB voltage drops below 1.16V, the power FET's V_{GS} voltage is less than a 3V or the output voltage is less than V_{IN}-1V, PG is switched low.

The PG output is pulled low when either the EN pin is below its threshold or the input UVLO/OVLO is triggered.

With no input, the power good stays at a logic low level in the presence of a pull-up supply.

FLTB Pin

The FLTB (fault bar) pin is an open drain output used to indicate that a fault has occurred. Pull up the FLTB pin to external power supply through 10k-100kΩ resistor.

When the device reaches its current limit, the die temperature exceeds the thermal shutdown threshold, or the MOSFET is shorted before power-up, the fault output is driven low with a 14μs propagation delay. If short circuit occurs and the 36A secondary current limit is reached, the FLTB will switch low immediately.

The FLTB goes high when the MP5022A resumes normal operation, which means the output voltage is higher than the setting voltage of the PG rising threshold and power FET is fully ON (V_{GS}>3V).

External Pull-up Voltage for PG and FLTB

The PG and FLTB need an external power supply. The open-drain output of PG can work well from the external pull-up voltage even when V_{IN}=0 and EN is disabled. Use a 10k-100kΩ pull-up resistor for PG and FLTB.

Power-Up Sequence

For hot-swap applications, the input of the MP5022A can experience a voltage spike or transient during the hot-plug procedure. This is caused by the parasitic inductance of the input trace and the input capacitor. An insertion delay determined by the external capacitor at the TIMER pin stabilizes the input voltage.

As per Figure 4 (EN floating), the input voltage rises immediately, and the internal V_{GS} voltage of power FET is pulled low by a 30Ω resistor.

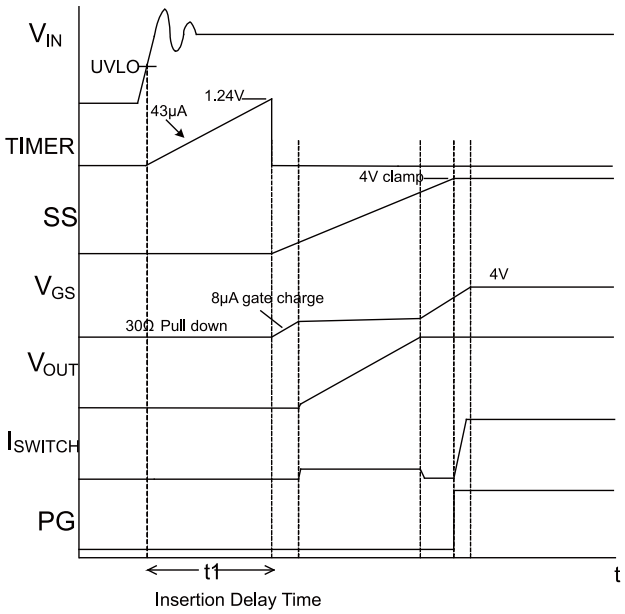


Figure 4: Start-Up Sequence

The TIMER pin charges through a 43μA constant current source when the input voltage reaches the UVLO threshold. When the TIMER pin voltage reaches 1.24V, an 8μA current source pulls up the power FET's gate-source voltage. Meanwhile, the TIMER pin voltage drops. Once the gate voltage reaches its threshold, V_{GSTH}, the output voltage rises. The rise time is determined by soft-start capacitor.

Soft-Start

A capacitor connected to the SS pin determines the soft-start time. When the insertion delay time ends, a constant current source that is proportional to input voltage ramps up the voltage on the SS pin. The output voltage rises at a similar slew rate to the SS voltage.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

The SS capacitor value is given by

$$C_{SS} = \frac{6 \cdot t_{SS}}{R_{SS}}$$

Where:

t_{SS}=soft start time

R_{SS}=1.1MΩ

For example, a 47nF capacitor gives a soft-start time of 8.6ms.

If the load capacitance is extremely large, the current required to maintain the preset soft-start time will exceed the current limit. In this case the rise time is controlled by the load capacitor and the current limit.

Float the SS pin to generate a fast ramp-up voltage. An 8μA current source pulls up the gate of the power FET. The gate charge current controls the output voltage rise time. The approximate soft start time is then 1ms and is the minimum soft-start time.

Enable and LOADEN

The EN and LOADEN pins are used to control ON/OFF of MP5022A.

During LOADEN blanking time, EN=1 alone is sufficient to turn on the switch.

After LOADEN blanking time is expired, both EN=1 and LOADEN=1 are required to turn on the switch.

At all times, EN=0 will turn off the switch. Recycle EN or VIN to restart the chip once it's latched off.

Note: LOADEN is used to shut down the power switch after LOADEN blanking time. But LOADEN can't turn on power switch by recycle LOADEN only.

Enable blanking time is over?	EN	LOADEN	Status
N	0	0	OFF
N	0	1	OFF
N	1	0	ON
N	1	1	ON
Y	0	0	OFF
Y	0	1	OFF
Y	1	0	OFF
Y	1	1	ON

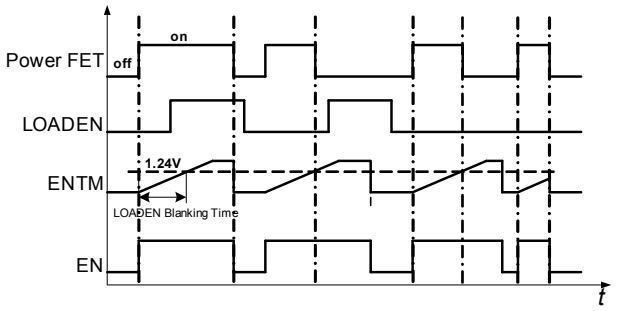


Figure 5: EN/LOADEN Timing Diagram

EN is pulled high internally with a 2μA internal pull-up current source.

Once the part is enabled, the insertion delay timer starts. When the insertion delay time ends, the internal 8μA current source charges the power FET's gate. Charging takes about 1ms for V_{GS} to reach its threshold. Then the output voltage rises following the SS controlled slew rate.

LOADEN Blanking Time

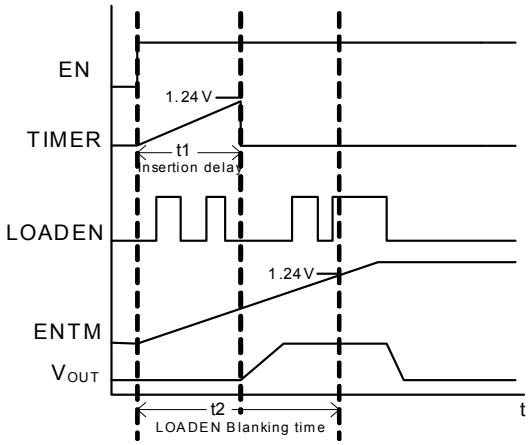


Figure 6: LOADEN Blanking Time

As shown in Figure 6, suppose EN is high. LOADEN has a programmable blanking time that prevents LOADEN from de-asserting during the blanking time. All fault functionality is operative during the start-up so that the power switch shuts down if a fault was detected; however, LOADEN going low during this blanking time won't turn off the switch. At the end of blanking time, LOADEN behaves as normal.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

The blanking time can be set by a capacitor connected to the ENTM pin. The blanking timer capacitor is given by:

$$C_{ENTM} = \frac{t_{LDNB} \cdot 10^{-6}}{1.24}$$

Where:

t_{LDNB}=LOADEN blanking time

C_{ENTM}=LOADEN blanking time capacitor on ENTM pin.

For example, a 1μF capacitor gives a blanking time of 1.24s.

Floating the ENTM pin generates a fast ramp-up voltage on the ENTM pin. The blanking time during this period is negligible.

Damaged MOSFET Detection

The MP5022A can detect a shorted pass FET during power up by treating an output voltage that exceeds V_{IN}-1V during power-up as a short on the MOSFET. The FLTB pin goes low to indicate a fault condition and the power switch is held off. Once the $V_{OUT} \leq V_{IN}$-1, the part starts up normally.

Internal VCC SUB-Regulator

The MP5022A has an internal 4V linear sub-regulator that steps down the input voltage to generate a 4V power supply that powers low-voltage circuitry. The regulator is enabled when V_{IN} exceeds its UVLO threshold and EN is high.

PD Pin

When the PD pin connects to output, the part is in pull-down mode. Output voltage is discharged much quicker than not connect PD to output when EN shutdown the part. Adding a more than 100ohm resistor between the PD pin and the output results in a slower output drop. If PD pin is floating, pull-down mode is disabled.

Under/Over Voltage Lock Out

If the supply (input) falls below the UVLO threshold or above the OVLO threshold, the output is disabled and the PG pin goes low.

When the supply goes exceeds the UVLO threshold without exceeding the OVLO threshold, the output is enabled and the PG line is released.

Monitoring Output Current

The IMON pin provides a current proportional to the output current (the current through the power device). The gain of the current sense amplifier is 10μA from IMON for 1A of MOSFET current. Placing 10k resistor to ground creates a 0V to 2V voltage when MOSFET current ranges from 0A to 20A. The voltage compliance for IMON pin is from 0V to 3V. Place a more than 10nF capacitor paralleled R_{MON} in application.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

APPLICATION INFORMATION

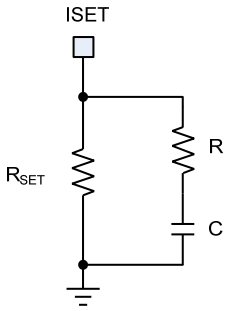
The Current Limit Set (R_{SET})

The MP5022A Current Limit value should be higher than the normal maximum load current, allowing the tolerances in the current sense value. The current limit can be set by the below equation:

$$I_{LIMIT} = \frac{1.3(V)}{R_{SET}} \times 10^5 (A)$$

We can get the theory result through above equation.

When current limit is setting lower than 7A, a RC circuit is necessary to parallel with ISET resistor as shown in below figure. Generally, choose R=20kΩ, C=560pF.



Below table gives the bench results on our evaluation board.

Current Limit vs. Current Limit Resistor

Current Limit Resistor (kΩ)	6.8	16.2	32.4
Current Limit (A)	19	8	4.06

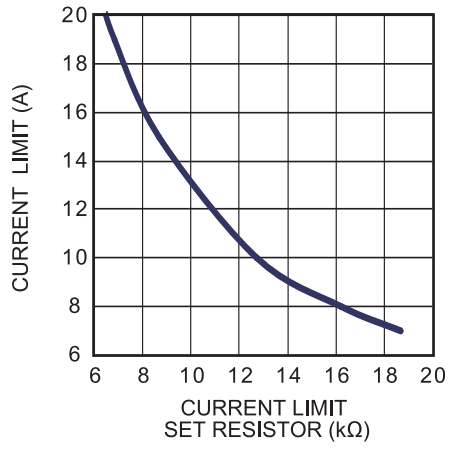


Figure 7: Current Limit vs. R_{SET} Value (Current Limit ≥ 7A)

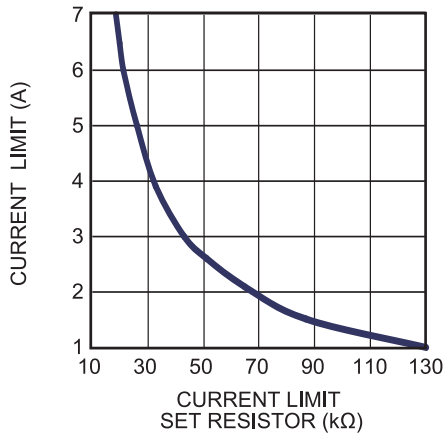


Figure 8: Current Limit vs. R_{SET} Value (Current Limit < 7A)

Current Monitor Set

MP5022A provide the function of monitoring the power MOSFET current. The users can get the useful data by utilize it. Users should place a resistor (R_{MON}) to ground to set the gain of the output. The theory equation is:

$$I_{MON} = \frac{I_{POWER_FET}}{10^5} (A)$$

The I_{POWER_FET} is the current flowing from power MOSFET. Placing 10kohm from IMON pin to GND can get 100mV per Amp. Place a more than 10nF capacitor from IMON to GND to smooth the indicator voltage.

PCB Layout Guide

The following guidelines should be followed when designing the PC board for the MP5022A:

1. The high current path from the board's input to output, and the return path, should be parallel and close to each other to minimize loop inductance.
2. Connect MP5022A GND pin and signal GND together at first, and then Kelvin connect to its PGND or internal GND layers.
3. Input decoupling capacitors on VIN pin should have minimal trace length to the VIN pins and to GND.
4. Place a transient voltage suppressor diode (TVS) to the VIN, the TVS can absorb the input voltage spike when load current decreased sharply.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

5. Place the schottky diode close to the OUT pin and GND to absorb negative voltage spike when the power FET is shut off
6. Place output capacitors as close to the part as possible to minimize the effect of PCB parasitic inductance.
7. Keep the IN and GND pads connected with large copper and place vias in the thermal pad to get better thermal performance.
8. Make sure all VIN and VOUT pins are connected to get equal current distribution to each lead.

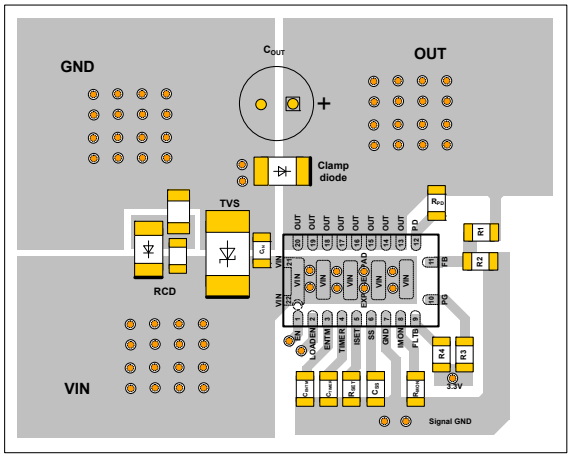


Figure 9: PCB Layout

Design Example

The detailed application schematic is shown in Figure 10, Figure 11 and Figure 12. Figure 10 shows the application circuit with optional RCD clamping circuit which prevent the input voltage lower than UVLO when output short-circuit happens (current limit ≥ 7A). Figure 11 is the application circuit with optional RCD clamping circuit (current limit < 7A). Figure 12 is the application circuit with Loaden unused. The typical performance and waveforms have been shown in the Typical Performance Characteristics section. For more detail device applications, please refer to the related Evaluation Board Datasheet of MP5022A.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL APPLICATION

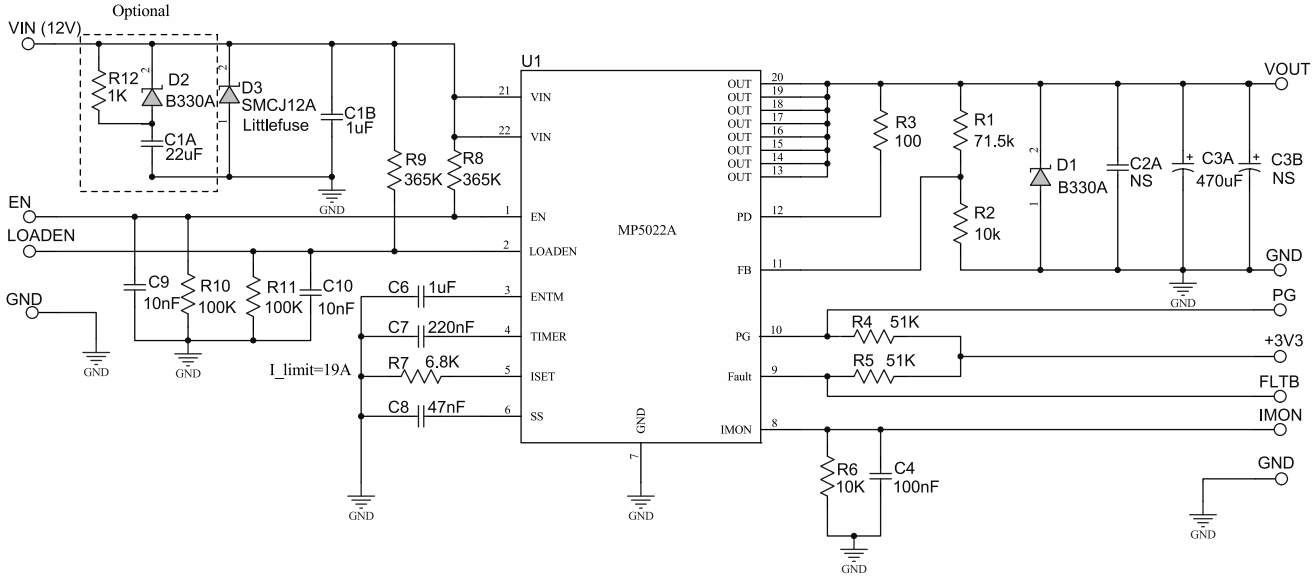


Figure 10: Typical Application Circuit with optional RCD clamping circuit (Current Limit ≥ 7A)

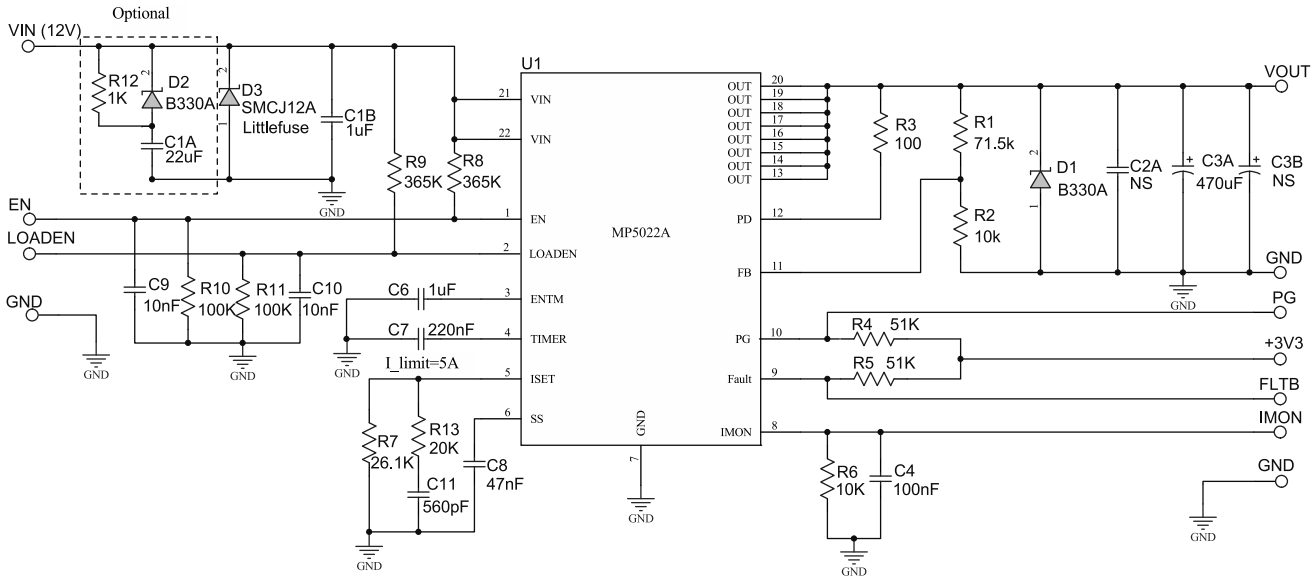


Figure 11: Typical Application Circuit with optional RCD clamping circuit (Current Limit < 7A)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

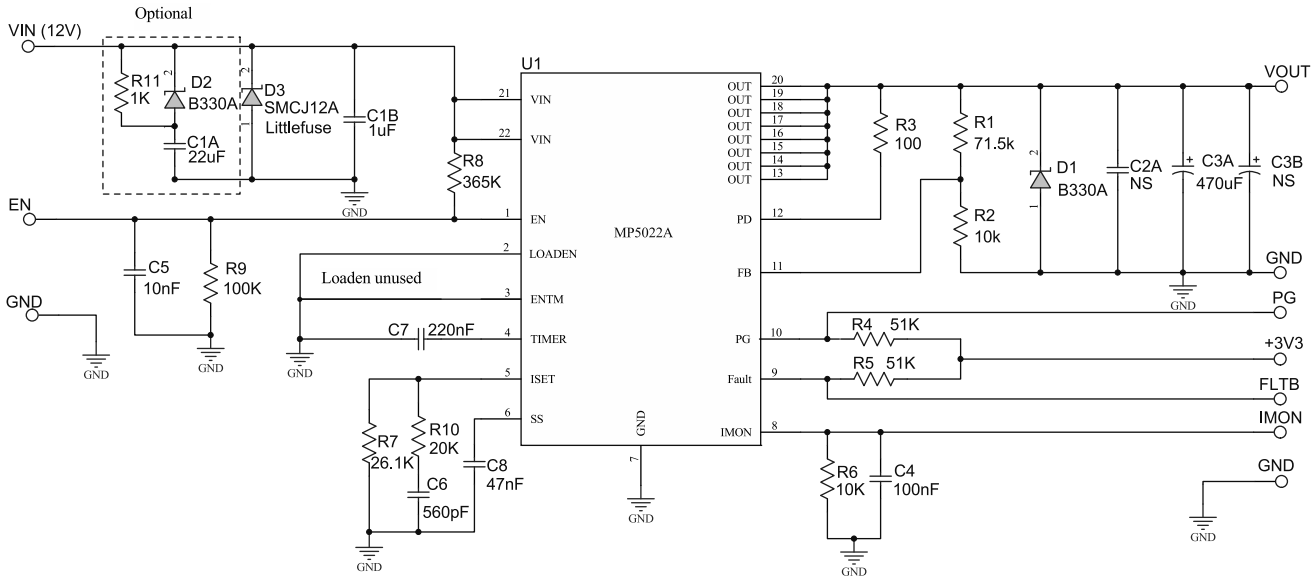
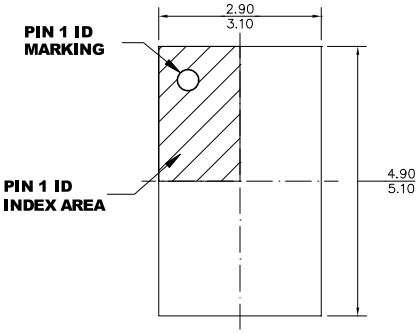


Figure 12: Typical Application Circuit with optional RCD clamping circuit (Loaden is not used)

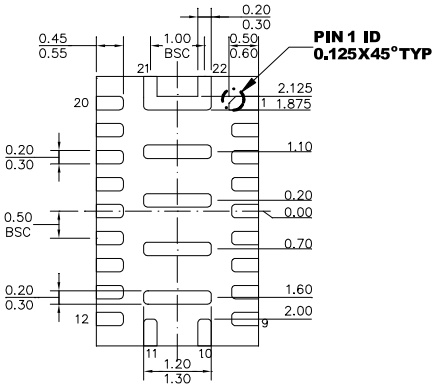
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE INFORMATION

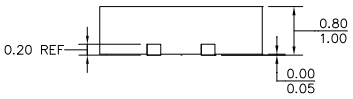
QFN-22 (3mmx5mm)



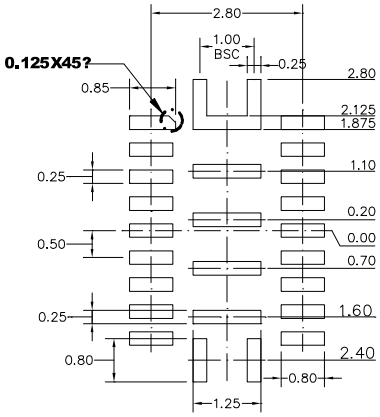
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.