The Future of Analog IC Technology

MP5021B

16V, 7mΩ R_{DS_ON} Hot-Swap Protection Device with Current Monitoring

DESCRIPTION

The MP5021B is a hot-swap protection device designed to protect circuitry on its output from transients on its input. Also, it protects its input from undesired shorts and transients coming from its output.

At start-up, the slew rate at the output limits the inrush current. An external capacitor at SS controls the slew rate.

The maximum output load is current limited using a sense FET topology where a low-power resistor from ISET to ground controls the magnitude of the current limit.

An internal charge pump drives the gate of the power device, allowing a power FET with a very low on resistance of 7mΩ.

The MP5021B includes an IMON option to produce a voltage proportional to the current through the power device, as set by a resistor from IMON to ground.

The MP5021B includes an optional discharge function that provides a discharge path for the external output capacitor when the part is disabled. Fault protections include current-limit protection, thermal shutdown, and damaged MOSFET detection. Both the current limit and thermal shutdown have user-settable auto-retry and latch-off mode. Also, the device features over-voltage protection (OVP) and under-voltage protection (UVP).

The MP5021B is available in a 3mm x 5mm QFN package.

FEATURES

- 4.8V to 16V Operating Input Range
- Integrated 7mΩ Power FET
- Adjustable Current Limit
- Output Current Measurement
- ±5% Current Monitor Accuracy
- Fast Response (<200ns) for Short Protection
- PG Detector and FLTB Indication
- PG Assert Low at VIN = 0
- Damaged MOSFET Detection
- External Soft-Start
- Programmable EN Blanking Time
- Under/Over-Voltage Lockout
- Thermal Protection
- Small QFN-22 (3mmx5mm) Package

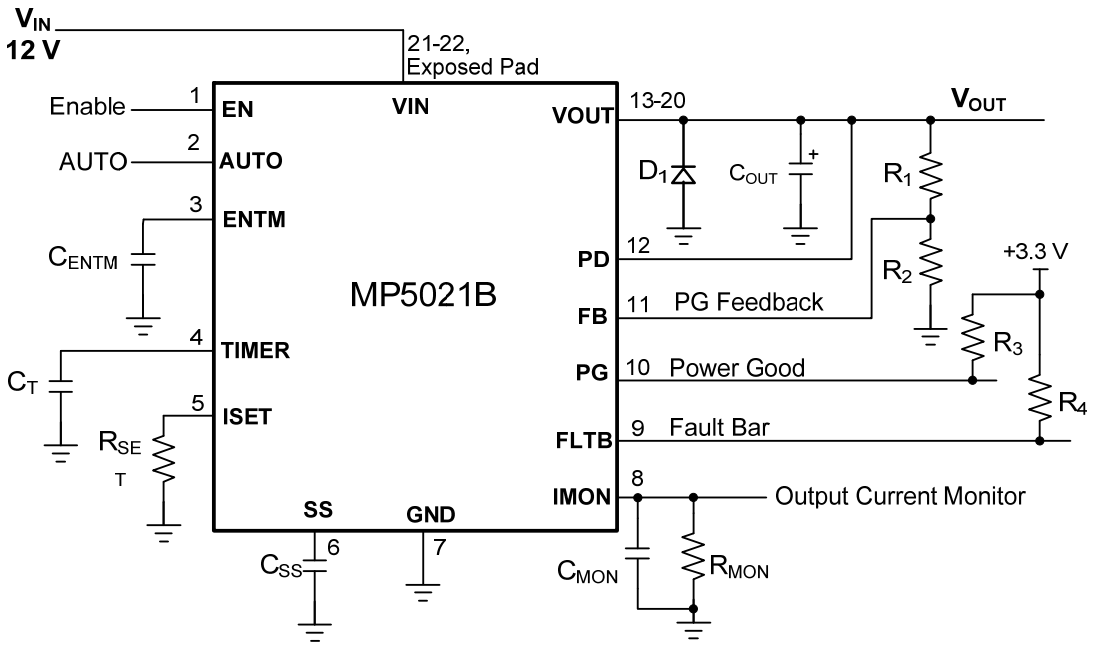
APPLICATIONS

- Hot Swappable
- PC Cards
- Disk Drives
- Laptops

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5021BGQV	QFN-22 (3mm×5mm)	*See Below*

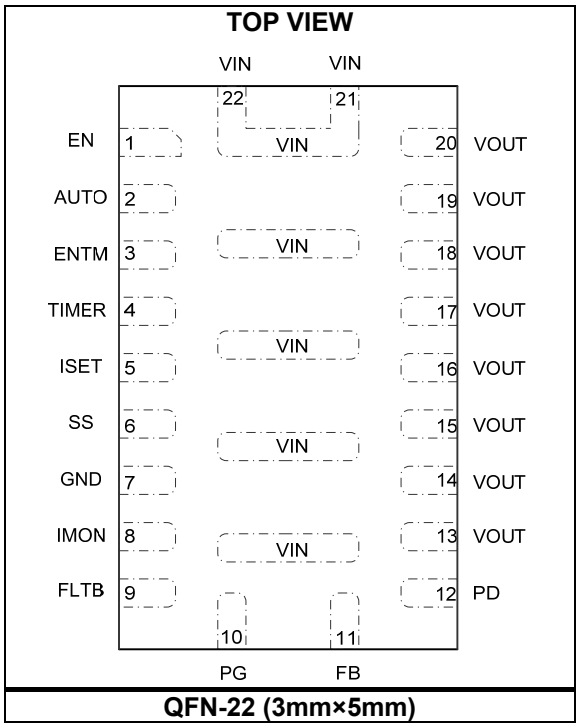
For Tape & Reel, add suffix –Z (e.g. MP5021BGQV–Z)

TOP MARKING

MPYW
5021
BLLL

MP: MPS prefix
Y: Year code
W: Week code
5021B: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-22 (3mm×5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

VIN ..... -0.3V to 36V
VOUT, PD ..... -0.3V to 20V
Other pins..... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2)
..... 2.7W
Storage temperature.....-65°C to +155°C
Operating temperature.....-40°C to +150°C

Recommended Operating Conditions(3)

Input voltage operating range..... 4.8V to 16V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-22 (3mm×5mm).....46 ..... 10... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, C_{OUT} = 470µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current						
Quiescent current	I_Q	EN = high, no load		1.1	2.0	mA
		Fault latch off		0.8		mA
		EN = 0, V_{IN} = 16V			170	µA
Power FET						
On resistance	R_{DSon}	T_J = 25°C		7	8.5	mΩ
		T_J = 85°C(5)		9		
Off-state leakage current	I_{OFF}	V_{IN} = 36V, EN = 0V			1	µA
Maximum Current Limit(5)	I_{LIMIT_MAX}	V_{IN} ≥ 8V			10	A
		V_{IN} = 5V			5	A
Thermal shutdown						
Shutdown temperature(5)	τ_{STD}			135		°C
Hysteresis	τ_{HYS}	Auto-retry mode only		15		°C
Under/over voltage protection						
Under-voltage lockout threshold	V_{UVLO}	UVLO, rising threshold	3.63	4.04	4.45	V
UVLO hysteresis	$V_{UVLOHYS}$			250		mV
Over-voltage lockout threshold	V_{OVLO}	OVLO, rising threshold	16.5	17.66	18.96	V
OVLO hysteresis	$V_{OVLOHYS}$			460		mV
AUTO						
Low-level input voltage	V_{AUTOL}	Latch-off mode			1	V
High-level input voltage	V_{AUTOH}	Auto-retry mode	2.5			V
Soft start						
SS pull-up current	I_{SS}	I_{SS} changes with input	10	12.5	15	µA
Current limit						
Current limit at normal operation	I_{Limit_NO}	R_{SET} = 4.99k	5.67	6.30	6.93	A
Current limit response time(5)	τ_{CL}	I_{Limit} = 3A, add 3Ω load		20		µs
Secondary current limit	I_{LimitH}	Regardless of R_{SET}		25		A
Short-circuit protection response time (5)	τ_{SC}			200		ns
Output current monitor						
Gain of current sense amplifier	A_{IMON}	1.5A < I_{OUT} < 6A	38	40	42	µA/A
Max voltage of IMON	V_{IMON_MAX}				3	V
Timer						
Upper threshold voltage	V_{TMRH}		1.187	1.23	1.273	V
Lower threshold voltage	V_{TMRL}	Over-current restart cycles		0.20		V
Insertion delay charge current	I_{INSERT}			38.5		µA
Fault detection charge current	I_{FLTD}			200		µA
Fault re-start sink current	I_{FLTS}	Auto-retry mode only		0.5		µA
Fault re-start duty cycle	D_{FAULT}	Auto-retry mode only		0.25		%
Discharge R_{ON}	R_{FLTE}	I_{OUT} < I_{Limit}		35		Ω
EN Blanking timer (ENTM)						
Upper threshold voltage	V_{ENTMRH}		1.187	1.23	1.273	V
Charge current	I_{ENTMCC}			0.85		µA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12 V, C_{OUT}= 470 µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable						
Rising threshold	V_{ENRS}		1.5	2	2.3	V
Hysteresis	V_{ENHYS}			200		mV
FB (power good feedback)						
Feedback voltage	V_{FBH}		0.621	0.667	0.713	V
Fault bar/power good						
Low-level output voltage	V_{OL}	Sink current 1mA			0.3	V
Off-state leakage current	I_{FLT_LKG}	V_{FLTB} = 5V			1	µA
Fault bar propagation delay	τ_{PDE}			21		µs
Power good rising threshold	PG_{Vth_HI}			90%		V_{FBH}
Power good falling threshold	PG_{Vth_LO}			75%		V_{FBH}
Power good off-State Leakage current	I_{PG_LKG}	V_{PG} = 3.3V			2.5	µA
PG low-level output voltage	V_{OL_100}	V_{IN} = 0V, Pull up to 3.3V through 100kΩ resistor		580	700	mV
	V_{OL_10}	V_{IN} = 0 V, Pull up to 3.3V through 10kΩ resistor		700	750	mV

NOTE:

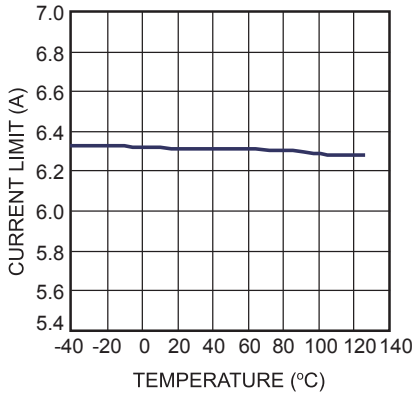
5) Guaranteed by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

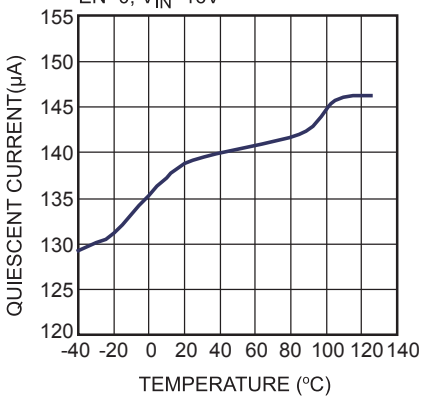
V_{IN} = 12V, C_{OUT} = 470µF, C_{ENTM} = 1µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 4.99kΩ, T_A = +25°C, unless otherwise noted.

Current Limit vs. Temperature



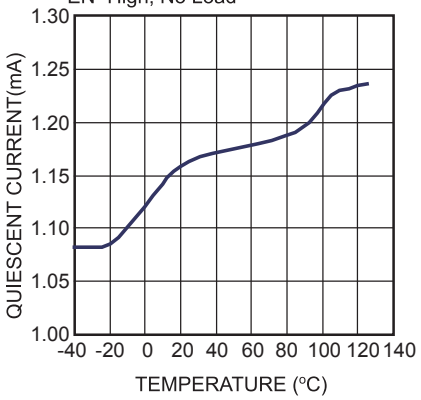
Quiescent Current vs. Temperature

EN=0, V_{IN}=16V

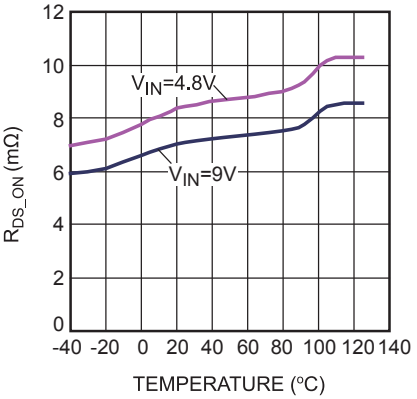


Quiescent Current vs. Temperature

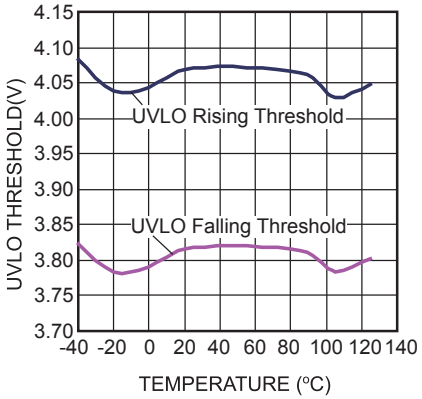
EN=High, No Load



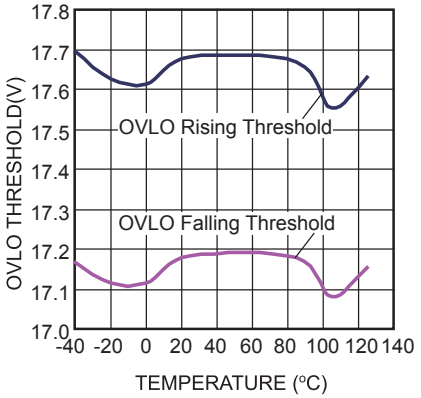
R_{DS_ON} vs. Temperature



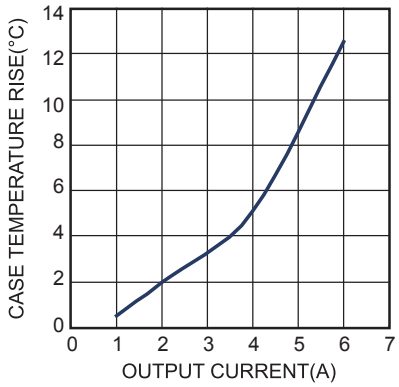
UVLO Threshold vs. Temperature



OVLO Threshold vs. Temperature



Case Temperature Rise vs. Output Current

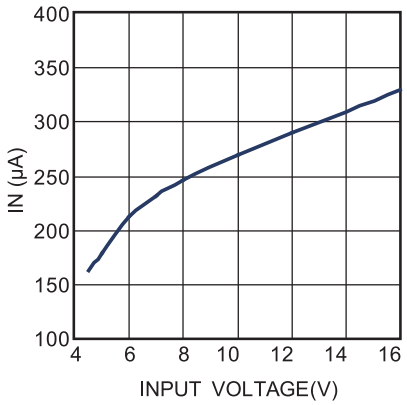


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

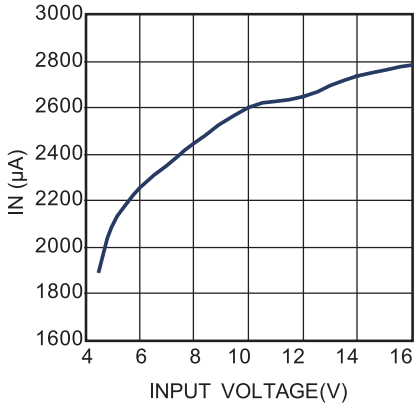
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, C_{OUT} = 470µF, C_{ENTM} = 1µF, C_T = 220nF, C_{SS} = 47nF, T_A = +25°C, unless otherwise noted.

Disable Supply Current vs. Input Voltage

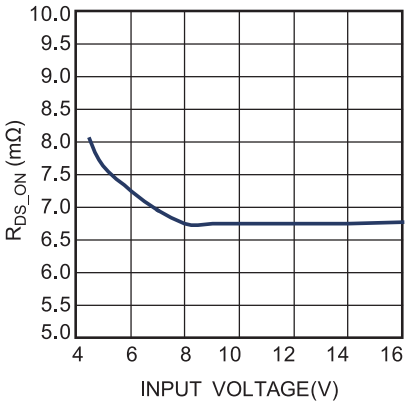


Enable Supply Current vs. Input Voltage

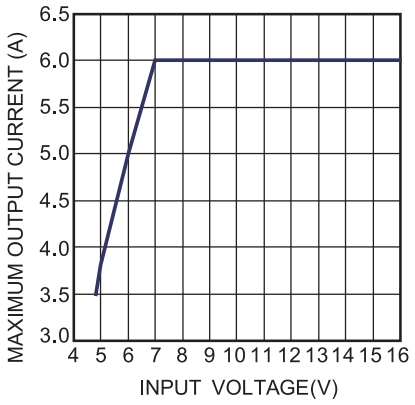


R_{DSON} vs. Input Voltage

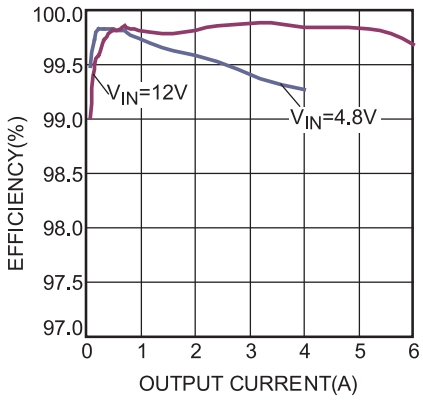
V_{IN}=12V, I_{OUT}=1A



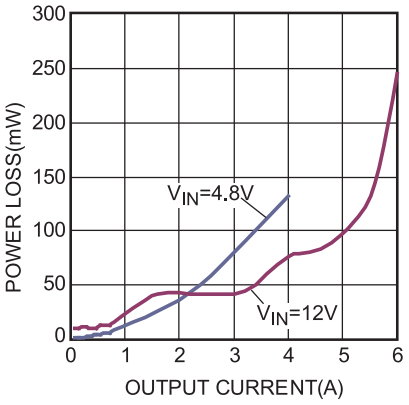
Maximum Continuous Current vs. Input Voltage



Efficiency vs. Load Current



Power Loss vs. Load Current

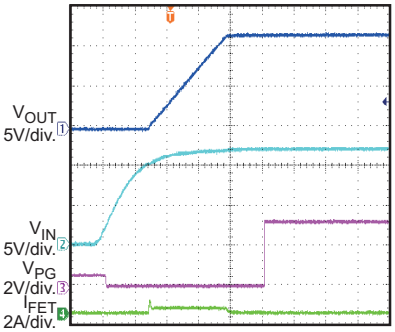


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

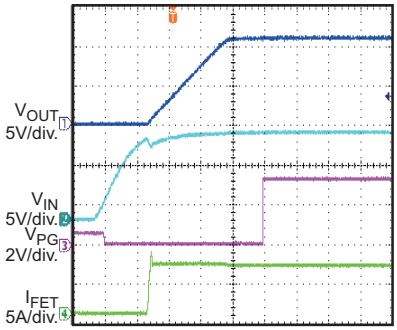
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, C_{OUT} = 470µF, C_{ENTM} = 1µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 3.16kΩ, T_A = +25°C, unless otherwise noted.

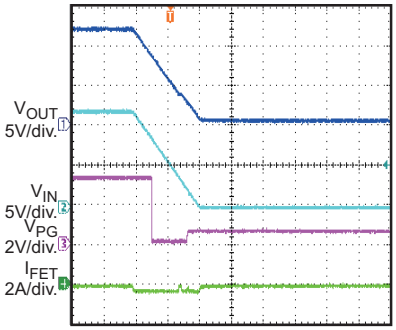
Start-Up through V_{IN}
I_{OUT} = 0A



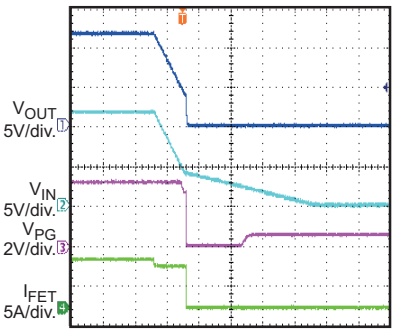
Start-Up through V_{IN}
I_{OUT} = 6A



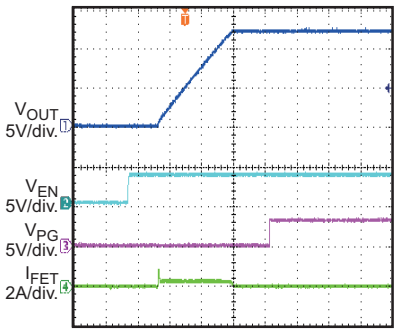
Shutdown through V_{IN}
I_{OUT} = 0A



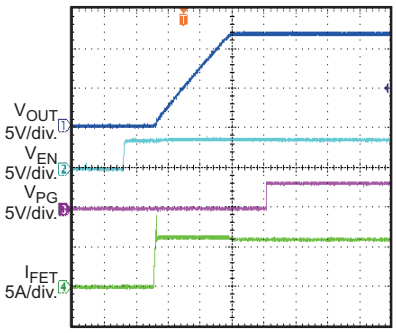
Shutdown through V_{IN}
I_{OUT} = 6A



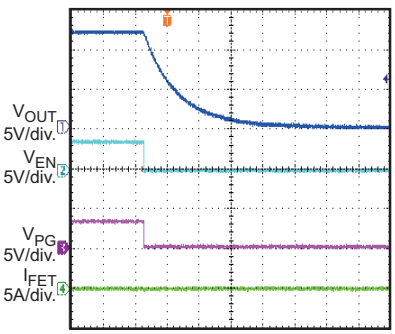
Start-Up through EN
I_{OUT} = 0A



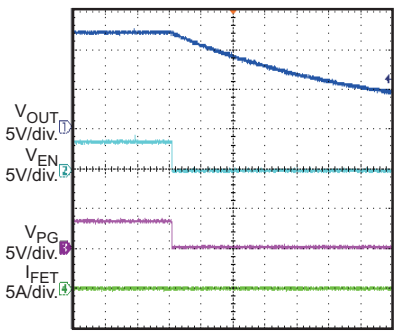
Start-Up through EN
I_{OUT} = 6A



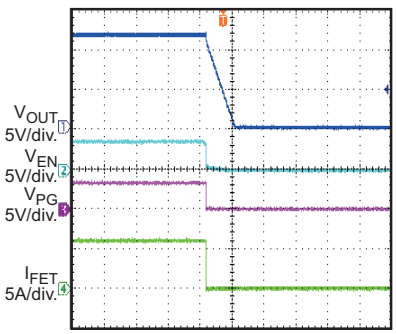
Shutdown through EN
I_{OUT} = 0A, with PD



Shutdown through EN
I_{OUT} = 0A, without PD



Shutdown through EN
I_{OUT} = 6A, with PD

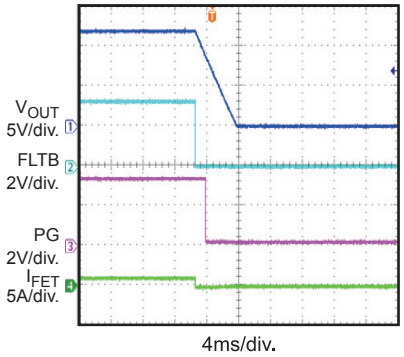


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

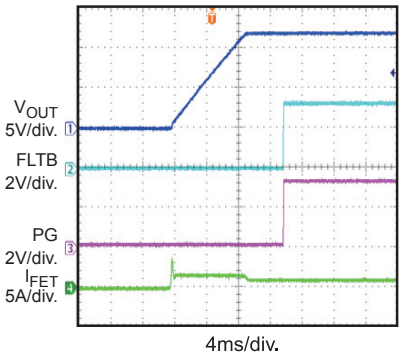
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, C_{OUT} = 470µF, C_{ENTM} = 1µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 3.16kΩ, T_A = +25°C, unless otherwise noted.

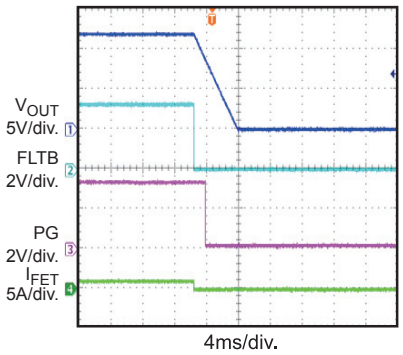
Thermal Shutdown
I_{OUT}=2A, Latch Mode



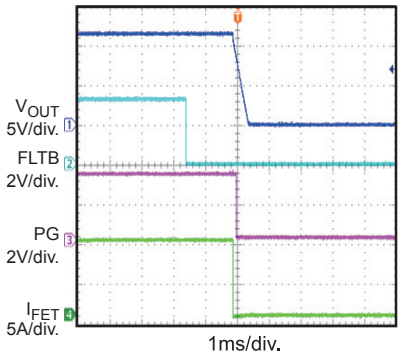
Thermal Recovery
I_{OUT}=2A, Retry Mode



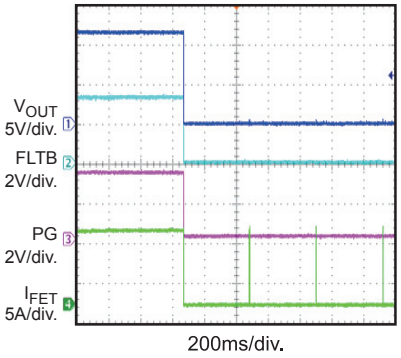
Thermal Shutdown
I_{OUT}=2A, Retry Mode



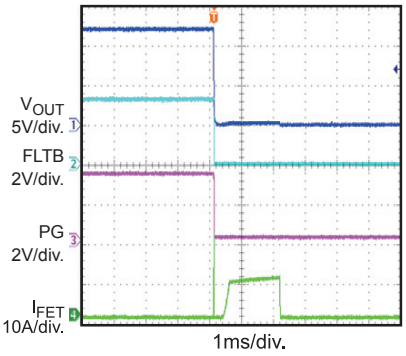
OCP
Latch Mode



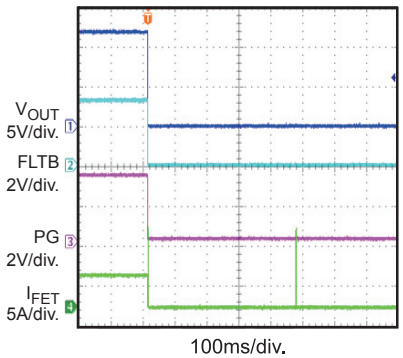
OCP
Retry Mode



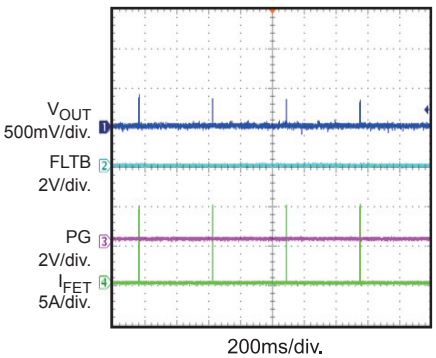
SCP Entry
Latch Mode



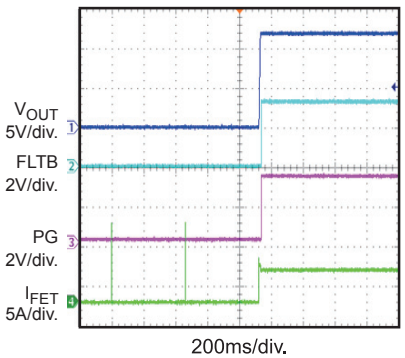
SCP Entry
Retry Mode



SCP Steady State
Retry Mode



SCP Recovery
Retry Mode

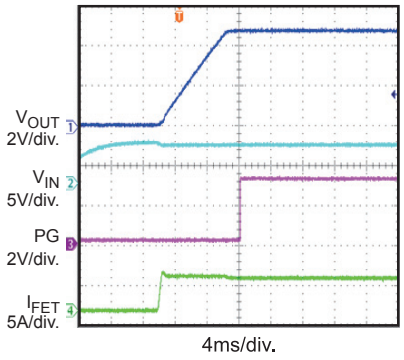


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

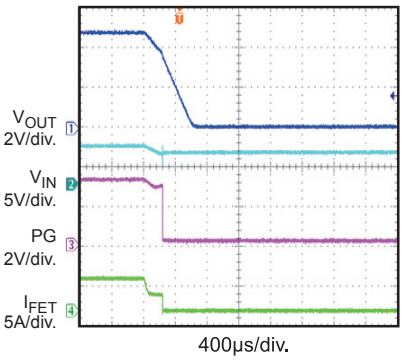
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, C_{OUT} = 470µF, C_{ENTM} = 1µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 6.04kΩ, T_A = +25°C, unless otherwise noted.

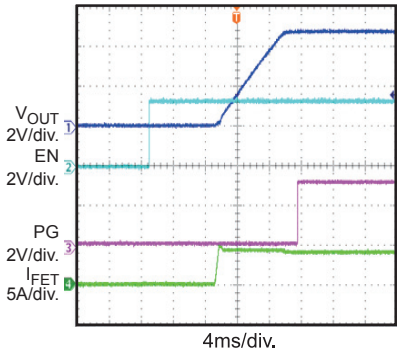
Start-Up through V_{IN}
I_{OUT}=3.8A



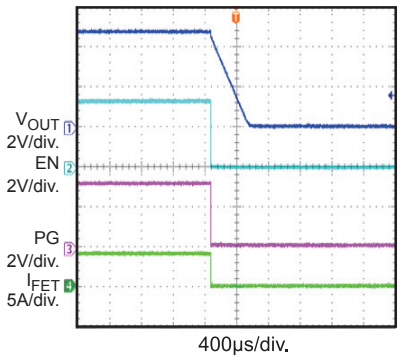
Shutdown through V_{IN}
I_{OUT}=3.8A



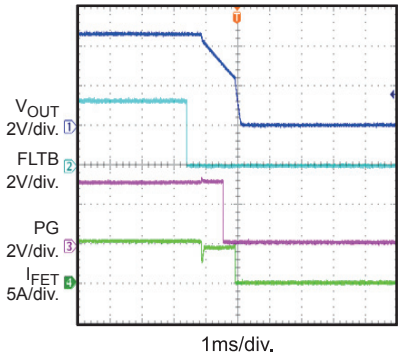
Start-Up through EN
I_{OUT}=3.8A



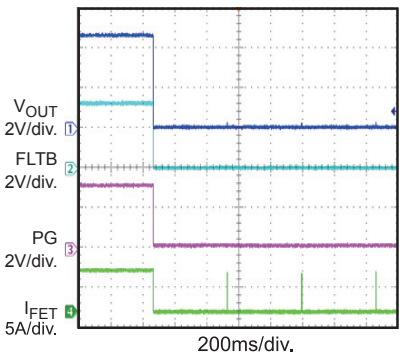
Shutdown through EN
I_{OUT}=3.8A, with PD



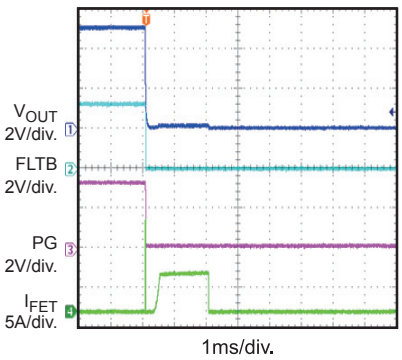
OCP
Latch Mode



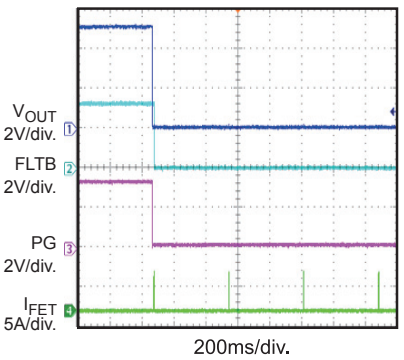
OCP
Retry Mode



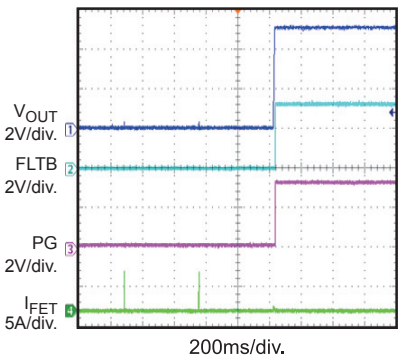
SCP Entry
Latch Mode



SCP Entry
Retry Mode



SCP Recovery
Retry Mode



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable input.** Pull EN below the threshold to shut down the chip. Pull EN above the threshold (or leave it floating) to enable the chip.
2	AUTO	**Auto reset enable.** Float AUTO to enable the auto reset once the fault is removed. Pull to ground to latch off when a fault occurs.
3	ENTM	**Enable blanking time set.** Connect an external capacitor to set the EN blanking time. Once EN is active, the timer starts, and the EN de-assertion is blanked. The switch shuts down in the presence of a fault. However, EN low during blanking has no effect. Leave it floating if disable Enable blanking time.
4	TIMER	**Timer set.** An external capacitor sets the fault timeout period, the re-start time, and the hot-plug-insertion time delay.
5	ISET	**Current limit set**. Place a resistor to ground to set the value of the current limit.
6	SS	**Soft start**. Connect an external capacitor to set the soft-start time of the output voltage. The internal circuit controls the slew rate of the output voltage at turn-on. Float SS to set the soft-start time (minimum of 1 ms).
7	GND	**Ground**.
8	IMON	**Output current monitor.** IMON provides a voltage proportional to the current flowing through the power device. Place a 10 kΩ resistor (R_{MON}) to ground to create a 0 V to 1.6 V voltage when the current ranges from 0 A to 4 A. Place a 100 nF capacitor in parallel with R_{MON}. Connect to GND is not used this pin.
9	FLTB	**Fault bar.** FLTB is an open-drain output that drives to ground when an over-current or a thermal shutdown occurs. Pull up to an external power supply through a 10 kΩ-100 kΩ resistor. Leave it floating if not used this pin.
10	PG	**Power good.** PG is an open-drain output. Pull up to an external power supply through a 10 kΩ-100 kΩ resistor. High = power good. Low indicates the output is outside the UVLO/OVLO window. PG begins to work when the pull-up supply is enabled, even if VIN and EN are still disabled. Leave it floating if not used this pin.
11	FB	**Feedback**. An external resistor divider from the output sets the output voltage where PG switches. The rising threshold is 90%*V_{FBH}; the falling threshold is 75%*V_{FBH}. Connect to GND if not used PG function.
12	PD	**Output discharge.** Connect to the output to provide a 500 Ω load to discharge the output when the part is disabled. No connection disables this function.
13-20	VOUT	**Output voltage controlled by the IC.** Place a Schottky diode between VOUT and GND to absorb the negative voltage spike.
21-22, Exposed Pads	VIN	**Input power supply.** Add a RCD clamping circuit close to VIN when the input capacitor is below 10uF. Please refer to Figure 9 in “TYPICAL APPLICATION” part. It is used to hold the line voltage when output short circuit happens.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

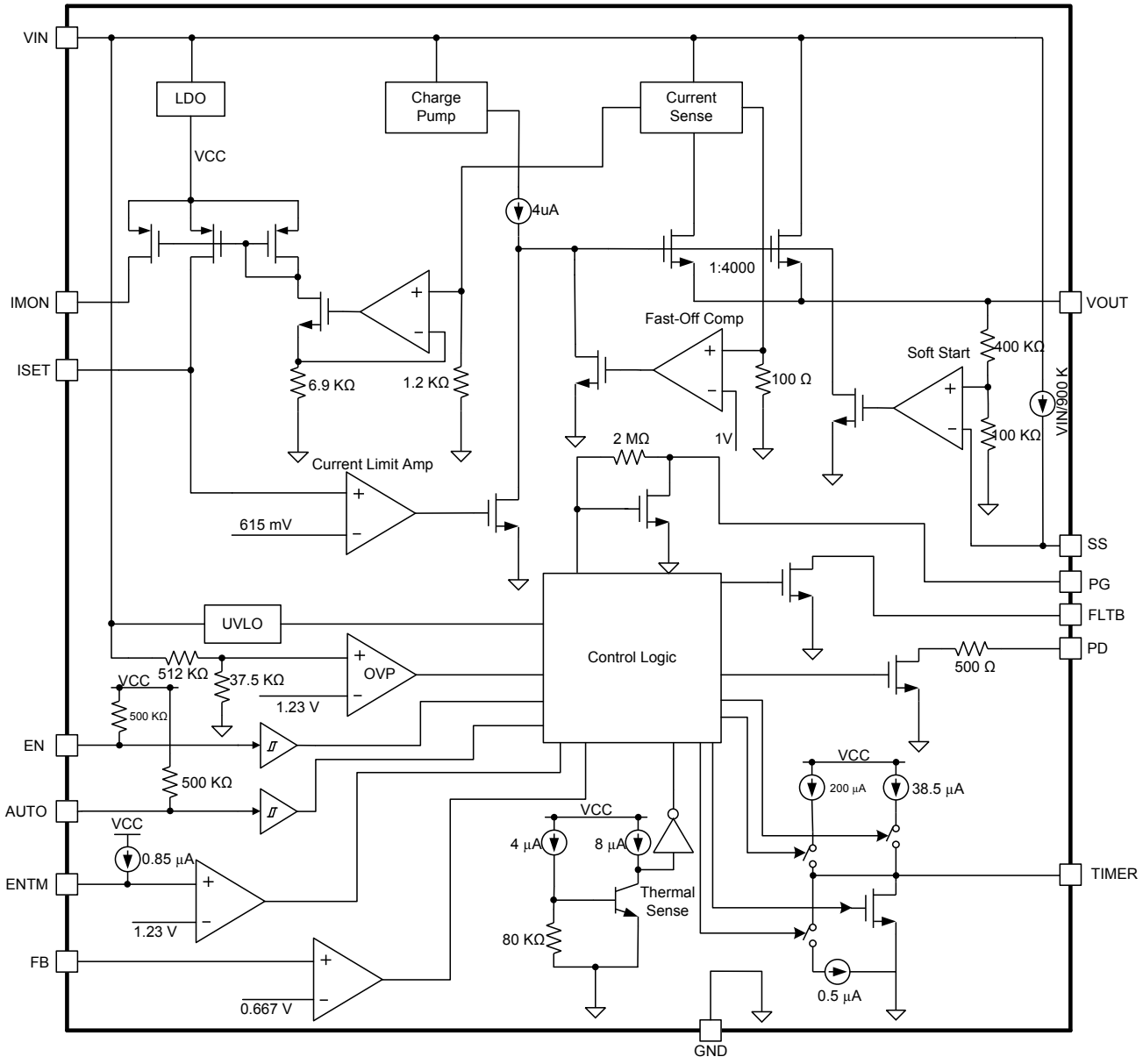


Figure 1—Functional block diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

OPERATION

The MP5021B limits the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop and the dv/dt of the voltage to the load. It provides an integrated solution to monitor the input voltage, output voltage, output current, and die temperature to eliminate the need for an external current-sense power resistor, power MOSFET, and thermal sense device.

Current Limit

The MP5021B provides a constant current limit that can be programmed by an external resistor. Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant. In order to limit the current, the gate to the source voltage must drop from 5V to around 1V. The typical response time is about 20μs. The output current may have a small overshoot during this time period.

When the current limit triggers, the fault timer starts. If the output current falls below the current limit threshold before the end of the fault timeout period, the MP5021B resumes normal operation. Otherwise, if the current limit duration exceeds the fault timeout period, the power FET turns off. The subsequent behavior relates to AUTO configuration. If the temperature reaches the thermal protection threshold during the fault timeout period, the power FET turns off.

When AUTO is floating, the part functions in auto-retry mode for over-current protection. The part enters latch-off mode when AUTO pulls to ground (once it detects an over-current condition) and the duration exceeds the pre-set value.

When the device reaches either its current limit or its over-temperature threshold, FLTB is driven low with a 21μs propagation delay to indicate a fault. The desired current limit at normal operation is a function of the external current-limit resistor.

Short-Circuit Protection

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold significantly before the control loop can respond. If the current reaches a 25A secondary current limit level, a fast turn-off circuit activates to turn off the power FET using a 100mA pull-down gate discharge current. This limits the peak current through the switch to limit the input voltage drop. The total short-circuit response time is about 200ns. When the chip triggers a short-circuit protection, it restarts again to check if the over-load condition exists or not. If a short circuit is induced by the input line transient, the part operates normally. If a real short circuit occurs, the part latches off or triggers auto retry, depending on the AUTO connection. For additional details see Figure 2, Figure 3 and Figure 4.

FLTB switches low once it reaches a 25A current limit, and it asserts low until the circuit resumes normal operation.

Fault Timer & Restart

When the current reaches its over-current limit threshold, a 200μA fault timer current source charges the external capacitor (C_T) at TIMER. If the current limit state ends before TIMER reaches 1.23V, the MP5021B returns to normal operation mode, and a low-value resistor discharges C_T after the TIMER voltage reaches 1.23V. If the current limit state continues after the TIMER voltage reaches 1.23V, the power FET switches off.

The capacitance of C_T can be determined with Equation (1):

$$C_T = \frac{200 \cdot \tau_{fault}}{1.23} \quad (1)$$

Where:

C_T = Fault timer capacitance in nF

τ_{fault} = Fault timer in ms

For example, a 100nF capacitor yields a fault timer of 0.615ms.

The subsequent re-start procedure then depends on the selected retry configuration.

If AUTO connects to ground or is low, the MP5021B will latch off. Re-start the input power or cycle the EN signal to resume operation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

Floating AUTO causes the device to work in hiccup mode (see Figure 3). At the end of the fault timeout period, the power switch turns off, and a low current sink of 0.5μA discharges the external capacitor C_T.

When the TIMER voltage reaches the low threshold (0.2V), the part re-starts. If the fault condition remains, the fault timeout period and re-start timer repeat.

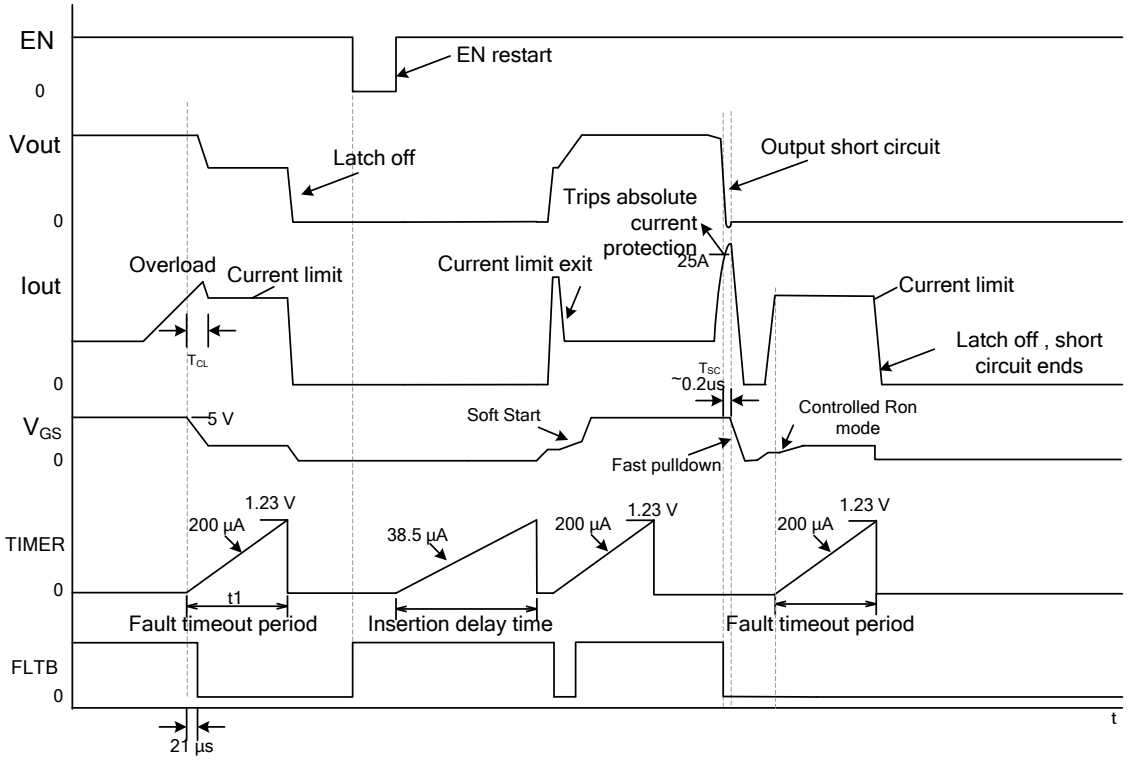


Figure 2—Over-current protection (latch-off Mode, AUTO = low)

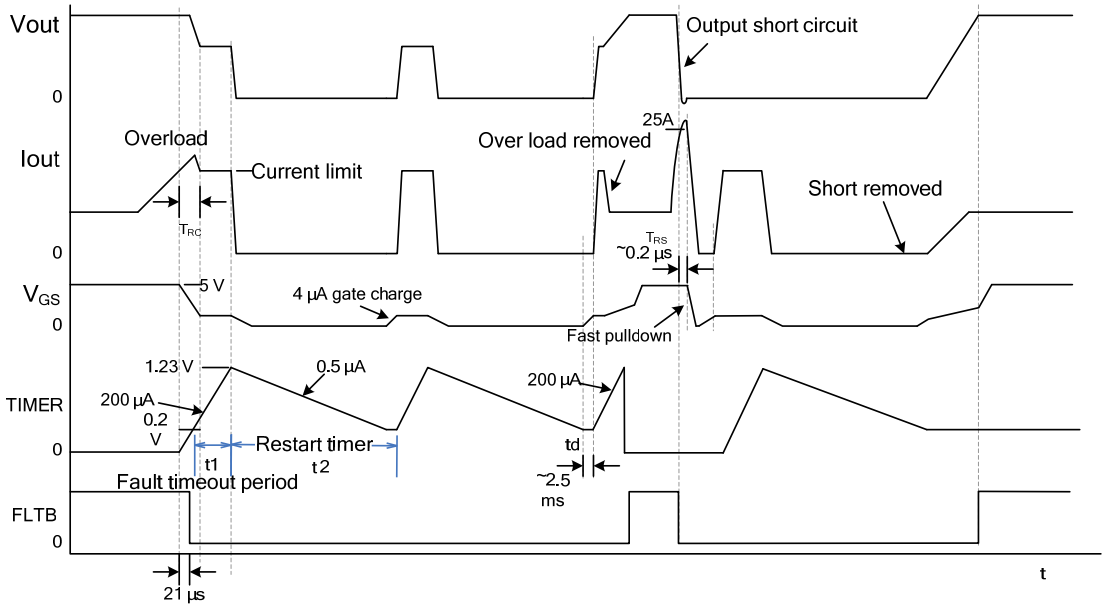


Figure 3—Over-current protection (auto-retry mode, AUTO = High)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

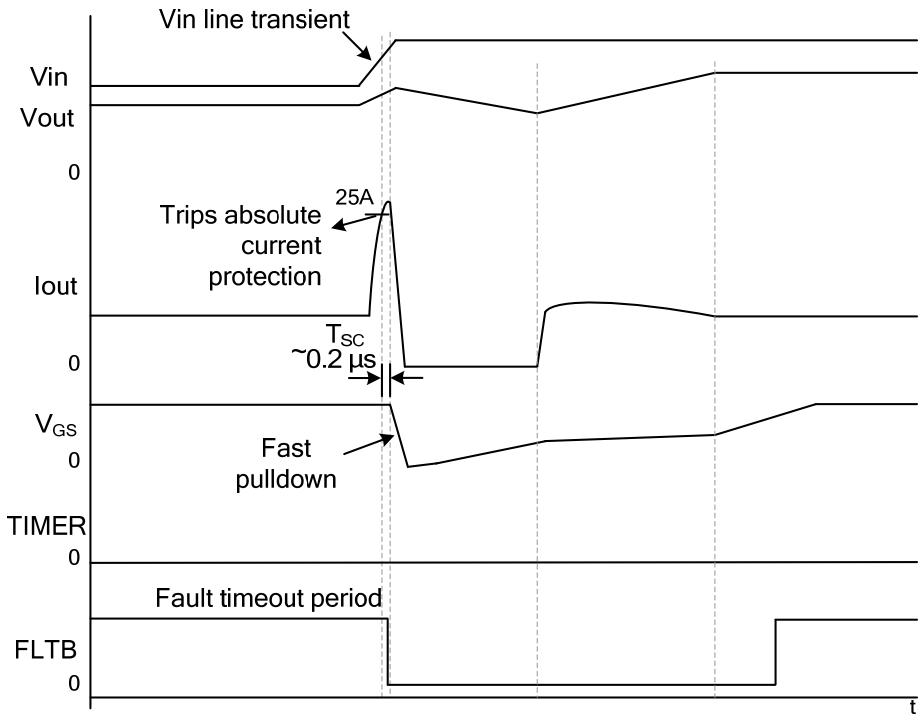


Figure 4—Input voltage line transient response

Power Good

The power good is the open drain of a FET and indicates whether the output voltage is in the normal range (relative to the input voltage). Pull PG up to the external power supply through a 10k-100kΩ resistor. During power-up, the power-good output is driven low. This directs the system to remain off and minimizes the load on VOUT to reduce inrush current and power dissipation during the start-up condition.

The power good signal is pulled high during the following conditions, allowing the system to draw full power:

1. V_{FB} > 90%*V_{FBH}
2. V_{GS} > 3V
3. V_{OUT} >V_{IN}-0.7V

When the FB voltage drops below 75%*V_{FBH}, PG is pulled low.

The PG output is pulled low when EN is below its threshold. With no input, the power good stays at a logic low level in the presence of a pull-up supply.

FLTB

The fault bar (FLTB) pin is an open-drain output used to indicate that a fault has occurred. Pull FLTB up to an external power supply through a 10k-100kΩ resistor.

When the device reaches its current limit, the die temperature exceeds the thermal shutdown threshold, or the MOSFET is shorted before power-up. The fault output is driven low with a 21µs propagation delay. If a short occurs and the current reaches its 25A secondary current limit, the FLTB switches low immediately.

FLTB goes high when the MP5021B resumes normal operation, which means the output voltage exceeds the setting voltage of the PG rising threshold, and the power FET is on completely (V_{GS} > 3 V).

External Pull-Up Voltage for PG and FLTB

The PG and FLTB need an external power supply. The open-drain output of PG works well from the external pull-up voltage even when V_{IN} = 0 and EN is disabled. Use a 10k-100kΩ pull-up resistor for PG and FLTB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

Power-Up Sequence

For hot-swappable applications, the input of the MP5021B can experience a voltage spike or transients during the hot-plug procedure. This spike is caused by the parasitic inductance of the input trace and the input capacitor. In order to stabilize the input voltage, an insertion delay is implemented before the MP5021B main FET is turned on. TIMER charges the external capacitor (C_T) through a 38.5μA constant current source when the input voltage reaches the UVLO threshold (see Figure 5). The insertion delay finishes when the TIMER voltage reaches 1.23V. The capacitance of C_T can be determined using Equation (2):

$$C_T = \frac{38.5 \cdot \tau_{delay}}{1.23} \quad (2)$$

Where:

C_T = Insertion delay timer capacitance in nF

τ_{delay} = Insertion delay in ms

For example, a 100nF capacitor yields a insertion delay time of 3.2ms.

This insertion delay timer capacitor determines the fault timer as specified in the “Fault Timer & Restart” section.

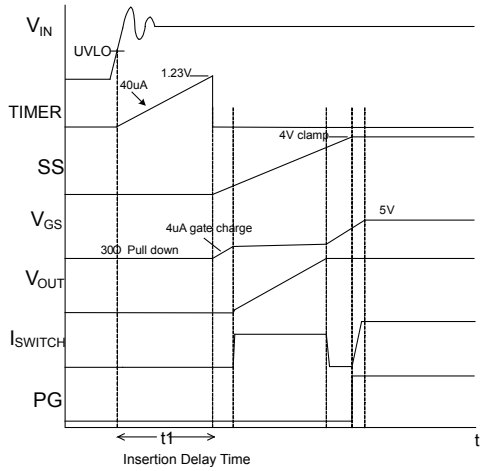


Figure 5—Start-Up Sequence

When EN enables the part, the insertion delay timer starts as well. When the TIMER voltage reaches 1.23V, the insertion delay time ends, and an internal 4μA current source charges the power FET’s gate. Meanwhile, the TIMER voltage drops. Charging takes about 1.5ms for V_{GS} to reach its threshold (V_{GSTH}). Then the output voltage rises following the SS controlled slew rate.

Soft Start (SS)

A capacitor connected to SS determines the soft-start time: When the insertion delay time ends, a constant current source that is proportional to the input voltage ramps up the voltage on SS. The output voltage rises at a similar slew rate to the SS voltage.

The SS capacitor value is given using Equation (3):

$$C_{SS} = \frac{5 \cdot \tau_{SS}}{R_{SS}} \quad (3)$$

Where:

τ_{SS} = Soft-start time

R_{SS} = 1MΩ

For example, a 100nF capacitor gives a soft-start time of 20ms.

If the load capacitance is extremely large, the current required to maintain the preset soft-start time will exceed the current limit. Then the load capacitor and the current limit control the rise time.

Float SS to generate a fast ramp-up voltage. A 4μA current source pulls up the gate of the power FET. The gate charge current controls the output voltage rise time. The approximate soft-start time is about 1ms, which is the minimum soft-start time.

ENABLE and EN Blanking Time

EN high enables the part; EN low disables the part. Floating EN sets the part to auto-startup due to an internal 1μA pull-up current source.

EN has a programmable blanking time of up to 1s that prevents EN from de-asserting during the blanking time (see Figure 6). All fault functionality continues to operate during the start-up, so that the power switch shuts down if a fault is detected. However, the switch will not turn off if EN goes low during the blanking time.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

When the blanking time ends, EN operates normally.

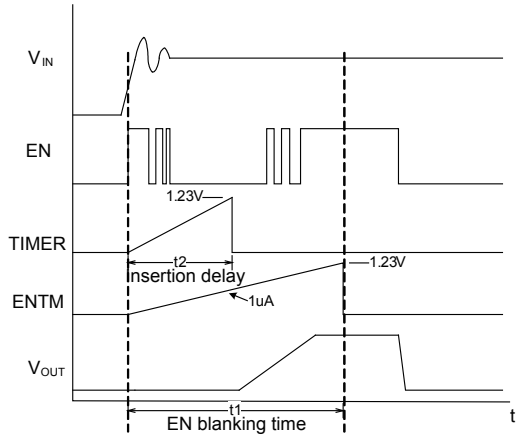


Figure 6—EN blanking time

Set the blanking time with a capacitor connected to ENTM. Equation 4 estimates a value for the blanking timer capacitor:

$$C_{ENB} = \frac{0.85 \cdot 10^{-6} \cdot \tau_{ENB}}{1.23} \quad (4)$$

Where:

τ_{ENB} = EN blanking time

C_{ENB} = EN blanking time capacitor

For example, a 1μF capacitor gives a blanking time of 1.45s.

Floating ENTM generates a fast ramp-up voltage on ENTM. The blanking time during this period is negligible. When EN enables the part, the insertion delay timer operates as specified in the "Power-Up Sequence" section.

Damaged MOSFET Detection

The MP5021B detects a shorted pass FET during power-up by treating an output voltage that exceeds V_{IN}-0.7V during power-up as a short on the MOSFET. FLTB goes low to indicate a fault condition, and the power switch remains off. Once $V_{OUT} \leq V_{IN}$-0.7V, the part starts up normally.

Internal VCC Sub-Regulator

The MP5021B has an internal 5V linear sub-regulator that steps down the input voltage to generate a 5V power supply that powers low-voltage circuitry. The regulator is enabled when V_{IN} exceeds its UVLO threshold, and EN is high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

PD Pin

When PD connects to the output, MP5021B has output discharge capability. When EN turns off the main switch, or the switch is turned off by a fault condition, an integrated 500Ω pull-down resistor (attached to the output) discharges the output. PD can be connected to V_{OUT} directly, adding a resistor between PD and the output results in a slower output drop. If PD is floating, the pull-down mode is disabled.

AUTO

When AUTO is floating, the part is in auto-retry mode. In auto-retry mode, the part turns off when it exceeds its thermal limit or current limit timeout. This causes the part to turn back on when the part cools 15°C or the re-start timer completes.

When AUTO is tied to ground, the part is in latched-fault mode. In latched-fault mode, a thermal fault or current limit fault latches the output off until the enable line is toggled from low to high, or the input voltage re-starts.

Under/Over-Voltage Lockout (UVLO/OVLO)

If the input supply falls below the UVLO threshold or above the OVLO threshold, the output is disabled.

When the supply exceeds the UVLO threshold without exceeding the OVLO threshold, the output is enabled, and the PG line is released.

Monitoring the Output Current

IMON provides a voltage proportional to the output current (the current through the power device). The gain of the current sense amplifier is 40μA from IMON for 1A of MOSFET current. Placing a 10 k resistor to ground creates a 0V to 2.4V voltage when the MOSFET current ranges from 0A to 6A at VIN = 12V. The voltage compliance for IMON is from 0V to 3V. Place a capacitor greater than 100nF in parallel with R_{MON}.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Current Limit (R_{SET})

The MP5021B current limit value must exceed the normal maximum load current, allowing tolerances in the current sense value. Estimate the current limit using Equation (5):

$$I_{limit} = \frac{0.615(V)}{R_{SET}} \times 5 \times 10^4 (A) \quad (5)$$

Where, R_{SET} is the current-limit resistor in Ω.

Table 1 and Figure 7 show the bench results from the evaluation board.

Table 1—Current limit vs. current limit resistor (R_{SET})

R_{SET} (kΩ)	7.5	10	20
Current L\limit (A)	3.96	3.08	1.5

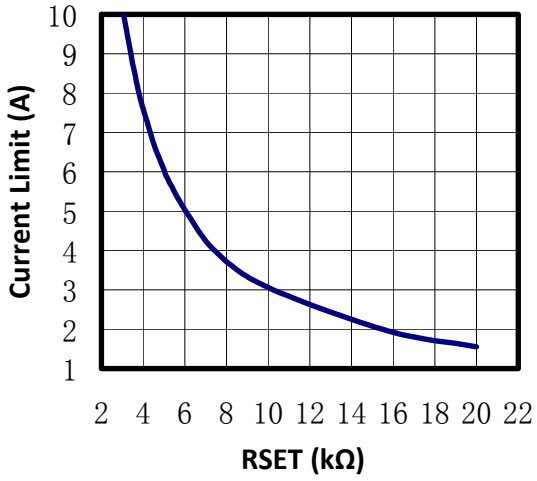


Figure 7—R_{SET} resistor vs. current limit @ VIN = 12 V

The maximum current limit value can be set to 10A if VIN ≥ 8V, for VIN = 5V applications, the maximum current limit value should be set lower than 5 A.

Current Monitor

MP5021B monitors the power FET current. Place a resistor (R_{MON}) to ground to set the gain of the output using Equation (6):

$$I_{IMON} = 40 \cdot I_{POWERFET} (\mu A) \quad (6)$$

Where $I_{POWERFET}$ is the power MOSFET current.

Placing a 10kΩ from IMON to GND gets 400mV per amp. Place a 100 nF capacitor from IMON to GND to smooth the indicator voltage.

PCB Layout Guide

Efficient PCB layout is critical for optimum performance. For best results, refer to Figure 8 and follow the guidelines below:

1. Place the high-current path from the board's input to output and the return path parallel and close to each other to minimize loop inductance.
2. First connect GND and the signal GND signal together, and then make a Kelvin connection to PGND or the internal GND layers.
3. Ensure the input decoupling capacitors on VIN have a minimal trace length to the VIN pins and GND.
4. Connect a transient voltage suppressor diode (TVS) to VIN. The TVS can absorb the input voltage spike if the load current decreases sharply.
5. Place the Schottky diode close to VOUT and GND to absorb the negative voltage spike when the power FET is shut off.
6. Place output capacitors as close to the part as possible to minimize the effect of PCB parasitic inductance.
7. Keep the IN and GND pads connected with a large copper plane and place vias in the thermal pad to improve thermal performance.
8. Ensure all VIN and VOUT pins are connected to get equal current distribution to each lead.

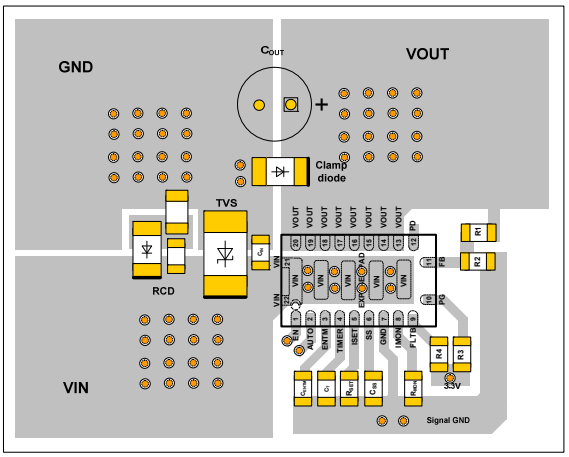


Figure 8—Recommended PCB layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

Design Example

The detailed application schematic is shown in Figure 9 and Figure 10. The typical performance and circuit waveforms have been shown in the "Typical Performance Characteristics" section. For additional device applications, please refer to the related evaluation board datasheets of MP5021B.

TYPICAL APPLICATION

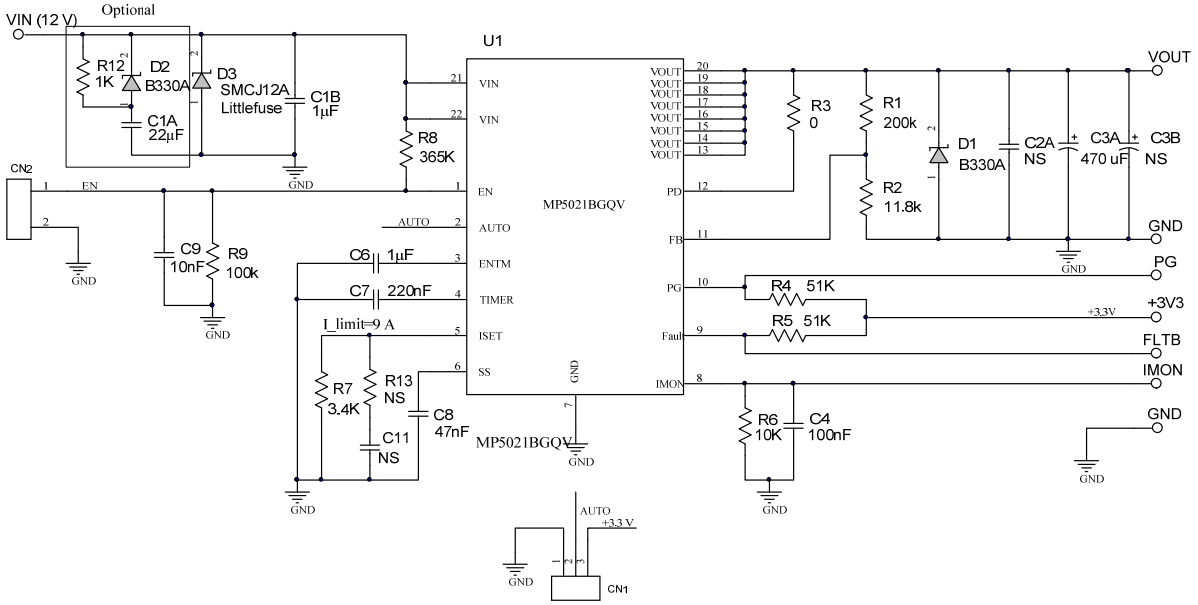


Figure 9—Typical application circuit with soft-start time 10 ms, current limit 9 A @ VIN = 12 V

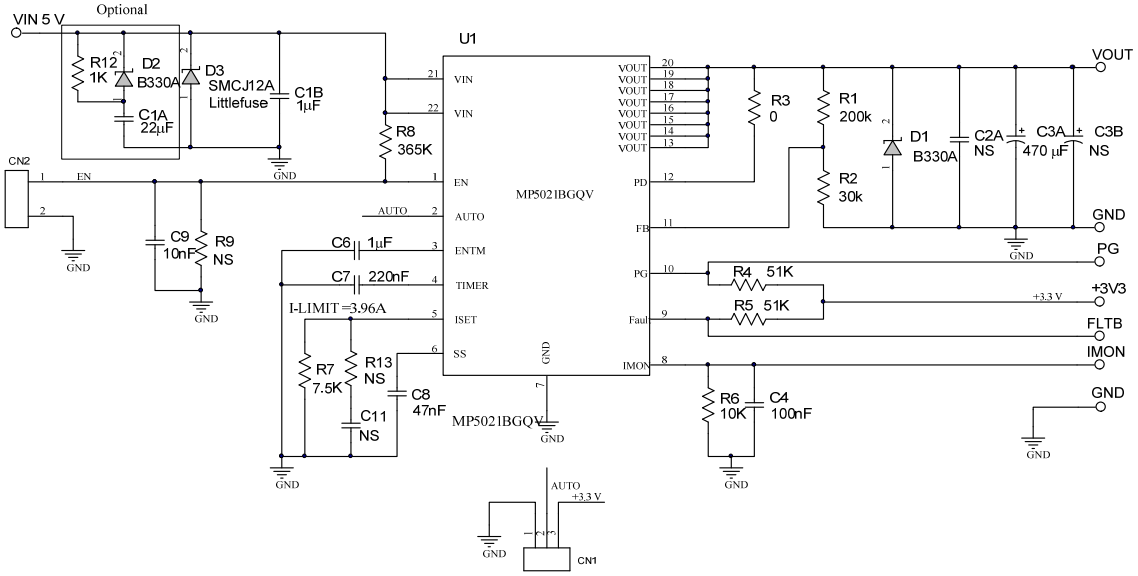
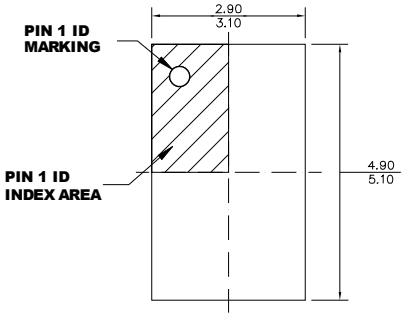


Figure 10—Typical application circuit with soft-start time 10 ms, current limit 3.96 A @ VIN = 5 V

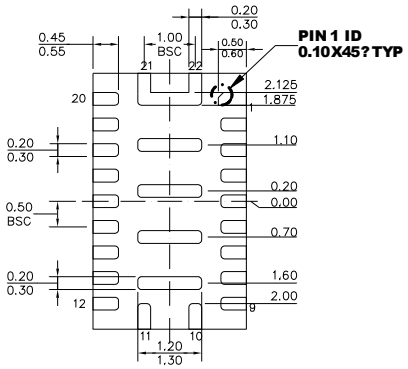
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE INFORMATION

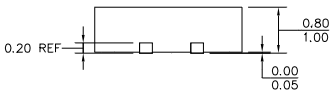
QFN22 (3mm x 5mm)



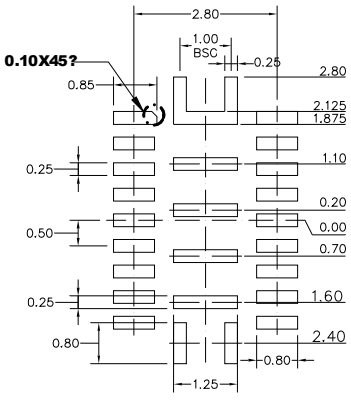
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.