MP5017

3V-.5.5V, 1A – 5A Current Limit Switch with Over-Voltage Clamp and Reverse Blocking in 2mmx3mm QFN Package

The Future of Analog IC Technology

DESCRIPTION

The MP5017 is a protection device designed to protect circuitry on the output from transients from the input. Also, it protects the input from unwanted shorts and transients coming from the output.

During start-up, the inrush current is controlled by limiting the slew rate at the output. The slew rate is controlled with a small capacitor at DV/DT.

The maximum load at the output is current limited. The magnitude of the current limit is controlled by an external resistor from ILIMIT to GND. By controlling the gate voltages with a pair of N-channel MOSFETs, any current flowing from the output to the input is blocked.

Under-voltage lockout (UVLO) ensures that the input is above the minimum operating threshold before the power device is turned on. If the input voltage rises above 5.8V, the output voltage is limited quickly to 5.8V. SAS/OV is used to program the input over-voltage protection threshold.

$\overline{\text{Fault}}$ is an open-drain output that reports a fail mode (low level) when any over-current, over-temperature, or output over-voltage is detected.

The MP5017 is available in a QFN-12 (2mmx3mm) package.

FEATURES

- 3V to 5.5V Continuous Operating Input Range
- 16V Absolute Maximum Input Voltage
- Output Discharge
- SAS/OV Disable to Support DEVSLP or POWER_DOWN
- 5.8V Fast Output OVP Response
- Reverse Current Blocking
- Integrated 45mΩ $R_{DS(ON)}$ Power FET
- Adjustable Current-Limit through ILIMIT
- 210µA Low Quiescent Current
- Programmable Soft-Start Time through DV/DT
- Fast Response for Hard-Short Protection
- Fault Indication for Over-Current, Over-Temperature, and Output Over-Voltage
- OTP Auto-Retry with 76ms Recovery Delay
- Available in a QFN-12 (2mmx3mm) Package

APPLICATIONS

- HDD and SSD
- Hot Swap
- Wireless Modem Data Cards
- PC Cards
- USB Power Distribution

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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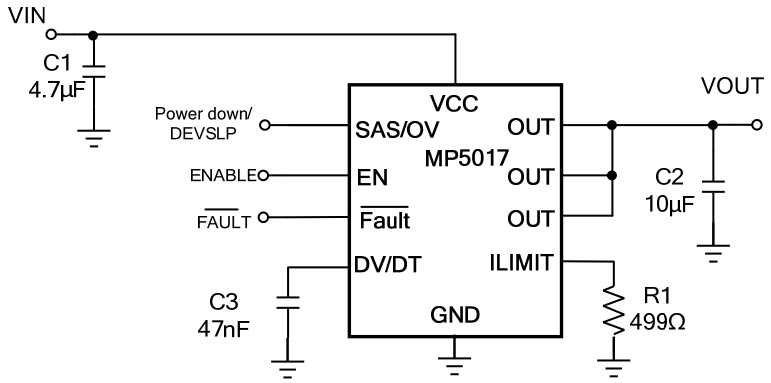
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5017GD	QFN-12 (2mmx3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP5017GD–Z)

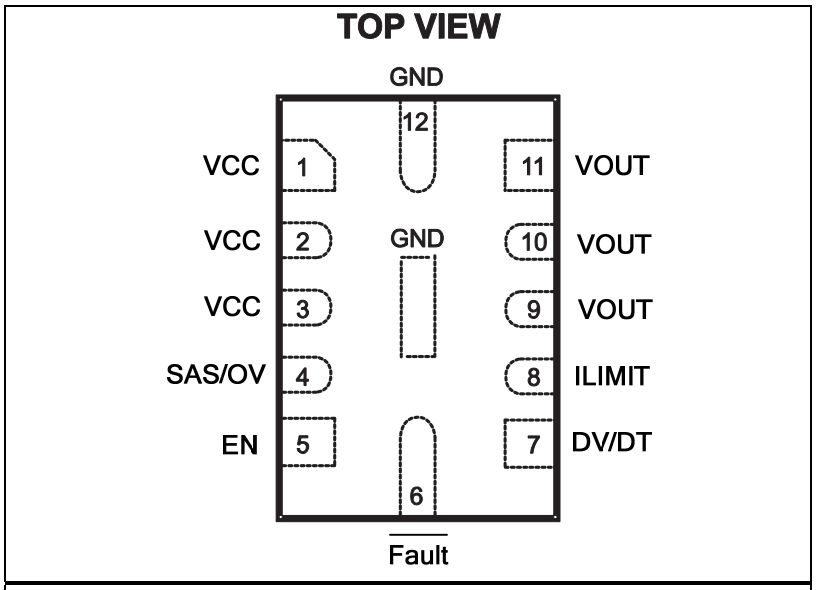
TOP MARKING

$\overline{\text{ANTY}}$

LLL

ANT: Product code of the MP5017GD
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-12 (2mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 16V
V_{OUT}..... 6.3V
All other pins .....-0.3V to +6V
Junction temperature ..... -40°C to +150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = +25°C) (2)
QFN-12 (2mmx3mm)..... 1.8W

Recommended Operating Conditions (3)

Continuous operation (V_{IN}).....3V to 5.5V
Supply maximum transient (V_{IN}) 16V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-12 (2mmx3mm)	70	15 °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, R_{LIMIT} = 499Ω, C_{OUT} = 10μF, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_Q	EN, no load		210	310	μA
		EN = 0, SAS/OV = 0V		10	15	μA
		SAS/OV = 3V, EN = 5V			120	μA
Power FET						
On resistance	R_{DSon}	T_J = 25°C		45		mΩ
On resistance[5]	R_{DSon}	T_J = 80°C		54		mΩ
Turn-on delay	T_{delay}	I_{OUT} = 0A, $C_{DV/DT}$ = 1nF		160		μs
Off-state leakage current	I_{OFF}	V_{IN} = 14V, EN = 0V			1	μA
Under-/Over-Voltage Protection						
Under-voltage lockout threshold	V_{UVLO}	UVLO rising threshold	2.45	2.7	2.95	V
UVLO hysteresis	$V_{UVLOHYS}$			250		mV
Output over-voltage clamp voltage	V_{OVLO}		5.5	5.8	6.1	V
Output over-voltage response time[6]	t_{OUT_OV}	C_{OUT} = 10μF, add 10Ω load resistor, V_{IN} = 5V to 7V/20μs		10	20	μs
DV/DT						
DV/DT current	$I_{DV/DT}$	Short DV/DT to GND, or add DV/DT cap	4.5	6.5	8.5	μA
Current Limit						
Current limit at normal operation	I_{Limit_NO}	R_{LIMIT} = 499Ω, V_{OUT} drops 10%	2	2.4	2.8	A
		R_{LIMIT} = 1.4kΩ, V_{OUT} drops 10%		0.9		A
Current limit response time[6]	t_{CL}	I_{LIMIT} = 3A, add 1Ω load resistor		10		μs
Secondary current limit[6]	I_{LimitH}	Any value of R_{LIMIT}		7.5		A
Reverse Current Limit						
Reverse current limit	$I_{Reverse}$	Any value of R_{LIMIT}	-5	-50	-200	mA
Reverse current limit deglitch time[6]	$t_{Reverse}$			80		μs
Secondary reverse current limit[6]	$I_{ReverseH}$	Fast response		-1		A
Secondary reverse current limit response time[6]	t_{SC}	V_{IN}_DV/DT = -5V/100μs		8		μs
Enable						
EN rising threshold	V_{EN_RISING}		1.4	1.47	1.55	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-up current	I_{EH_PL}	V_{ENABLE} = 0V		3.4		μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, R_{LIMIT} = 499Ω, C_{OUT} = 10μF, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SAS/OV						
Rising threshold	V_{SAS/OV_RISING}	Output disabled	1.2	1.25	1.3	V
Hysteresis	V_{SAS/OV_HYS}			40		mV
Input over-voltage deglitch time	$t_{IN_SAS/OV}$			5		μs
$\overline{\text{Fault}}$						
$\overline{\text{Fault}}$ output logic low voltage	V_{FAULT_L}	Sink 1mA			200	mV
$\overline{\text{Fault}}$ output high leakage current	I_{FAULT_OFF}	$V_\overline{\text{Fault}}$ = 5.5V			1	μA
$\overline{\text{Fault}}$ deglitch time	$T_{FAULT_DEG_OC}$	Delay time for assertion or deassertion due to OCP fault condition		5		ms
	$T_{FAULT_DEG_OV_OUTPUT}$ (5)	Delay time for assertion or deassertion due to output OVP fault condition		10		μs
Output Discharge						
Discharge resistance	R_{DIS}	V_{CC} = 5V		130		Ω
OTP						
Thermal shutdown(5)	T_{SD}			175		°C
Thermal hysteresis(5)	T_{SD-HYS}			50		°C

NOTES:

5) Guaranteed by characterization test.
6) Guaranteed by design.

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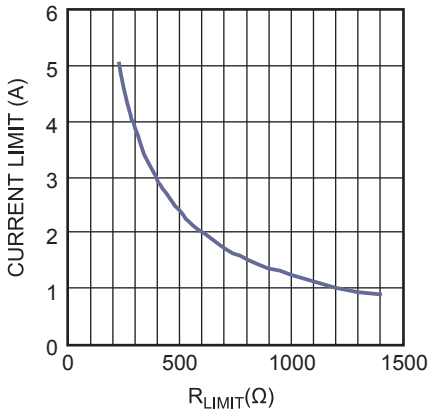
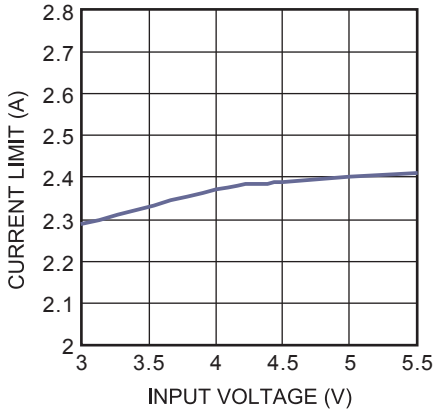
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 499Ω , SAS/OV float, C_{OUT} = 10μF, T_A = 25°C, unless otherwise noted.

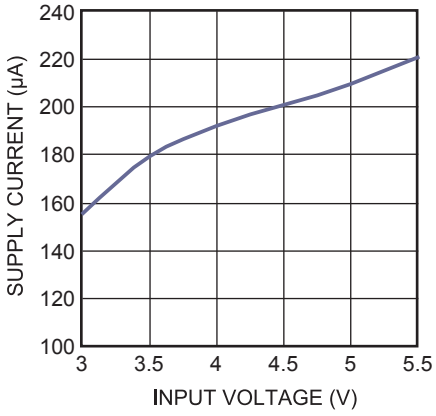
Current Limit vs.R_{LIMIT}
V_{OUT} drops 10%



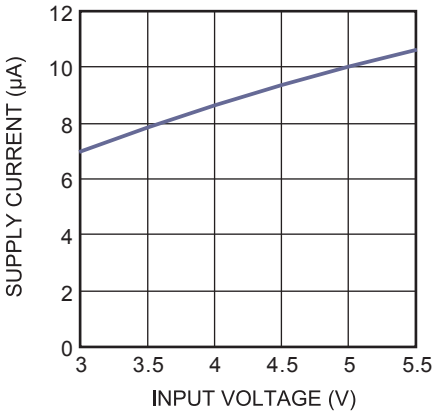
Current Limit vs. Input Voltage
R_{LIMIT} =499Ω



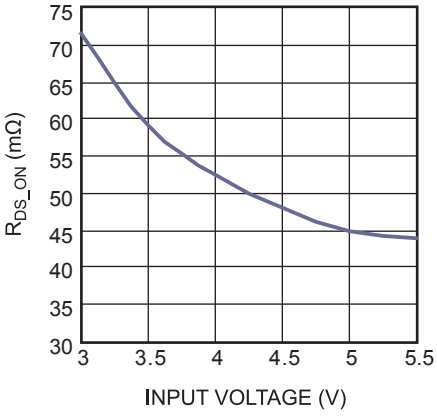
Supply Current, Output Enabled vs. Input Voltage



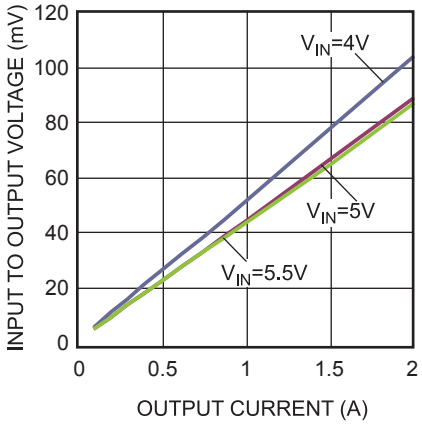
Supply Current, Output Disabled vs. Input Voltage



R_{DS_ON} vs. Input Voltage
I_{OUT}=0.5A



Input to Output Voltage vs. Output Current
R_{LIMIT} =499Ω



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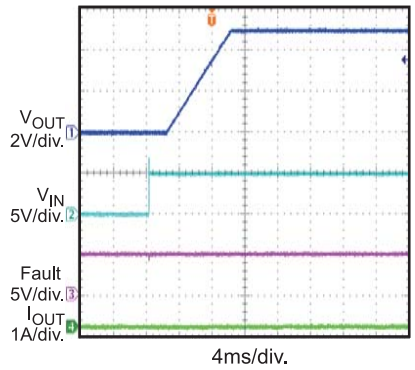
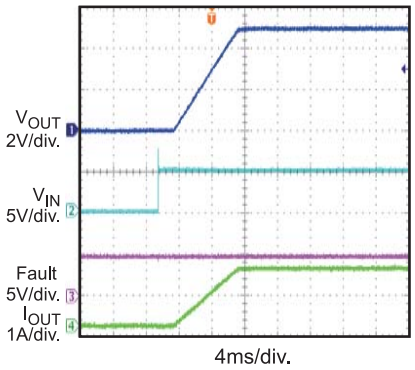
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 499Ω, SAS/OV float, C_{OUT} = 10μF, T_A = 25°C, unless otherwise noted.(7)

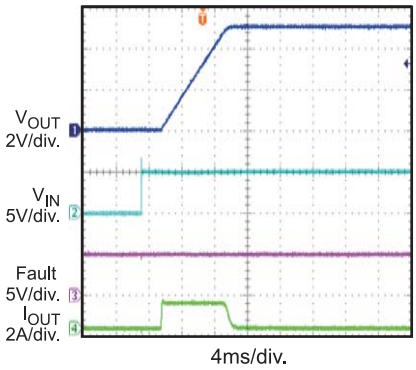
Start-Up through Input Voltage
No Load



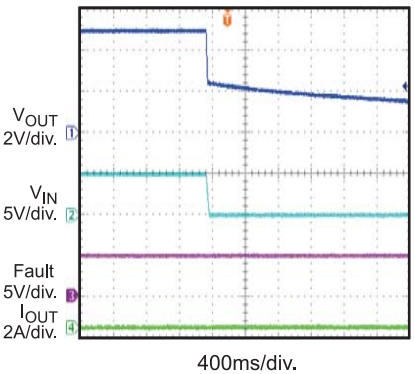
Start-Up through Input Voltage
R_{LOAD} = 3.3Ω



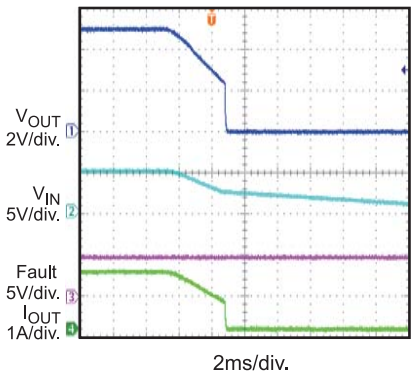
Start-Up through Input Voltage
No Load, C_{OUT} = 2200μF



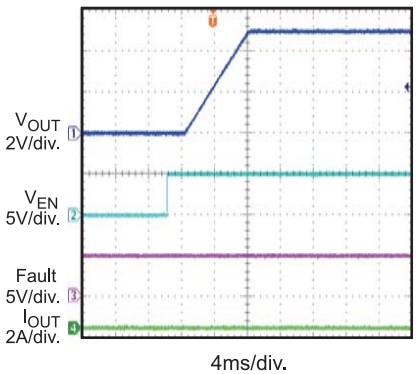
Shutdown through Input Voltage
No Load



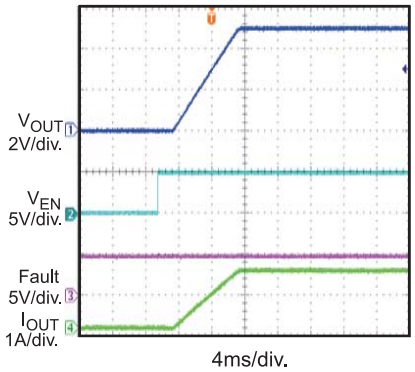
Shutdown through Input Voltage
R_{LOAD}=3.3Ω



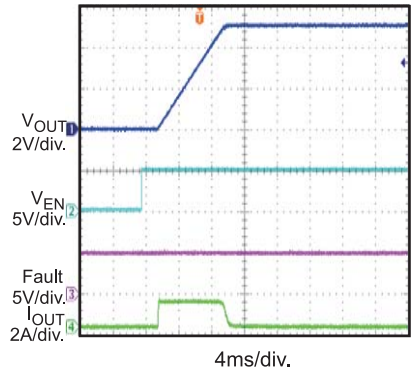
Start-Up through EN
No Load



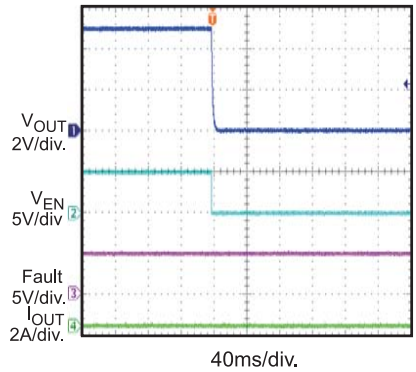
Start-Up through EN
R_{LOAD} = 3.3Ω



Start-Up through EN
No Load, C_{OUT} = 2200μF



Shutdown through EN
No Load



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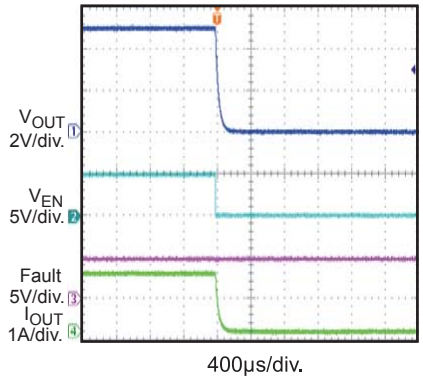
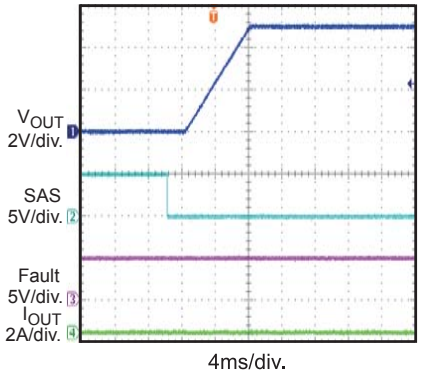
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 499Ω, SAS/OV float, C_{OUT} = 10μF, T_A = 25°C, unless otherwise noted.(7)

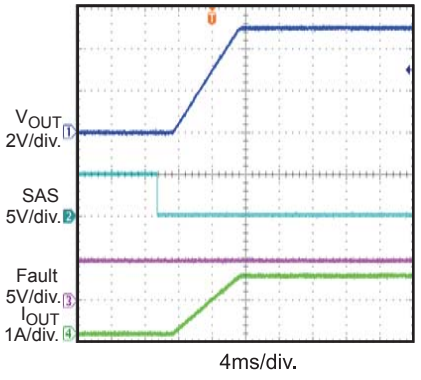
Shutdown through EN
R_{LOAD}=3.3Ω



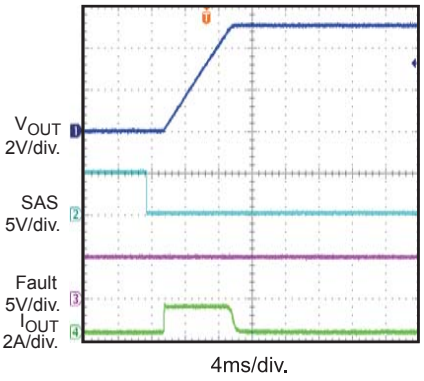
Start-Up through SAS
No Load



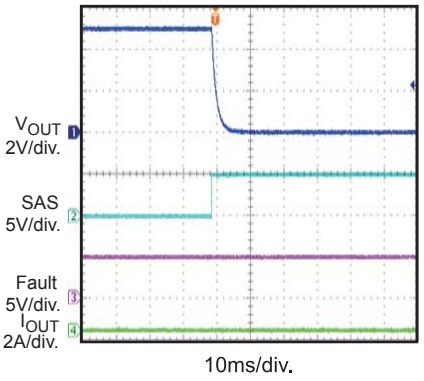
Start-Up through SAS
R_{LOAD}=3.3Ω



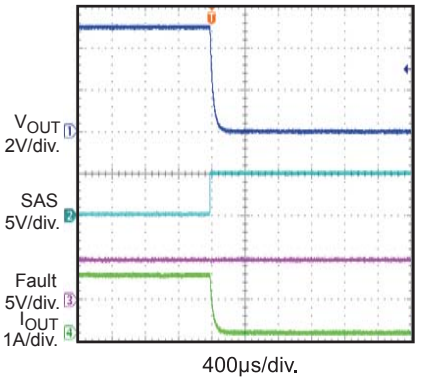
Start-Up through SAS
No Load, C_{OUT} = 2200μF



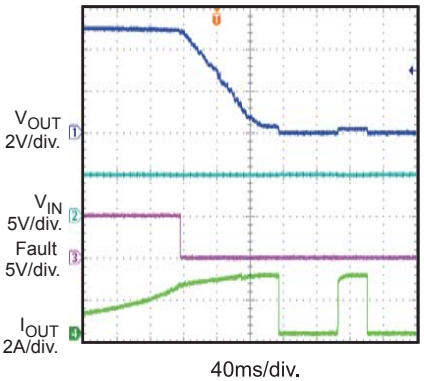
Shutdown through SAS
No Load



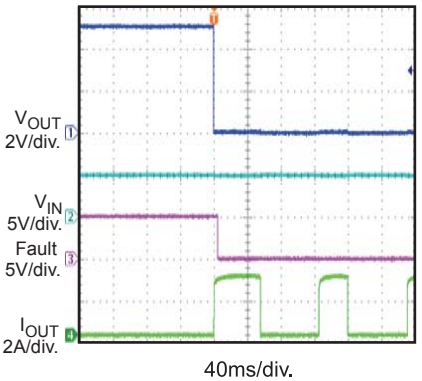
Shutdown through SAS
R_{LOAD}=3.3Ω



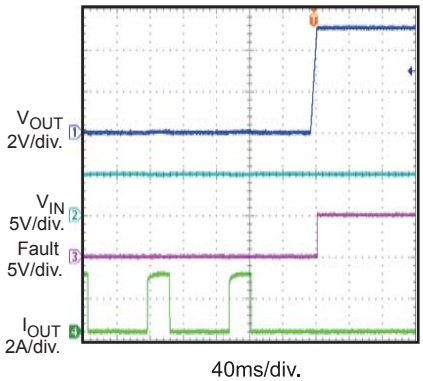
Over-Current Protection



Short-Circuit Protection Entry



Short-Circuit Protection Recovery



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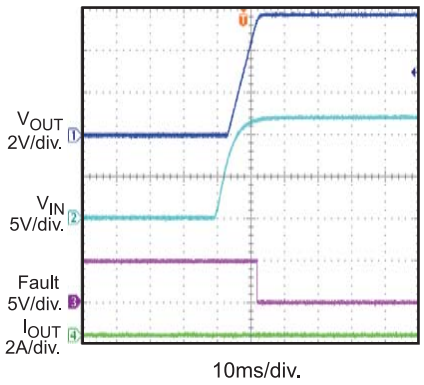
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 499Ω, SAS/OV float, C_{OUT} = 10μF, T_A = 25°C, unless otherwise noted.(7)

Start-Up into OVP
V_{IN}=12V, No Load



NOTE:
7) $\overline{\text{Fault}}$ is connected to an external 5V source through a 100k pull-up resistor.

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PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3	VCC	**Supply voltage.** The MP5017 operates on a 3V to 5.5V continuous input voltage range with up to 16V of maximum transient input voltage. Decouple the input rail with a 4.7µF ceramic capacitor. Connect using a wide PCB trace.
4	SAS/OV	**SAS disable.** Pull SAS/OV low to enable the part; pull SAS/OV high to disable the part. SAS/OV has an internal 1MΩ pull-down resistor to ground, so it can start up automatically when SAS/OV is floating. Connect SAS/OV to the tap of an external resistor divider from input to GND to set the input over voltage.
5	EN	**Enable.** EN is a digital input that turns the regulator on or off. Float EN or drive EN high to turn on the regulator; drive EN low to turn off the regulator.
6	$\overline{\text{Fault}}$	**Open drain output.** If OCP, OTP, or output OVP occurs, $\overline{\text{Fault}}$ is pulled low.
7	DV/DT	**Slew rate.** The internal DV/DT circuit controls the slew rate of the output voltage at turn on. An external capacitor from DV/DT to ground is needed to set the soft-start time.
8	ILIMIT	**Current limit set.** Place a resistor between ILIMIT and ground to set the value of the current limit.
9, 10, 11	VOUT	**Output voltage.** VOUT is controlled by the IC.
12, Exposed Pad	GND	**System ground.**

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FUNCTIONAL BLOCK DIAGRAM

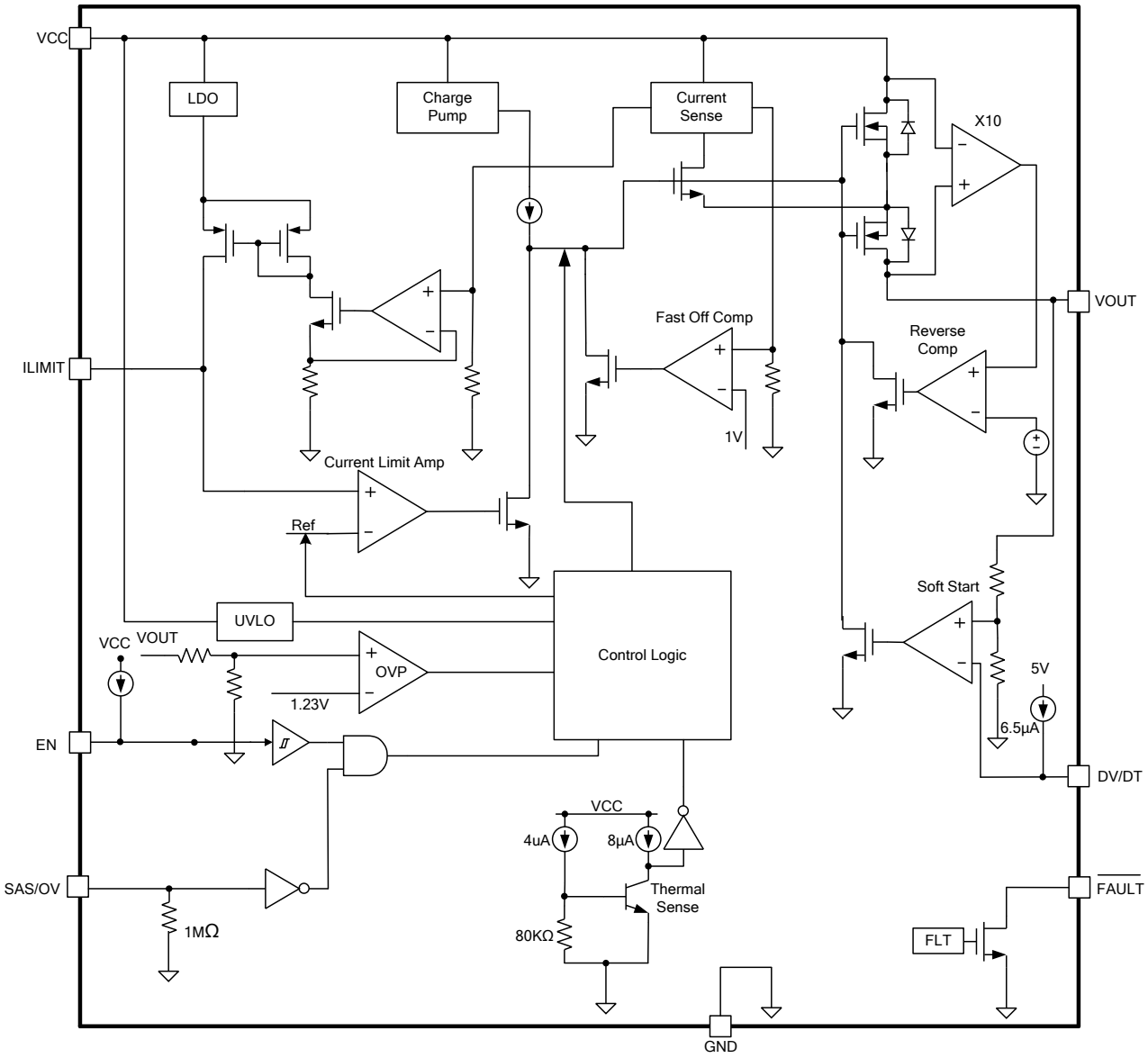

Figure 1: Functional Block Diagram

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OPERATION

The MP5017 is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source. This limits the backplane's voltage drop, as well as the DV/DT of the voltage to the load. It offers an integrated solution that monitors the input voltage, output voltage, output current, and die temperature, eliminating the need for an external current sense power resistor, power MOSFET, and thermal sense device.

Under-Voltage Lockout (UVLO)

The nominal input supply voltage is 5V, but high energy transients can occur during normal operation or hot swaps. These transients depend on the parasitic inductance, resistance of the wire, and the capacitor at VCC. If the power clamp (TVS, Tranzorb) is not used, the E-Fuse must be able to withstand this transient voltage. The MP5017 uses a high-voltage MOSFET of up to 16V and a high-voltage circuit on VCC to guarantee safe operation.

SAS/OV Control

SAS/OV can control the part during start-up and shutdown. Floating or pulling SAS/OV low enables the part; pulling it high disables the part. It also can be used as an input OVP control. The input OVP limit can be set by a divider from VCC to SAS/OV (see Figure 2). When the SAS/OV voltage exceeds 1.25V, the part shuts down. When the voltage drops below 1.21V or SAS/OV is floated, the part is enabled again.

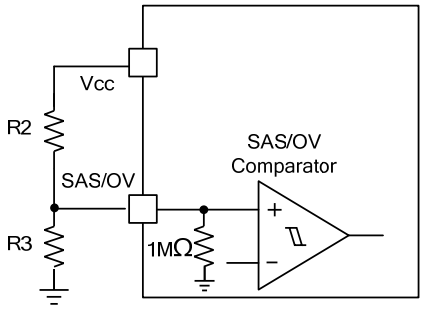

Figure 2: Adjustable Input OVP

Soft Start (SS)

The rise time is a function of the capacitor ($C_{DV/DT}$). The approximate value can be calculated with Equation (1):

$$t_{DV/DT}(ms) = \frac{1V \times C_{SS}(nF)}{6.5\mu A} \quad (1)$$

Where $t_{DV/DT}$ is the soft-start time.

For example, a 47nF capacitor generates a soft-start time of approximately 7.2ms.

Fast Output Over-Voltage Protection (OVP)

The MP5017 uses an output OVP function to protect the downstream loading when there is a voltage surge at the input. An accurate and fast comparator monitors the over-voltage condition on the output. If the output voltage rises above the threshold (typically 5.8V), the gate of the internal MOSFET is pulled down quickly and is regulated to a specific value to keep the output voltage clamped at 5.8V. The rapid loop response speed (typically 10μs) keeps the over-voltage overshoot small.

Current Limit

The MP5017 provides a constant current limit, which can be programmed by an external resistor. Once the current limit threshold is reached, the internal circuit regulates the gate voltage to hold the current in the power FET. To limit the current, the gate-to-source voltage needs to be regulated from 5V to around 1V. The typical response time is about 10μs. During this period, the output current may have a small overshoot.

The desired current limit is a function of the external current limit resistor.

Reverse Current Blocking

The MP5017 uses a pair of back-to-back N-channel MOSFETs for reverse current protection. Once the reverse current limit threshold (-50mA) is reached and exceeds the 80μs deglitch time, the internal circuit pulls the gate voltage down to shut down the MOSFETs. If the reverse current reaches the -1A threshold, the part shuts the MOSFETs down immediately to prevent VOUT from being pulled down. $\overline{Fault}$ does not change its state during the reverse current limit. The reverse current is

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blocked, and this state continues until VCC > VOUT-2mV. When VCC > VOUT-2mV, the part restarts. If the input voltage drops below the UVLO threshold, the back-to-back MOSFETs are turned off, eliminating any reverse current.

Fault

$\overline{\text{Fault}}$ is an open-drain configuration. If any over current is detected, $\overline{\text{Fault}}$ reports a fail mode (low level) after a 5ms deglitch timeout. There is a 10µs deglitch timeout when the output over voltage is triggered. This ensures that no false fault signals are reported. The internal deglitch circuit eliminates the need for external components. $\overline{\text{Fault}}$ does not deglitch during an over-temperature condition (see Table 1).

Table 1: $\overline{\text{Fault}}$ Function Truth Table

Description	$\overline{\text{Fault}}$	E-Fuse State	Latch	Output Discharge
Under-voltage lockout	High	Off	No	No
EN low	High	Off	No	Yes
SAS/OV high	High	Off	No	Yes
V_{OUT} OVP clamp	Low (10µs deglitch time)	High Z	No	No
Thermal shutdown	Low	Off	No	No
Current limit	Low (5ms deglitch time)	High Z	No	No
Fast current limit	Low	Off	No	No
Reverse current protection	High	Off	No	No
SAS/OV floating	High	On	No	No
SAS/OV low	High	On	No	No

Short-Circuit Protection

If the load current increases too rapidly due to a short-circuit event, the current may exceed the current limit threshold before the control loop is able to respond. If the current reaches 7.5A, a secondary current limit level from a fast turn-off circuit is activated. The power FET turns off with a 100mA pull-down gate discharge current. This helps limit the peak current through the switch, keeping the input voltage from dropping excessively. After the FET is switched off, the part restarts. If the short remains during the restart process, the MP5017 regulates the gate voltage to hold the current at a normal current limit level.

Output Discharge

The MP5017 uses a discharge function to provide a resistive discharge path for the external output capacitor. The function is active

when the part is disabled (EN low or SAS high). and is done in a very limited amount of time.

EN Control

EN enables the part when it is high and disables the part when it is low. Floating EN automatically starts the part up because an internal current source pulls EN up to the internal supply. The maximum internal pull-up voltage source is about 5V.

Thermal Shutdown (OTP Auto-Retry)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 175°C, the entire chip shuts down and $\overline{\text{Fault}}$ reports a fail mode. When the temperature drops below its lower threshold, typically 125°C, the chip is enable again after a 76ms delay.

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APPLICATION INFORMATION

Setting the Current Limit

The MP5017 current limit value should exceed the normal maximum load current to account for the variations in the current sense value. The current limit is a function of the external current-limit resistor. The value can be approximated with Equation (2):

$$I_{LIMIT}(A) = \frac{1.16V \times 10^3}{R_{LIMIT}(\Omega)} \quad (2)$$

Table 2 and Figure 3 below list examples of current limit values as a function of the resistor value.

Table 2: Current Limit vs. Current Limit Resistor

Current Limit Resistor (Ω)	1400	806	499	324	226
Current Limit (A)	0.9	1.51	2.40	3.61	5.04

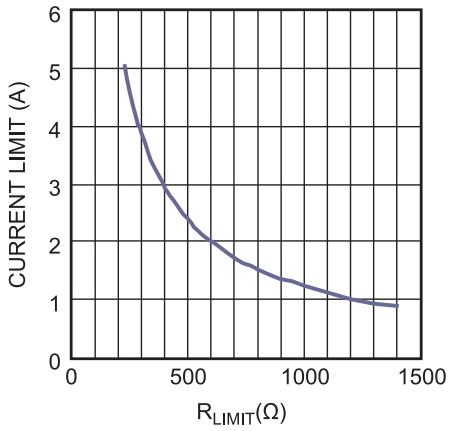
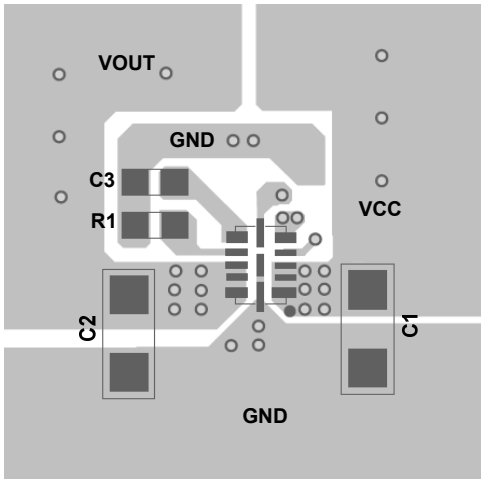


Figure 3: Current Limit vs. Current Limit Resistor

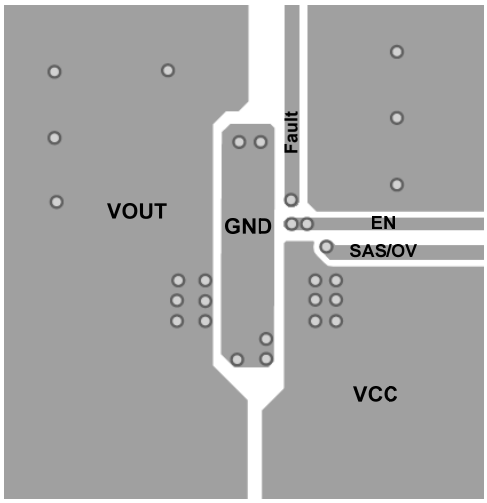
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and follow the guidelines below.

1. Place the high-current paths (VCC and VOUT) close to the device using short, direct, and wide traces.
2. Place the input capacitor (C1) as close to VCC and GND as possible.
3. Connect the VCC and VOUT pads to large copper traces for better thermal performance.
4. Place R_{LIMIT} (R1) close to ILIMIT.
5. Place DV/DT capacitor (C3) close to DV/DT.



Top Layer



Bottom Layer

Figure 4: Recommended Layout

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Design Example

Below is a design example following the application guidelines for the given specifications:

Table 3: Design Example

V_{IN}	5V
Current limit	2.4A
SS time	7.2ms

The detailed application schematic is shown in Figure 5. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more detailed device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

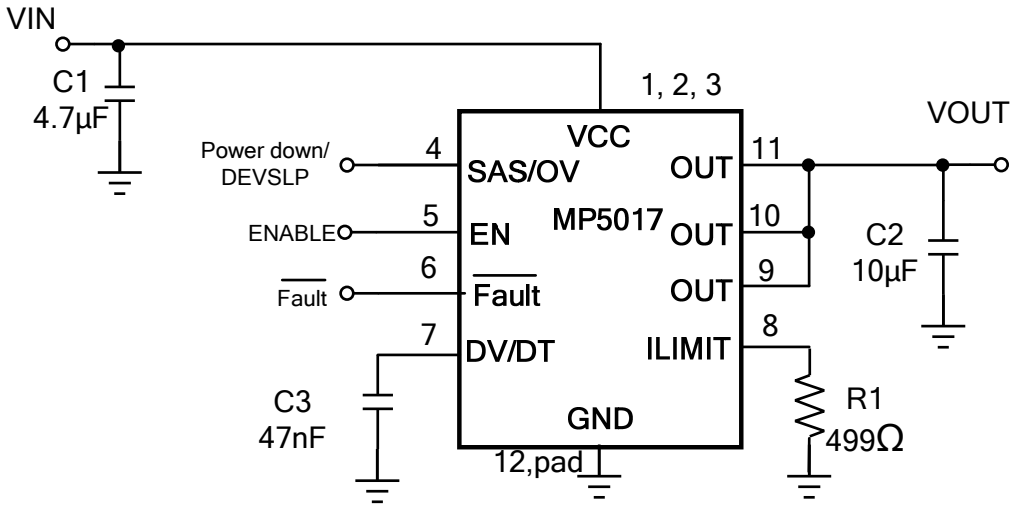

Figure 5: 5V V_{IN} Application

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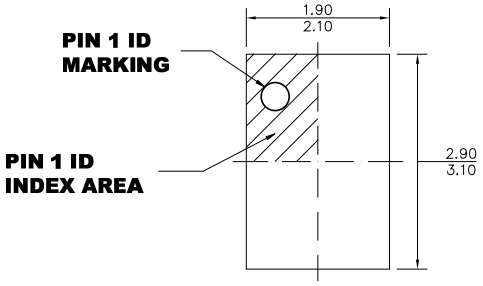
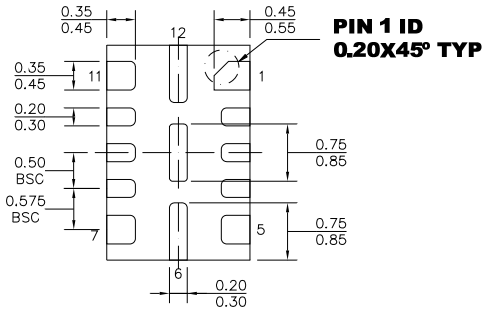
PACKAGE INFORMATION

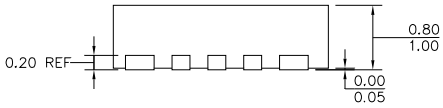
QFN-12 (2mmx3mm)



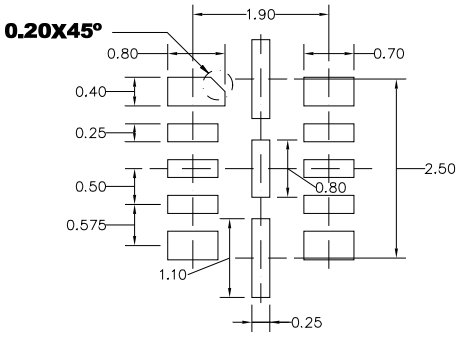
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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