

## DESCRIPTION

The MP5013E is a protection device designed to protect circuitry on the output (source) from transients on the input ( $V_{CC}$ ). It also protects the input from unwanted shorts and transients coming from the source.

A small capacitor on DV/DT controls the slew rate that limits the inrush current at the source. An internal circuit in DV/DT allows it to be floated (no connection) and still receive 1.2ms of ramp time at the source. The maximum load at the source is current-limited using sense FET topology. An external resistor between I-Limit and SOURCE controls the magnitude of the current limit.

An internal charge pump drives the gate of the power device, allowing the DMOS power FET to have a very low on resistance of only 36m $\Omega$ .

The MP5013E protects the source from the input being too low or too high. Under-voltage lockout (UVLO) ensures that the input remains above the minimum operating threshold before the power device turns on. If the input rises above the high output threshold, the MP5013E limits the source voltage.

## FEATURES

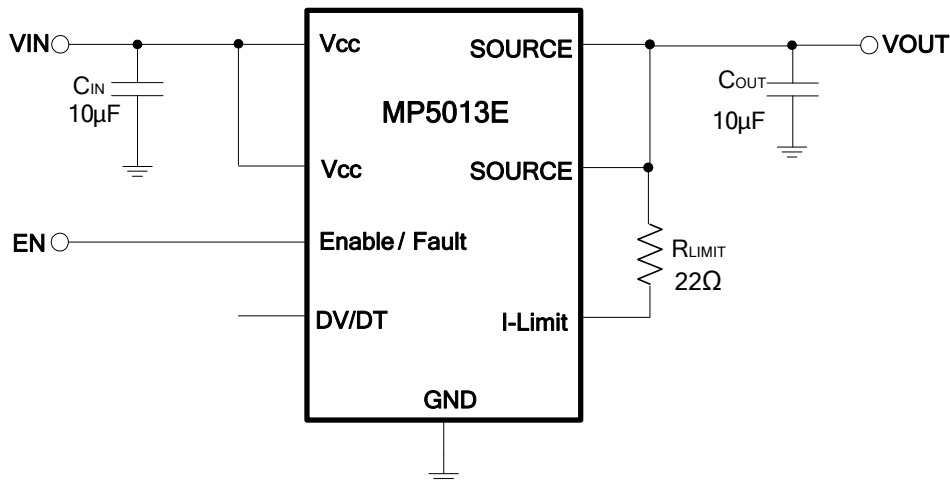
- 3V to 5.5V Operating Input Range
- 2A DC, 5A Peak Current
- 5.7V Typical Output Over-Voltage Clamp
- 22V Absolute Maximum Voltage
- Input Under-Voltage Lockout (UVLO)
- Low Inrush Current during Start-Up
- Integrated 36m $\Omega$  Power FET
- Enable/Fault Pin
- Adjustable Output Voltage Slew Rate
- Adjustable Current Limit
- Thermal Shutdown Protection
- Available in a TSOT23-8 Package

## APPLICATIONS

- Storage (HDDs, SSDs)
- Hot-Swap Systems
- Set-Top Boxes
- USB Ports/Hubs
- Gaming

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

## TYPICAL APPLICATION



**ORDERING INFORMATION**

Part Number*	Package	Top Marking
MP5013EGJ	TSOT23-8	See Below

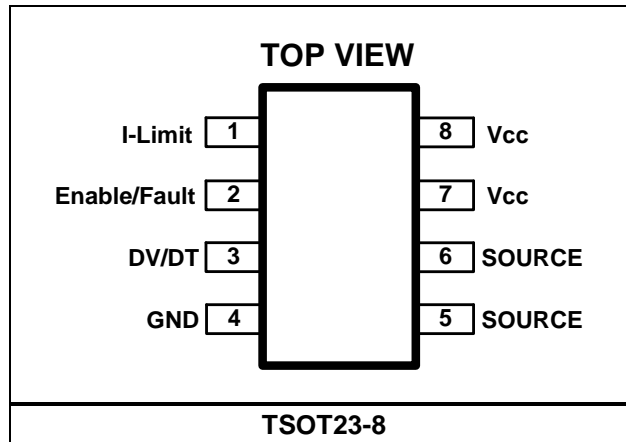
\* For Tape & Reel, add suffix -Z (e.g. MP5013EGJ-Z)

**TOP MARKING**

|AWBY

AWB: Product code of MP5013EGJ  
Y: Year code

**PACKAGE REFERENCE**



**ABSOLUTE MAXIMUM RATINGS (1)**

V<sub>CC</sub>, SOURCE, I-Limit..... -0.3V to 22V  
 DV/DT, Enable/Fault..... -0.3V to 6V  
 Storage temperature..... -65°C to +155°C  
 Junction temperature ..... +150°C  
 Lead temperature ..... +260°C  
 Continuous power dissipation (T<sub>A</sub> = +25°C) (2)  
 ..... 1.25W

**Recommended Operating Conditions (3)**

Input voltage operating range ..... 3V to 5.5V  
 Current capability..... 2A/5A peak  
 (100% duty cycle, and <1s response time)  
 Operating junction temp. (T<sub>J</sub>) ... -40°C to +125°C

Thermal Resistance (4)	$\theta_{JA}$	$\theta_{JC}$
TSOT23-8 .....	100.....	55 ... °C/W

**NOTES:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>, the maximum allowable power dissipation at any ambient temperature is calculated using: P<sub>D</sub>(MAX)=(T<sub>J</sub>(MAX)-T<sub>A</sub>)/  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Reduce 0.1W for every 10°C ambient temperature increase.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7 4-layer board.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$ ,  $R_{LIMIT} = 22\Omega$ , capacitive load =  $10\mu F$ ,  $T_J = 25^\circ C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Power FET</b>						
Delay time	$T_{DLY}$	Enable chip to $I_D = 40mA$ with a $5\Omega$ resistive load, float DV/DT		0.2		ms
On resistance	$R_{DS(ON)}$	$T_J = 85^\circ C^{(5)}$			65	m $\Omega$
Off state output voltage	$V_{OFF}$	$V_{CC} = 18V$ , $V_{EN} = 0V$ , $R_L = 500\Omega$			120	mV
<b>Thermal Latch</b>						
Shutdown temperature <sup>(5)</sup>	$T_{SD}$			175		$^\circ C$
<b>Under- (UVP) and Over-Voltage Protection (OVP)</b>						
Output clamp voltage	$V_{CLAMP}$	Over-voltage protection, $V_{CC} = 8V$	5.5	5.7	5.9	V
Under-voltage lockout	$V_{UVLO}$	Rising edge	2.5	2.7	2.9	V
Under-voltage lockout hysteresis	$V_{HYST}$			0.13		V
<b>Current Limit<sup>(5)</sup></b>						
Hold current	$I_{LIM-SS}$	$0\Omega$ short resistance, $R_{LIM} = 22\Omega$	2.7	3.5	4.3	A
Trip current	$I_{LIM-OL}$	$R_{LIM} = 22\Omega$		6.5		A
<b>DV/DT Circuit</b>						
Rise time	$T_r$	Float DV/DT, output rises from 10% to 90%	0.84	1.2	2.75	ms
<b>Enable/Fault</b>						
Low-level input voltage	$V_{IL}$	Output disabled			0.5	V
Intermediate-level input voltage	$V_{I(INT)}$	Thermal fault, output disabled	0.82	1.3	1.95	V
High-level input voltage	$V_{IH}$	Output enabled	2.5			V
High-state maximum voltage	$V_{I(MAX)}$			4.95		V
Pull-up current (source)	$I_{IL}$	$V_{ENABLE} = 0V$	15	25	35	$\mu A$
Maximum fan-out for Enable/Fault signal		Maximum number of chips for simultaneous shutdown			3	units
Maximum voltage on enable (EN) <sup>(6)</sup>	$V_{MAX}$				$V_{CC}$	V
<b>Total Device</b>						
Bias current	$I_{BIAS}$	Device operational		890	950	$\mu A$
		Enable shutdown		580	650	
		Thermal shutdown		600	700	
Minimum operating voltage for under-voltage lockout	$V_{MIN}$	Enable < 0.5V			2.5	V

**NOTES:**

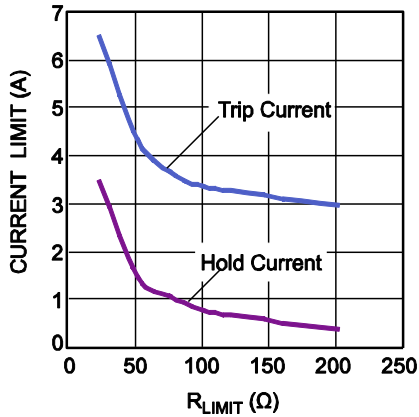
5) Guaranteed by characterization test.

6) Maximum input voltage on Enable/Fault is  $\leq 6V$  if  $V_{CC} \geq 6V$ . Maximum input voltage on Enable/Fault is  $V_{CC}$  if  $V_{CC} \leq 6V$ .

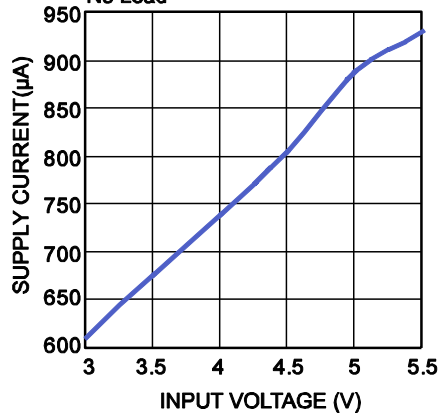
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5V$ ,  $V_{EN} = 5V$ ,  $R_{LIMIT} = 22\Omega$ ,  $C_{OUT} = 10\mu F$ ,  $C_{DV/DT} = \text{float}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

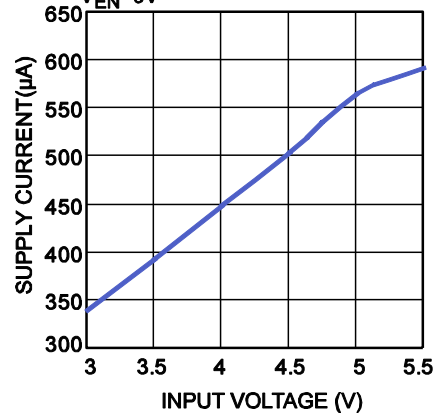
**Trip Current & Hold Current vs.  $R_{LIMIT}$**



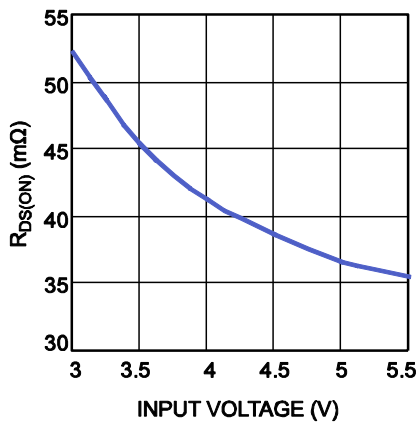
**Supply Current, Output Enable vs. Input Voltage**  
No Load



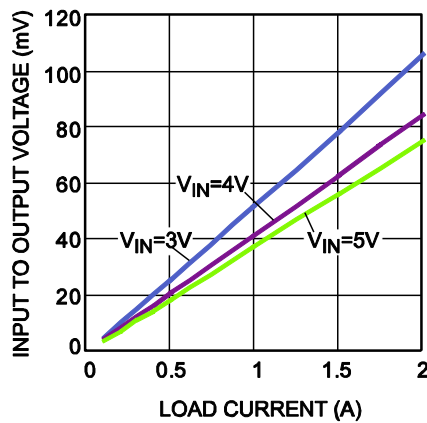
**Supply Current, Output Disable vs. Input Voltage**  
 $V_{EN}=0V$



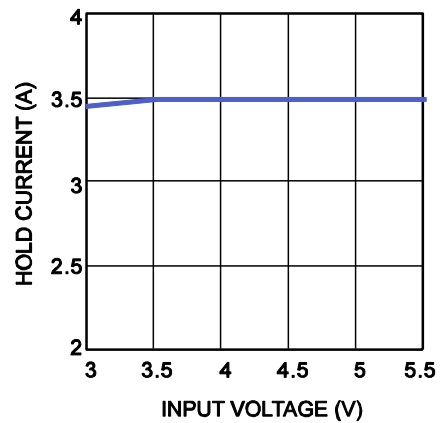
**$R_{DS(ON)}$  vs. Input Voltage**



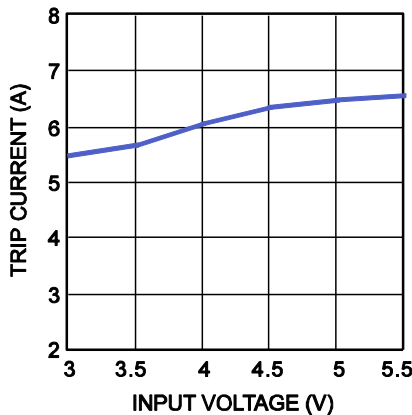
**Input to Output Voltage vs. Load Current**



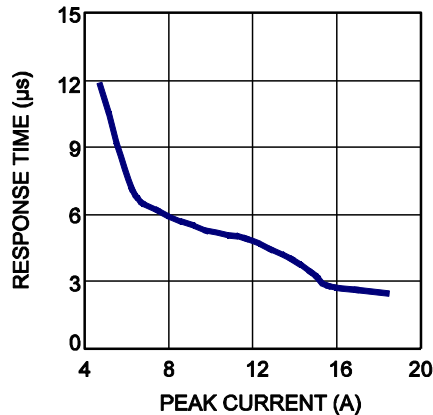
**Hold Current vs. Input Voltage**



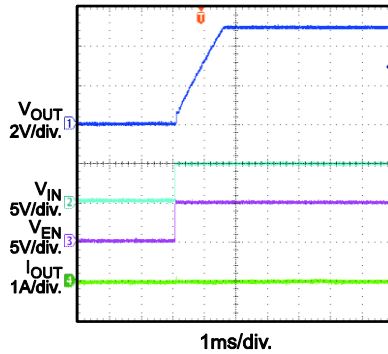
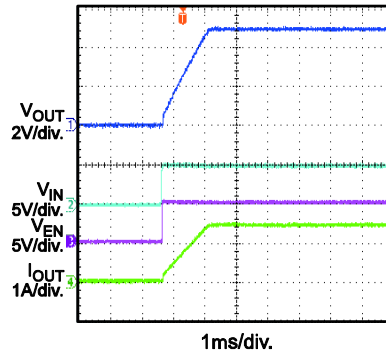
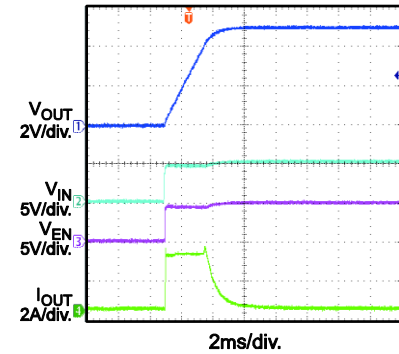
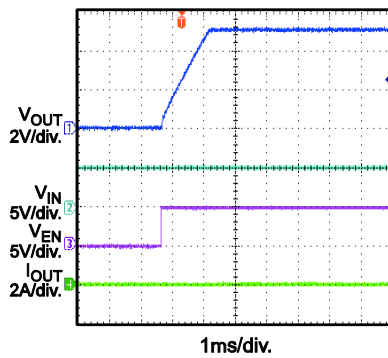
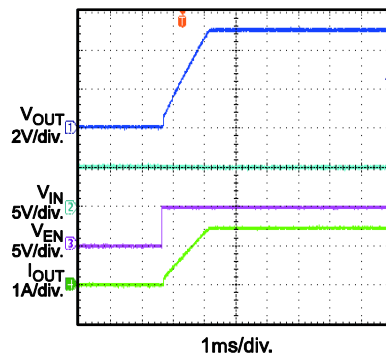
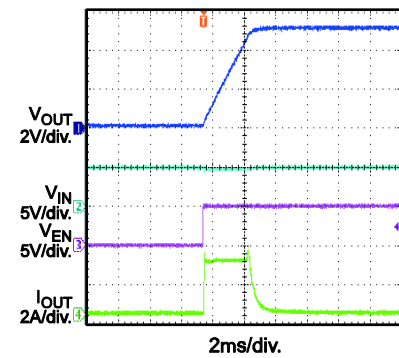
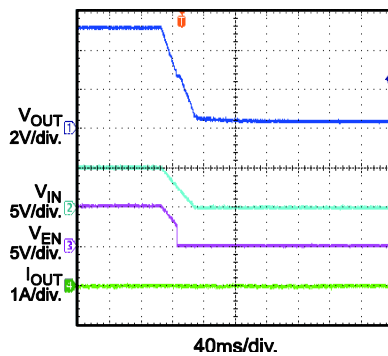
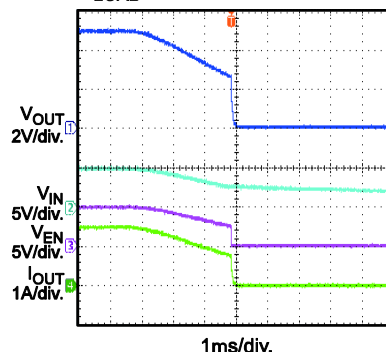
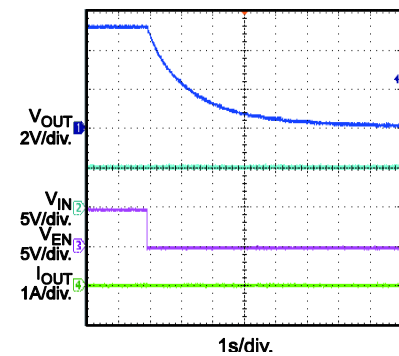
**Trip Current vs. Input Voltage**



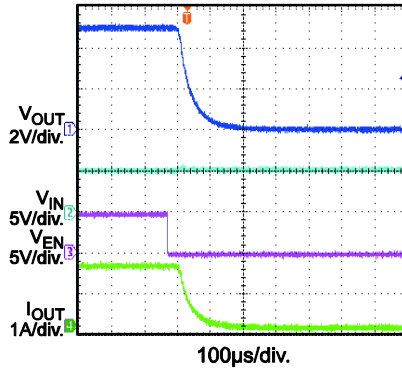
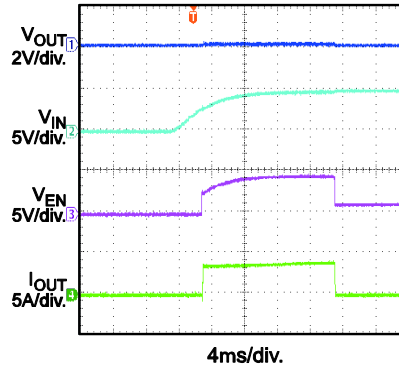
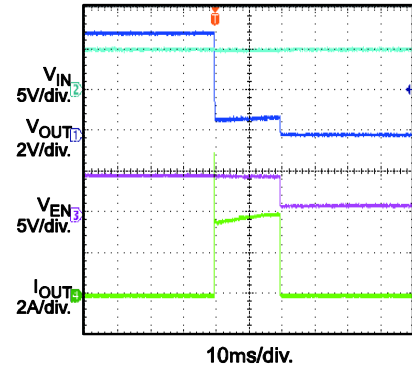
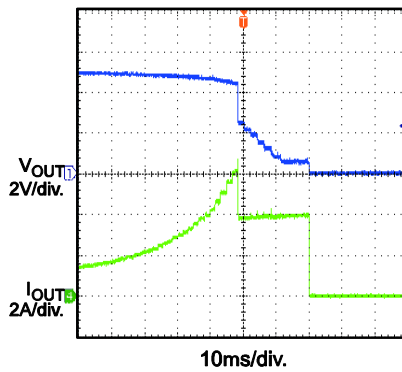
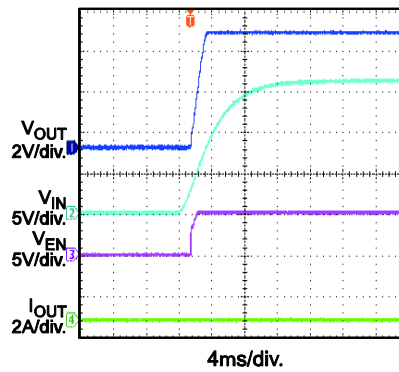
**Current Limit Response vs. Peak Current**



**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*
 $V_{IN} = 5V$ ,  $V_{EN} = 5V$ ,  $R_{LIMIT} = 22\Omega$ ,  $C_{OUT} = 10\mu F$ ,  $C_{DV/DT} = \text{float}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Start-Up through Input Voltage**  
No Load

**Start-Up through Input Voltage**  
 $R_{LOAD} = 3.3\Omega$ 

**Start-Up through Input Voltage**  
 $C_{OUT} = 2200\mu F$ 

**Start-Up through Enable/Fault**  
No Load

**Start-Up through Enable/Fault**  
 $R_{LOAD} = 3.3\Omega$ 

**Start-Up through Enable/Fault**  
 $C_{OUT} = 2200\mu F$ 

**Shutdown through Input Voltage**  
No Load

**Shutdown through Input Voltage**  
 $R_{LOAD} = 3.3\Omega$ 

**Shutdown through Enable/Fault**  
No Load


**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*
 $V_{IN} = 5V$ ,  $V_{EN} = 5V$ ,  $R_{LIMIT} = 22\Omega$ ,  $C_{OUT} = 10\mu F$ ,  $C_{DV/DT} = \text{float}$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Shutdown through Enable/Fault**
 $R_{LOAD} = 3.3\Omega$ 

**Short Circuit before Input Voltage Start-Up and Thermal Shutdown**

**Short Circuit during Normal Operation and Thermal Shutdown**

**Current Limit**

**Start-Up into OVP**
 $V_{IN} = 16V$ 


**PIN FUNCTIONS**

Pin #	Name	Description
1	I-Limit	<b>Current limit.</b> Use a resistor between I-Limit and SOURCE to set the overload and short circuit current-limit levels.
2	Enable/Fault	<b>Enable/fault.</b> Enable/Fault is a tri-state, bidirectional interface. Leave Enable/Fault floating to enable the output. Pull Enable/Fault to ground using an open drain or open collector device to disable the output. If a thermal fault occurs, Enable/Fault enters an intermediate state to signify that the device is in thermal shutdown.
3	DV/DT	<b>Output voltage slew rate.</b> The internal DV/DT circuit controls the slew rate of the output voltage during start-up. DV/DT has an internal capacitor that allows it to ramp up in 1.2ms. An external capacitor can be added to DV/DT to increase the ramp time. If an additional time delay is not required, leave DV/DT open.
4	GND	<b>Ground.</b> GND is the internal IC reference.
5, 6	SOURCE	<b>Source.</b> SOURCE is the internal power FET source. SOURCE is an IC output.
7, 8	V <sub>CC</sub>	<b>Input.</b> V <sub>CC</sub> is the positive input voltage.

BLOCK DIAGRAM

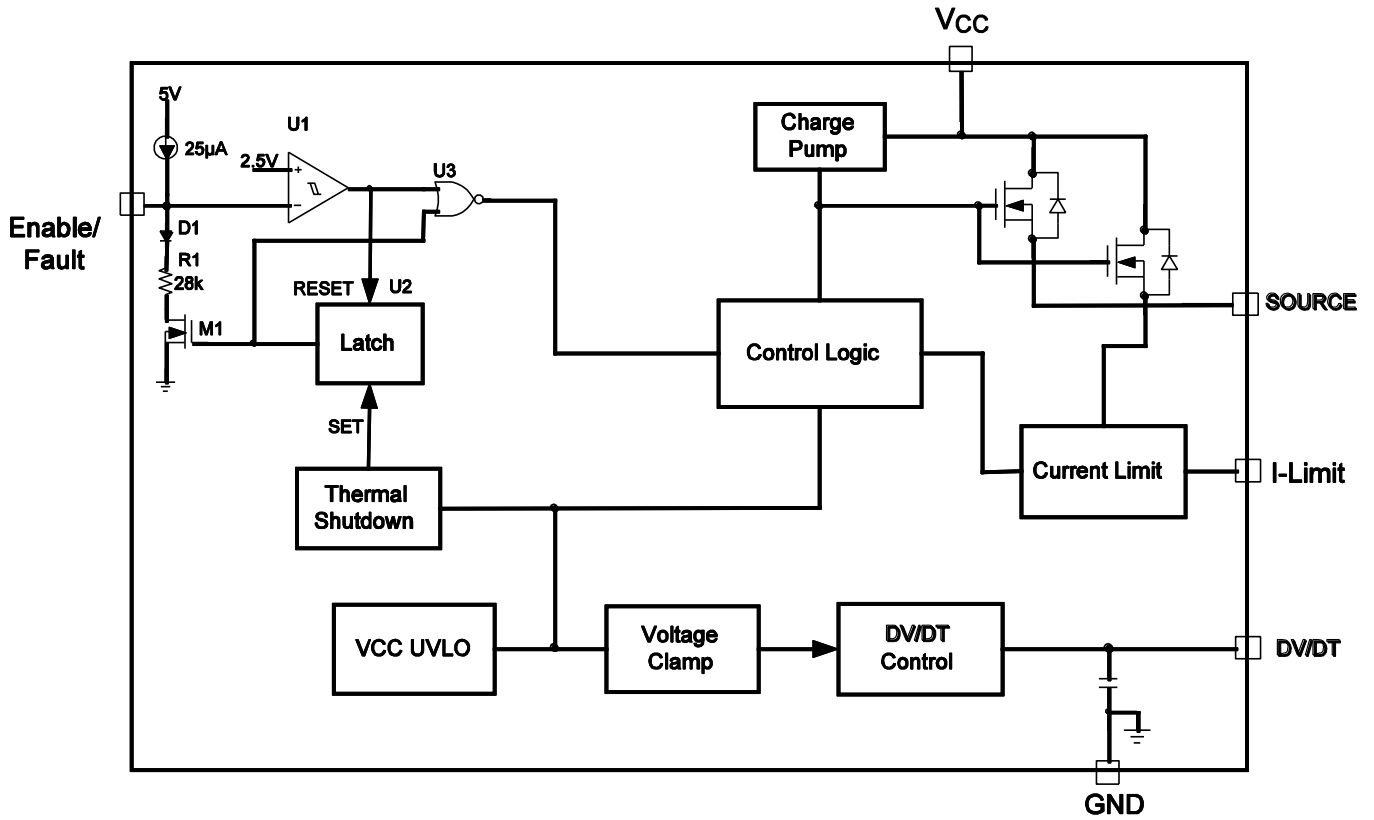


Figure 1: Functional Block Diagram



## OPERATION

The MP5013E limits the inrush current to the load when a circuit card connects to a live backplane power source, thereby limiting the backplane's voltage drop and the DV/DT of the voltage to the load. The MP5013E offers an integrated solution to monitor the input voltage, output voltage, output current, and die temperature while eliminating the external current-sense power resistor, power MOSFET, and thermal sensor.

### Under-Voltage Lockout (UVLO) Operation

If the supply (input) is below the under-voltage lockout (UVLO) threshold, the output is disabled, and the Enable/Fault line is driven low. When the supply rises above the UVLO threshold, the output is enabled, and Enable/Fault is pulled high through a 25 $\mu$ A current source without an external pull-up resistor. The pull-up voltage is limited to 4.95V.

### Output Over-Voltage Protection (OVP)

If the input voltage exceeds the over-voltage protection (OVP) threshold, the output is clamped at 5.7V, typically.

### Current Limiting

When the chip is active, if the load reaches the over-current protection (OCP) threshold (trip current) or a short is present, the MP5013E switches to constant-current mode (hold current). The MP5013E shuts down only if the over-current condition triggers thermal protection. However, when the MP5013E is powered up by  $V_{CC}$  or enable (EN), the load current should be smaller than the hold current. Otherwise, the part cannot be fully turned on.

In a typical application with a 22 $\Omega$  current-limiting resistor, the trip current is 6.5A, and the hold current is 3.5A. If the MP5013E is in normal operation and passes 2.0A, it only needs to dissipate 144mW with a low 36m $\Omega$  on resistance. For a package dissipation of 100 $^{\circ}$ C/W, the temperature rise is +14 $^{\circ}$ C. Given a 25 $^{\circ}$ C ambient temperature, the typical package temperature is 39 $^{\circ}$ C.

The MP5013E requires a heat sink during constant-current mode (i.e.: from a short circuit) to prevent an unwanted shutdown. During a short-circuit condition, the MP5013E must dissipate the power from a 5V drop. Without additional heat dissipation at 100 $^{\circ}$ C/W, the temperature exceeds the thermal threshold (+175 $^{\circ}$ C), and the MP5013E shuts down to force the temperature to drop.

### Thermal Protection

If the temperature exceeds the thermal threshold, the MP5013E disables its output and drives the Enable/Fault line to middle (mid) level (see the following Enable/Fault section for more detail). The thermal fault condition is latched, and the MP5013E remains in a latched-off state until the power is restarted or Enable/Fault is reset.

### Enable/Fault

Enable/Fault is a bidirectional, three-level I/O pin with a weak pull-up current (typically 25 $\mu$ A). The three levels are low, mid, and high. The Enable/Fault functions enable or disable the MP5013E and relay fault information.

When Enable/Fault functions as an input, low and mid levels disable the MP5013E. A low level can also clear the fault flag. A high level enables the MP5013E if the fault flag is clear.

When Enable/Fault functions as an output, the pull-up current allows a wired-NOR pull-up to enable the MP5013E if the current is not overridden. An under-voltage condition causes a low level on Enable/Fault and clears the fault flag. A thermal fault sets a mid level on Enable/Fault and sets the fault flag.

The Enable/Fault line must remain high for the output to turn on.

The fault flag is an internal flip-flop that can be set or reset under the following conditions:

- Thermal shutdown: set fault flag.
- Under-voltage: reset fault flag.
- Low on Enable/Fault: reset fault flag.
- Mid on Enable/Fault: no effect.

Under thermal shutdown, Enable/Fault is driven to mid level.

There are four types of faults. Each fault has a direct and indirect effect on Enable/Fault and the internal fault flag (see Table 1). In a typical application, there are one or more MP5013E chips in a system. The Enable/Fault lines are connected together, typically.

**Table 1: Fault Function Influence in Application**

Fault Description	Internal Action	Effect on Enable/Fault	Effect on Flag	Effect on Secondary Part
Short/over current	Limit current	None	None	None
Under voltage	Output turns off	Internally drives Enable/Fault to logic low	Flag is reset	Disables secondary output and resets fault flag
Over voltage	Limit output voltage	None	None	None
Thermal shutdown	Shutdown. The MP5013E is latched off or until UVLO is driven to ground externally.	Internally drives Enable/Fault to mid	Flag is set	Disables secondary part output

## APPLICATION INFORMATION

### Current Limit

The current limit is a function of the external current-limit resistor. Table 2 lists some current values as a function of the resistor value.

**Table 2: Current Limit vs. Current Limit Resistor**  
( $V_{CC} = 5V$ )

$R_{LIMIT} (\Omega)$	22	51	75	100	220
<b>Trip Current (A)</b>	6.5	4.3	3.7	3.38	3
<b>Hold Current (A)</b>	3.5	1.5	1.1	0.81	0.4

### Rise Time

The rise time is a function of the capacitor ( $C_{DV/DT}$ ) on DV/DT. Table 3 lists typical rise times as a function of the capacitance.

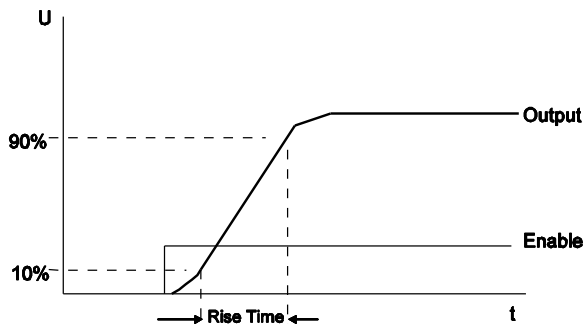
**Table 3: Rise Time vs.  $C_{DV/DT}$**

$C_{DV/DT}$	none	150pF	470pF	1nF
<b>Rise Time (ms)</b>	1.2	5.7	15.3	31.2

Calculate the rise time with Equation (1):

$$\text{Risetime (ms)} = 0.03\text{ms} * C_{DV/DT} (\text{pF}) + 1.2\text{ms} (1)$$

The rise time is measured from 10% to 90% of the output voltage (see Figure 2).

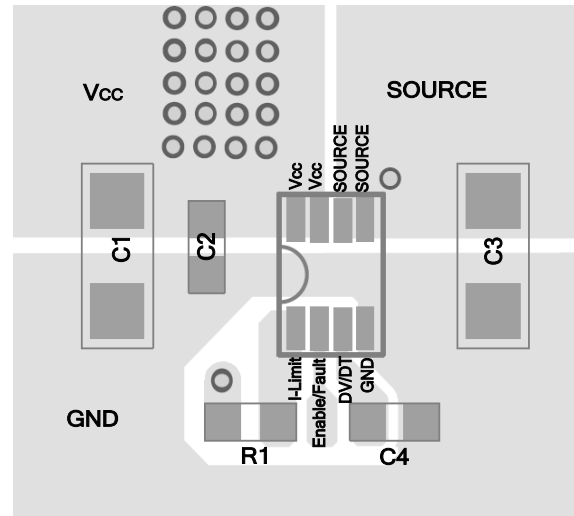


**Figure 2: Rise Time**

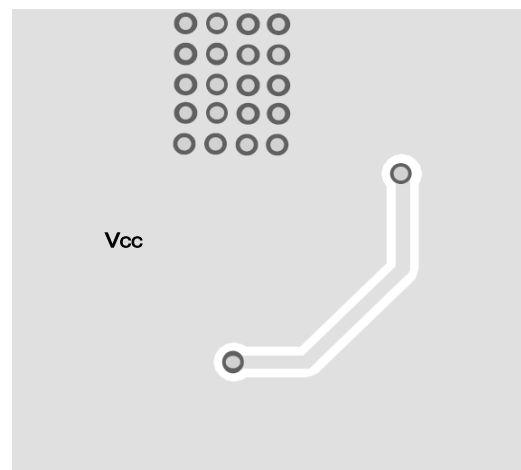
### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 3 and follow the guidelines below.

1. Place  $R_{LIMIT}$  close to I-Limit.
2. Place  $C_{DV/DT}$  close to DV/DT.
3. Place the input capacitor close to  $V_{CC}$ .
4. Place enough copper area near  $V_{CC}$  and SOURCE for thermal dissipation.



**Top Layer**



**Bottom Layer**

**Figure 3: Recommended PCB Layout**

### Design Example

Table 4 is a design example following the application guidelines for the specifications below.

**Table 4: Design Example**

$V_{IN}$	5V
<b>Trip Current</b>	6.5A
<b>Hold Current</b>	3.5A

Figure 4 shows the typical application schematic. The Typical Performance Characteristics section shows the circuit waveforms. For more device applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUIT

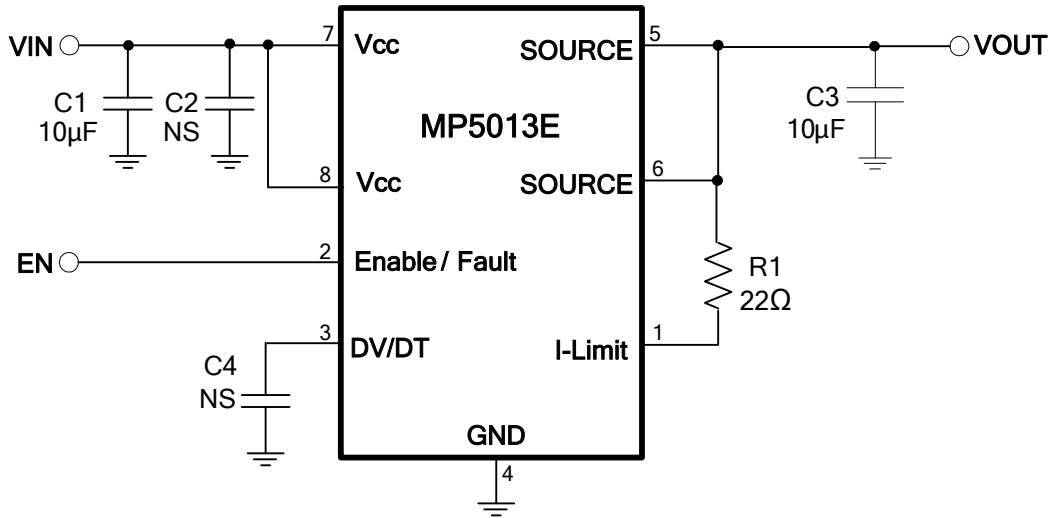
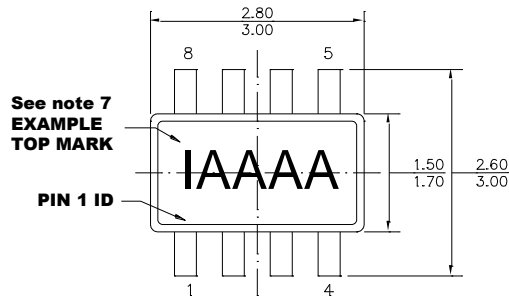


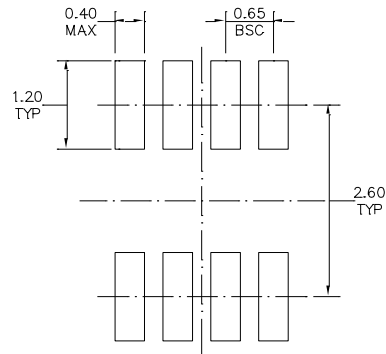
Figure 4: Typical Application Schematic

PACKAGE INFORMATION

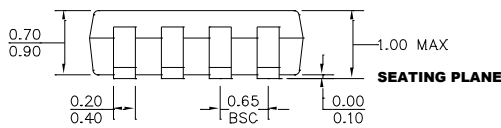
TSOT23-8



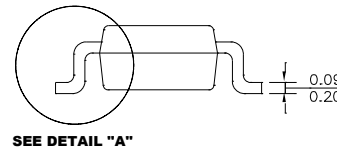
**TOP VIEW**



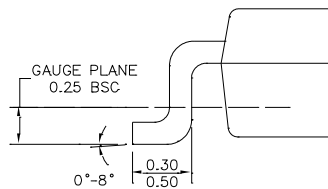
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



**DETAIL "A"**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-193, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

**NOTICE:** The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.