MP5006

5V, 1A- 5A Programmable Current Limit Switch with Slew Rate Control and Auto Enable

The Future of Analog IC Technology

DESCRIPTION

The MP5006 is a protection device designed to protect circuitry on the output (V_{OUT}) from transients on input (V_{IN}). It also protects V_{IN} from undesired shorts and transients coming from the load.

At start up, inrush current is controlled by limiting the slew rate at the V_{OUT}. The slew rate is controlled by a small capacitor at the dv/dt pin. The dv/dt pin has an internal circuit that allows the customer to float this pin (no connect) and still receive a 1.1ms ramp time at the V_{OUT}.

The max load at the output (V_{OUT}) is current limited. This is accomplished by utilizing a sense FET topology. The magnitude of the current limit is controlled by an external resistor connected between the I_{LIMIT} pins.

An internal charge pump drives the gate of the power device, allowing a very low on-resistance DMOS power FET of just 0.044Ω.

V_{OUT} is protected from V_{IN} being too low or too high. Under Voltage Lockout (UVLO) assures that the input is above the minimum operating threshold, before the power device is turned on. If V_{IN} goes above the high output threshold, the output voltage will be limited.

FEATURES

- Integrated 44mΩ Power FET
- Enable/Fault Pin
- Adjustable Slew Rate for Output Voltage
- Adjustable Current Limit
- Automatic Startup/Retry after Thermal Protection
- Over Voltage Limit

APPLICATIONS

- Hot Swap
- PC Cards
- Laptops
- SSD
- HDD

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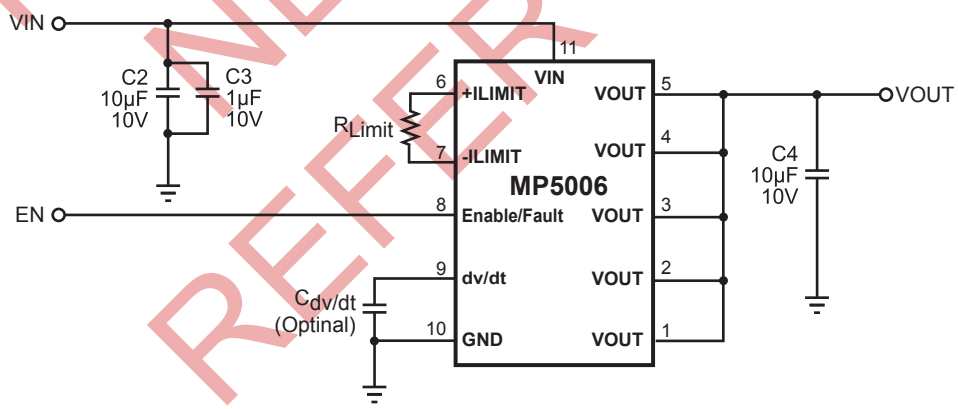
TYPICAL APPLICATION



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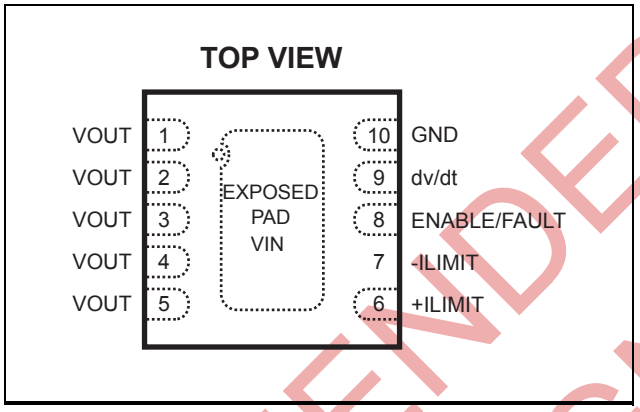
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP5006EQ	QFN10 (3x3)	8M	–20°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP5006EQ–Z).
For RoHS Compliant Packaging, add suffix –LF (e.g. MP5006EQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{OUT}, $+I_{LIMIT}$, $-I_{LIMIT}$ 22V
dv/dt, ENABLE/FAULT 6V
Junction Temperature..... –20°C to +150°C
Continuous Power Dissipation (T_A=+25°C) (2)
.....2.5W
Storage Temperature..... –65°C to +155°C

Recommended Operating Conditions

Input Voltage Operating Range ..... 4V to 10V
Operating Junct. Temp (T_J)..... –20°C to +125°C

Thermal Resistance (3) ..... θ_{JA} θ_{JC}

QFN10	50	12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A the maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
Reduce 0.2 Watts for every 10°C ambient temperature increasing
3) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{IN} =5V, R_{LIMIT}=24Ω, C_{OUT}=10μF, T_J=25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power FET						
Delay Time	t_{DLY}	Enabling of chip to I_D=100mA with a 12Ω resistive load		0.2		ms
ON Resistance	R_{DSon}	T_J=25°C		44	82	mΩ
		T_J=80°C, Note 4		95		
Off State Output Voltage	V_{OFF}	V_{IN} =18Vdc, Enable=0V, R_L=500Ω			120	mV
Continuous Current	I_D	0.5 in^2 pad, Note 4, T_J=25°C		4.2		A
		minimum copper, T_J=80°C		2.3		
Thermal Shutdown						
Shutdown Temperature	T_{SD}	Note 4		175		°C
Under/Over Voltage Protection						
Output Clamping Voltage	V_{CLAMP}	Over Voltage Protection V_{IN} =8V	5	5.4	5.9	V
Under Voltage Lockout	V_{UVLO}	Turn on, Voltage going high	3.2	3.6	4.0	V
Under Voltage Lockout (UVLO) Hysteresis	V_{HYST}			0.2		V
Current Limit						
Hold Current	I_{LIM-SS}	R_{LIMIT}=24Ω, Note 4	1.2	1.55	1.9	A
Trip Current	I_{LIM-OL}	R_{LIMIT}=24Ω, Note 4	2.3	3	3.7	A
dv/dt Circuit						
Rise Time	T_r	Float dv/dt pin, Note 5	0.64	1.1	2.0	ms
Enable/Fault						
Low Level Input Voltage	V_{IL}	Output Disabled			0.5	V
High Level Input Voltage	V_{IH}	Output Enabled	2.5			V
High State Maximum Voltage	$V_{I\ (MAX)}$			4.8		V
Low Level Input Current (Sink)	I_{IL}	V_{ENABLE}=0V		-60	-80	μA
Maximum Fanout for Fault Signal		Total number of chips that can be connected for simultaneous shutdown			5	Units
Maximum Voltage on Enable Pin	V_{MAX}	Note 6			V_{IN}	V
Total Device						
Bias Current	I_{BIAS}	Device Operational		1.5	2.0	mA
		Thermal Shutdown		1		
Minimum Operating Voltage for UVLO	V_{MIN}	Enable<0.5V			3.0	V

Notes:

4) Guaranteed by design.
5) Measured from 10% to 90%.
6) Maximum Input Voltage to be ≤ 6V if V_{IN} > 6V. Maximum Input Voltage to be V_{IN} if V_{IN} ≤ 6V.

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PIN FUNCTIONS

Pin #	Name	Description
1-5	VOUT	This pin is the V_{OUT} of the internal power FET and the output terminal of the IC.
6	+ILIMIT	A resistor between these pins sets the overload and short circuit current limit levels.
7	-ILIMIT	A resistor between these pins sets the overload and short circuit current limit levels.
8	Enable/Fault	The Enable/Fault pin is a bi-directional interface. It can be used to enable the output of the device by floating the pin, or disable the chip by pulling it to ground (using an open drain or open collector device). If a thermal fault occurs, the voltage on this pin will drive to ground, automatically.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over the period of 1.1ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
10	GND	Negative Input Voltage to the Device. This is used as the internal reference for the IC.
11	VIN	Positive input voltage to the device (Exposed Pad).

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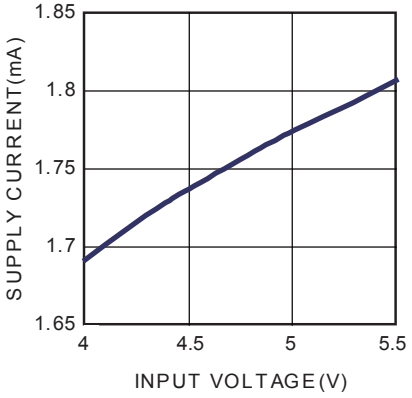
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =5V, V_{EN} =3.3V, R_{LIMIT}=24Ω, C_{OUT} =10μF, $C_{dv/dt}$ =1nF, T_A =25°C, unless otherwise noted.

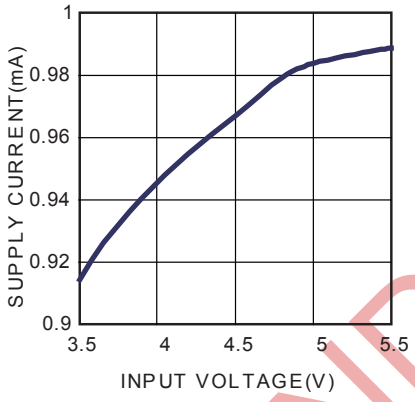
Supply Current,Output Enabled vs.Input Voltage

No load, EN floating



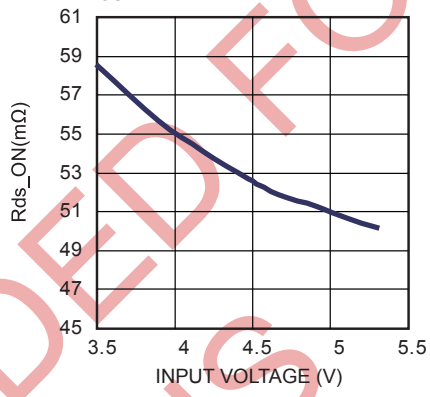
Supply Current,Output Disabled vs.Input Voltage

V_{EN}=0V



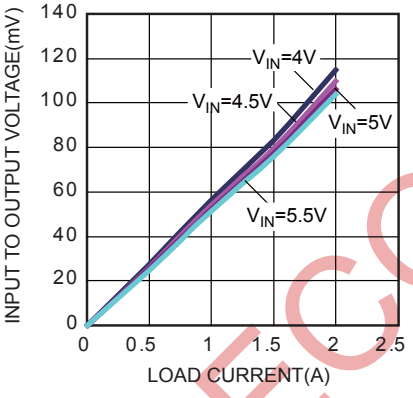
Static Drain-Source On-State Resistance vs. Input Voltage

I_{OUT}=1A



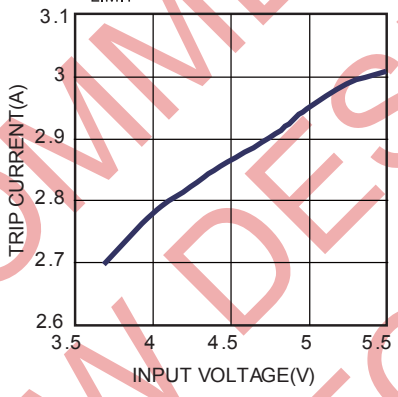
Input to Output Voltage vs. Load Current

R_{LIMIT}=24Ω



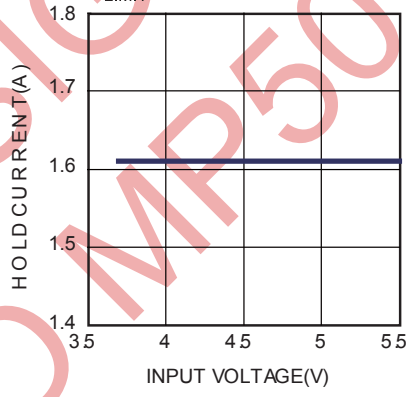
Threshold Trip Current vs. Input Voltage

R_{LIMIT}=24Ω



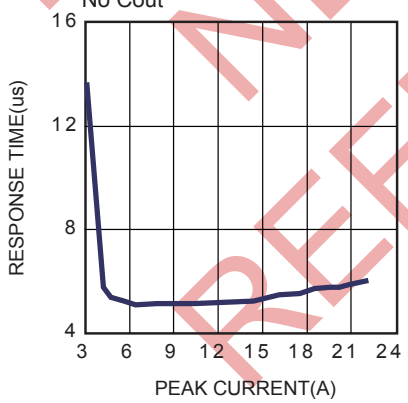
Hold Current vs. Input Voltage

R_{LIMIT}=24Ω

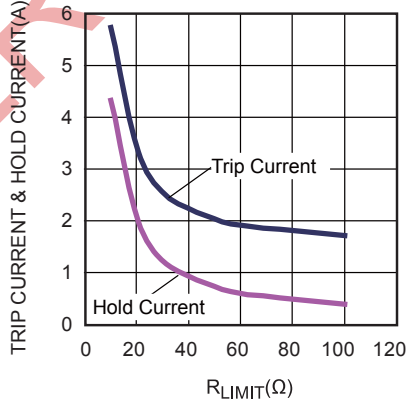


Current Limit Response vs. Peak Current

No Cout



Trip and Hold Current vs. R_{LIMIT}



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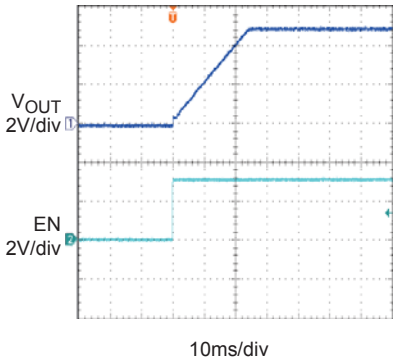
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =5V, V_{EN} =3.3V, R_{LIMIT}=24Ω, C_{OUT} =10μF, $C_{dv/dt}$ =1nF, T_A =25°C, unless otherwise noted.

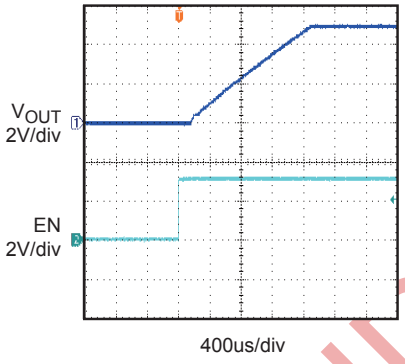
Turn on Delay and Rise Time

Cdv/dt=1nF,C_{OUT}=10uF,no load



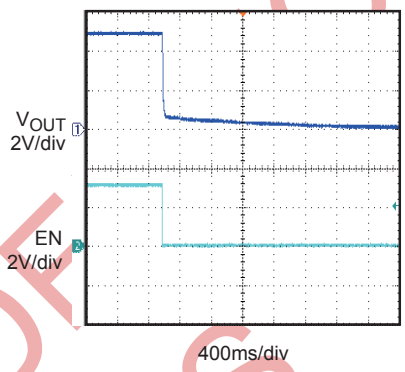
Turn on Delay and Rise Time

No Cdv/dt,C_{OUT}=10uF,no load



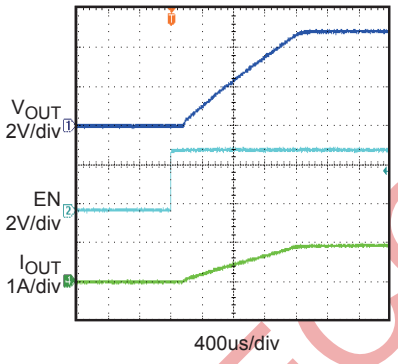
Turn off Delay and Fall Time

No Cdv/dt,C_{OUT}=10uF,no load



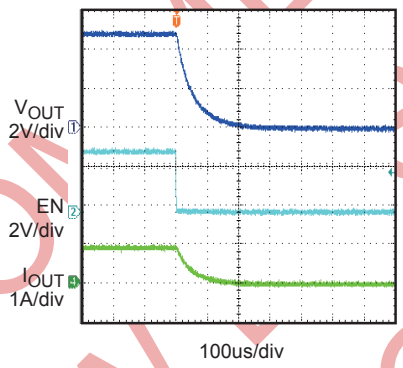
Turn on Delay and Rise Time

No Cdv/dt,C_{OUT}=10uF, R_{LOAD}=5Ω



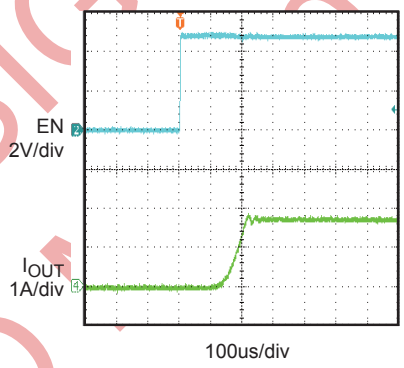
Turn off Delay and Fall Time

No Cdv/dt,C_{OUT}=10uF, R_{LOAD}=5Ω



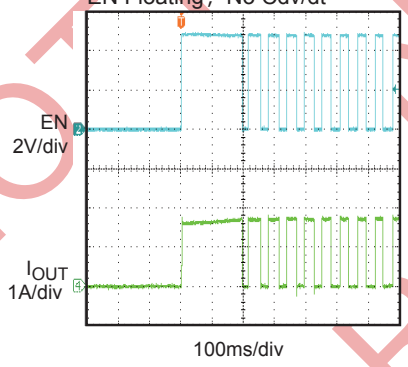
Short Circuit Current, Device Enabled into Short

No Cdv/dt



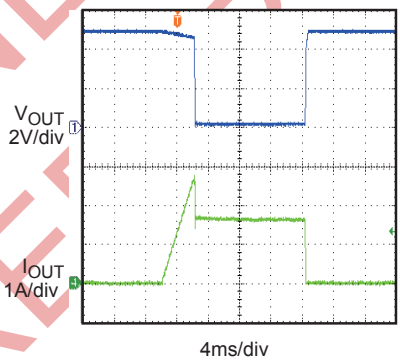
Short Circuit Current, Device Enabled into Short, and Thermal Shut down and Auto Start Up

EN Floating, No Cdv/dt



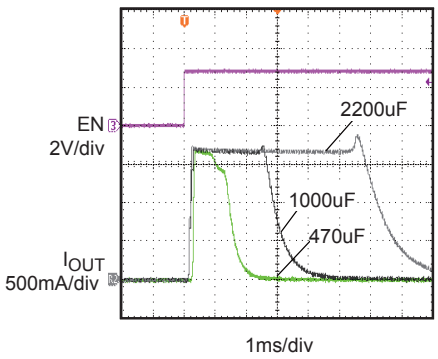
Trip Current with Ramped Load on Enabled Device

No Cdv/dt



Inrush Current with Different Load Capacitance

No Cdv/dt



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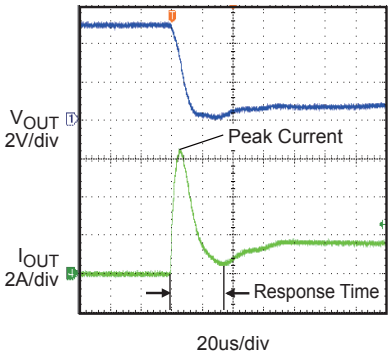
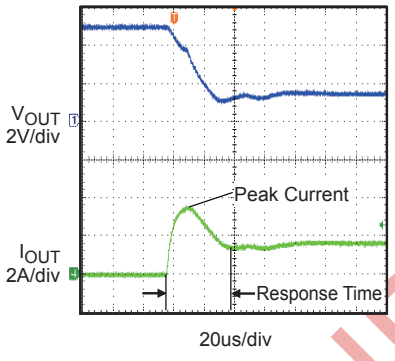
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =5V, V_{EN} =3.3V, R_{LIMIT}=24Ω, C_{OUT} =10μF, $C_{dv/dt}$ =1nF, T_A =25°C, unless otherwise noted.

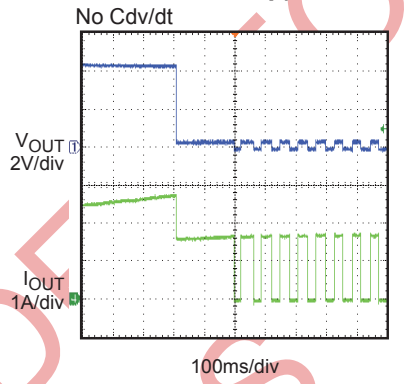
0.33Ω Load Connected to Enabled Device
No Cdv/dt, No C_{OUT}



0.66Ω Load Connected to Enabled Device
No Cdv/dt, No C_{OUT}



Current Limit (trip→hold→thermal shut down) →Auto Start Up)
No Cdv/dt



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BLOCK DIAGRAM

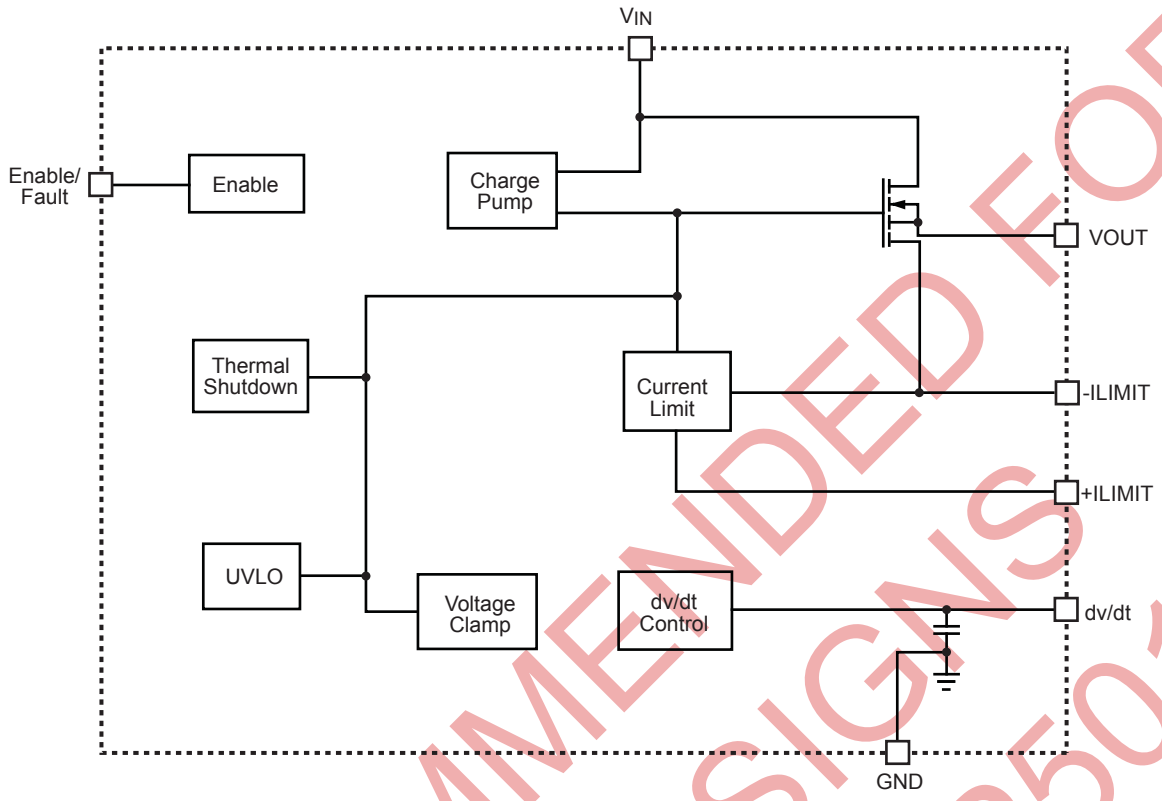

Figure 1—Function Block Diagram

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CURRENT LIMIT

The desired current limit is a function of the external current limit resistor.

Table 1—Current Limit vs. Current Limit Resistor (V_{IN} =5V)

Current Limit Resistor (Ω)	24	50	75	100
Trip Current (A)	3	2	1.78	1.67
Hold Current (A)	1.55	0.76	0.5	0.38

When the part is active, if load reaches trip current (minimum threshold current triggering overcurrent protection) or a short is present, the part switches into to a constant-current (hold current) mode. Part will enter thermal cycling only if the overcurrent condition stays long enough to trigger thermal protection.

However, when the part is powered up by V_{CC} or EN, the load current should be smaller than hold current. Otherwise, the part can't be fully turned on.

In a typical application using a current limit resistor of 24Ω, the trip current will be 3A and the hold current will be 1.55A. If the device is in its normal operating state and passing 1.55A it will need to dissipate only 105.7mW with the very low on resistance of 44mΩ. For the package dissipation of 50°C/Watt, the temperature rise will only be + 5.3°C. Combined with a 25°C ambient, this is only 30.3°C total package temperature.

During a short circuit condition, the device now has 5V across it and the hold current clamps at 1.55A and therefore must dissipate 7.75W. At 50°C/watt, if uncontrolled, the temperature would rise above the MP5006 thermal protection (+175°C) and shutdown the device to cause the temperature to drop below a hysteresis level. Proper heat sink must be used if the device is intended to supply the hold current and not shutdown. Without a heat sink, hold current should be maintained below 600mA at + 25°C and below 360mA at +85°C to prevent the device from activating the thermal shutdown.

RISE TIME

The rise time is a function of the capacitor ($C_{dv/dt}$) on the dv/dt pin.

Table 2—Rise Time vs. Cdv/dt

$C_{dv/dt}$	none	50pF	500pF	1nF
Rise Time* (TYPICAL) (ms)	1.1	2.2	12.3	23.5

* **Notes:** Rise Time = K_{RT}*(50pF+Cdv/dt), K_{RT} =22E6

The "rise time" is measured by from 10% to 90% of output voltage.

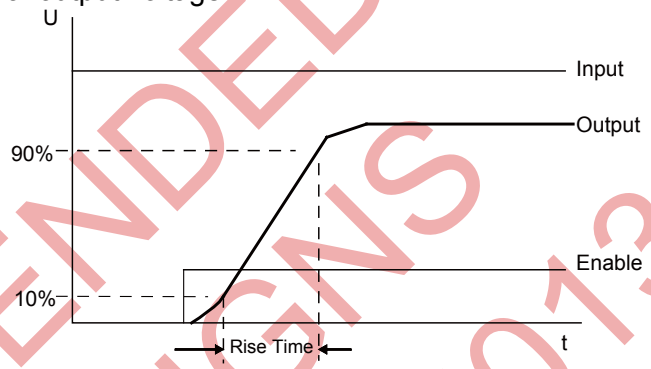

Figure 2—Rise Time

FAULT AND ENABLE PIN

The Enable/Fault Pin is a Bi-Directional I/O with a weak pull up current (25uA typical). It functions to enable/disable the part.

Enable pin as an input:

1. Low disables the part.
2. High enables the part.

Enable pin as an output:

1. The pull up current may (if not over ridden) allow a "wired nor" pull up to enable the part.
2. An under voltage will cause a low on the enable pin.
3. A thermal fault will cause a low level on the enable pin.

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There are 4 types of faults, and each fault has a direct and indirect effect on the Enable/Fault pin and the internal fault flag. In a typical application there are one or more of the MP5006 chips in a system. The Enable/Fault lines will typically be connected together.

Table 3—Fault Function Influence in Application

Fault description	Internal action	Effect on Fault Pin	Effect on Flag	Effect on secondary Part
Short/over current	Limit current	none	None	none
Under Voltage	Output is turned off	Internally drives Enable/Fault pin to Logic low	Flag is reset	Secondary part output is disabled, and fault flag is reset.
Over Voltage	Limit output voltage	None	None	None
Thermal Shutdown	Shutdown part. The part retries to start up automatically	Internally drives Enable/Fault pin to low level, and after part cools down, Enable/Fault pin will be pulled high	Flag is set at thermal shut down, and is set to high after auto start up.	Secondary part output is disabled when thermal shut down, and is enabled after MP5006 auto start up.

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THERMAL PROTECTION

The MP5006 only considers a thermal overload to be a fault. Under a fault condition the mp5006 will have two actions:

1) Turn off the output power device.
2) Drive the enable/fault pin to the low level.

The power device will remain off until the die temperature drops below the hysteresis level.

When the die cools down below the thermal hysteresis level, the MP5006 will restart in the start up mode and the fault line will be pulled high through a 25uA pull up current. If the cause of the fault has been removed, the output will ramp up in a controlled fashion with the ramp rate controlled by the dv/dt function. If the cause of the fault is still present, the excess power dissipation will heat up the part. When the die temperature reaches the thermal shutdown temperature, the output will be turned off and the enable/fault pin will be driven to the low level, again. This cycle will repeat until the cause of the fault is removed.

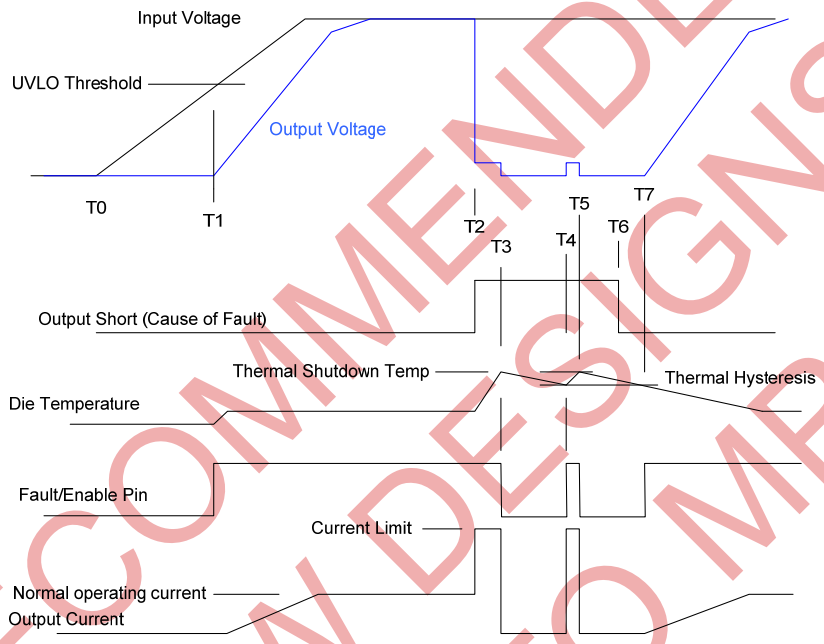

Figure 3—Thermal Protection in Short Condition

The drawing above shows the initial start up sequence and the occurrence of a short at the output.

At time T0 the input voltage begins to rise. At T1 the input voltage rises above the UVLO threshold and the part starts up. The output current ramps up and settles at the normal operating current level until time T2. There is a very small temperature heating of the die in normal operation.

At time T2 the output is shorted. This brings the output very close to ground. The output current increases to the current limit level and is held there by the MP5006. Because of the large current and the large voltage across the power device, the die will begin to heat up.

At time T3 the die temperature is at the thermal shutdown level and the part will turn the power device off. The enable/fault pin is driven to the low level. Once the power device is off, the die temperature will begin to drop.

At time T4 the part has cooled down below the thermal hysteresis level. The enable pin goes high and the part turns on again. But the short is still present, causing the die temperature to increase.

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At time T5 the power device turns off and the Enable/Fault pin is driven to the low level, again. The temperature begins to fall.

The cycle between times T3, T4 and T5 could repeat indefinitely, but at time T6 the short is removed. At time T7 the die temperature is below the thermal hysteresis level and the part turns on once again. This time there is no short, so the output starts in normal operation and the die temperature cools down to the normal operating range.

UNDER VOLTAGE LOCK OUT OPERATION

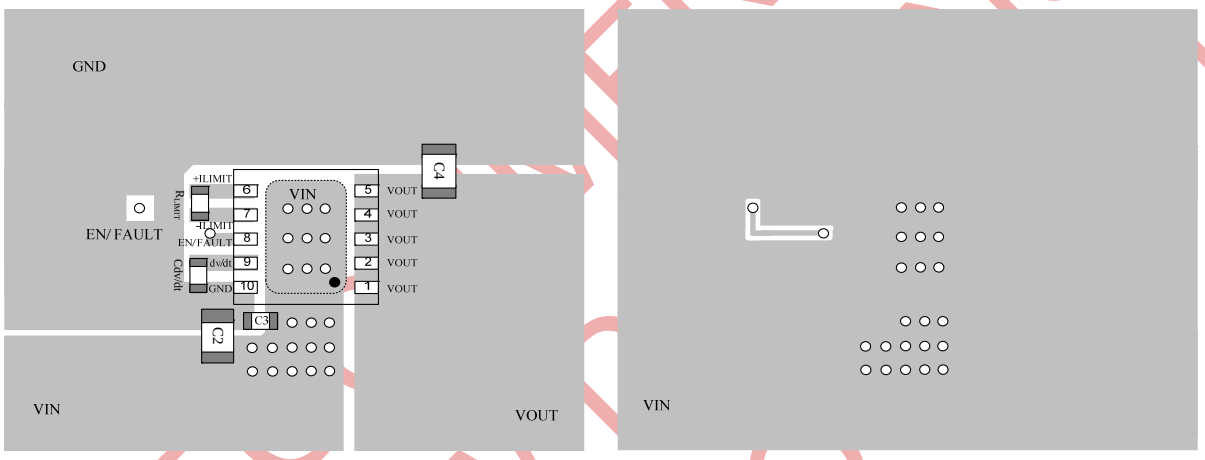
If the supply (input) is below the UVLO threshold, the output is disabled, and the fault line is driven low.

When the supply goes above the UVLO threshold, the output is enabled and the Enable/fault pin is released. When the Enable/fault pin is released it will be pulled high by a 25uA current V_{OUT}. No external pull up resistor is required. In addition, the pull up voltage is limited to 5 volts.

PCB LAYOUT

PCB layout is very important to achieve stable operation. Please follow these guidelines and take below Figure for reference.

Place Rlimit close to Ilimit pin, Cdv/dt close to dv/dt pin and input cap close to VIN (Exposed Pad). Keep the N/C pin float. Put vias in thermal pad and ensure enough copper area near VIN and VOUT to achieve better thermal performance.



Top Layer **Bottom Layer**

Figure 4—PCB Layout

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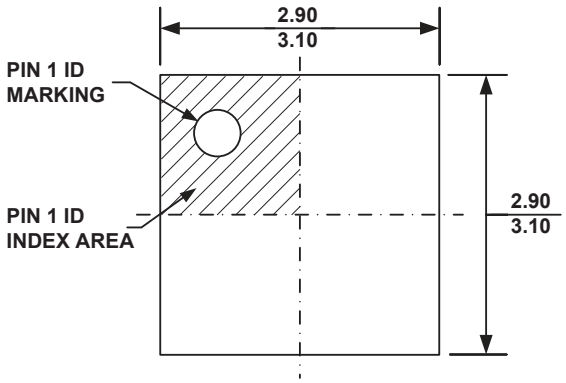
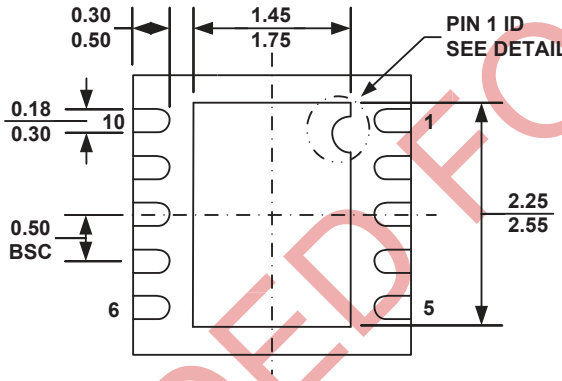
PACKAGE INFORMATION

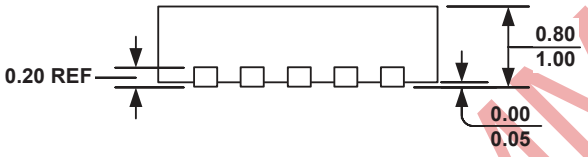
QFN10 (3mm x 3mm)



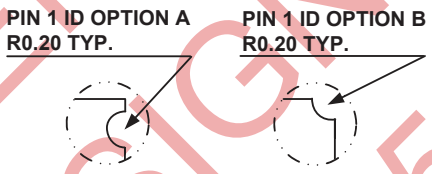
TOP VIEW



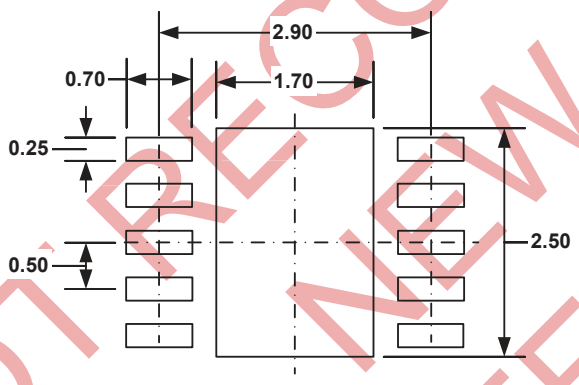
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

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