

DESCRIPTION

The MP4832A is a 32-channel, high-voltage, single-pole single-throw (SPST) analog switch with integrated output bleed resistors designed for medical ultrasound imaging applications. It can multiplex the transmit and receive voltages from multiple piezoelectric transducers (PZT).

The output switches are controlled by a 32-bit serial shift register followed by a 32-bit data latch. A data out pin (D_{OUT}) allows for multiple devices to be cascaded together. This minimizes the number of input/output (I/O) control lines. A logic high in the data latch turns on the corresponding analog switch; a logic low turns it off.

The MP4832A does not require any high voltage supplies. It uses two low voltage supplies: 3.3V and 12V. The analog switch can block or pass analog voltages up to ±90V with peak currents of up to ±2.0A. The MP4832A is available in QFN-72 (10mmx10mm) package.

FEATURES

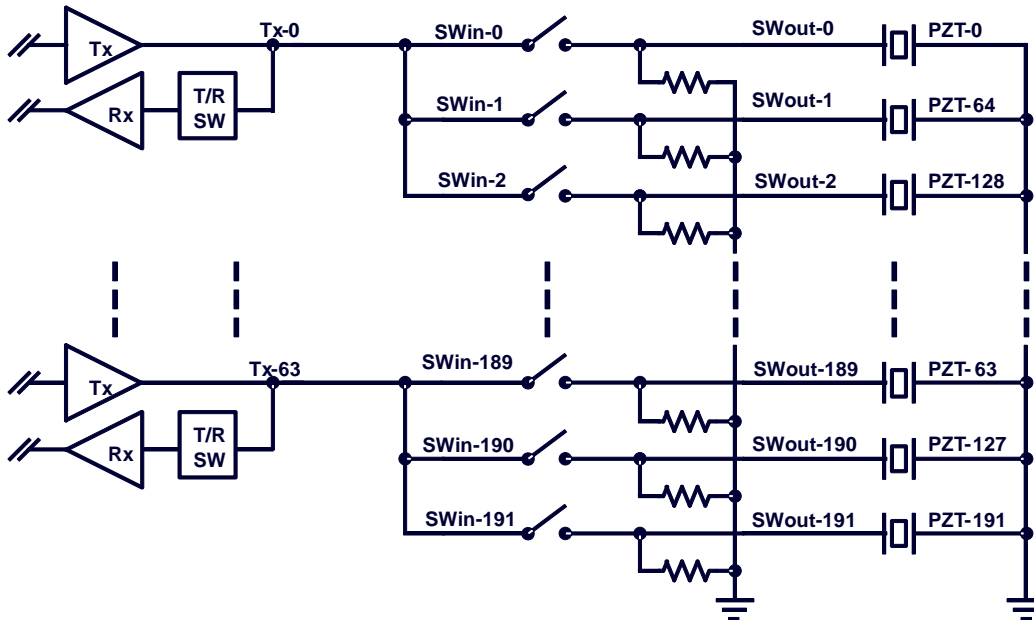
- No High Voltage Supplies Required
- 32 Channels
- Up to ±90V Analog Signals
- 14Ω Typical Switch Resistance
- ±2.0A Typical Switch Peak Current
- Off-Isolation of -66dB at 5.0MHz
- Integrated Output Bleed Resistor
- 80MHz Clock Frequency
- Available QFN-72 (10mmx10mm) Package

APPLICATIONS

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT)

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TYPICAL APPLICATION



ORDERING INFORMATION

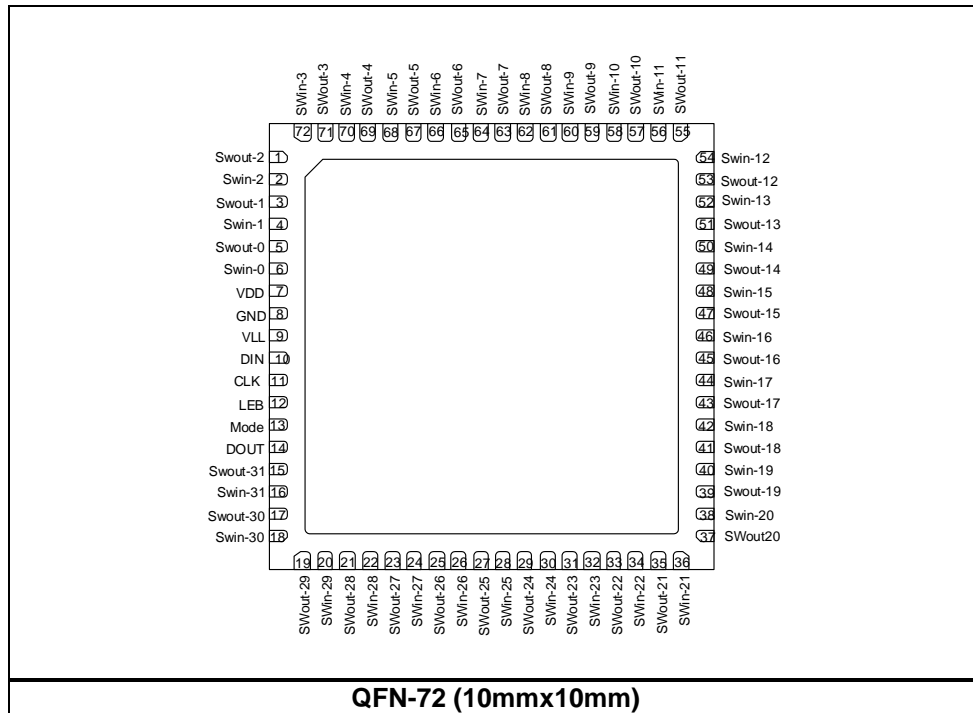
Part Number*	Package	Top Marking	MSL Rating
MP4832AGR	QFN-72 (10mmx10mm)	See Below	Level 3

TOP MARKING

MPSYYWW
MP4832A
LLLLLLLLL

MP4832A: Product code of MP4832AGR
 MPS: MPS prefix
 YY: Year code
 WW: Week code
 LLLLLLLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	SWout-2	Analog switch output 2. Connect to the piezoelectric transducer.
2	SWin-2	Analog switch input 2. Connect to the high voltage pulser/transmitter.
3	SWout-1	Analog switch output 1. Connect to the piezoelectric transducer.
4	SWin-1	Analog switch input 1. Connect to the high voltage pulser/transmitter.
5	SWout-0	Analog switch output 0. Connect to the piezoelectric transducer.
6	SWin-0	Analog switch input 0. Connect to the high voltage pulser/transmitter.
7	V _{DD}	Translators supply voltage. 10V to 14V operating range.
8	GND	Device ground. Connect to center DAP externally.
9	V _{LL}	Logic supply voltage. 2.7V to 5.5V operating range.
10	D _{IN}	Logic input pin. When Mode is logic low, D _{IN} is the data input for the 32-bit serial shift register. When Mode is logic high, D _{IN} turns all 32 output switches on or off.
11	CLK	Logic input. Clock input for the 32-bit serial shift register. Data loads in during the rising edge of the clock.
12	LEB	Logic input. Latch enable bar for the 32-bit latch. Logic low transfers data from the shift registers to the latches. Logic high holds data in the latches (see Truth Table on page 8).
13	Mode	Logic input pin. When Mode is logic low, the output switch states are controlled by the serial shift registers and parallel data latches. When Mode is logic high, the D _{IN} pin turns all 32 output switches on or off.
14	D _{OUT}	Logic output. Data output for the 32-bit serial shift register.
15	SWout-31	Analog switch output 31. Connect to the piezoelectric transducer.
16	SWin-31	Analog switch input 31. Connect to the high voltage pulser/transmitter.
17	SWout-30	Analog switch output 30. Connect to the piezoelectric transducer.
18	SWin-30	Analog switch input 30. Connect to the high voltage pulser/transmitter.
19	SWout-29	Analog switch output 29. Connect to the piezoelectric transducer.
20	SWin-29	Analog switch input 29. Connect to the high voltage pulser/transmitter.
21	SWout-28	Analog switch output 28. Connect to the piezoelectric transducer.
22	SWin-28	Analog switch input 28. Connect to the high voltage pulser/transmitter.
23	SWout-27	Analog switch output 27. Connect to the piezoelectric transducer.
24	SWin-27	Analog switch input 27. Connect to the high voltage pulser/transmitter.
25	SWout-26	Analog switch output 26. Connect to the piezoelectric transducer.
26	SWin-26	Analog switch input 26. Connect to the high voltage pulser/transmitter.
27	SWout-25	Analog switch output 25. Connect to the piezoelectric transducer.
28	SWin-25	Analog switch input 25. Connect to the high voltage pulser/transmitter.
29	SWout-24	Analog switch output 24. Connect to the piezoelectric transducer.
30	SWin-24	Analog switch input 24. Connect to the high voltage pulser/transmitter.
31	SWout-23	Analog switch output 23. Connect to the piezoelectric transducer.
32	SWin-23	Analog switch input 23. Connect to the high voltage pulser/transmitter.
33	SWout-22	Analog switch output 22. Connect to the piezoelectric transducer.
34	SWin-22	Analog switch input 22. Connect to the high voltage pulser/transmitter.
35	SWout-21	Analog switch output 21. Connect to the piezoelectric transducer.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
36	SWin-21	Analog switch input 21. Connect to the high voltage pulser/transmitter.
37	SWout-20	Analog switch output 20. Connect to the piezoelectric transducer.
38	SWin-20	Analog switch input 20. Connect to the high voltage pulser/transmitter.
39	SWout-19	Analog switch output 19. Connect to the piezoelectric transducer.
40	SWin-19	Analog switch input 19. Connect to the high voltage pulser/transmitter.
41	SWout-18	Analog switch output 18. Connect to the piezoelectric transducer.
42	SWin-18	Analog switch input 18. Connect to the high voltage pulser/transmitter.
43	SWout-17	Analog switch output 17. Connect to the piezoelectric transducer.
44	SWin-17	Analog switch input 17. Connect to the high voltage pulser/transmitter.
45	SWout-16	Analog switch output 16. Connect to the piezoelectric transducer.
46	SWin-16	Analog switch input 16. Connect to the high voltage pulser/transmitter.
47	SWout-15	Analog switch output 15. Connect to the piezoelectric transducer.
48	SWin-15	Analog switch input 15. Connect to the high voltage pulser/transmitter.
49	SWout-14	Analog switch output 14. Connect to the piezoelectric transducer.
50	SWin-14	Analog switch input 14. Connect to the high voltage pulser/transmitter.
51	SWout-13	Analog switch output 13. Connect to the piezoelectric transducer.
52	SWin-13	Analog switch input 13. Connect to the high voltage pulser/transmitter.
53	SWout-12	Analog switch output 12. Connect to the piezoelectric transducer.
54	SWin-12	Analog switch input 12. Connect to the high voltage pulser/transmitter.
55	SWout-11	Analog switch output 11. Connect to the piezoelectric transducer.
56	SWin-11	Analog switch input 11. Connect to the high voltage pulser/transmitter.
57	SWout-10	Analog switch output 10. Connect to the piezoelectric transducer.
58	SWin-10	Analog switch input 10. Connect to the high voltage pulser/transmitter.
59	SWout-9	Analog switch output 9. Connect to the piezoelectric transducer.
60	SWin-9	Analog switch input 9. Connect to the high voltage pulser/transmitter.
61	SWout-8	Analog switch output 8. Connect to the piezoelectric transducer.
62	SWin-8	Analog switch input 8. Connect to the high voltage pulser/transmitter.
63	SWout-7	Analog switch output 7. Connect to the piezoelectric transducer.
64	SWin-7	Analog switch input 7. Connect to the high voltage pulser/transmitter.
65	SWout-6	Analog switch output 6. Connect to the piezoelectric transducer.
66	SWin-6	Analog switch input 6. Connect to the high voltage pulser/transmitter.
67	SWout-5	Analog switch output 5. Connect to the piezoelectric transducer.
68	SWin-5	Analog switch input 5. Connect to the high voltage pulser/transmitter.
69	SWout-4	Analog switch output 4. Connect to the piezoelectric transducer.
70	SWin-4	Analog switch input 4. Connect to the high voltage pulser/transmitter.
71	SWout-3	Analog switch output 3. Connect to the piezoelectric transducer.
72	SWin-3	Analog switch input 3. Connect to the high voltage pulser/transmitter.
Center DAP		Substrate. Connect to ground externally.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

V_{LL}, Logic supply -0.5V to +6.6V
 V_{DD}, Translator supply -0.5V to +16V
 V_{SIG}, Analog signal range 0V to ±105V
 Junction temperature 150°C
 Lead temperature 260°C
 Continuous power dissipation, T_A = 25°C ⁽²⁾
 8.3W
 Storage temperature -55°C to 150°C

ESD Ratings

Human-body model (HBM): JEDEC standard
 SWOTx Class 1B
 SWINx Class 1C
 Other pins Class 2
 Charged-device model (CDM): JEDEC
 Standard
 All pins Class 3

Recommended Operating Conditions ⁽³⁾

Logic supply voltage, V_{LL} 2.7V to 5.5V
 Translator supply voltage, V_{DD} 10V to 14V
 Analog signal range, V_{SIG} 0 to ±90V
 Junction temperature, T_J -25°C to +125°C

Thermal Resistance ⁽⁴⁾ **θ_{JA}** **θ_{JC}**
 QFN-72 (10mmx10mm) 15 3 °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation causes excessive die temperature, resulting in permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = 12V$, $V_{LL} = 5.0V$, unless otherwise noted. ⁽⁵⁾

Parameter	Sym	Conditions	$T_J = 0^\circ C$		$T_J = 25^\circ C$			$T_J = 70^\circ C$		Units
			Min	Max	Min	Typ	Max	Min	Max	
Analog signal range	V_{SIG}	Applied to SWin pin	0	± 90	0		± 90	0	± 90	V
On-resistance	R_{ON}	$I_{SIG} = \pm 5.0mA$, $SW_{OUT} = 0V$, See test circuit 1 on page 10		20		14	24		30	Ω
		$I_{SIG} = \pm 200mA$, $SW_{OUT} = 0V$, See test circuit 1 on page 10		16		13.5	19		24	Ω
Small signal on-resistance matching	ΔR_{ON}	$I_{SIG} = \pm 5.0mA$, $SW_{OUT} = 0V$				5.0				%
Large signal on-resistance**	R_{ONL}	$I_{SIG} = \pm 1.0A$, $t_{PW} \leq 500ns$, duty cycle $\leq 1.0\%$, $SW_{OUT} = 0V$ See test circuit 2 on page 10				13				Ω
Switch output peak current	I_{SWPK}	$t_{PW} \leq 100ns$, duty cycle $\leq 1.0\%$				± 2.0				A
Output bleed resistor	R_{BLEED}	$I_{SIG} = \pm 50\mu A$			20	30	50			k Ω
Switch Off DC offset	V_{DC-OFF}	No Load, No V_{SIG} See test circuit 3		± 50			± 50		± 50	mV
Switch On DC offset	V_{DC-ON}	No Load, No V_{SIG} See test circuit 3 on page 10		± 50			± 50		± 50	mV
V_{LL} quiescent current	I_{LLQ}	All logic inputs are static		50			50		50	μA
V_{DD} quiescent current	I_{DDQ}	All switches On or Off, $SW_{IN} = SW_{OUT} = \text{Ground}$		90			90		90	μA
V_{LL} average dynamic current	I_{LL}	$f_{CLK} = 40MHz$, $D_{IN} = 20MHz$				4.5	9			mA
		$f_{CLK} = 80MHz$, $D_{IN} = 40MHz$ ⁽⁶⁾				8.7				mA
V_{DD} average dynamic current	I_{DD}	All output switches are turning on and off at 50kHz				5.4	10.8			mA
Input voltage logic low	V_{IL}		0	$0.2V_{LL}$	0		$0.2V_{LL}$	0	$0.2V_{LL}$	V
Input voltage logic high	V_{IH}		$0.8V_{LL}$	V_{LL}	$0.8V_{LL}$		V_{LL}	$0.8V_{LL}$	V_{LL}	V
Input current logic low	I_{IL}		-1.0		-1.0			-1.0		μA
Input current logic high	I_{IH}			1.0			1.0		1.0	μA
Logic input capacitance ⁽⁶⁾	C_{IN}			10			10		10	pF

Notes:

5) Production test is at 25°C only. 0°C and 70°C limits are guaranteed by design and characterization.

6) Parameters are not tested in mass production, only guaranteed by design or bench characterization.

AC ELECTRICAL CHARACTERISTICS *(continued)*

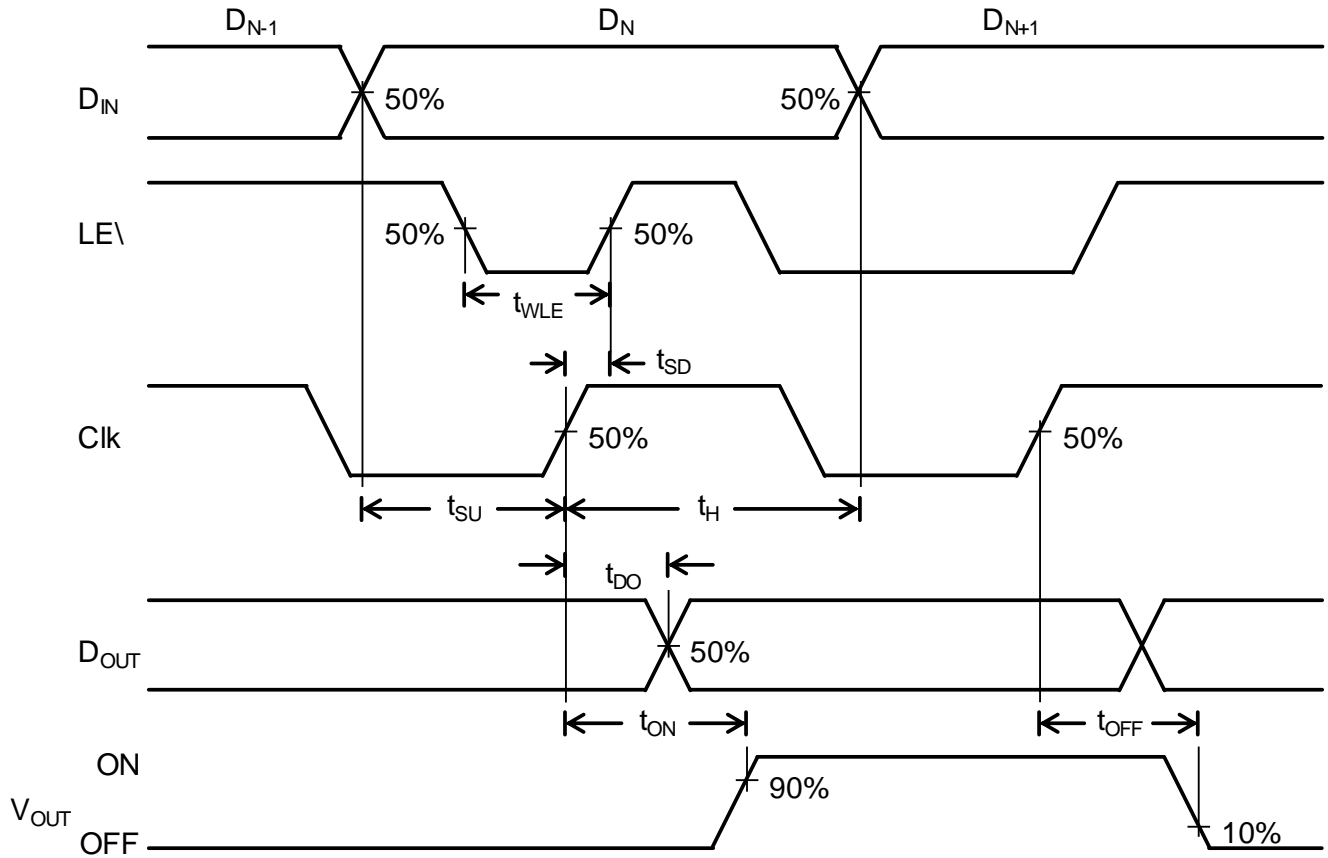
$V_{DD} = 12V$, $V_{LL} = 5.0V$, unless otherwise noted. ⁽⁵⁾

Parameter	Sym	Conditions	$T_J = 0^\circ C$		$T_J = 25^\circ C$			$T_J = 70^\circ C$		Units	
			Min	Max	Min	Typ	Max	Min	Max		
Clock frequency ⁽⁶⁾	f _{CLK}	50% duty cycle	$V_{LL} = 3.3V$	0	40	0		40	0	40	MHz
			$V_{LL} = 5.0V$	0	80	0		80	0	80	
Clock rise time ⁽⁶⁾	t _r				50			50		50	ns
Clock fall time ⁽⁶⁾	t _f				50			50		50	ns
Set-up time from data to rising edge of clock ⁽⁶⁾	t _{SU}			1.0		1.0			1.0		ns
Hold time from rising edge of clock to data ⁽⁶⁾	t _H			1.0		1.0			1.0		ns
Set-up time before LE bar rises ⁽⁶⁾	t _{SD}			6.0		6.0			6.0		ns
LE\ pulse width ⁽⁶⁾	t _{WLE bar}			6.0		6.0			6.0		ns
Data out propagation delay time from rising edge of clock ⁽⁶⁾	t _{DOHL} , t _{DOLH}	20pF on D _{OUT} to ground		4.0	11	4.0		11	4.0	11	ns
Output switch turn on time	t _{ON}	S _{Win} = 2.0V, S _{Wout} = 50Ω to ground.			2.0			2.0		2.0	μs
Output switch turn off time	t _{OFF}	See test circuit 4 on page 11			2.0			2.0		2.0	μs
Analog signal slew rate ⁽⁶⁾	dv/dt				20			20		20	V/ns
Off-Isolation ⁽⁶⁾	K _O	Freq = 5.0MHz, R _{load} = 50Ω See test circuit 5 on page 11					-66				dB
Switch Crosstalk ⁽⁶⁾	K _{CR}	Freq = 5.0MHz, R _{load} = 50Ω See test circuit 6 on page 11					-60				dB
Switch off capacitance ⁽⁶⁾	C _{SWin-OFF}						10				pF
Switch on capacitance ⁽⁶⁾	C _{SW-ON}						13				pF
Positive output voltage spike ⁽⁶⁾	+V _{SPK}	S _{Win} = 1kΩ to ground, S _{Wout} = 50Ω to ground See test circuit 7					160				mV
Negative output voltage spike ⁽⁶⁾	-V _{SPK}						-20				mV
Output charge injection ⁽⁶⁾	Q _{INJ}	C _{load} = 1000pF See test circuit 8 on page 12					30				pC
Data outlogic low voltage	V _{OL}	I _{sink} = 10mA			1.0			1.0		1.0	V
Data outlogic high voltage	V _{OH}	I _{source} = 10mA	$V_{LL}-1.0$			$V_{LL}-1.0$			$V_{LL}-1.0$		V

Notes:

- 5) Production test is at 25°C only. 0°C and 70°C limits are guaranteed by design and characterization.
6) Parameters are not tested in mass production, only guaranteed by design or bench characterization.

TIMING DIAGRAM



LOGIC TRUTH TABLE (7)

Logic Input								Switch State				
D0	D1	D2	---	D31	D_{IN}	LE bar	Mode	SW0	SW1	SW2	---	SW31
L	-	-		-	x	L	L	Off	-	-		-
H	-	-		-	x	L	L	On	-	-		-
-	L	-		-	x	L	L	-	Off	-		-
-	H	-		-	x	L	L	-	On	-		-
-	-	L		-	x	L	L	-	-	Off		-
-	-	H		-	x	L	L	-	-	On		-
-	-	-		L	x	L	L	-	-	-		Off
-	-	-		H	x	L	L	-	-	-		On
x	x	x		x	x	H	L	Holds previous state				
x	x	x		x	L	x	H	All switches off				
x	x	x		x	H	x	H	All switches on				

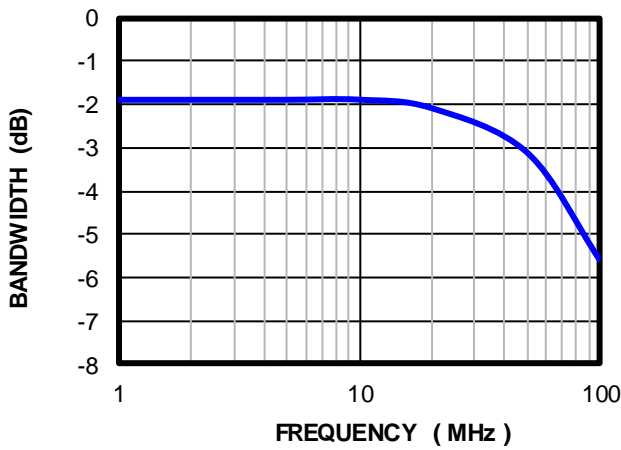
Notes:

7) L denotes logic level low, H denotes logic level high, and x denotes no change.

TYPICAL CHARACTERISTICS

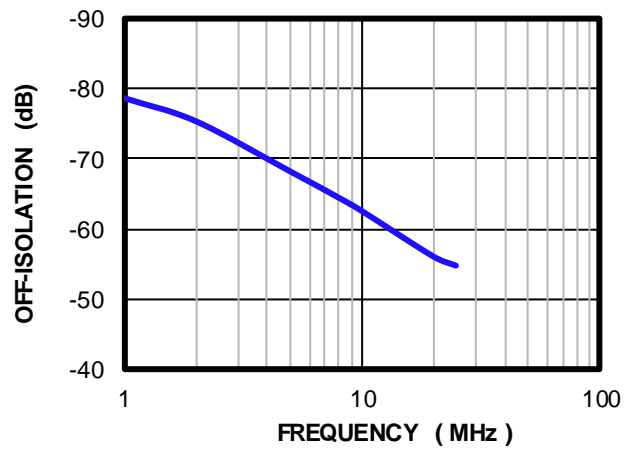
Bandwidth vs. Frequency

$R_{LOAD} = 50\Omega$



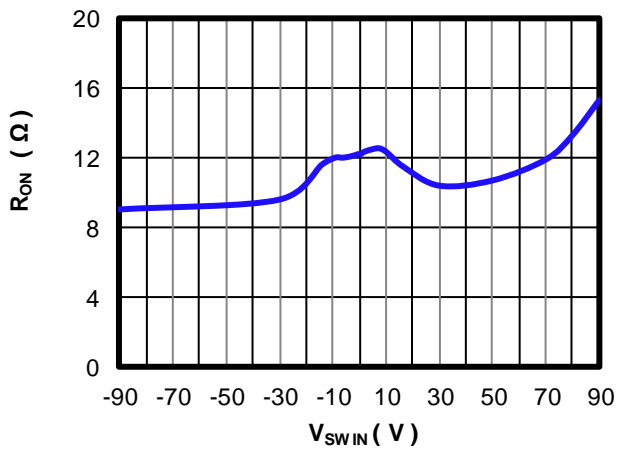
Off-Isolation vs. Frequency

$R_{LOAD} = 50\Omega$



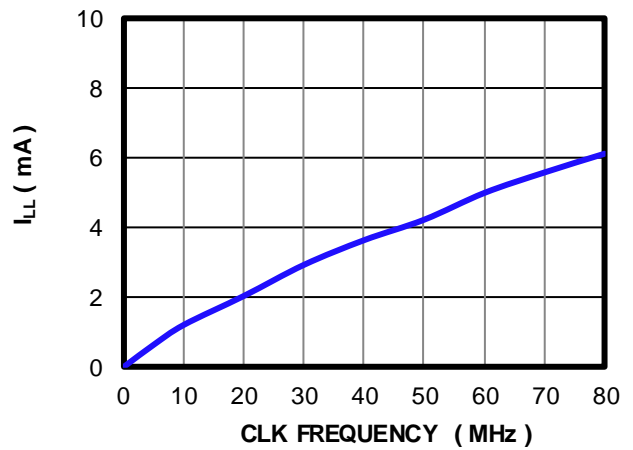
Switch Resistance vs. Switch Input Voltage

$R_{LOAD} = 50\Omega$



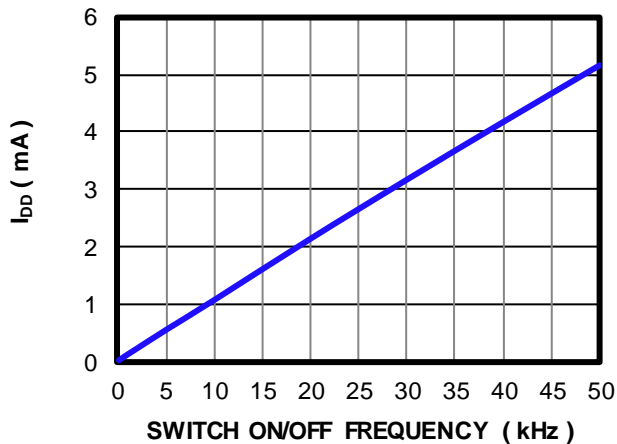
I_{LL} vs. Clock Frequency

$V_{LL} = 5.0V, V_{DD} = 10V$



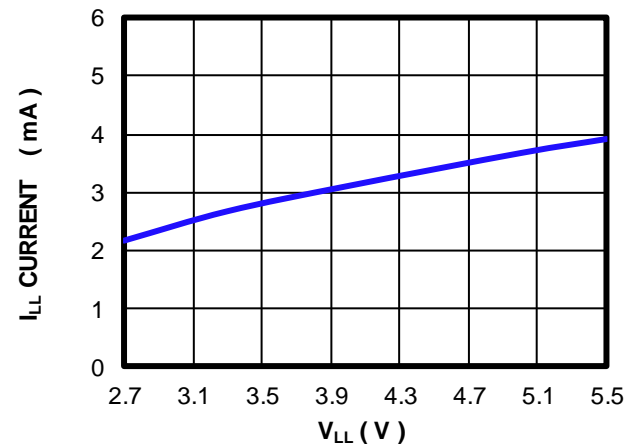
I_{DD} vs. Switch On/Off Frequency

$V_{LL} = 5.0V, V_{DD} = 10V, \text{All 32 channels switching}$



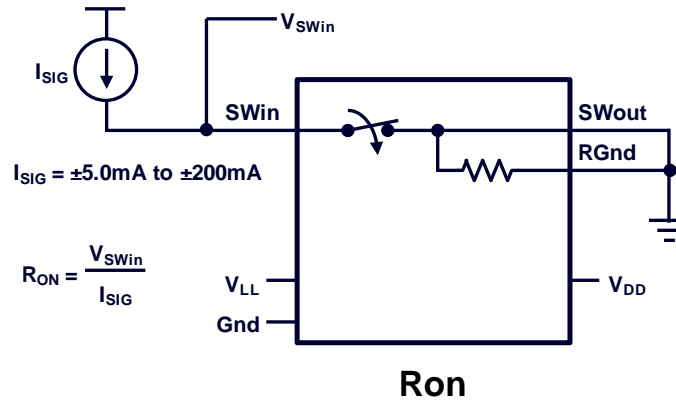
I_{LL} Current vs. V_{LL} Voltage

$CLK = 40MHz, D_{IN} = 20MHz$

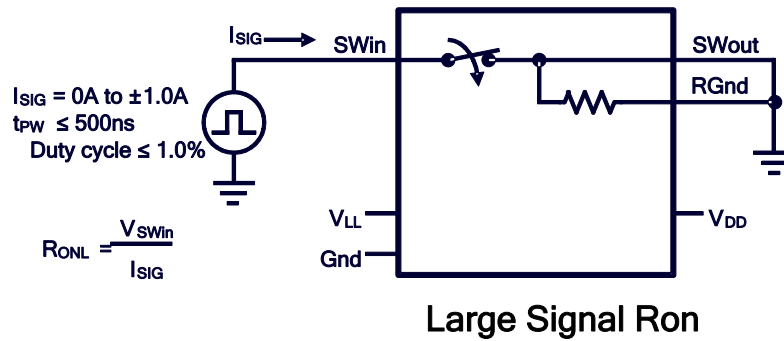


TEST CIRCUITS

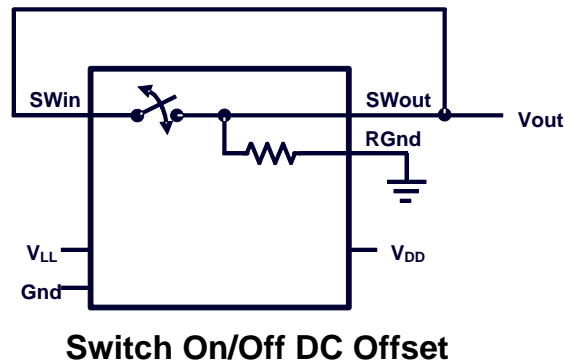
Test Circuit 1



Test Circuit 2

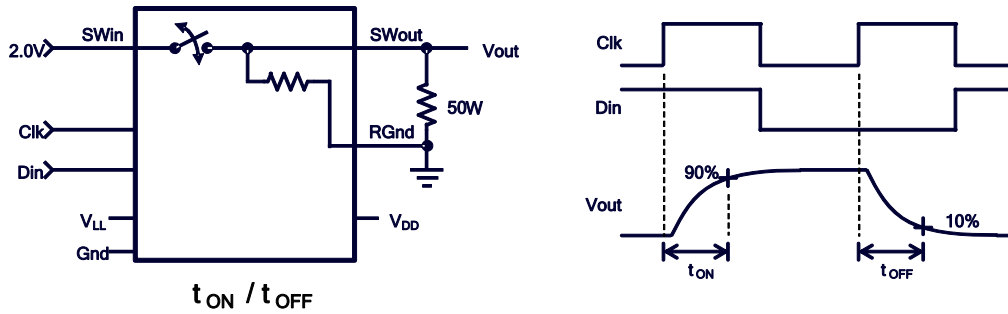


Test Circuit 3

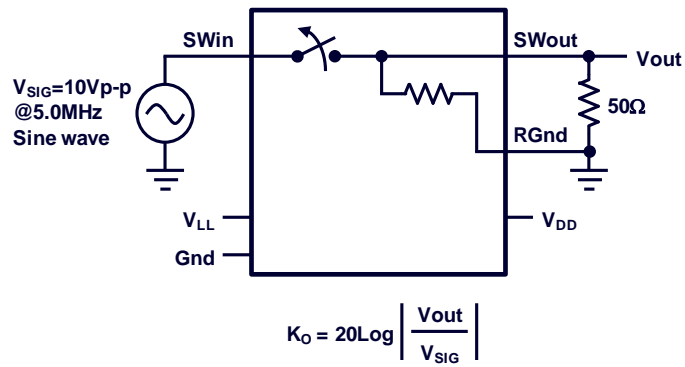


TEST CIRCUITS (continued)

Test Circuit 4

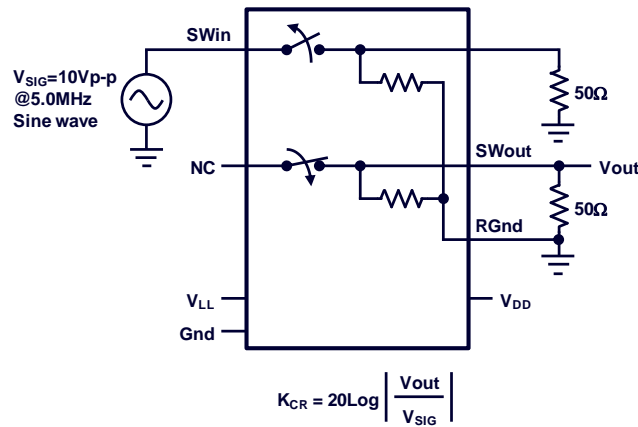


Test Circuit 5



Switch Off-Isolation

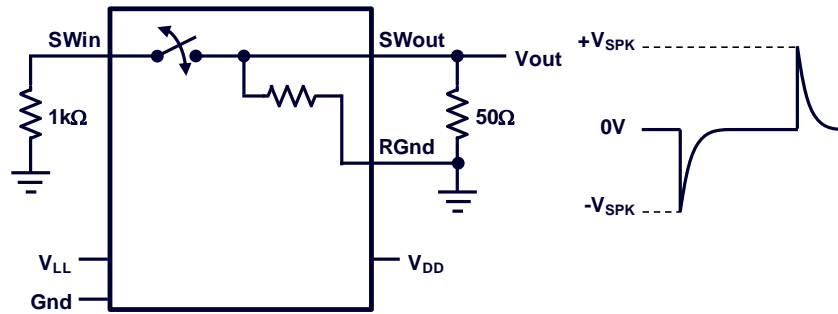
Test Circuit 6



Switch Crosstalk

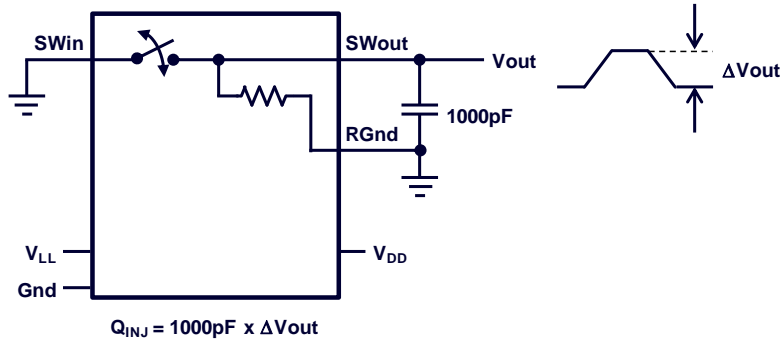
TEST CIRCUITS (continued)

Test Circuit 7



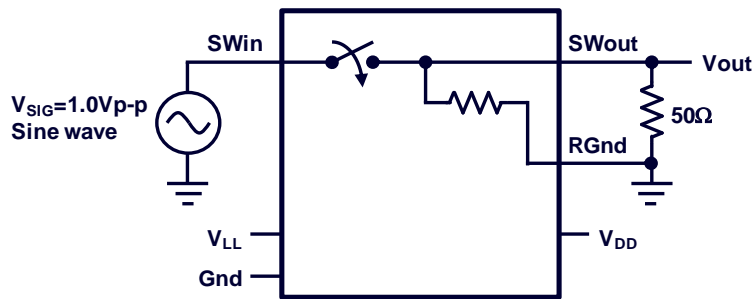
Output Voltage Spike

Test Circuit 8



$Q_{INJ} = 1000\text{pF} \times \Delta V_{out}$
Charge Injection

Test Circuit 9



Small Signal Bandwidth

FUNCTIONAL BLOCK DIAGRAM

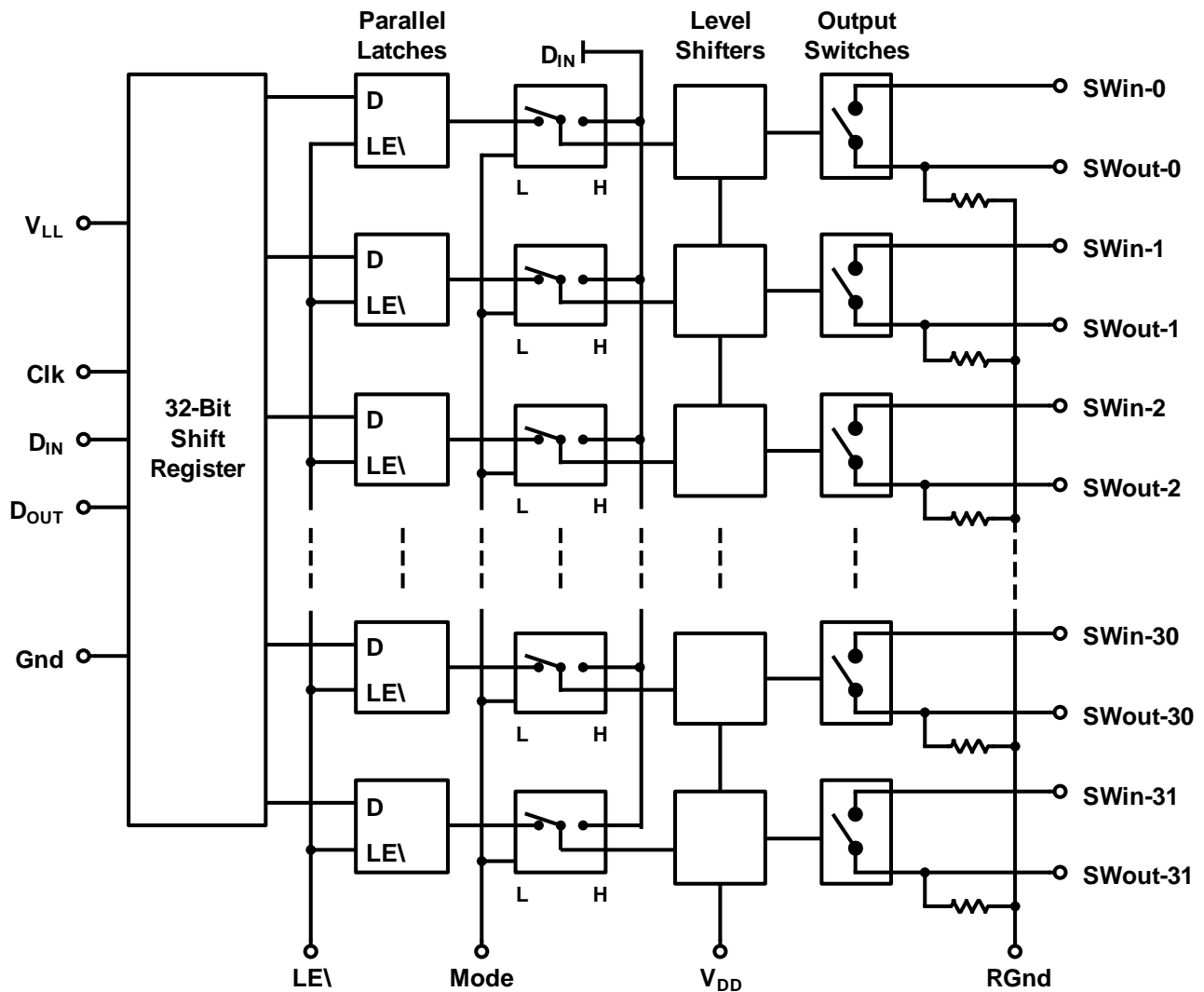


Figure 1: Functional Block Diagram

APPLICATION INFORMATION

Detailed Description

The MP4832A is a 32-channel, high voltage, single-pole single-throw (SPST) analog switch with integrated output bleed resistors. It is designed for medical ultrasound imaging applications, but it can also be used for non-destructive testing (NDT) applications.

The device is designed to multiplex the high transmit voltages to selected piezoelectric transducers and to multiplex the small analog echo signal to a selected receiver. A data out (D_{OUT}) pin allows for multiple devices to be cascaded together. This minimizes the number of input/output (I/O) control lines.

There are two modes that control the states of the output switches. When the Mode pin is low, the output switches are controlled by a 32-bit serial shift register followed by a 32-bit data latch. A logic high in the data latch turns on the corresponding analog switch; a logic low turns it off. When the Mode pin is high, the D_{IN} pin becomes a global control for all 32 output switches. D_{IN} high turns on all 32 output switches; D_{IN} low turns them off.

The MP4832A has a unique patent pending design that does not require any negative or positive high voltage supplies. This eliminates the requirement to generate high voltage positive and negative supplies and the requirement to place high voltage bypass capacitors next to each device. It also resolves safety concerns regarding high voltage buses and concerns over power up/down fault conditions.

Analog Switch

The analog switches have a typical switch resistance of 14Ω. In the on-state, it can transmit voltages up to ±90V with peak currents of up to ±2.0A. In the off-state, it can block voltages up to ±90V.

Each switch has a dedicated input and output pin, SW_{in} and SW_{out}. Connect the transmit voltages to the SW_{in} pins and connect the PZT load to the SW_{out} pins. The SW_{in} and SW_{out} pins are not interchangeable.

Typical high voltage transmission waves are short bursts of high voltage pulses. The burst

can consist of a single cycle or multiple cycles with 1.0MHz to 15MHz pulses starting at 0V and ending at 0V (see Figure 2).

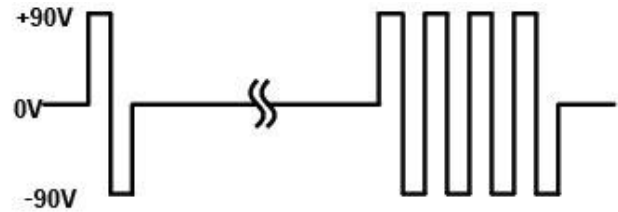


Figure 2: Typical Tx High Voltage Burst

The SW_{in} input must be close to ground before sending the high voltage pulses. This allows the internal circuitry to properly drive the output switches.

Transmit voltages exceeding ±5V must have frequencies higher than 500kHz. When receiving the echo signals where the voltages are below ±0.5V, there is no restriction. The switch can pass low-voltage DC signals.

Logic Interface in Low Mode

The MP4832A is controlled by a 32-bit serial shift register followed by a 32-bit latch. Data loads into the shift register during the rising edge of the clock. No data is transferred during the falling edge. Data shifts into register 0 and shifts out from register 31.

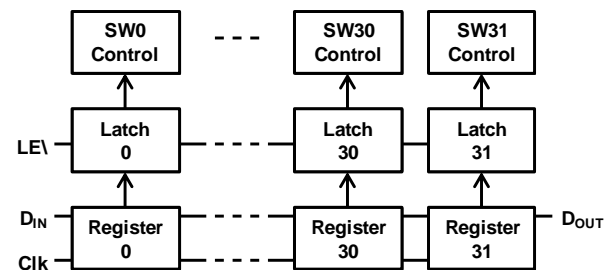


Figure 3: Logic Interface Details

Figure 3 shows the logic interface details. On the first clock cycle, the first data bit enters into shift register 0. After 31 more clocked cycles, the first bit is in register 31.

When the latch enable bar (LE) is low, the data in the shift registers are transferred into the 32-bit latch. When LE is high, the data in the latches are held. When LE is high, new data can shift into the 32-bit serial shift register without affecting the data in the 32-bit latch. The output switch states follow the data in the 32-bit latch.

APPLICATION DIAGRAM

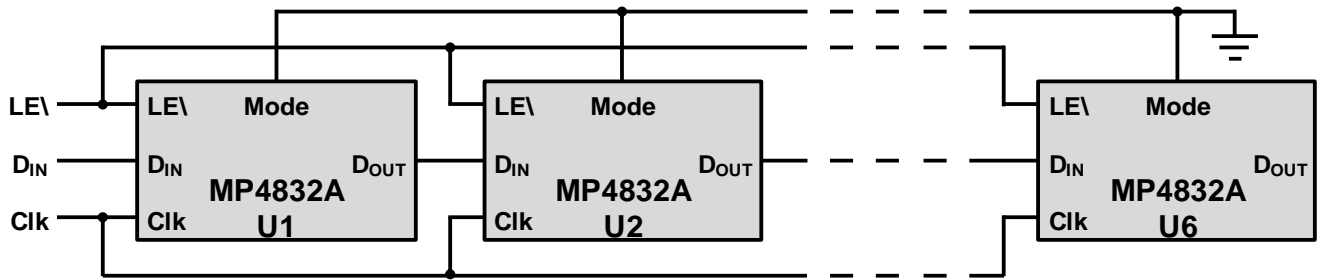


Figure 4: Configuration of 6 MP4832A Devices with a Single Data Input Line

The maximum clock frequency for the MP4832A is 80MHz. The frontend logic control minimizes the number of input and output (I/O) control lines. A system requiring 192 channels must have 6 devices ($192 / 32 = 6$). Figure 4 shows 6 MP4832A devices in a single daisy-chain

configuration. With an 80MHz clock, all 6 devices can update in $2.4\mu\text{s}$. Only three control lines are required; clock, data in, and latch enable bar. For systems requiring a faster update, multiple data in lines can be used (see Figure 5).

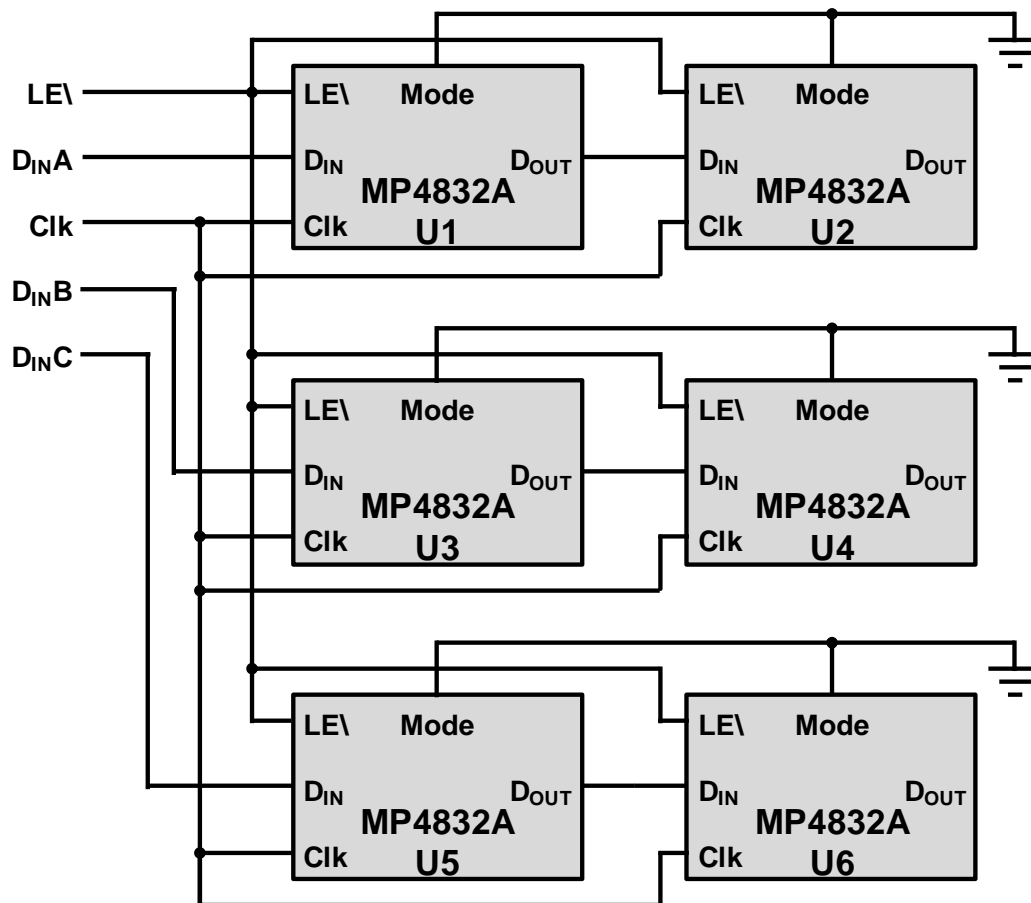


Figure 5: Daisy-Chaining MP4832A Devices with Multiple Data Input Lines

Figure 5 is a 192-channel system incorporating three data input lines: D_{INA} , D_{INB} , and D_{INC} . Each data input line is for two devices daisy-chained

together. There are now five control lines. With an 80MHz clock, all 192 channels can update in 800ns.

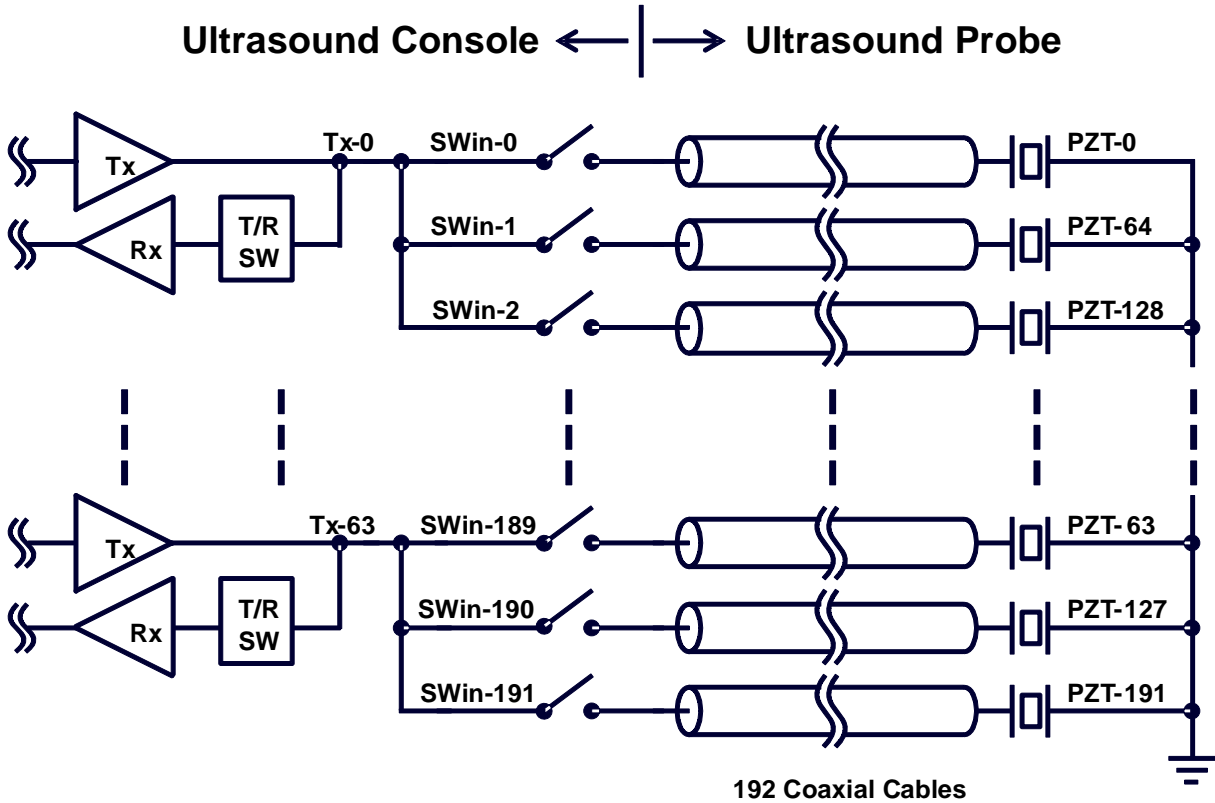


Figure 6: The MP4832A in the Console

Figure 6 shows where the MP4832A analog switches reside in an ultrasound system with a 1:3 multiplexing configuration. Multiplexing configurations can range from 1:2 to 1:8 or even higher. If the ratio is 1:8 or higher, the images will be lower quality due to slower frame rates. These devices are generally used for the lower cost ultrasound market. The MP4832A can be used in any ratio.

The main advantage of using the MP4832A is to reduce the amount of transmitter and receiver

circuitry. Figure 6 shows that without any analog switches, the ultrasound console requires 192 transmitters and receivers to drive an ultrasound probe with 192 PZT elements.

With analog switches, only 64 transmitters and receivers are required. This reduction saves board space, power, and cost, as the transmitter and receiver circuitry can be quite complex. These benefits are especially important for portable ultrasound systems where space, battery life, and weight are all premiums.

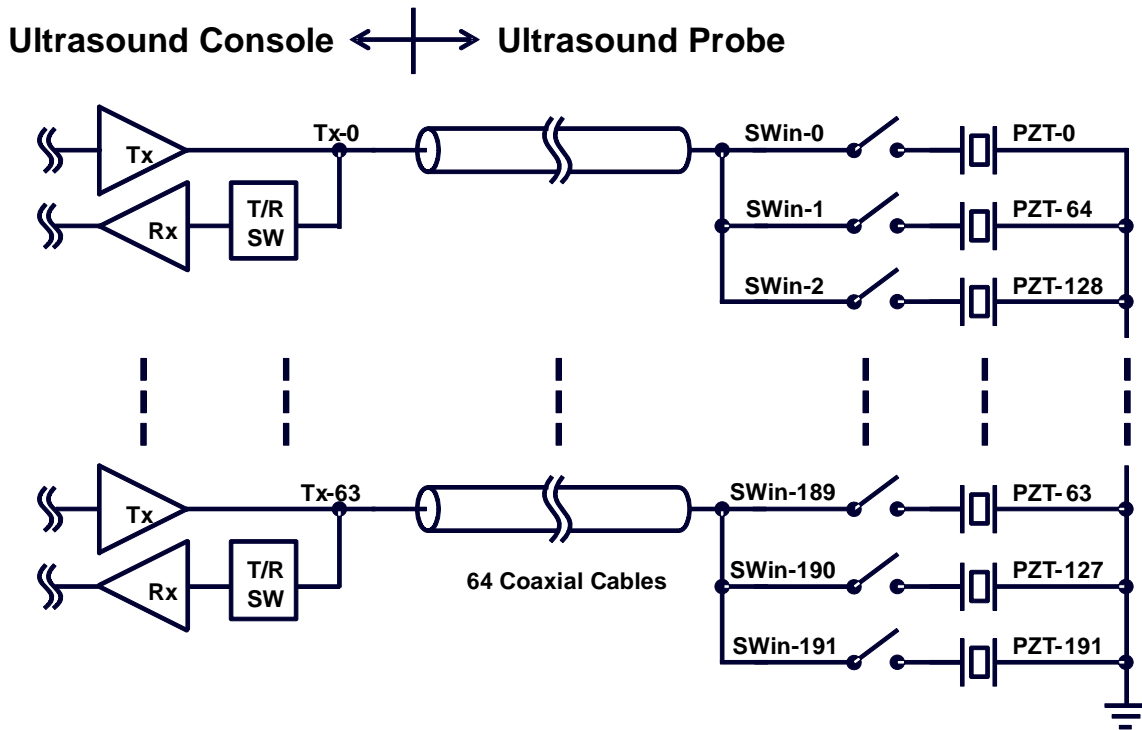


Figure 7: Inside the Ultrasound Probe Head

Figure 7 shows the advantages of putting analog switches inside the probe head (an active probe). The probe head is generally space-limited and thermal-limited. The housing is water proof as it must be submerged in alcohol for sterilization. By employing analog switches inside the probe head, the number of coaxial cables is reduced. Instead of 192 coaxial cables, only 64 coaxial cables are required for the PZT, plus 10 or fewer additional coaxial cables for the supply lines and logic interface.

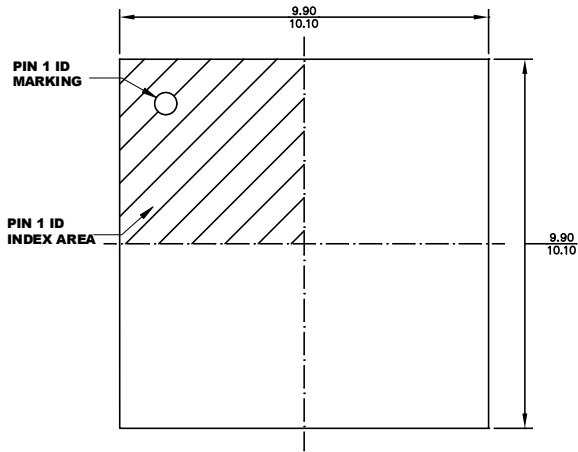
Fewer coaxial cables reduces the cost of the probe head because the material cost and the labor to connect the cables can be costly.

An additional benefit is that the probe head becomes more maneuverable, which means sonographers experience less fatigue when using the active probe.

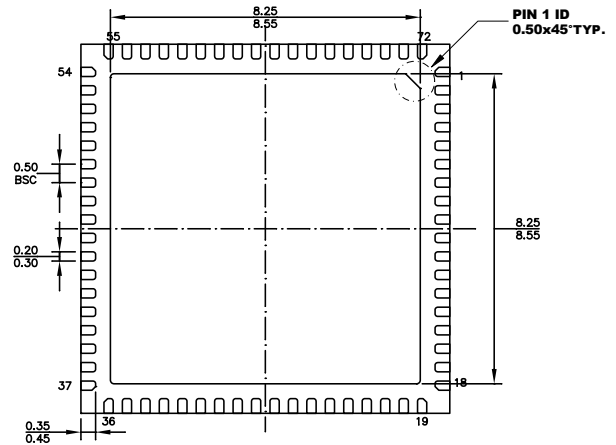
The MP4832A does not require high voltage supplies, and that eliminates concerns with running high voltage DC lines on the coaxial cables. The minimal power dissipation design eliminates the concern of thermal constraints inside the probe head, and the higher clock speed reduces the number of data lines.

PACKAGE INFORMATION

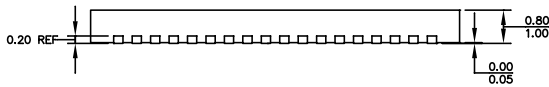
QFN-72 (10mmx10mm)



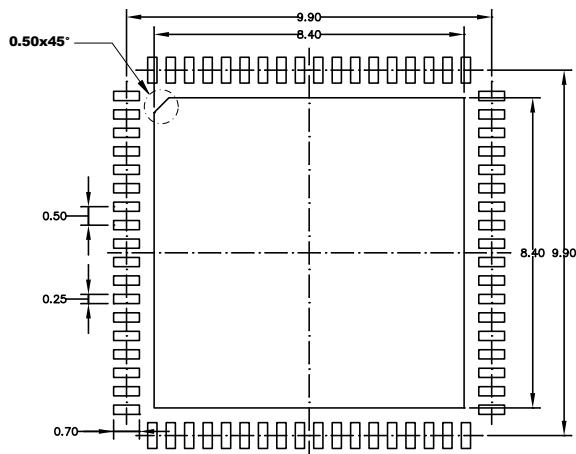
TOP VIEW



BOTTOM VIEW



SIDE VIEW

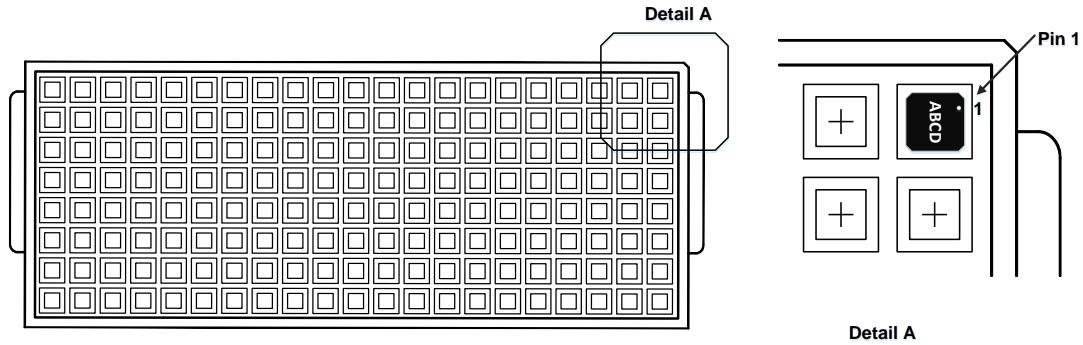


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHOULD BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Note:

This is a schematic diagram of Tray. Different packages correspond to different trays with different length, width and height.

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4832A GRD-T	QFN-72 (10mmx10mm)	N/A	N/A	240	N/A	N/A	N/A

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