MP4423C

6A, 36V, Step-Down Converter with Configurable Frequency

DESCRIPTION

The MP4423C is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve up to 6A of continuous output current (I_{OUT}), with excellent load and line regulation across a wide input supply voltage (V_{IN}) range. The MP4423C features synchronous mode operation for higher efficiency across the I_{OUT} load range.

Current mode control provides fast transient response and eases loop stabilization.

Fault protections include current limiting with hiccup mode, output over-voltage protection (OVP), and thermal shutdown (TSD).

The MP4423C requires a minimal number of readily available, standard external components, and is available in a QFN-16 (3mmx4mm) package.

FEATURES

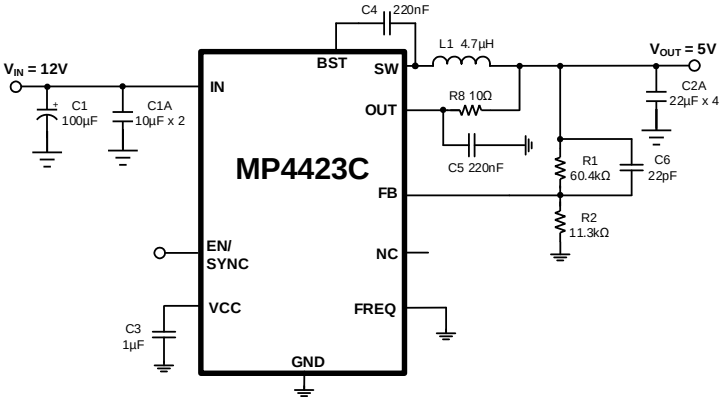
- Wide 4V to 36V Continuous Operating Input Voltage (V_{IN}) Range
- 50mΩ/30mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Up to 6A Output Current (I_{OUT})
- Up to 2.2MHz Switching Frequency (f_{SW})
- 420kHz/2.2MHz f_{SW} with Frequency Spread Spectrum (FSS)
- Bias Circuit from OUT Pin to VCC Pin Improves Efficiency
- Synchronizable to a 200kHz to 2.2MHz External Clock
- Adjustable Forced Pulse-Width Modulation (PWM) Mode or Automatic Pulse-Frequency Modulation (PFM)/PWM Mode
- Passive Output Discharge
- Output Over-Voltage Protection (OVP)
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown (TSD)
- Adjustable Output Voltage (V_{OUT}) from 0.8V
- Available in a QFN-16 (3mmx4mm) Package with Wettable Flanks

MPL Optimized Performance with MPS Inductor MPL-AY1050-4R7 Series

APPLICATIONS

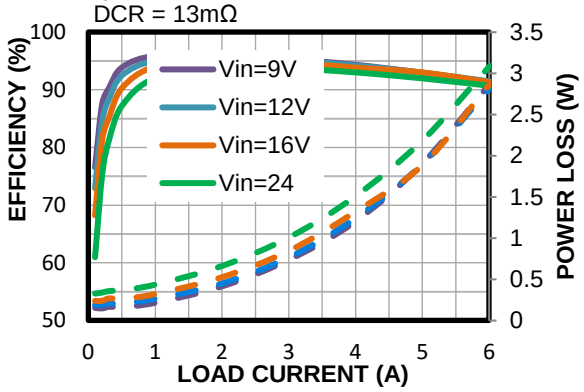
- DC/DC Power Supplies
- Wireless Charging
- USB Power Delivery (PD)

TYPICAL APPLICATION



Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 5V, FREQ = GND,
f_{SW} = 420kHz, FPWM, L = 4.7µH,
DCR = 13mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4423CGLE	QFN-16 (3mmx4mm)	*See Below*	1

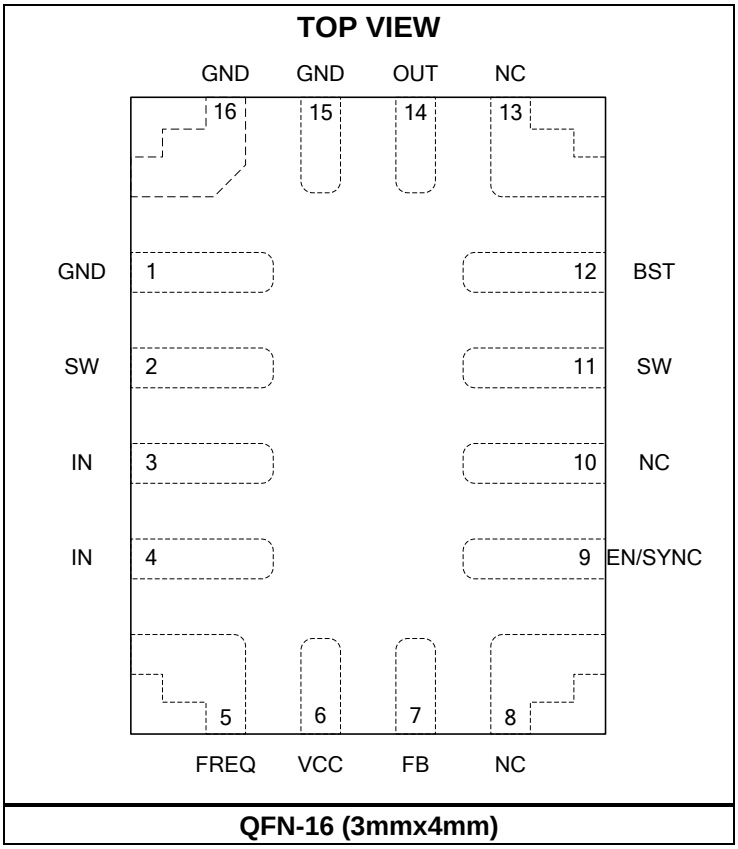
* For Tape & Reel, add suffix -Z (e.g. MP4423CGLE-Z).

TOP MARKING

MPYW
4423
CLLL
E

MP: MPS prefix
Y: Year code
W: Week code
4423C: Part number
LLL: Lot number
E: Wettable flank package

PACKAGE REFERENCE



QFN-16 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 15, 16	GND	**Power ground.**
2, 11	SW	**Switch output.** Use a wide PCB trace to connect the SW pin and the inductor.
3, 4	IN	**Supply voltage.** The MP4423C operates from a 4V to 36V input voltage (V_{IN}) rail. Place the input capacitor (C_{IN}) as close to the IC as possible using a wide PCB trace.
5	FREQ	**Switching frequency (f_{SW}) and mode selection pin.** The FREQ pin supports three modes: 1. FREQ connected to GND, 420kHz with frequency spread spectrum (FSS) and forced pulse-width modulation (PWM) mode 2. FREQ left floating, f_{SW} = 420kHz with FSS and automatic pulse-frequency modulation (PFM)/PWM mode 3. FREQ connected to VCC, f_{SW} = 2.2MHz with FSS and forced PWM (FPWM) mode
6	VCC	**Internal 5V LDO regulator output.** Decouple the VCC pin using a 1µF capacitor.
7	FB	**Feedback.** To set the output voltage (V_{OUT}), connect the FB pin to the tap of an external resistor divider connected between the OUT pin and GND. The frequency foldback comparator lowers f_{SW} when the FB voltage (V_{FB}) is below 400mV to prevent current limit runaway during a short-circuit fault condition.
8, 10, 13	NC	**No connection.** The NC pin can be tied to GND. Pin 10 can be connected to SW for better performance in PCB layout.
9	EN/SYNC	**On/off control input.** The EN/SYNC pin is pulled to GND internally via a 500kΩ resistor. Apply an external clock on this pin to sync f_{SW}.
12	BST	**Bootstrap.** A 220nF capacitor is connected between the BST pin and SW to form a floating supply across the high-side MOSFET (HS-FET) driver.
14	OUT	**Buck output.** Connect the OUT pin to an external power supply (5V ≤ V_{OUT} ≤ 20V) or connect it to V_{OUT} to reduce power dissipation and improve efficiency. Float OUT or connect it to GND if it is not used.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}), V_{OUT} .....-0.4V to +40V
V_{SW} .....
-0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{EN} .....-0.3V to +5.5V (2)
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (3) (6)
QFN-16 (3mmx4mm) 5.34W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Rating (4)

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions (5)

Operation input voltage (V_{IN}) range .... 4V to 36V
Output voltage (V_{OUT}) range.....0.8 to V_{IN} x D_{MAX}
Output current (I_{OUT})..... 6A
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (3mmx4mm)		
EV4423C-L-00A (6)	23.4	7.1 °C/W
JESD51-7 (7)	48	11 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For details on EN's abs max rating, see the EN/SYNC Control section on page 15.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. HBM with regards to GND.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on the EV4423C-L-00A, a 4-layer PCB, 70mmx55mm.
7) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V, T_J = 25°C			1	μA
		V_{EN} = 0V, T_J = -40°C to +125°C			8	
Supply current (quiescent)	I_Q	V_{FB} = 1V		0.75	1.1	mA
EN rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN falling threshold	$V_{EN\_FALLING}$		1.05	1.25	1.45	V
EN input current	I_{EN1}	V_{EN} = 2V		4.5	6	μA
	I_{EN2}	V_{EN} = 0V		0	0.2	
Thermal shutdown (8)	T_{STD}			165		°C
Thermal hysteresis (8)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}	I_{CC} = 0mA	4.8	5	5.2	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 5mA		1.5	4	%
Step-Down Converter						
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{IN_UVLO}		3.5	3.7	3.9	V
V_{IN} UVLO falling threshold	$V_{IN\_UV\_FALLING}$		3.05	3.25	3.45	V
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$			50		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			30		mΩ
Output discharge resistance	R_{DIS}			200		Ω
Feedback (FB) voltage	V_{FB}		776	792	808	mV
FB current	I_{FB}	V_{FB} = 820mV		10	100	nA
Sync frequency range	f_{SYNC}		0.2		2.4	MHz
Switching frequency	f_{SW1}	V_{FB} = 750mV, FREQ = float	340	420	500	kHz
	f_{SW2} (8)	V_{FB} = 750mV, FREQ = V_{CC}		2.2		MHz
Frequency spread spectrum (FSS) span	f_{SS1}	FREQ = GND, based on 420kHz		±10		%
	f_{SS2} (8)	FREQ = V_{CC}, based on 2.2MHz		±10		%
Foldback frequency	F_{FB}	V_{FB} < 400mV		1/2		
Maximum duty cycle	D_{MAX}	f_{SW} = 420kHz	94.5	96		%
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +125°C			10	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-side (HS) current limit (8)	I_{LIMIT1}		7	10		A
Low-side (LS) valley current limit (8)	I_{LIMIT2}			9		A
LS negative current limit (8)	I_{LSNEG}			-3		A
Minimum on time (8)	t_{ON_MIN}			60		ns
Output over-voltage protection (OVP) rising threshold	V_{OVP1}		112	115	118	%
Output OVP recovery	V_{OVP1_R}			105		%
Soft-start (SS) time	t_{SS}	Output from 10% to 90%		1.5		ms

Note:

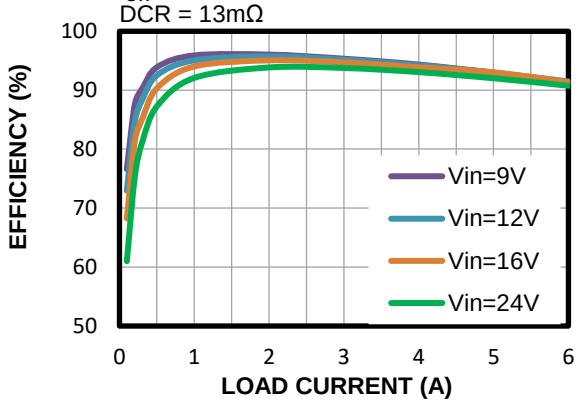
8) Guaranteed by design and engineering sample characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

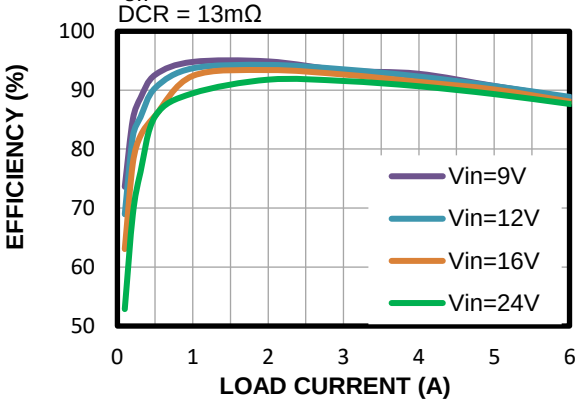
Efficiency vs. Load Current

V_{OUT} = 5V, FREQ = GND,
f_{SW} = 420kHz, FPWM, L = 4.7µH,
DCR = 13mΩ



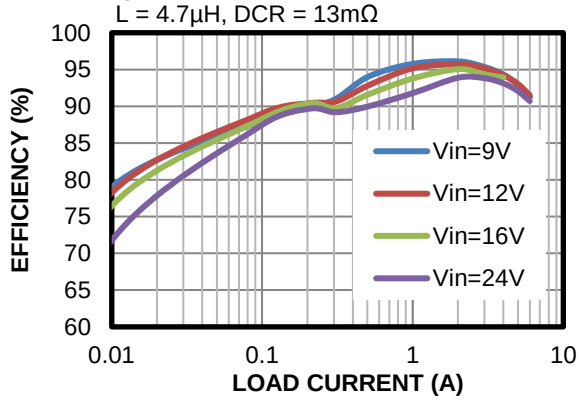
Efficiency vs. Load Current

V_{OUT} = 3.3V, FREQ = GND,
f_{SW} = 420kHz FPWM, L = 4.7µH,
DCR = 13mΩ



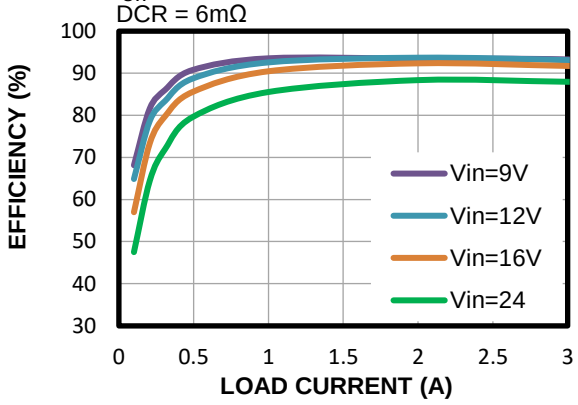
Efficiency vs. Load Current

V_{OUT} = 5V, FREQ = floating,
f_{SW} = 420kHz, auto-PFM/PWM,
L = 4.7µH, DCR = 13mΩ



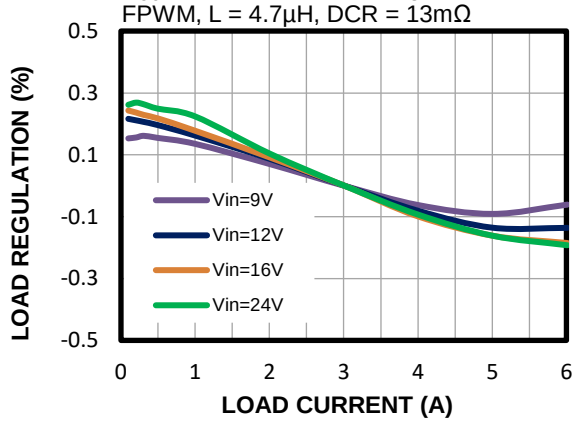
Efficiency vs. Load Current

V_{OUT} = 5V, FREQ = VCC,
f_{SW} = 2.2MHz, FPWM, L = 2.2µH,
DCR = 6mΩ



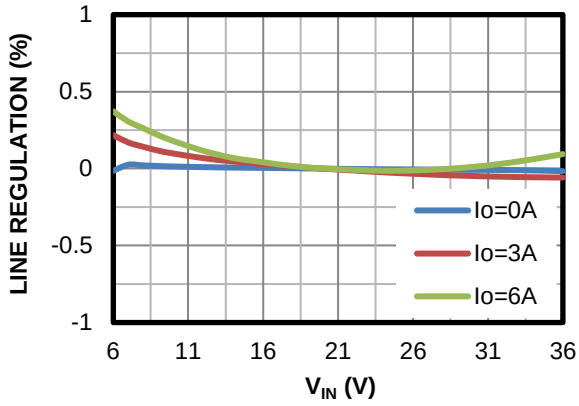
Load Regulation vs. Load Current

V_{OUT} = 5V, FREQ = GND, f_{SW} = 420kHz,
FPWM, L = 4.7µH, DCR = 13mΩ



Line Regulation vs. Input Voltage

V_{OUT} = 5V, FREQ = GND,
f_{SW} = 420kHz, FPWM, L = 4.7µH,
DCR = 13mΩ

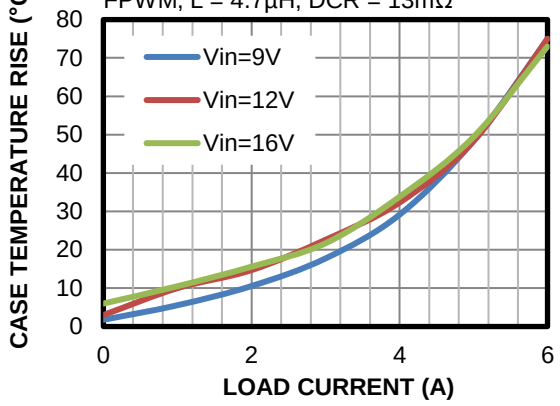


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

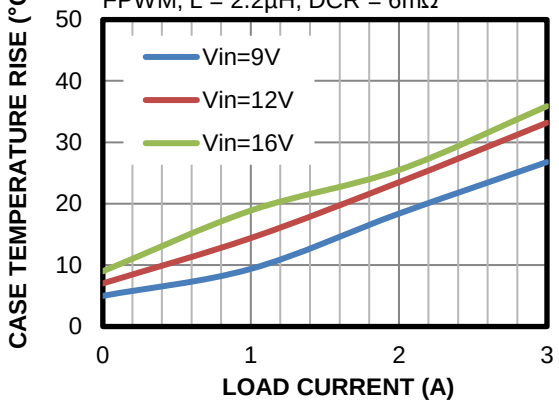
Case Temperature Rise vs. Load Current

V_{OUT} = 5V, FREQ = GND, f_{SW} = 420kHz, FPWM, L = 4.7µH, DCR = 13mΩ

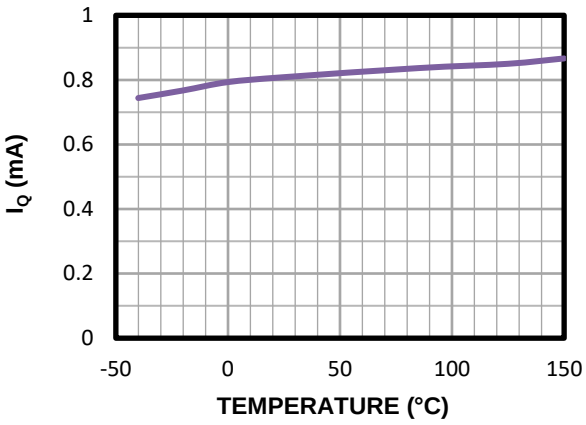


Case Temperature Rise vs. Load Current

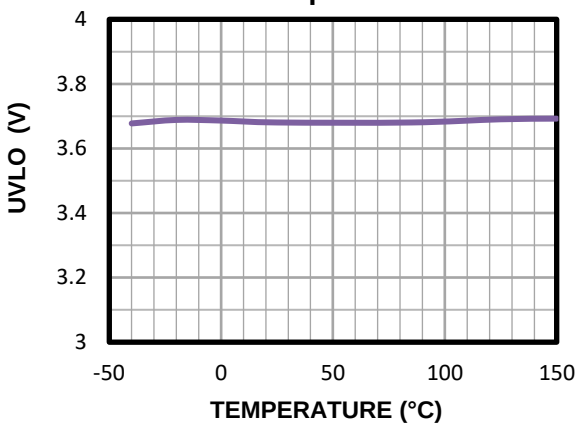
V_{OUT} = 5V, FREQ = VCC, f_{SW} = 2.2MHz, FPWM, L = 2.2µH, DCR = 6mΩ



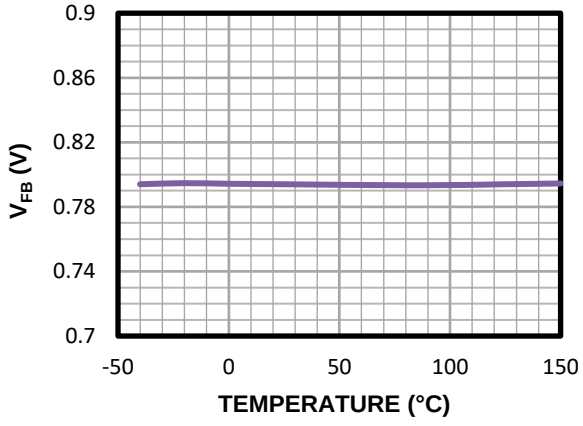
Quiescent Current vs. Temperature



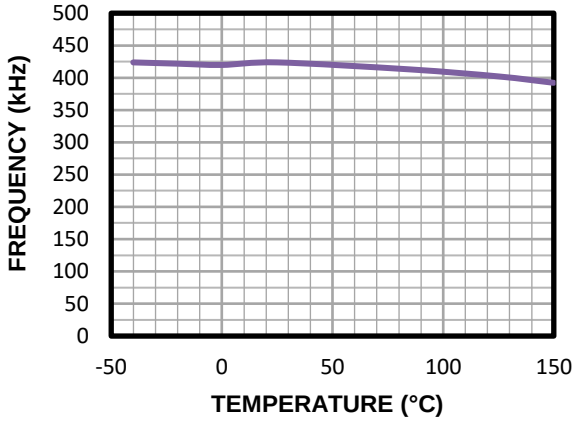
UVLO vs. Temperature



Feedback Voltage vs. Temperature



Frequency vs. Temperature

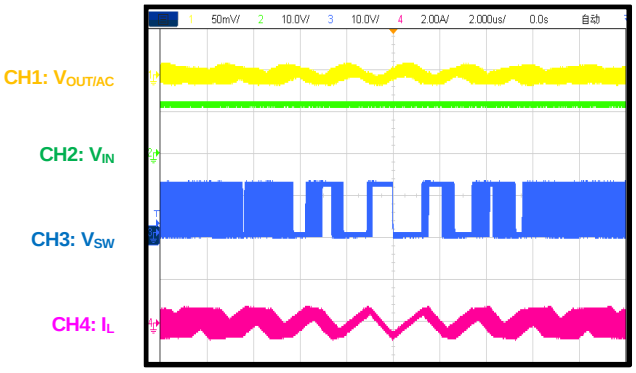


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

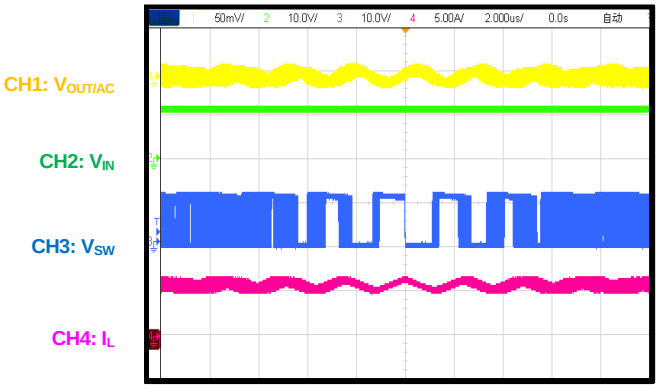
Steady State

FREQ = GND, f_{SW} = 420kHz, FPWM, I_{OUT} = 0A



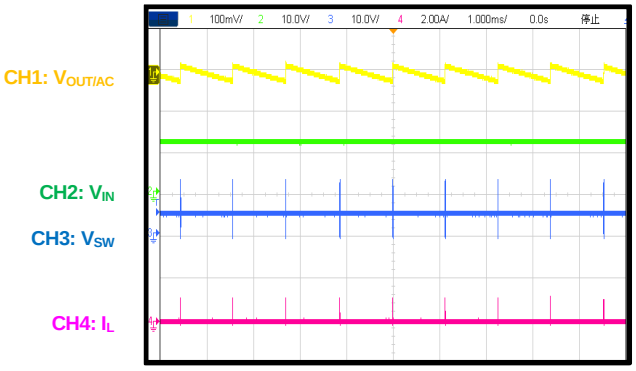
Steady State

FREQ = GND, f_{SW} = 420kHz, FPWM, I_{OUT} = 6A



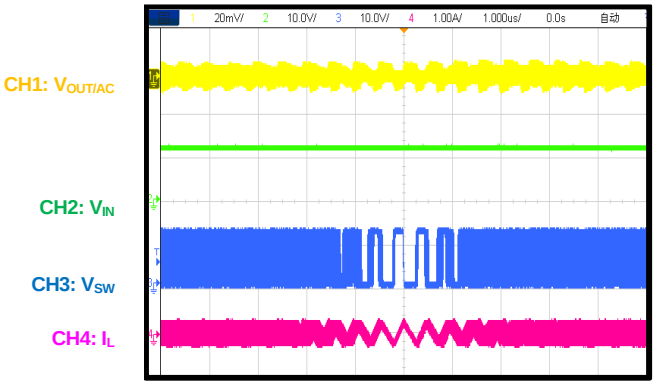
Steady State

FREQ = floating, f_{SW} = 420kHz, auto-PFM/PWM, I_{OUT} = 0A



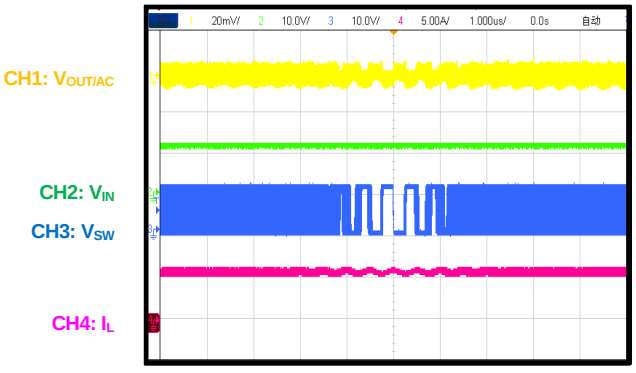
Steady State

FREQ = VCC, L = 2.2µH, f_{SW} = 2.2MHz, FPWM, I_{OUT} = 0A



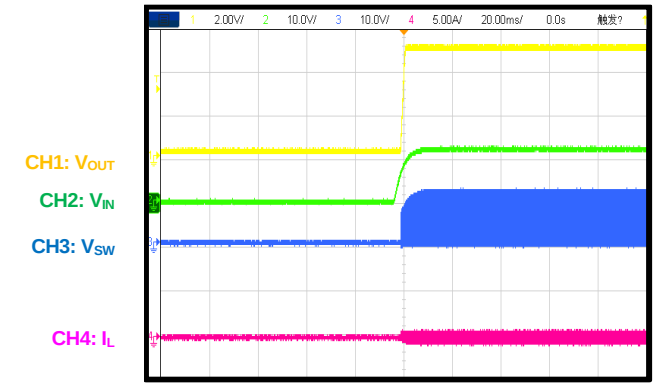
Steady State

FREQ = VCC, L = 2.2µH, f_{SW} = 2.2MHz, FPWM, I_{OUT} = 6A



Start-Up

I_{OUT} = 0A

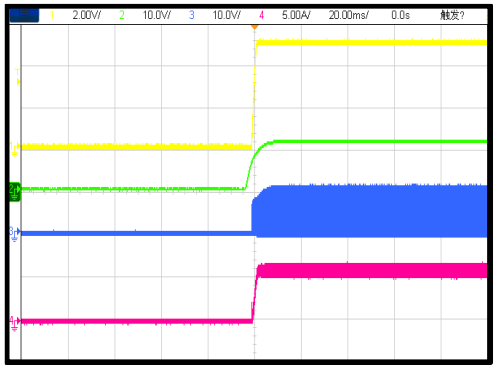


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

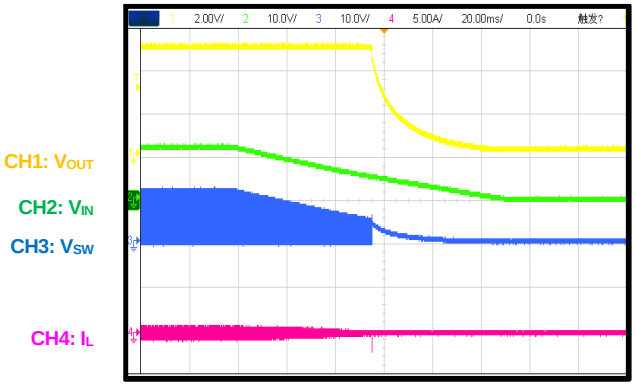
Start-Up

I_{OUT} = 6A



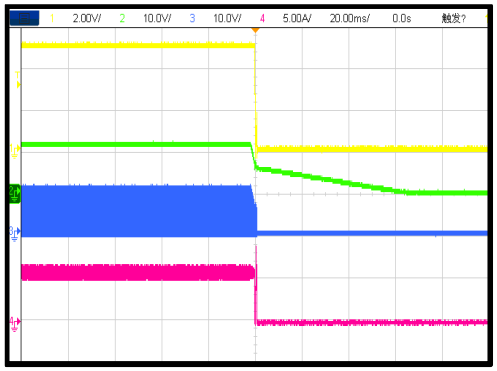
Shutdown

I_{OUT} = 0A



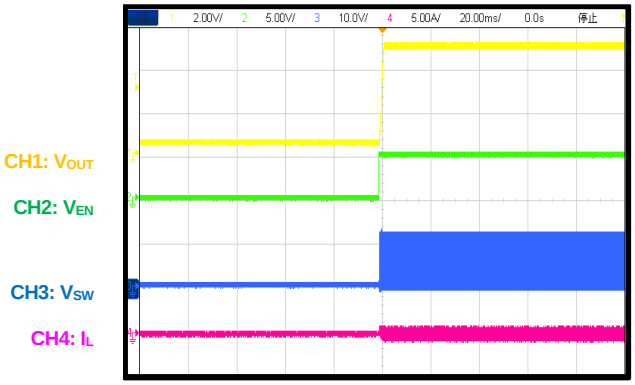
Shutdown

I_{OUT} = 6A



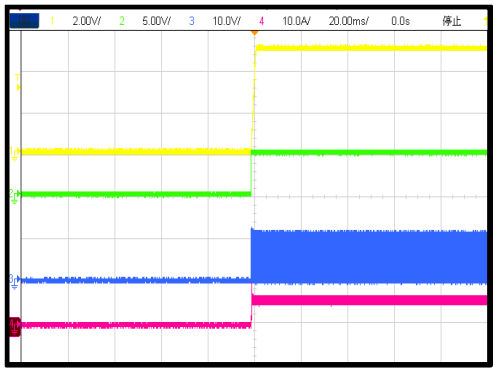
Start-Up through EN

I_{OUT} = 0A



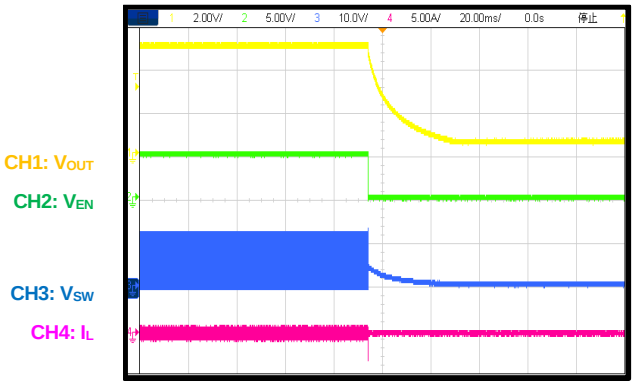
Start-Up through EN

I_{OUT} = 6A



Shutdown through EN

I_{OUT} = 0A

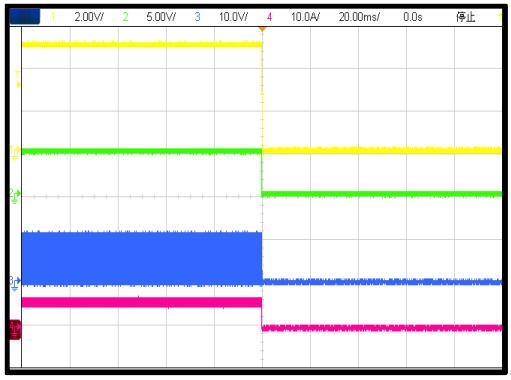


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

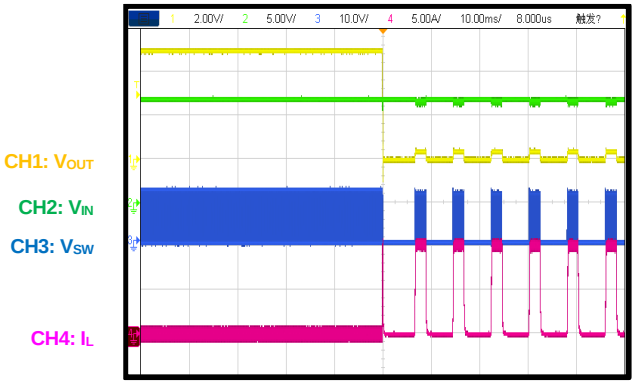
Shutdown through EN

I_{OUT} = 6A



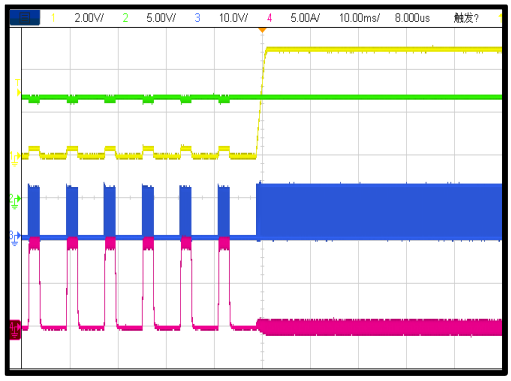
SCP Entry

I_{OUT} = 0A



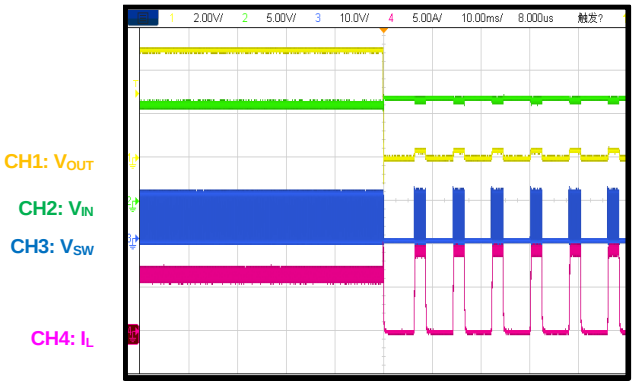
SCP Recovery

I_{OUT} = 0A



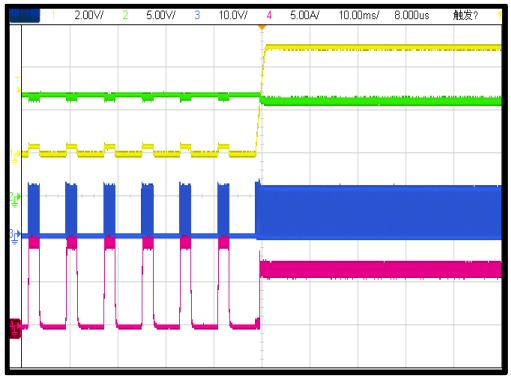
SCP Entry

I_{OUT} = 6A

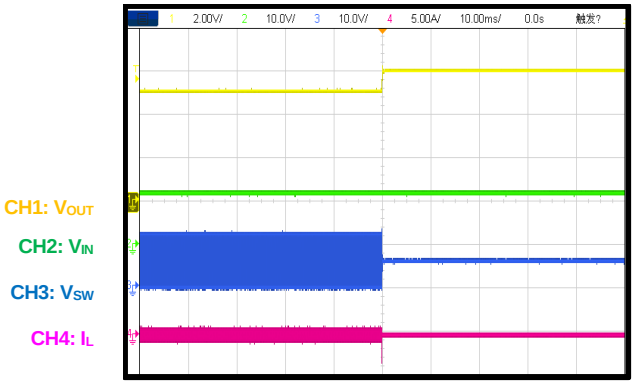


SCP Recovery

I_{OUT} = 6A



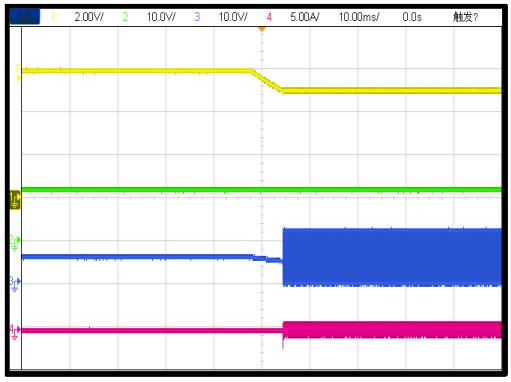
OVP Entry



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

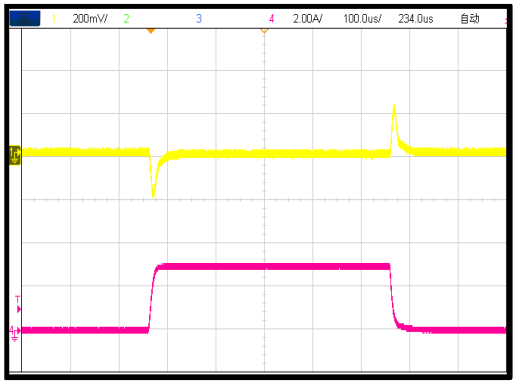
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

OVP Recovery



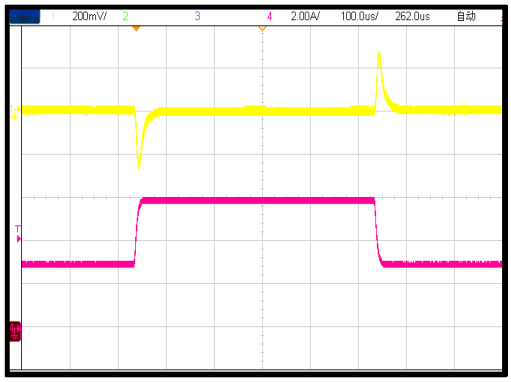
Load Transient

I_{OUT} = 0A to 3A, slew rate = 0.4A/µs

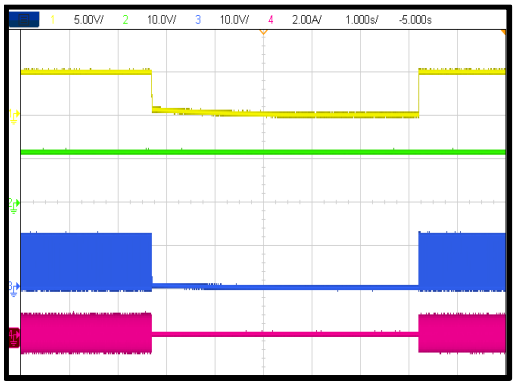


Load Transient

I_{OUT} = 3A to 6A, slew rate = 0.4A/µs

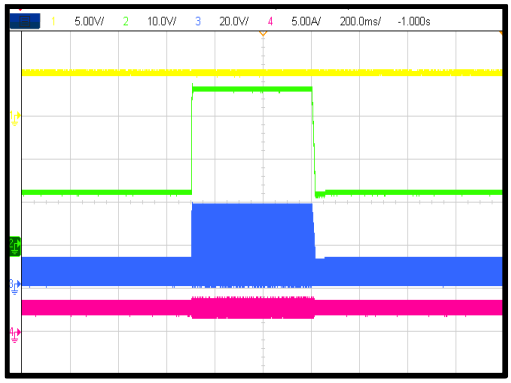


OTP Entry and Recovery



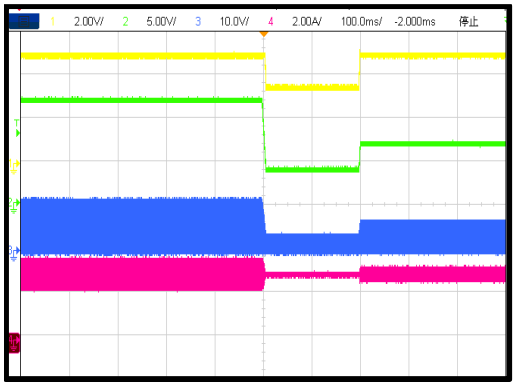
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 3A



Cold Crank

V_{IN} = 12V to 4V to 7V, I_{OUT} = 3A



FUNCTIONAL BLOCK DIAGRAM

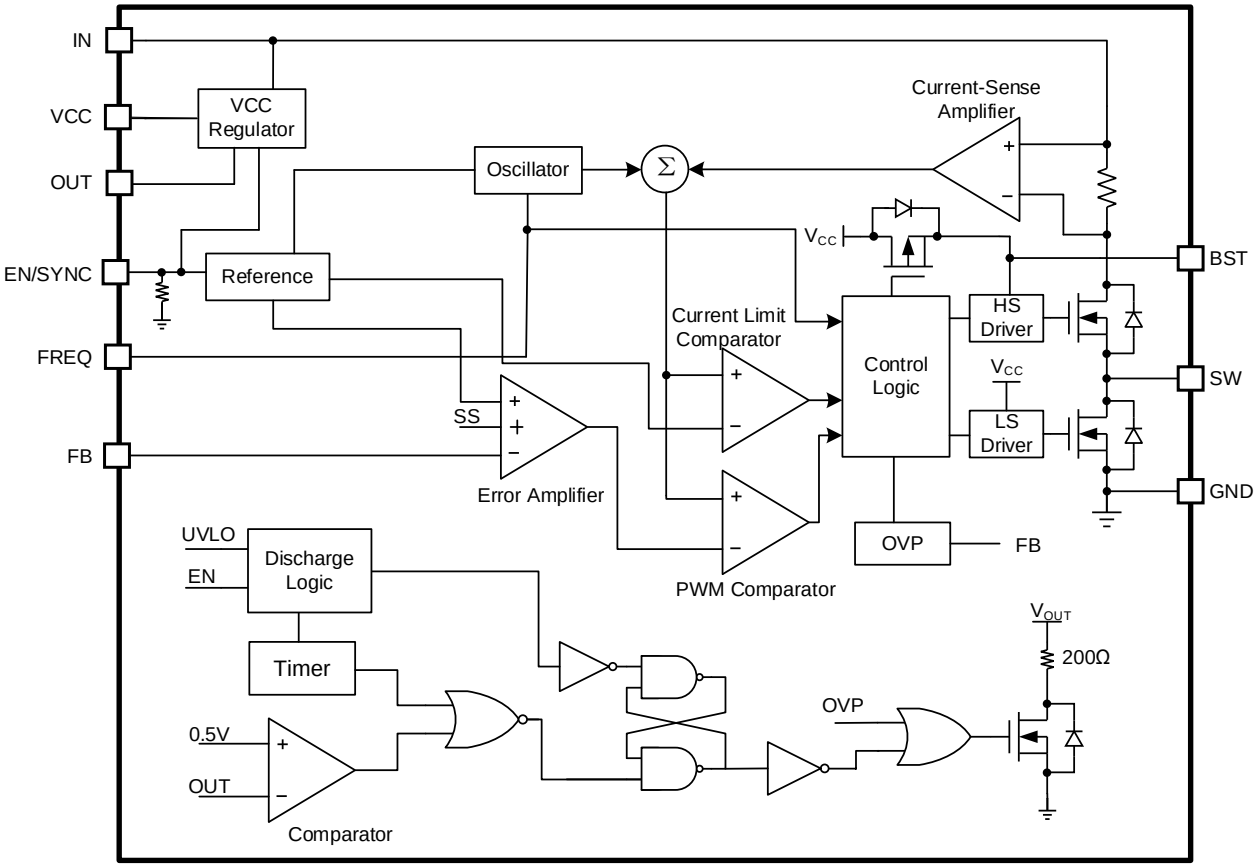


Figure 1: Functional Block Diagram

OPERATION

The MP4423C integrates a monolithic synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a compact solution to achieve up to 6A of continuous output current (I_{OUT}) across a wide input supply voltage (V_{IN}) range, with excellent load and line regulation.

The MP4423C operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). An internal clock initiates a pulse-width modulation (PWM) cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the HS-FET is off, it remains off until the next clock cycle starts. If the MOSFET current does not reach the current set by COMP within 96% of one PWM period (at a 420kHz switching frequency [f_{SW}]), the HS-FET is forced off.

Error Amplifier (EA)

The error amplifier (EA) compares the feedback (FB) voltage (V_{FB}) against the internal 0.792V reference voltage (V_{REF}) and outputs V_{COMP}. V_{COMP} controls the MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Internal VCC Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator takes either V_{OUT} or V_{IN} as its supply. When V_{IN} exceeds 5V, the regulator's output is in full regulation. If V_{IN} is below 5V, the output decreases with V_{IN}. When V_{OUT} is established and exceeds 4.75V, the VCC regulator uses V_{OUT} as its supply via the OUT pin to save LDO power loss. The VCC pins requires an external, 0.22µF to 1µF ceramic decoupling capacitor.

EN/SYNC Control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN high to turn the regulator on, drive it low to turn it off. An internal 500kΩ resistor connected between EN/SYNC and GND allows EN/SYNC to be floated to shut down the chip.

The EN pin is clamped internally using a 6.5V series Zener diode (see **Error! Reference source not found.**2). It is recommended to connect EN to VIN and GND through resistor dividers. When selecting a pull-up resistor, ensure that it has sufficient resistance to limit the current flow into EN to less than 100µA.

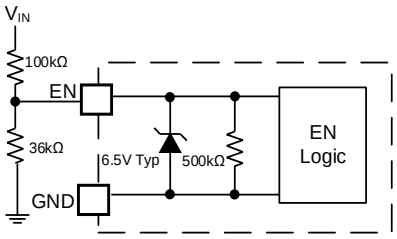


Figure 2: 6.5V Zener Diode

For example, if the EN pull-up resistor is 100kΩ, and the pull-down resistor is 36kΩ, the IC can start up when V_{IN} exceeds 6V.

Connecting the EN pin directly to a voltage source without any pull-up resistor requires limiting the voltage amplitude to less than 5.5V to prevent damage to the Zener diode.

Setting the Switching Frequency (f_{SW})

Connect an external clock with a range of 200kHz to 2.2MHz. The external clock signal's pulse width should have a duty cycle below 10%. It is recommended to float the FREQ pin when synchronizing f_{SW} with an external clock.

The FREQ pin can set be used to set f_{SW} to one of three possible options:

1. If FREQ is connected to GND, f_{SW} = 420kHz, and the device operates with frequency spread spectrum (FSS) in forced PWM (FPWM) mode.
2. If FREQ is left floating, f_{SW} = 420kHz, and the device operates with FSS in automatic pulse-frequency modulation (PFM)/PWM mode.
3. If FREQ is connected to VCC, f_{SW} = 2.2MHz, and the device operates in FSS and FPWM mode.

Auto-PFM/PWM Mode (FREQ = Floating)

The MP4423C works in continuous conduction mode (CCM) under heavy loads. As the load decreases, the MP4423C first enters

discontinuous conduction operation (DCM) and maintains a fixed frequency as long as the inductor current (I_L) approaches 0A. If the load is further decreased or there is no load and makes the peak I_L (I_{L_PEAK}) falls below the advanced asynchronous modulation (AAM) mode peak current threshold, the MP4423C enters pulse-skip mode (PSM) to further improve light-load efficiency.

Under very light loads or no load, V_{FB} decreases slowly and V_{COMP} ramps up until it trips the AAM mode voltage (V_{AAM}). When the clock goes high, the HS-FET turns on and remains on until the sensed voltage on I_L ($V_{ILSENSE}$) reaches the value set by V_{COMP}. When $V_{COMP} < V_{AAM}$, the internal clock is blocked and the MP4423C skips some pulses during PFM mode (see Figure 3). This control scheme helps achieve high efficiency by scaling down f_{SW} to reduce switching and gate driver losses.

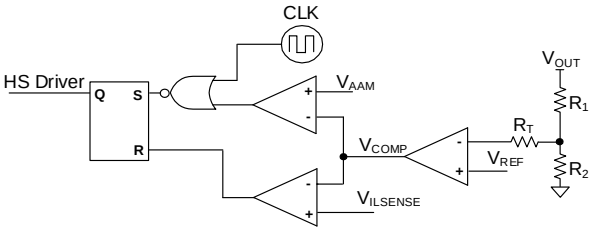


Figure 3: Auto-PFM/PWM Operation Control Logic

As I_{OUT} increases from light-load conditions, V_{COMP} and f_{SW} both increase. If I_{OUT} exceeds the critical level set by COMP, the MP4423C resumes fixed-frequency PWM control.

Forced PWM Mode (FREQ Connected to GND or VCC)

In FPWM mode, the MP4423C works in CCM mode continuously. It operates with a fixed f_{SW} regardless of whether it is operating with a light load or a full load. The advantage of CCM is the controllable f_{SW}, smaller V_{OUT} ripple, and sufficient bootstrap (BST) charge time, but it also has low efficiency under light-load conditions. A proper inductance (L) should be selected to avoid triggering the low-side MOSFET's (LS-FET's) negative current limit (typically 3A, from SW to GND). If the negative current limit is triggered, the LS-FET turns off and the HS-FET turns on once internal clock begins.

Frequency Spread Spectrum (FSS)

The purpose of FSS is to minimize the peak emissions at a specific frequency.

The MP4423C uses a 4kHz triangle wave (125μs rising, 125μs falling) to modulate the internal oscillator. The FSS span is ±10% (see Figure 4).

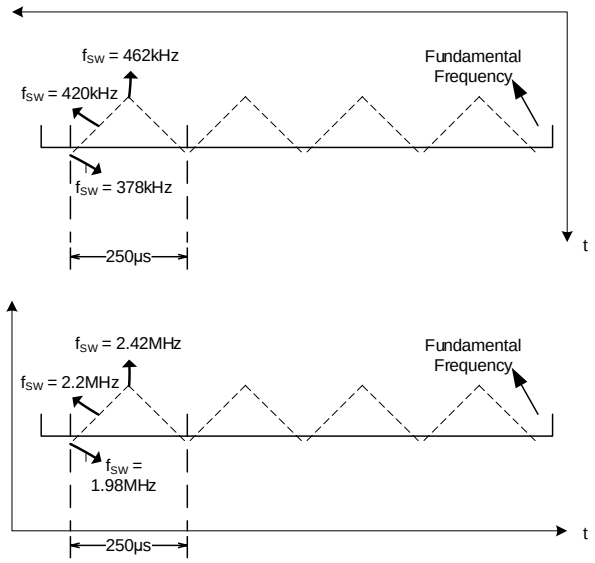


Figure 4: Frequency Spread Spectrum

Connect the FREQ pin to GND or leave it floating for a 420kHz f_{SW} with FSS. Connect the FREQ pin to VCC for a 2.2MHz f_{SW} with FSS.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors V_{IN}. The UVLO rising threshold is 3.7V; its falling threshold is 3.25V.

Internal Soft Start (SS)

Soft start (SS) prevents V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} falls below V_{REF}, the EA uses V_{SS} as the reference. When V_{SS} is above V_{REF}, the EA uses V_{REF} as the reference.

If the output of the MP4423C is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor (C_{SS}) exceeds the internal V_{FB}.

Over-Current Protection (OCP)

The MP4423C has a cycle-by-cycle over-current (OC) limit when I_{L_PEAK} exceeds the current-limit threshold, and V_{FB} drops below the under-voltage (UV) threshold (typically 50% below V_{REF}). Once under-voltage protection (UVP) is triggered, the MP4423C enters hiccup mode to periodically restart the part. This protection mode is especially useful if the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. Once the over-current condition is removed, the MP4423C exits hiccup mode and resumes normal operation.

Over-Voltage Protection (OVP)

The MP4423C detects V_{OUT} over-voltage (OV) conditions through FB. If V_{FB} exceeds than 115% of its target voltage, the over-voltage protection (OVP) comparator output goes high. If OVP is triggered, the MP4423C enters an output discharge state. Once V_{OUT} falls below 105% of its target voltage, the MP4423C auto-recovers and resumes normal operation.

Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor (C_{BST}, also called C4) powers the floating MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V with a 150mV hysteresis. The C_{BST} voltage is regulated internally by IN and VCC through D1, D2, M1, C4, L1, and C2 (see Figure 5). The C_{BST} voltage is charged up quickly by VCC through M1. The 1μA input to the BST current source can also charge C_{BST} when the LS-FET is not on.

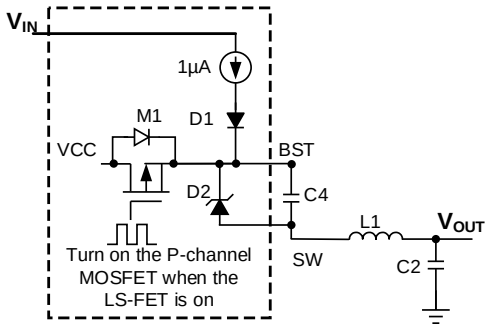


Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both VIN and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN or IN going low, or thermal shutdown. During the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Output Discharge

The MP4423C has an output discharge function that provides a resistive discharge path for the external output capacitor (C_{OUT}). Output discharge is active when any of the following conditions are true:

- The part is disabled (V_{IN} is under its UVLO threshold or EN is off)
- An OV condition occurs
- The discharge path is turned off when V_{OUT} is below 0.5V or the 200ms maximum output discharge time elapses

System

Thermal Shutdown (TSD)

Thermal shutdown (TSD) prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 165°C, the chip shuts down. Once the temperature falls below its lower threshold (typically 145°C), the chip is enabled and resumes normal operation.

APPLICATION INFORMATION

Component Selection

Setting the Output Voltage

The external resistor divider sets V_{OUT} voltage (see the Typical Application circuit on page 2). The feedback (FB) resistor (R1) also sets the FB loop bandwidth with the internal compensation capacitor. Choose R1 to be about 60.4kΩ. R2 can be calculated using Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.792V} - 1} \quad (1)$$

It is strongly recommended to use a T-type network when V_{OUT} is low (see Figure 6).

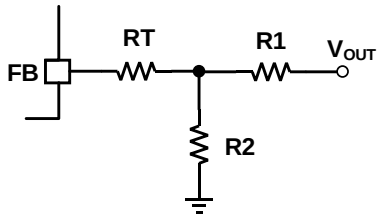


Figure 6: T-Type Network

RT+R1 is used to set the loop bandwidth. The higher the value of RT+R1, the lower the bandwidth. To ensure the loop stability, it is recommended to limit the bandwidth to less than 40kHz based on the 420kHz default f_{SW}. Table 1 lists the recommended T-type resistances for common V_{OUT} at a 420kHz f_{SW}.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
3.3	60.4	19
5	60.4	11.3
9	64.9	6.2

Selecting the Inductor

MPL Optimized Performance with MPS Inductor MPL-AY1050-4R7 Series

For most applications, it is recommended to use an inductor with a DC current rating at least 25% greater than the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. The inductance for most designs can be calculated with Equation (2):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose ΔI_L to be approximately 30% to 50% of the maximum load current. The maximum inductor peak current ($I_{L(MAX)}$) can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Typically, a 4.7μH inductance is recommended a for 420kHz f_{SW}, and a 2.2μH inductance for a 2.2MHz f_{SW}.

Table 2: Recommended Inductors

Part Number	Inductance	Manufacturer
MPL-AY1050-4R7	4.7μH	MPS
MPL-AY1050-6R8	6.8μH	MPS
MPL-AY1050-100	10μH	MPS

Selecting the Buck Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC V_{IN}. Use low-ESR capacitors for optimal performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

Since the input capacitor (C_{IN}, also called C1) absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor (I_{C1}) can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose C_{IN} to have an RMS current rating greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum or ceramic. When using an electrolytic capacitor, place two

additional, high-quality ceramic capacitors as close to the IN pin as possible. Estimate the V_{IN} ripple (ΔV_{IN}) caused by the capacitance with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC V_{OUT}. Estimate the V_{OUT} ripple (ΔV_{OUT}) with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of C_{OUT}.

For an electrolytic capacitor, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The characteristics of C_{OUT} affect the stability of the regulatory system. It is recommended to use ceramic capacitors for a low ΔV_{OUT} and good control loop stability. For polymer or tantalum capacitors, a 100µF capacitor with an ESR below 50mΩ and a 10µF ceramic capacitor are recommended.

Setting V_{IN} Under-Voltage Lockout (UVLO)

The MP4423C has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.7V, and the falling threshold is about 3.25V. If the application requires a higher UVLO point, an external resistor divider between EN/SYNC and IN can be used to achieve a higher equivalent UVLO threshold (see Figure 7).

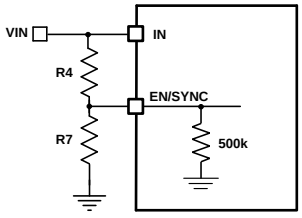


Figure 7: Adjustable UVLO Using the EN/SYNC Divider

The UVLO rising and falling thresholds can be calculated with Equation (9) and Equation (10), respectively:

$$V_{IN\_UV\_RISING} = (1 + \frac{R4}{500k\Omega // R7}) \times V_{EN\_RISING} \quad (9)$$

$$V_{IN\_UV\_FALLING} = (1 + \frac{R4}{500k\Omega // R7}) \times V_{EN\_FALLING} \quad (10)$$

Where V_{EN_RISING} is 1.4V, and $V_{EN\_FALLING}$ is 1.25V.

Ensure that R4 is large enough to limit the current flowing into EN/SYNC below 100µA.

PCB Layout Guidelines [9]

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 8 and follow guidelines below:

1. Place the high-current paths (GND, IN, and SW) as close as possible to the device with short, direct, and wide traces.
2. Place C_{IN} as close to the IN and GND pins as possible.
3. Place the VCC decoupling capacitor (C_{VCC}) as close to VCC as possible. Add three or more vias on C_{VCC}'s GND node.
4. Use a large copper plane for GND. Add multiple vias to improve thermal dissipation.
5. Route SW and BST away from sensitive analog areas such as FB.

Note:

9) The recommended PCB layout is based on Figure 9 on page 20.

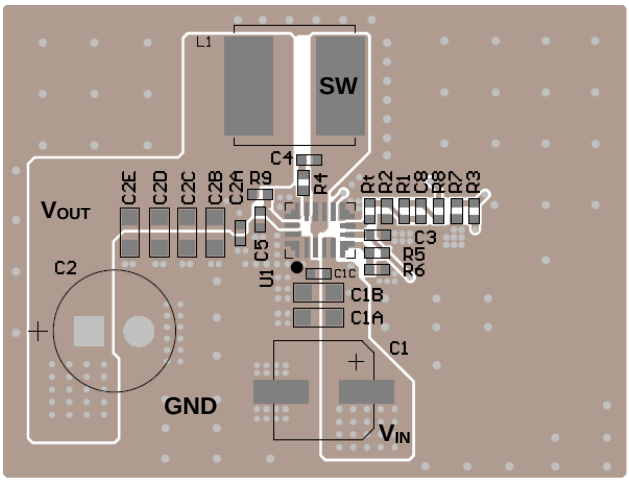


Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

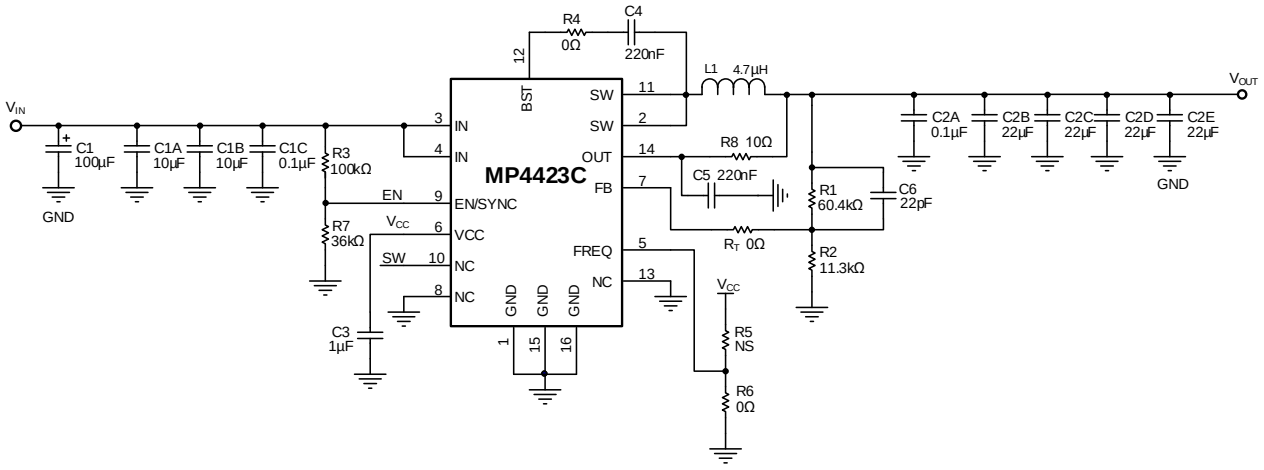


Figure 9: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, f_{SW} = 420kHz with Frequency Spread Spectrum)

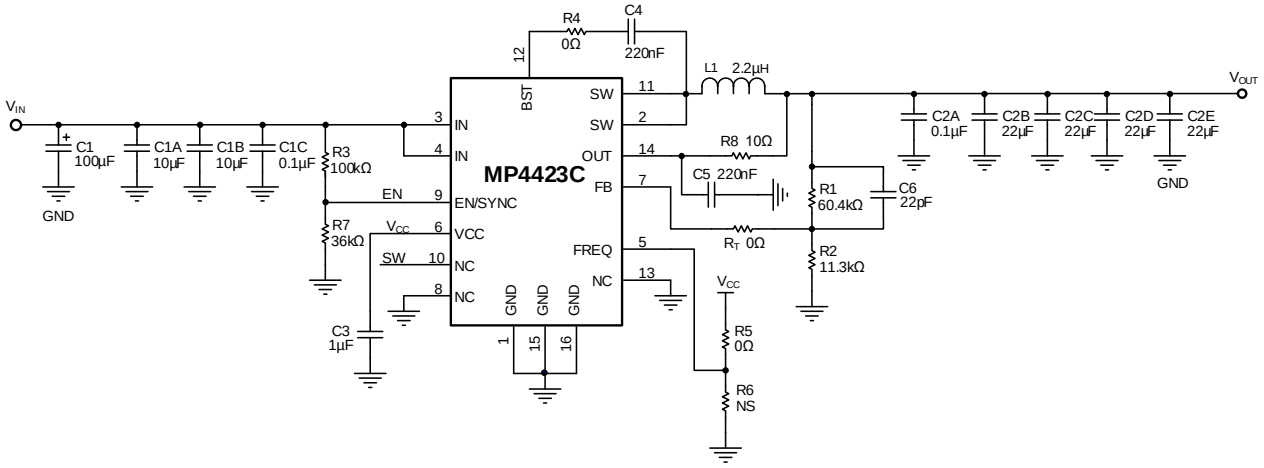


Figure 10: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 2.2MHz with Frequency Spread Spectrum)

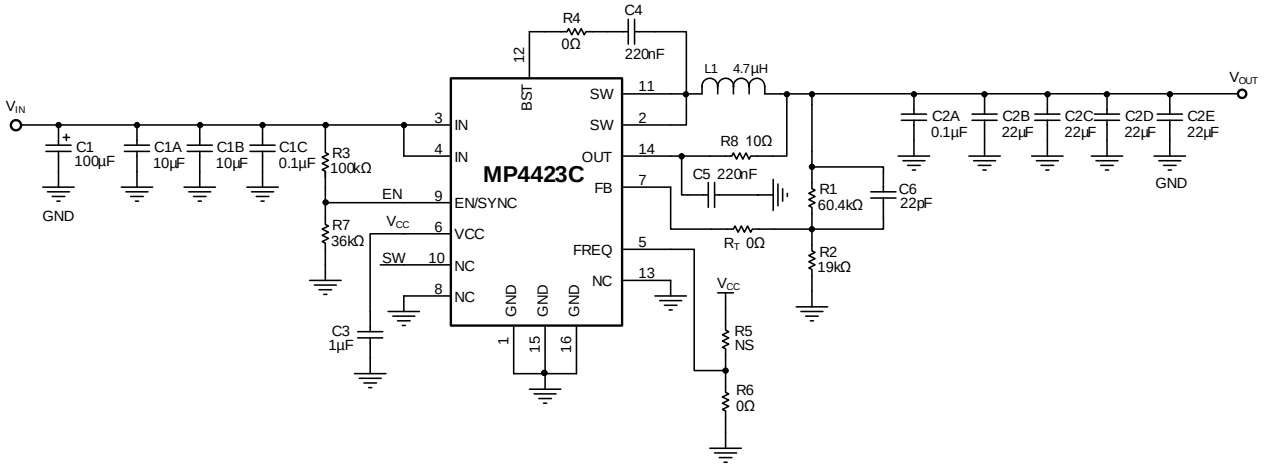


Figure 11: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 6A, f_{SW} = 420kHz with Frequency Spread Spectrum)

TYPICAL APPLICATION CIRCUITS *(continued)*

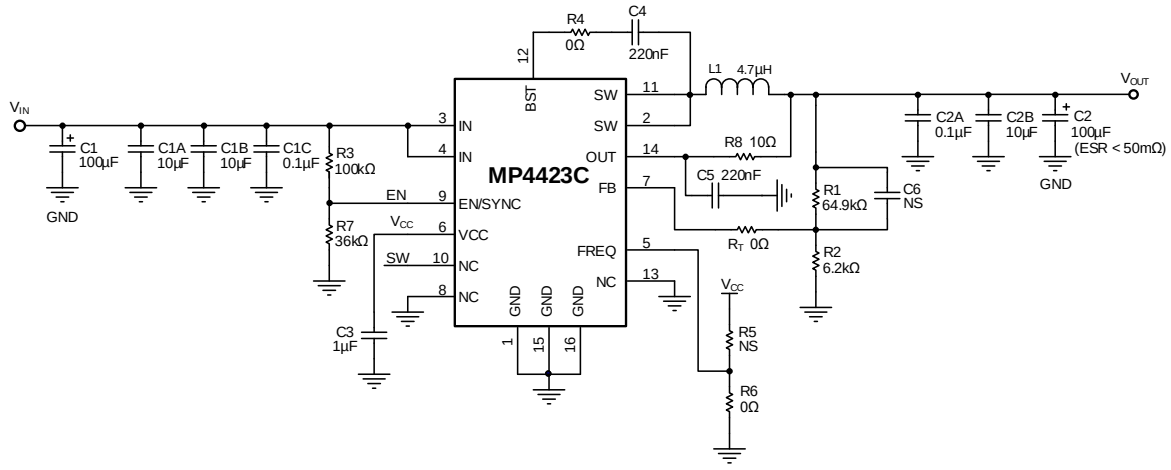
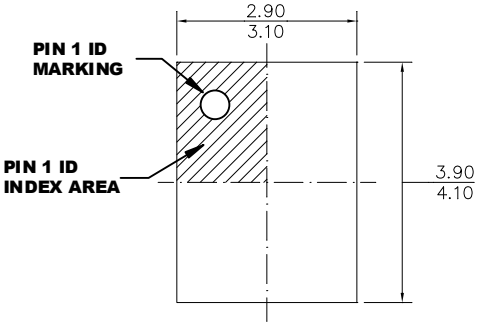


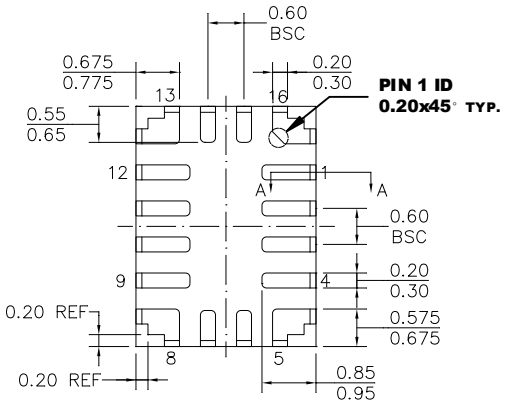
Figure 12: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 9V, I_{OUT} = 6A, f_{SW} = 420kHz with Frequency Spread Spectrum)

PACKAGE INFORMATION

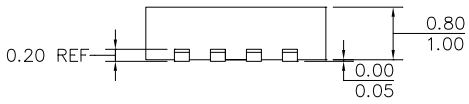
QFN-16 (3mmx4mm)



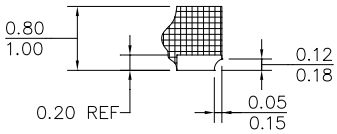
TOP VIEW



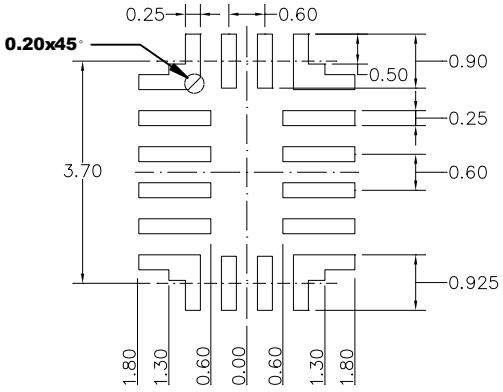
BOTTOM VIEW



SIDE VIEW



SECTION A-A

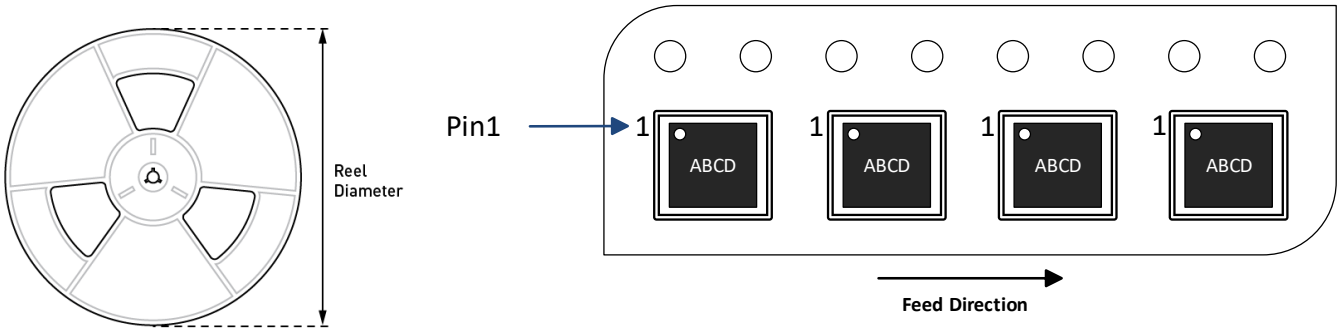


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4423CGLE-Z	QFN-16 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/3/2025	Initial Release	-