MP4316A

45V, 6A, Low-I_Q, Synchronous Step-Down Converter with Frequency Spread Spectrum

DESCRIPTION

The MP4316A is a frequency-configurable, synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs. The device provides 6A (or less) of highly efficient output current (I_{OUT}) with current mode control for fast loop response.

The wide 3.3V to 45V input voltage (V_{IN}) range accommodates a variety of step-down applications in automotive input environments. A 1.7µA shutdown mode quiescent current allows the device to be used in battery-powered applications.

The device achieves high power conversion efficiency across the wide load range by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce the switching and gate driving losses.

An open drain power good signal indicates when the output is within 95% to 105% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

The device provides a high duty cycle and low-dropout mode for automotive cold-crank conditions.

The MP4316A is available in a QFN-20 (4mmx4mm) package.

FEATURES

- Designed for Automotive Applications:
  - Wide 3.3V to 45V Operating Voltage Range
  - 6A Continuous Output Current (I_{OUT})
  - 100ns Minimum On Time
  - Junction Temperature Operation from -40°C to +125°C
- Increases Battery Life:
  - 1.7µA Low Shutdown Supply Current
  - 18µA Sleep Mode Quiescent Current
  - AAM Mode Increases Efficiency under Light Loads
- High Performance for Improved Thermals:
  - Internal 48mΩ High-Side and 20mΩ Low-Side MOSFET
- Optimized for EMC/EMI:
  - 350kHz to 1000kHz Configurable Switching Frequency (f_{SW}) for Car Battery Applications
  - Can Be Synchronized to External Clock
  - Out-of-Phase Synchronized Clock Output
  - Frequency Spread Spectrum (FSS) Modulation
  - Symmetric VIN Pinout
  - CISPR25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Power Good Output
  - External Soft-Start
  - Selectable AAM Mode or FCCM
  - Low-Dropout Mode
  - Hiccup Over-Current Protection (OCP)
  - Available in a QFN-20 (4mmx4mm) Package with Wettable Flank

APPLICATIONS

- Radios
- Battery-Powered Systems
- General-Purpose Consumer Applications
- Industrial Power Systems

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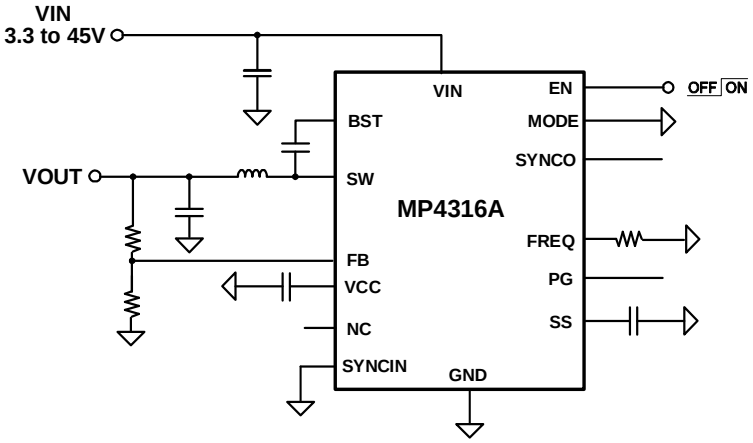
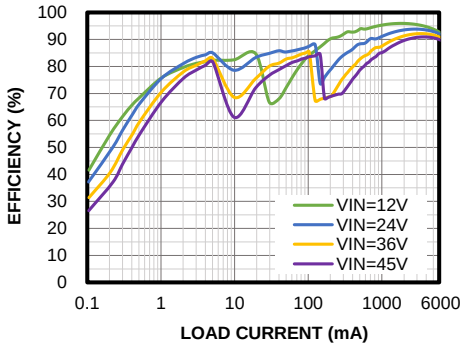
TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 470kHz, L = 4.7µH (DCR = 15mΩ), AAM mode



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MP4316AGRE***	QFN-20 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP4316AGRE-Z).

** Moisture Sensitivity Level Rating

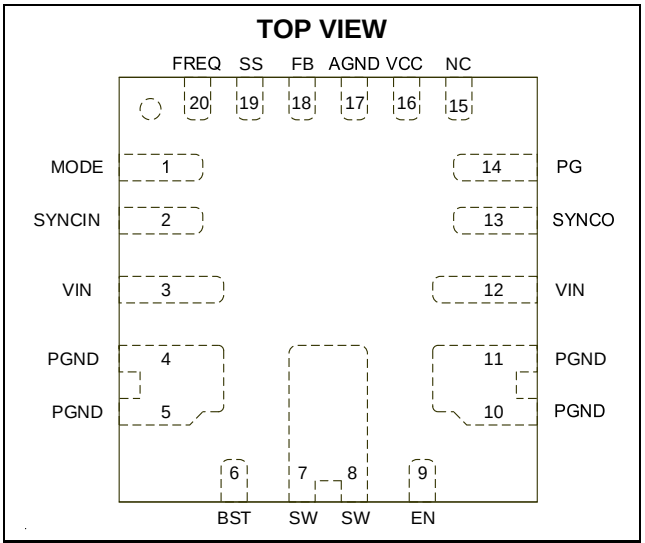
*** Wettable Flank

TOP MARKING

MPSYWW
M4316A
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M4316A: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**AAM or FCCM selection pin.** Pull MODE high to force the device to operate in forced continuous conduction mode (FCCM), or pull MODE low to force the device to operate in advanced asynchronous modulation (AAM) mode under light loads. Do not float the MODE pin.
2	SYNCIN	**SYNC input.** Apply a 350kHz to 1000kHz clock signal to the SYNCIN pin to synchronize the internal oscillator frequency to the external clock. This pin has an internal high impedance. Do not float this pin. If using the SYNCIN pin, ensure that the external sync clock has adequate pull-up and pull-down capability. It is recommended to place a ≤51kΩ resistor between the SYNCIN pin and GND if the external sync clock's pull-down capability is not sufficient, or if the pin enters a high impedance state.
3, 12	VIN	**Input supply.** VIN supplies power to all the internal control circuitry, as well as the power switch connected to SW. To minimize switching spikes, it is recommended to connect a decoupling capacitor from VIN to ground, and close to VIN.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between the BST and SW pins. To calculate the size of the capacitor, see the Selecting the External BST Diode and Resistor section on page 32.
7, 8	SW	**Switch node.** SW is the output of the internal power switch.
9	EN	**Enable.** Pull the EN pin below the specified threshold (0.85V) to shut down the chip. Pull the EN pin above the specified threshold (1V) to enable the chip.
13	SYNCO	**SYNC output.** The SYNCO pin outputs a clock signal that is 180° out of phase with the internal oscillator signal. It can also output a signal that is opposite to the clock signal applied at the SYNCIN pin. Float the SYNCO pin if it is not used.
14	PG	**Power good indicator.** The output of PG is an open drain. Use a pull-up resistor when connecting PG to a power source. PG goes high if the output voltage is within 95% to 105% of the nominal voltage. PG goes low if the output voltage is above 106.5% or below 93% of the nominal voltage.
15	NC	**Not connected.** Float the NC pin if it is not used.
16	VCC	**Bias supply.** The VCC pin supplies 4.9V to power the internal control circuit and gate drivers. Connect a decoupling capacitor from VCC to ground, and place it close to VCC. To calculate the size of the capacitor, see the Selecting the VCC Capacitor section on page 33.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** Set V_{OUT} by connecting FB to the center point between the external resistor divider from the output and AGND. The feedback threshold voltage is about 0.815V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
19	SS	**Soft-start input.** Place a capacitor from SS to GND to set the soft-start period. The MP4316A sources 13µA from SS to the soft-start capacitor (C_{SS}) at start-up. As the SS voltage rises, the feedback threshold voltage increases to limit the inrush current during start-up.
20	FREQ	**Switching frequency configuration.** Connect a resistor from FREQ to ground to set the switching frequency (f_{SW}). See the f_{SW} vs. R_{FREQ} curve on page 15 to set the frequency.

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ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN .....-0.3V to +50V
SW ..... -0.3V to $V_{IN(MAX)}$ + 0.3V
BST ..... V_{SW} + 5.5V
All other pins .....-0.3V to + 5.5V
Continuous power dissipation (T_A = 25°C) (2) (7)
QFN-20 (4mmx4mm) 5.4W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Electrostatic Discharge (ESD) Ratings

Human body model (HBM) .....Class 2 (3)
Charged device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN}) .....3.3V to 45V
Output voltage (V_{OUT})..... 0.815V to 0.95 x V_{IN}
Operating junction temp (T_J)……...
……-40°C to +125°C (5)

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (4mmx4mm)			
JESD51-7	44	9	°C/W (6)
EVQ4316A-R-00A	23	2.5	°C/W (7)

Notes:

1) Exceeding these ratings may damage the device.
2) The allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per ANSI/ESDA/JEDEC JS-001.
4) Per ANSI/ESDA/JEDEC JS-002.
5) An operating junction temperature above 125°C may be supported. Contact MPS for details.
6) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
7) Measured on an MPS standard EVB: 9cmx9cm, 2oz. copper thickness, 4-layer PCB, the value of θ_{JC} shows the thermal resistance from junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (8), typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold	IN_{UVLO_RISING}		2.8	3.0	3.2	V
V_{IN} UVLO falling threshold	$IN_{UVLO_FALLING}$		2.5	2.7	2.9	V
V_{IN} UVLO hysteresis	IN_{UVLO_HYS}			280		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
VIN quiescent current	I_Q	FB = 0.85V, no load, (sleep mode)		18	26	µA
VIN quiescent current (switching) (9)	I_{Q_ACTIVE}	MODE = GND (AAM mode), switching, no load, R_{FB_UP} = 1MΩ, R_{FB_DOWN} = 324kΩ		20		µA
		MODE = high (FCCM), switching, f_{SW} = 2MHz, no load		40		mA
		MODE = high (FCCM), switching, f_{SW} = 470kHz, no load		9.5		mA
VIN shutdown current	I_{SHDN}	EN = 0V		1.7	3.5	µA
FB reference voltage	V_{FB}	V_{IN} = 3.3V to 45V, T_J = 25°C	0.807	0.815	0.823	V
		V_{IN} = 3.3V to 45V	0.799	0.815	0.831	V
FB current	I_{FB}	V_{FB} = 0.85V,	-50	0	+50	nA
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
		R_{FREQ} = 26.1kΩ	820	1000	1180	
Minimum on time (9)	t_{ON_MIN}			100		ns
Minimum off time (9)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		1000	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		Tested under SYNCIN		180		Deg
HS current limit	I_{LIMIT}	Duty cycle = 30%	10	13	16	A
LS valley current limit	I_{LIMIT_VALLEY}		8	10	12	A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (8), typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ZCD current	I_{ZCD}	AAM mode	-0.15	0.1	+0.35	A
LS reverse current limit	$I_{LIMIT_REVERSE}$	FCCM	2	4.5	7	A
Switch leakage current	I_{SW_LKG}			0.01	1	µA
HS switch on resistance	$R_{ON(HS)}$	V_{BST} - V_{SW} = 5V		48	80	mΩ
LS switch on resistance	$R_{ON(LS)}$	V_{CC} = 5V		20	40	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	8	13	19	µA
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			190		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE_FALLING}$				0.4	V
PG rising threshold (VFB/VREF)	PG_{RISING}	V_{FB} rising	92%	95%	98%	V_{REF}
		V_{FB} falling	102%	105%	108%	
PG falling threshold (VFB/VREF)	$PG_{FALLING}$	V_{FB} falling	90.5%	93.5%	96.5%	
		V_{FB} rising	103.5%	106.5%	109.5%	
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch	$t_{PG_R_DELAY}$			35		µs
PG falling deglitch	$t_{PG_F_DELAY}$			35		µs
Thermal shutdown (9)	T_{SD}			170		°C
Thermal shutdown hysteresis (9)	T_{SD_HYS}			20		°C

Notes:

8) Not tested in production and guaranteed by over-temperature correlation.
9) Derived from bench characterization. Not tested in production.

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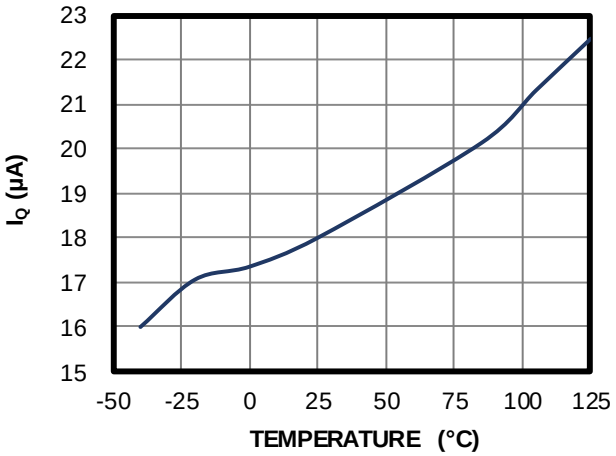
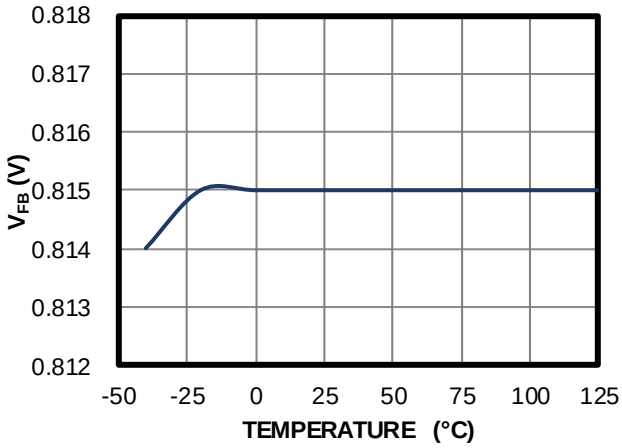
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

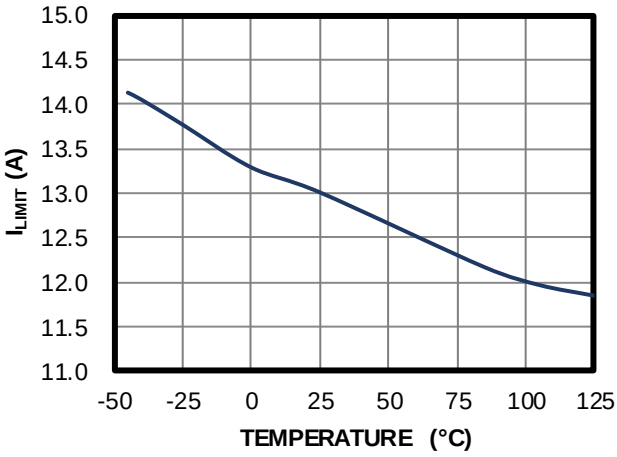
I_Q vs. Temperature



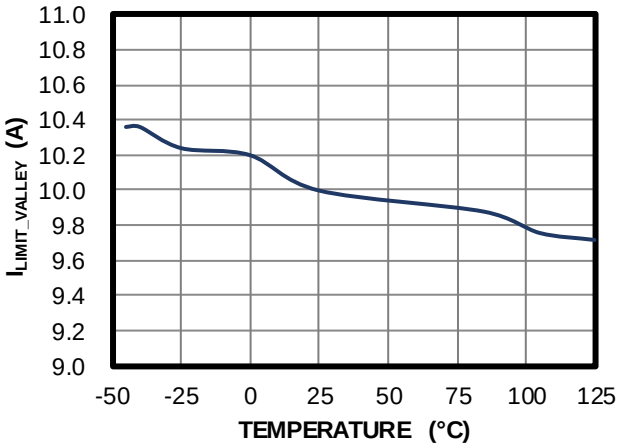
V_{FB} vs. Temperature



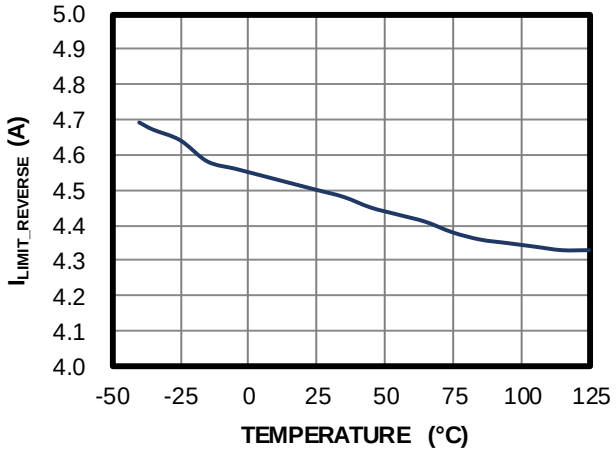
I_{LIMIT} vs. Temperature



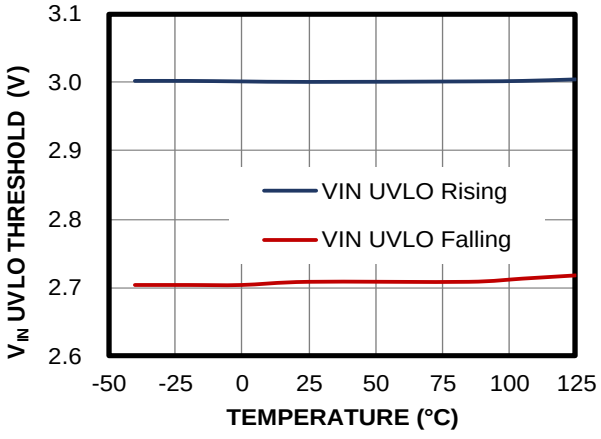
Valley Current Limit vs. Temperature



Reverse Current Limit vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



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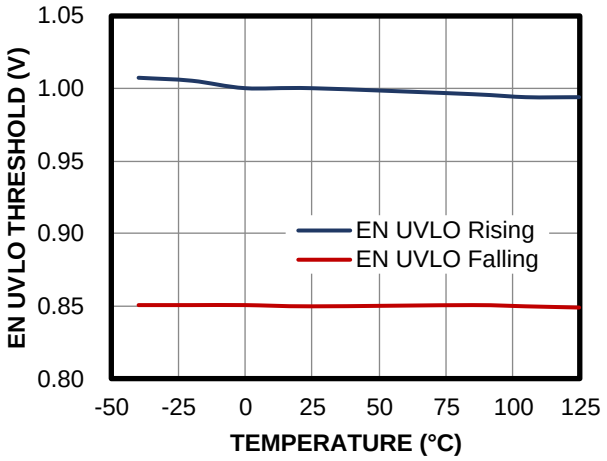
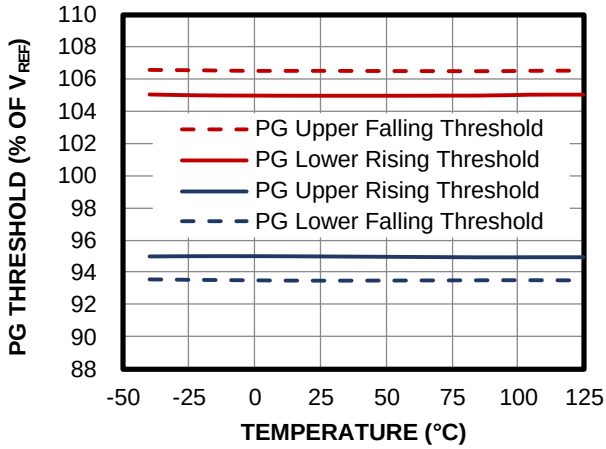
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

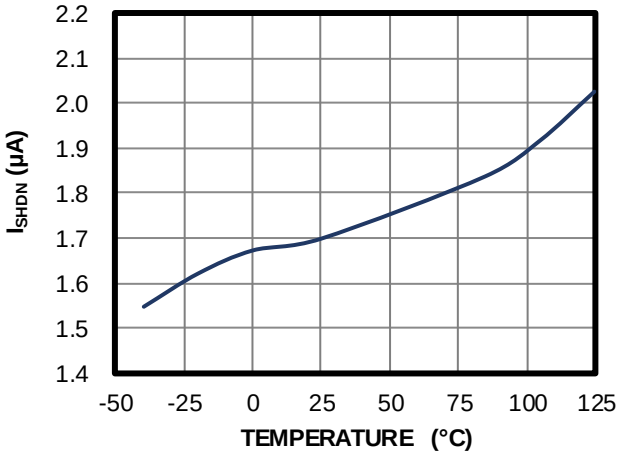
EN UVLO Threshold vs. Temperature



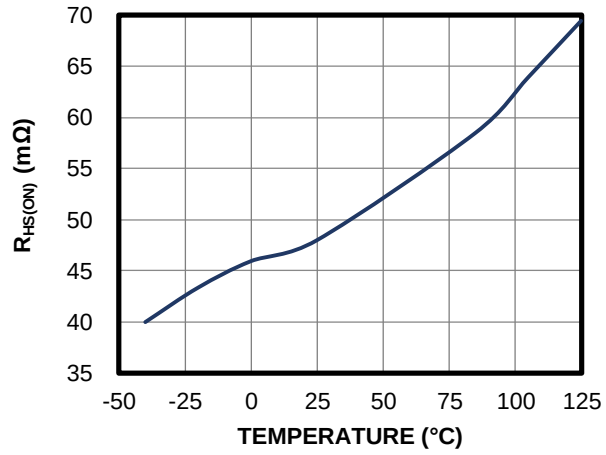
PG Rising/Falling Threshold vs. Temperature



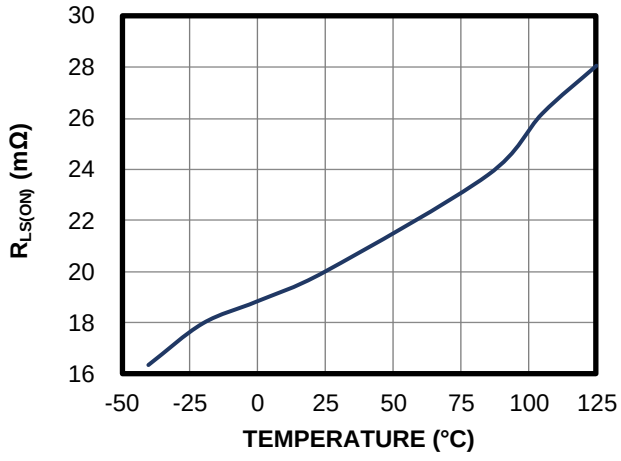
VIN Shutdown Current vs. Temperature



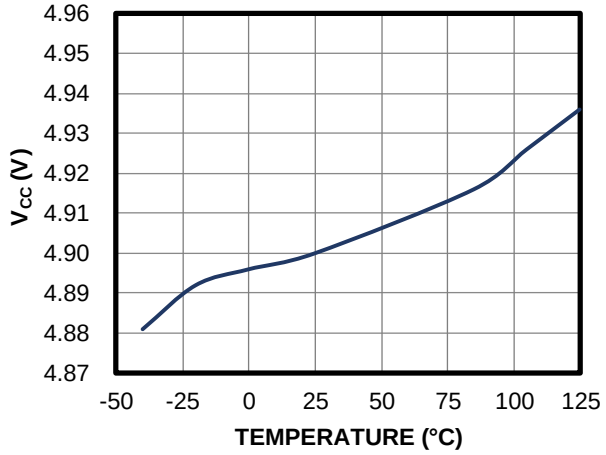
$R_{HS(ON)}$ vs. Temperature



$R_{LS(ON)}$ vs. Temperature



V_{CC} vs. Temperature



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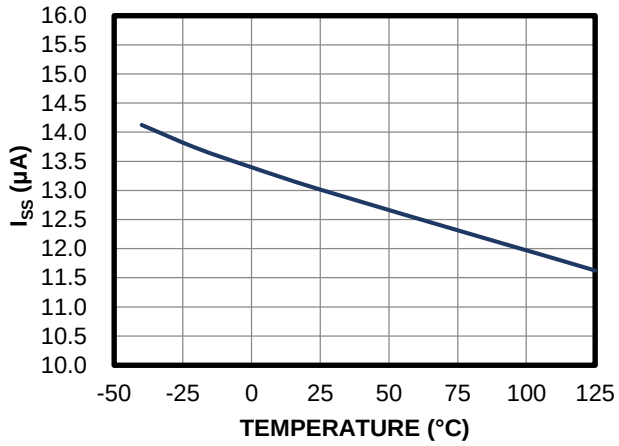
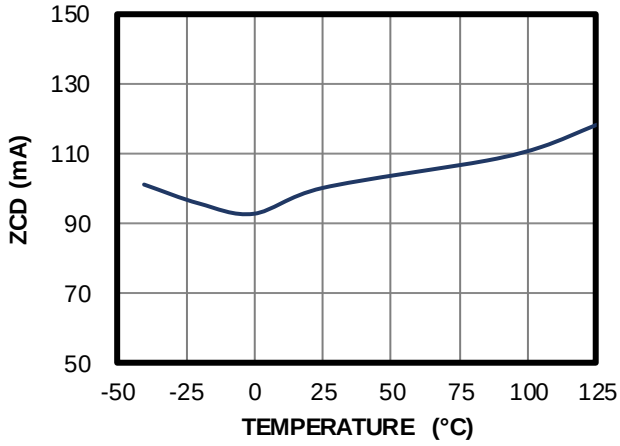
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Soft-Start Current vs. Temperature

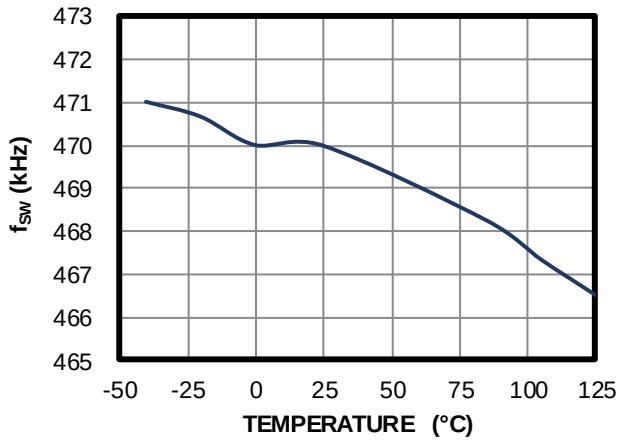


ZCD vs. Temperature



f_{SW} vs. Temperature

R_{FREQ} = 62kΩ



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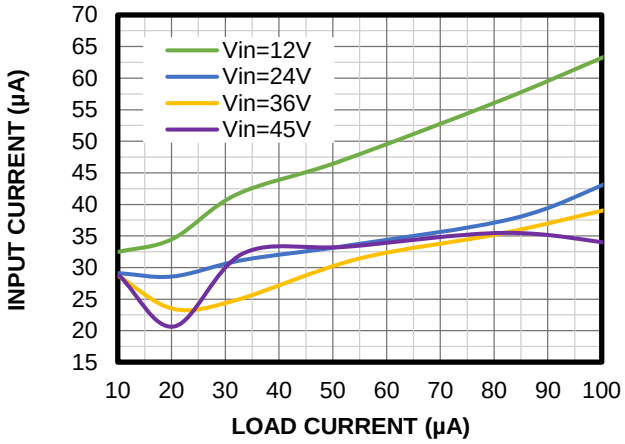
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (10), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

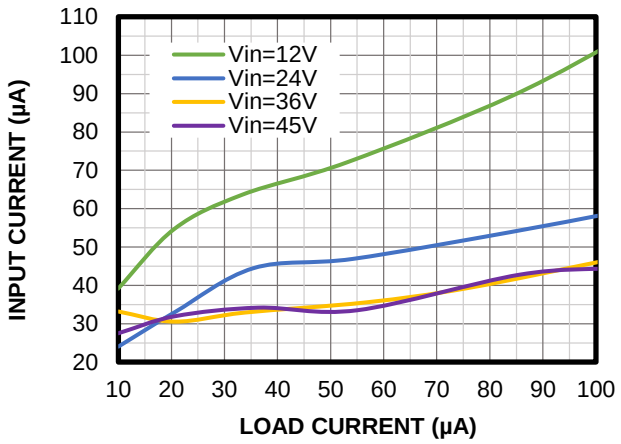
Input Current vs. Load Current

AAM mode, V_{OUT} = 3.3V



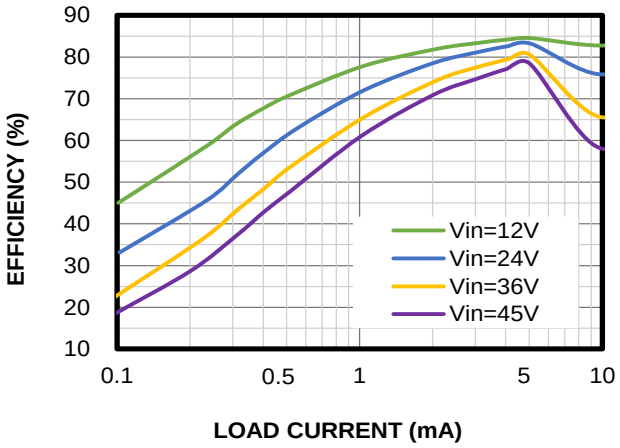
Input Current vs. Load Current

AAM mode, V_{OUT} = 5V



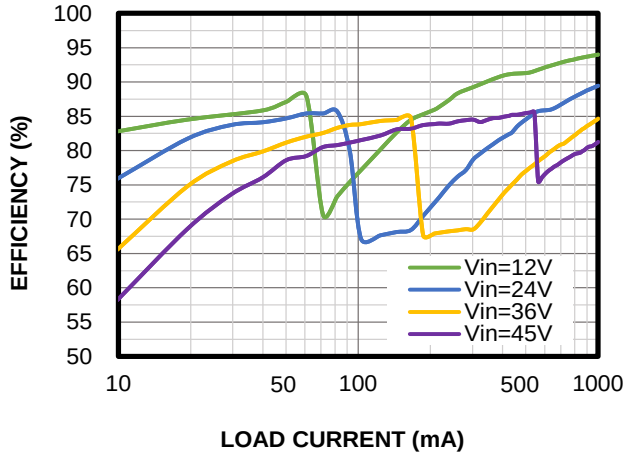
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V



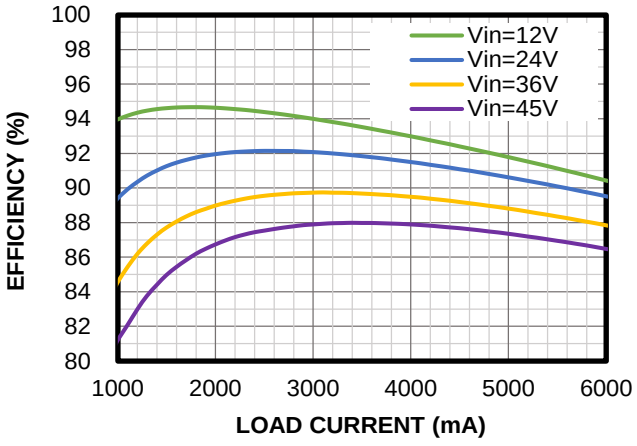
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V



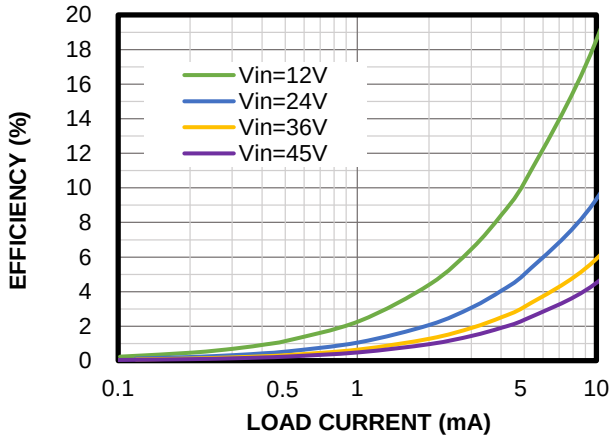
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V



Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V



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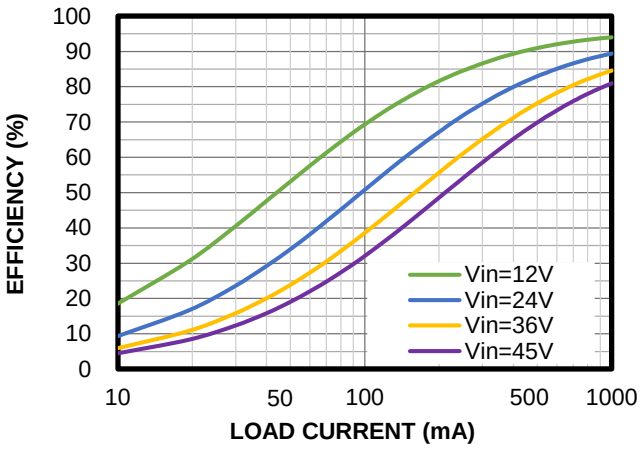
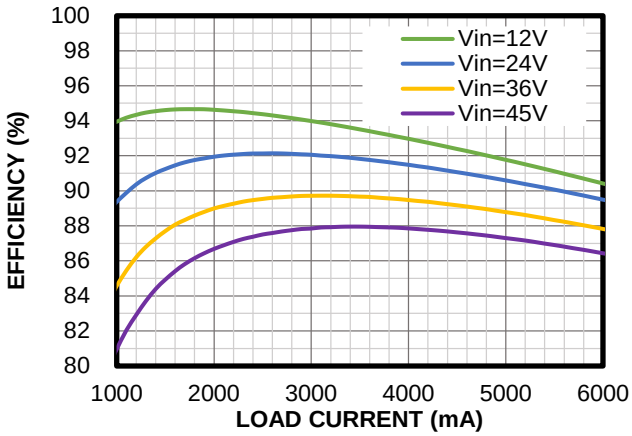
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (10), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

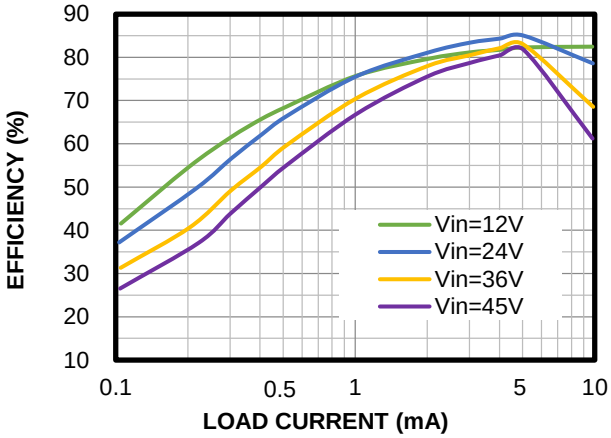
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



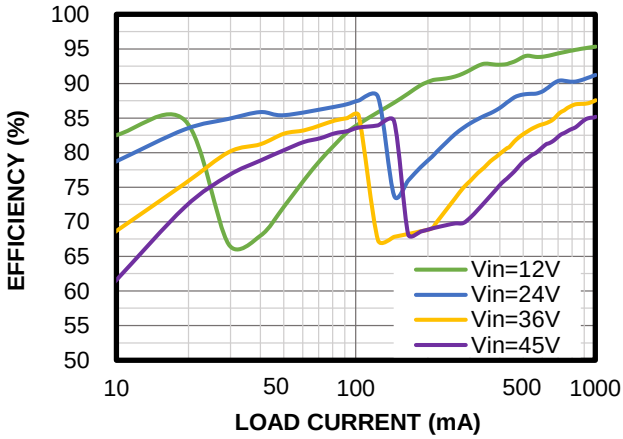
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



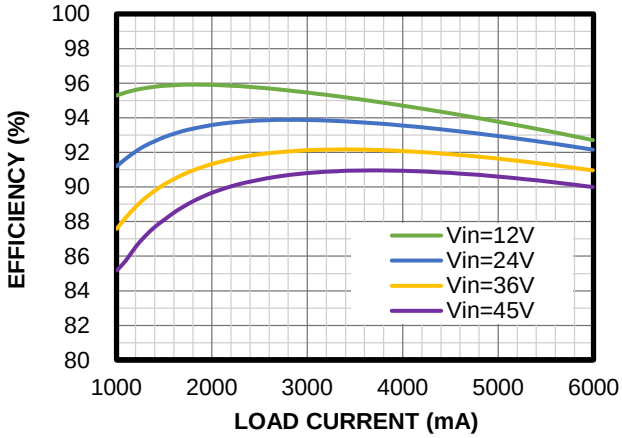
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



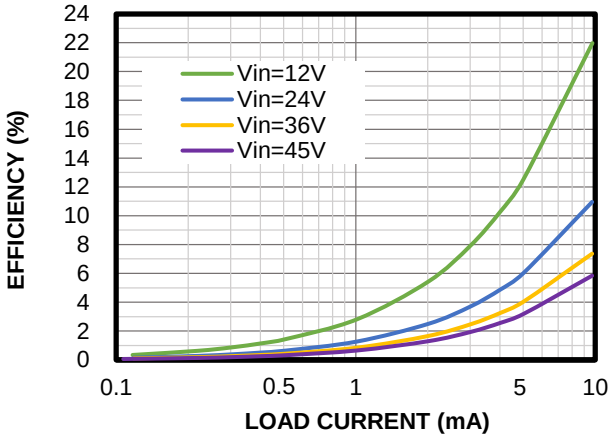
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



Efficiency vs. Load Current
FCCM, V_{OUT} = 5V



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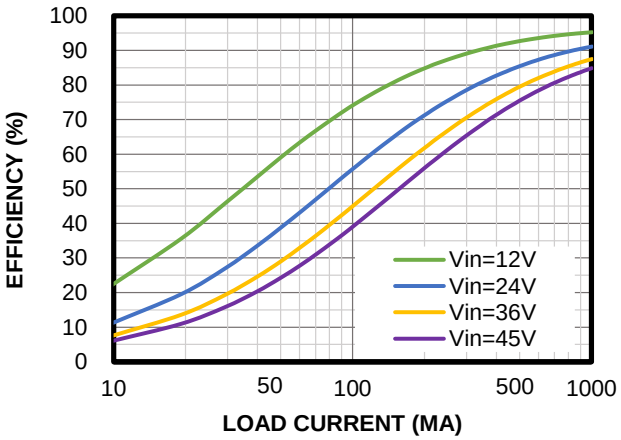
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (10), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

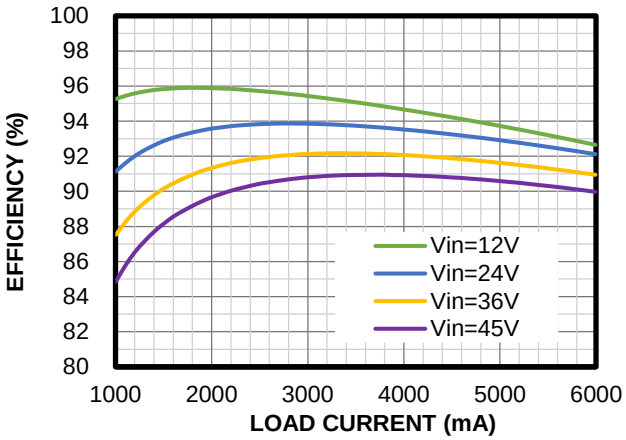
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



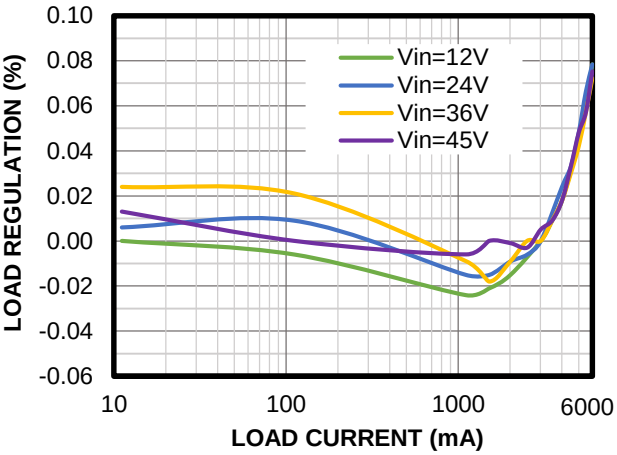
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



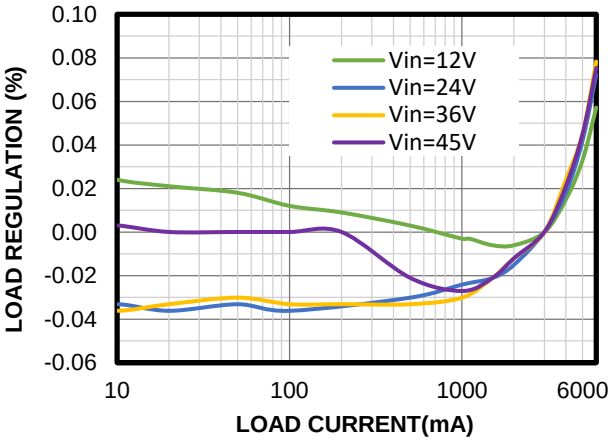
Load Regulation vs. Load Current

AAM mode, V_{OUT} = 3.3V



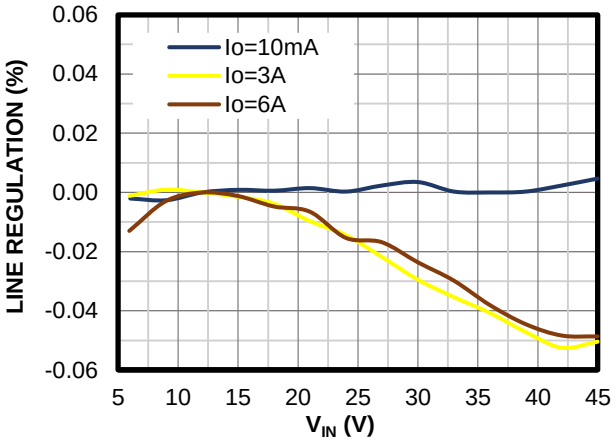
Load Regulation vs. Load Current

FCCM, V_{OUT} = 3.3V



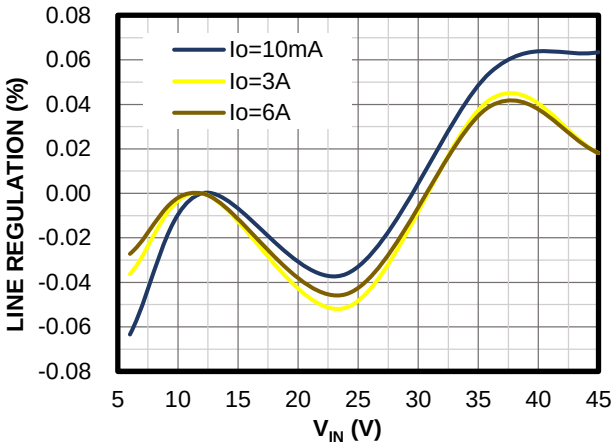
Line Regulation vs. V_{IN}

AAM mode, V_{OUT} = 3.3V



Line Regulation vs. V_{IN}

FCCM, V_{OUT} = 3.3V



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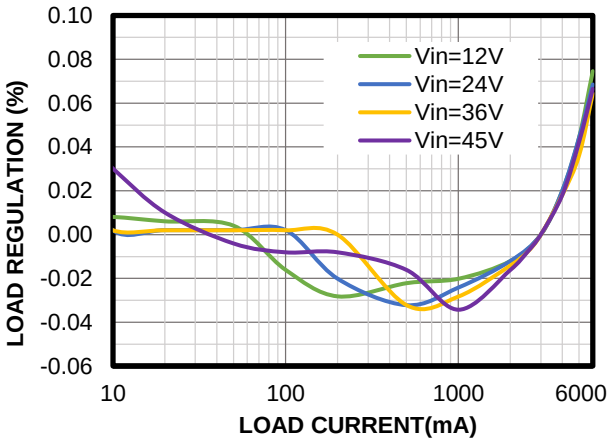
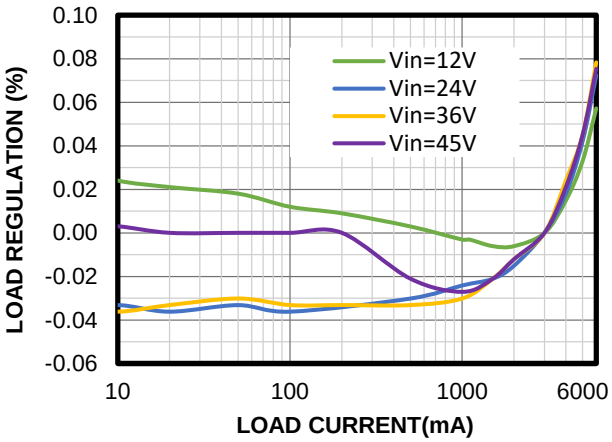
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (10), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

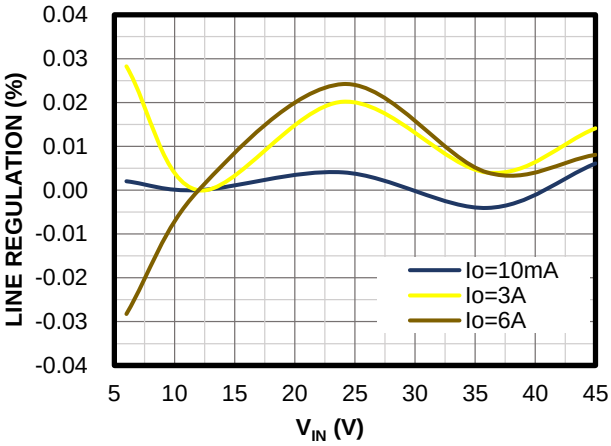
Load Regulation vs. Load Current
AAM mode, V_{OUT} = 5V



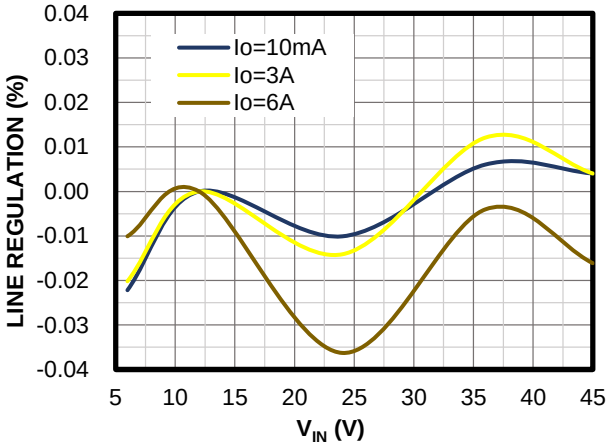
Load Regulation vs. Load Current
FCCM, V_{OUT} = 5V



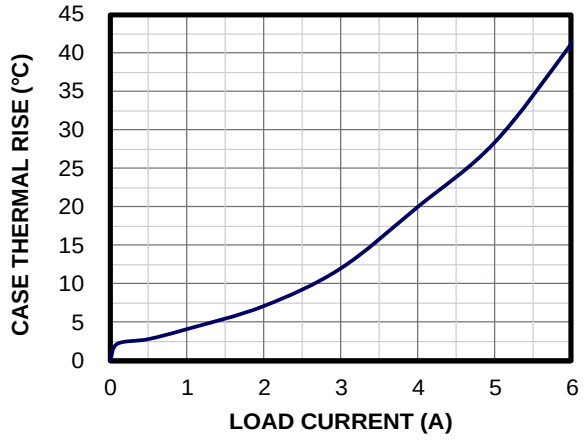
Line Regulation vs. V_{IN}
AAM mode, V_{OUT} = 5V



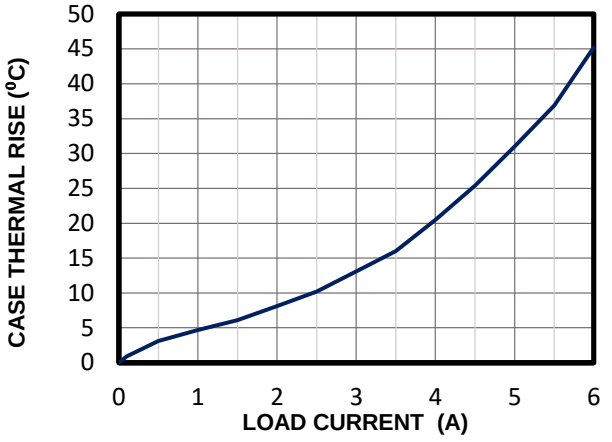
Line Regulation vs. V_{IN}
FCCM, V_{OUT} = 5V



Case Thermal Rise vs. Load Current
V_{OUT} = 3.3V



Case Thermal Rise vs. Load Current
V_{OUT} = 5V



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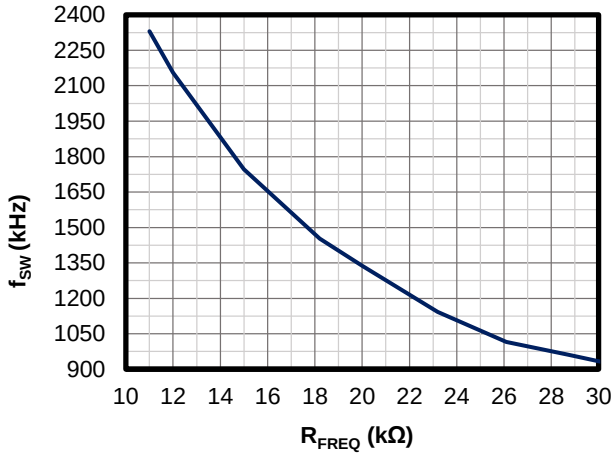
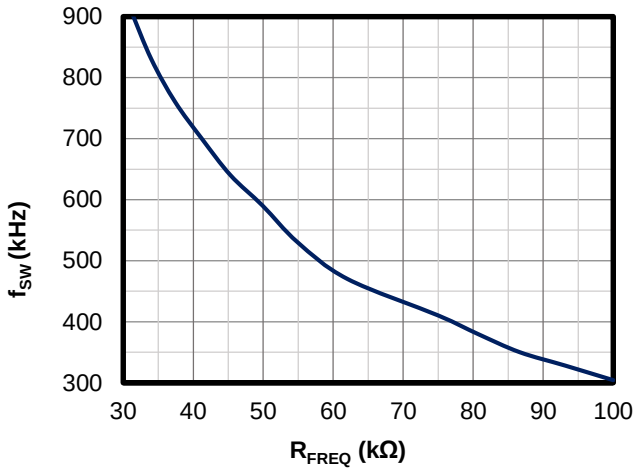
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (10), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

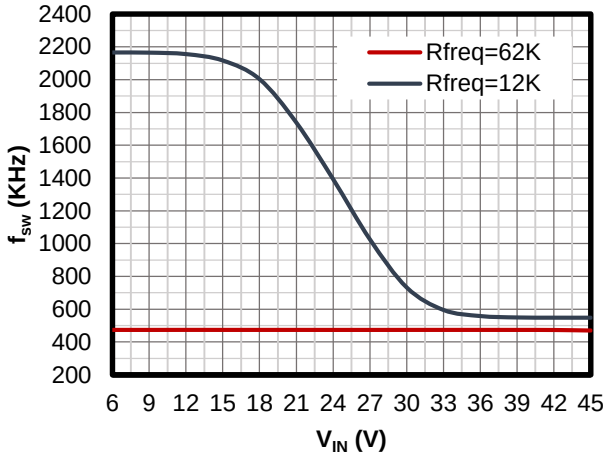
f_{SW} vs. R_{FREQ}
R_{FREQ} = 10kΩ to 30kΩ



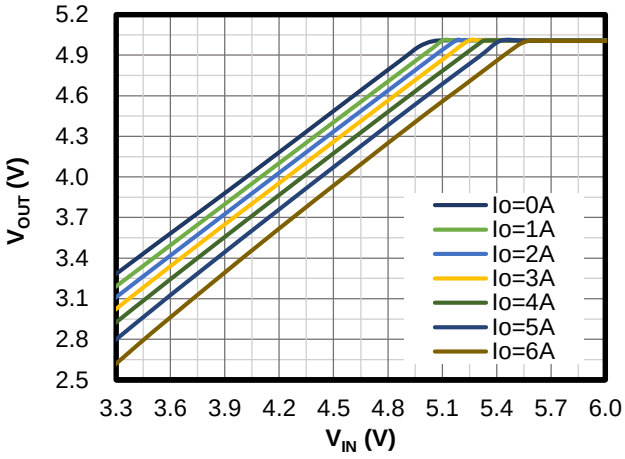
f_{SW} vs. R_{FREQ}
R_{FREQ} = 30kΩ to 100kΩ



f_{SW} vs. V_{IN}



V_{OUT} vs. V_{IN}
Low-dropout mode, V_{OUT} = 5V



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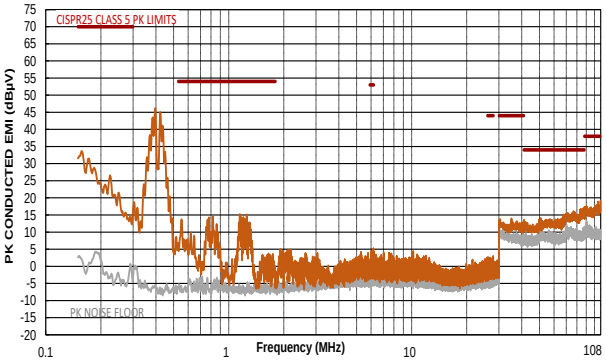
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH (10), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. (11)

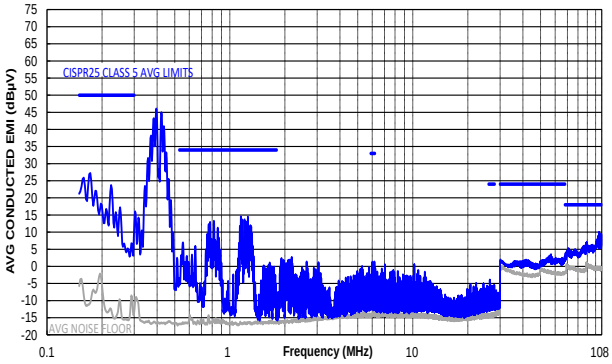
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



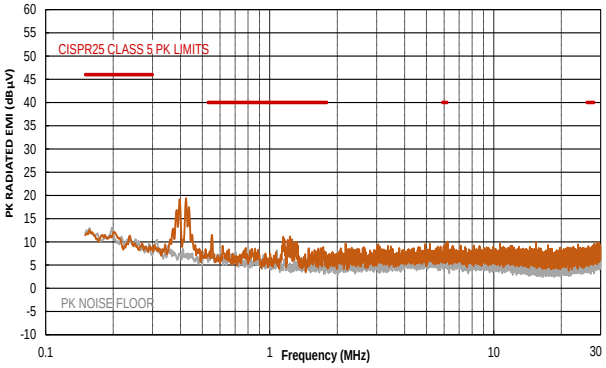
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



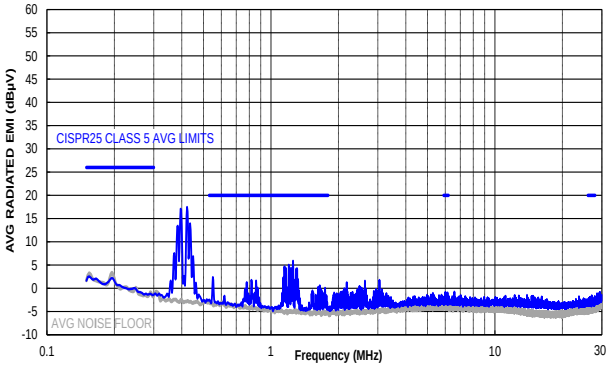
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



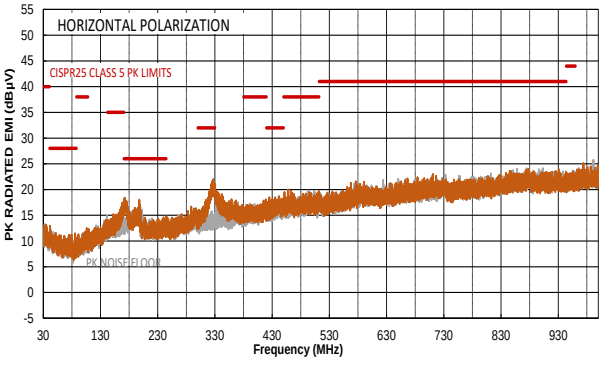
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



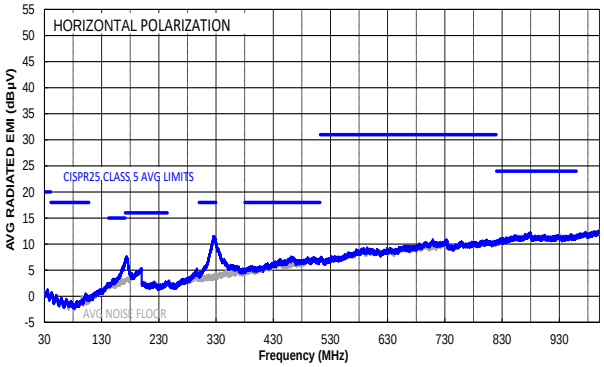
CISPR25 Class 5 Peak Radiated Horizontal

30MHz to 1GHz



CISPR25 Class 5 Average Radiated Horizontal

30MHz to 1GHz



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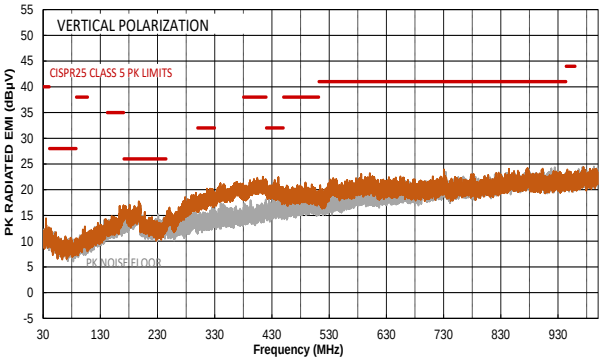
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH (10), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. (11)

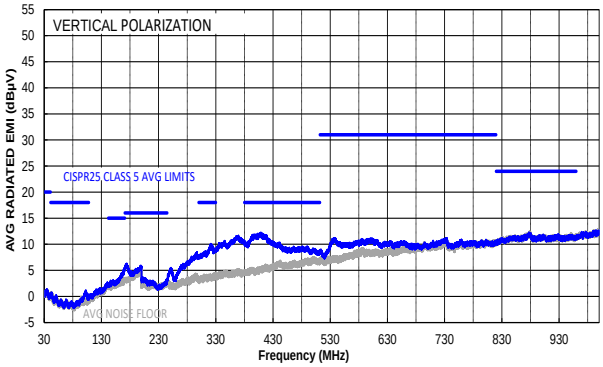
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

10) Inductor part number: XAL6060-472MEC. DCR = 15mΩ.

11) The EMC test results are based on the application circuit with EMI filters (see Figure 11 on page 34).

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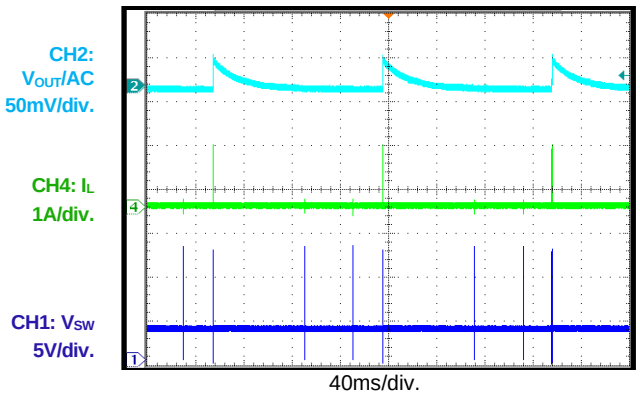
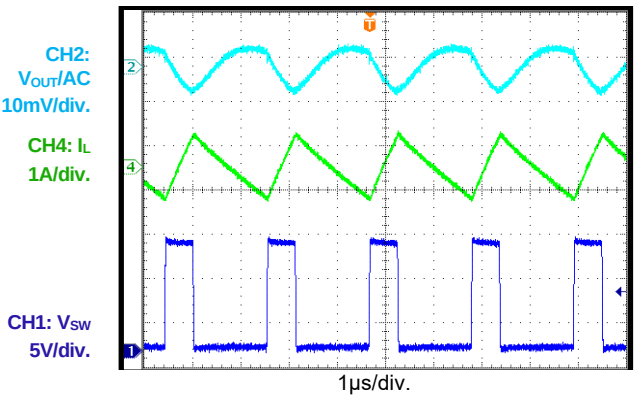
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

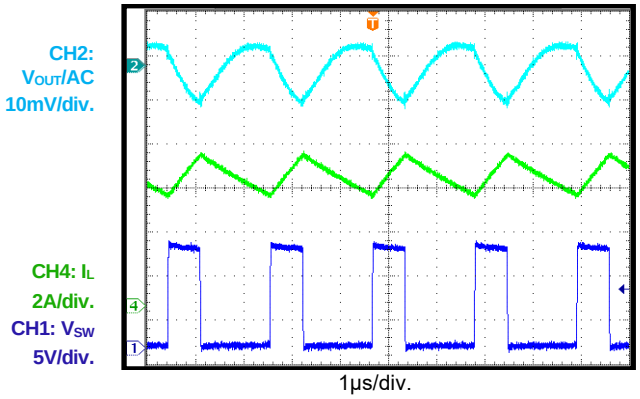
Steady State
I_{OUT} = 0A, AAM mode



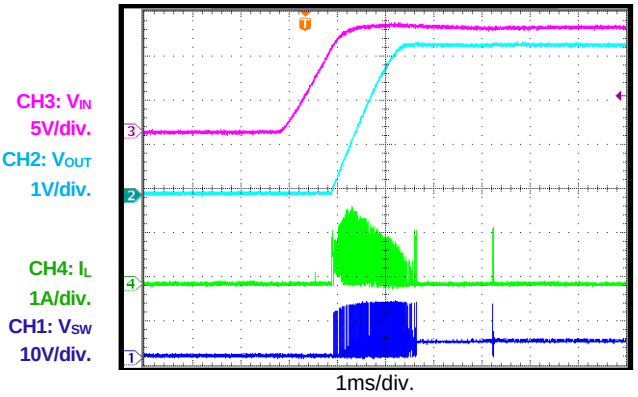
Steady State
I_{OUT} = 0A, FCCM



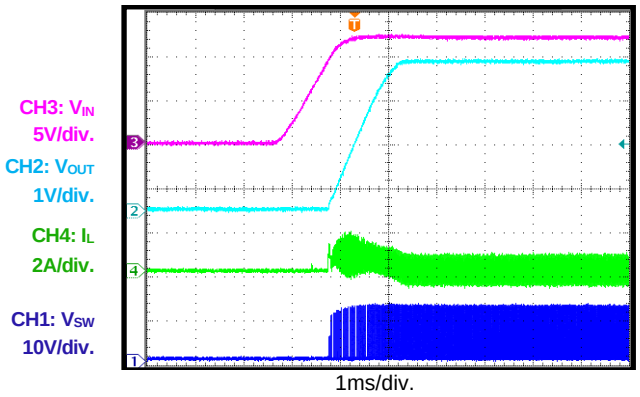
Steady State
I_{OUT} = 6A



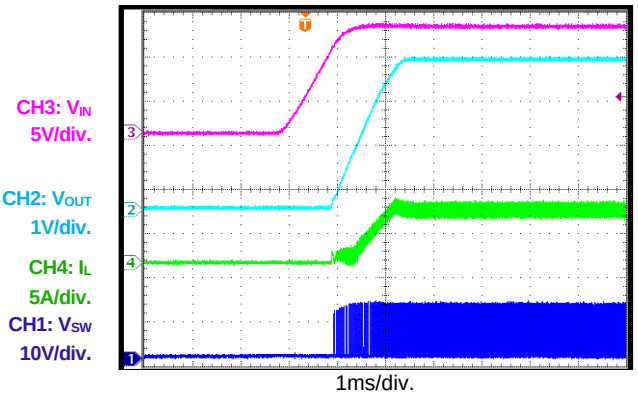
Start-Up through VIN
I_{OUT} = 0A, AAM mode



Start-Up through VIN
I_{OUT} = 0A, FCCM



Start-Up through VIN
I_{OUT} = 6A



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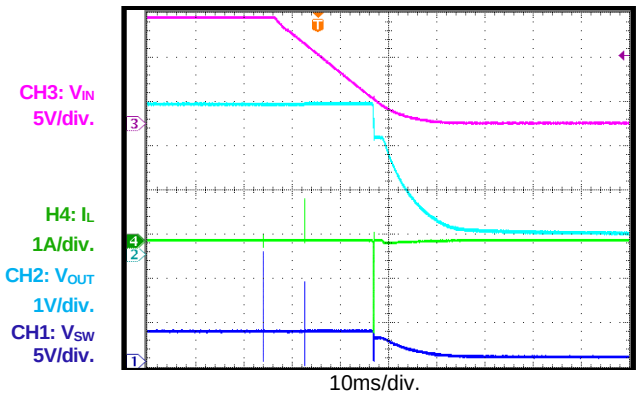
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

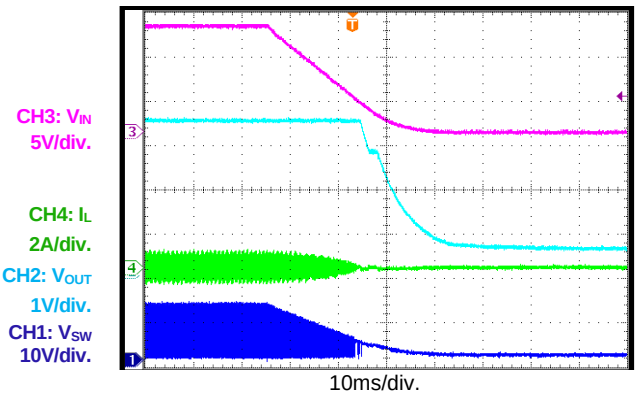
Shutdown through VIN

I_{OUT} = 0A, AAM mode



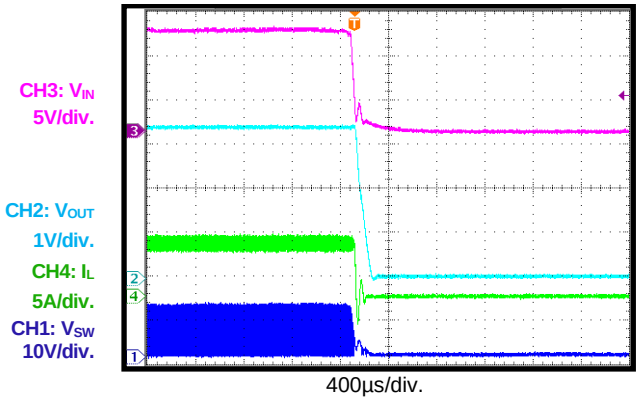
Shutdown through VIN

I_{OUT} = 0A, FCCM



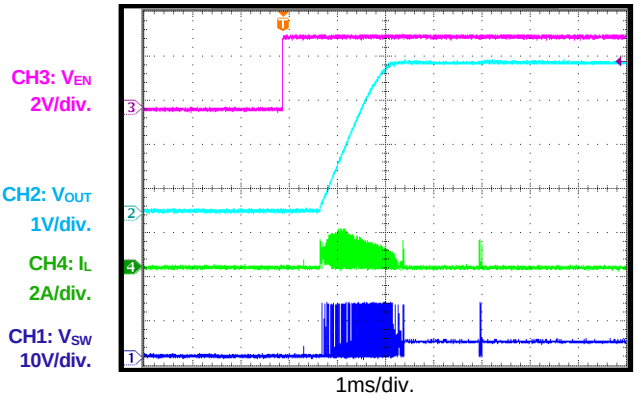
Shutdown through VIN

I_{OUT} = 6A



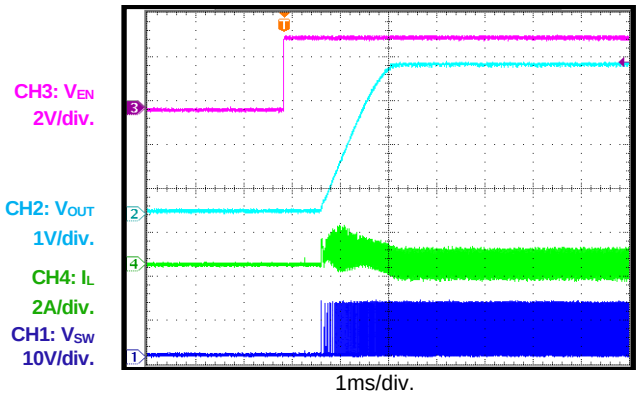
Start-Up through EN

I_{OUT} = 0A, AAM mode



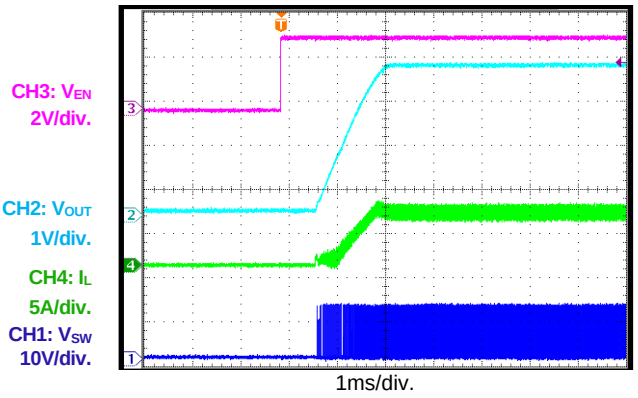
Start-Up through EN

I_{OUT} = 0A, FCCM



Start-Up through EN

I_{OUT} = 6A



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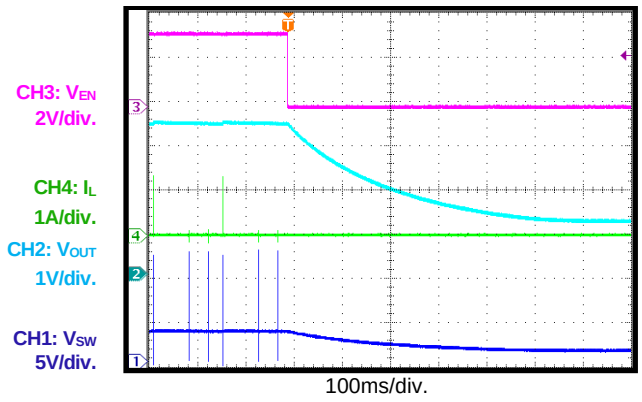
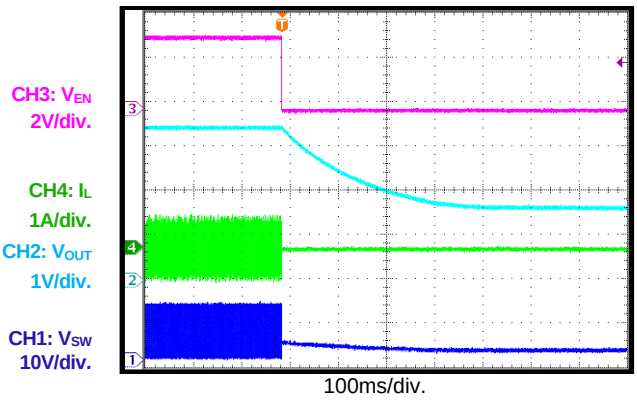
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

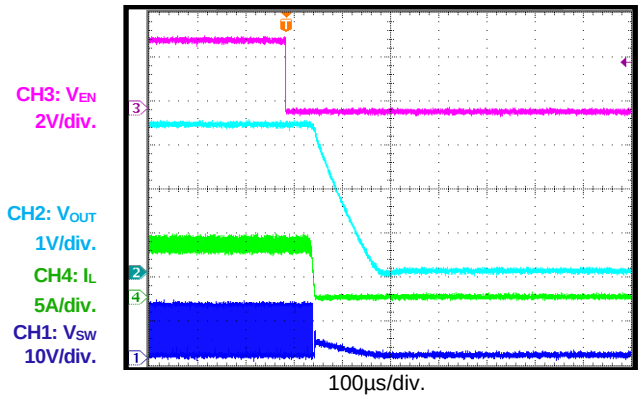
Shutdown through EN
I_{OUT} = 0A, AAM mode



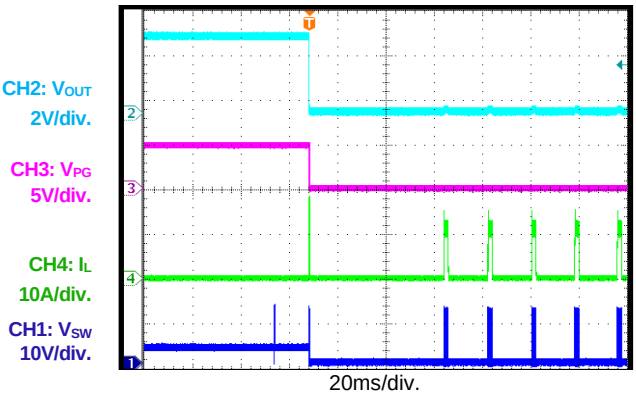
Shutdown through EN
I_{OUT} = 0A, FCCM



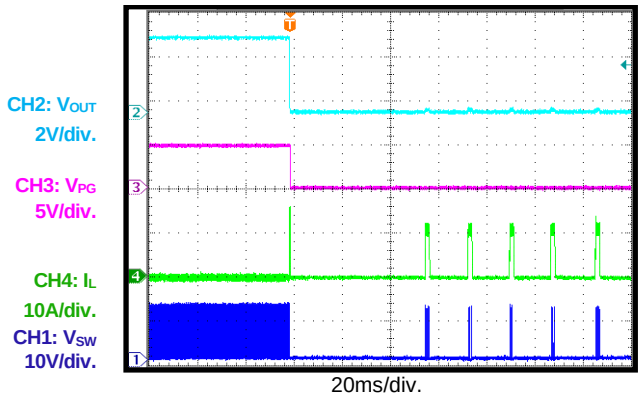
Shutdown through EN
I_{OUT} = 6A



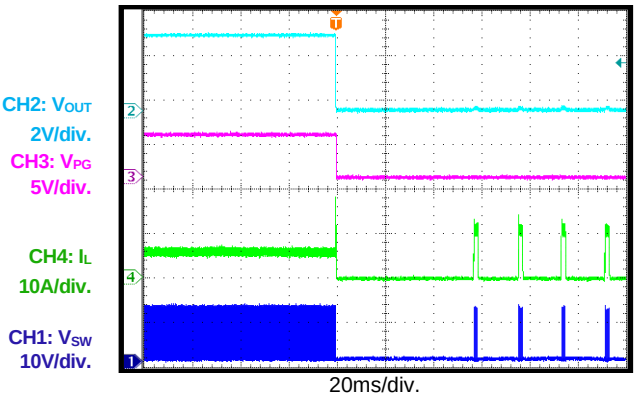
SCP Entry
I_{OUT} = 0A, AAM mode



SCP Entry
I_{OUT} = 0A, FCCM



SCP Entry
I_{OUT} = 6A



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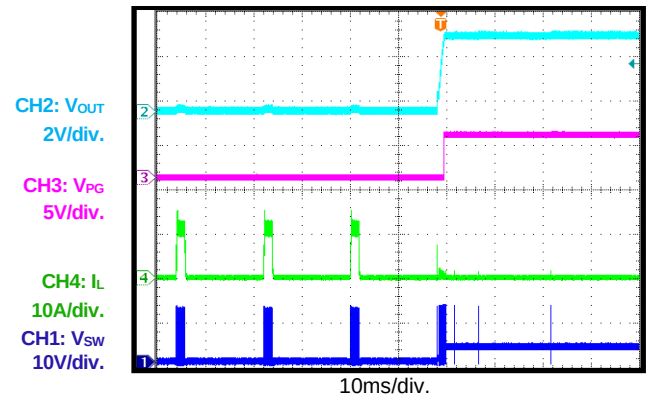
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

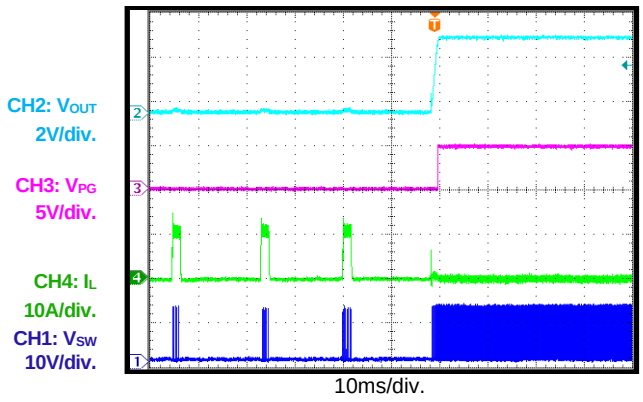
SCP Recovery

I_{OUT} = 0A, AAM mode



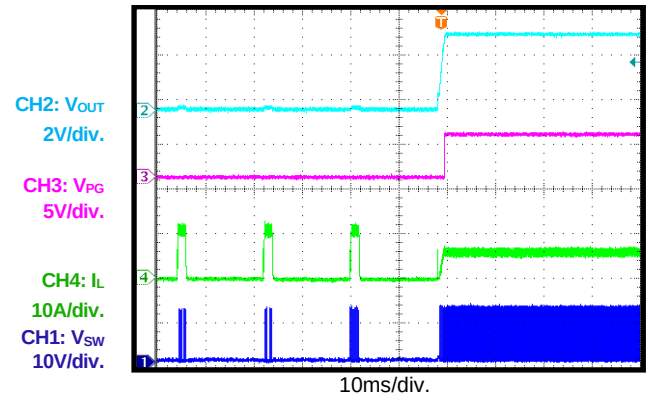
SCP Recovery

I_{OUT} = 0A, FCCM

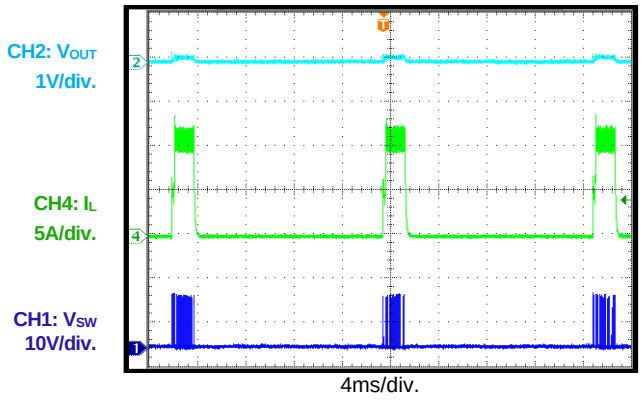


SCP Recovery

I_{OUT} = 6A

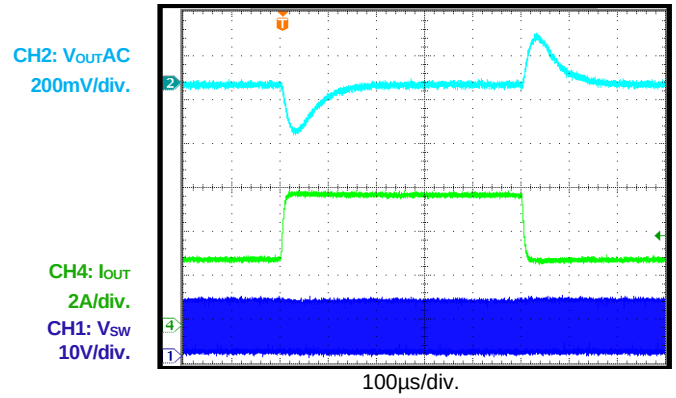


SCP Steady State



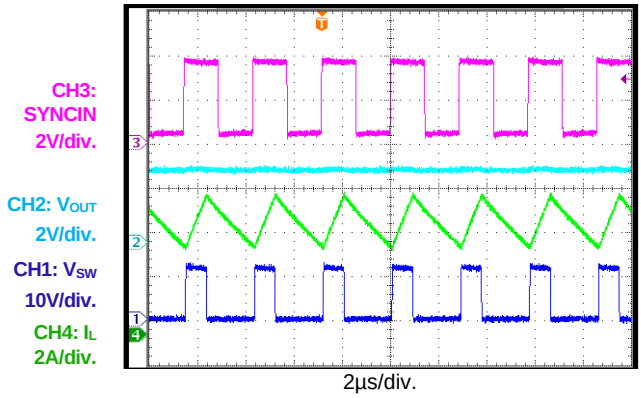
Load Transient

I_{OUT} = 3A to 6A, 1.6A/µs



SYNC Operation

I_{OUT} = 6A, SYNC frequency = 350kHz



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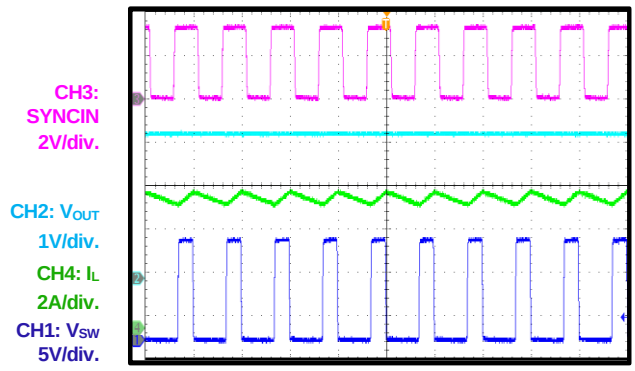
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

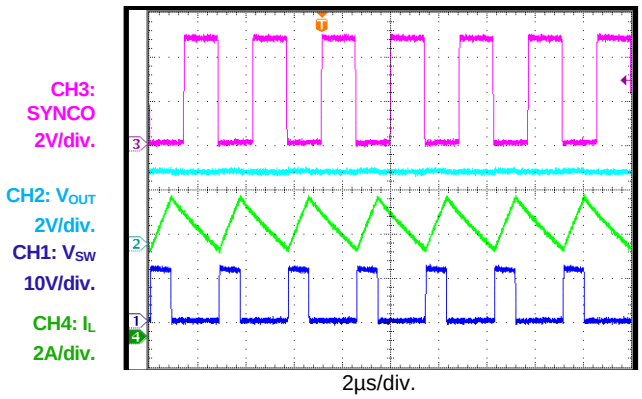
SYNC Operation

I_{OUT} = 6A, SYNC frequency = 1000kHz



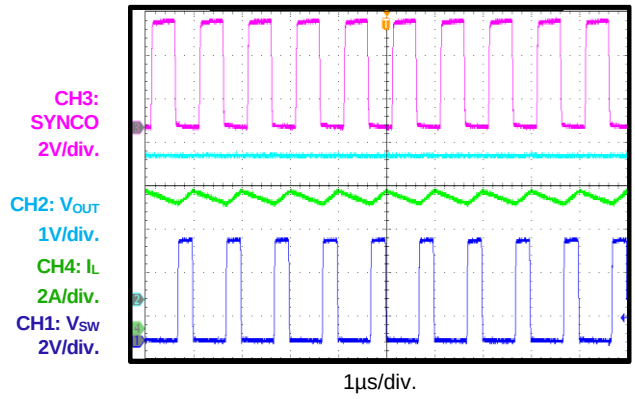
SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 350kHz



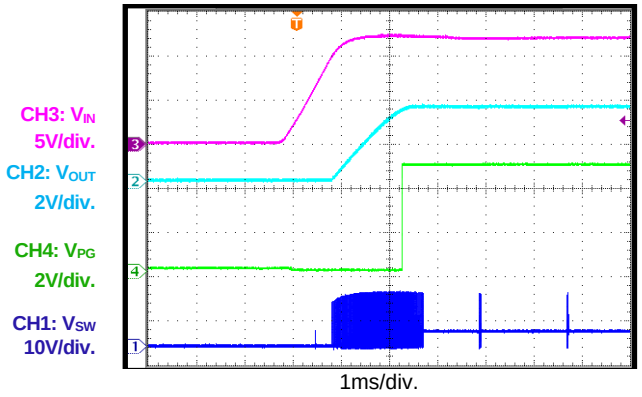
SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 1000kHz



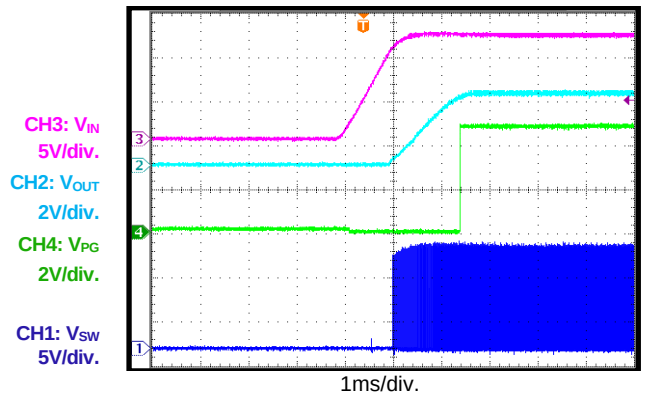
PG in Start-Up through VIN

I_{OUT} = 0A



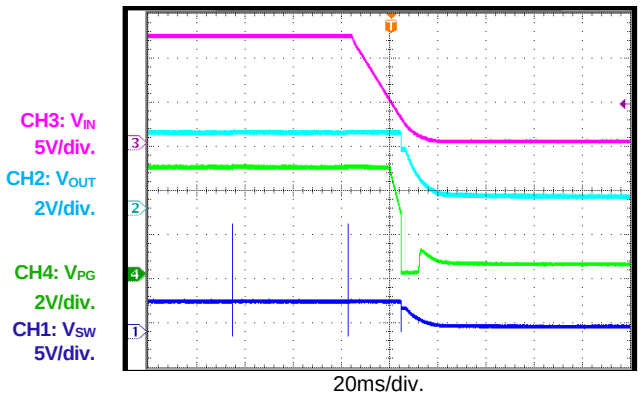
PG in Start-Up through VIN

I_{OUT} = 6A



PG in Shutdown through VIN

I_{OUT} = 0A



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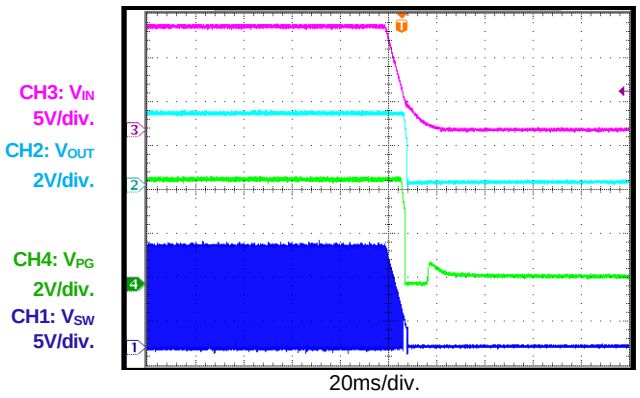
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

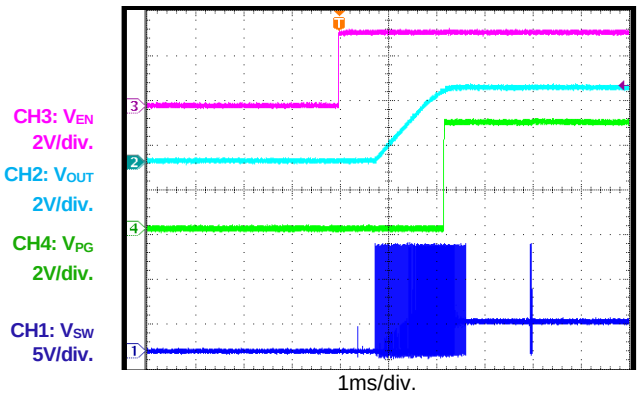
PG in Shutdown through VIN

I_{OUT} = 6A



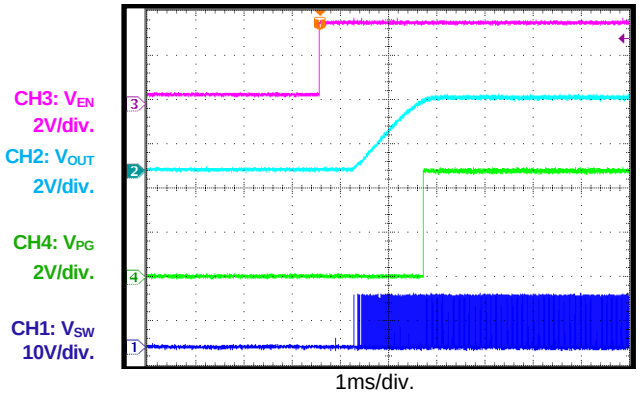
PG in Start-Up through EN

I_{OUT} = 0A



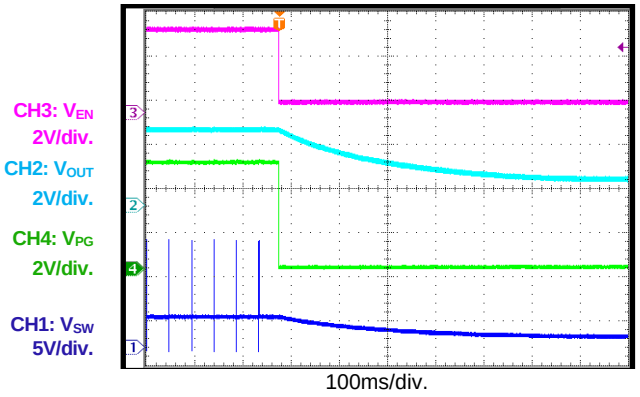
PG in Start-Up through EN

I_{OUT} = 6A



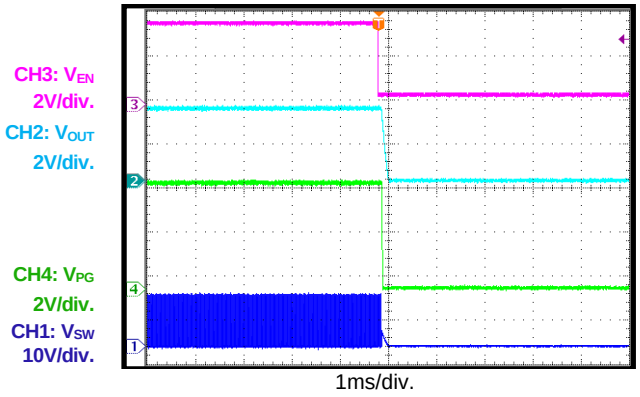
PG in Shutdown through EN

I_{OUT} = 0A



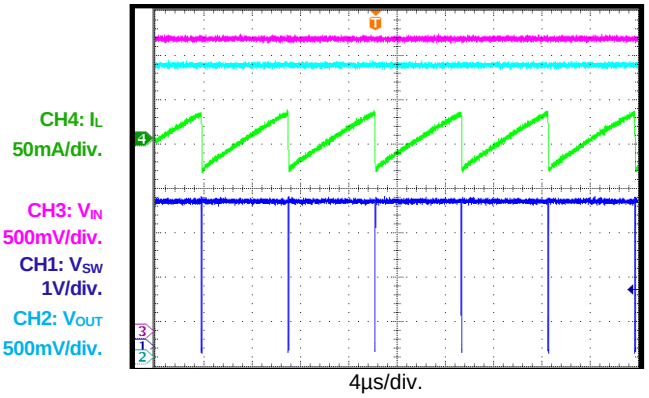
PG in Shutdown through EN

I_{OUT} = 6A



Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



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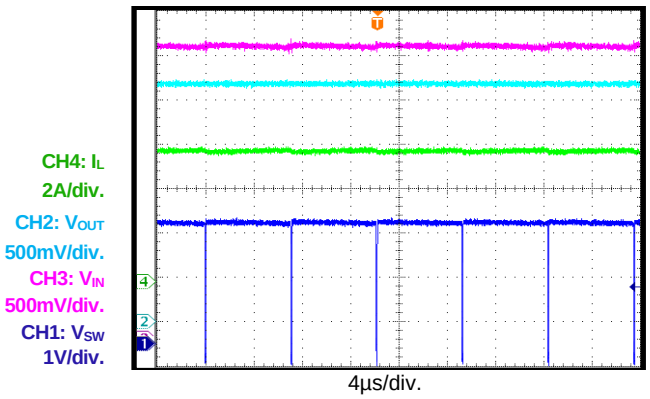
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

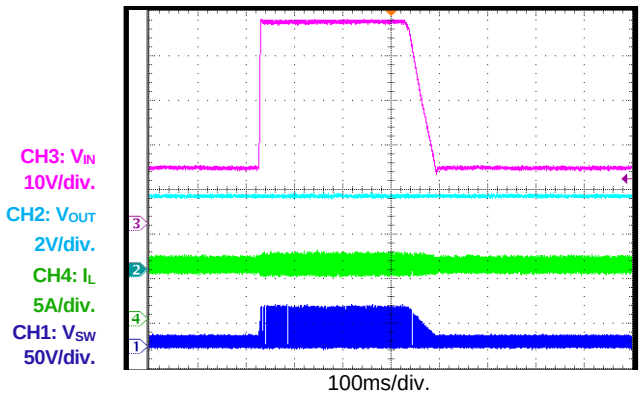
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 6A



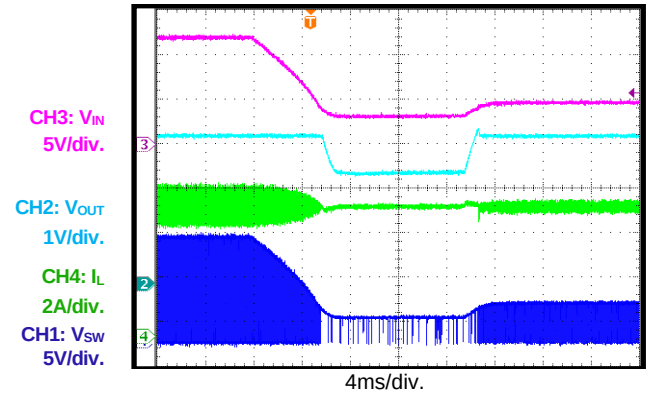
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 6A



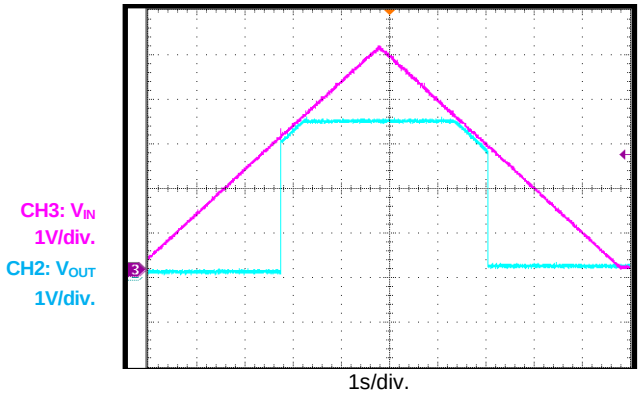
Cold-Crank Condition

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 6A



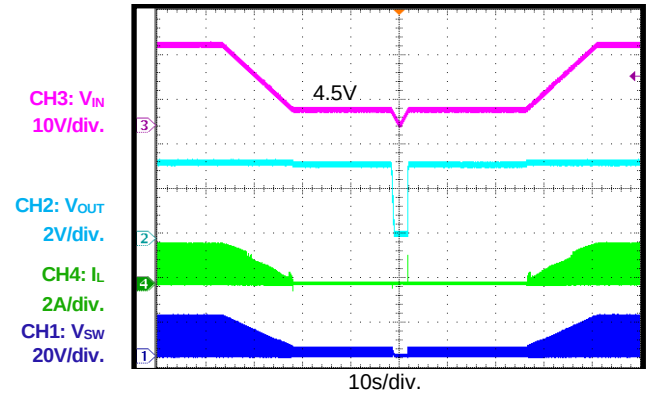
VIN Ramping Up and Down

I_{OUT} = 0.1A



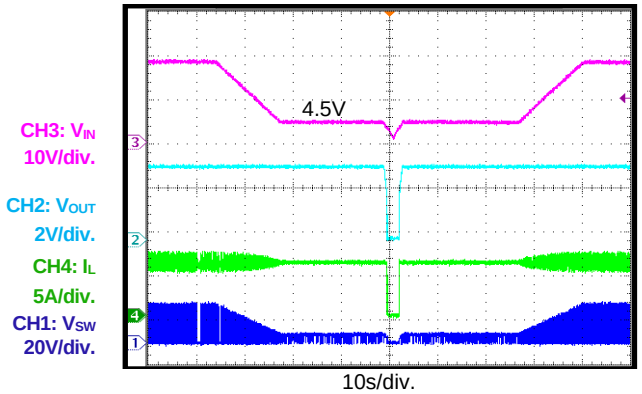
VIN Ramping Down and Up

I_{OUT} = 1mA



VIN Ramping Down and Up

I_{OUT} = 6A



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FUNCTIONAL BLOCK DIAGRAM

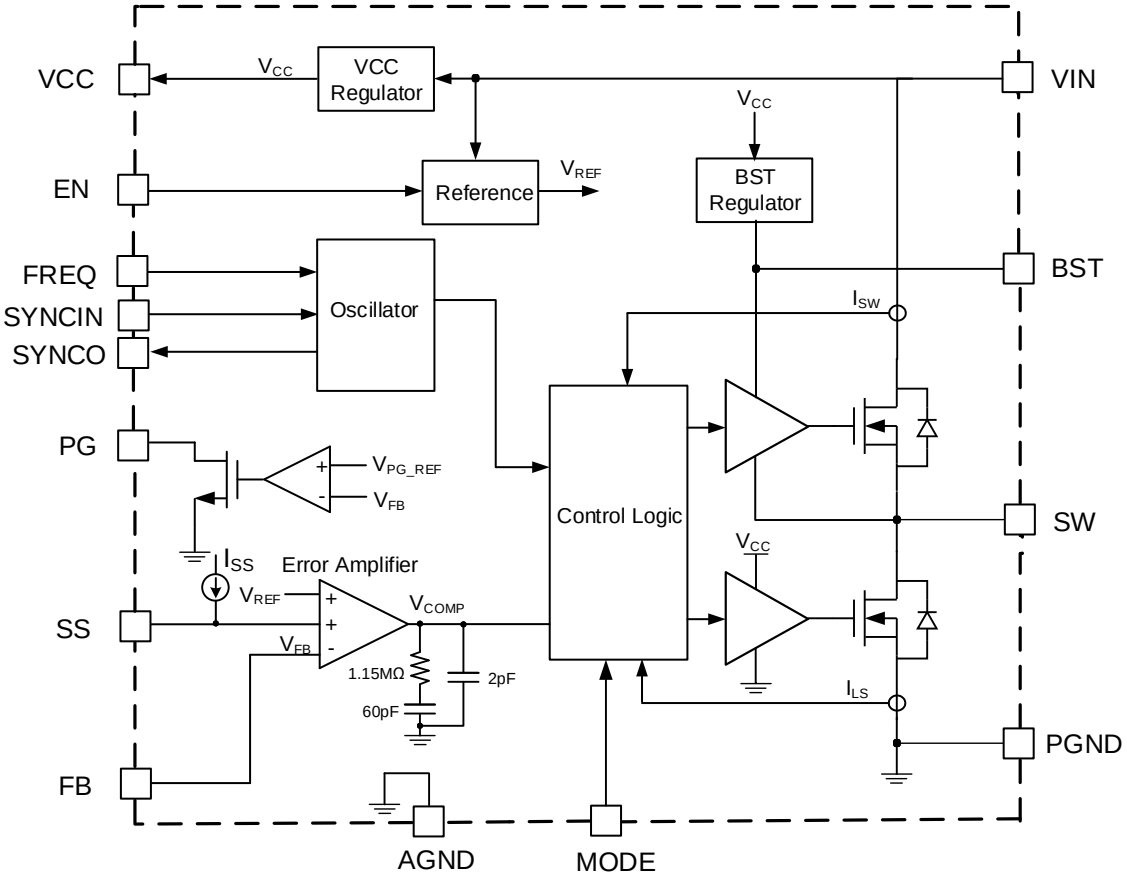

Figure 1: Functional Block Diagram

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TIMING SEQUENCE

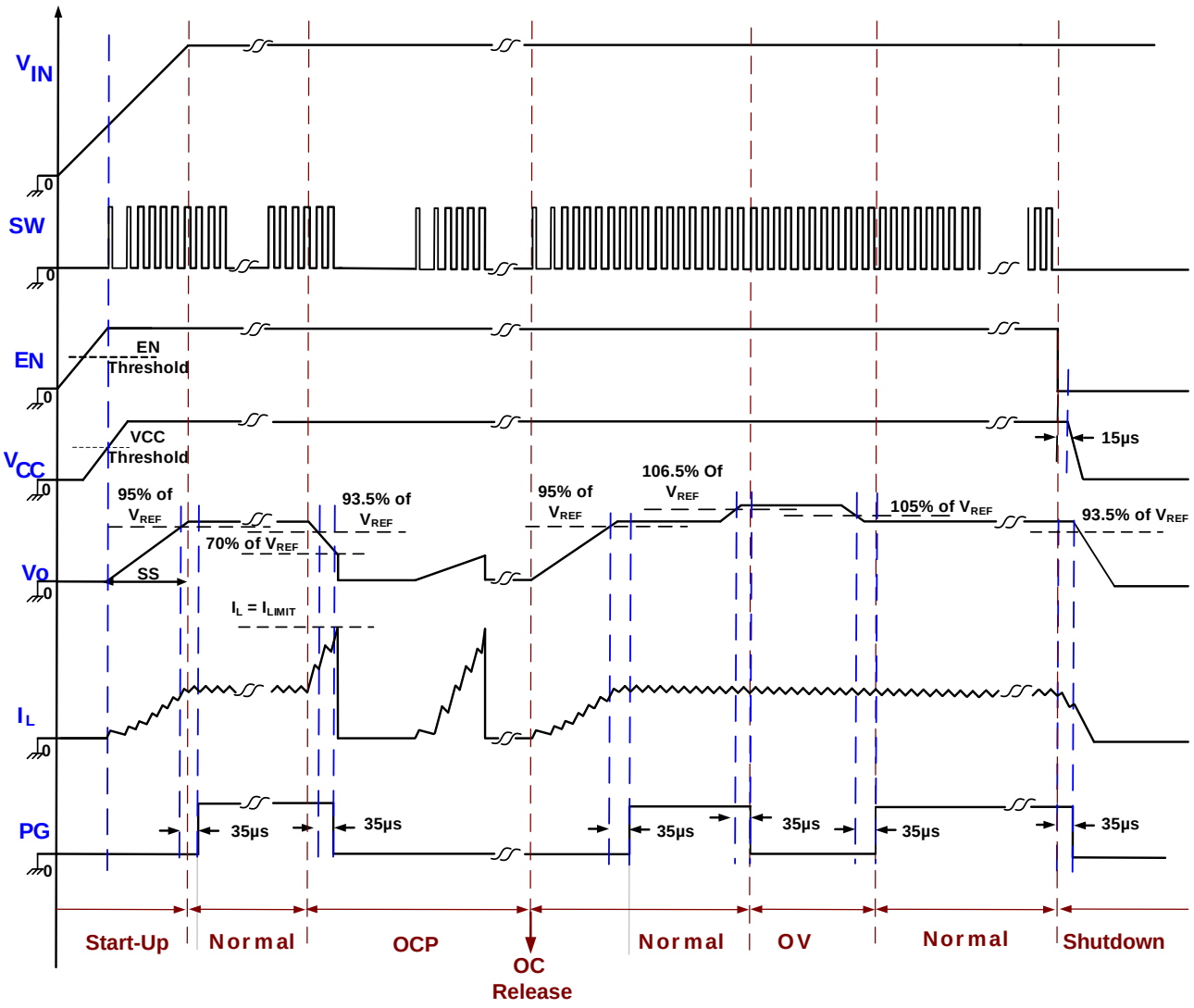

Figure 2: Timing Sequence

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OPERATION

The MP4316A is a synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs. The device provides 6A of highly efficient output current (I_{OUT}) with current mode control.

The MP4316A features a wide input voltage (V_{IN}) range, configurable switching frequency (f_{SW}), external soft start, and a precise current limit. The device's low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

PWM Control

At moderate to high output currents, the MP4316A operates with fixed-frequency, peak current control to regulate the output voltage (V_{OUT}). A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) turns on. The HS-FET stays on until its current reaches the value set by the internal COMP voltage (V_{COMP}). The HS-FET stays on for at least 100ns.

When the HS-FET is off, the low-side MOSFET (LS-FET) immediately turns on, and stays on until the next cycle starts. The LS-FET remains on for at least 80ns before the next cycle starts.

If the current in the HS-FET does not reach the value set by COMP within one PWM period, the HS-FET remains on, which saves a turn-off operation. The HS-FET is forced off if it stays on for about 10µs, even if it does not reach the value set by COMP.

Light-Load Operation

Under light-load conditions, the MP4316A can work in two different operation modes based on the MODE pin.

The MP4316A works in forced continuous conduction mode (FCCM) when the MODE pin is pulled above 1.8V. In FCCM, the device works with a fixed frequency from no-load to full-load conditions. The advantages of FCCM are its controllable frequency and lower output ripple under light loads.

The MP4316A works in advanced asynchronous modulation (AAM) mode when the MODE pin is pulled below 0.4V. AAM mode optimizes efficiency under light-load and no-load conditions.

When AAM is enabled, the MP4316A enters asynchronous operation while the inductor current approaches 0A under light loads (see Figure 3). If the load is further decreased or there is no load, the internal COMP voltage (V_{COMP}) drops to the set value, and the MP4316A enters AAM mode.

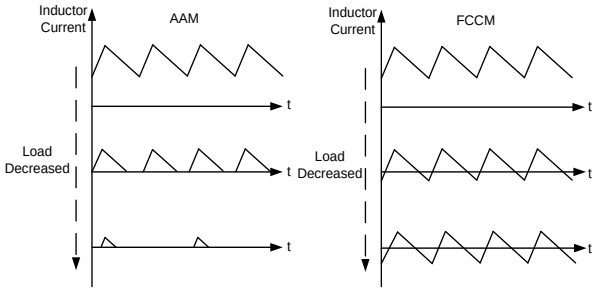

Figure 3: AAM Mode and FCCM

In AAM mode, the internal clock resets when V_{COMP} crosses the set value. The crossover time is used as a benchmark for the next clock. When the load increases and V_{COMP} exceeds the set value, the device operates in discontinuous conduction mode (DCM) or CCM, which have a constant switching frequency (f_{SW}).

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin voltage (V_{FB}) to the internal reference voltage (0.815V), and outputs a current that is proportional to the difference between the voltages. This output current charges the compensation network to form V_{COMP}, which controls the power MOSFET current.

During normal operation, the minimum V_{COMP} is clamped to 0.9V, and its maximum is clamped to 2.0V. COMP is internally pulled down to GND when the device shuts down.

Internal Regulator (VCC)

The internal 4.9V regulator (VCC) powers most of the internal circuitry. This regulator uses VIN as the input and operates across the full V_{IN} range. When V_{IN} exceeds 4.9V, VCC is in full regulation. When V_{IN} is below 4.9V, the VCC output degrades.

Bootstrap Charging

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between

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the BST and SW nodes drops below its regulated value, a N-channel MOSFET pass transistor connected from VCC to BST turns on to charge the bootstrap capacitor. The external circuit should provide enough voltage headroom to facilitate the charging. When the HS-FET is on, BST exceeds VCC, which means that the bootstrap capacitor cannot be charged.

Under higher duty cycles, there is less time for the bootstrap capacitor to charge, so the bootstrap capacitor may not be charged sufficiently. If the external circuit has an insufficient voltage (or not enough time) to charge the bootstrap capacitor, use additional external circuitry to ensure that the bootstrap voltage stays in the normal operation region.

Low-Dropout Operation and Refreshing BST

To improve dropout, the MP4316A is designed to operate at close to 100% duty cycle when the difference between the voltages on the BST and SW pins exceeds 2.5V. When the voltage from BST to SW drops below 2.5V, the high side MOSFET turns off using an under-voltage lockout (UVLO) circuit. This allows the LS-FET to conduct and refresh the charge on the BST capacitor. In DCM or pulse-skip mode (PSM), the LS-FET is forced on to refresh the BST voltage.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. As a result, the effective duty cycle of the switching regulator is high.

The regulator's effective duty cycle during dropout is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off.

Enabled by an External Logic (High/Low) Signa*l*

When EN is pulled below its falling threshold voltage (about 0.85V), the chip operates in the lowest shutdown current mode. Force EN above its rising threshold voltage (about 1V) to turn the part on.

Configurable V_{IN} Under-Voltage Lockout (UVLO)

When V_{IN} is sufficiently high, the chip can be enabled and disabled via the EN pin. With an internal current source, the circuit can generate a configurable V_{IN} UVLO threshold and hysteresis. Use resistor dividers to set the EN voltage (see Figure 4).

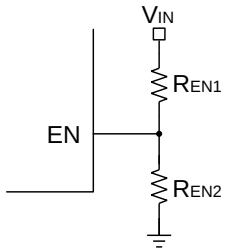

Figure 4: Enable Divider Circuit

Configurable Frequency and Foldback

The MP4316A's oscillating frequency can be configured via an external resistor (R_{FREQ}) connected from the FREQ pin to ground, or by a logic level SYNC signal.

To set f_{SW}, select R_{FREQ} using the f_{SW} vs. R_{FREQ} curve on page 15. Note that when f_{SW} is set high, it may fold back at high input voltages to avoid triggering a minimum on time and forcing the output out of regulation.

The f_{SW} for car battery applications is between 350kHz and 1000kHz. Table 1 lists the recommended R_{FREQ} values for common frequencies. Higher frequencies can be used in applications that do not have a critical f_{SW} limit, as well as applications with a low and stable V_{IN}.

Table 1: R_{FREQ} vs. f_{SW}

R_{FREQ} (kΩ)	f_{SW} (kHz)
86.6	350
80.6	380
75	410
62	470
59	500
54.9	530
49.9	590
45.3	640
41.2	700
37.4	760
34	830
30.9	910
28.7	960
26.1	1000

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Frequency Spread Spectrum (FSS)

The MP4316A uses a 12kHz modulation frequency with a fixed 128-step triangular profile to spread the internal oscillator frequency across a 20% (±10%) window (see Figure 5). The steps are fixed and independent of the set oscillator frequency, which optimizes the frequency spread spectrum (FSS) performance.

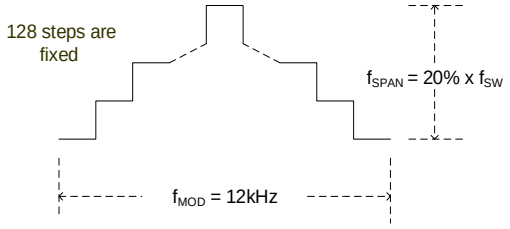

Figure 5: Spread Spectrum Scheme

Side bands are created by modulating f_{SW} with the triangle modulation waveform. This reduces the emission power of the fundamental f_{SW}, as well as its harmonics, which then reduces peak EMI noise.

Soft Start

Soft start is implemented to prevent the converter's V_{OUT} from overshooting during start-up.

When soft start begins, an internal current source begins charging the external soft-start capacitor. When the soft-start voltage (V_{SS}) is below the internal reference voltage (V_{REF}), V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 13.5 \times t_{SS}(ms) \quad (1)$$

The SS pin can be used for tracking and sequencing.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} - 150mV during start-up, this means that the output has a pre-biased voltage. In the scenario, the HS-FET and LS-FET do not turn on until V_{SS} rises above V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to protect the chip from thermal runaway. If the silicon die temperature rises above its upper threshold, the device shuts down the power MOSFETs. When the temperature falls below the lower threshold, the chip is re-enabled.

Current Comparator and Current Limit

The power MOSFET's current is accurately sensed via a current-sense MOSFET. Then this current is fed to the high speed current comparator for current mode control. The current comparator uses this sensed current as one of its inputs.

When the HS-FET turns on, the comparator is blanked until the end of the turn-on transition to mitigate noise. The comparator compares the power switch's current to the value set by the COMP voltage. When the sensed current exceeds the value set by COMP, the comparator outputs low to turn off the HS-FET. The maximum current of the internal power MOSFET is internally limited cycle by cycle.

Hiccup Protection

If the output is shorted to ground, V_{OUT} may drop below 70% of its nominal output. If this occurs, the MP4316A shuts down momentarily and begins discharging the soft-start capacitor. The device restarts with a full soft start when the soft-start capacitor is fully discharged. This process is repeated until the fault is removed.

Start-Up and Shutdown

If both V_{IN} and EN exceed their appropriate thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank the start-up glitches. When the soft-start block is enabled, the SS output stays low to ensure that the remaining circuitries are ready before slowly ramping up.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. When shutdown is initiated, the signaling path is first blocked to avoid any fault triggering. Next, the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

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Power Good (PG) Output

The MP4316A includes an open-drain power good (PG) output. If using the PG pin, connect it to a power source using a pull-up resistor. PG goes high if V_{OUT} is within 95% to 105% of the nominal voltage. PG goes low if V_{OUT} is above 106.5% or below 93.5% of its nominal voltage.

SYNCIN and SYNCO

f_{SW} can be synchronized to the rising edge of the clock signal applied at SYNCIN. The recommended SYNCIN frequency range is between 350kHz and 1000kHz. Ensure that SYNCIN's off time is shorter than the internal oscillator period. Otherwise, the internal clock may turn on the HS-FET before the rising edge of SYNCIN.

There is no limit for the SYNCIN pulse width, but there is always parasitic capacitance on the pad. If the pulse width is too short, a clear rising and falling edge may not be achieved due to the parasitic capacitance. It is recommended to make the pulse longer than 100ns.

When using SYNCIN in AAM mode, drive SYNCIN below its specified threshold (about 0.4V), or float the SYNCIN pin before starting up the MP4316A. Then add the external SYNCIN clock. Connect a resistor from SYNCIN to GND to avoid floating SYNCIN when using this function. It recommended to use a 10kΩ to 51kΩ resistor.

The SYNCO pin provides a default 180° phase-shifted clock for the internal oscillator. If there is no external SYNCIN clock, SYNCO can provide a 180° phase-shift clock that is compared to the internal clock.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 6).

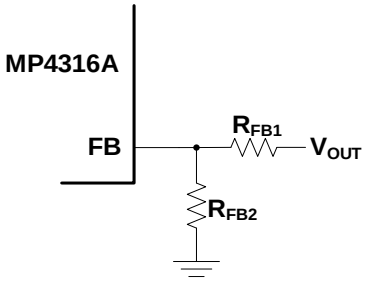

Figure 6: Feedback Network

Calculate R_{FB2} with Equation (2):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.815V} - 1} \quad (2)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection for Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	100 (1%)	32.4 (1%)
5	100 (1%)	19.6 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the device as possible.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be calculated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (6)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

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For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP4316A can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance can be estimated with Equation (9):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (10):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

V_{IN} Under-Voltage Lockout (UVLO) Setting

The MP4316A has an internal fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3V, while the falling threshold is about 2.7V. For applications that require a higher UVLO point, place an external resistor divider between VIN and EN to raise the equivalent UVLO threshold (see Figure 7).

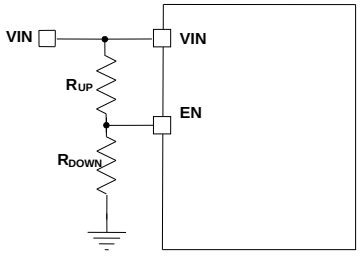

Figure 7: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (11) and Equation (12), respectively:

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN_RISING} \quad (11)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN_FALLING} \quad (12)$$

Where V_{EN_RISING} is 1V, and $V_{EN_FALLING}$ is 0.85V.

Selecting the External BST Diode and Resistor

An external BST diode can enhance the regulator's efficiency when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external bootstrap diode. It is recommended to make V_{CC} or V_{OUT} the power supply in the circuit (see Figure 8).

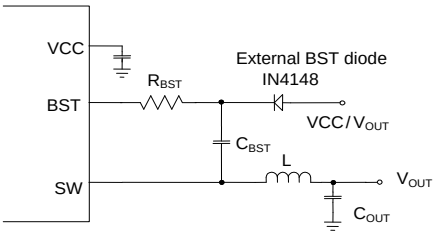

Figure 8: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is between 0.1µF and 1µF. Connect a resistor (R_{BST}) in series with the BST capacitor to reduce the SW rising rate and voltage spikes. This enhances EMI performance and reduces voltage stress at higher input voltages. A higher resistance reduces SW spikes but compromises efficiency. It is recommended for R_{BST} to be ≤20Ω.

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Selecting the VCC Capacitor

The VCC capacitor should have a capacitance that is 10 times larger than the boost capacitor's capacitance. It is not recommended for the VCC capacitor to exceed 68µF.

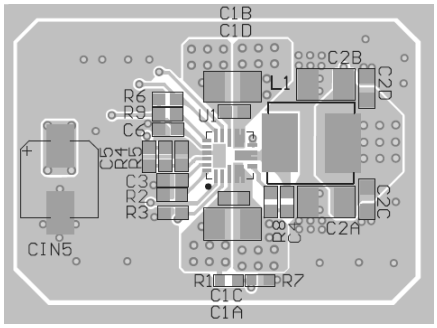
PCB Layout Guidelines (12)

Efficient PCB layout, especially for the input capacitor placement, is critical for stable operation. A four-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 9 and follow the guidelines below:

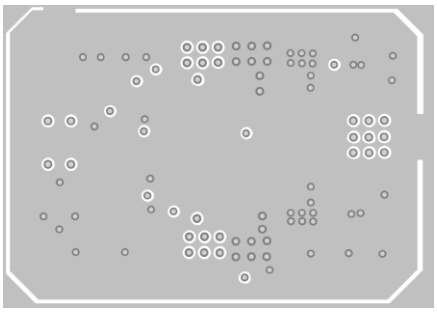
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Connect a large copper plane directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure that the trace connecting to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

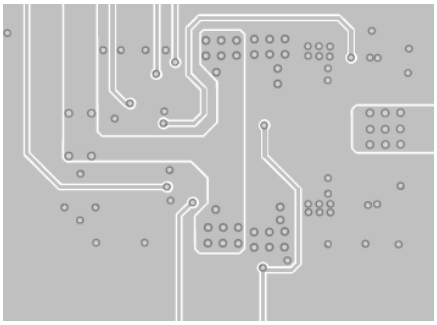
12) The recommended PCB layout is based on Figure 10 on page 34.



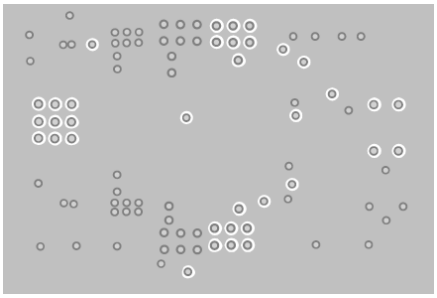
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 9: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

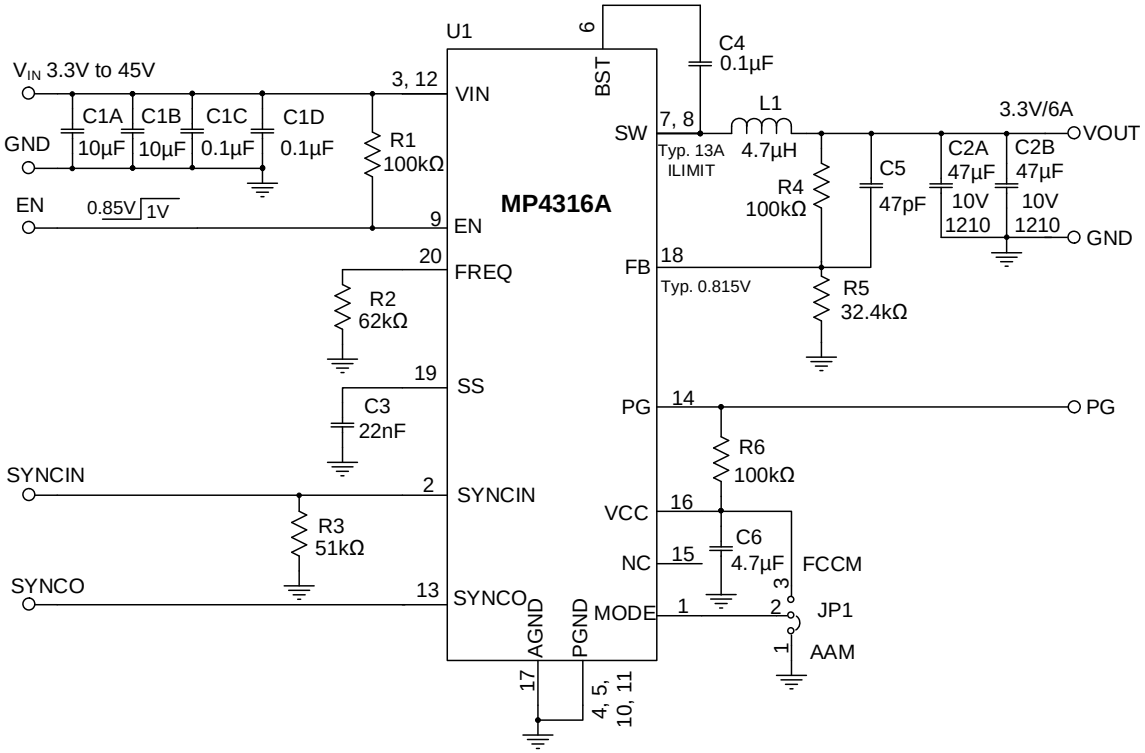

Figure 10: V_{OUT} = 3.3V, f_{SW} = 470kHz

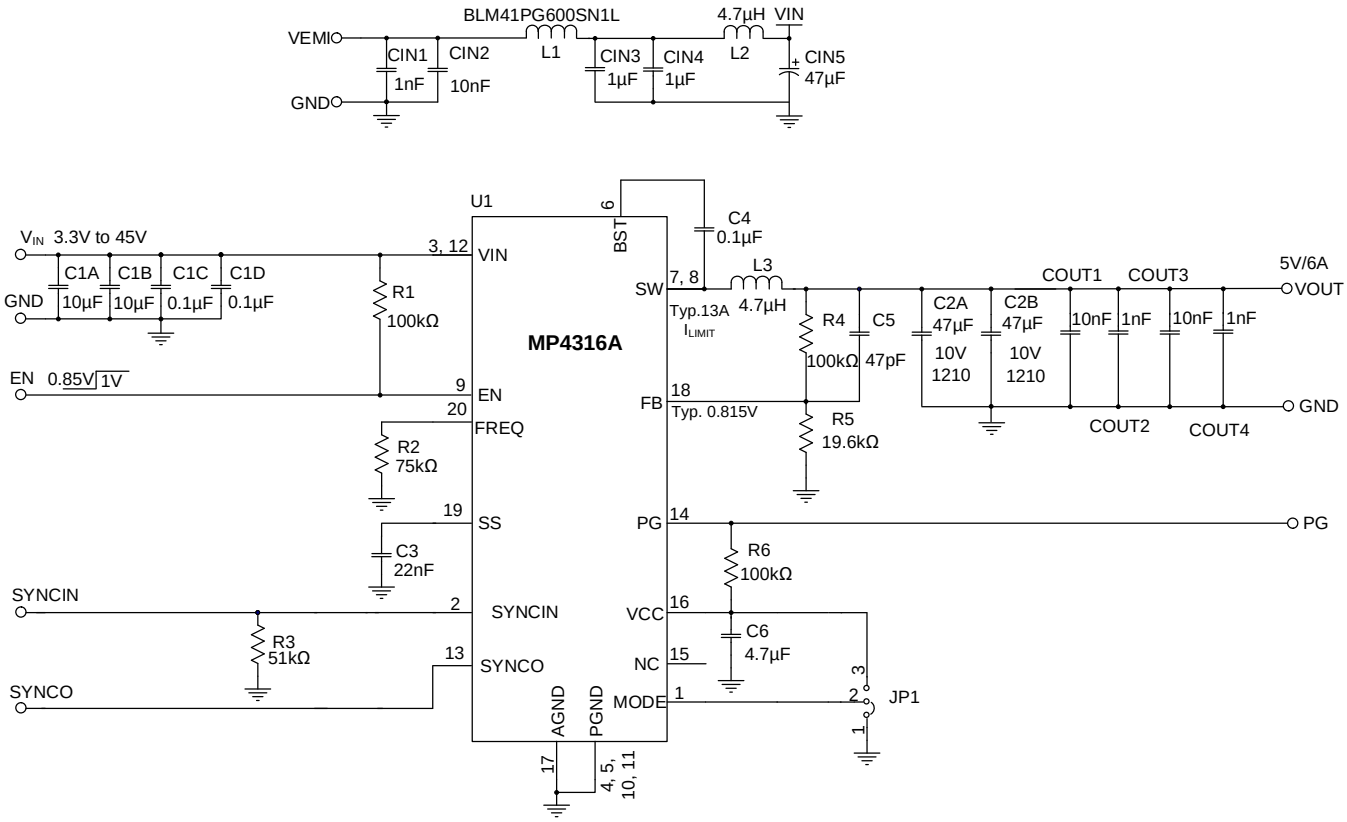

Figure 11: V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filters

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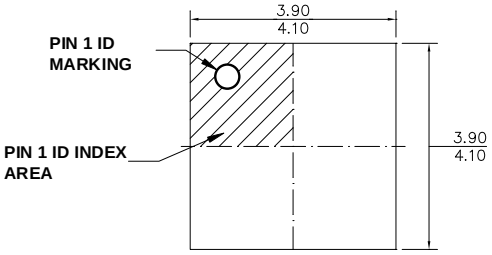
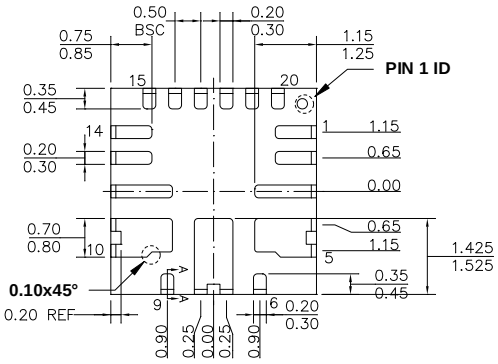
PACKAGE INFORMATION

QFN-20 (4mmx4mm)
Wettable Flank

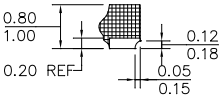


TOP VIEW

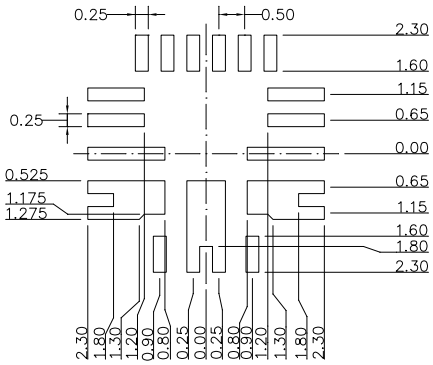


BOTTOM VIEW

SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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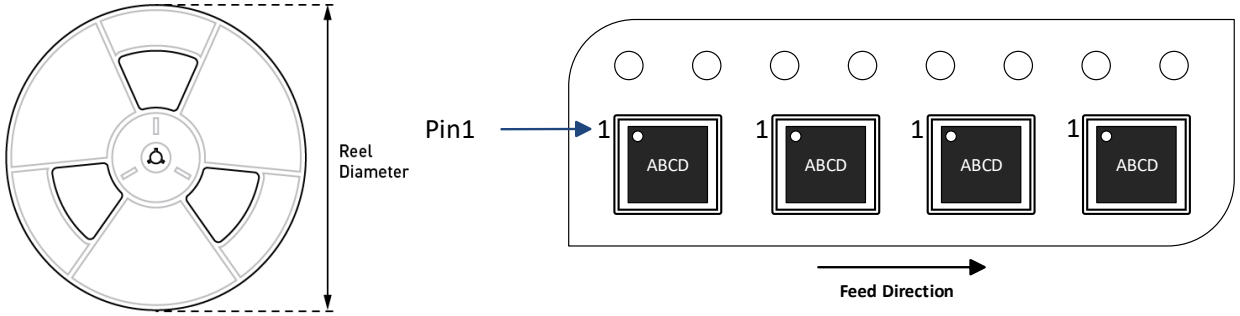
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (13)	Quantiy/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4316AGRE-Z	QFN-20 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

13) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, contact the factory. (The order code for a 500-piece partial reel order is “-P”. Tape & reel dimensions are the same as the full reel.)

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/29/2022	Initial Release	-

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