MP4247

36V, 100W, Buck-Boost Converter with Integrated Low-Side MOSFETs and I²C Interface

DESCRIPTION

The MP4247 is a buck-boost converter with two integrated low-side power switches. The device can deliver up to 100W of peak output power at certain input supplies with excellent efficiency.

The MP4247 is well-suited for USB power delivery (USB PD) applications. The device can work with an external USB PD controller via the I²C interface. The I²C interface and one-time programmable (OTP) memory provide flexible and configurable parameters.

Fault condition protection includes constant current (CC) current limiting, output over-voltage protection (OVP), and thermal shutdown (TSD).

The MP4247 requires a minimal number of readily available, standard external components, and is available in a QFN-20 (3mmx5mm) package.

FEATURES

- UL and IEC62368-1 Certified, Efile #322138
- 100W Buck-Boost Converter with Integrated Low-Side MOSFETs (LS-FETs)
- Integrated Gate Driver for High-Side Power MOSFETs (HS-FETs)
- 3.6V to 36V Start-Up Input Voltage (V_{IN}) Range
- Supports 2.8V Falling V_{IN} when the Output Voltage (V_{OUT}) > 3.5V
- 1V to 24V [(1)] V_{OUT} Range with 1% Accuracy
- Up to 5A Output Current (I_{OUT})
- Up to 98% Peak Efficiency
- Configurable Reference Voltage (V_{REF}) Range (0.1V to 2.147V) with 1mV Resolution via I²C Interface
- Accurate Output CC Current Limit: ±5%
- Meets USB PD 3.0 with PPS Specifications
- Selectable 280kHz, 420kHz, or 600kHz Switching Frequency (f_{SW})
- Selectable Forced PWM or Auto-PFM/PWM
- Output Biased VCC LDO for Higher Efficiency
- Output Current Monitor (IMON) Function
- Line Drop Compensation via R_{SENS}
- I²C, Alert, and One-Time Programmable (OTP) Memory
- EN Shutdown Passive Discharge
- Output OCP, OVP, and Thermal Shutdown
- Available in a QFN-20 (3mmx5mm) Package

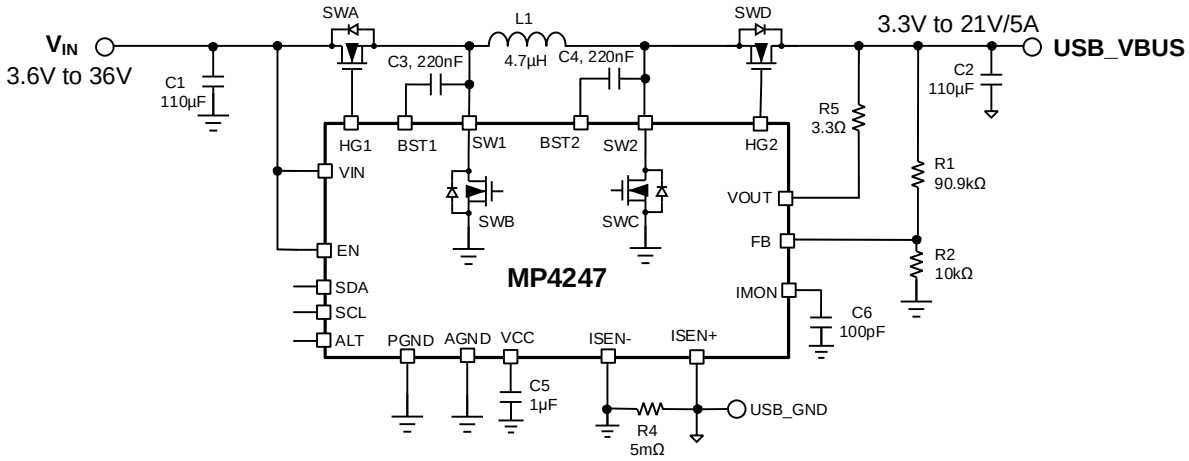
APPLICATIONS

- USB Type-C and USB Power Delivery
- USB Type-C PD Monitors and Docking Stations
- USB Type-C Car Chargers
- Wireless Charging

Note:

1) The MP4247GQV-0012 can support output voltages up to 36V. Contact an MPS FAE for its suffix code datasheet in details.

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL
MP4247GQV-0000	QFN-20 (3mmx5mm)	*See Below*	1
MP4247GQV-0002			
MP4247GQV-0011			
MP4247GQV-xxxx**			

* For Tape & Reel, add suffix -Z (e.g. MP4247GQV-xxxx-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the MTP. Each “x” can be a hexadecimal value between 0 and F.

TOP MARKING

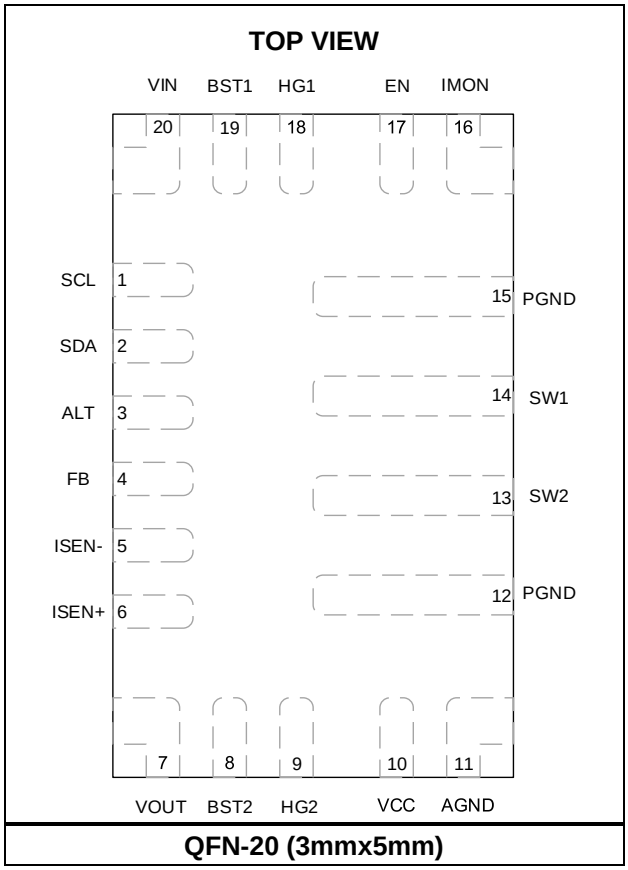
MPYW

4247

LLL

MP: MPS prefix
Y: Year code
W: Week code
4247: Part number
LLL: Lot number

PACKAGE REFERENCE



QFN-20 (3mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	SCL	**I²C clock signal input.**
2	SDA	**I²C data line.**
3	ALT	**I²C alert pin.** The ALT pin is an open-drain, active low output.
4	FB	**Feedback pin.** To set the output voltage (V_{OUT}), connect FB to the tap of an external resistor divider from the output to AGND.
5	ISEN-	**Negative node of current-sense signal input.** Place a current-sense resistor between PGND and the GND capacitor (C_{OUT}). Then connect the ISEN- pin to the PGND side of the capacitor.
6	ISEN+	**Negative node of current-sense signal input.** Place a current-sense resistor between PGND and the GND capacitor (C_{OUT}). Then connect the ISEN+ pin to the GND side of the capacitor.
7	VOUT	**Output voltage-sense input.** VOUT provides the VCC supply under certain V_{OUT} conditions.
8	BST2	**Bootstrap.** A 0.22µF capacitor should be kelvin connected to SW2 pin from BST2 to form a floating supply across the high-side switch driver.
9	HG2	**High-side 2 gate drive output for boost mode's high-side MOSFET (SWD).**
10	VCC	**Internal 5V LDO regulator output.** Decouple VCC with a 0.47 µF to 1µF capacitor. If the VCC is used to supply other controller, suggest the total VCC capacitor is <1.5µF.
11	AGND	**Analog ground.** Connect AGND to PGND. Connect AGND to the VCC capacitor's ground node.
12, 15	PGND	**Power ground.** PGND requires extra consideration during PCB layout. Connect PGND to GND with copper traces and vias.
13	SW2	**Switch 2 node for buck-boost mode.** Connect SW1 to SW2 using a power inductor. Use a wide PCB trace to make the inductor connection.
14	SW1	**Switch 1 node for buck-boost mode.** Connect SW1 to SW2 using a power inductor. Use a wide PCB trace to make the inductor connection.
16	IMON	**Current monitor output.** IMON indicates the signal between ISEN+ and ISEN-.
17	EN	**EN input.** Apply a high logic to EN to enable the chip.
18	HG1	**High-side 1 gate drive output for buck mode's high-side MOSFET (SWA).**
19	BST1	**Bootstrap.** Connect a 0.22µF capacitor between SW1 and BST1 to form a floating supply across the high-side MOSFET driver.
20	VIN	**Supply voltage for internal logic circuitry (but not for power MOSFETs).** Kelvin connect Vin pin to SWA MOSFET drain with wide PCB trace, and it can't be shared by other DC-DC.

ABSOLUTE MAXIMUM RATINGS (2)

Supply voltage (V_{IN}) .....-0.4V to +40V
V_{SW1}.....-0.3V (-8V for <10ns) to V_{IN} + 0.3V (+43V for <10ns)
V_{SW2}.....-0.3V (-8V for <10ns) to V_{OUT} + 0.3V (+43V for <10ns)
$V_{BST1/2}$, $V_{HG1/2}$ ..... $V_{SW1/2}$ + 6V
V_{OUT} .....-0.3V to +40V
V_{EN}.....-0.3V to +40V
V_{CC}..... -0.3V to +6V (7.5V for <500µs)
All other pins .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (3) (7)
QFN-20 (3mmx5mm)..... 6W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (4)

Human body model (HBM)
SW1, HG1, and BST1 …....……-2kV to +1.7kV
All other pins……..±2kV
Charged device model (CDM).....±750V

Recommended Operating Conditions (5)

Operating input voltage.....3.6V to 36V
Operating output voltage .....1V to 24V (6)
Output current..... 5A
Output power…….. 100W
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EVL4247-V- 00A (7)……20.7…2.4…°C/W
QFN-20 (3mmx5mm) (8)……..39.1…..2.5…°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
5) The device is not guaranteed to function outside of its operating conditions.
6) The MP4247GQV-0012 can support output voltages up to 36V. Contact an MPS FAE for details.
7) Measured on EVL4247-V-00A, 4-layer PCB, 64mmx64mm.
8) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{Q_STD}	V_{EN} = 0V		1	30	μA
Quiescent supply current	I_{Q1}	No switching, I²C set operation on, EN on, PFM mode, T_J = 25°C		775	1250	μA
	I_{Q2}	I²C set operation off, EN on, T_J = 25°C		130	250	μA
EN rising threshold	V_{EN_RISING}	EN to enable switching	-5%	1.22	+5%	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-down resistor	R_{EN}	EN = 2V		2		MΩ
Thermal shutdown (10)	T_{STD}			160		°C
Thermal hysteresis (10)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}		4.85	5.15	5.45	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		2	5	%
VCC power source change threshold	V_{CC_VTH}	V_{IN} = 12V, ramp V_{OUT} from 5V to 10V	6.4	6.8	7.5	V
V_{CC} under-voltage lockout (UVLO) rising threshold	$V_{CC\_UVLO\_R}$		3.15	3.35	3.55	V
V_{CC} UVLO threshold hysteresis	$V_{CC\_UVLO\_HYS}$			200		mV
V_{IN} UVLO falling threshold	V_{UVLO_VIN}		2.35	2.55	2.75	V
Buck-Boost Converter						
Switch B on resistance	$R_{DS\_ON\_B}$			20	40	mΩ
Switch C on resistance	$R_{DS\_ON\_C}$			14	30	mΩ
Feedback voltage	V_{FB1}		-3%	330	+3%	mV
	V_{FB2}		-2%	500	+2%	mV
	V_{FB3}		-1.5%	2	+1.5%	V
Output over-voltage protection (OVP) rising threshold	$VOUT_{OVP\_R}$		114%	120%	126%	V_{FB}
Output absolute OVP	$VOUT_{OVP\_ABS}$	OTP can program it to 36.2V	23.5	25.5	27.5	V
Output OVP falling threshold	$VOUT_{OVP\_F}$		105%	110%	115%	V_{FB}
Output absolute OVP hysteresis	$VOUT_{OVP\_ABS\_HYS}$			0.75		V
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 36V, T_J = -40°C to +125°C			80	
Hiccup off timer	t_{HICCUP}			40		ms
Switching frequency	f_{SW1}	T_J = 25°C	220	280	340	kHz
	f_{SW2}	T_J = 25°C	340	420	500	
	f_{SW3}	T_J = 25°C	480	580	680	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Frequency dithering span	f_{SRANGE}			±15		%
Soft-start time	t_{SS}	Output from 10% to 90%, V_{OUT} = 5V, constant slew rate for other V_{REF}		1		ms
Minimum on time (10)	$t_{ON\_MIN\_BT}$	Boost SWC		180		ns
Minimum off time (10)	t_{OFF_MIN}	Buck SWB		180		ns
ISENS OC thresholds	I_{OC1}	OC threshold = 1A, R_{SENS} = 5mΩ	4.25	5	5.75	mV
	I_{OC2}	OC threshold = 3.6A, R_{SENS} = 5mΩ	-5%	18	+5%	mV
Low-side B valley current limit	I_{LIMIT2}	Switch B, 0XD3, D[7:6] = 10b		13		A
Low-side C peak current limit	I_{LIMIT3}	Switch C, 0XD3, D[7:6] = 10b		15	20	A
Line drop compensation	V_{DROP}	I_{OUT} = 1A		100		mV
Output discharge resistor	R_{DISCHG}			75	150	Ω
Mode Transition Threshold						
Buck-boost mode to buck mode transition threshold (10)	V_{MODE_TH2}	V_{IN} / V_{OUT}		120		%
Buck-boost mode to boost mode transition hysteresis (10)	V_{MODE_HYS2}	V_{IN} / V_{OUT}		82		%
High-Side Gate Driver						
Gate source current capability (10)	I_{DR1H_SRC}	5.2V_{BST_SW}, 4.7nF load		0.8		A
	I_{DR2H_SRC}	5.2V_{BST_SW}, 4.7nF load		1.2		A
Gate source resistance	R_{DR1H_SRC}	5.2V_{BST_SW}		3	5	Ω
	R_{DR2H_SRC}	5.2V_{BST_SW}		2	3	Ω
Gate sink current capability (10)	I_{DR1H_SIN}	5.2V_{BST_SW}, 4.7nF load		1.8		A
	I_{DR2H_SIN}	5.2V_{BST_SW}, 4.7nF load		3.3		A
Gate sink resistance	R_{DR1H_SIN}			1	2	Ω
	R_{DR2H_SIN}			1	2	Ω
Dead time of two edges (10)	$t_{DHS1\_HS3\_RISE}$	Body-diode conduct current duration		12		ns
	$t_{DHS2\_HS4\_FALLING}$	Body-diode conduct current duration		20		ns
ALT pin leakage	I_{ALT_LKG}	V_{ALT} = 5V		0.1		μA
ALT pin pull low resistance	R_{ALT}				20	Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C [9], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specification[10]						
Input logic high	V_{IH}		1.25			V
Input logic low	V_{IL}				0.6	V
Output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400	1000	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0	60		ns
Set-up time for a repeated start command	t_{SU_STA}		160			ns
Hold time for a repeated start command	t_{HD_STA}		160			ns
Bus free time between a start and stop command	t_{BUF}		160			ns
Set-up time for a stop command	t_{SU_STO}		160			ns
SCL and SDA rise time	t_R		10		300	ns
SCL and SDA falling time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF
Power Good (PG) Indication						
PG lower rising threshold	$V_{PG\_R\_L}$	PG goes high	88.5%	93%	98.5%	V_{FB}
PG lower falling threshold	$V_{PG\_F\_L}$	PG goes low	77%	82.5%	88%	V_{FB}
PG upper rising threshold	$V_{PG\_R\_H}$	PG goes low	115%	120.5 %	126%	V_{FB}
PG upper falling threshold	$V_{PG\_F\_H}$	PG goes high	105%	110%	115%	V_{FB}
Current Monitor Function						
IMON V_{OUT} gain	G_{IMON1}	R_{SENS} = 5mΩ, 2.5mV to 27mV IMON sense voltage		68		V/V
IMON V_{OUT} gain	G_{IMON2}	R_{SENS} = 10mΩ, 5mV to 55mV IMON sense voltage	-8%	34	+8%	V/V

Notes:

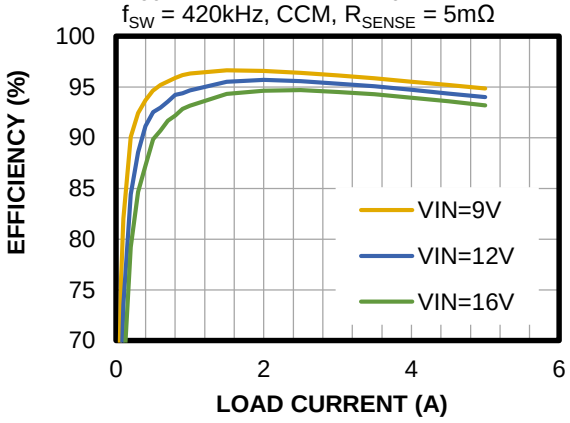
9) All minimum and maximum parameters are tested at T_J = 25°C. Over-temperature limits are guaranteed by characterization and correlation.
10) Guaranteed by characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

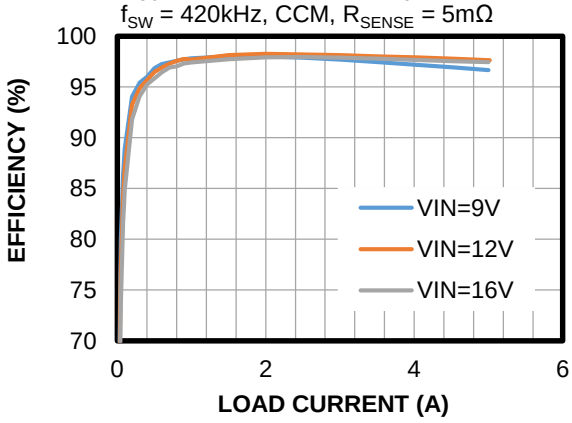
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



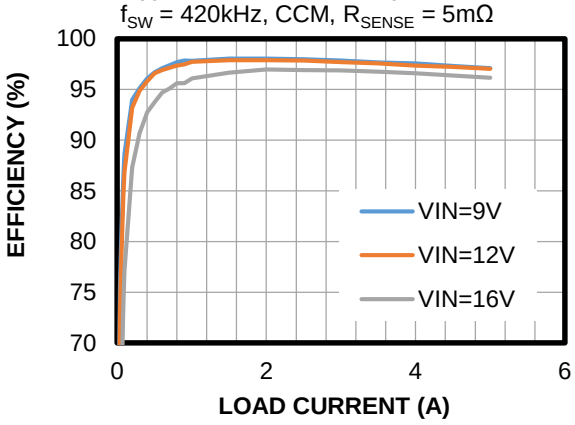
Efficiency vs. Load Current

V_{OUT} = 12V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



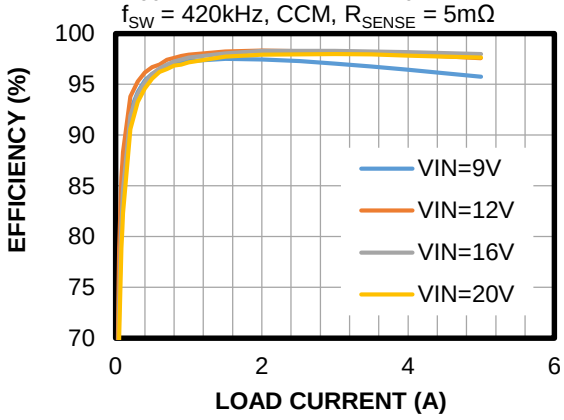
Efficiency vs. Load Current

V_{OUT} = 9V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



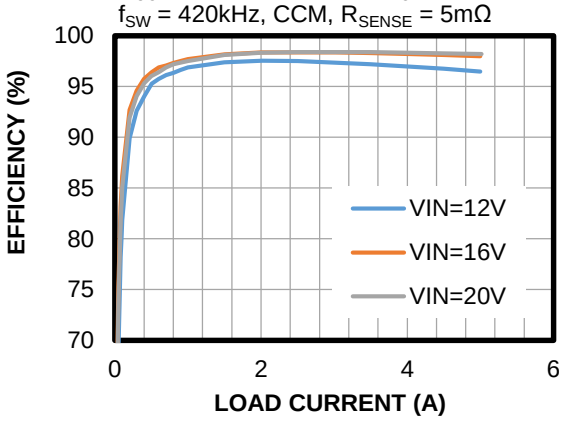
Efficiency vs. Load Current

V_{OUT} = 15V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



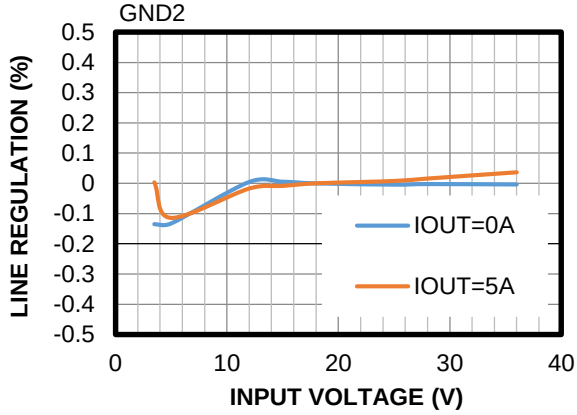
Efficiency vs. Load Current

V_{OUT} = 20V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



Line Regulation

V_{OUT} = 5V,measured between VOUT and GND2

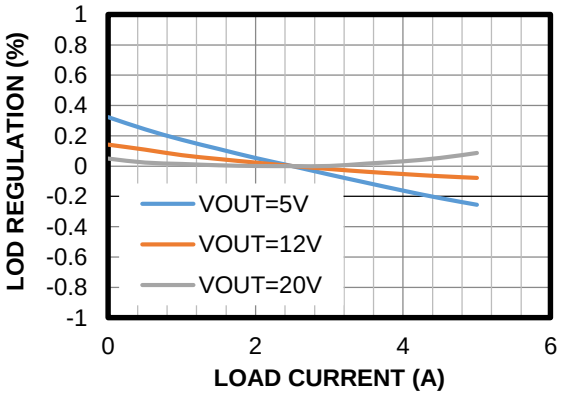


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

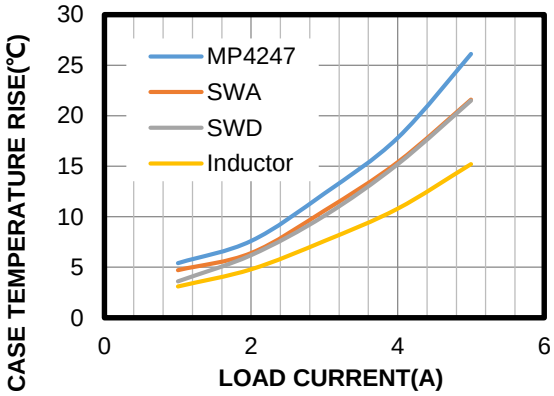
Load Regulation

R_{SENSE} = 5mΩ, no line drop compensation, measure V_{OUT} between VOUT and GND2



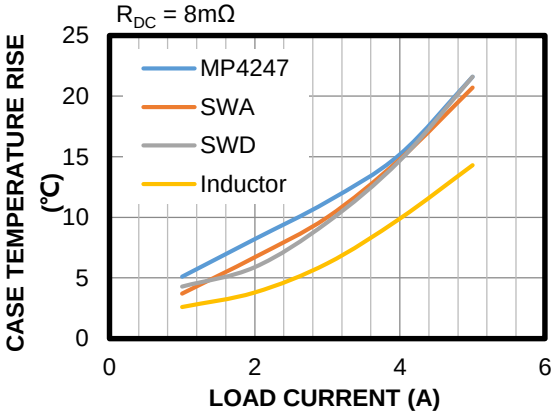
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ



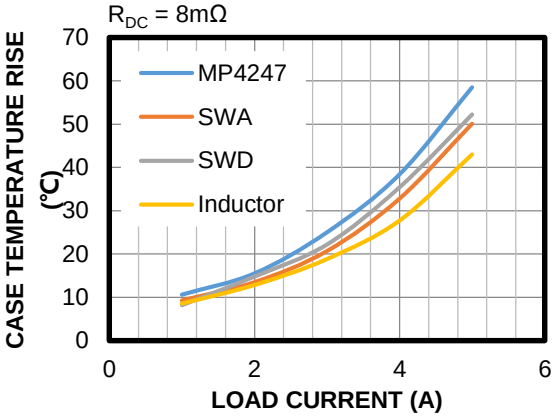
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 12V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ



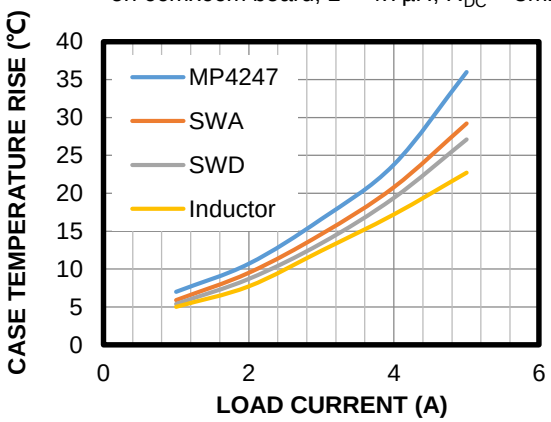
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 20V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ



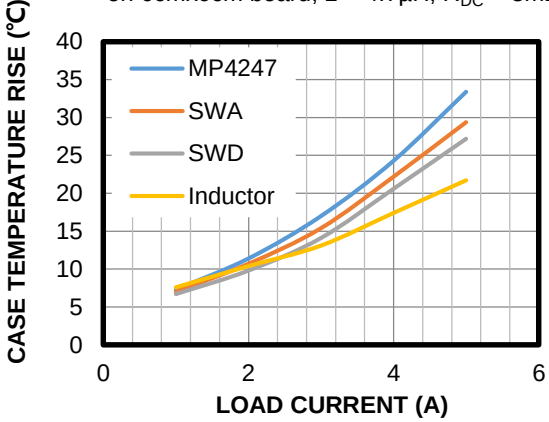
Case Temperature Rise

V_{IN} = 19V, V_{OUT} = 5V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ



Case Temperature Rise

V_{IN} = 19V, V_{OUT} = 9V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ

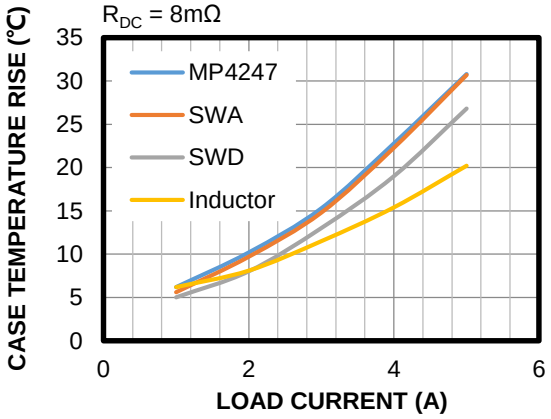


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

Case Temperature Rise

V_{IN} = 19V, V_{OUT} = 15V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ



Case Temperature Rise

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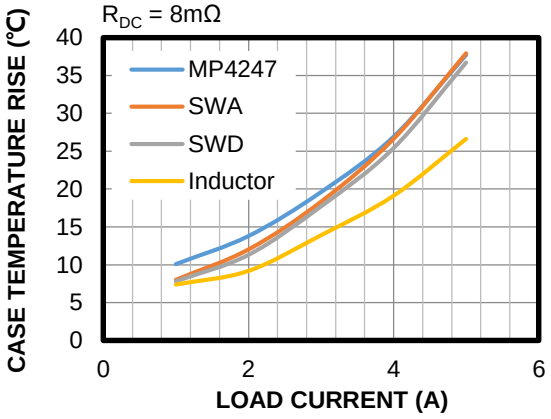
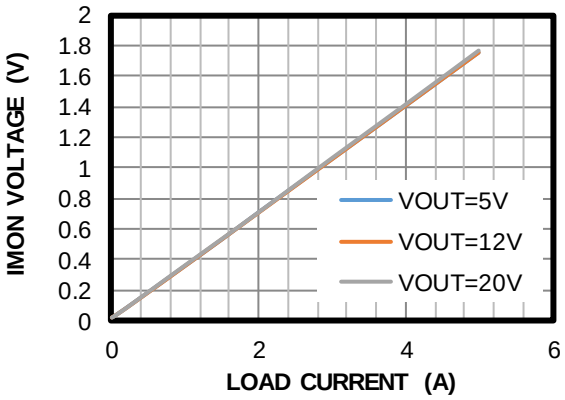
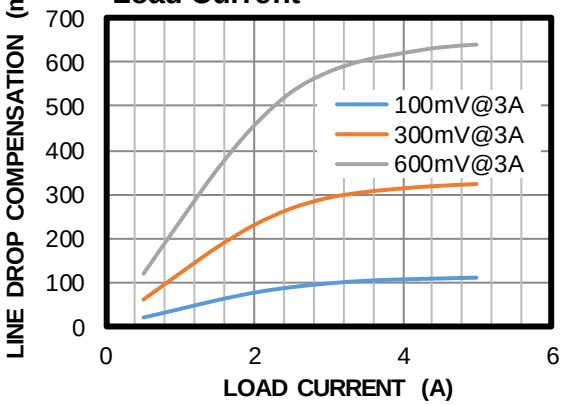


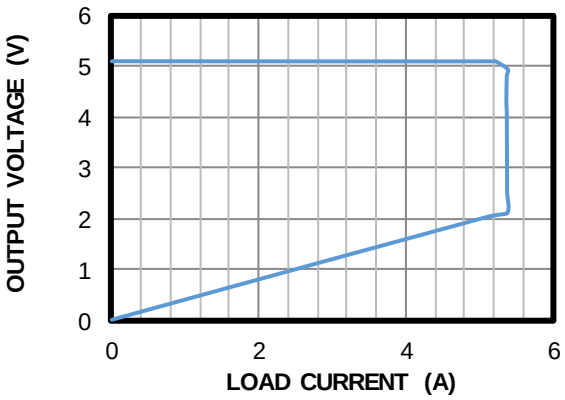
IMON Voltage vs. Load Current



Line Drop Compensation vs. Load Current

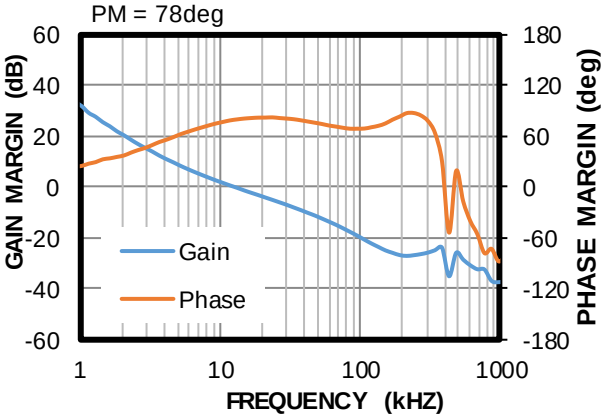


CC/CV Curve



Bode Plot

V_{OUT} = 5V, I_{OUT} = 5A, BW =12kHz, PM = 78deg

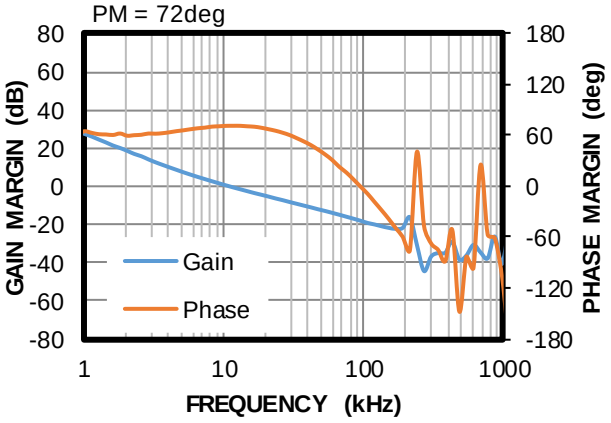


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

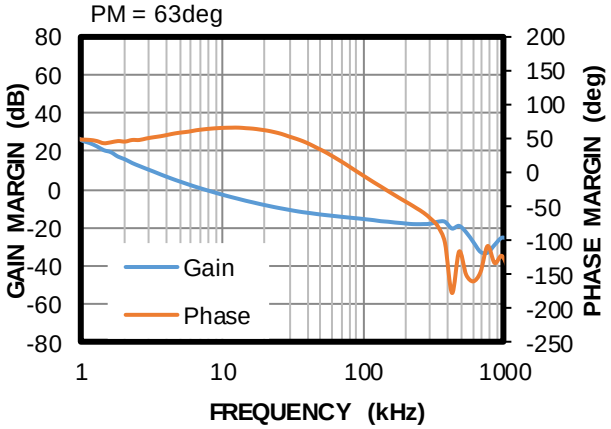
Bode Plot

V_{OUT} = 12V, I_{OUT} = 5A, BW =10kHz, PM = 72deg



Bode Plot

V_{OUT} = 20V, I_{OUT} = 5A, BW =7.5kHz, PM = 63deg

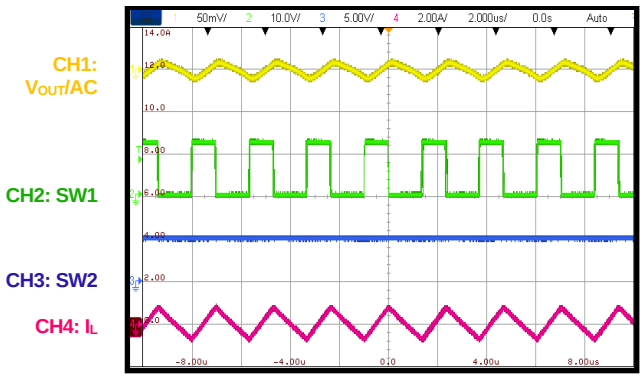


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

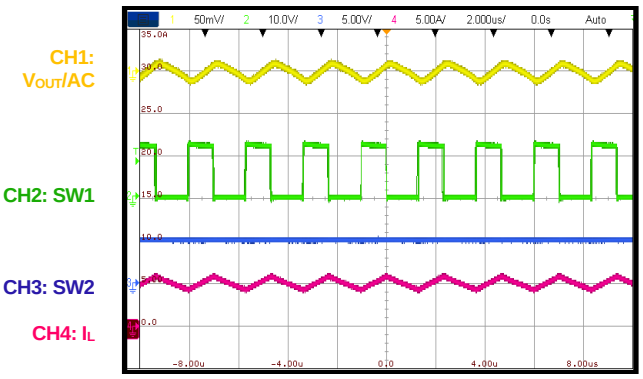
Output Voltage Ripple

V_{OUT} = 5V, load = 0A



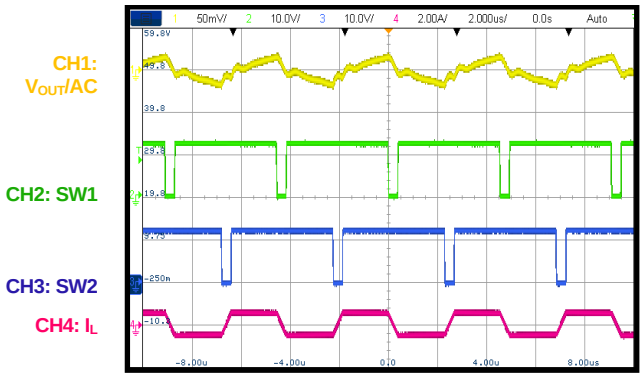
Output Voltage Ripple

V_{OUT} = 5V, load = 5A



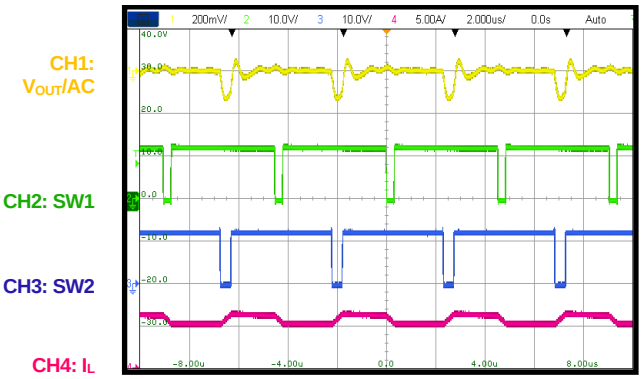
Output Voltage Ripple

V_{OUT} = 12V, load = 0A, f_{SW} drops by 50% in buck-boost mode



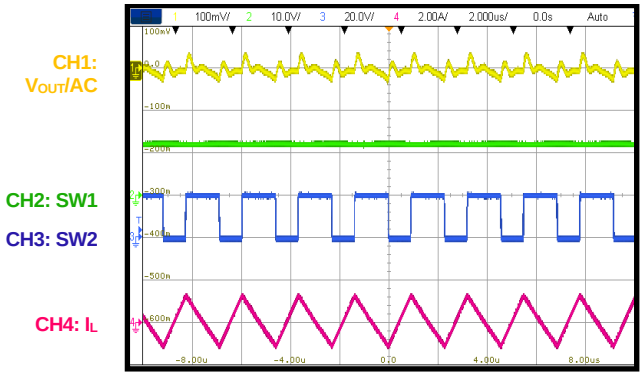
Output Voltage Ripple

V_{OUT} = 12V, load = 5A, f_{SW} drops by 50% in buck-boost mode



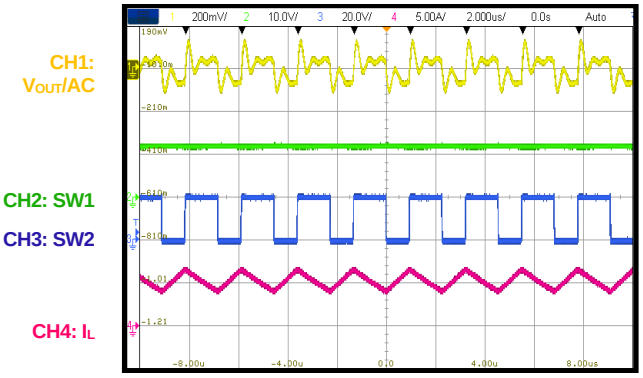
Output Voltage Ripple

V_{OUT} = 20V, load = 0A



Output Voltage Ripple

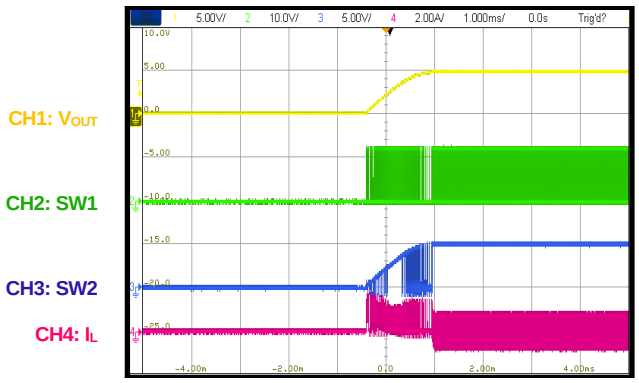
V_{OUT} = 20V, load = 3A



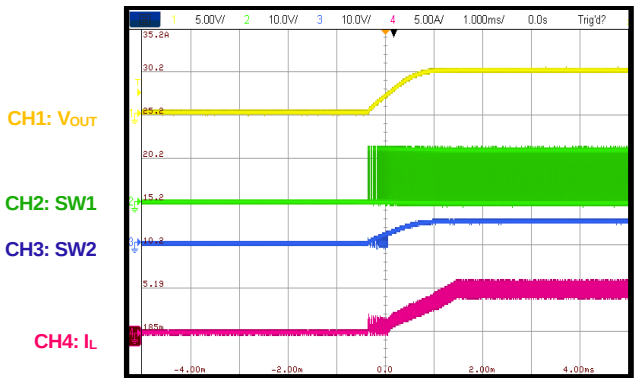
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

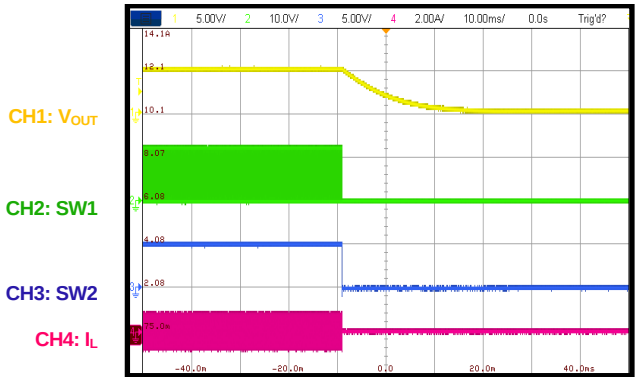
I²C Operation On
Load = 0A



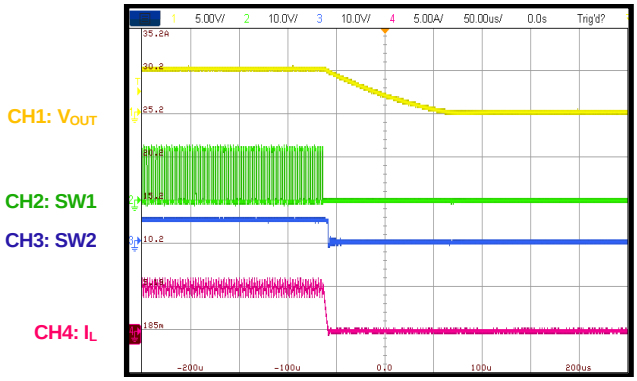
I²C Operation On
Load = 5A



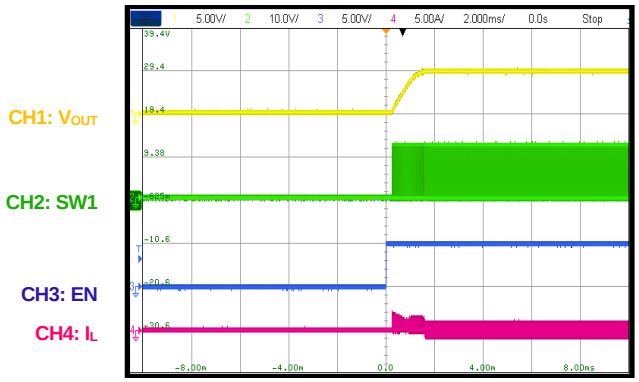
I²C Operation Off
Load = 0A



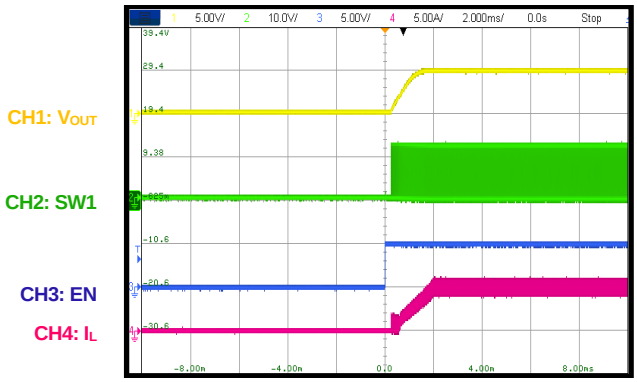
I²C Operation Off
Load = 5A



EN Pin Enabled
Load = 0A



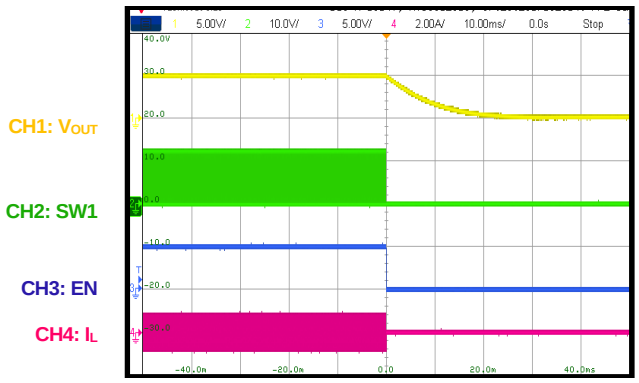
EN Pin Enabled
Load = 5A



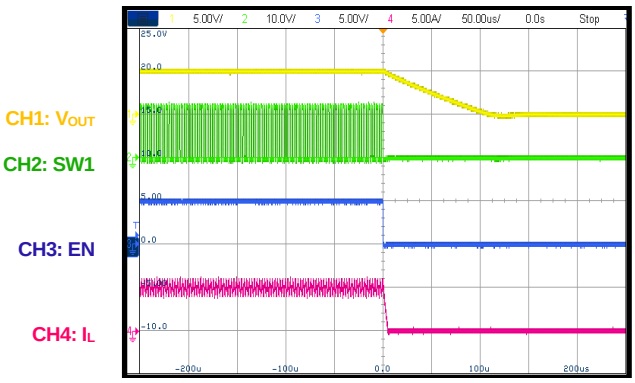
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

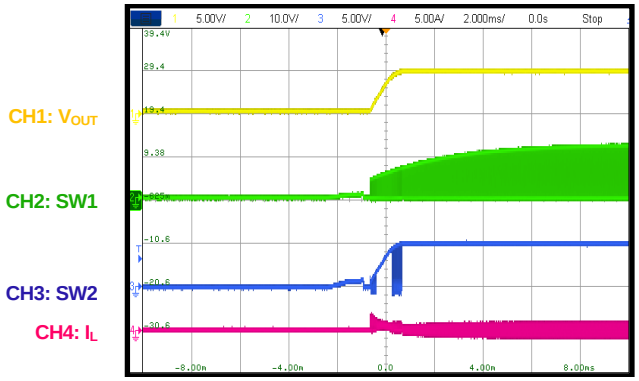
EN Pin Disabled
Load = 0A



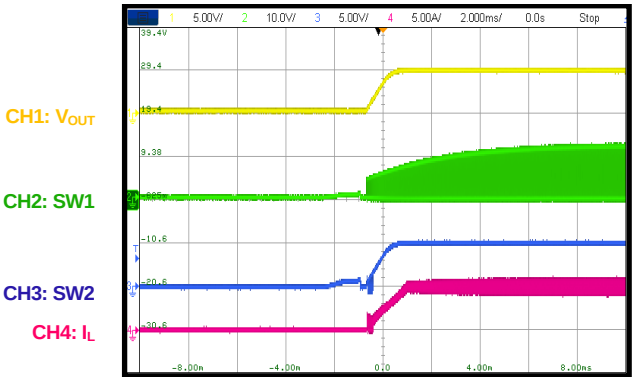
EN Pin Disabled
Load = 5A



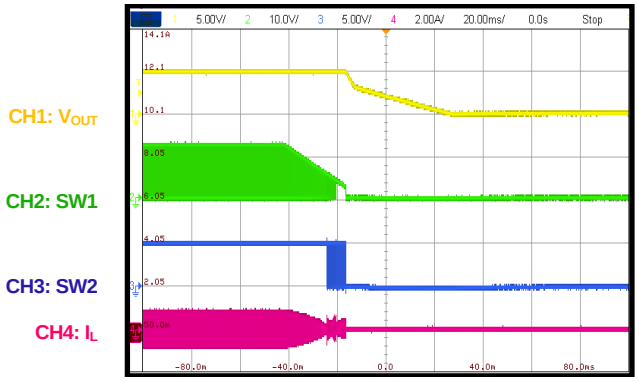
Start-Up through VIN
Load = 0A



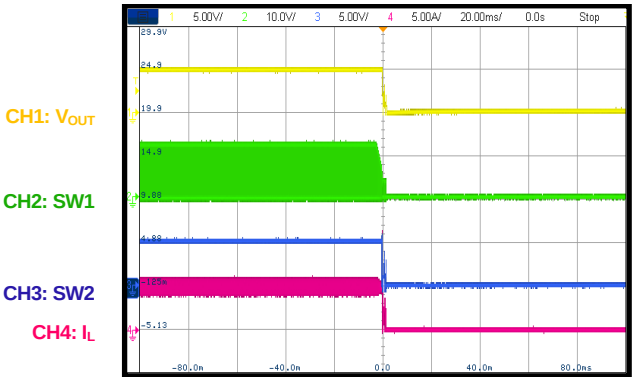
Start-Up through VIN
Load = 5A



Shutdown through VIN
Load = 10mA



Shutdown through VIN
Load = 5A

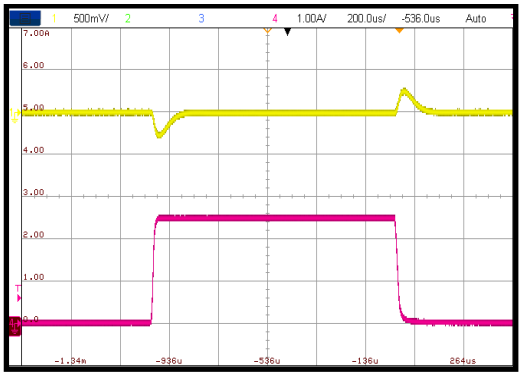


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

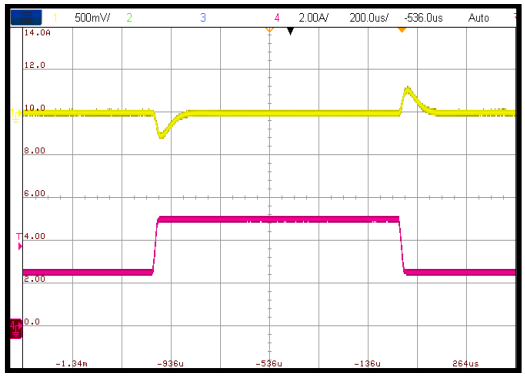
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A to 2.5A, 150mA/µs



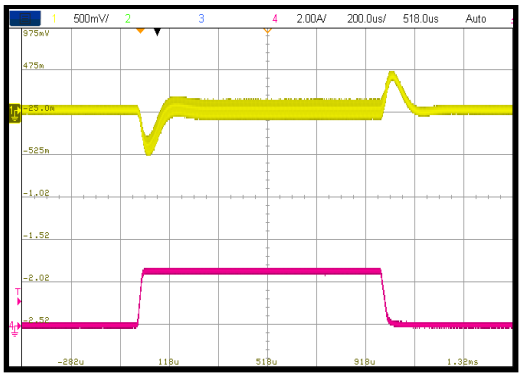
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.5A to 5A, 150mA/µs



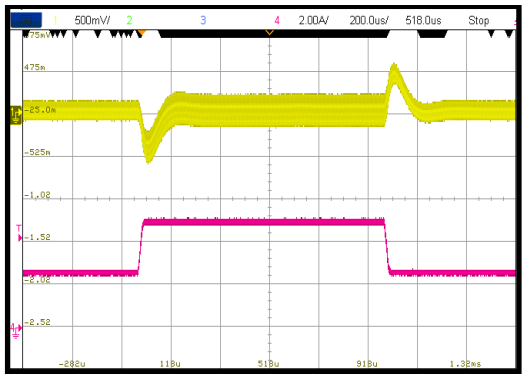
Load Transient Response

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 0A to 2.5A, 150mA/µs



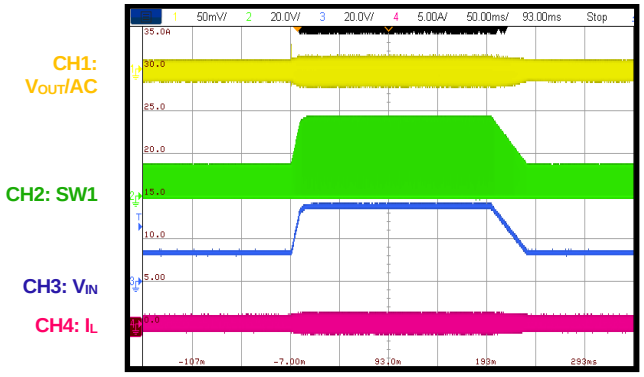
Load Transient Response

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 2.5A to 5A, 150mA/µs



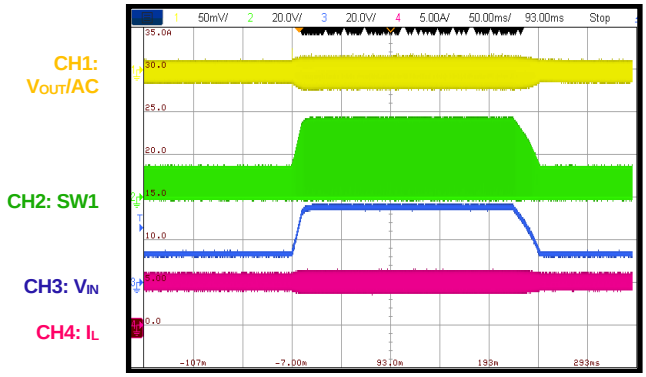
Input Voltage Transient

V_{IN} = 14V to 35V, V_{OUT} = 5V, load = 0A



Input Voltage Transient

V_{IN} = 14V to 35V, V_{OUT} = 5V, load = 5A

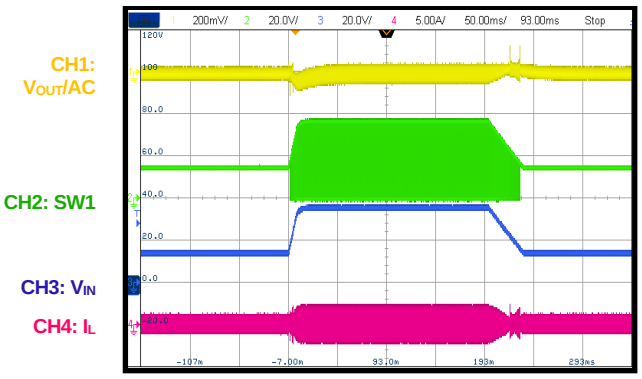


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

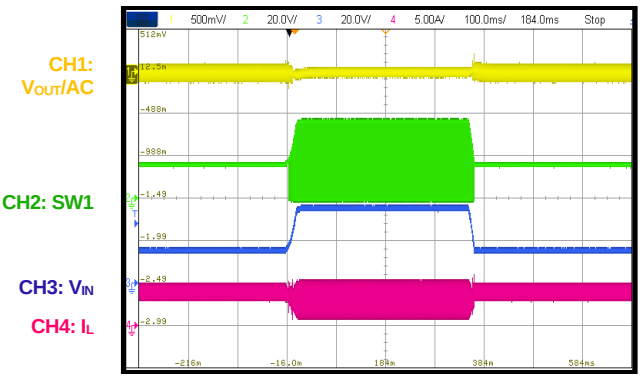
Input Voltage Transient

V_{IN} = 14V to 35V, V_{OUT} = 20V, load = 0A



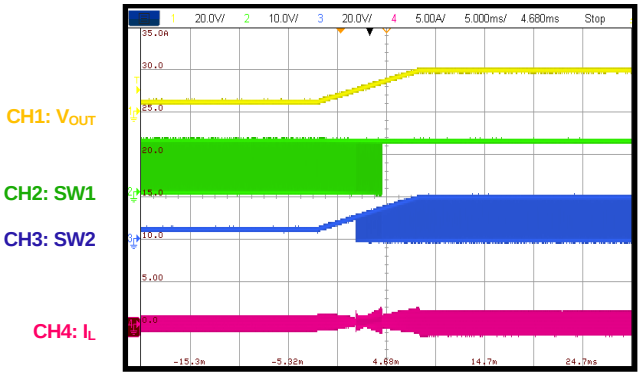
Input Voltage Transient

V_{IN} = 14V to 35V, V_{OUT} = 20V, load = 3A



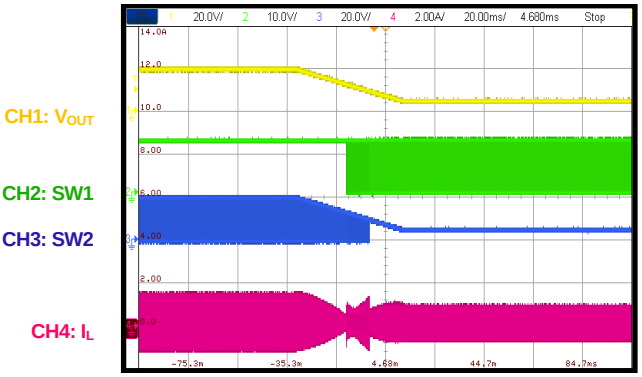
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 0A



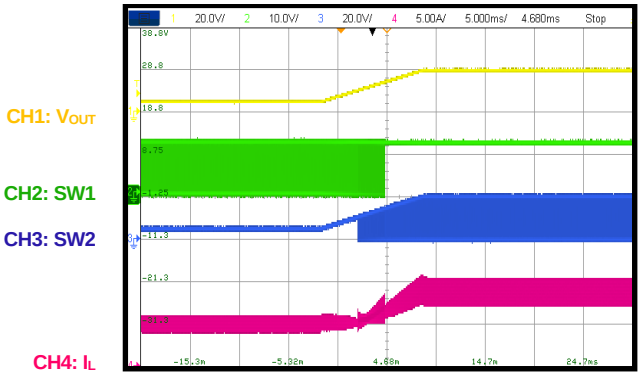
Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 0A



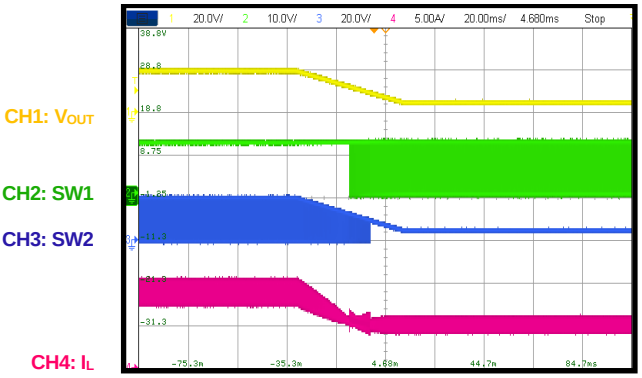
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 5A



Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 5A

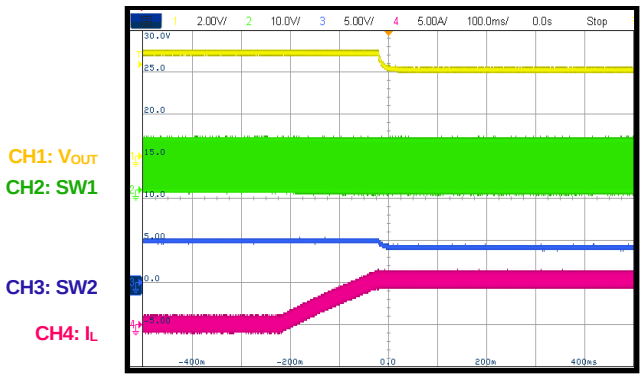


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

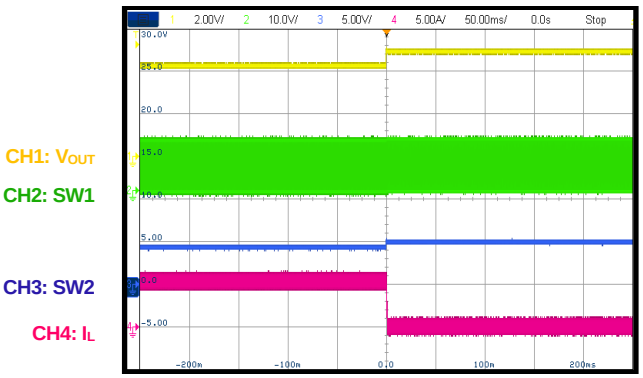
CC Entry

CV load = 4V, CC limit = 5.4A

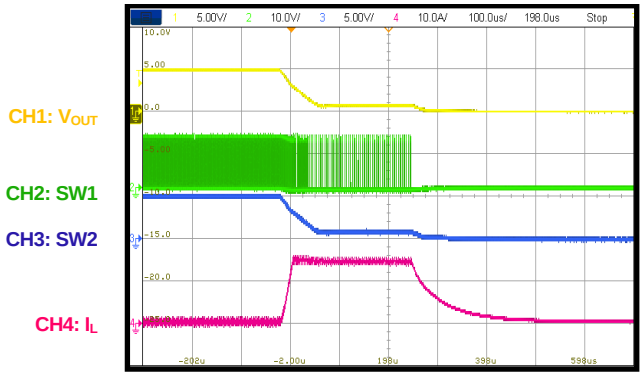


CC Recovery

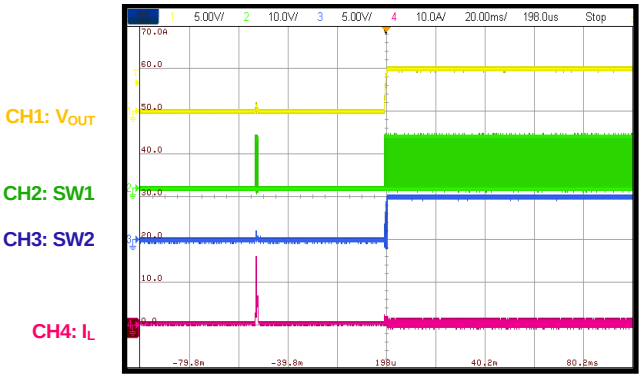
CV load = 4V, CC limit = 5.4A



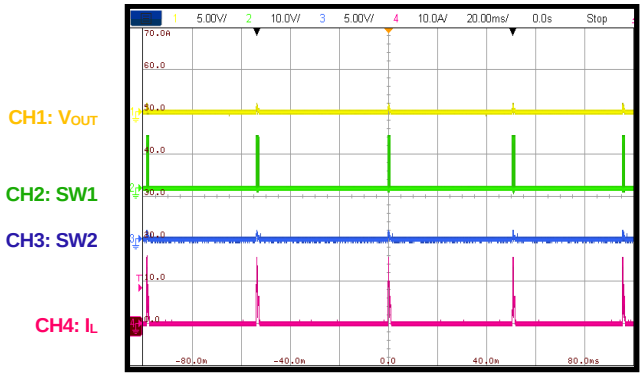
Short-Circuit Protection Entry



Short-Circuit Protection Recovery



SCP Steady State



FUNCTIONAL BLOCK DIAGRAM

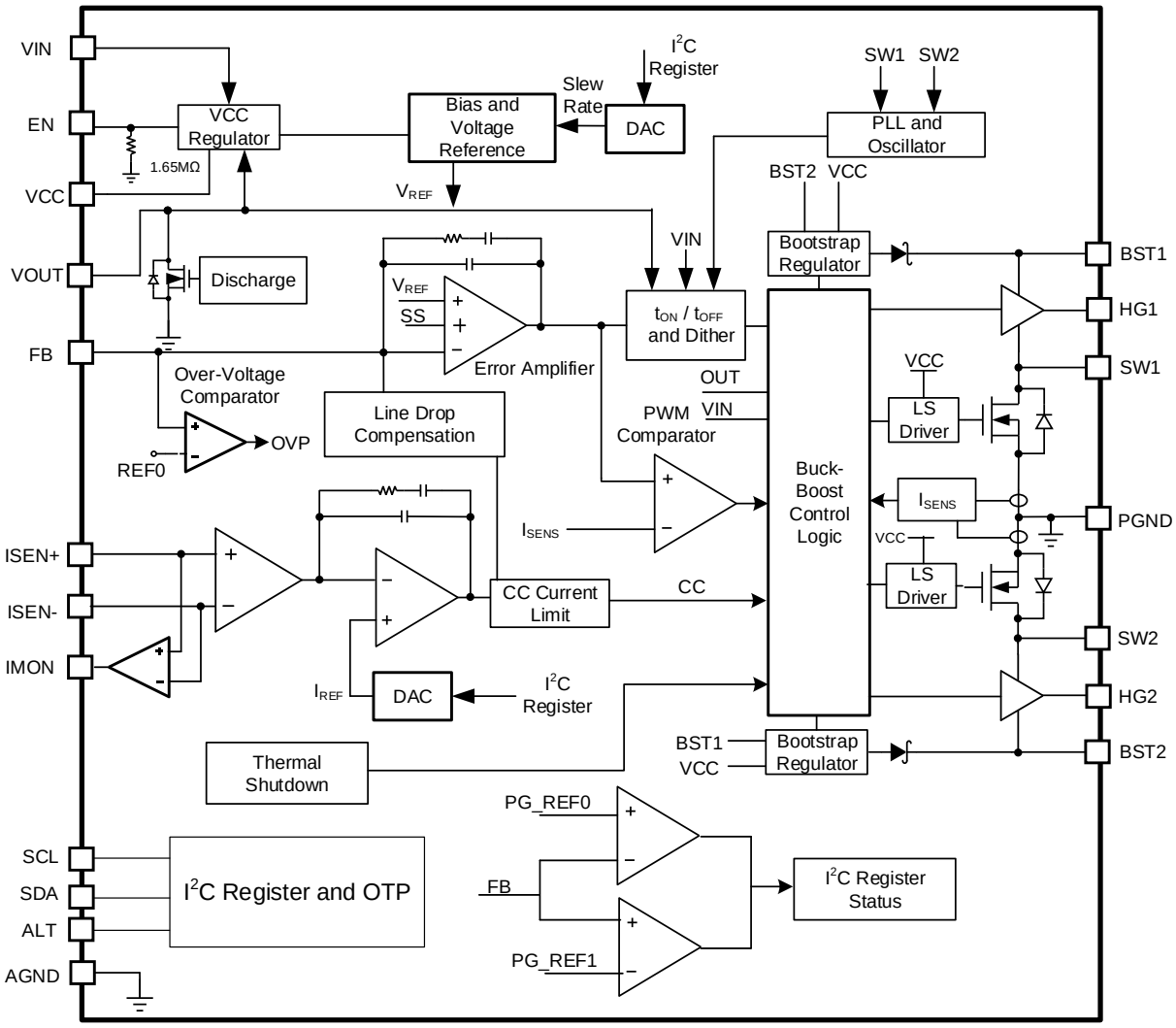


Figure 1: Functional Block Diagram

OPERATION

The MP4247 is a buck-boost converter with integrated low-side MOSFETs (LS-FETs). The device operates with a fixed frequency for all modes (buck, boost, and buck-boost). A special buck-boost control strategy provides high efficiency across the full input range, with a smooth transient between different modes. Figure 1 on page 19 shows the internal block diagram.

Buck-Boost Operation

The MP4247 can regulate the output voltage (V_{OUT}) above, equal to, or below the input voltage (V_{IN}). The device has a one inductor, four-switch (SWA, SWB, SWC, and SWD) power structure (see Figure 2).

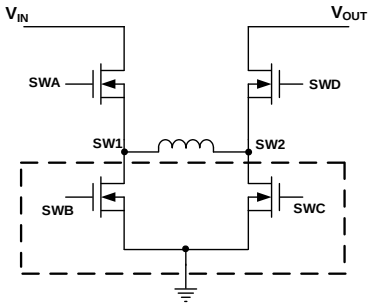


Figure 2: Buck-Boost Topology

Based on this architecture, the MP4247 can operate in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 3).

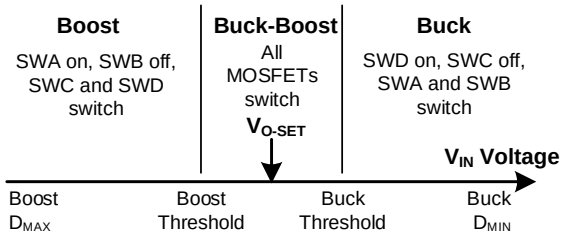


Figure 3: Buck-Boost Operation Range

Buck Mode (V_{IN} > V_{OUT})

When V_{IN} is significantly greater than V_{OUT}, the MP4247 works in buck mode. SWA and SWB switch for buck regulation. Meanwhile, SWC is off, and SWD remains on to conduct the inductor current (I_L).

In each buck mode cycle, SWA first turns on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). After SWA turns off, SWB turns on to conduct I_L until it triggers the COMP control signal. By repeating this operation, the converter regulates V_{OUT}.

Boost Mode (V_{IN} < V_{OUT})

When V_{IN} is significantly lower than V_{OUT}, the MP4247 operates in boost mode. In boost mode, SWC and SWD switch for boost regulation. Meanwhile, SWB is off, and SWA remains on to conduct I_L.

In each boost mode cycle, SWC turns on to conduct I_L. When I_L rises and triggers the control signal on the COMP pin, SWC turns off and SWD turns on for the freewheel current. Then SWC turns on and off repeatedly to regulate V_{OUT}.

Buck-Boost Mode (V_{IN} ≈ V_{OUT})

When V_{IN} is almost equal to V_{OUT}, the converter cannot provide enough energy to the load in buck mode due to SWA's minimum off time. In boost mode, the converter supplies too much power to load due to SWC's minimum on time. Under these conditions, the MP4247 utilizes buck-boost control to regulate the output.

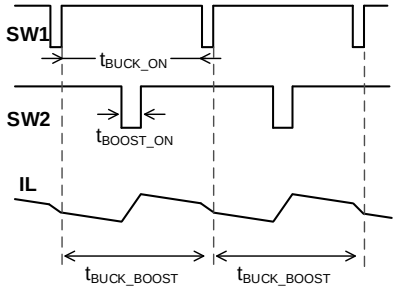


Figure 4: Buck-Boost Waveform

If V_{IN} is almost equal to V_{OUT}, the device operates in buck-boost mode, and one boost switching cycle is inserted into each buck switching period. The MOSFETs turn on in the following sequence:

1. SWA and SWD
2. SWA and SWC
3. SWA and SWD
4. SWB and SWD

This process allows I_L to meet the COMP voltage (V_{COMP}) requirement while also supplying sufficient current to the output.

Working Mode Selection

The MP4247 works with a fixed frequency under heavy-load conditions. When the load current decreases, the MP4247 can operate in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

Forced Continuous Conduction Mode (FCCM) (Forced PWM)

When the MP4247 works in FCCM, the buck on time and boost off time are determined by the internal circuit to achieve a fixed frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average input current (I_{IN}) drops, and I_L may go negative from VOUT to VIN during the off time (while SWD is on). This forces I_L to work in FCCM with a fixed frequency, which produces a lower output voltage ripple than in PSM.

Pulse-Skip Mode (PSM) (Auto-PFM/PWM)

Once I_L drops to 0A in pulse-skip mode (PSM), SWD turns off to prevent the current from flowing from VOUT to GND. This forces I_L to work in discontinuous conduction mode (DCM). Simultaneously, the internal off time clock becomes longer once the MP4247 enters DCM. When the I_L conduction period decreases, the frequency drops, which saves power loss and reduces the output voltage ripple.

If V_{COMP} drops to the PSM threshold, the MP4247 stops switching to reduce switching power loss. The MP4247 resumes switching once V_{COMP} exceeds the PSM threshold. The switching pulse skip is based on V_{COMP} under very light-load conditions. PSM has a higher efficiency than FCCM under light loads, but the output voltage ripple may be higher due to the group switching pulse.

Power Supply

The MP4247 internal circuit (including the gate drivers) is powered by VCC. When V_{IN} is sufficient and EN is high, the MP4247 tries to regulate the VCC voltage (V_{CC}) at 5V. V_{CC} and BST have separate under-voltage lockout (UVLO) thresholds that can keep the gate signal off.

If V_{IN} and V_{OUT} are both above 7.5V, then the MP4247 powers VCC from the lower voltage source of the two values to reduce power loss. If V_{IN} and V_{OUT} are not both above 7.5V, the MP4247 powers VCC from the higher voltage power source between V_{IN} and V_{OUT} to ensure that the VCC voltage is sufficiently high. Both V_{CC} and BST should have sufficient voltage to enable the MP4247 to switch.

EN Control

The MP4247 has an enable control pin (EN). Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.

The MP4247 EN is a high voltage pin, it can be connected to VIN directly or through a resistor. It also can program EN divider resistor to set VIN on/off threshold. It is recommended to use a resistor when using an external analog signal to control EN (see Figure 5).

Suggest to add a EN divider resistor to set the VIN shutdown threshold voltage >4V, which can protect the input current extremely high during input power down at boost mode. If operation input voltage is always <4V, suggest to connect Vin and EN directly.

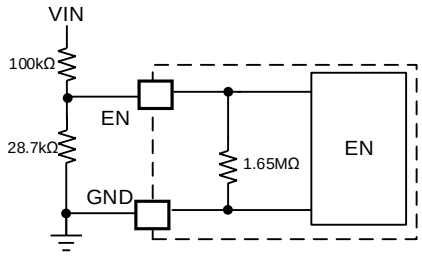


Figure 5: EN Connection

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors V_{IN} and V_{CC}. The MP4247 is enabled when V_{CC} exceeds its rising UVLO threshold. The MP4247 stops working if either V_{IN} or V_{CC} falls below its respective UVLO falling threshold.

Internal Soft Start (SS)

Internal soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} is below V_{REF}, the error amplifier (EA) uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

If the output of the MP4247 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side MOSFETs (HS-FETs and LS-FETs, respectively) until the voltage on the internal SS capacitor (C_{SS}) exceeds the internal V_{FB}.

Constant Current (CC) Mode Over-Current-Protection

The MP4247 senses the ground current using the ISEN+ and ISEN- pins. If the output current (I_{OUT}) exceeds the set current limit threshold, the MP4247 enters constant current (CC) limit mode. In this mode, the current amplitude is limited. As the load resistance is reduced, V_{OUT} drops until V_{FB} falls below the under-voltage (UV) threshold, which is about 40% below V_{REF}. Once the UV threshold is triggered and V_{OUT} falls below 3V, the MP4247 enters hiccup mode to periodically restart the part.

This protection is especially useful when the output is dead-shorted to ground, as it greatly reduces the average short circuit current, alleviates thermal issues, and protects the regulator. Once the over-current (OC) condition is removed, the MP4247 exits hiccup mode and resumes normal operation.

Switching Current Limit

The MP4247 senses the LS-FET current in the loop control. This allows the device to provide valley current limiting in buck mode and peak current limiting in boost mode, during each cycle-by-cycle switching period. In buck mode, the next period does not start until I_L drops to the valley current limit, so the device may fold back the frequency when the valley current limit is triggered.

Based on the cycle-by-cycle switching current limit, the MP4247 maximum input current (I_{IN_MAX}) in buck mode can be calculated with Equation (1):

$$I_{IN\_MAX}(A) = \frac{V_{OUT}}{V_{IN}} \times \eta \times (Valley\_Current\_Limit(A) + \frac{V_{IN} - V_{OUT}}{2 \times L(\mu H) \times f(kHz)} \times \frac{V_{OUT}}{V_{IN}} \times 10^3) \quad (1)$$

Where η is the efficiency.

The MP4247's I_{IN_MAX} in boost mode can be calculated with Equation (2):

$$I_{IN\_MAX}(A) = Peak\_Current\_Limit(A) - \frac{V_{IN}}{2 \times L(\mu H) \times f(kHz)} \times \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times 10^3 \quad (2)$$

The buck valley current limit is typically 13A. The boost peak current limit is typically 15A. The switching current limit can be configured in the I²C register (0xD3, bits D[7:6]).

Output Over-Voltage Protection (OVP)

The MP4247 has output over-voltage protection (OVP). If V_{OUT} exceeds 120% of V_{REF}, then SWA, SWC, and SWD turn off. The resistor discharge path from the VOUT pin to ground turns on. When V_{FB} drops to 110% of V_{REF}, the chip resumes normal operation.

The absolute output OVP threshold is about 25.5V. The discharge resistor turns on when absolute OVP is triggered. Set OUTPUT_OVP_EN to 0 to disable both OVP and absolute OVP. If the output is biased by external power supply, the output reverse current should be smaller than 1.5A.

Gate Driver and BST Power

The MP4247 provides two N-channel MOSFET gate drivers for the H-bridge MOSFETs. Each driver is capable of sourcing and sinking current. In buck mode, HG1 switches while HG2 stays on continuously. In boost mode, HG2 switches while HG1 stays on continuously. HG1 and HG2 are both powered by BST1 and BST2.

Capacitors between BST1-to-SW1 and BST2-to-SW2 are necessary to supply the power, which is powered by internal diode from VCC or charge them by each other.

The BST power has its own UVLO control. Its UVLO rising threshold is about 2.7V, with a 200mV hysteresis.

Switching Frequency and Frequency Spread Spectrum Function

The MP4247 configures the switching frequency (f_{SW}) with the 2-bit FREQ register. f_{SW} can be set to 280kHz, 420kHz, or 600kHz. A 420kHz f_{SW} is typically recommended.

The MP4247 has a frequency spread spectrum function. Set DITHER_ENABLE to 1 (0xD0, bit D[7]) to enable this function. Set the bit to 0 to disable the function. The purpose of spread spectrum is to minimize the peak emissions at certain frequencies.

The MP4247 uses a 4kHz triangle wave to modulate the internal oscillator. The frequency

span for spread spectrum operation is ±15%.

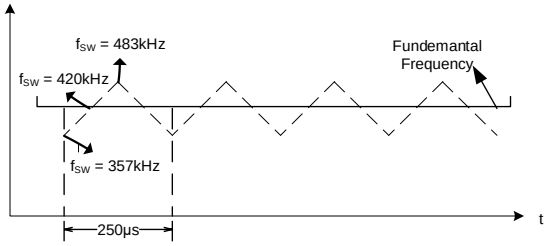


Figure 6: Frequency Spread Spectrum

The MP4247 spread frequency function can be enabled for all configurable f_{SW} values.

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Slew Rate Control and Output Discharge

The MP4247 can adjust the output voltage slew rate. The rising slew rate can be changed via the internal SR bits (0xD3, bits D[4:3]), and the falling slew rate can be changed via the SR bits (0xD3, bits D[2:1]). There are four potential V_{REF} changes (rising and falling), or slew rates, that can be selected for different application requirements.

If the output capacitance is too high, V_{OUT} may not discharge to the target voltage by the time that V_{REF} charging is complete. If this occurs, the OVP discharge function can continue discharging C_{OUT}.

The output discharge function is enabled if the following conditions are met:

1. The output OVP threshold (about 120% of V_{FB}) has been reached, or absolute OVP is triggered.
2. The I²C OPERATION command sends an off command, or the EN pin is off. Discharge works until a 200ms delay passes, or if V_{FB} drops below 50mV.
3. If V_{IN} UVLO is triggered but VCC has residual voltage, the MP4247 V_{OUT} discharges for a limited time. This discharge function is disabled after the VCC voltage drops below 1.8V.

Output Line Drop Compensation

The MP4247 can compensate for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant load-side voltage.

See the MFR_CTRL2 section on page 30 for details on the line drop compensation amplitude.

Current Monitor Output

The MP4247 senses the average load current through one sensing resistor, and the device outputs a voltage signal on the IMON pin. This signal is amplified by the voltage difference between ISEN+ and ISEN-. It is recommended to place a small capacitor from IMON to AGND.

In PFM, IMON can only work normally when the MP4247 operates in FCCM.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. Once the temperature returns to below the lower threshold (typically 140°C), the chip is enabled and resumes normal operation.

PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. When connected to the lines, a master device generates an SCL signal and device address, then arranges the communication sequence. This is based on I²C operation principles.

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and end of the PMBus transfer. A start (S) command is defined as the SDA signal transitioning from high to low while SCL is high. A stop (P) command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 7).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge (ACK) bit.

PMBus Update Sequence

The MP4247 requires a start command, a valid PMBus address, a register address byte, and a data byte for a single data update. The device acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MP4247. The device performs an update on the falling edge of the LSB byte.

PMBus Bus Message Format

Figure 8 on page 25 shows the PMBus message format. Unshaded cells indicate that the bus host is actively driving the bus, while shaded cells indicate that the MP4247 is driving the bus.

- S = Start command
- Sr = Repeated start command
- P = Stop command
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

“A” represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is successfully received by a device.

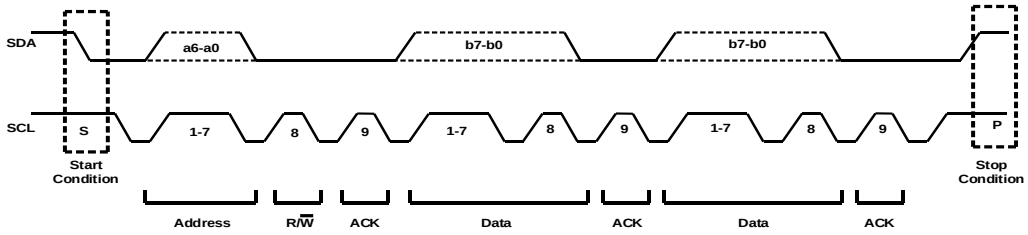


Figure 7: Data Transfer Over the PMBus

a) Send Byte

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	P

b) Write Byte

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

c) Write Word

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

d) Read Byte

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	$\overline{A}$	P

e) Read Word

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	$\overline{A}$	P

Figure 8: PMBus Message Format

REGISTER DESCRIPTION

I²C/PMBus Register

Once V_{IN} and EN both exceed the UVLO threshold, the I²C is enabled. The default register value is based on MP4247-0000.

CMD Name	Command Code	Description	Type	Data Format	Unit	OTP	Default Value
OPERATION	0x01	On/off	R/W byte	Reg		Y	On
CLEAR_FAULTS	0x03		Send byte	Reg		N	
VOUT_COMMAND	0x21		R/W word	L16	V	Y	5V
STATUS_WORD	0x79		R word	Reg		N	
STATUS_TEMPERATURE	0x7D		R byte	Reg		N	
MFR_CTRL1	0xD0		R/W byte	Reg		Y	
MFR_CURRENT_LIMIT	0xD1	Sets the continuous CC limit	R/W byte	Reg		Y	5.4A
MFR_CTRL2	0xD2	Sets line drop compensation	R/W byte	Reg		Y	
MFR_CTRL3	0xD3		R/W byte	Reg		Y	
MFR_CTRL4	0xD4		R/W byte	Reg		Y	
MFR_STATUS_MASK	0xD8	Masks the ALT# pin indication	R/W byte	Reg		Y	
MFR_OTP_CONFIGURATION_CODE	0xD9	OTP configuration code	R/W byte	Reg		Y	
MFR_OTP_REVISION_NUMBER	0xDA	OTP software revision	R/W byte	Reg		Y	

Data Format

Linear16 (L16) format is used for VOUT_COMMAND. Figure 9 shows how to read V_{OUT}.

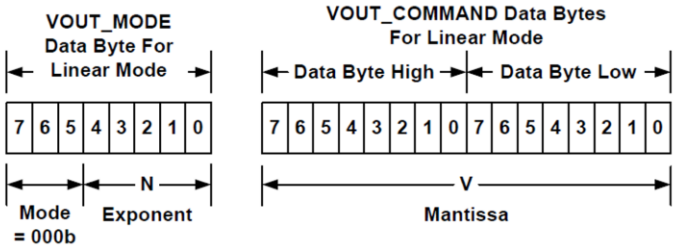


Figure 9: Reading V_{OUT}

The MODE bits are set to 000b. The voltage can calculated with Equation (3):

$$Voltage = V \times 2^{N} \quad (3)$$

Where Voltage is the parameter of interest (in V); V is a 16-bit unsigned binary integer; and N is a 5-bit, two's complement, binary integer.

PMBUS COMMANDS

OPERATION

The OPERATION command configures the converter's operational state.

Bits	Description	Hex	Meaning
7:0	Sets the device to the on or off state. Note that the EN pin has a higher control priority than this bit.	00h	The output is off.
		01h or 80h	The output is on. This is the default value.

CLEAR_FAULTS

The CLEAR_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. Meanwhile, the device clears (releases) its ALT# signal output if the ALT# signal has been asserted.

If the MP4247 has latched off due to a fault, issuing a CLEAR_FAULTS command does not restart the device. If the fault is still present once the bit is cleared, then the the fault bit is immediately set again and the host is notified. This command is write-only (see Figure 8 on page 25).

VOUT_COMMAND

The VOUT_COMMAND sets V_{OUT}. It follows Linear16 data format.

Command	VOUT_COMMAND															
Format	Linear16															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Data byte high								Data byte low							
Default value (5V)	5120 decimal															

The output voltage (V_{OUT}) can be estimated with Equation (4):

$$V_{OUT} = V \times 2^{-10} \quad (4)$$

Where V is a 16-bit, unsigned binary integer determined by VOUT_COMMAND, bits[15:0].

The valid V_{OUT} range is 1V to 21.47V. Any voltages outside this range are considered abnormal.

The feedback resistor ratio should be $V_{OUT} / V_{FB} = 10$. The VOUT_COMMAND resolution is 10mV.

The internal reference voltage (V_{REF}) is equal to $V_{OUT} / 10$. The internal V_{REF} range is 0.1V to 2.147V with 1mV/step, for a total of 2047 steps. This value is controlled by the 11-bit DAC. When the DAC input is set to 0, the DAC output is 0.1V.

STATUS_WORD

The STATUS_WORD command returns 2 bytes of information with a summary of the MP4247's fault conditions. Based on the information in these bytes, the host can obtain more information by reading the relevant status registers.

Byte	Bit	Bit Name	Meaning
Low	7	RESERVED	Reserved. The default value is 0b.
	6	RESERVED	Reserved. The default value is 0b.
	5	VOUT_OV_FAULT	Indicates whether a V_{OUT} over-voltage (OV) fault has occurred.
	4	IOUT_OC_FAULT	Indicates whether an output current (I_{OUT}) over-current (OC) fault has occurred. If the device reaches the constant current (CC) limit or the peak current limit, or if the device enters hiccup mode, then this bit is set.
	3	RESERVED	Reserved. The default value is 0b.
	2	TEMPERATURE	Indicates whether a temperature-related fault has occurred.
	1	RESERVED	Reserved. The default value is 0b.
	0	RESERVED	Reserved. The default value is 0b.
High	7	VOUT	Indicates whether a V_{OUT} fault or warning has occurred.
	6	IOUT	Indicates whether an I_{OUT} fault has occurred. If the device reaches the constant current (CC) limit or the peak current limit, or if the device enters hiccup mode, then this bit is set.
	5	RESERVED	Reserved. The default value is 0b.
	4	OC_EXIT	Indicates whether I_{OUT} has exited the constant current (CC) limit. This bit is only set high when I_{OUT} exits CC mode (before entering hiccup mode). This bit does not reset once the device recovers from hiccup mode.
	3	PG_STATUS#	The POWER_GOOD signal, if present, is ignored. If V_{OUT} is not power good, this bit is set to 1. Once V_{OUT} is power good, this bit is cleared.
	2	RESERVED	Reserved. The default value is 0b.
	1	RESERVED	Reserved. The default value is 0b.
	0	RESERVED	Reserved. The default value is 0b.

All STATUS bits remain set, except for the PG_STATUS# bit. This bit always reflects the current state of the POWER_GOOD signal (if present).

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns 1 data byte with information regarding the MP4247.

Bit	Bit Name	Description
7	OT_FAULT	Indicates whether an over-temperature (OT) fault has occurred. The OTP entry threshold is 160°C.
6	RESERVED	Reserved.
5	RESERVED	Reserved.
4	RESERVED	Reserved.
3	RESERVED	Reserved.
2	RESERVED	Reserved.
1	RESERVED	Reserved.
0	RESERVED	Reserved.

I²C REGISTER MAP

Name	REG (0x)	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MFR_CTRL1	D0	R/W	DITHER_ ENABLE	FREQ		SWA_FET_ RON		OUTPUT_ OVP_EN	OUTPUT_ DISCHARGE_ EN	PFM/PWM_ MODE
MFR_CURRENT_ LIMIT	D1	R/W	LDC_ DISABLE	CONSTANT_CURRENT_LIMIT (1A to 5.4A, 50mA/step)						
MFR_CTRL2	D2	R/W							LINE_DROP_ COMPENSATION	
MFR_CTRL3	D3	R/W	SWITCHING_ CURRENT_LIMIT		RSENS	SLEW_ RATE_RISE		SLEW_RATE_FALL		FREQ_ MODE
MFR_CTRL4	D4	R/W	CC_BLANK_TIMER		SW2_ EDGE	I2C_ADDRESS				
MFR_STATUS_MASK	D8	R/W	Masks the ALT# pin indication if a fault or event occurs							
MFR_OTP_ CONFIGURATION_ CODE	D9	R/W	OTP configuration code, defined by MPS							
MFR_OTP_REVISION _NUMBER	DA	R/W	OTP software revision number, defined by MPS							

I²C Slave Address

The I²C slave address is 67h by default (see Table 1).

Table 1: I²C Address

I²C Address A7:A1	
Binary	**Hex**
1100 111 (Default)	67h
I²C/OTP adjustable for A5~A1	Set by MFR_CTRL4, bits D[4:0]

MFR_CTRL1

Address: 0xD0
Reset value: Set via the OTP
Type: Read and write

Bits	Bit Name	Description
D[7]	DITHER_ENABLE	0: No dithering (default) 1: Enables frequency spread spectrum
D[6:5]	FREQ	Sets the switching frequency. These bits are set to 01 by default. 00: 280kHz 01: 420kHz 10: 600kHz 11: Reserved
D[4:3]	SWA_FET_RON	Those bits set the external switch FET A's Ron resistance under 5Vgs. The value selection will affect the ZCD and negative current limit in boost mode. It should match the real MOSFET value. These bits are set to 01 by default. 00: 5mΩ 01: 10mΩ 10: 15mΩ 11: 20mΩ
D[2]	OUTPUT_OVP_EN	Enables V_{OUT} over-voltage protection (OVP) control. This bit is set to 1 by default. 1: Enabled 0: Disabled

D[1]	OUTPUT_ DISCHARGE_EN	Enables the output discharge function. For output discharge, a passive discharge resistor connected from VOUT to ground turns on. Discharge works until V_{OUT} drops below 50mV, or the maximum 200ms timer ends. The bit is set to 1 by default. 1: The MP4247 turns on the output discharge function during an EN, V_{IN}, or I^2C shutdown until V_{OUT} is fully discharged 0: Disables the output discharge function during an EN, V_{IN}, or I^2C shutdown
D[0]	PFM/PWM_MODE	Sets the buck-boost work mode. This bit is set to 1 by default. 1: Forced PWM 0: Auto-PFM/PWM

MFR_CURRENT_LIMIT

Address: 0xD1
Reset value: Set via the MTP
Type: Read and write

Sets the output constant current (CC) limit threshold.

Bit Name	LDC_ DISABLE	CONSTANT_CURRENT_LIMIT						
Format	Direct, unsigned binary integer							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value (5.4A)	0	108 integer						

The real-world IOUT_OC (in A) can be calculated with Equation (5):

$$IOUT\_OC\ (A) = IOUT\_LIM \times 0.05 \quad (5)$$

Where IOUT_LIM is a 7-bit unsigned binary integer of IOUT_LIM, bits D[6:0].

The IOUT_OC resolution (or minimum step) is 50mA, with a 5.4A maximum. If the current is set outside this range, then the current limit is clamped at 5.4A.

Bit D[7] enables line drop compensation control. If this bit is set to 0, then line drop compensation is controlled by the 0xD2 register. If this bit is set to 1, then line drop compensation is disabled.

MFR_CTRL2

Address: 0xD2
Reset value: Set via the OTP
Type: Read and write

Bits	Bit Name	Description
D[7:2]	RESERVED	Reserved.
D[1:0]	LINE_DROP_ COMPENSATION	Sets the V_{OUT} compensation value vs. load current. The compensation amplitude is fixed for any V_{OUT}. Line drop compensation is only enabled when $V_{OUT} \geq 5V$. These bits are set to 00 by default. 00: No compensation 01: V_{OUT} compensates 100mV when I_{OUT} is 3A 10: V_{OUT} compensates 300mV when I_{OUT} is 3A 11: V_{OUT} compensates 600mV when I_{OUT} is 3A

MFR_CTRL3

Address: 0xD3
Reset value: Set via the OTP
Type: Read and write

<table>
<tr><th>Bits</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>D[7:6]</td><td>SWITCHING_
CURRENT_LIMIT</td><td>Sets the SWB and SWC current limit.
<table>
<tr><th></th><th>SWC Peak Current Limit</th><th>SWB Valley Current Limit</th></tr>
<tr><td>00</td><td>8A</td><td>6A</td></tr>
<tr><td>01</td><td>12A</td><td>9A</td></tr>
<tr><td>10 (default)</td><td>15A</td><td>13A</td></tr>
<tr><td>11</td><td>20A</td><td>17A</td></tr>
</table></td></tr>
<tr><td>D[5]</td><td>RSENS</td><td>Selects the value for R_{SENS}. This bit is set to 0 by default.

0: 5mΩ
1: 10mΩ</td></tr>
<tr><td>D[4:3]</td><td>SLEW_RATE_RISE</td><td>Sets the V_{OUT} rising slew rate. These bits are set to 01 by default. The slew rate can be calculated with the following equation:

V_{OUT}_Slew_Rate = V_{REF}_Slew_Rate x Feedback_Ratio

Where Feedback_Ratio = 10.

00: 0.08mV/µs V_{REF} rising slew rate
01: 0.16mV/µs V_{REF} rising slew rate
10: 0.4mV/µs V_{REF} rising slew rate
11: 0.8mV/µs V_{REF} rising slew rate</td></tr>
<tr><td>D[2:1]</td><td>SLEW_RATE_FALL</td><td>Sets the V_{OUT} rising slew rate. These bits are set to 01 by default. The slew rate can be calculated with the following equation:

V_{OUT}_Slew_Rate = V_{REF}_Slew_Rate x Feedback_Ratio

Where Feedback_Ratio = 10.

00: 0.02mV/µs V_{REF} falling slew rate
01: 0.04mV/µs V_{REF} falling slew rate
10: 0.1mV/µs V_{REF} falling slew rate
11: 0.2mV/µs V_{REF} falling slew rate</td></tr>
<tr><td>D[0]</td><td>FREQ_MODE</td><td>Sets the frequency mode in buck-boost mode. This bit is set to 0 by default.

0: Reduce the frequency to half of that in buck or boost mode (default)
1: Keep the same frequency as in buck or boost mode</td></tr>
</table>

MFR_CTRL4

Address: 0xD4
Reset value: Set via the OTP
Type: Read and write

Bits	Name	Description
D[7:6]	CC_BLANK_TIMER	Sets the blank time before entering constant current (CC) mode. These bits are set to 00 by default. 00: 320µs 01: 4.2ms 10: 8ms 11: 12ms
D[5]	SW2_EDGE	Selects the SW2 rising and falling speed. This bit is set to 1 by default. 0: Normal 1: Faster (default)

D[4:0]	I2C_ADDRESS	Sets the I²C slave address (A5–A1 bits). The default value is 00111b, which makes the default I²C slave address 67h.

MFR_STATUS_MASK

Address: 0xD8
Reset value: Set via the OTP
Type: Read and write

This register only can mask off the ALT# pin behavior. The STATUS register still indicates each event.

Bit	Status Bit Name	Description
7	VOUT_MSK	0: No mask 1: Mask enabled (default)
6	IOUT/POUT_MSK	This bit masks IOUT_OC_FAULT, IOUT/POUT and OC_EXIT. This bit is set to 0 by default. 0: No mask (default) 1: Mask enabled
5	RESERVED_MSK	0: No mask 1: Mask enabled (default)
4	TEMP_MSK	Masks temperature-related faults. 0: No mask 1: Mask enabled (default)
3	PG_STATUS#_MSK	Masks higher-level PG control. 0: No mask 1: Mask enabled (default)
2	PG_ALT_EDGE_MSK	0: No mask. The ALT pin indicates both the PG_STATUS# rising and falling edges 1: Mask enabled (default). The ALT pin only indicates the PG_STATUS# falling edge, which means V_{OUT} has changed from not good to good.
1	RESERVED_MSK	0: No mask 1: Mask enabled (default)
0	UNKNOWN_MSK	0: No mask 1: Mask enabled (default)

MFR_OTP_CONFIGURATION_CODE

Address: 0xD9
Reset value: Set via the OTP
Type: Read and write

Bits	Bit Name	Description
D[7:0]	OTP_CONFIGURATION_CODE	Sets the OTP configuration code, defined by MPS.

MFR_OTP_REVISION_NUMBER

Address: 0xDA
Reset value: Set via the OTP
Type: Read and write

Bits	Bit Name	Description
D[7:0]	OTP_REVISION_NUMBER	Sets the OTP software revision number, defined by MPS.

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

Inductor selection should be based on the work mode. The inductance for buck mode (L_{BUCK}) can be estimated with Equation (6):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Where ΔI_L is the peak-to-peak inductor ripple current, which is 30% to 50% of the maximum load current.

For boost mode, the inductor should limit the peak-to-peak current ripple (ΔI_L) to be between 30% and 50% of the maximum input current. The inductance for boost mode (L_{BOOST}) can be calculated with Equation (7):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (7)$$

Where $I_{LOAD(MAX)}$ is the maximum load current, and ΔI_L is the peak-to-peak ripple current (about 30% to 50% of the maximum input current).

$I_{IN(MAX)}$ can be estimated with Equation (8):

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)})}{V_{IN} \times \eta} \quad (8)$$

Where η is the efficiency.

Choosing a larger-value inductor reduces the ripple current, but also increases the size of the inductor and reduces the converter's achievable bandwidth by moving the right half-plane zero to lower frequencies. Choose an inductor that meets the application requirements.

Selecting the Input Capacitor

The input current is discontinuous in buck mode, but it is continuous in boost mode. This means that the capacitor must supply the AC current to the converter in buck mode while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and should be placed as close to the VIN pin as possible. Ceramic capacitors with X5R or X7R dielectrics are recommended because they are fairly stable amid temperature fluctuations. The capacitors must have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current in buck mode (I_{CIN}) can be estimated with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition in buck mode occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple (ΔV_{IN}) in buck mode can be estimated with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (12)$$

For the MP4247, a minimum 1µF ceramic capacitor should be placed near SWA.

Selecting the Output Capacitor

The output current is discontinuous in boost mode, so the output capacitor (C_{OUT}) must be able to reduce the output voltage ripple.

A higher capacitance may be required to reduce the output ripple and transient response. It is recommended to use low-ESR ceramic capacitors with X5R or X7R dielectrics.

With ceramic capacitors, the capacitance dominates the impedance at the switching frequency. This means the output voltage ripple is independent of the ESR.

The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} \quad (13)$$

Where V_{RIPPLE} is the output ripple voltage, and C_{OUT} is the output capacitance.

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output voltage ripple (ΔV_{OUT}) can be calculated with Equation (14):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} + \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}} \quad (14)$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

Choose output capacitors that satisfy the design's output ripple and load transient requirements. Consider the capacitance derating when designing applications with a high V_{OUT}.

Selecting the External MOSFETs (SWA and SWD)

The MP4247 requires two external N-channel power MOSFETs (SWA and SWD) (see Figure 9). In buck mode, SWA and SWB switch while SWD remains on. In boost mode, SWC and SWD switch while SWA remains on.

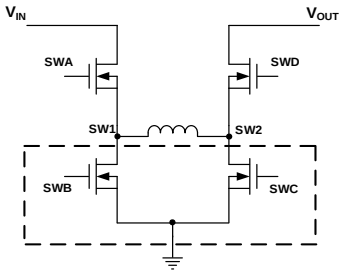


Figure 9: Buck-Boost Topology

The critical parameters when selecting a MOSFET are listed below:

1. Maximum drain-to-source voltage ($V_{DS(MAX)}$): SWA must be able to withstand the maximum V_{IN}. Additionally, SWA must withstand the transient spikes at SW1 during switching. Select SWA and SWB to have a $V_{DS(MAX)}$ that is 1.5 times V_{IN}.

   SWD must be able to handle V_{OUT} and additional transient spikes at SW2 during switching. Select SWD to have a $V_{DS(MAX)}$ that is 1.5 times V_{OUT}.
2. The maximum current ($I_{D(MAX)}$).
3. V_{TH}: The MP4247's driver voltages are supplied by VCC, so the gate plateau voltages of the MOSFETs should be below the minimum V_{CC}. Otherwise the MOSFETs may not fully turn on during start-up or under overload conditions.
4. The on resistance ($R_{DS(ON)}$).
5. Total gate charge (Q_G): For the MP4247, all switches Q_G should be smaller than 30nC (at a 5V GATE condition). The SW1 rising time and SW2 falling time are smaller than 15ns.

SWA

When the MP4247 works in boost mode, SWA is always on. Calculate SWA's conduction power loss ($P_{C\_LOSS(SWA)}$) with Equation (15):

$$P_{C\_LOSS(SWA)} = (I_{OUT}\times\frac{V_{OUT}}{V_{IN}})^2\times R_{DSON(SWA)} \quad (15)$$

Assume that the MOSFET's thermal resistance from junction to ambient is 50°C/W (this is determined by the board power dissipation), and the maximum acceptable temperature rise is 50°C. The maximum power loss ($P_{C\_LOSS(SWA)}$) can be estimated with Equation (16):

$$P_{C\_LOSS(SWA)} < 1W \quad (16)$$

Based on the above equations, select the MOSFET's on resistance.

When the MP4247 works in buck mode, the conduction loss ($P_{C\_LOSS(SWA)}$) and switching loss ($P_{SW\_LOSS(SWA)}$) on SWA can be calculated with Equation (17) and Equation (18), respectively:

$$P_{C\_LOSS(SWA)} = \frac{V_{OUT}}{V_{IN}}\times {I_{OUT}}^2\times R_{DSON(SWA)} \quad (17)$$

$$P_{SW\_LOSS(SWA)} = \frac{1}{2}V_{IN}\times I_{OUT}\times(t_{ON}+t_{OFF})\times f_{sw} \quad (18)$$

Figure 10 shows the switching on/off state.

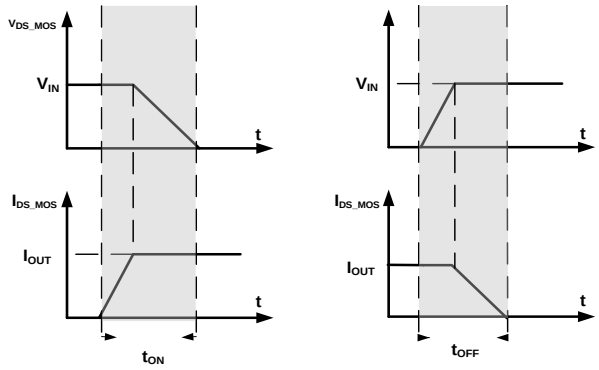


Figure 10: Switching On/Off State

The switching on time (t_{ON}) and the switching off time (t_{OFF}) are based on the MOSFET datasheet information.

SWD

When the MP4247 works in buck mode, SWD is always on, and its power loss ($P_{C\_LOSS(SWD)}$) can be calculated with Equation (19):

$$P_{C\_Loss(SWD)} = I_{OUT}^{2} \times R_{DSON(SWD)} \quad (19)$$

Similar to $P_{C\_LOSS(SWA)}$, $P_{C\_LOSS(SWD)}$ should also be below the maximum power loss.

When the MP4247 works in boost mode, the conduction power loss ($P_{C\_LOSS(SWD)}$) can be estimated with Equation (20):

$$P_{C\_Loss(SWD)} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^{2} \times R_{DS\_ON(SWD)} \quad (20)$$

The dead time and LS-FET switching loss can be ignored.

PCB Layout Guidelines (11)

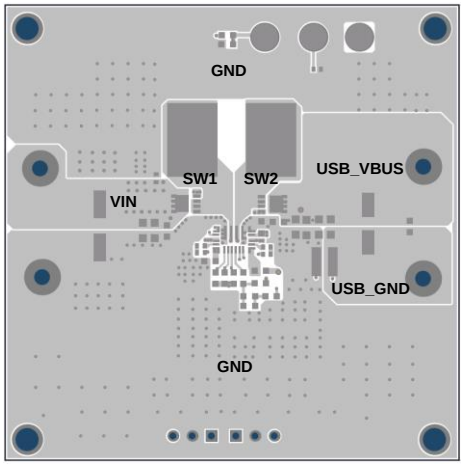
Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 11 and the follow the guidelines below:

Efficient PCB layout is critical for standard operation and thermal dissipation. Refer to Figure 12 and the PCB layout guide lines below to ensure an effective layout design:

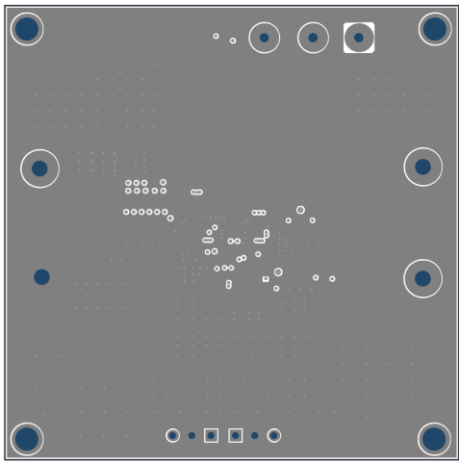
1. For the buck bridge, place the input power loop including the input filter capacitor (CIN), the power MOSFET SWA and SW1 node as close as possible.
2. For the boost bridge, place the output power loop including the output filter capacitor (COUT), the power MOSFET SWD, and SW2 node as close as possible.
3. Use short, direct, and wide traces to connect OUT.
4. Add vias to GND after the output filter if needed.
5. Use a large copper plane for PGND, and add multiple vias to improve thermal dissipation.
6. Connect AGND to PGND.
7. To improve EMI performance, place two ceramic input decoupling capacitors as close as possible to SWA and SWD drain and PGND.
8. Place the input filter at the bottom layer for better EMI performance.
9. Place the VCC decoupling capacitor as close as possible to VCC.
10. The output current-sense traces (ISEN+, ISEN-) must use Kelvin connection.
11. The switching nodes of BST1/2 capacitors must be kelvin connected to SW1 and SW2 pins with wide PCB trace.
12. Kelvin connect MP4247 VIN pin to SWA drain with wide PCB trace.

Notes:

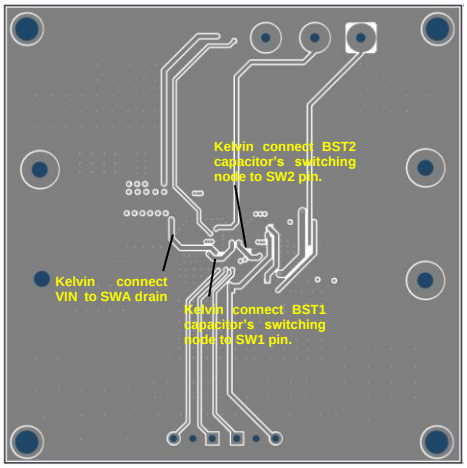
11) The recommended layout is based on the Typical Application Circuit section (see Figure 12 on page 38).



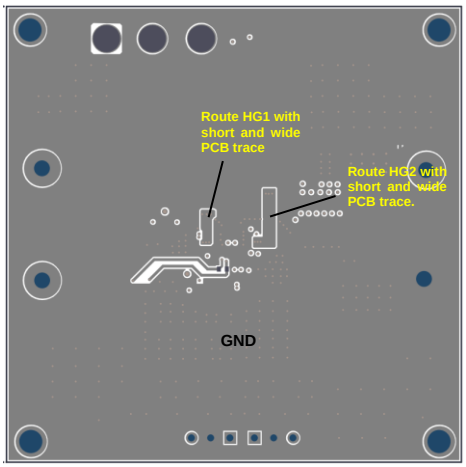
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

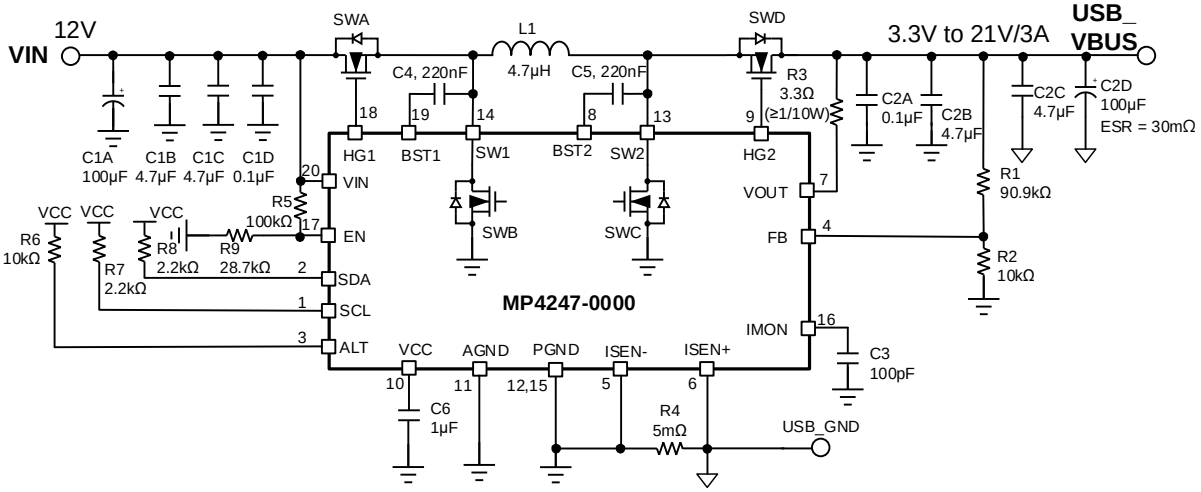


Figure 12: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 3.3V to 21V/3A USB PD Application)

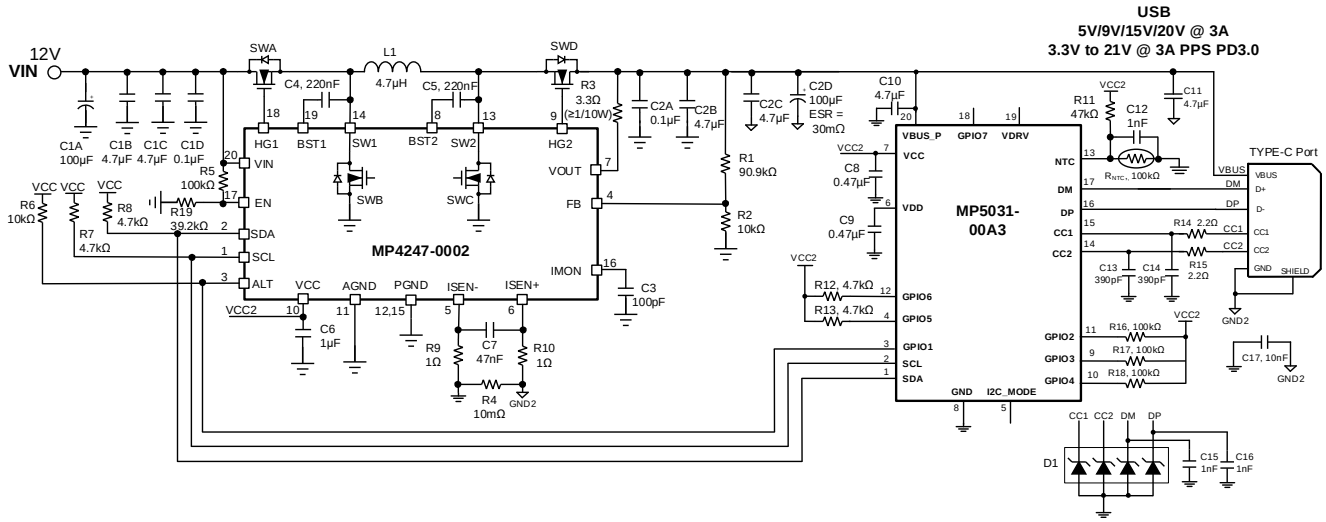


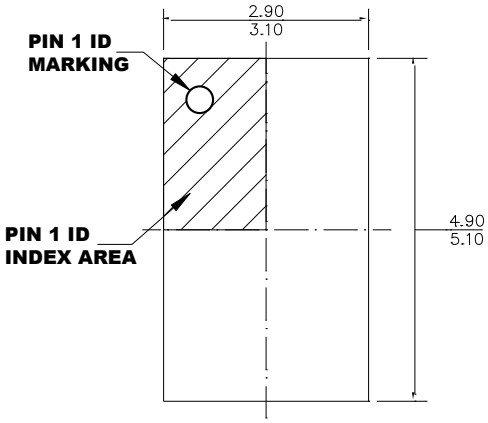
Figure 13: Typical Application Circuit (MP4247 and MP5031 for 60W PD Application)

MP4247GQV-0000 CONFIGURATION TABLE

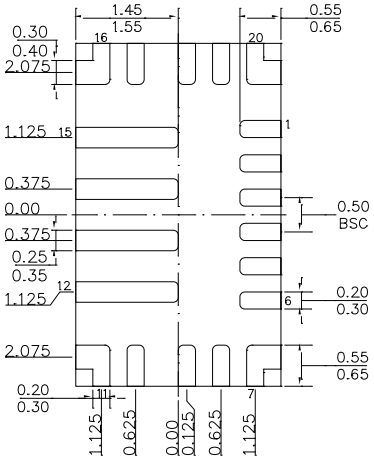
OTP Items	Description	Value
OPERATION	Sets the MP4247 on/off state.	1: On
VOUT_VOLTAGE (V)	Sets V_{OUT}.	5V
DITHER_ENABLE	Enables frequency spread spectrum.	0: Disabled (default)
FREQ	Sets f_{SW}.	01: 420kHz (default)
SWA_FET_RON	Sets the external switch SWA's on resistance under $5V_{GS}$.	01: 10mΩ
OUTPUT_OVP_EN	Enables output over-voltage protection (OVP).	1: Enabled (default)
OUTPUT_DISCHARGE_EN	Enables the output discharge function when V_{IN}, EN, or the I²C is off.	1: Enabled (default)
PFM/PWM_MODE	Selects auto-PFM/PWM or forced PWM.	1: Forced PWM (default)
LDC_DISABLE	Enables line drop compensation.	0: Enable line drop compensation (default)
CURRENT_LIMIT	Sets the output current limit.	5.4A
LINE_DROP_COMPENSATION_GAIN	Sets the V_{OUT} compensation value vs. the load current.	00: No compensation (default)
SWITCHING_CURRENT_LIMIT	Sets the SWB valley current limit and SWC peak current limit.	10: 15A SWC peak current limit, 13A SWB valley current (default)
RSENSE	Selects the R_{SENSE} value.	0: 5mΩ (default)
SLEW_RATE_RISE	Sets the V_{REF} rising slew rate. (V_{OUT} slew rate = V_{REF} slew rate x feedback ratio. Where the feedback ratio = 10.)	01: 0.16mV/μs (default)
SLEW_RATE_FALL	Sets the V_{REF} falling slew rate. (V_{OUT} slew rate = V_{REF} slew rate x feedback ratio. Where the feedback ratio = 10.)	01: 0.04mV/μs (default)
FREQ_MODE	Sets the frequency mode in buck-boost mode.	0: Reduce frequency to half of that in buck and boost mode (default)
CC blank time	Set the blank time before enters CC mode	00: 320μs
SW2_EDGE	Selects the SW2 rising and falling speed.	1: Faster (default)
Absolute OVP	select absolute OVP thresold	25.5V
I2C_ADDRESS	Sets the I²C slave address.	00111: 07
VOUT_MSK	Masks the ALT pin indication.	1: Masked
IOUT/POUT_MSK		0: No mask
RESERVED_MSK		1: Masked
TEMP_MSK		1: Masked
PG_STATUS#_MSK		1: Masked
PG_ALT_EDGE_MSK		1: Masked
RESERVED_MSK		1: Masked
UNKNOWN_MSK		1: Masked

PACKAGE INFORMATION

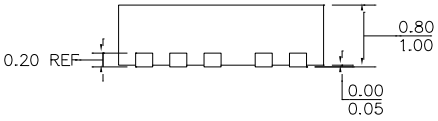
QFN-20 (3mmx5mm)



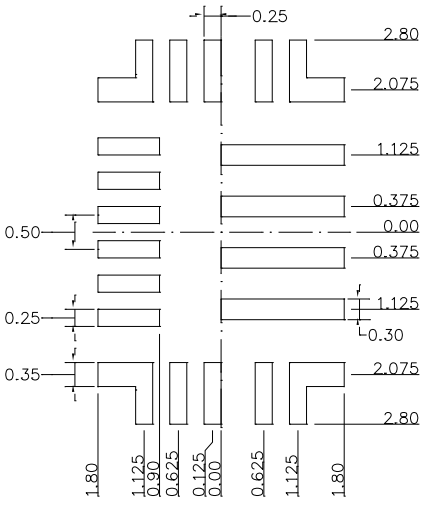
TOP VIEW



BOTTOM VIEW



SIDE VIEW

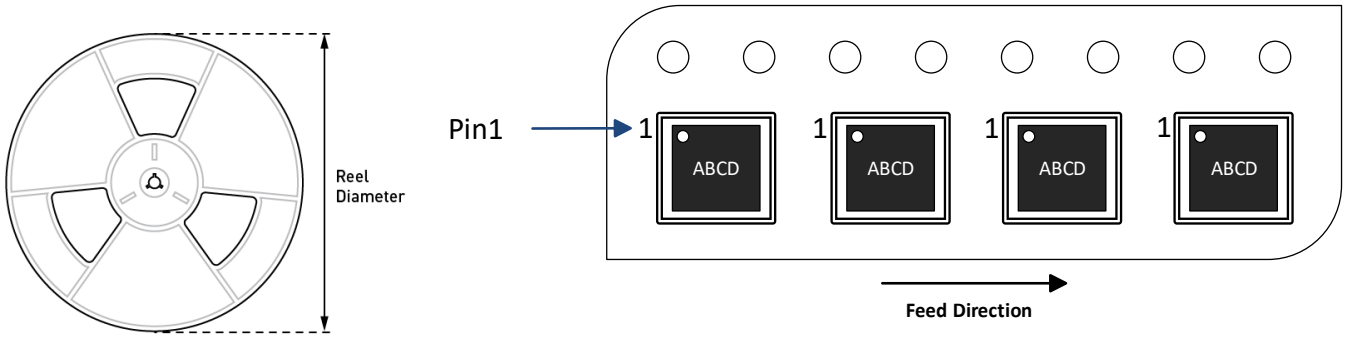


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch	Trailer Leader/ Reel
MP4247GQV-0000-Z	QFN-20 (3mmx5mm)	5000	N/A	N/A	13in	12mm	8mm	125&125
MP4247GQV-0002-Z								
MP4247GQV-0011-Z								
MP4247GQV-xxxx-Z								

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/20/2022	Initial Release	-