MP4078

Primary-Side Control, CV Output, Single-Stage Offline Controller with Active PFC

DESCRIPTION

The MP4078 is an single-stage offline controller with active power factor correction (PFC) for constant voltage output applications. The device implements primary-side regulation (PSR) control without requiring a secondary feedback circuit or optocoupler for flyback applications. It is also available for non-isolated topologies (e.g. buck-boost).

The device achieves ultra-low standby power consumption. Its pulse frequency modulation (PFM) implements a minimum operating frequency under no-load conditions. The MP4078 works in discontinuous conduction mode (DCM) with valley switching for improved efficiency performance.

The MP4078 operates in constant-on-time (COT) mode to achieve a high power factor across the universal input. It adopts a cascode MOSFET technique to achieve fast start-up with few external components.

The MP4078 integrates multiple protection features that greatly enhance system reliability and safety, including output over-voltage protection (OVP), output short-circuit protection (SCP), primary-side over-current protection (OCP), and over-temperature protection (OTP).

The MP4078 is available in an SOIC-8 package.

FEATURES

- Primary-Side Control with Simple Design and Minimal External Components
- Ultra-Low No-Load Power Consumption, Typically below 50mW with 230V_{AC}
- Good Performance on PF and THD
- Fast Transient Response
- Fast Start-Up
- Novel Control Scheme with Continuous Peak Current Limitation
- Primary-Side Over-Current Protection (OCP)
- Output Over-Voltage Protection (OVP)
- Output Short-Circuit Protection (SCP)
- Brownout Protection
- Thermal Shutdown
- Available in an SOIC-8 Package

APPLICATIONS

- Smart LED Lighting
- Front-End Pre-Regulators

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TYPICAL APPLICATION CIRCUIT

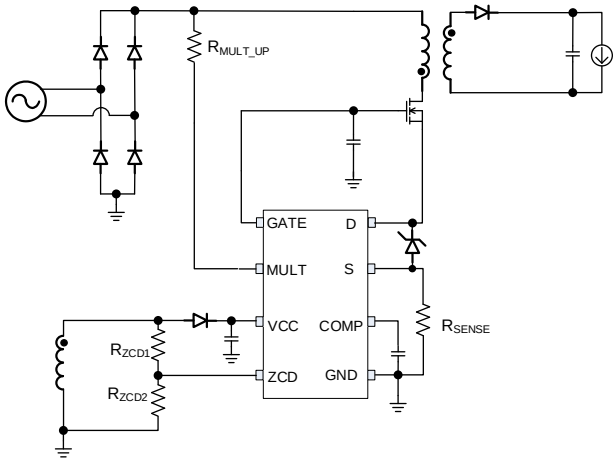

Figure 1: Isolated Flyback Application

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4078GS	SOIC-8	*See Below*	2

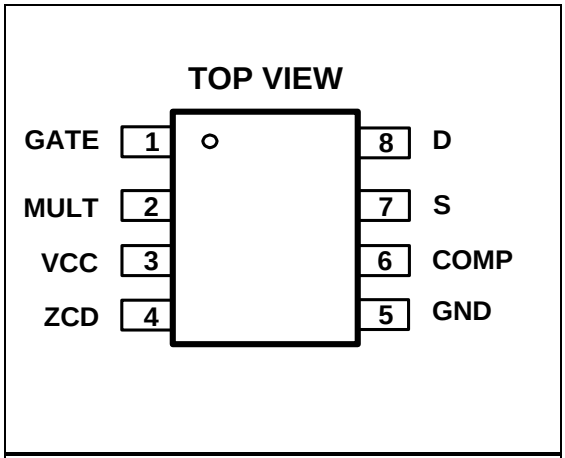
* For Tape & Reel, add suffix –Z (e.g. MP4078GS–Z).

TOP MARKING

MP4078
LLLLLLLL
MPSYWW

MP4078: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



SOIC-8

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PIN FUNCTIONS

Pin #	Name	Description
1	GATE	**Gate driver output for external MOSFET**. The GATE pin is only used in the cascode architecture. For a stable voltage, connect a ceramic capacitor (e.g. 0.47μF) from this pin to ground.
2	MULT	**Rectified input sensing with multiple functions**. Connect MULT to the rectified input with pull-up resistors. The MULT pin can change GATE before the MP4078 turns on. Once the device turns on, this pin is pulled down internally and forms a resistor divider to detect the peak rectified input voltage.
3	VCC	**Power supply input**. Place a bypass capacitor between VCC and GND, as close to the device as possible.
4	ZCD	**Zero-current detection with multiple functions**. The ZCD pin provides output voltage sensing for primary regulation. It is also used for zero-current detection, and can be configured to set the maximum operating frequency.
5	GND	**Ground**. The current returns for both the control signal and the gate drive signal.
6	COMP	**Loop compensation**. The COMP pin provides loop compensation and the output of the feedback error amplifier. Connect a compensation network between COMP and GND.
7	S	**Source of internal low-side main MOSFET**. Place a resistor between S and GND to sense the peak primary current.
8	D	**Drain of internal low-side main MOSFET**. Connect D to the source of the external cascode MOSFET.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{CC})…… ...-0.3V to +28V
GATE…….....-0.3V to +28V
GATE max sink current...……5mA
MULT…….....-0.3V to +28V
MULT max sink current……2mA
ZCD...……-0.7V to +6.5V
ZCD max source current……-1mA
Low-side MOSFET drain-to-source voltage
……..-0.7V to +35V
All other pins ...……-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8……..1.3W
Junction temperature ...……150°C
Lead temperature ……260°C
Storage temperature..……-65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±1800V
Charged device model (CDM).....±2000V

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) .. ……8.4V to 25V
Operating junction temp (T_J) …. -40ºC to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8……..…….....96.....45....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +125°C, min and max are guaranteed by characterization, typically tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Operating range	V_{CC}	After turn-on	8.4		25	V
V_{CC} upper level: internal charging circuit stops and the IC turns on	V_{CCH}	V_{CC} rising	9.9	10.5	11.1	V
V_{CC} lower level: internal charging circuit starts	V_{CCL}	V_{CC} falling	7.4	7.9	8.4	V
V_{CC} hysteresis	V_{CC_HYS}		2.2	2.6	2.9	V
Supply Current						
Operating current	I_{CC}	V_{COMP} = 0.3V		180	300	µA
		V_{COMP} = 3V		300	400	µA
V_{CC} charging current from the D pin	I_{D_CHARGE}	V_D = 16V, V_{CC} = 9.8V	3	5	7.4	mA
Operating current under a fault condition	I_{FAULT}	IC latch off, V_{CC} = 15V	200	360	500	µA
GATE						
GATE clamp voltage	V_{GATE_CLAMP}	I_{GATE} = 2mA	17	18.2	19.4	V
MULT						
MULT leakage current	$I_{MULT_LEAKAGE}$	V_{MULT} = 15V		10	500	nA
MULT pull-down resistor	R_{MULT}		28.5	30	32.5	kΩ
MULT detection time delay	t_{MULT_DELAY}			11	19.8	ms
Brown-in threshold	V_{MULT_BI}		280	320	350	mV
Brownout threshold	V_{MULT_BO}		180	210	240	mV
Brownout hysteresis	$V_{MULT_BO_HYS}$		86	110	130	mV
Brownout detection time	t_{MULT_BO}		19	24	36	ms
Error Amplifier						
Transconductance (5)	G_{EA}			100		µA/V
COMP higher clamp voltage	V_{COMPH}		4.07	4.25	4.39	V
COMP lower clamp voltage	V_{COMPL}			0	50	mV
Maximum source current	I_{COMP+}			730	1200	µA
Maximum sink current	I_{COMP-}			900	1350	µA
COMP voltage vs. V_{CS_MAX}	V_{COMP_FULL}		2.7	2.85	3.01	V
COMP voltage vs. V_{CS_MIN}	V_{COMP_MIN}		0.8	0.9	1	V
COMP voltage vs. on-time increasing (6)	V_{COMP_HALF}			2.2		V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to +125°C, min and max are guaranteed by characterization, typically tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Sense Comparator						
Leading-edge blanking time	t_{LEB}		460	620	810	ns
Leading-edge blanking time for OCP	t_{LEB_OCP}		340	430	660	ns
OCP threshold	V_{CS_OCP}		1.9	2	2.1	V
Maximum current limit	V_{CS_MAX}		0.72	0.88	0.98	V
Minimum current limit	V_{CS_MIN}		0.1	0.17	0.21	V
Zero-Current Detection (ZCD) and Feedback						
ZCD threshold voltage	V_{ZCD_TH}	V_{ZCD} falling	79	100	112	mV
ZCD hysteresis	V_{ZCD_HYS}		88	105	124	mV
ZCD sensing delay time	t_{ZCD_DELAY}	After shutdown, V_{CS} > 0.3V	1.3	1.79	2.5	µs
		After shutdown, V_{CS} ≤ 0.3V	0.9	1.16	1.75	µs
ZCD turn-on delay time (6)	t_{ZCD_ON}	After ZCD falling detected		300		ns
Minimum off time (6)	t_{OFF_MIN}			6.5		µs
Maximum working cycle (6)	t_{CYCLE_MAX}			6		ms
Minimum working cycle	t_{CYCLE_MIN}	R_{ZCD1} // R_{ZCD2} > 8.8kΩ	9.6	11	12.7	µs
		2.8kΩ < R_{ZCD1} // R_{ZCD2} < 3.3kΩ	14	15.3	17.5	
Reference voltage	V_{REF}		2.41	2.49	2.55	V
FB transient low trigger threshold	V_{FB_LOW}		1.93	2.08	2.23	V
FB transient low recovery threshold	$V_{FB_LOW_REC}$		2.12	2.23	2.44	V
FB transient low hysteresis (6)	$V_{FB_LOW_HYS}$	Greater than V_{FB_LOW}		0.15		V
FB transient high trigger threshold	V_{FB_HIGH}		2.67	2.87	3.06	V
FB transient high recovery threshold	$V_{FB_HIGH_REC}$		2.5	2.67	2.86	V
FB transient high hysteresis (6)	$V_{FB_HIGH_HYS}$	Lower than V_{FB_HIGH}		0.2		V
FB start-up finish threshold (5)	V_{FB_NORMAL}			2.4		V
FB start-up finish hysteresis (5)	$V_{FB_NORMAL_HYS}$			0.15		V
Over-voltage protection threshold	V_{FB_OVP}		2.84	2.96	3.1	V
Short-circuit protection threshold	V_{FB_SCP}		165	200	235	mV
Short-circuit protection duration	t_{SCP}			2.3	6	ms
Short-circuit protection duration for start-up (5)	$t_{SCP_STARTUP}$			100		ms
Starter						
Start timer period	t_{START}		40	49	70	µs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to +125°C, min and max are guaranteed by characterization, typically tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Internal Main MOSFET						
Breakdown voltage	BV_{DSS_MAIN}	V_{GS} = 0V	35			V
Drain-source on resistor	$R_{DS(ON)_MAIN}$	I_{DS} = 100mA, T_A = 25°C		265	320	mΩ
		I_{DS} = 100mA, T_A = 125°C		370	430	
		I_{DS} = 100mA, T_A = 25°C, V_{CC} = V_{CCH} + 50mV		270	330	
		I_{DS} = 100mA, T_A = 125°C, V_{CC} = V_{CCH} + 50mV		380	440	
Leakage current on the D pin	$I_{LEAKAGE_D}$				1	μA
Internal OVP Pull-Up MOSFET						
Breakdown voltage	$BV_{DSS_D_VCC}$	V_{GS} = 0V	28			V
Drain-source on resistor	$R_{DS(ON)_D_VCC}$	I_{DS} = 50mA, T_A = 25°C		225	300	Ω
Thermal Shutdown						
Thermal shutdown threshold (5)	T_{TSD}			160		°C
Thermal shutdown hysteresis (5)	T_{TSD_HYS}			60		°C

Notes:

5) Guaranteed by design.
6) Guaranteed by characterization.

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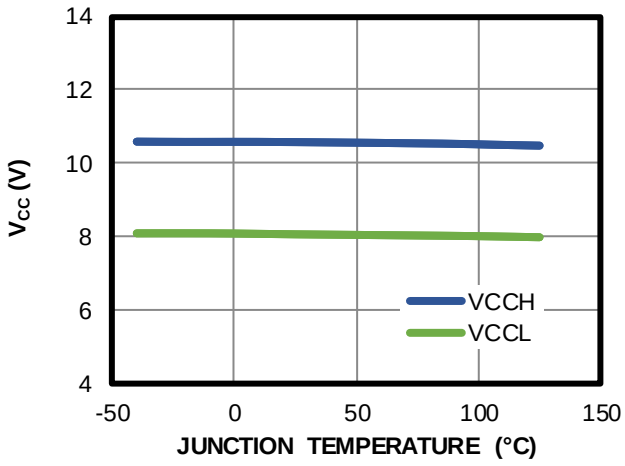
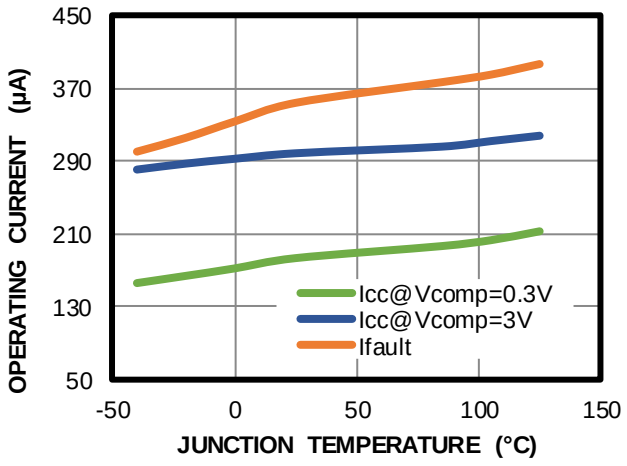
TYPICAL CHARACTERISTICS

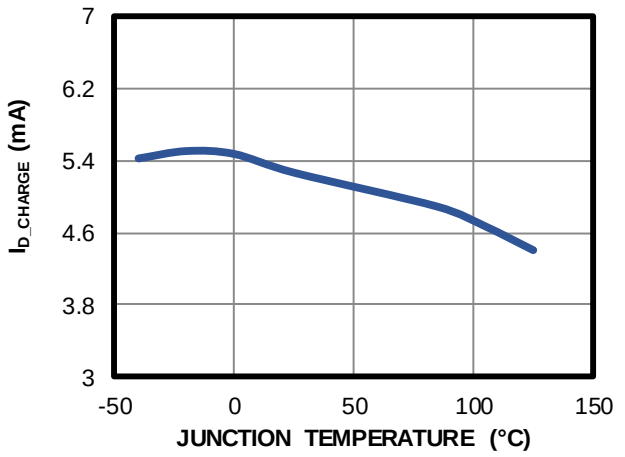
V_{CC} vs. Junction Temperature



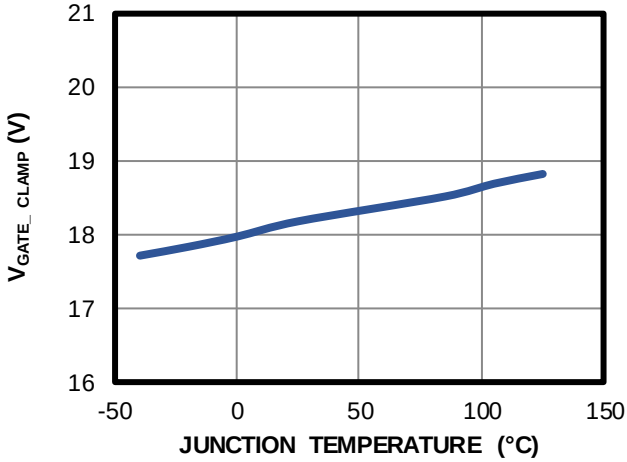
Operating Current vs. Junction Temperature



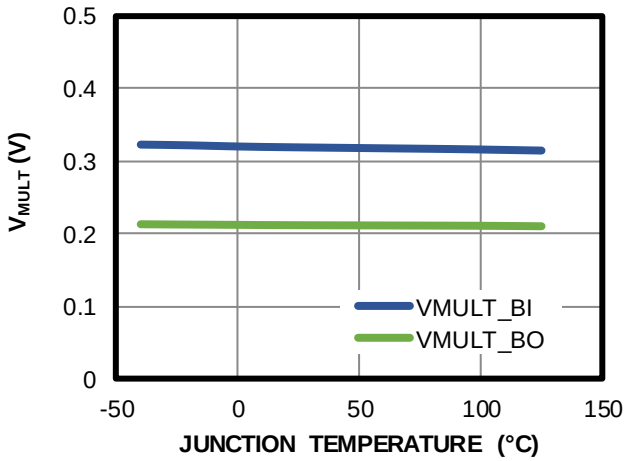
VCC Charging Current from the D Pin vs. Junction Temperature



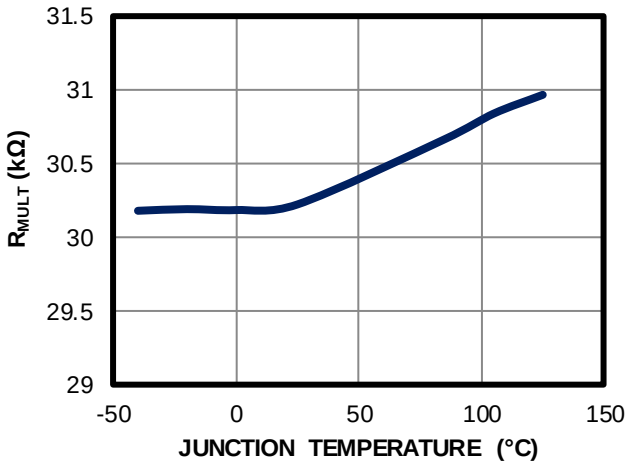
GATE Clamp Voltage vs. Junction Temperature



Brown-In/Brownout Threshold vs. Junction Temperature



MULT Pull-Down Resistor vs. Junction Temperature



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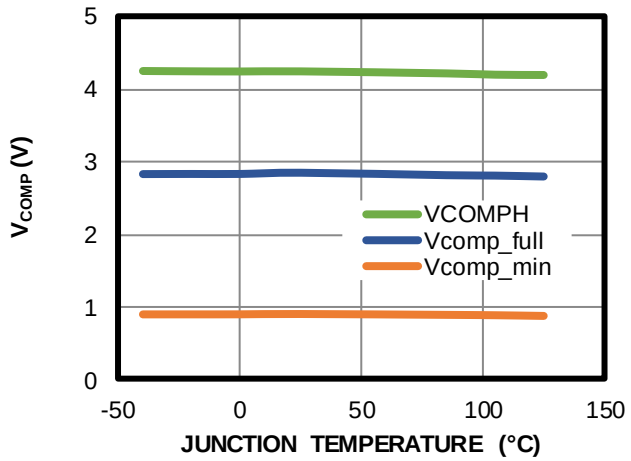
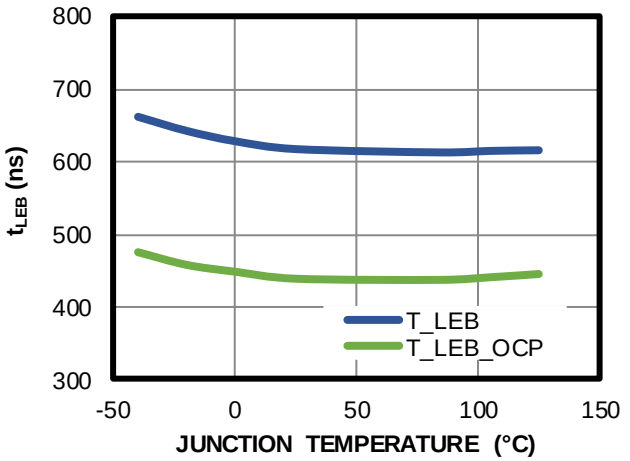
TYPICAL CHARACTERISTICS *(continued)*

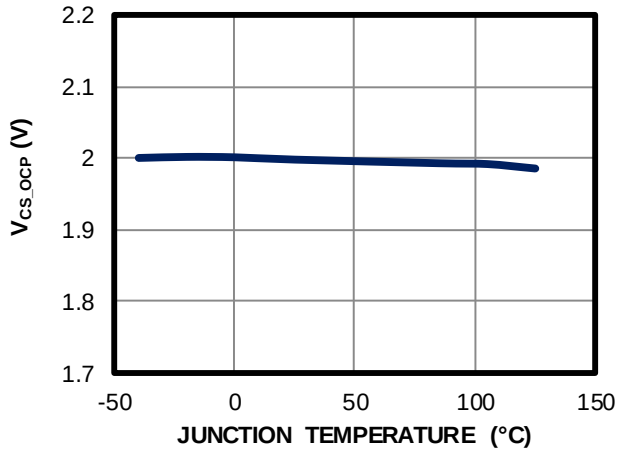
COMP Voltage vs. Junction Temperature



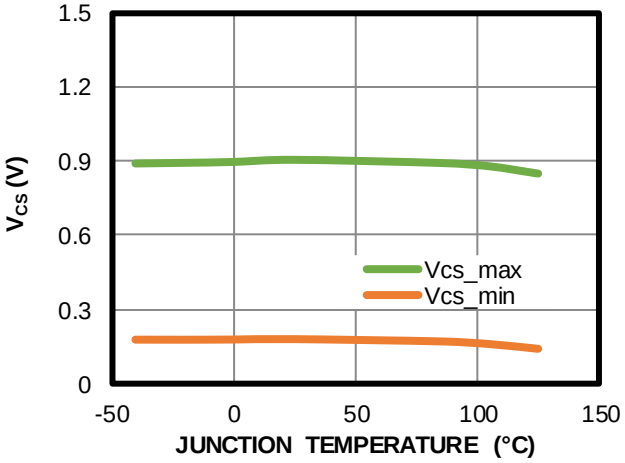
Leading-Edge Blanking Time vs. Junction Temperature



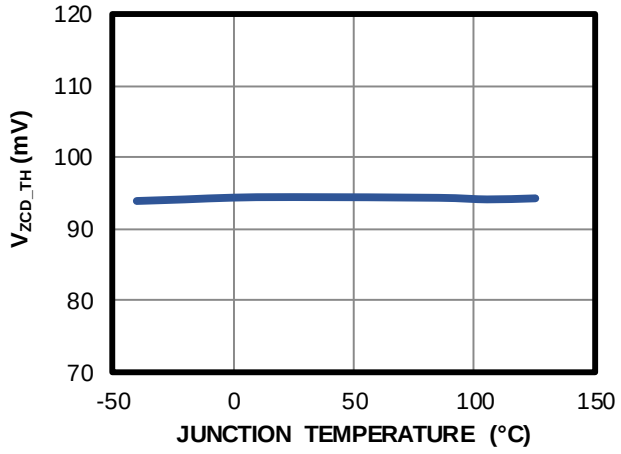
OCP Threshold vs. Junction Temperature



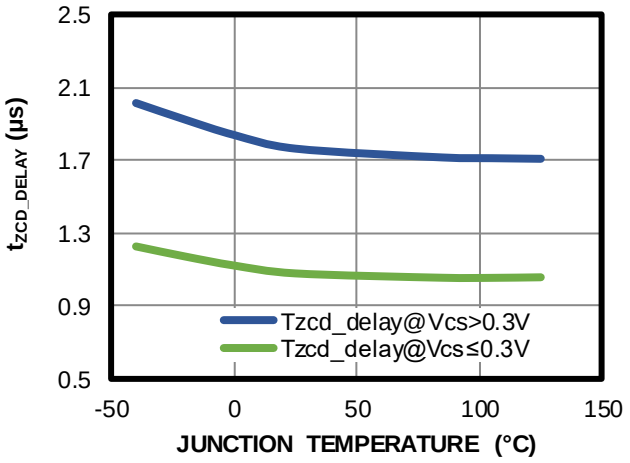
Current Limit Threshold vs. Junction Temperature



ZCD Threshold vs. Junction Temperature



ZCD Sensing Delay Time vs. Junction Temperature



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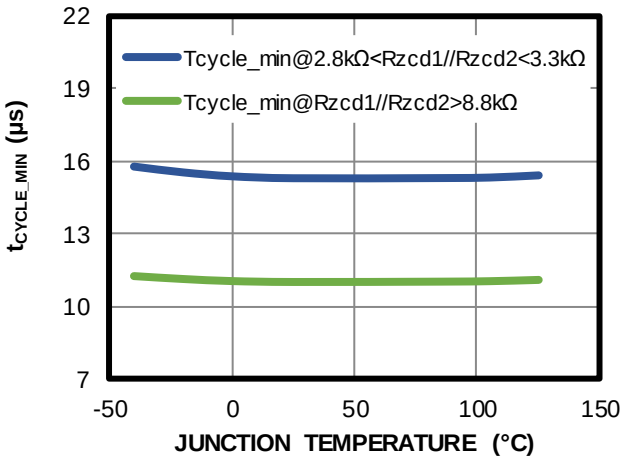
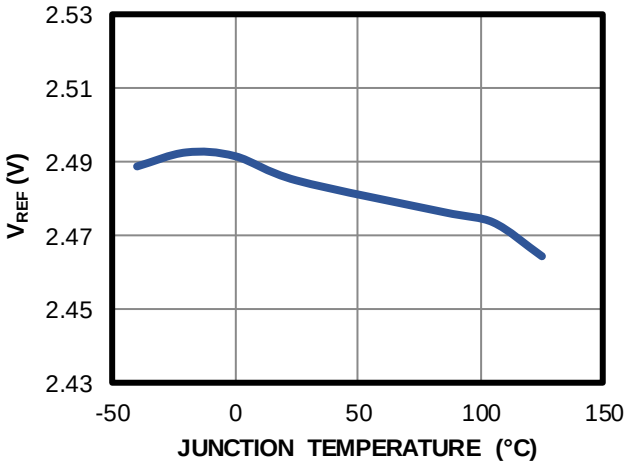
TYPICAL CHARACTERISTICS *(continued)*

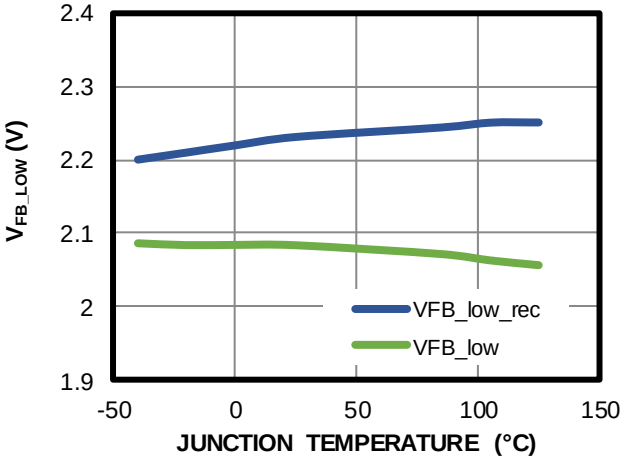
Minimum Working Cycle vs. Junction Temperature



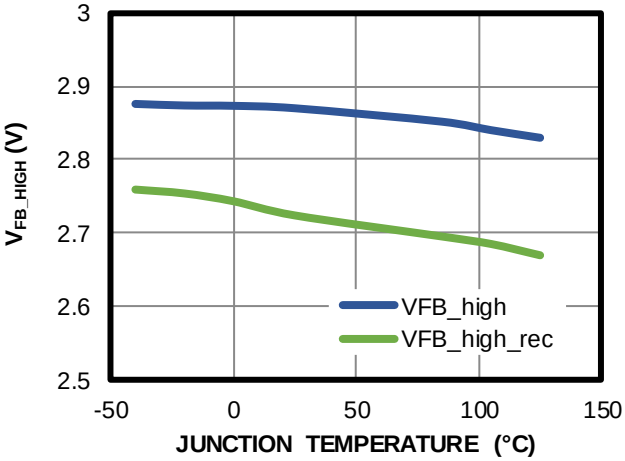
Reference Voltage vs. Junction Temperature



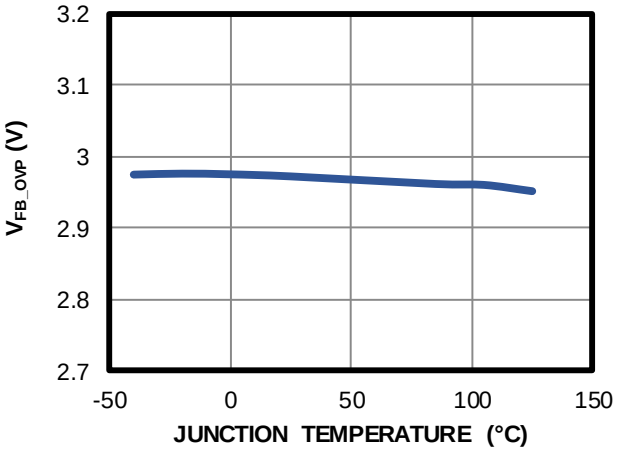
FB Transient Low Threshold vs. Junction Temperature



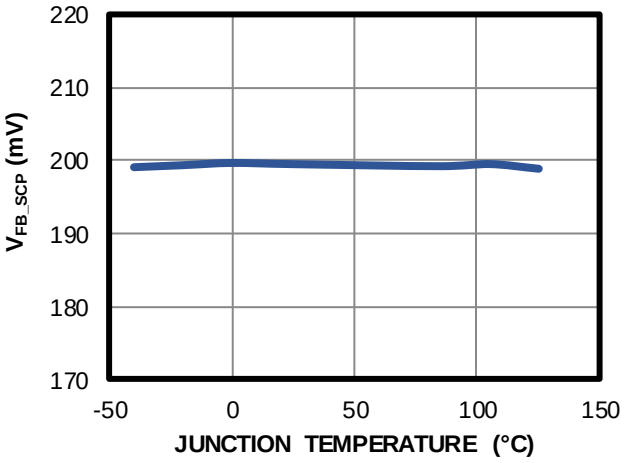
FB Transient High Threshold vs. Junction Temperature



OVP Threshold vs. Junction Temperature



SCP Threshold vs. Junction Temperature



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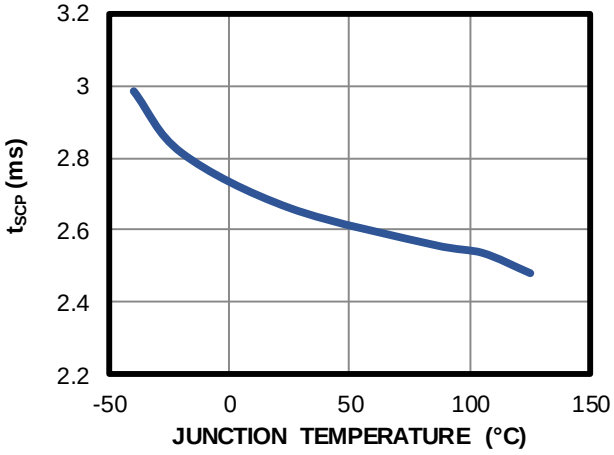
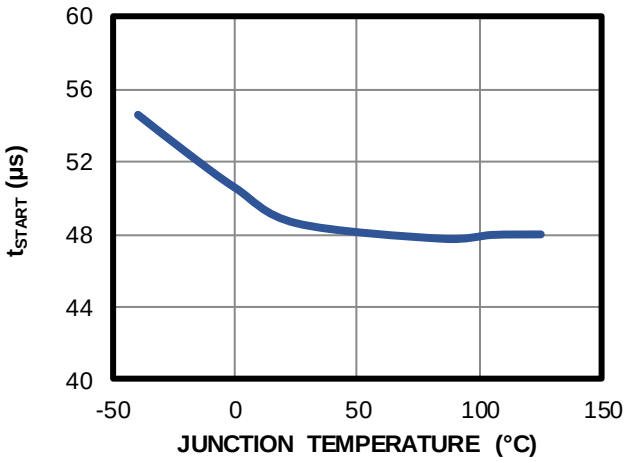
TYPICAL CHARACTERISTICS *(continued)*

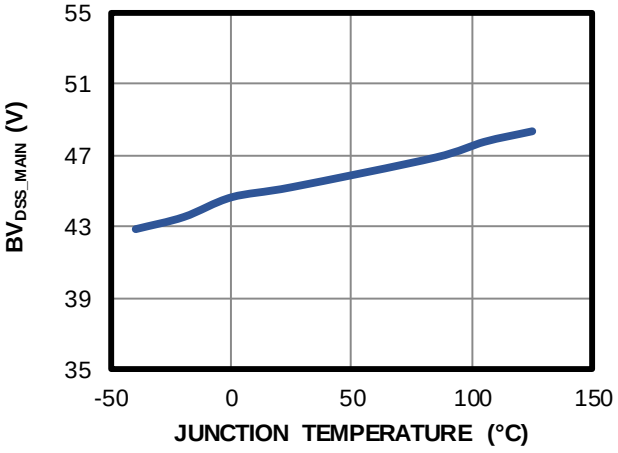
SCP Duration vs. Junction Temperature



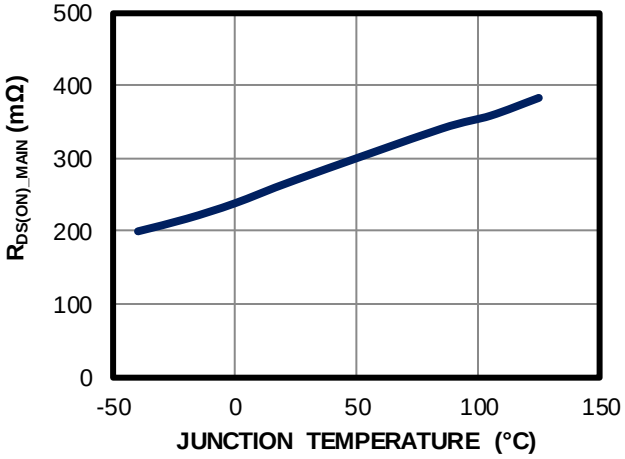
Start Timer Period vs. Junction Temperature



Internal Main MOSFET Breakdown Voltage vs. Junction Temperature



Internal Main MOSFET On Resistor vs. Junction Temperature



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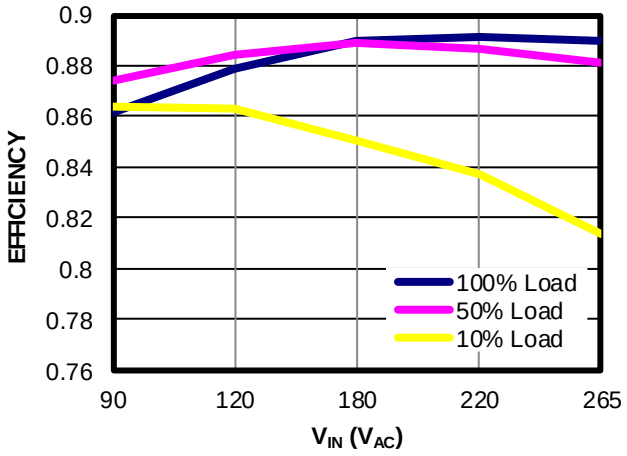
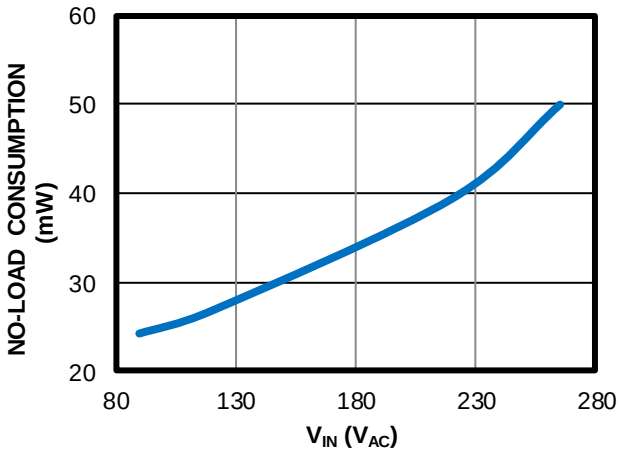
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the EV4078-S-00A evaluation board, V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 50V, I_{OUT} = 600mA, T_A = 25°C, unless otherwise noted.

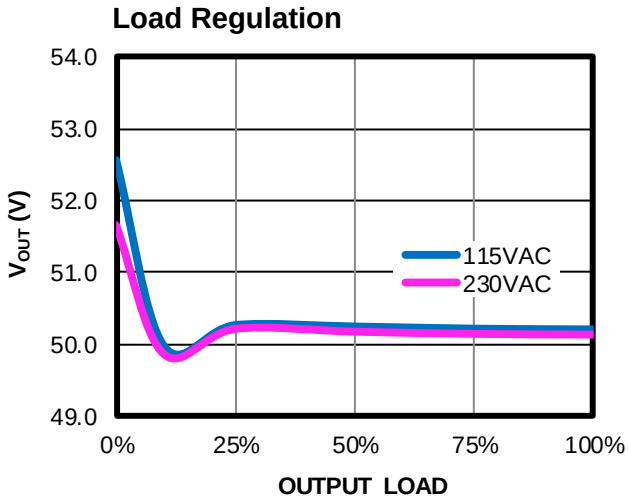
Efficiency



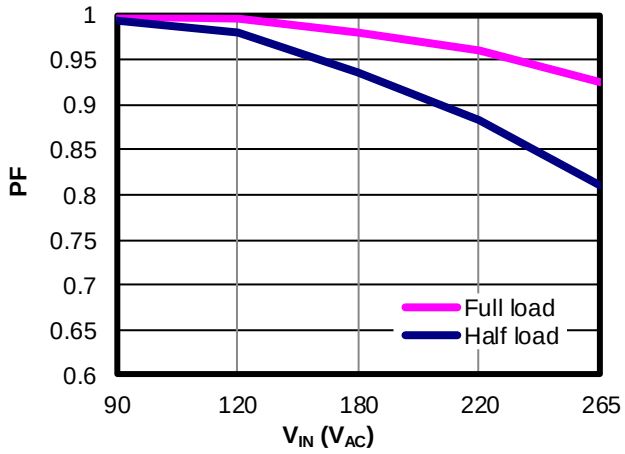
No-Load Consumption



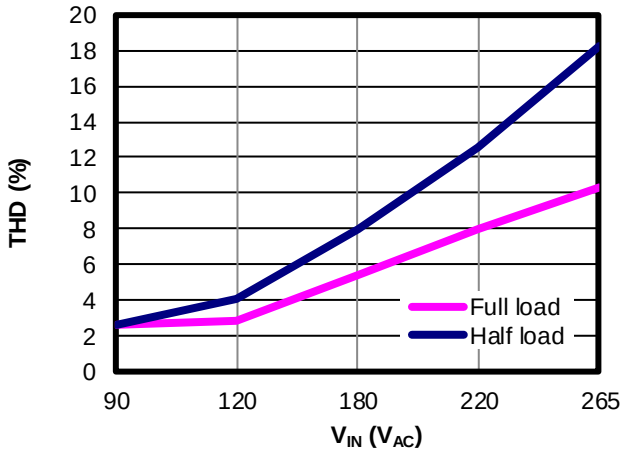
Load Regulation



PF vs. V_{IN}



THD vs. V_{IN}



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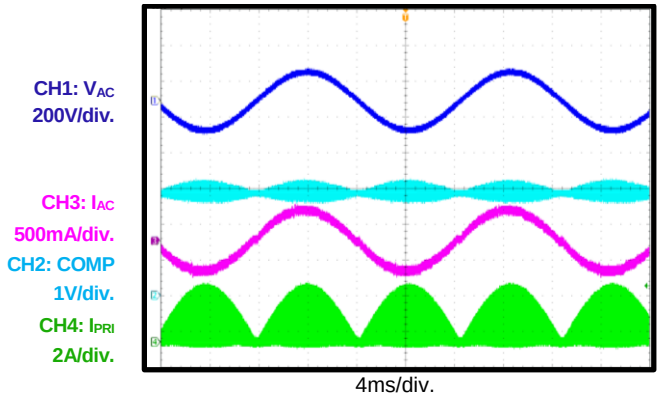
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the EV4078-S-00A evaluation board, V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 50V, I_{OUT} = 600mA, T_A = 25°C, unless otherwise noted.

Input Voltage and Current

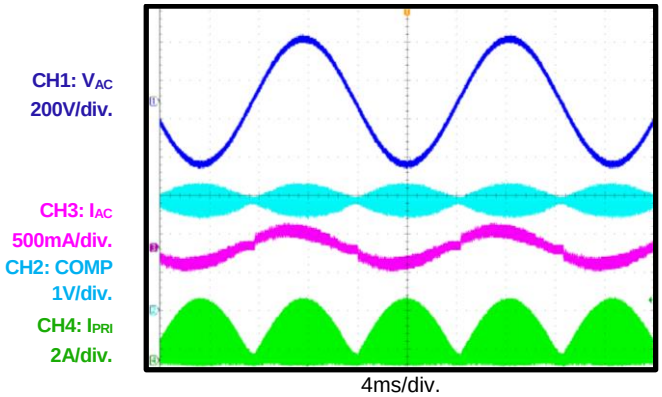
115V_{AC}, full load



4ms/div.

Input Voltage and Current

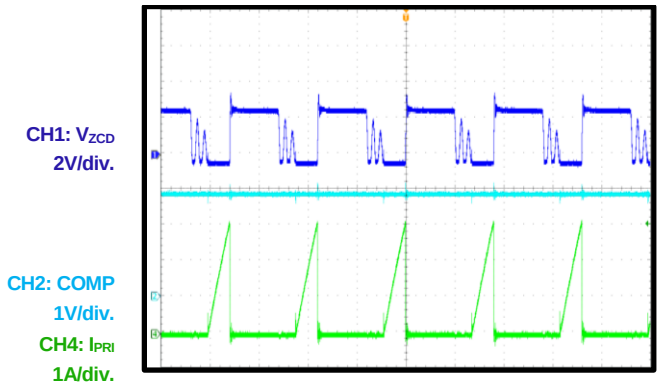
230V_{AC}, dull load



4ms/div.

Steady State

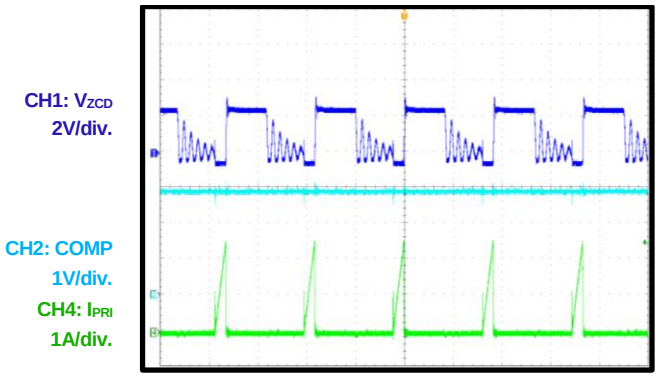
115V_{AC}, full load



10µs/div.

Steady State

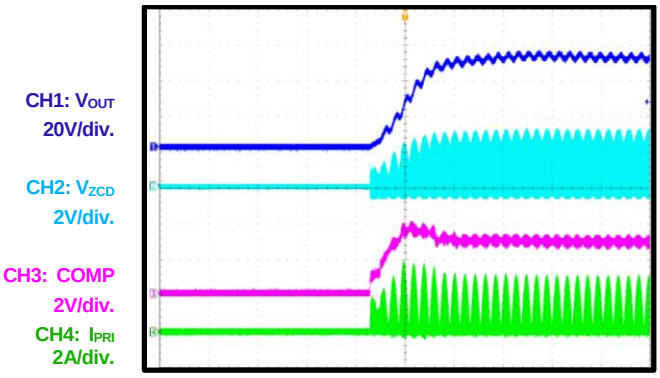
230V_{AC}, full load



10µs/div.

Start-Up

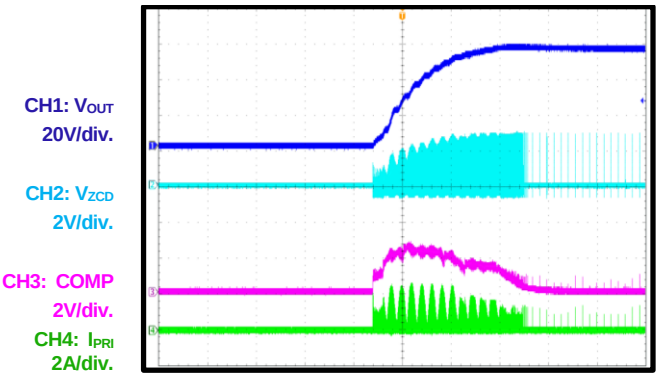
230V_{AC}, full load



40ms/div.

Start-Up

230V_{AC}, no load



40ms/div.

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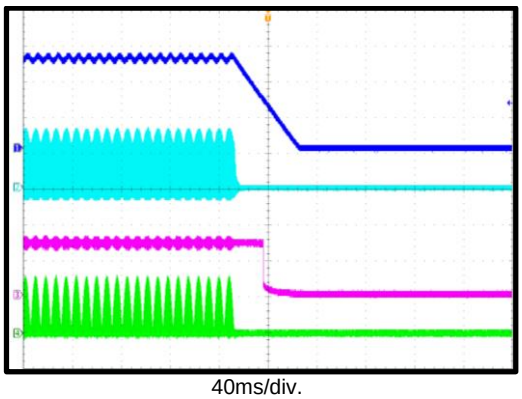
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the EV4078-S-00A evaluation board, V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 50V, I_{OUT} = 600mA, T_A = 25°C, unless otherwise noted.

Shutdown

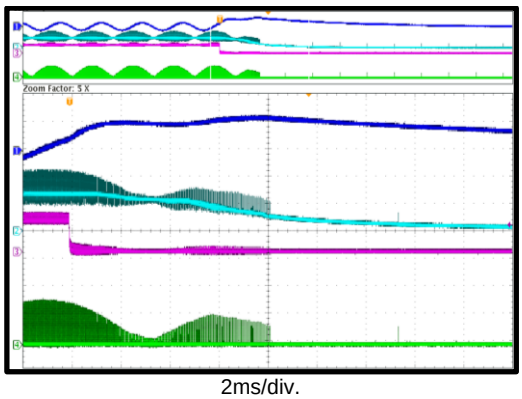
230V_{AC}, full load



40ms/div.

Transient High Triggering

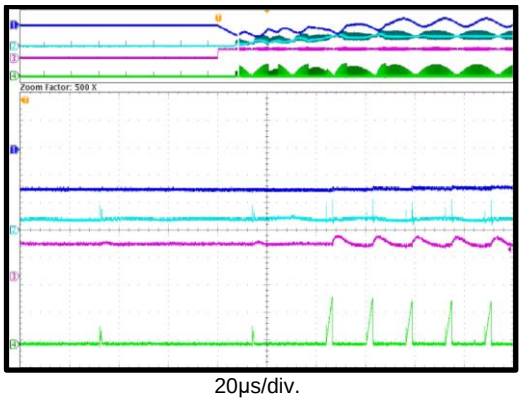
230V_{AC}, full load to no load



2ms/div.

Transient High Triggering

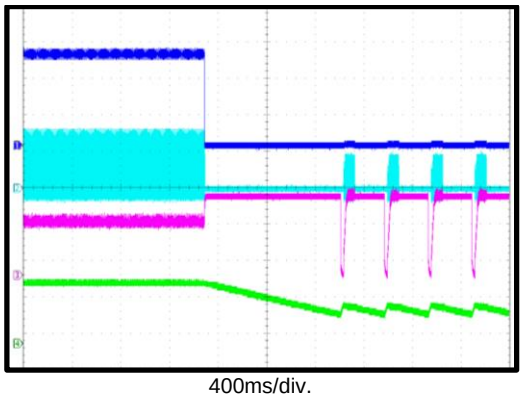
230V_{AC}, full load to no load



20µs/div.

SCP

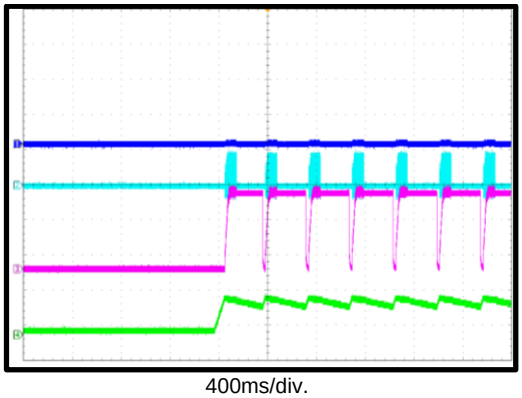
230V, full load



400ms/div.

Short then Start

230V, full load



400ms/div.

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FUNCTIONAL BLOCK DIAGRAM

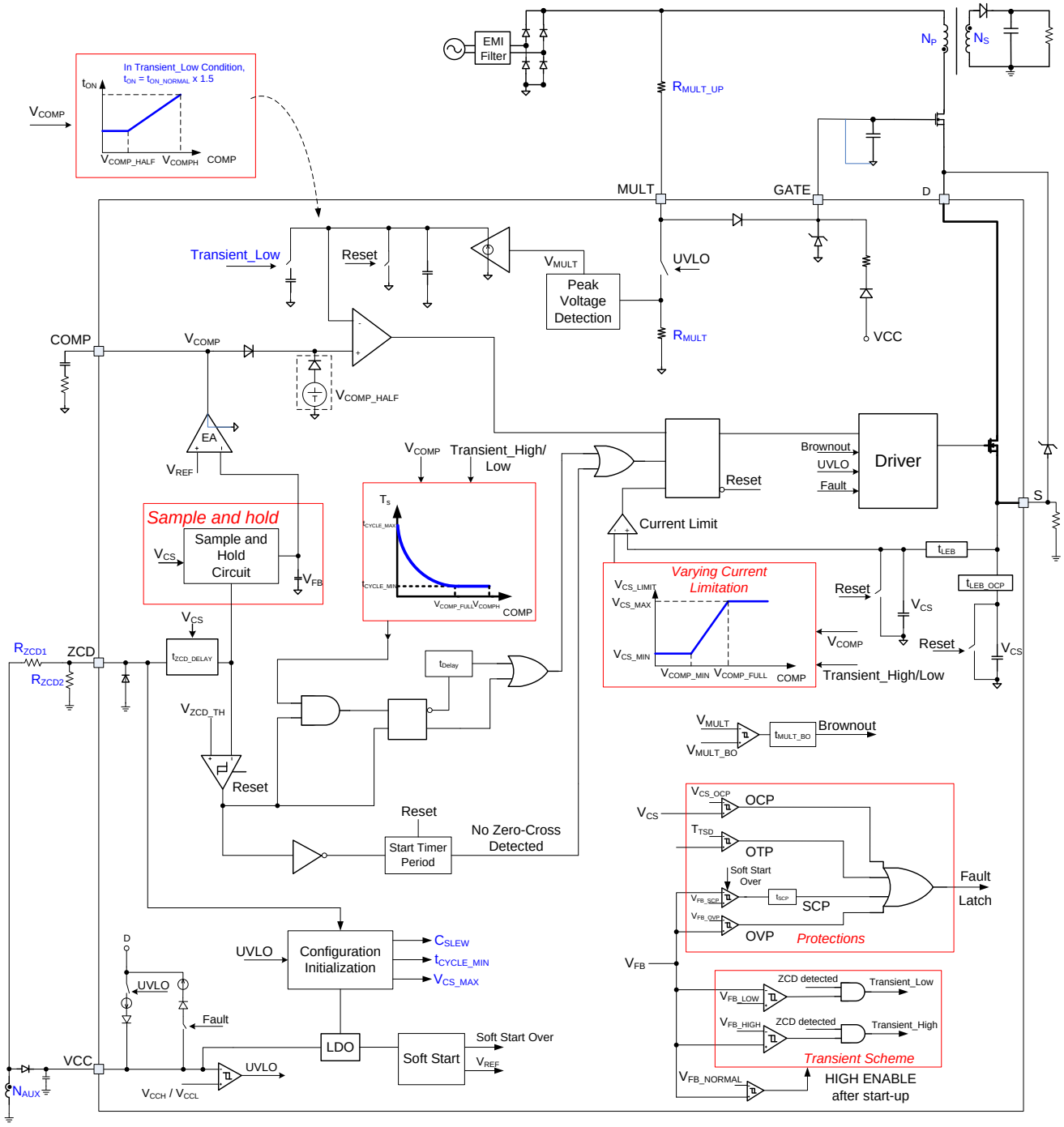

Figure 2: MP4078 Functional Block Diagram

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OPERATION

The MP4078 is a primary-side regulation (PSR) controller with power factor correction (PFC) for applications with offline, constant-voltage LED drivers or pre-regulators. The MP4078 achieves good performance with high power factor (PF), low total harmonic distortion (THD), fast transient response, and ultra-low standby power consumption. It also eliminates the cost of the optocoupler and secondary regulation circuits required in conventional flyback design applications.

Start-Up

Initially, the voltage on the GATE pin (V_{GATE}) is charged through the external pull-up resistor (R_{MULT_UP}), which is placed between the MULT pin and the rectified input voltage. When V_{GATE} reaches the gate threshold of the external MOSFET, the MP4078 uses cascode MOSFET architecture to charge the voltage on the VCC pin (V_{CC}) through a built-in current source. When V_{CC} reaches the IC turn-on threshold (V_{CCH}), the MP4078 initializes the configuration of the minimum working cycle (t_{CYCLE_MIN}) and the coefficient of the on-time generator (K_{SLEW}) (see Table 1).

Table 1: Configuration Options

	Condition	Condition
R_{ZCD1} // R_{ZCD2}	2.8kΩ to 3.3kΩ	Minimum 8.8kΩ
t_{CYCLE_MIN}	15.3μs	11μs
K_{SLEW}	9 x 10^{-7}s	4.5 x 10^{-7}s
Application Input Range (7)	Universal input (85V_{AC} to 277V_{AC})	220V_{AC} / 230V_{AC} ±20%

Note:

7) Recommended in design.

After V_{CC} reaches V_{CCH}, the MP4078 also stops charging V_{CC} internally and pulls down the MULT pin through an internal pull-down resistor (R_{MULT}). R_{MULT} and R_{MULT_UP} form a resistor divider to sense the input voltage. Once the peak voltage on the MULT pin (V_{MULT}) exceeds the brown-in threshold (V_{MULT_BI}), the MP4078 begins to switch with a soft start.

Primary-Side Regulation

Figure 3 shows a simplified flyback converter circuit.

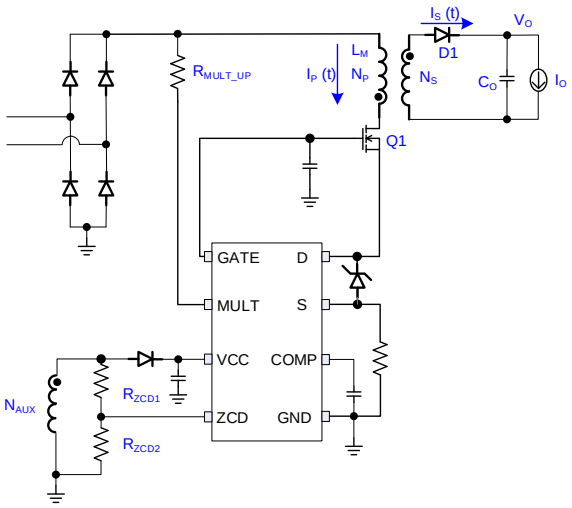

Figure 3: Flyback Converter

Figure 4 illustrates the key waveforms of the flyback converter.

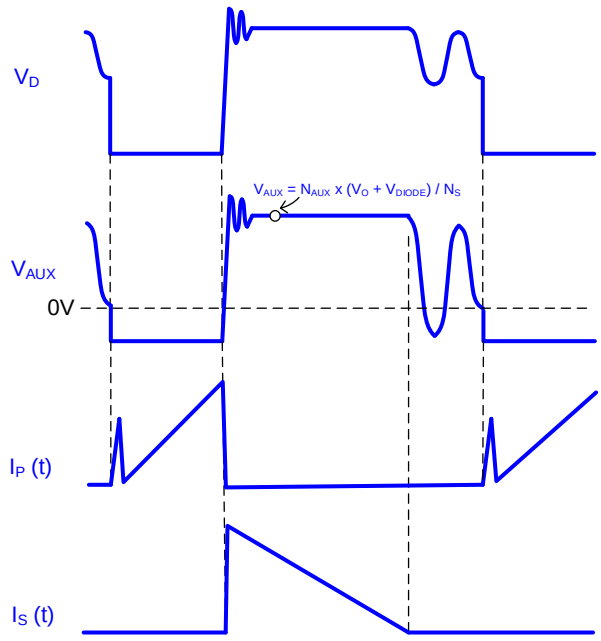

Figure 4: Key Waveforms of Flyback Converters

While the external MOSFET (Q1) turns on, the rectified input voltage applied on the primary inductor (L_M) makes the primary current increase linearly. The rectified diode (D1) is reversely biased, and the load current (I_O) is supplied by the secondary capacitor (C_O). Then Q1 turns off, D1 conducts, and the stored energy in the transformer is delivered to the output.

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To regulate the output, all information regarding the output voltage must be accurately sensed.

The plateau voltage of the auxiliary winding is proportional to the output voltage while D1 conducts, so this value can be used to indicate the output voltage. The MP4078 monitors this signal on the ZCD pin through a resistor divider.

Because the auxiliary winding voltage is not stable or constant, it requires a sample hold circuit to generate a feedback voltage (V_{FB}) that is equal to the sensed plateau voltage. V_{FB} represents the output voltage, and is regulated by the internal reference (V_{REF}). Calculate the ZCD resistor divider ratio with Equation (1):

$$V_{REF} \times \frac{R_{ZCD1} + R_{ZCD2}}{R_{ZCD2}} = (V_O + V_{DIODE}) \times \frac{N_{AUX}}{N_S} \quad (1)$$

Where R_{ZCD1} and R_{ZCD2} are external resistor dividers around the ZCD pin, V_O is the output voltage, V_{DIODE} is the forward voltage drop of the rectified diode (D1), N_{AUX} is the number of turns on the auxiliary winding for VCC, and N_S is the number of turns on the secondary winding for the output.

Because of the parasitic capacitance and inductance in circuits, switching spikes inevitably exist on the windings when Q1 turns off. This affects the sensing accuracy on the ZCD pin without any blanking time delay. It also inaccurately senses the plateau voltage with a long blanking time delay, since the D1 current drops to zero (especially under light-load conditions).

The MP4078 has an internal variable delay time for ZCD sensing (t_{ZCD_DELAY}). Its value depends on the peak voltage (V_{CS}) on the S pin (the source of the internal MOSFET), which represents the load condition. Under heavy-load conditions (V_{CS} > 0.3V), t_{ZCD_DELAY} is set to about 1.79μs. Under light-load conditions (V_{CS} ≤ 0.3V), t_{ZCD_DELAY} is adjusted to about 1.16μs.

Figure 5 shows the ZCD sensing delay time.

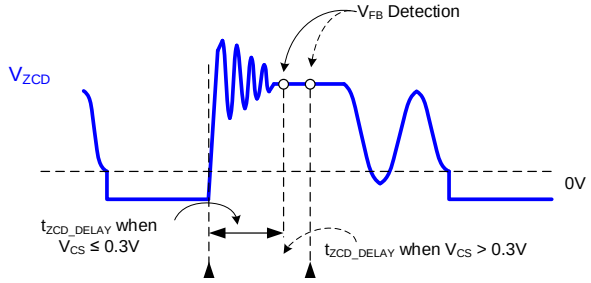

Figure 5: ZCD Sensing Delay Time

Constant-On-Time (COT) Operation

To achieve a high power factor under universal input, the MP4078 adopts constant-on-time (COT) control.

Figure 6 shows the internal on-time generation block diagram.

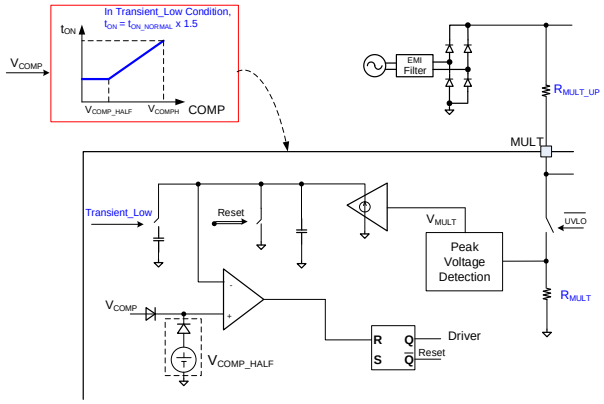

Figure 6: On-Time Generation

In normal operation, the peak voltage on the MULT pin (V_{MULT}) represents the input voltage, which is converted to a charge current. This current charges the slew rate capacitor once the external MOSFET turns on and makes the voltage on the capacitor increase linearly. The voltage on the slew rate capacitor is compared to the output of the error amplifier (V_{COMP}) for feedback to determine the turn-off time for both the internal and external MOSFETs. When the output load decreases, V_{COMP} drops accordingly.

As an input of the on-time generation comparator, the value is maintained at a certain voltage (V_{COMP_HALF}) when V_{COMP} drops below V_{COMP_HALF}. That means the on time does not decrease with a constant input voltage. However, it does achieve COT in a sinusoidal period with the whole output load range.

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If V_{COMP} > V_{COMP_HALF}, the on time can be calculated with Equation (2):

$$t_{ON} = \frac{K_{SLEW} \times V_{COMP}}{V_{MULT}} \quad (2)$$

If V_{COMP} ≤ V_{COMP_HALF}, the on time is fixed, and can be calculated with Equation (3):

$$t_{ON} = \frac{K_{SLEW} \times V_{COMP_HALF}}{V_{MULT}} \quad (3)$$

Where V_{MULT} is the peak voltage on the MULT pin, estimated with Equation (4):

$$V_{MULT} = \frac{\sqrt{2} \times V_{IN_rms} \times R_{MULT}}{R_{MULT} + R_{MULT_UP}} \quad (4)$$

Where V_{IN_RMS} is the effective value of the input voltage.

Unlike the variable frequency control of conventional boundary conduction mode, the MP4078 works at an approximate fixed frequency across an input sinusoidal period. The working cycle is inversely proportional to V_{COMP}, which is determined by the output load. When V_{COMP} reaches V_{COMP_FULL} according to the increasing output load, the MP4078 works at its maximum operating frequency (corresponding to the minimum working cycle, t_{CYCLE_MIN}). The MP4078 lowers its operating frequency when the output load decreases. Its maximum working cycle (t_{CYCLE_MAX}) guarantees output regulation under light-load conditions, and also initiates ultra-low, no-load power consumption.

Figure 7 shows the working cycle and turn-on time curve.

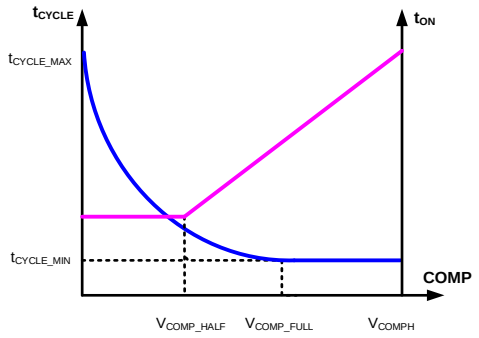

Figure 7: Working Cycle and Turn-On Time Curve

Valley Switching Mode

The MP4078's working cycle (inversely proportional to operating frequency) is determined by V_{COMP}. However, the MP4078 does not turn on the switch inflexibly when the working cycle ends. The MP4078 optimizes its turn-on logic with zero-current detection through the ZCD pin.

The MP4078 has a ZCD threshold voltage (V_{ZCD_TH}, typically 100mV). If the voltage on the ZCD pin exceeds 205mV (105mV hysteresis on V_{ZCD_TH}) then drops below V_{ZCD_TH}, the MP4078 recognizes this as a ZCD falling edge. After a working cycle ends, the MP4078 monitors the ZCD pin and turns on the switch with a delay time (t_{ZCD_ON}, typically 300ns) since a ZCD falling edge is detected. This decreases the switching loss on both the external and internal MOSFETs for high efficiency. It also guarantees discontinuous conduction mode (DCM) operation.

Figure 8 shows the valley switching.

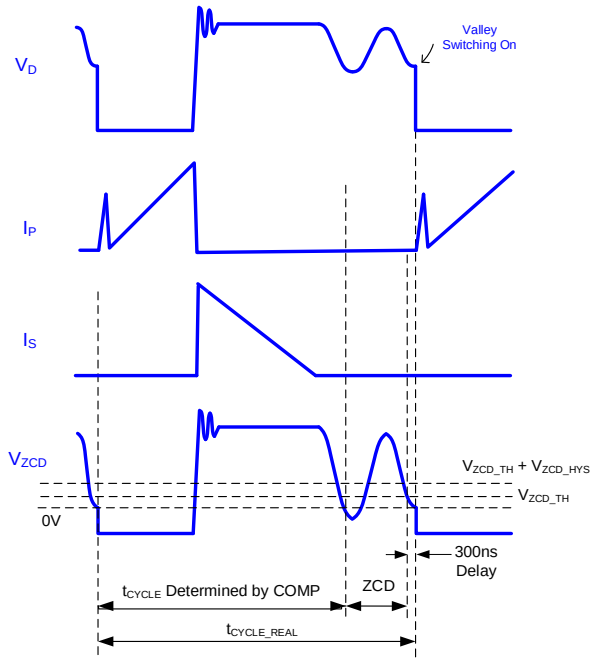

Figure 8: Valley Switching

If no ZCD falling edge is detected under particular states (e.g. start-up), the MP4078 turns on the switch via an internal timer with a fixed period (t_{START}, typically 49μs), unless a fault condition occurs.

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Adjustable Current Limitation

The MP4078 implements cycle-by-cycle current limitation through the S pin. When the voltage on the S pin (V_{CS}) reaches the internal current limit, the device immediately stops switching. Unlike a conventional scheme with a fixed current limit, the MP4078 adopts an optimized design to adjust current limitation. Under light-load conditions, the operating frequency decreases according to V_{COMP}. To reduce the audible noise influence, the current limit is kept at its minimum value (V_{CS_MIN}) when V_{COMP} drops below V_{COMP_MIN}. When the output load increases, the upper limit rises linearly and reaches its maximum value (V_{CS_MAX}) when V_{COMP} reaches V_{COMP_FULL}.

Figure 9 shows adjustable current limitation.

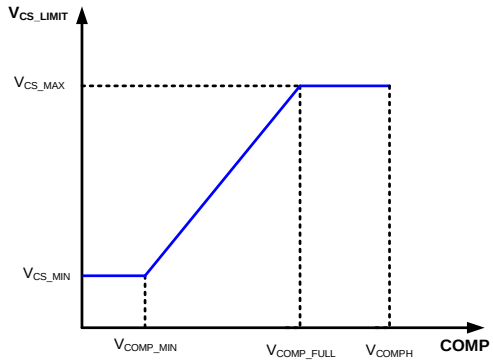

Figure 9: Adjustable Current Limitation

Over-Current Protection (OCP)

If there is an excessive short event or another unexpected condition, the primary current increases sharply out of limitation. To protect the system from damage, the MP4078 integrates independent over-current protection (OCP). If V_{CS} reaches the OCP threshold (V_{CS_OCP}), the MP4078 stops switching immediately and maintains the latch-off state. The device resets when V_{CC} falls below V_{CCL}, then rises up to V_{CCH} again.

Fast Transient Response

Due to the low bandwidth, the conventional PFC has slow responses in transient conditions. The MP4078 enhances the dynamic behavior of system through the ZCD pin. In normal operation, the device generates V_{FB} via the sensed plateau voltage on the ZCD pin. If the output voltage drops and V_{FB} falls below V_{FB_LOW}, the MP4078 forces the on time to increase by 1.5 times t_{ON} under real-time V_{COMP}. It also immediately pushes the operating frequency to its maximum value. Then the output voltage stops dropping and returns to its normal value.

If the output voltage rises and V_{FB} exceeds V_{FB_HIGH}, the MP4078 immediately lowers the on time and the operating frequency to their minimum values. Then the output voltage stops rising.

For smooth start-up, the MP4078 enables fast transient response, since the output voltage is set up and V_{FB} exceeds V_{FB_NORMAL} for the first start-up.

Output Over-Voltage Protection (OVP) and Short-Circuit Protection (SCP)

The MP4078 integrates output over-voltage protection (OVP) and short-circuit protection (SCP) to protect the system from damage. Output OVP and SCP are implemented by detecting V_{FB}. If V_{FB} exceeds the OVP threshold (V_{FB_OVP}), the MP4078 stops switching and enters latch-off mode.

If an output short circuit occurs during normal operation, V_{FB} drops according to the output voltage. If V_{FB} falls below V_{FB_SCP}, the MP4078 does not detect the ZCD falling edge, and works with a start timer period (t_{START}, typically 49μs). If this conditions remains for the output short-circuit protection duration (t_{SCP}, typically 2.3ms), the device recognizes an SCP condition. Then the MP4078 stops switching and latches off.

During start-up, consider setting V_{FB} to avoid mistriggering SCP. To prevent a mistrigger, the MP4078 implements an output short-circuit protection period during start-up ($t_{SCP_STARTUP}$, typically 100ms).

The MP4078 shuts down during OVP and SCP. It does not turn on again until the chip is reset when V_{CC} drops below V_{CCL} then rises up to V_{CCH} again.

Brownout Protection

The MP4078 integrates brownout protection. The device detects the peak value (V_{MULT}) of the divided rectified input voltage through the MULT pin. If V_{MULT} drops below the brownout threshold (V_{MULT_BO}) and lasts for a brownout-detection time (t_{MULT_BO}), the MP4078 recognizes the brownout condition and shuts down the device.

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The MP4078 is released from brownout protection when V_{MULT} exceeds the brown-in threshold (V_{MULT_BI}) with a hysteresis ($V_{MULT_BO_HYS}$).

Thermal Shutdown

To protect the chip from a thermal hazard, the MP4078 shuts down if the junction temperature exceeds the thermal shutdown threshold (T_{TSD}, typically 160°C) and indicates a fault. The MP4078 keeps the switching off until the following conditions are met:

- The temperature drops below about 100°C (typically a 60°C hysteresis)
- V_{CC} drops below V_{CCL}, then rises up to V_{CCH} again

Then the MP4078 works normally.

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APPLICATION INFORMATION

Selecting the Input Capacitor

If using the MP4078 for a PFC application, do not place a bulk capacitor after the bridge rectifier. Place a bypass capacitor after the bridge rectifier to filter the high-frequency switching ripple across the rectified input voltage with twice the AC line frequency. Under universal input conditions, a 0.22μF to 0.47μF CBB capacitor is recommended for a 30W output power application.

Because there is no bulk capacitor placed at the input, there may be notable surge protection weakness. To improve the reliability during a surge test without sacrificing PF or THD performance, it is recommended to use a circuit with few external components (see Figure 10).

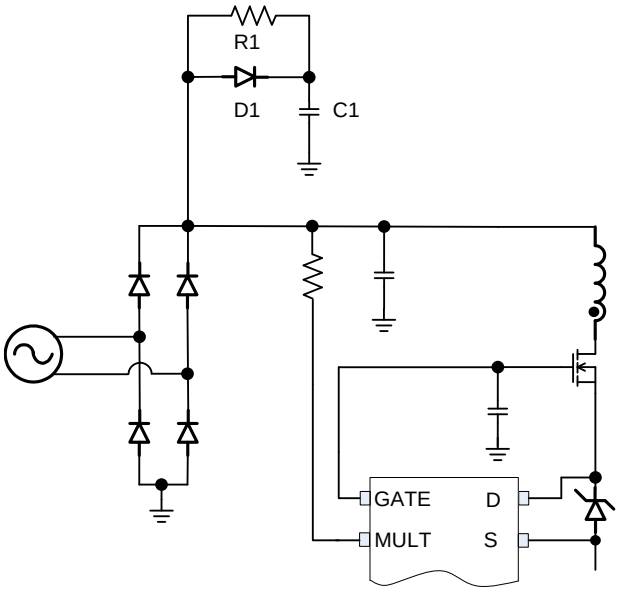

Figure 10: External Circuit for Surge Protection

A larger capacitance with C1 results in improved surge protection. It is recommended to use a 1μF to 2.2μF electrolytic capacitor to pass EN61000-4-5, ±1kV level specifications. R1 is the dissipated resistor for C1, and it is recommended for R1 to be several hundred to thousands of kΩ.

Selecting the Transformer

The MP4078 works in DCM due to its control mode across the whole operating input range. For improved efficiency in low line, it is recommended to make the MP4078 work in an approaching boundary conduction mode at the peak of low-line input voltage. The duty cycle (D_{MAX}) at the peak of the low-line input voltage can be estimated with Equation (5):

$$D_{MAX} \approx \frac{(V_O + V_{DIODE}) \times N}{(V_O + V_{DIODE}) \times N + \sqrt{2} \times V_{IN_RMS_MIN}} \quad (5)$$

Where N is the turning ratio of the primary and secondary winding, and $V_{IN_RMS_MIN}$ is the effective value of the low-line input voltage.

The maximum turn-on time (t_{ON_MAX}) of the primary MOSFET can be estimated with Equation (6):

$$t_{ON_MAX} = D_{MAX} \times t_{CYCLE_MIN} \quad (6)$$

Where t_{CYCLE_MIN} is the configured minimum working cycle.

The input power (P_{IN_MAX}) at the low-line input can be calculated with Equation (7):

$$P_{IN_MAX} = \frac{V_O \times I_O}{\eta} \quad (7)$$

Where I_O is the rated output current, and Ƞ is the estimated efficiency of the low-line input.

The maximum peak for the primary-side current ($I_{PRI_PK_MAX}$) can be estimated with Equation (8):

$$I_{PRI_PK_MAX} = \frac{2\sqrt{2} \times P_{IN_MAX}}{V_{IN_RMS_MIN} \times D_{MAX}} \quad (8)$$

The maximum effective value of the primary-side current ($I_{PRI_RMS_MAX}$) can be estimated with Equation (9):

$$I_{PRI_RMS_MAX} = I_{PRI_PK_MAX} \times \sqrt{\frac{D_{MAX}}{6}} \quad (9)$$

The primary-side inductance (L_M) can be calculated with Equation (10):

$$L_M = \frac{\sqrt{2} \times V_{IN_RMS_MIN} \times t_{ON_MAX}}{I_{PRI_PK_MAX}} \quad (10)$$

Then the required maximum area product (AP_{MAX}) of the transformer can be calculated with Equation (11):

$$AP_{MAX} = \frac{L_M \times I_{PRI_RMS_MAX} \times I_{PRI_PK_MAX} \times (\sqrt{D_{MAX}} + \sqrt{1-D_{MAX}})}{B_{MAX} \times K_U \times J \times \sqrt{D_{MAX}}} \quad (11)$$

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Where B_{MAX} is the maximum allowable flux density (T) (typically 0.2T to 0.3T for common ferrite cores), K_U is the window factor of the transformer (typically 0.15 to 0.3), and J is the current density coefficient (typically 4A/mm^2 to 6A/mm^2).

Choose a ferrite core with an effective area product (AP_{REAL}) that exceeds AP_{MAX}. Calculate the turns on the primary winding (N_P) and secondary winding (N_S) with Equation (12) and Equation (13), respectively:

$$N_P = \frac{L_M \times I_{PRI_PK_MAX}}{B_{MAX} \times A_E} \quad (12)$$

$$N_S = \frac{N_P}{N} \quad (13)$$

Where A_E is the effective core area.

The auxiliary winding provides the power supply for the MP4078 through a diode on the VCC pin during normal operation. The auxiliary winding (N_{AUX}) can be estimated with Equation (14):

$$N_{AUX} = \frac{V_{CC_NOM} + V_{DIODE_AUX}}{V_O + V_{DIODE}} \times N_S \quad (14)$$

Where V_{CC_NOM} is the voltage on the VCC pin during normal operation, and V_{DIODE_AUX} is the forward voltage of VCC diode.

Ensure the inductance leakage on the transformer is sufficiently low. This helps to decrease the switching spike for ZCD sensing and EMI performance.

Selecting the External Pull-Up Resistor on MULT

The peak voltage on the MULT pin (V_{MULT}) is directly related to the on time, and is determined by the external pull-up resistor on the MULT pin (R_{MULT_UP}) and the internal pull-down resistor (R_{MULT}).

In most cases, it is recommended to match the output of the error amplifier (V_{COMP}) with the V_{COMP_FULL} value under full-load conditions. The corresponding on time is the turn-on time during full-load conditions (t_{ON_FULL}) (see Figure 11).

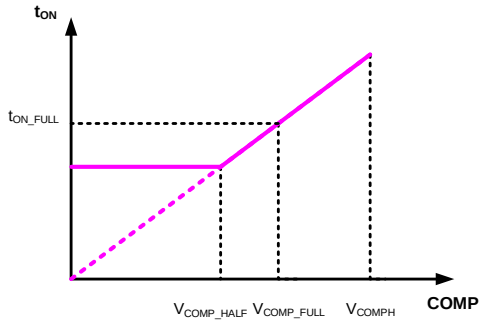

Figure 11: t_{ON} vs V_{COMP}

R_{MULT_UP} can be estimated with Equation (15):

$$R_{MULT_UP} = R_{MULT} \times \left(\frac{\sqrt{2} \times V_{IN_RMS_MIN} \times t_{ON_MAX}}{K_{SLEW} \times V_{COMP_FULL}} - 1 \right) \quad (15)$$

Selecting the Current-Sense Resistor

A proper current-sense resistor both ensures normal operation across the output load range and implements cycle-by-cycle current limitation to guarantee circuit reliability in the event of an overload condition.

The current-sense resistor (R_{SENSE}) can be calculated with Equation (16):

$$R_{SENSE} = \frac{V_{CS_MAX}}{\alpha_{OL} \times I_{PRI_PK_MAX}} \quad (16)$$

Where V_{CS_MAX} is the maximum current limit (typically 880mV), and α_{OL} is the coefficient of the peak primary-side current during overload (1.3 to 1.5 is typically recommended).

Selecting the External Primary MOSFET

The drain-source voltage rating and current rating are two dominant factors to consider when choosing the external primary MOSFET. The maximum drain-to-source voltage ($V_{DS_EXT_MAX}$) appears at the high-line input voltage ($V_{IN_RMS_MAX}$). $V_{DS_EXT_MAX}$ can be calculated with Equation (17):

$$V_{DS_EXT_MAX} = \sqrt{2} \times V_{IN_RMS_MAX} + N \times (V_O + V_{DIODE}) + \Delta V_{PRI_SPIKE} \quad (17)$$

Where ΔV_{PRI_SPIKE} is the turn-off spike on an external MOSFET. This spike is caused by parasitic parameters and the transformer's leakage inductance. With proper transformer and primary snubber design, this value should not exceed 100V in normal operation for universal input applications.

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The maximum effective current on the drain-to-source is the maximum effective primary-side current ($I_{PRI_RMS_MAX}$) that appears at the low-line input voltage ($V_{IN_RMS_MIN}$). It can be calculated with Equation (9).

Selecting the Secondary Rectifier

The maximum voltage across the secondary rectifier (V_{SREC_MAX}) also appears at the high-line input voltage and can calculated with Equation (18):

$$V_{SREC_MAX} = V_O + \frac{\sqrt{2} \times V_{IN_RMS_MAX}}{N} + \Delta V_{SEC_SPIKE} \quad (18)$$

Where ΔV_{SEC_SPIKE} is the switching spike on the secondary rectifier. It is recommended to choose a low-voltage rectifier with a properly designed transformer and secondary snubber for efficiency.

For rectifier diode selection, the maximum current rating is the maximum average forward rectified current, which is equal to the rated output current (I_O).

Selecting the ZCD Resistor Divider

The MP4078 uses the ZCD pin for multiple functions. Besides indicating the output voltage, the ZCD divider also determines the initial configuration for the minimum working cycle.

The paralleled resistance of ZCD ($R_{ZCD_PARALLEL}$) must follow the required t_{CYCLE_MIN} values (see Table 1 on page 15). $R_{ZCD_PARALLEL}$ can be calculated with Equation (19):

$$R_{ZCD_PARALLEL} = \frac{R_{ZCD1} \times R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} \quad (19)$$

Meanwhile, the upper ZCD resistor divider (R_{ZCD1}) can be calculated with Equation (20):

$$R_{ZCD1} = \frac{V_O + V_{DIODE}}{V_{REF} \times R_{ZCD_PARALLEL}} \times \frac{N_{AUX}}{N_S} \quad (20)$$

The down resistor of the ZCD divider (R_{ZCD2}) can also be calculated with Equation (19).

Selecting the Output Capacitor

To achieve a high PF, the bandwidth of the control loop is very slow (typically below 100Hz). This means a large voltage ripple may appear across the output capacitor.

This ripple has two components. One is related to the high-frequency triangles by transformer magnetizing current , which is mostly dependent on the ESR of the output capacitor. Another is related to the twice line frequency envelope from rectified input voltage, which is mostly determined by the capacitance value.

The output ripple (ΔV_{O_RIPPLE}) has a relationship with the output capacitance (C_{OUT}) that can be estimated with Equation (21):

$$\Delta V_{O_RIPPLE} = I_O \times \sqrt{\frac{1}{\left(2\pi \times 2f_{LINE} \times C_{OUT}\right)^2} + R_{ESR}^{\ 2}} \quad (21)$$

Where f_{LINE} is the frequency of the input line voltage, and R_{ESR} is the ESR of the output capacitor.

Use low-ESR capacitors in parallel on the output. The high-frequency switching ripple can be negligible.

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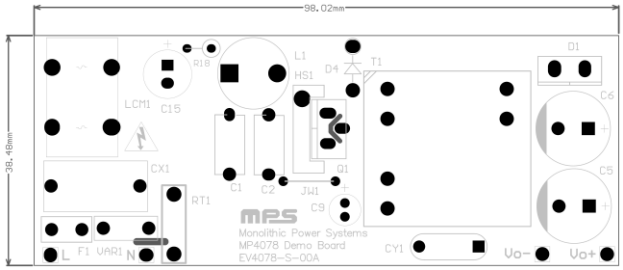
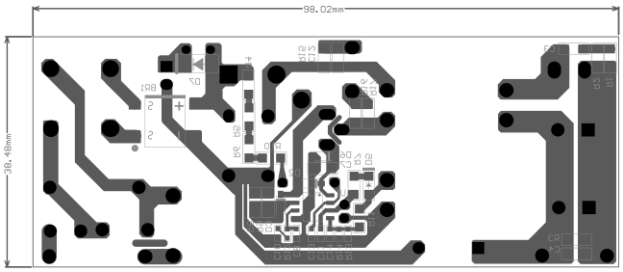
PCB Layout Guidelines

PCB layout is a critical factor for stable operation and EMI performance. For the best results, refer to Figure 12 and follow the guidelines below:

1. Make the primary and secondary power loops as small as possible.
2. Connect one port of the current-sensing resistor to the ground of the input capacitor with the shortest path possible.
3. Separate the reference ground of the MP4078 and control signals circuit from the ground of the power loop. Then connect this signal ground to the ground of the input capacitor with a single-point junction.
4. Make the areas of high dV/dt junctions (e.g. the drain of the external primary MOSFET) as small as possible. Place the MP4078 and control circuits far away from these areas.
5. Do not place the MP4078 inside the power loop.



Top Layer



Bottom Layer

Figure 12: Recommended PCB Layout

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EVALUATION DESIGN CIRCUIT

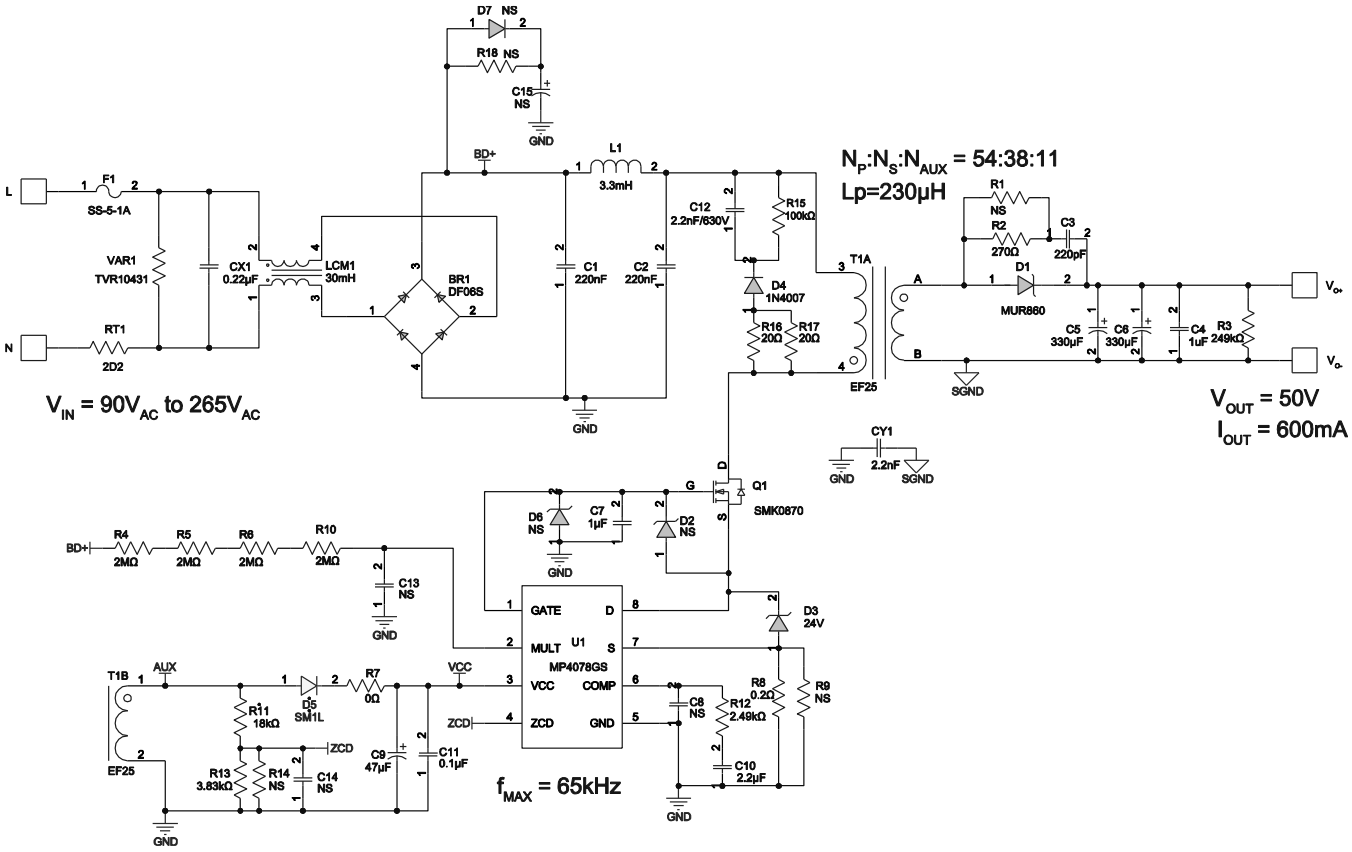

Figure 13: Evaluation Board Schematic

EV4078-S-00A: 90V_{AC} to 265V_{AC} Input, 50V/600mA Output

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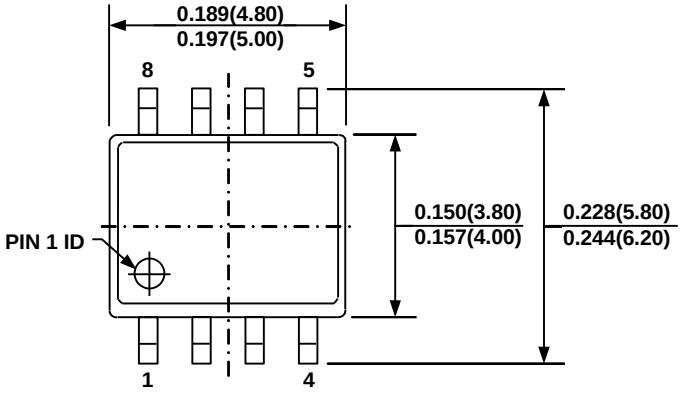
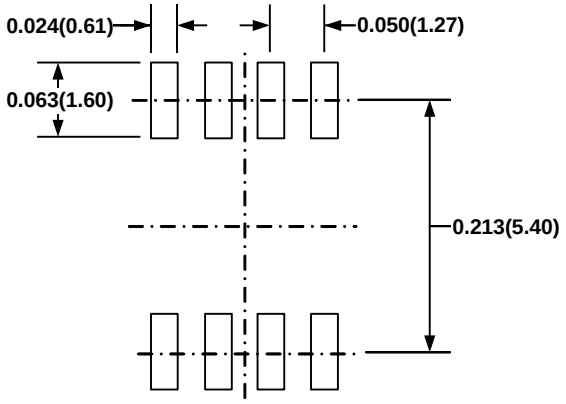
PACKAGE INFORMATION

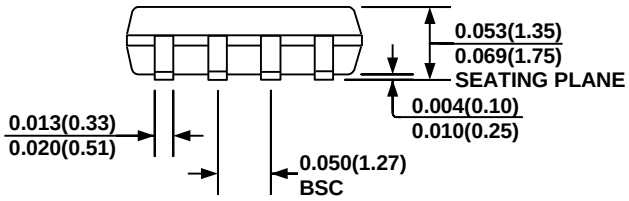
SOIC-8



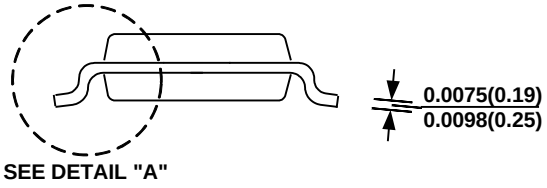
TOP VIEW



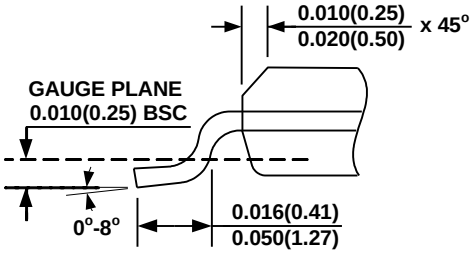
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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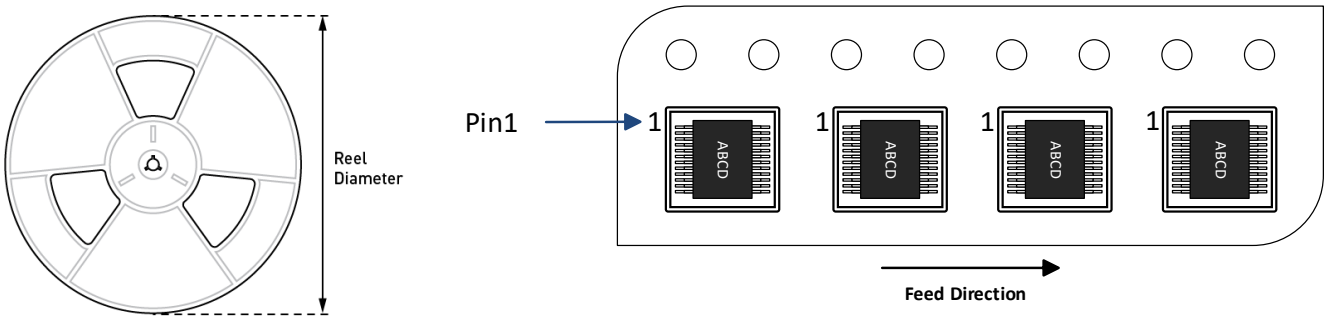
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4078GS–Z	SOIC-8	2500	100	N/A	13in	12mm	8mm

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	7/21/2020	Initial Release	-

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