MP4026

Primary-Side-Control, Offline LED Controller with Active PFC

The Future of Analog IC Technology

DESCRIPTION

The MP4026 is a primary-side-control, offline LED controller that achieves high-power factor and accurate LED current for isolated, single-power-stage lighting applications in a tiny TSOT23-6 package. It is the next generation of the successful MP4021A. The proprietary real-current-control method accurately controls LED current from primary-side information with good line and load regulation. The primary-side-control eliminates the secondary-side feedback components and the opto-coupler to significantly simplify LED-lighting-system design.

The MP4026 integrates power-factor correction and works in valley switching mode to reduce MOSFET switching losses.

The MP4026's multiple protection features greatly enhance system reliability and safety. These features include over-voltage protection, short-circuit protection, primary-side over-current protection, brown out protection, cycle-by-cycle current limiting, V_{CC} under-voltage lockout, and auto-restart over-temperature protection.

FEATURES

- Real-Current Control without Secondary-Feedback Circuit
- Good Line/Load Regulation
- High Power Factor (≥0.9) over Universal Input Voltage
- Valley Switching Mode for Improved Efficiency
- Brown-Out Protection
- Over-Voltage Protection
- Short-Circuit Protection
- Over-Temperature Protection
- Primary-Side Over-Current Protection
- Cycle-by-Cycle Current Limit
- Input UVLO
- Available in TSOT23-6

APPLICATIONS

- Industrial and Commercial Lighting
- Residential Lighting

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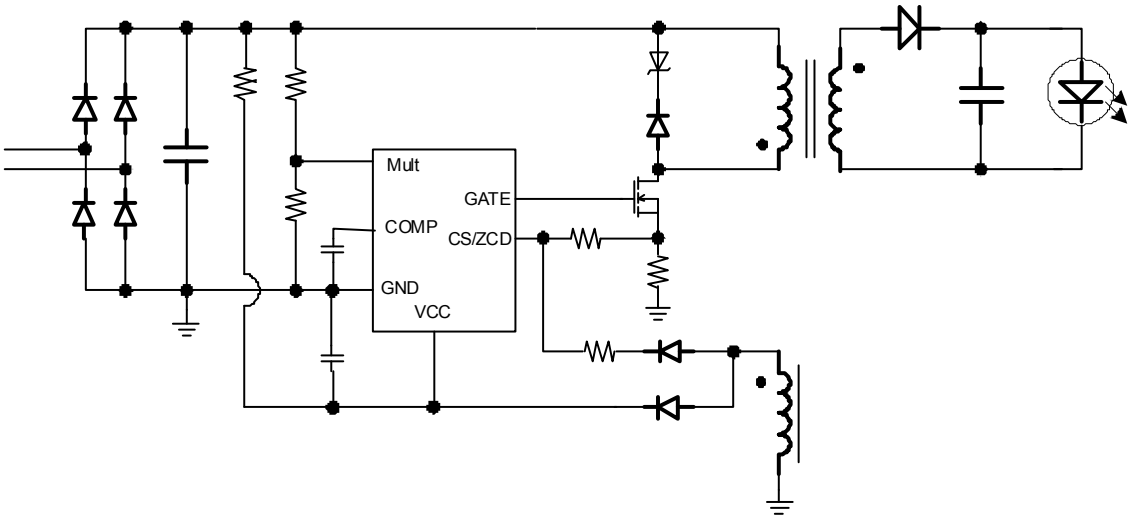
TYPICAL APPLICATION CIRCUIT



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ORDERING INFORMATION

Part Number	Package	Top Marking
MP4026GJ*	TSOT23-6	*See Below*

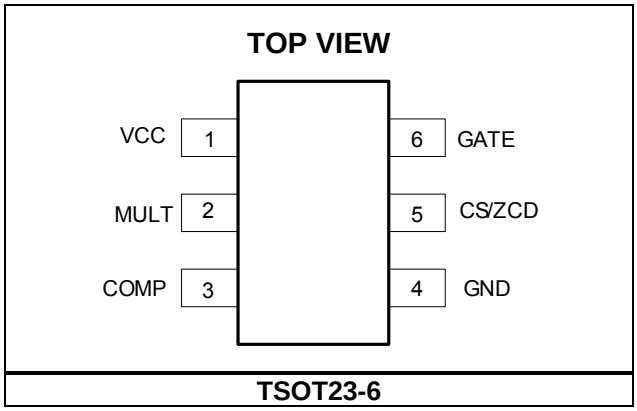
* For Tape & Reel, add suffix –Z (e.g. MP4026GJ–Z);

TOP MARKING

|AFSY

AFS: product code of MP4026GJ;
Y: year code.

PACKAGE REFERENCE



TSOT23-6

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ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{CC} .....-0.3V to +30V
Gate Drive Voltage .....-0.3V to +17V
ZCD Pin .....-0.3V to 6.5V
Other Analog Inputs and Outputs ..-0.3V to 6.5V
Max. Gate Source Current..... 0.8A
Max. Gate Sink Current .....-1A
Continuous Power Dissipation (T_A = +25°C)(2)
TSOT23-6 ..... 1.25W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{CC} .....12V to 28V
Operating Junction Temp. (T_J)..-40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
TSOT23-6……..	100....	55.. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

Typical values are at VCC = 20V, T_J = +25°C, unless otherwise noted.
Minimum and maximum values are at VCC = 20V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Operating Range	V_{CC}	After turn on	12		28	V
Turn-On Threshold	V_{CC_ON}	V_{CC} rising edge	23	24.9	28	V
Turn-Off Threshold	V_{CC_OFF}	V_{CC} falling edge	8.2	9.3	10.8	V
Hysteretic Voltage	V_{CC_HYS}		14.2	15.6	17.3	V
Supply Current						
Start-up Current	$I_{STARTUP}$	V_{CC}= V_{CC_ON} -1V		20	50	µA
Quiescent Current	I_Q	No switching		0.6	0.82	mA
Operating Current Under Fault Condition		No switching		2		mA
Operating Current	I_{CC}	f_s =70kHz, C_{GATE}=1nF		2	3	mA
Multiplier						
Linear Operation Range	V_{MULT}		0		3	V
Gain	$K^{(5)}$			1.3		1/V
Brown-Out Protection Threshold			280	300	316	mV
Brown-Out Detection Time			25	42	60	ms
Brown-Out-Protection-Hysteretic Voltage			90	100	110	mV
Error Amplifier						
Feedback Voltage	V_{FB}		0.401	0.413	0.425	V
Transconductance [6]	G_{EA}			125		µA/V
Upper Clamp Voltage	V_{COMP_H}		4.5	4.75	5.1	V
Lower Clamp Voltage	V_{COMP_L}		1.42	1.5	1.58	V
Max. Source Current[6]	I_{COMP}			50		µA
Max. Sink Current[6]	I_{COMP}			-200		µA
Current Sense Comparator and Zero Current Detector						
CS/ZCD Bias Current	$I_{BIAS_CS/ZCD}$				500	nA
Leading-Edge-Blanking Time	t_{LEB_CS}		200	320	550	ns
Current-Sense-Clamp Voltage	V_{CS_CLAMP}		1.9	2.0	2.1	V
Over-Current-Protection, Leading-Edge-Blanking Time	t_{LEB_CSOCP}		130	200	380	ns
Over-Current-Protection Threshold	V_{CS_OCP}		2.4	2.5	2.6	V
Zero-Current-Detection Threshold	V_{ZCD_T}	V_{ZCD} falling edge	0.270	0.295	0.318	V
Zero-Current-Detect Hysteresis	V_{ZCD_HYS}		562	595	628	mV

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ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at VCC = 20V, T_J = +25°C, unless otherwise noted.
Minimum and maximum values are at VCC = 20V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ZCD Blanking Time	t_{LEB_ZCD}	After turn-off, V_{MULT_O} >0.3V	1.2	1.6	2.1	μs
	t_{LEB_ZCD}	After turn-off, V_{MULT_O} ≤0.3V	0.6	0.8	1.1	μs
Over-Voltage Blanking Time	t_{LEB_OVP}	After turn-off, V_{MULT_O} >0.3V	1.2	1.6	2.1	μs
	t_{LEB_OVP}	After turn-off, V_{MULT_O} ≤0.3V	0.6	0.8	1.1	μs
Over-Voltage Threshold	V_{ZCD_OVP}	1.6μs delay after turn-off	4.9	5.1	5.4	V
Minimum Off Time	t_{OFF_MIN}		4	5.5	8	μs
Starter						
Start-Timer Period	t_{START}			190		μs
Gate Driver						
Output-Clamp Voltage	V_{GATE_CLAMP}	V_{CC}=28V	13	14.5	17	V
Minimum-Output Voltage	V_{GATE_MIN}	V_{CC}=V_{CC_OFF} + 50mV	6.7			V
Max. Source Current(6)	I_{GATE_SOURCE}			0.8		A
Max. Sink Current(6)	I_{GATE_SINK}			-1		A
Thermal Shutdown						
Thermal Shutdown Threshold(7)	T_{SD}			150		℃
Thermal Shutdown Recovery Hysteresis(7)	T_{HYS}			25		℃

Notes:
5) The multiplier output is given by: Vcs=k*V_{MULT}*(V_{COMP}-1.5)
6). Guaranteed by design.
7). Guaranteed by characterization.

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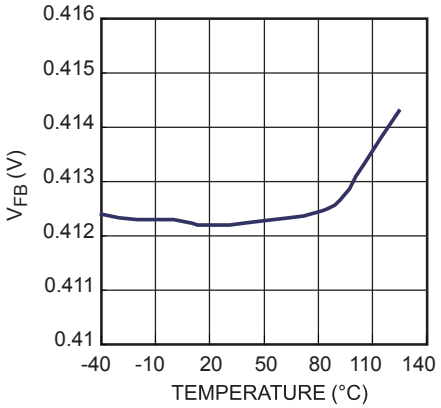
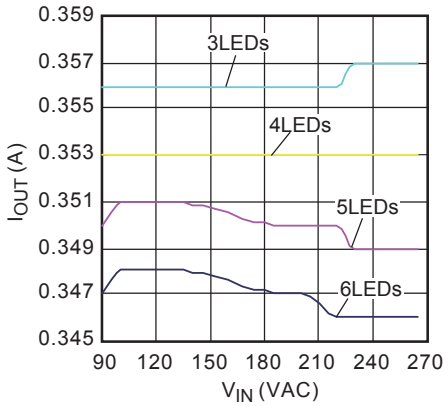
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 90V-265V, V_{OUT} = 10-20V, I_{LED}=350mA, T_A = 25°C, unless otherwise noted.

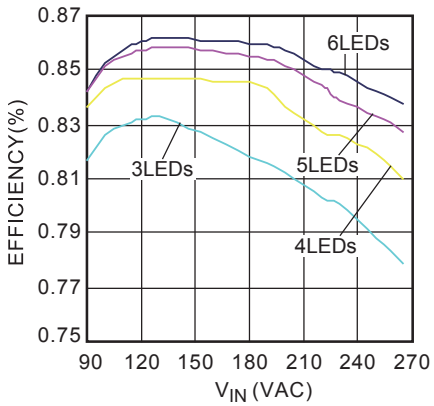
V_{FB} Temperature Tendency



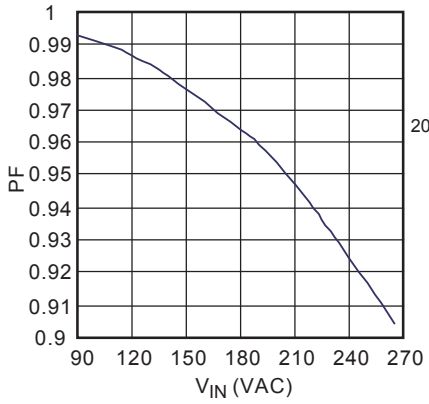
Line/Load Regulation



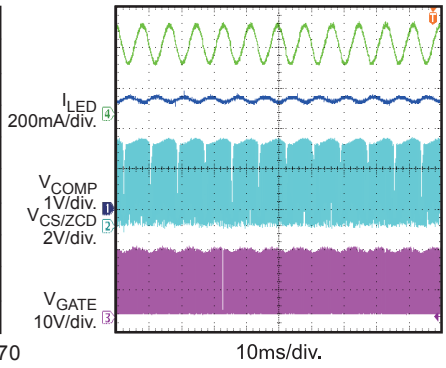
Efficiency



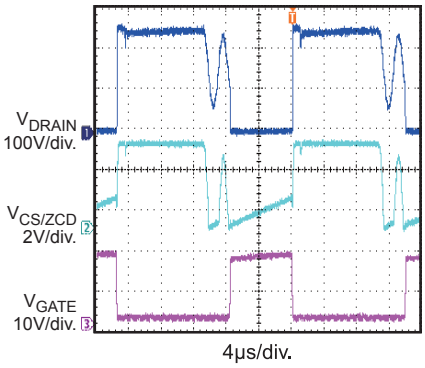
PF @Full Load



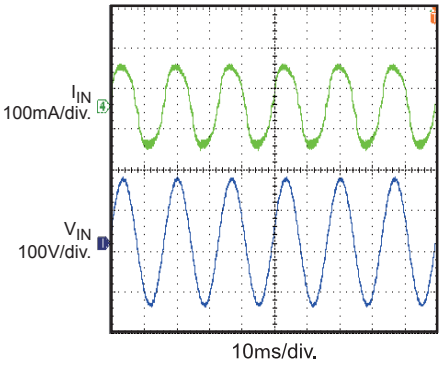
Steady State
V_{IN} =110V



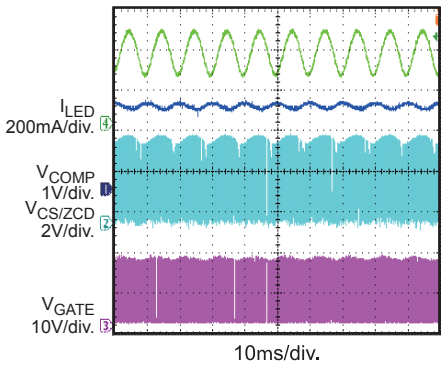
Steady State
V_{IN} =110V



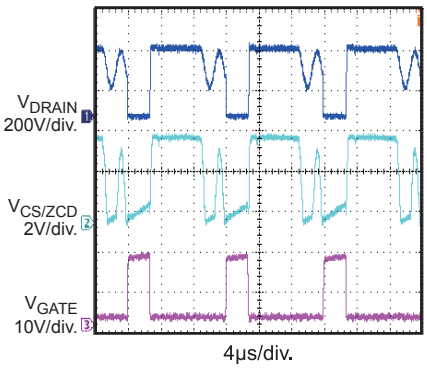
Steady State
V_{IN} =110V



Steady State
V_{IN} =230V



Steady State
V_{IN} =230V



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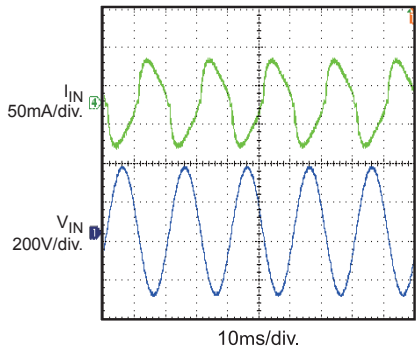
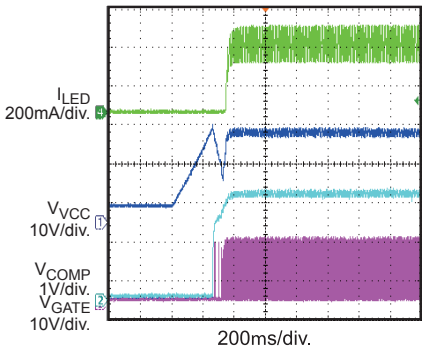
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 90V-265V, V_{OUT} = 10-20V, I_{LED}=350mA, T_A = 25°C, unless otherwise noted.

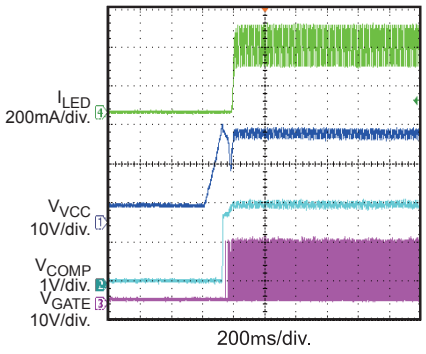
Steady State
V_{IN} =230V



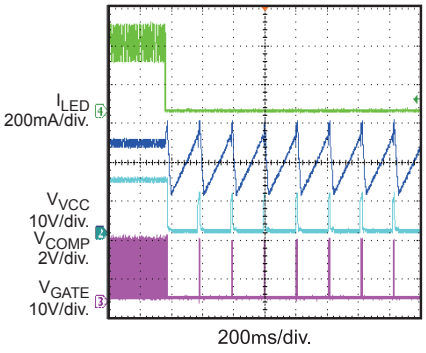
VIN Start up
V_{IN} = 110V



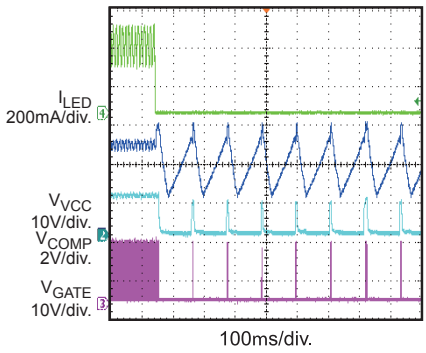
VIN Start up
V_{IN} = 230V



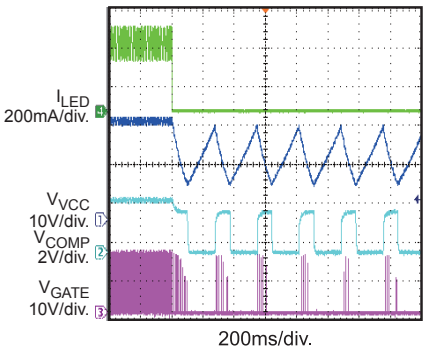
Open LED Protection
V_{IN} = 110V, Open LED @ Working



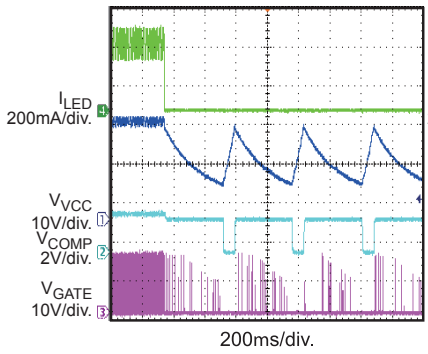
Open LED Protection
V_{IN} =230V, Open LED @ Working



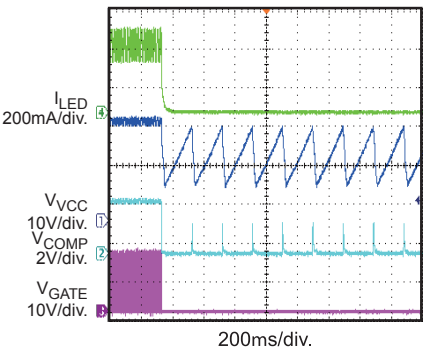
Short Circuit Protection
V_{IN} =110V
Short LED+ to LED- @ Working



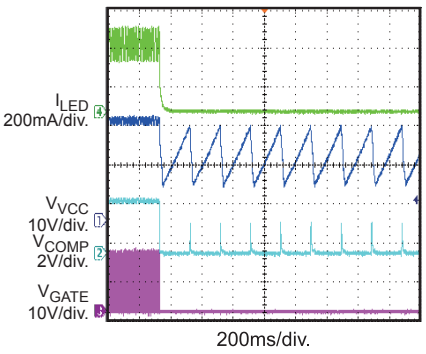
Short Circuit Protection
V_{IN} =230V
Short LED+ to LED- @ Working



Primary-Side OCP Protection
V_{IN} =110V
Short primary winding @ Working



Primary-Side OCP Protection
V_{IN} =230V
Short primary winding @ Working



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PIN FUNCTIONS

Pin	Name	Description
1	VCC	Power Supply. Supplies power for the control signals and the high-current MOSFET. Bypass to ground with an external bulk capacitor (typically 4.7μF).
2	MULT	Input Voltage Sense. Connect to the tap of resistor divider between the rectified AC line and GND. The half-wave sinusoid provides a reference signal for the internal-current-control loop. The MULT pin is also used for brown-out protection detection.
3	COMP	Loop Compensation. Connect a compensation network to stabilize the LED driver and maintain an accurate LED current.
4	GND	Ground. Current return for the control signal and the gate-drive signal.
5	CS/ZCD	Current Sense or Zero-Current Detection. When the gate driver turns on, a sensing resistor senses the MOSFET current. The comparison between the sensed voltage and the internal sinusoidal-current reference determines when the MOSFET turns off. If the pin voltage exceeds the current limit (2.0V, after turn-on blanking) the gate drive turns off. When the gate driver turns off, the negative falling-edge (after the blanking time) triggers the external MOSFET's turn-on signal. Connect this pin to a resistor divider though a diode between the auxiliary winding and GND. Over-voltage condition is detected through ZCD. For every turn-off interval, if the ZCD voltage exceeds the over-voltage-protection threshold after the 1.6μs (V_{mult_o} >0.3V) or 0.8μs (V_{mult_o} ≤0.3V) blanking time, over-voltage protection triggers and the system stops switching until auto-restart. CS/ZCD is also used for primary-side over-current-protection, if the sensing voltage reaches to 2.5V after a blanking time at gate turn-on interval, the primary-side over-current-protection triggers and the system stops switching until auto-restart. A 10pF ceramic cap is recommended to connect from CS/ZCD to GND to bypass the high frequency noise. In order to reduce the RC delay influence to the sample accuracy of the current sensing signal, the CS/ZCD down side resistance (R_{ZCD2} in figure 7) is suggested to be selected as small as 1kΩ.
6	GATE	Gate Drive Output. This totem-pole output stage can drive a high-power MOSFET with a peak current of 0.8A source and 1A sink. The high-voltage limit is clamped to 14.5V to avoid excessive gate-drive voltage. The low-voltage is higher than 6.7V to guarantee a sufficient drive capacity.

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FUNCTION DIAGRAM

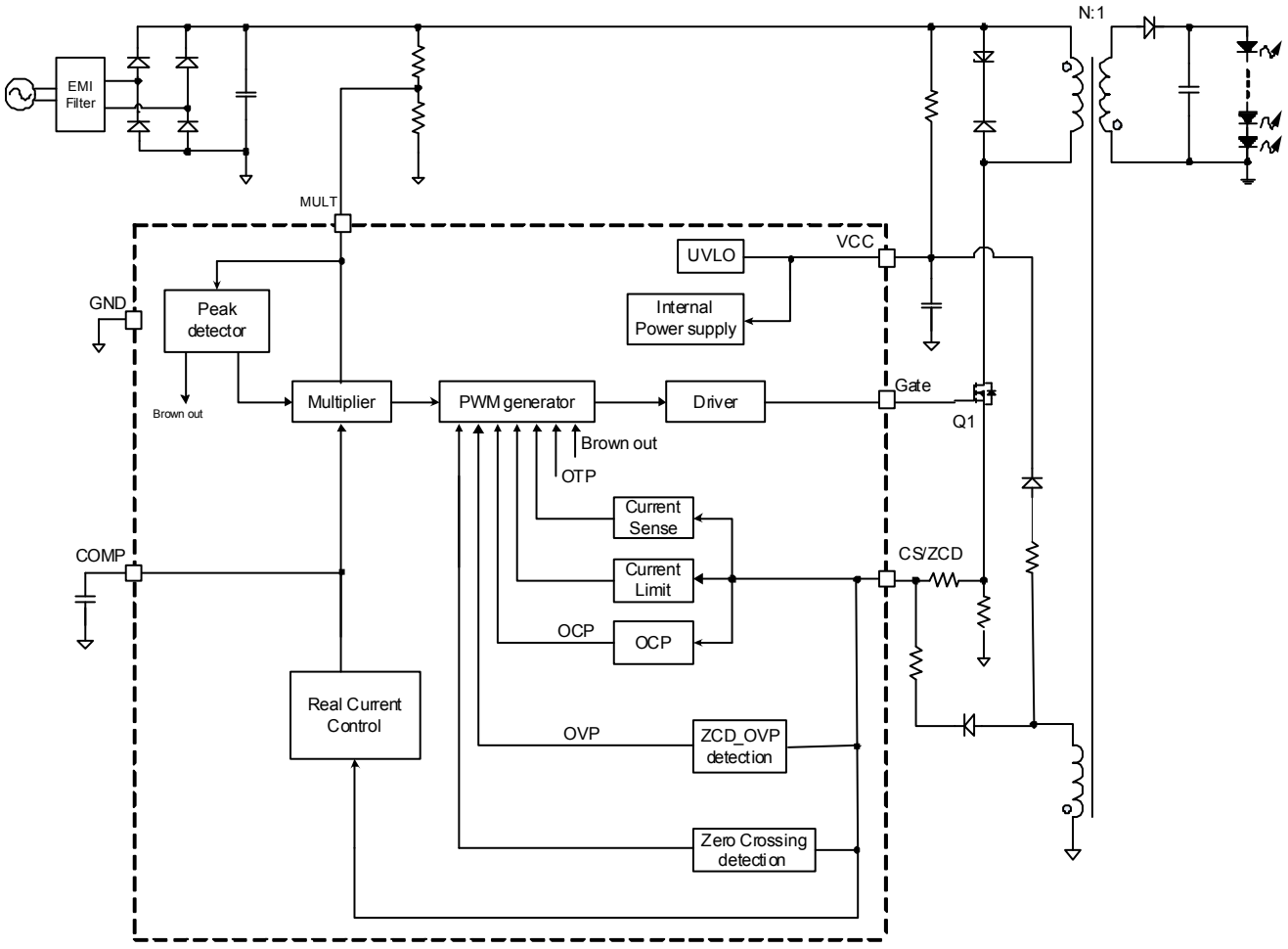

Figure 1—MP4026 Function Block Diagram

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OPERATION

The MP4026 is a primary-side-controlled, offline LED controller for high-performance LED lighting. It has primary-side real-current control for accurate LED current regulation. It also has active power factor correction (PFC) to eliminate harmonic noise on the AC line. The rich protections can achieve a high safety and reliability in real application.

Start Up

Initially, AC line charges up V_{CC} through the start-up resistor. When V_{CC} reaches 24.9V, the control logic starts. Then the power supply is taken over by the auxiliary winding when the voltage of auxiliary winding builds up.

The MP4026 will shut down when V_{CC} drops below 9.3V.

The high hysteretic voltage allows for a small VCC capacitor (typically 4.7μF) to shorten the start-up time.

Valley Switching Mode

During the external MOSFET ON-time (t_{ON}), the rectified-input voltage (V_{BUS}) charges the primary-side inductor (L_P) causing the primary-side current (I_{PRI}) to increase linearly from zero to peak value (I_{PK}). When the MOSFET turns off, the energy stored in the inductor is transferred to the secondary-side, which activates the secondary-side diode to power the load. The secondary current (I_{SEC}) decreases linearly from its peak value to zero. When the secondary current decreases to zero, the MOSFET drain-source voltage starts oscillating, which is caused by the primary-side magnetizing inductance and parasitic capacitances—the voltage ring also is reflected on the auxiliary winding (see Figure 2). To improve primary-control precision, the chip monitors when ZCD voltage falls to zero twice before the next switching period. The zero-current detector from CS/ZCD generates GATE turn-on signal when the ZCD voltage falls below 0.295V the second time (see Figure 3).

This virtually eliminates switch turn-on loss and diode reverse-recovery losses, ensuring high efficiency and low EMI noise.

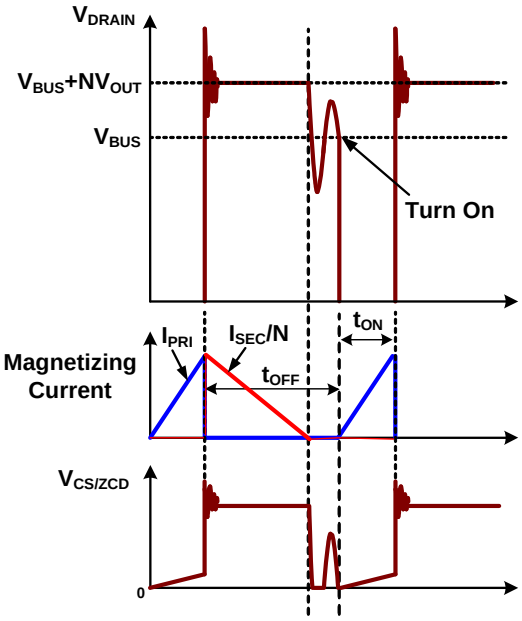

Figure 2: Valley Switching Mode

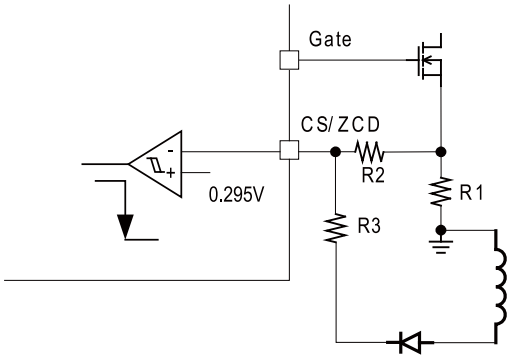

Figure 3: Zero-Current Detector

Real-Current Control

The proprietary real-current-control method allows the MP4026 to control the secondary-side LED current using primary-side information. The mean output LED current is approximately:

$$I_o \approx \frac{N \cdot V_{FB}}{2 \cdot R_s}$$

Where:

- N is the primary-side-to-secondary-side turn ratio,
- V_{FB} is the feedback reference voltage (typically 0.413V), and
- R_s is the sensing resistor connected between the MOSFET source and GND.

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Power-Factor Correction

The MULT pin is connected to a pull up resistor from the rectified-instantaneous-line voltage and fed as one input of the Multiplier. The multiplier output is sinusoidal.. This signal provides the reference for the current comparator and comparing with the primary-side-inductor current, which sets the sinusoidal primary-peak current. This helps to achieve a high-power factor.

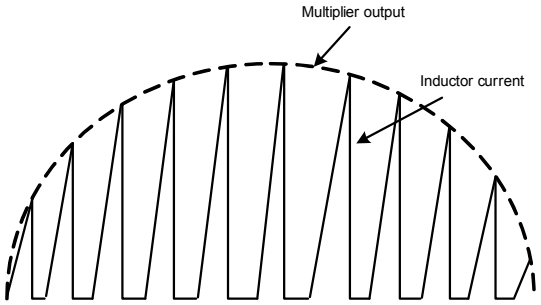

Figure 4: Power-Factor Correction

The maximum voltage of the multiplier output to the current comparator is clamped at 2V for a cycle-by-cycle current limit.

VCC Under-Voltage Lockout

When V_{CC} drops below the UVLO threshold (9.3V), the MP4026 stops switching and shuts down. The operating current is very low under this condition, the V_{CC} will be charged up again by the external start up resistor from AC line. Figure 5 shows the typical V_{CC} under-voltage lockout waveform.

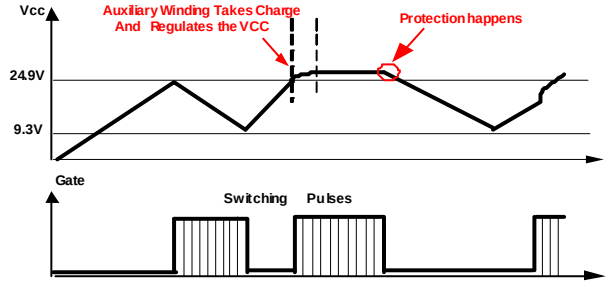

Figure 5: VCC Start-Up Waveform

Auto Starter

The MP4026 has an integrated auto starter. The starter times when the MOSFET is OFF: If ZCD fails to send out another turn-on signal after 190μs, the starter will automatically send out the turn-on signal to avoid unnecessary shutdowns due to missing ZCD detections.

Minimum Off Time

The MP4026 operates with a variable switching frequency; the frequency changes with the instantaneous-input-line voltage. To limit the maximum frequency and get a good EMI performance, the MP4026 employs an internal, minimum-off-time limiter—5.5μs.

Leading-Edge Blanking

To avoid premature switching-pulse termination due to the parasitic capacitances discharging when the MOSFET turns on at normal operation, the MP4026 uses an internal-leading edge blanking (LEB) unit between the CS/ZCD pin and the current-comparator input. During the blanking time, the path from the CS/ZCD pin to the current comparator input is blocked. Figure 6 shows the leading-edge blanking. The LEB time of primary-side OCP detection is relatively short, 200ns.

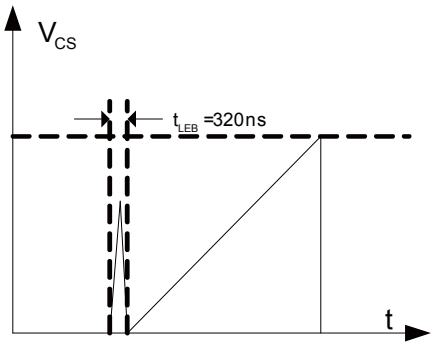

Figure 6: Leading-Edge Blanking

Output Over-Voltage Protection

Output over-voltage protection prevents component damage during an over-voltage condition. The auxiliary-winding voltage's positive plateau is proportional to the output voltage: the OVP uses the auxiliary winding voltage instead of directly monitoring the output voltage. Figure 7 shows the OVP sampling unit. Once the ZCD voltage exceeds 5.1V at gate turn off interval, the OVP signal will be triggered and latched, the gate driver will be turned off and the IC works at quiescent mode, the V_{CC} voltage dropped below the UVLO which will make the IC shut down, and the system restarts again.

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The output-OVP-set point is then:

$$V_{OUT_OVP} \cdot \frac{N_{AUX}}{N_{SEC}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 5.1V$$

Where:

- V_{OUT_OVP} is the output-over-voltage-protection point,
- N_{AUX} is the number of auxiliary-winding turns, and
- N_{SEC} is the number of secondary-winding turns.

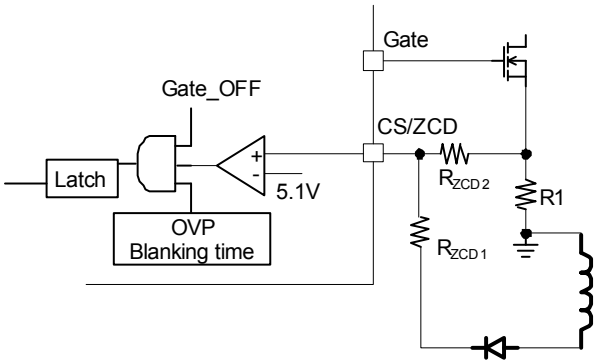

Figure 7: OVP Sampling Unit

To prevent a voltage spike from mis-triggering OVP after the switch turns off, OVP sampling has a t_{LEB_OVP} blanking period (typically 1.6μs when V_{MULT_O} > 0.3V and 0.8μs when V_{MULT_O} ≤ 0.3V) as shown in Figure 8.

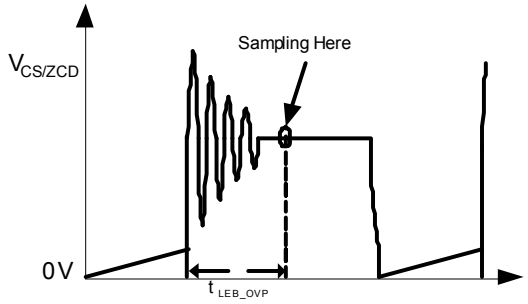

Figure 8: ZCD Voltage and OVP Sampler

Output Short-Circuit Protection

If an output short occurs, the ZCD can not detect the transformer's zero-current-crossing point, so the 190μs auto-restart timer triggers the power MOSFET's turn-on signal. Then the switching frequency of the power circuit drops to about 5kHz, and the output current is limited to its nominal current. The auxiliary-winding voltage drops to follow the secondary-winding voltage, V_{CC} drops to less than the UV threshold, and the system restarts. This sequence limits the output power and IC temperature rise if an output short occurs.

Primary-Side Over-Current Protection

The primary-side over-current protection prevents device damage caused by extremely excessive current, like primary winding short. If the CS/ZCD pin voltage rising to 2.5V at gate turn on interval, as shown in Figure 9, the primary-side over-current protection signal will be triggered and latched, the gate driver will be turned off and the IC works at quiescent mode, the V_{CC} voltage dropped below the UVLO which will make the IC shut down, and the system restarts again.

To avoid mis-trigger by the parasitic capacitances discharging when the MOSFET turns on, a LEB time is needed, this LEB time is relatively smaller than current regulation sensing LEB time, typical 200ns.

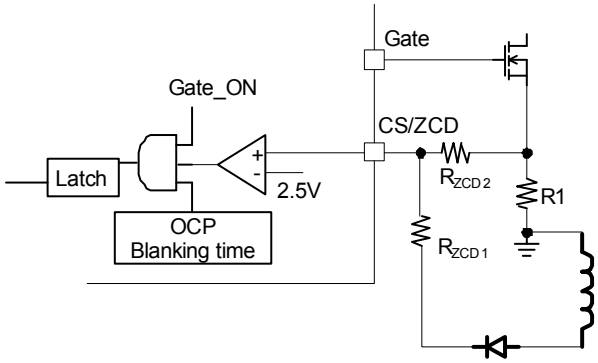

Figure 9: Primary-side OCP Sampling Unit

Brown-Out Protection

The MP4026 has brown-out protection: the internal peak detector detects the peak value of the rectified sinusoid waveform in MULT pin. If the peak value is less than the brown-out-protection threshold 0.3V for 42ms, the IC recognizes this condition as a brown-out, quickly drops the COMP voltage to zero, and disables the power circuit. If the peak value exceeds 0.4V, the IC restarts and the COMP voltage rises softly again. This feature prevents both the transformer and LED currents from saturating during fast ON/OFF switching. Figure 10 shows the brown-out waveforms.

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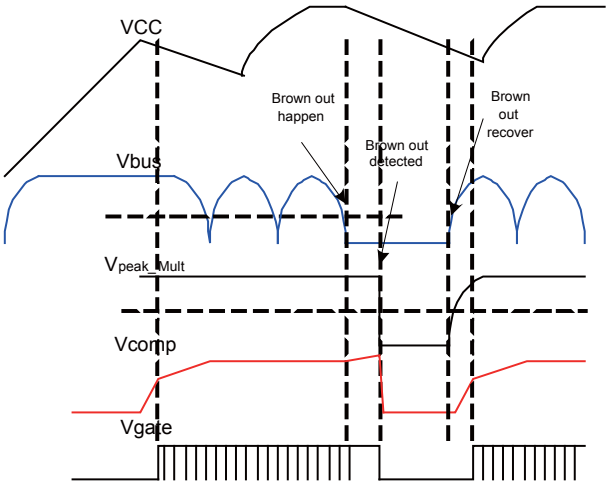

Figure 10: Brown-Out Protection Waveforms

IC Thermal Shut Down

To prevent from any lethal thermal damage, when the inner temperature exceeds the OTP threshold, the MP4026 shuts down switching cycle and latched until VCC drop below UVLO and restart again.

Design Example

For the design example, please refer to MPS application note AN076 for the detailed design procedure.

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NON-ISOLATED APPLICATIONS

The isolated solution can prevent human body from an electric shock by grid when touching the load. But the power loss and the cost are increased. Recur to safety enclosure frame of the lamp, compared with isolated solution, the non-isolated solution can achieve higher efficiency and highly cost-effective.

Generally, the Flyback converter is common for the offline isolated applications. As topology transmutation, the non-isolated low-side Buck-boost converter is also popular. Besides fitting in isolated application, the MP4026 can also operate in the offline non-isolated LED lighting applications.

Figure 16 is a 30W low-side Buck-boost LED driver with MP4026.

Operation of Low-side Buck-boost

The low-side Buck-boost can be treated as Flyback converter with 1:1 turn ratio transformer. So, the whole operation is absolutely same as the description above. Different from isolated solution, there are no separate primary- and secondary-winding, so a smaller core size is available for design. Without the impact of the leakage inductance, the snubber is unnecessary. All of these can save cost and improve the efficiency of the driver.

The Selection of FET & Rectifier Diode

Since it is just an inductor for non-isolated solution, compared with isolated solution, at same output voltage, the power FET can be selected with lower voltage rating. But, oppositely, the voltage rating of rectifier diodes for output and aux-winding must be increased.

Improvement of RF EMI

CY1 in Figure 16 is added for RF EMI improvement. The recommended value is from 10nF to 47nF with 630V rating.

Improvement of PFC & THD

The impact of non-turn-ratio is that the duty cycle of the converter becomes smaller at same spec. Based on MP4026 PFC principle, the PF and THD of the converter drops compared with isolated solution. So, generally, the non-isolated solution is especially suitable for high output voltage, since the higher output voltage can extend the duty cycle to improve the PF and THD and the efficiency can also be improved meanwhile.

For the non-isolated solution with low output voltage, the tapped-inductor can be applied to improve the PF and THD.

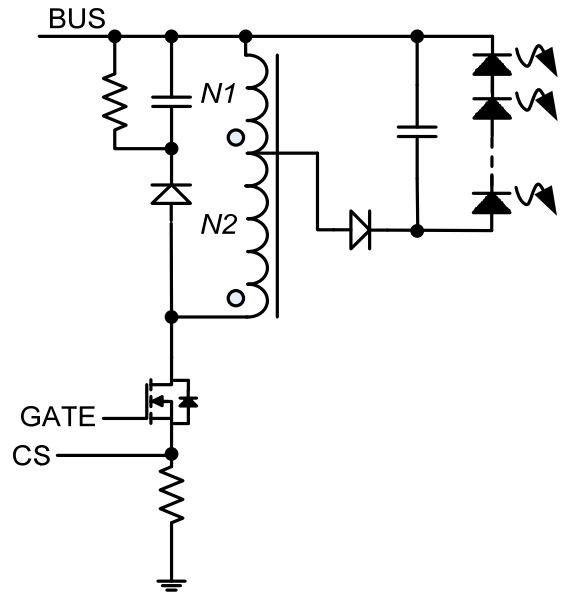

Figure 11: Tapped-inductor for Low-side Buck-boost Solution

Shown in Figure 11, the tapped-inductor includes two windings (N1 & N2) and a tap to connect the rectifier diode. When the power FET is turned on, the current goes thru both of the windings. But when the power FET is off, just N1 conducts the current thru the rectifier diode. The stored energy of N2 is released by flux couple. So, the tapped-inductor features a similar turn-ratio like the transformer in isolated solution.

The nominal turn-ratio is

$$n = \frac{N1 + N2}{N1} > 1$$

The duty cycle of the converter is obviously extended by tapped-inductor, and then the better PF and THD are available.

But, like transformer, the snubber is necessary to clamp the voltage spike caused by leakage inductance.

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On the other hand, the non-dimmable solution usually needs to cover universal input range. The input range is very wide, from 85VAC to 264VAC. The MULT pin is used to detect the input voltage signal, but the resistor divider of MULT is fixed. So, at high line input, the signal for MULT input is very low, which results in adverse effect for internal multiplier sampling, then affect the PFC performance.

Figure 12 shows an improved circuitry on MULT resistor divider to adjust the ratio of the divider to achieve better THD.

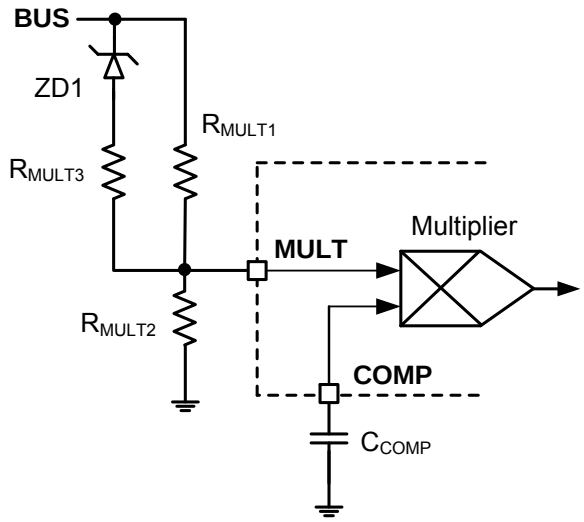

Figure 12: THD Improved Circuitry

The ZD1 is a HV Zener diode. The common voltage rating is from 80V to 130V.

At low line input, the BUS can not breaks down ZD1, the MULT pin signal is

$$V_{MULT} = V_{BUS} \times \frac{R_{MULT2}}{R_{MULT1} + R_{MULT2}}$$

When the input voltage rises up, once the BUS breaks down ZD1, R_{MULT3} is paralleled with R_{MULT1} to increase the ratio of the divider to raise the MULT signal.

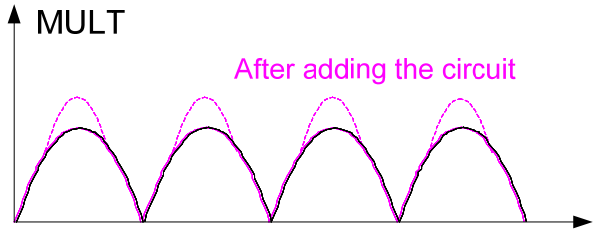

Figure 13: The MULT Signal with THD Improved Circuitry

As Figure 13 shown, after adding the THD improved circuitry, the top part of the MULT voltage rises up as the dashed line. Then the input current at top of BUS is increased while the input current at the zero-crossing is reduced, which results in the input current more like sinusoid and then the THD is improved.

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TYPICAL APPLICATION CIRCUITS

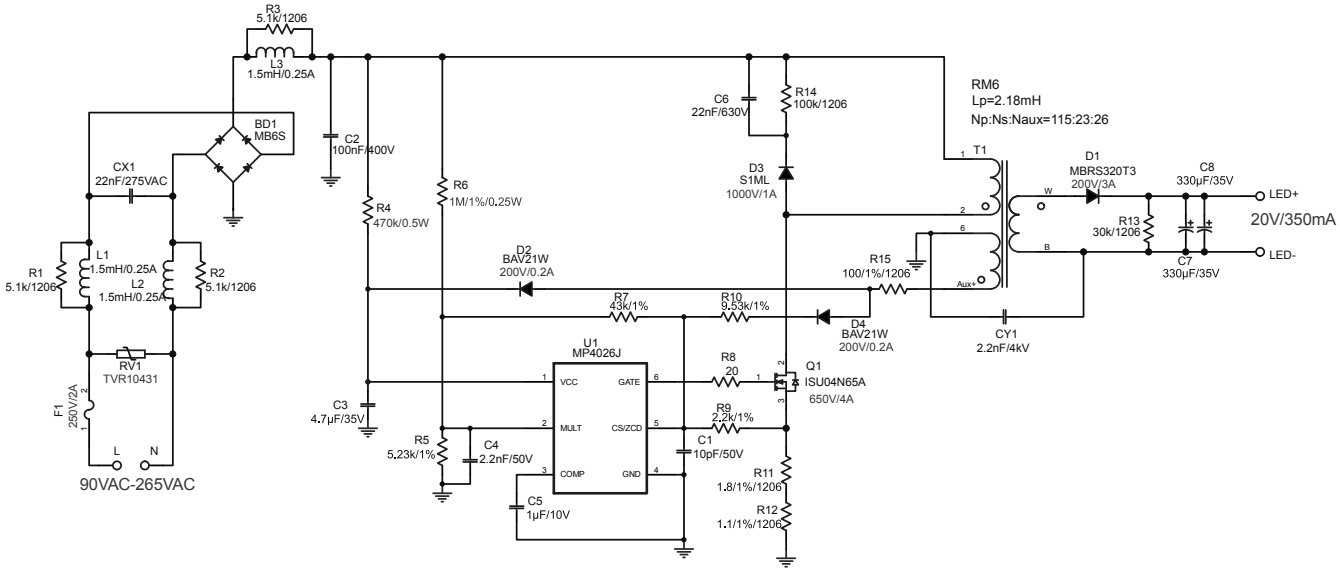

Figure 14: A19 Bulb Driver, 90-265VAC Input, Isolated Flyback Converter, V_O =20V, I_O=350mA
EVB Model: EV4026-J-00A

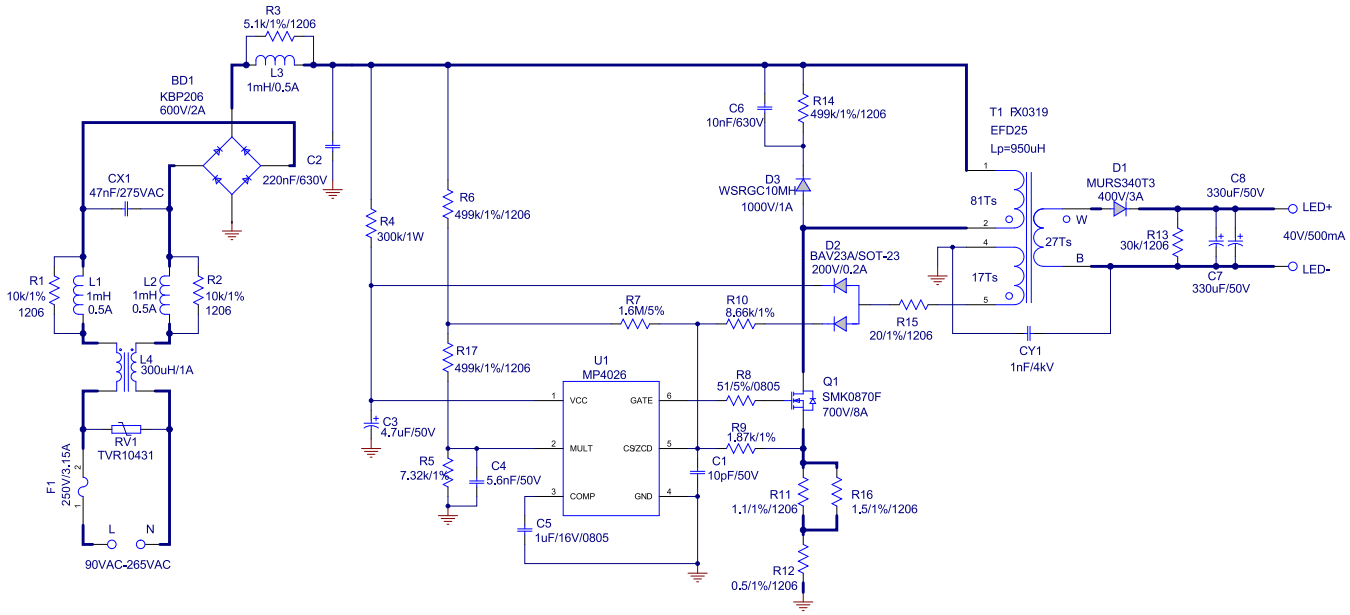

Figure 15: PAR38 Driver, 90-265VAC Input, Isolated Flyback Converter, V_O =40V, I_O=500mA
EVB Model: EV4026-J-00B

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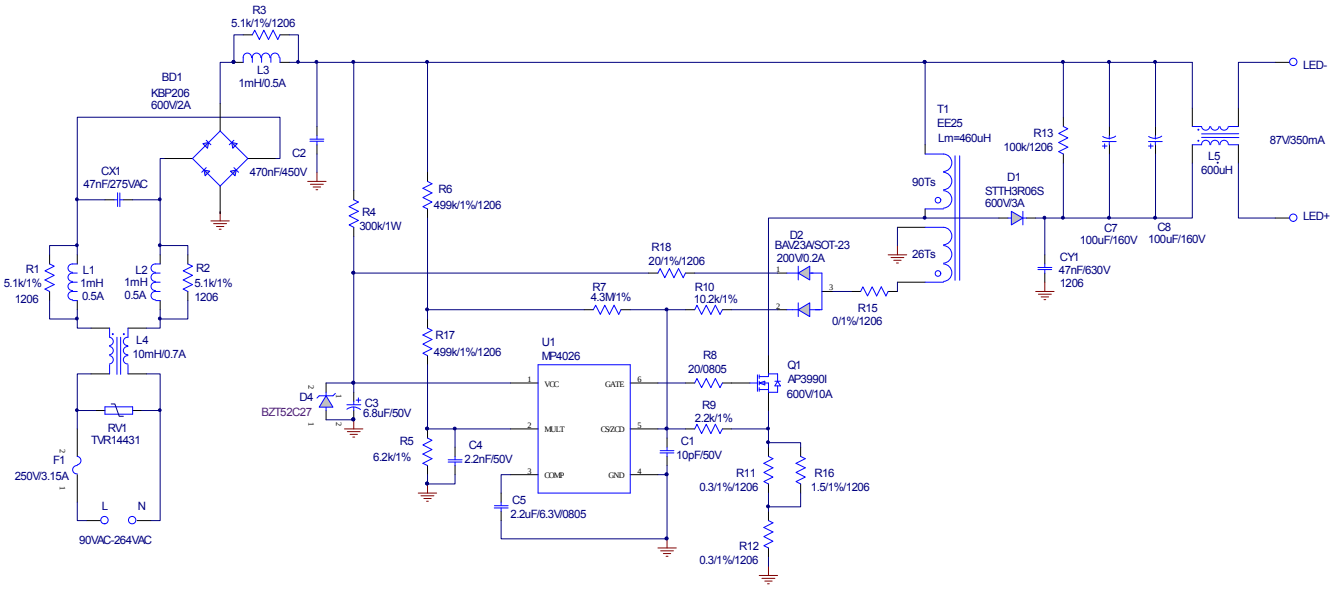

Figure 16: 90-264VAC Input, Non-isolated Low-side Buck-boost Converter, V_O =87V, I_O=350mA

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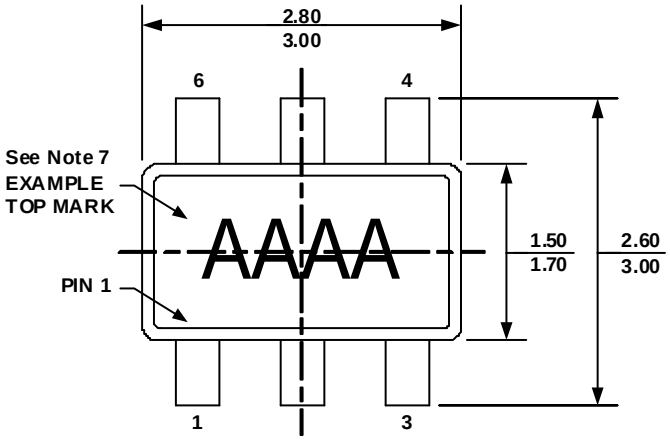
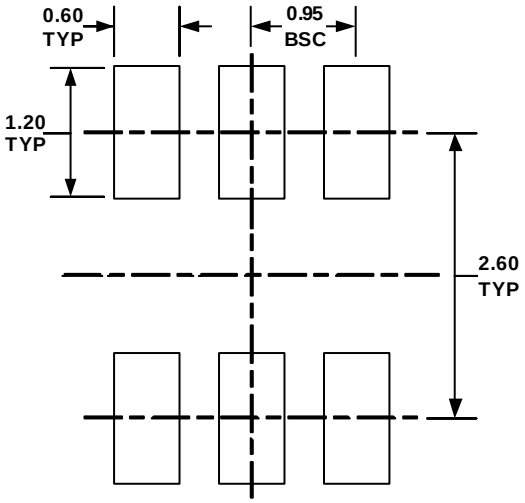
PACKAGE INFORMATION

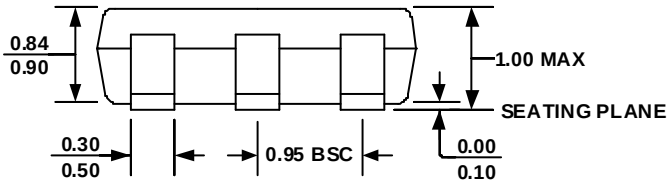
TSOT23-6



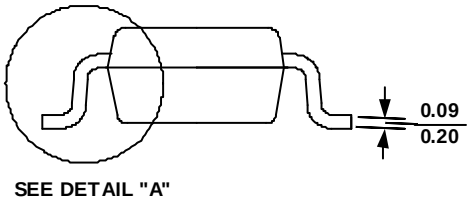
TOP VIEW



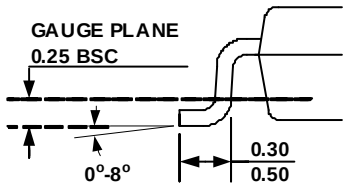
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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