MP4021A

Primary Side Control
Offline LED Controller with Active PFC

The Future of Analog IC Technology

DESCRIPTION

The MP4021A is a primary-side–control offline LED lighting controller that achieves high power factor and accurate LED current for isolated single-power-stage lighting applications in a single SOIC8 package. The proprietary real-current control method accurately controls LED current from primary-side information. Eliminating the secondary-side feedback components and the optocoupler significantly simplifies the LED lighting system design.

The MP4021A integrates power factor correction and works in boundary conduction mode to reduce the MOSFET switching losses.

The extremely low start-up current and quiescent current reduces the total power consumption and provides a high-efficiency solution for lighting applications.

The multi-protection features of MP4021A greatly enhance system reliability and safety. The MP4021A features over-voltage protection, short-circuit protection, cycle-by-cycle current limiting, V_{CC} UVLO, and auto-restart over-temperature protection.

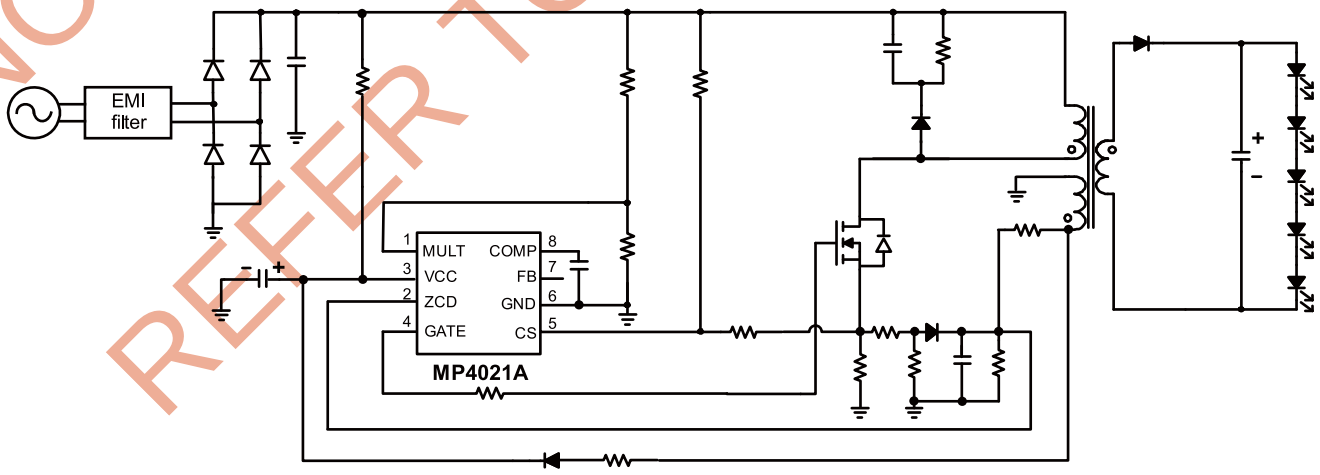
FEATURES

- Real current control without secondary-feedback circuit
- Typical ±1.5% load regulation
- Unique architecture for superior line regulation
- High power factor≥0.9 over universal input voltage
- Boundary conduction mode improves efficiency
- Ultra-low (20μA) start-up current
- Low (1mA) quiescent current
- Input UVLO
- Cycle-by-cycle current limit
- Over-voltage protection
- Short-circuit protection
- Over-temperature protection
- Available in an SOIC8 package

APPLICATIONS

- Solid-state lighting
- Industrial and commercial lighting
- Residential lighting

TYPICAL APPLICATION

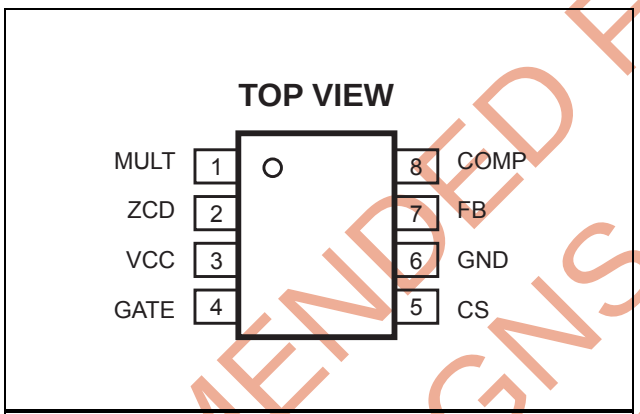


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4021GS-A	SOIC8	MP4021-A

* For Tape & Reel, add suffix –Z (e.g. MP4021GS-A–Z);

PACKAGE REFERENCE



SOIC8

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{CC} ..... -0.3V to +30V
ZCD Pin ..... -7V to +7V
Other Analog Inputs and Outputs ..... -0.3V to 7V
Max. Gate Current ..... ±1.2A
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8 ..... 1.3W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{CC} ..... 10.3V to 23V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8 ..... 96 ..... 45 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{CC} = 14V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Operating Range	V_{CC}	After turn on	10.3		23	V
Turn-on Threshold	V_{CC_ON}	V_{CC} rising edge	12.6	13.6	14.6	V
Turn-off Threshold	V_{CC_OFF}	V_{CC} falling edge	8.4	9.0	9.6	V
Hysteretic Voltage	V_{CC_HYS}			4.5		V
Supply Current						
Start-up Current	$I_{STARTUP}$	V_{CC}=11V		20	30	µA
Quiescent Current	I_Q	No switching		0.75	1	mA
Operating Current	I_{CC}	F_s =70kHz		2	3	mA
Multiplier						
Operation Range	V_{MULT}		0		3	V
Gain	K[5]			1		1/V
Error Amplifier						
Feedback Voltage	V_{FB}		0.403	0.414	0.425	V
Transconductance [6]	G_{EA}			222		µA/V
Upper Clamp Voltage	V_{COMP_H}		5.3	5.65	6	V
Lower Clamp Voltage	V_{COMP_L}		1.3	1.5	1.7	V
Max Source Current [6]	I_{COMP}			75		µA
Max Sink Current [6]	I_{COMP}			-400		µA
Current Sense Comparator						
Leading Edge Blanking Time	t_{LEB}			280		ns
Current Sense Clamp Voltage	V_{CS_CLAMP}		2.3	2.5	2.7	V
Zero Current Detector						
Zero Current Detect threshold	V_{ZCD_T}	V_{ZCD} falling edge		0.31		V
Zero Current Detect Hysteresis	V_{ZCD_HYS}			650		mV
ZCD Blanking Time	t_{LEB_ZCD}	After turn-off	1.8	2.5	3.2	µs
Over-voltage Blanking Time	t_{LEB_OVP}	After turn-off		1.5		µs
Over-voltage Threshold	V_{ZCD_OVP}	1.5µs delay after turn-off	5.1	5.4	5.7	V
Over-current Blanking Time	t_{LEB_OCP}	After turn-on, same as t_{LEB}		280		ns
Over-current Threshold	V_{ZCD_OCP}	280ns delay after turn-on	0.57	0.60	0.63	V
Minimum Off Time	t_{OFF_MIN}		2	3.5	5	µs
Starter						
Start Timer Period	t_{START}			130		µs

ELECTRICAL CHARACTERISTICS *(Continued)*

V_{CC} = 14V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate Driver						
Output Clamp Voltage	V_{GATE_CLAMP}	V_{CC}=23V	12	13.5	15	V
Minimum Output Voltage	V_{GATE_MIN}	V_{CC}=V_{CC_OFF} + 50mV	6.0			V
Max Source Current(6)	I_{GATE_SOURCE}			1		A
Max Sink Current(6)	I_{GATE_SINK}			-1.2		A

Notes:

5) The multiplier output is given by: V_{CS}=K•V_{MULT}• (V_{COMP}-1.5)

6) Guaranteed by design.

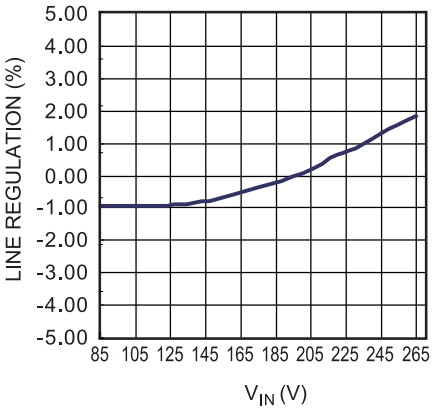
PIN FUNCTIONS

Pin #	Name	Pin Function
1	MULT	Multiplier input. Connect this pin to the tap of resistor divider from the rectified voltage of the AC line. The half-wave sinusoid signal to this pin provides a reference signal for the internal current control loop.
2	ZCD	Zero-current detection. A negative going-edge triggers the turn-on signal of the external MOSFET. Connect this pin to a resistor divider between the auxiliary winding to GND. Over-voltage condition is detected through ZCD. Every switching turn-off interval, if ZCD voltage is higher than the over-voltage-protection (OVP) threshold after the 1.5μs blanking time, the over-voltage protection will trigger and the system will stop switching until auto-restart comes. ZCD pin can also monitor over-current condition. Connect this pin thru a diode to a resistor divider between CS to GND. Every switching turn-on interval, if ZCD voltage is higher than the over-current-protection (OCP) threshold after the 280ns blanking time, the over-current protection will trigger and the system will stop switching until auto-restart comes.
3	VCC	Power supply input. This pin supplies the power for the control signal and the high-current MOSFET grade drive output. Bypass this pin to ground with an external bulk capacitor of typically 22μF in parallel with a 100pF ceramic cap to reduce noise.
4	GATE	Gate drive output. This totem pole output stage is able to drive a high-power MOSFET with a peak current of 1A source capability and 1.2A sink capability. The high level voltage of this pin is clamped to 13.5V to avoid excessive gate drive voltage. And the low level voltage is higher than 6V to guarantee enough drive capacity.
5	CS	Current sense. The MOSFET current is sensed via a sensing resistor to its source lead. The comparison between the resulting voltage and the internal sinusoidal-current reference signal determines when the MOSFET turns off. A feed-forward from the rectified AC line voltage connected to the current sense pin maximizes the line regulation. If the pin voltage is higher than the current limit threshold of 2.5V (after turn-on blanking) the gate drive will turn off.
6	GND	Ground. Current return for the control signal and the gate drive signal.
7	FB/NC	Feedback signal. Leave this pin floating (NC) for primary-side control.
8	COMP	Loop compensation input. Connect a compensation network to stabilize the LED drive and maintain an accurate LED current.

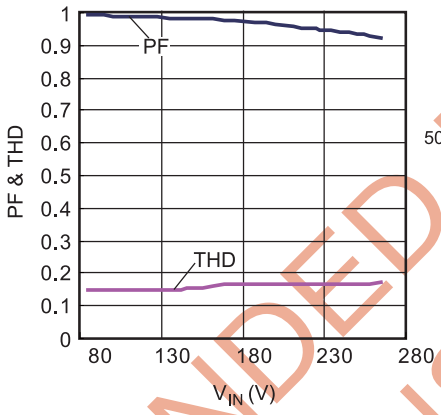
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =110V_{AC}/220V_{AC}, 5 LEDs in series, I_{LED}=500mA, Lm=2.2mH, N_P:N_S:N_{AUX} =144:24:27, unless otherwise noted.

Line Regulation

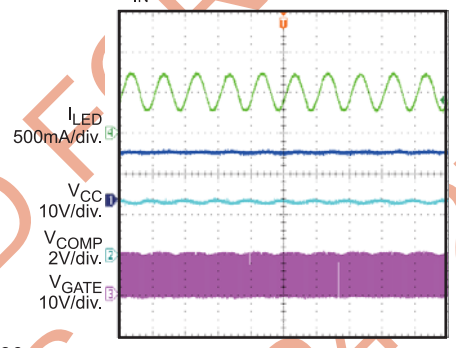


PF & THD vs. V_{IN}



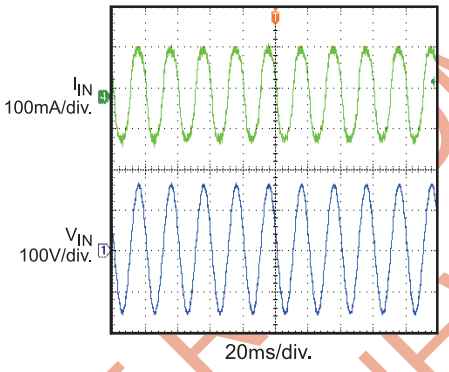
Steady State

V_{IN}=110V



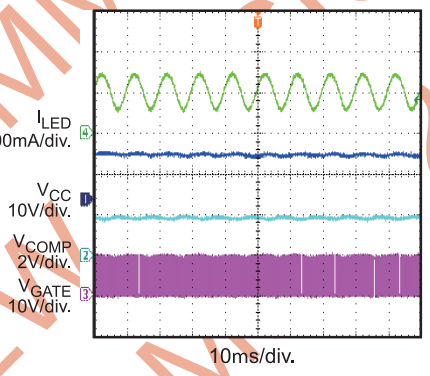
Steady State

V_{IN}=110V



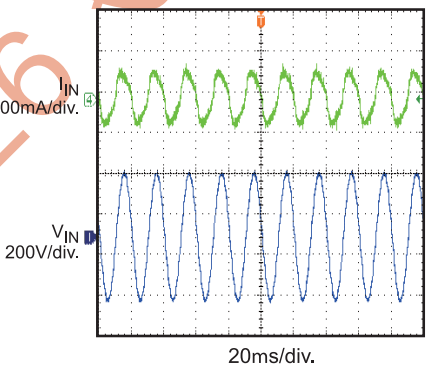
Steady State

V_{IN}=220V



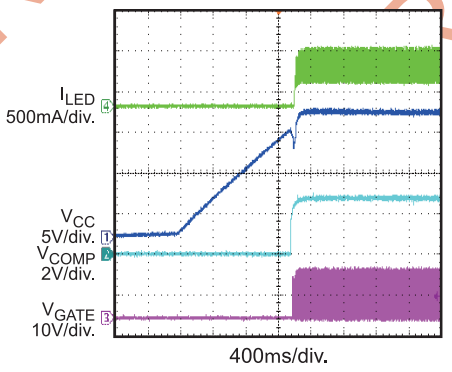
Steady State

V_{IN}=220V



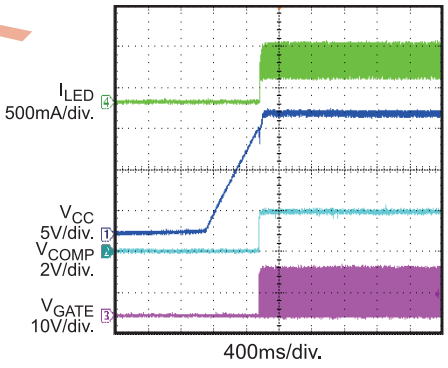
V_{IN} Startup

V_{IN}=110V



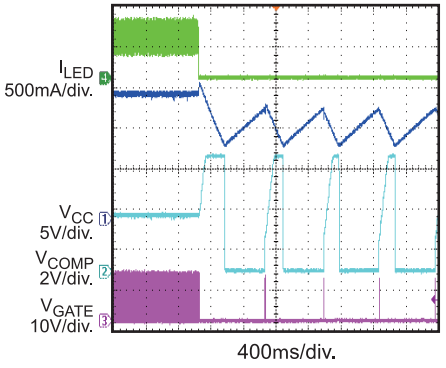
V_{IN} Startup

V_{IN}=220V



Open LED Protection

V_{IN}=110V, Open LED @ working

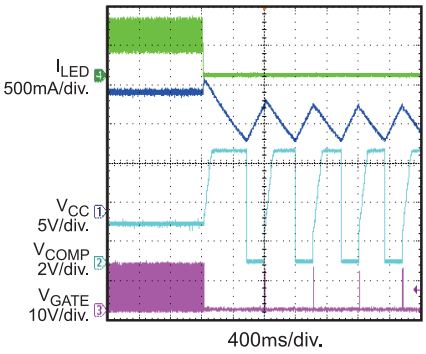


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =110V_{AC}/220V_{AC}, 5 LEDs in series, I_{LED}=500mA, Lm=2.2mH, N_P:N_S:N_{AUX} =144:24:27, unless otherwise noted.

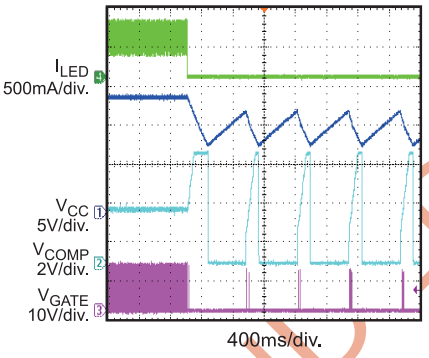
Open LED Protection

V_{IN}=220V, Open LED @ working



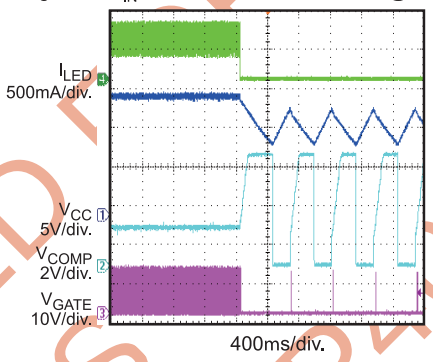
Short Circuit Protection

V_{IN}=110V, Short LED+ to LED- @ working



Short Circuit Protection

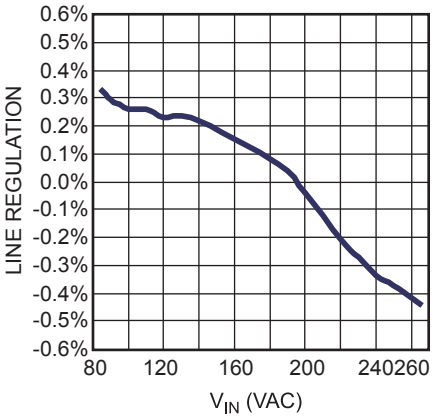
V_{IN}=220V, Short LED+ to LED- @ working



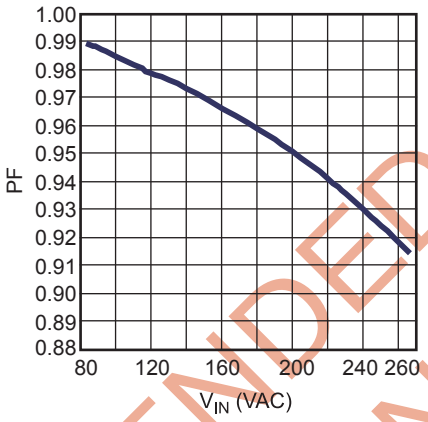
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =110V_{AC}/220V_{AC}, V_{OUT}=30V, I_{OUT_MAX}=330mA, Constant Voltage Control, Lm=2.4mH, N_P:N_S:N_{AUX}=205:41:27, unless otherwise noted.

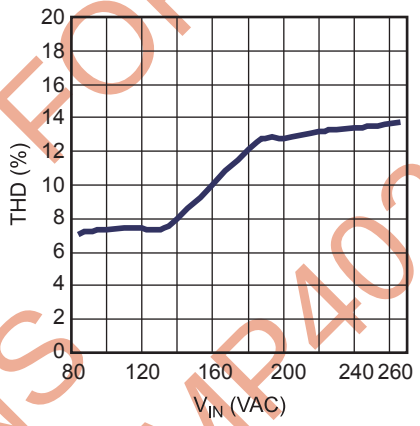
Line Regulation



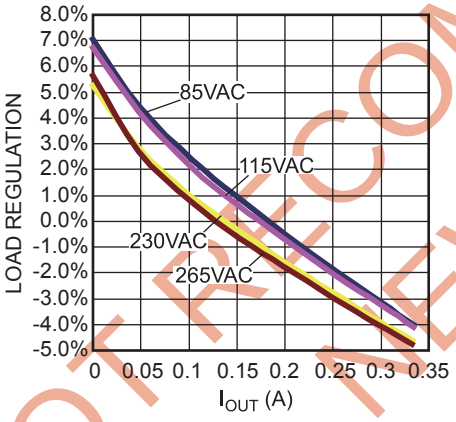
PF vs. V_{IN} @ Full-Load



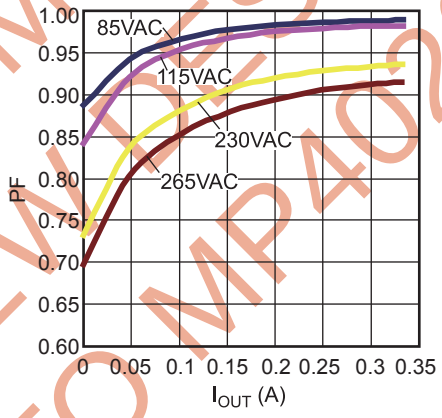
THD vs. V_{IN} @ Full-Load



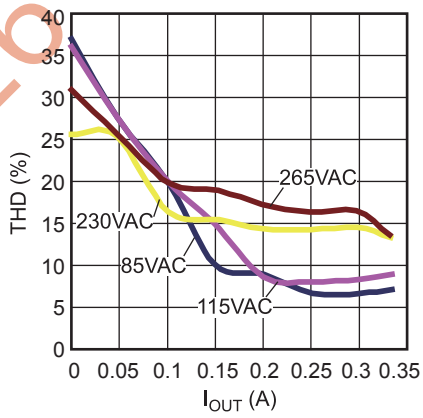
Load Regulation



PF vs. I_{OUT}



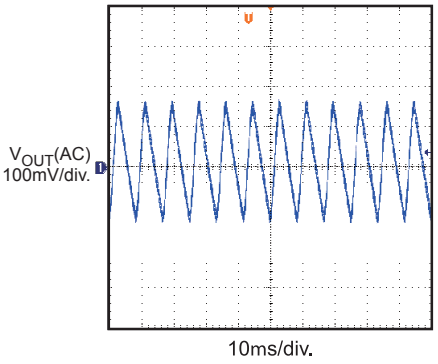
THD vs. I_{OUT}



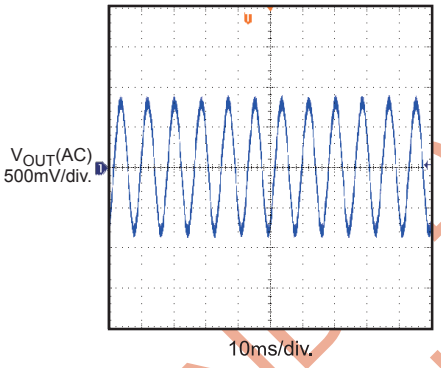
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =110V_{AC}/220V_{AC}, V_{OUT}=30V, I_{OUT_MAX}=330mA, Constant Voltage Control, Lm=2.4mH, N_P:N_S:N_{AUX}=205:41:27, unless otherwise noted.

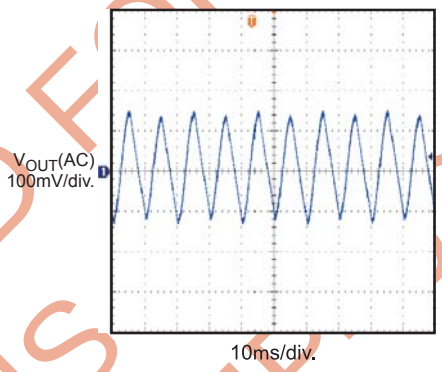
Output Voltage Ripple
V_{IN} = 110V, No Load



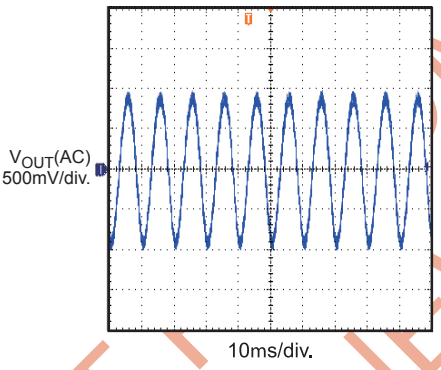
Output Voltage Ripple
V_{IN} = 110V, Full Load



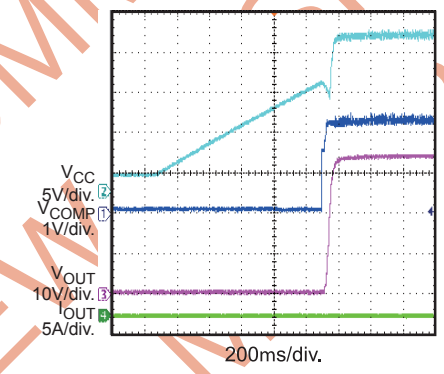
Output Voltage Ripple
V_{IN} = 220V, No Load



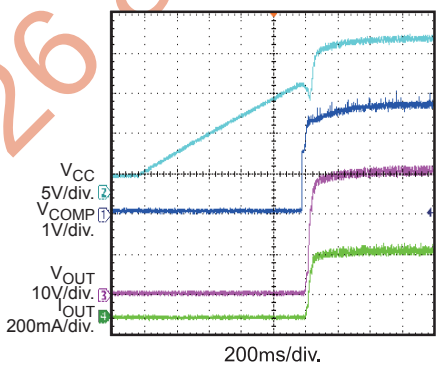
Output Voltage Ripple
V_{IN} = 220V, Full Load



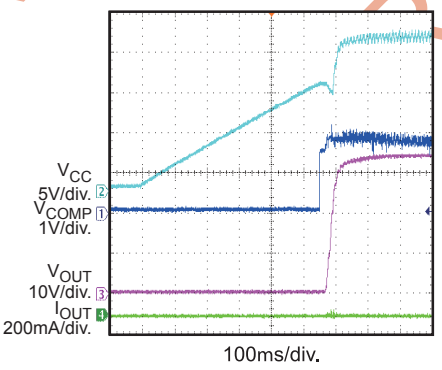
Start-Up
V_{IN} = 110V, No Load



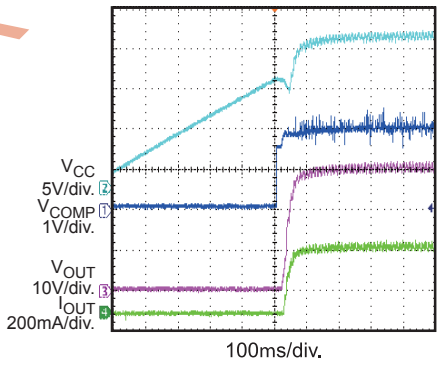
Start-Up
V_{IN} = 110V, Full Load



Start-Up
V_{IN} = 220V, No Load



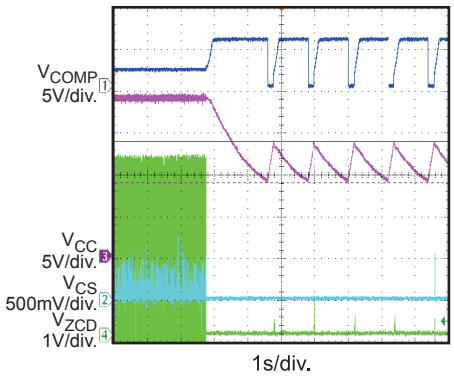
Start-Up
V_{IN} = 220V, Full Load



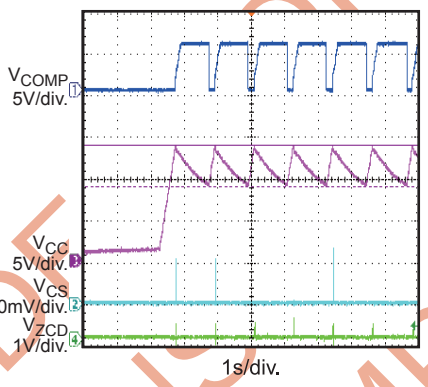
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =110V_{AC}/220V_{AC}, V_{OUT}=30V, I_{OUT_MAX}=330mA, Constant Voltage Control, Lm=2.4mH, N_P:N_S:N_{AUX}=205:41:27, unless otherwise noted.

Short Circuit Protection
V_{IN} = 265V, Short Circuit @ Working



Short Circuit Protection
V_{IN} = 265V, Short Circuit @ Start-Up



FUNCTION DIAGRAM

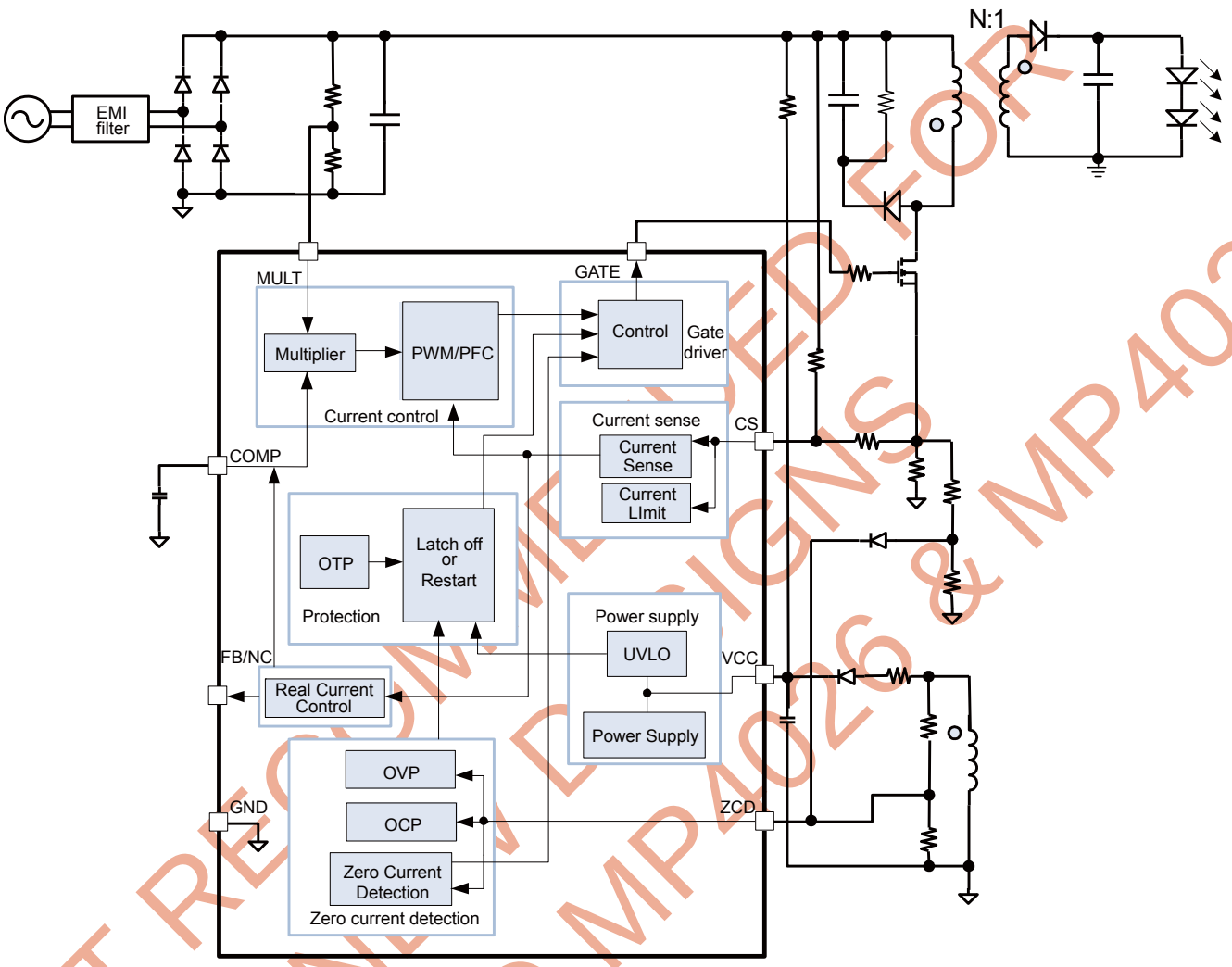


Figure 1—MP4021A Function Block Diagram

OPERATION

The MP4021A is a primary-side control offline LED controller which incorporates all the features for high-performance LED lighting. The LED current can be accurately controlled with the real current control method from the primary-side information. Active Power Factor Correction (PFC) eliminates unwanted harmonic noise to pollute the AC line.

Start Up

Initially, VCC of the MP4021A is charged through the start up resistor from the AC line. When VCC reaches 13.6V, the control logic works and the gate drive signal begins to switch. Then the power supply is taken over by the auxiliary winding.

The MP4021A will shut down when VCC drops below 9V.

Boundary Conduction Mode Operation

During the external MOSFET on time (t_{ON}), the rectified input voltage (V_{BUS}) applies to the primary-side inductor (Lm), and the primary current (I_{pri}) increases linearly from zero to the peak value (I_{pk}). When the external MOSFET turns off, the energy stored in the inductor is transferred to the secondary-side and turns on the secondary-side diode to power the load. The secondary current (I_{sec}) begins to decrease linearly from the peak value to zero. When the secondary current decreases to zero, the primary-side leakage inductance, magnetizing inductance and all the parasitic capacitances decrease the MOSFET drain-source voltage—this decrease is also reflected on the auxiliary winding (see Figure 2). The zero-current detector in the ZCD pin generates the turn-on signal of the external MOSFET when the ZCD voltage falls below 0.31V (see Figure 3).

As a result, there are virtually no primary-switch turn-on losses and no secondary-diode reverse-recover losses. It ensures high efficiency and low EMI noise.

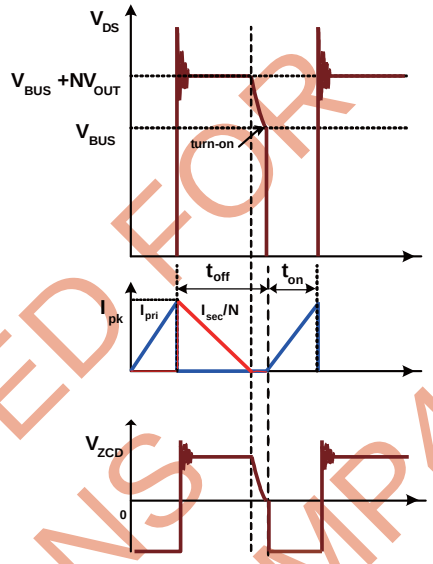


Figure 2—Boundary Conduction Mode

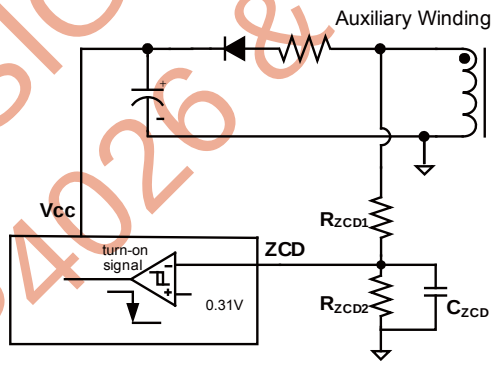


Figure 3—Zero Current Detector

Real Current Control

The proprietary real-current control method allows the MP4021A to control the secondary-side LED current from primary-side information. The mean output LED current can be calculated approximately as:

$$I_o \approx \frac{N \cdot V_{FB}}{2 \cdot R_s}$$

N—Turn ratio of primary side to secondary side

V_{FB}—The feedback reference voltage (typical 0.4V)

R_s—The sensing resistor connected between the MOSFET source and GND.

Power Factor Correction

The MULT pin is connected to the tap of the resistor divider from the rectified instantaneous line voltage and fed as one input of the Multiplier. The output of the multiplier will be shaped as sinusoid too. This signal provides the reference for the current comparator and comparing with the primary side inductor current which sets the primary peak current shaped as sinusoid with the input line voltage. High power factor can be achieved.

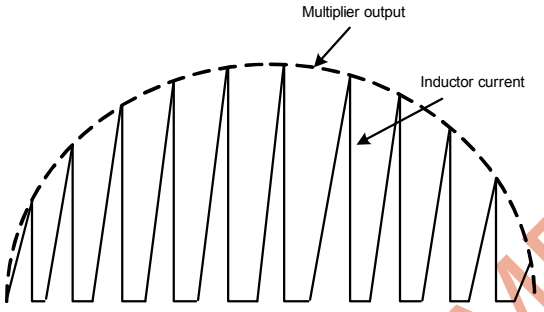


Figure 4—Power Factor Correction Scheme

The maximum voltage of the multiplier output to the current comparator is clamped to 2.5V to get a cycle-by-cycle current limitation.

VCC Under-voltage Lockout

When the VCC voltage drops below UVLO threshold 9V, the MP4021A stops switching and totally shuts down, the VCC will restart charging by the external start up resistor from AC line. Figure 5 shows the typical waveform of VCC under-voltage lockout

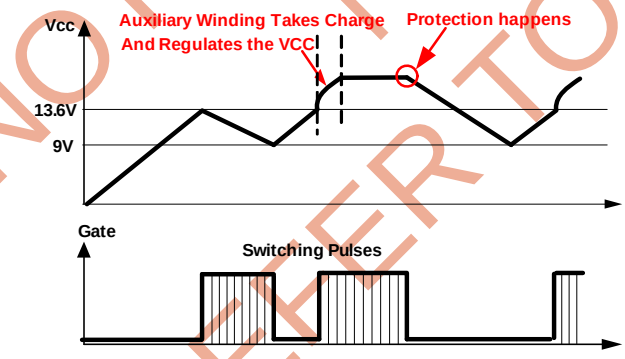


Figure 5—VCC Under-Voltage Lockout

Auto Starter

The MP4021A integrates an auto starter, the starter starts timing when the MOSFET is turned off, if ZCD fails to send out another turn on signal after 130μs, the starter will automatically send out the turn on signal which can avoid the IC unnecessary shut down by ZCD missing detection.

Minimum Off Time

The MP4021A operates with variable switching frequency, the frequency is changing with the input instantaneous line voltage. To limit the maximum frequency and get a good EMI performance, MP4021A employs an internal minimum off time limiter—3.5μs, show as Figure 6.

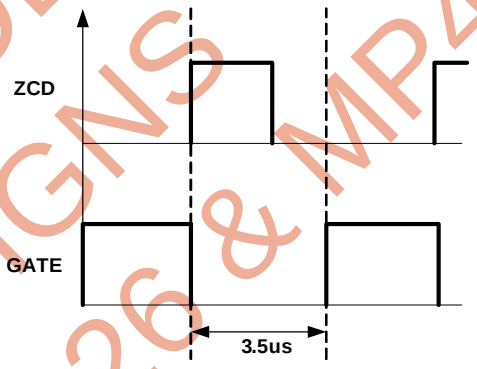


Figure 6—Minimum Off Time

Leading Edge Blanking

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance discharging at MOSFET turning on, an internal leading edge blanking (LEB) unit is employed between the CS Pin and the current comparator input. During the blanking time, the path, CS Pin to the current comparator input, is blocked. Figure 7 shows the leading edge blanking.

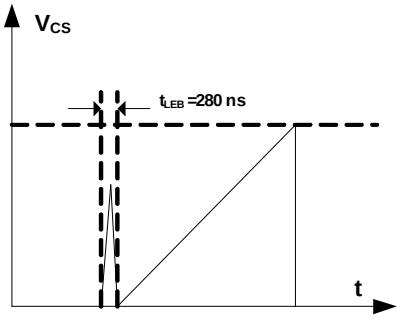


Figure 7—Leading Edge Blanking

Output Over-Voltage Protection (OVP)

Output over voltage protection can prevent the components from damage in the over voltage condition. The positive plateau of auxiliary winding voltage is proportional to the output voltage, the OVP uses the auxiliary winding voltage instead of directly monitoring the output voltage, the OVP sample is shown in Figure 8. Once the ZCD pin voltage is higher than 5.4V, the OVP signal will be triggered and latched, the gate driver will be turned off and the IC work at quiescent mode, the VCC voltage dropped below the UVLO which will make the IC shut down and the system restarts again. The output OVP setting point can be calculated as:

$$V_{OUT\_OVP} \cdot \frac{N_{AUX}}{N_{SEC}} \cdot \frac{R_{ZCD2}}{R_{ZCD1}+R_{ZCD2}} = 5.4V$$

V_{OUT_OVP}—Output over voltage protection point

N_{AUX}—The auxiliary winding turns

N_{SEC}—The secondary winding turns

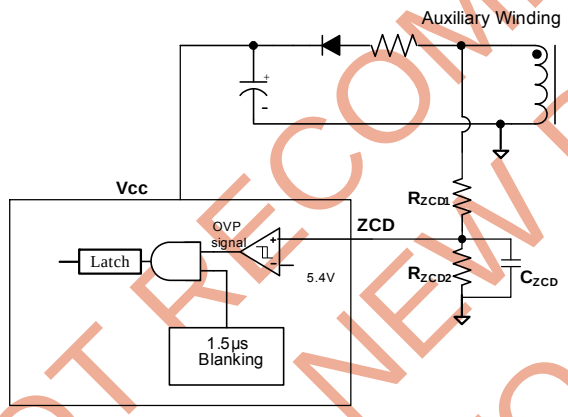


Figure 8—OVP Sample Unit

To avoid the mis-trigger OVP by the oscillation spike after the switch turns off, the OVP sampling has a t_{LEB_OVP} blanking period, typical 1.5µs, shown in Figure 9.

The current-limiting resistor between the output of the aux-winding and the ZCD resistor divider can also work as suppresser to avoid the OVP mis-trigger.

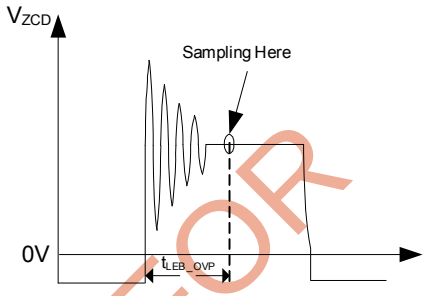


Figure 9—ZCD Voltage and OVP Sample

Output Short Circuit Protection

The MP4021A clamps the CS pin voltage to less than 2.5V to limit the available output power. If the short circuit of the secondary-side occurs, the voltage of the auxiliary winding will fall down following the voltage of the secondary winding and the VCC drops to less than UV threshold and re-start the system.

As supplementary, tie a resistor divider form CS sensing resistor to ZCD pin, shown in Figure 10. When the power MOSFET in the primary-side is turned on, the ZCD pin monitors the rising primary-side current, once the ZCD pin reaches OCP threshold, typical 0.6V, the gate driver will be turned off to prevent the chip form damage and the IC works at quiescent mode, the VCC voltage dropped below the UVLO which will make the IC shut down and the system restarts again. Please note that the value of the resistors to set the OCP threshold (R_{OCP1} & R_{OCP2}) should be much smaller than those of the ZCD zero-current detector (R_{ZCD1} & R_{ZCD2})

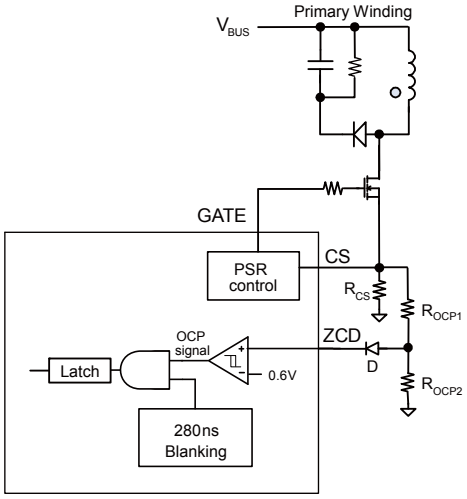


Figure 10—OCP Sample Unit

The primary-side OCP setting point can be calculated as:

$$I_{PRI\_OCP} \cdot R_{CS} \cdot \frac{R_{OCP2}}{R_{OCP1} + R_{OCP2}} - V_D = 0.6V$$

I_{PRI_OCP}—Primary-side over current protection point.

For some applications, the primary-side inductance value is very small, the minimal-off time feature could make the system work in DCM at the zero-crossing of the BUS voltage. To improve the OCP function in this condition, please remove C_{ZCD} and reduce the value of R_{ZCD1} and R_{ZCD2} proportionally.

Thermal Shut Down

To prevent from any lethal thermal damage, when the inner temperature exceeds OTP threshold, the MP4021A shuts down switching cycle and latched until VCC drop below UVLO and restart again.

Compensation for Wide Output Voltage

For wide output voltage applications, sample VCC level thru a resistor to COMP pin. Since the output voltage of AUX-winding follows the output voltage, the resistor can import output voltage information to COMP level to compensate the LED current variation with different LED voltage drop. The typical COMP source current is only 75μA and the tolerance could affect the action of the compensation. So the inject current form VCC should be smaller than 10μA. The compensation resistor should be larger than 3MΩ.

Design Example

For the design example, please refer to MPS application note AN059 for the detailed design procedure and information.

PRIMARY-SIDE CONSTANT-VOLTAGE CONTROL

For LED lighting application, a single-stage PFC converter needs large output capacitor to reduce the 100Hz ripple. On the other hand, the two-stage solution is also proposed to remove the 100Hz ripple from the LED current. Figure 11 shows a two-stage solution system based on MP4021A and MP2489, offline isolated PFC flyback constant-voltage regulator plus DC to DC LED driver.

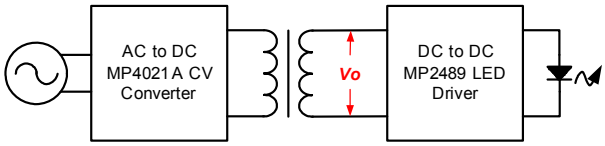


Figure 11—Two-stage LED Driver Solution

The MP4021A can be designed as a primary-side constant-voltage control, offline isolated flyback controller with Active Power Factor Correction (PFC). The output voltage V_O can be regulated without opto-coupler under a wide AC main input voltage range in a single-stage flyback converter.

Primary-side Voltage Control

The MP4021A can implement feedback control function with FB pin.

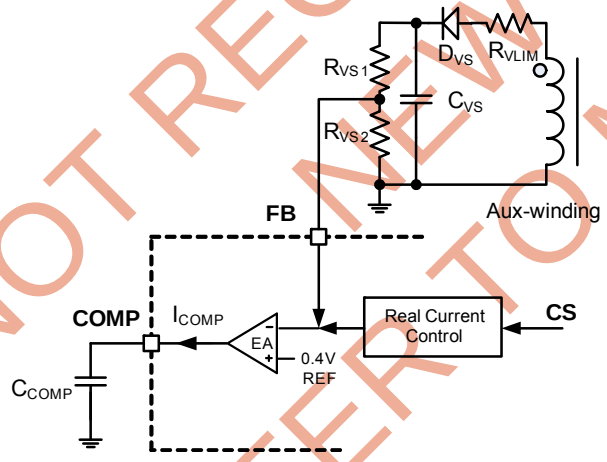


Figure 12—FB Pin Structure

Shown in Figure 12, the FB signal is fed to the error amplifier and comparing with the 0.4V reference. So, at steady state, the average value of FB level will be regulated at 0.4V. The Real Current Control block's output is internally connected to FB with about 200kΩ impedance, if there is no other external feedback signal on FB pin, the sample signal from CS pin is regulated. If there is external FB signal with low input impedance (<20kΩ) applied in FB pin, the external FB signal is regulated. This feature makes the MP4021A suitable both for primary side control application without other feedback signals and direct control application with external feedback signal applied.

The FB pin is used to regulate the output voltage by sampling the aux-winding. As a flyback converter, during the flyback period, the primary MOSFET is off and the secondary diode is conducting current. Before the secondary current drops to zero, the aux-winding voltage is proportional to the output voltage.

$$V_{AUX} = \frac{N_{AUX}}{N_{SEC}} \cdot V_O$$

A simple D-R-C circuitry sample-holds the aux-winding voltage and a resistor divider reduces the amplitude to match the internal 0.4V reference. So the output voltage can be calculated as:

$$V_O = \frac{N_{SEC}}{N_{AUX}} \cdot \frac{R_{VS1} + R_{VS2}}{R_{VS2}} \cdot V_{REF}$$

The current-limit resistor R_{VLIM} helps to attenuate the energy of the leakage inductance to improve the voltage regulation precision.

Power Factor Correction

Same as CC mode, the MULT pin is connected to the tap of the resistor divider from the rectified instantaneous line voltage and fed as one input of the multiplier. The COMP level, which is regulated from the feedback signal, is fed as the other input of the internal multiplier. The output of the multiplier will be shaped as sinusoid wave too. This signal provides the reference for the current comparator and comparing with the primary side inductor current which sets the primary peak current shaped as sinusoid with the input line voltage. High power factor can be achieved.

Primary Inductor Current Detection

The system is based on the peak current mode control. A sensing resistor is tied from the Source of the MOSFET and ground to sample the primary inductor peak current. Different from working in CC mode, since the MP4021A regulates the FB signal, the Real Current Control signal from CS pin is shielded. The CS pin is just applied as primary peak current detector like traditional CV converter.

Tuning the value of the CS sensing resistor can change the COMP level. With larger sensing resistor, the COMP level is higher and with smaller sensing resistor, the COMP level is lower. So, select a suitable sensing resistor to avoid the COMP level to trigger Upper/Lower COMP Voltage.

In order to avoid hitting the current limit, the voltage across the sensing resistor should be less than 80% of the worst case current limit voltage. And the clamp voltage on CS pin is typical 2.5V.

Loop Compensation

Unlike voltage mode has only a single pole roll off due to the output filter, the MP4021A uses peak-current-mode control to achieve more stable control loop.

Since MP4021A is designed with PFC feature, so the loop response is very slow with large COMP cap. For Primary-side CC mode, the part samples the primary-side current. With large output cap, although the output voltage builds up slowly, the primary current should be not small, so the COMP cap can not be charged to overshoot. For CV mode control, the feedback voltage is from the output voltage of the aux-winding, which reflects the output voltage of the secondary winding at flyback period. The impact of the slow loop response results in that the COMP level is easy to be charged to overshoot or drops to normal level slowly.

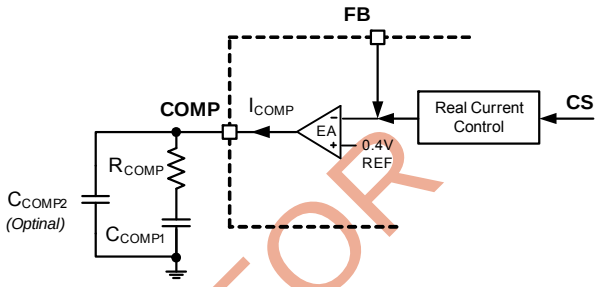


Figure 13—COMP Pin Structure

A series capacitor-resistor combination net sets a pole-zero combination to control the characteristics of the control system.

The C_{COMP1} is a big-value capacitor (2.2μF to10μF) to achieve high PF and stable loop. The R_{COMP1} in series with C_{COMP} adds a zero in the loop to improve the phase margin, it is helpful to limit the start-up voltage spike. As an option, a small-value capacitor C_{COMP2} can also be applied to add a high-frequency pole to achieve a beneficial effect of attenuating high-frequency noise.

Feedforward Compensation

In order to limit the output voltage spike and improve the voltage regulation, adding feed-forward compensation from aux-winding feedback voltage to CS pin, shown in Figure 14,

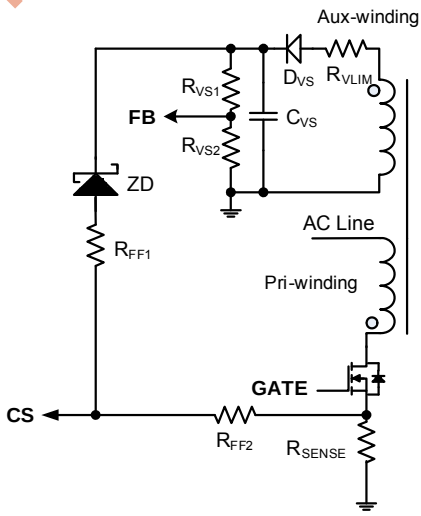


Figure 14—The Feedforward Compensation on CS Pin

The higher output voltage is, the higher feed-forward offset is. The Zener Diode is used to set the compensation trigger level. The resistor divider of R_{FF1} and R_{FF2} adjusts the action. Once the output voltage rises up too high, the aux-winding output also rises up to break the ZD to add a feedforward bias on CS pin, then the primary current is reduced quickly to prevent the output voltage from rising to the higher level further. With lower zener voltage range, the effect of the feedfoward compensation is enhanced, but the power loss is increased.

Dummy Load

For primary constant voltage control, sensing the output voltage requires the secondary diode conducts current, when the system is delivering power to the output. When the load is very light, the power consuming is very small. The conduction of the secondary diode becomes very short. The FB signal is hard to be coupled with the real output voltage. So the output voltage rises up to trigger OVP. The feedforward compensation greatly reduces the power delivered to output but a dummy load is still required to dissipate the remaining power to limit the voltage rising further. As a result, the dummy load increases the power loss of whole system to achieve the desired load regulation precision.

Protection

Different from CC mode control, CV mode makes the system can work in no load condition. So the OVP can not be triggered at normal operation. But the MP4021A can still set a OVP threshold thru ZCD R-divider to prevent the components from damage in fault cases.

Other protection mechanisms, like SCP, OTP, cycle by cycle current limit, are all same as working in CC mode.

TYPICAL APPLICATION CIRCUIT

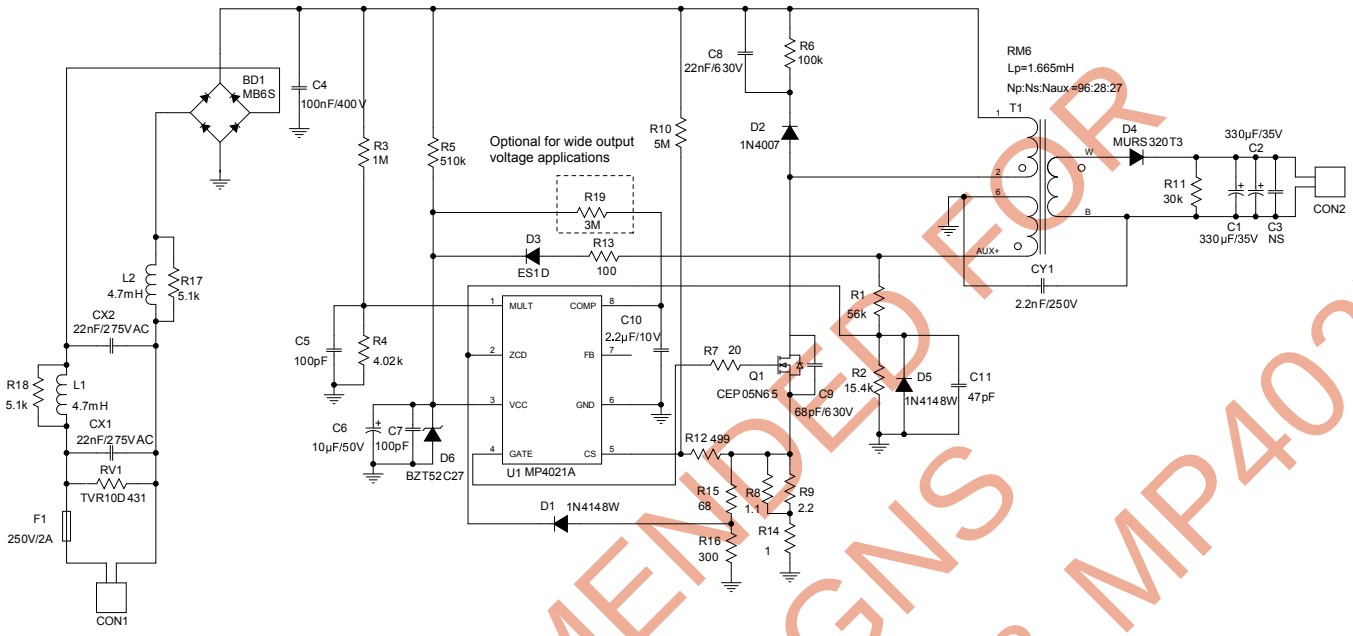


Figure 15—Universal Input, Isolated Flyback Converter, Drive 3-6 LEDs in Series, 350mA LED Current for LED Bulb Lighting

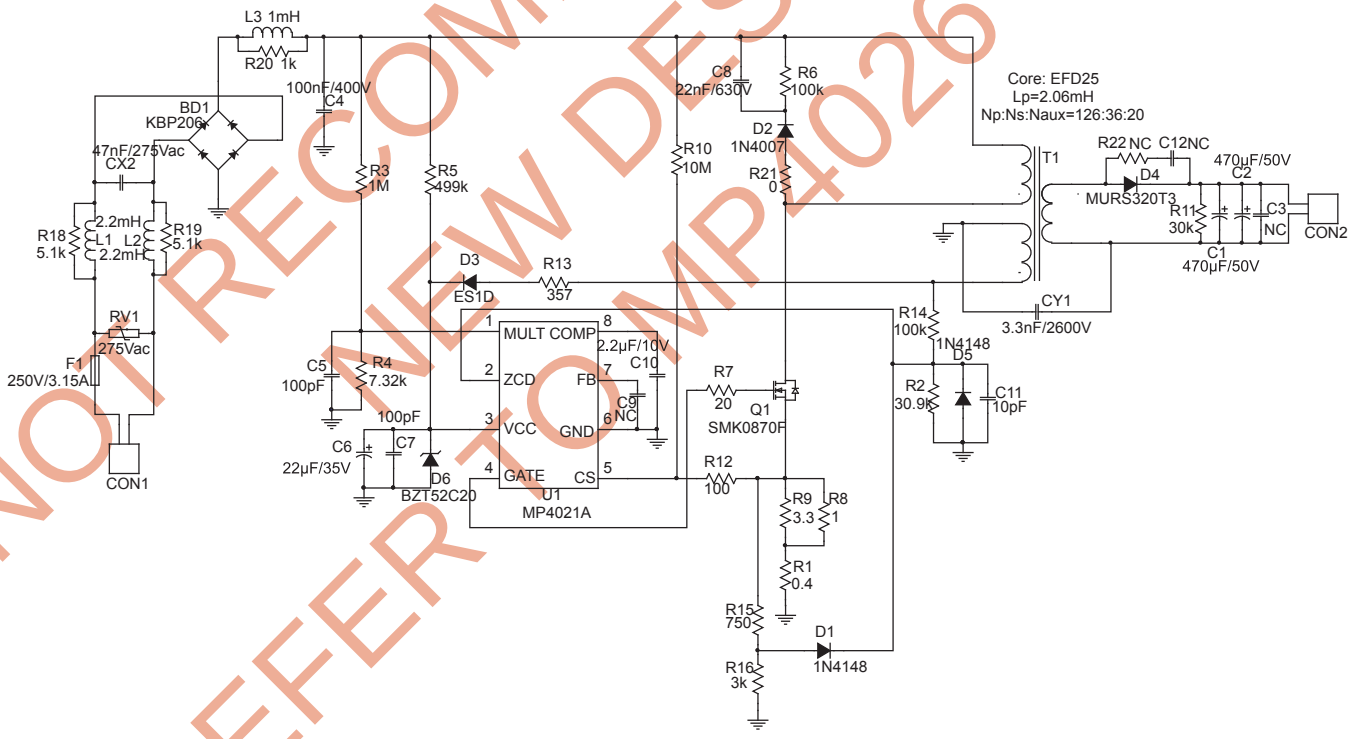


Figure 16—Universal Input, Isolated Flyback Converter, Drive 9 LEDs in Series, 500mA LED Current for 15W LED Tube Lighting

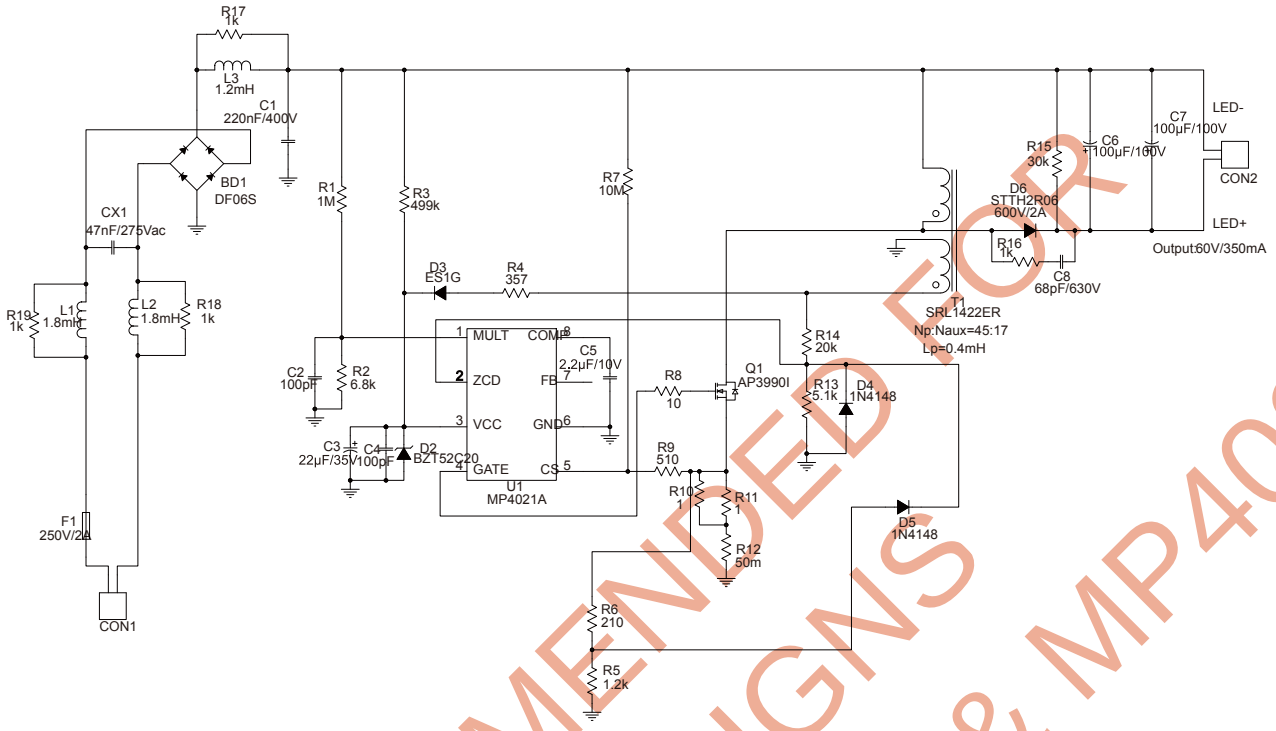


Figure 17—Universal Input, Non-isolated Buck-boost Converter, Drive 19 LEDs in Series, 350mA LED Current for 21W LED Tube Lighting

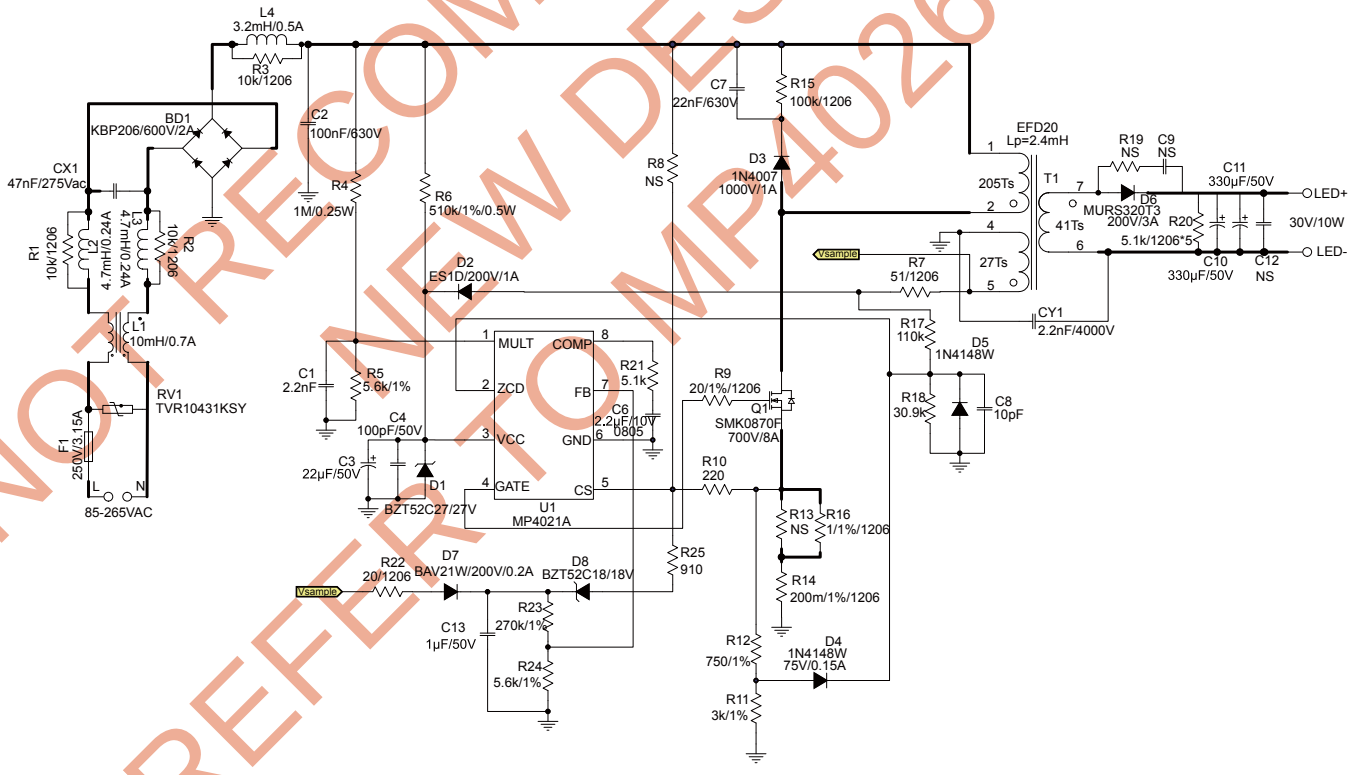
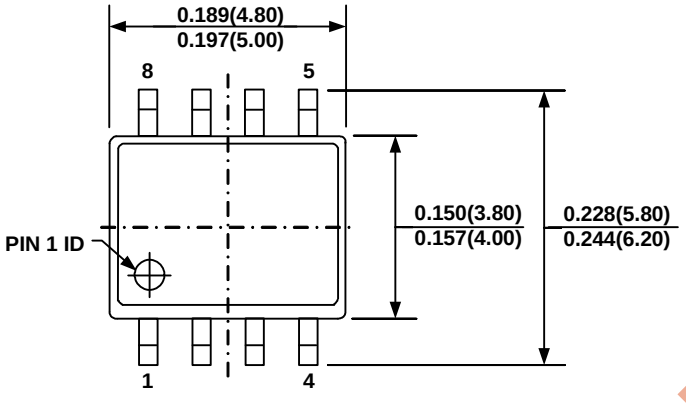


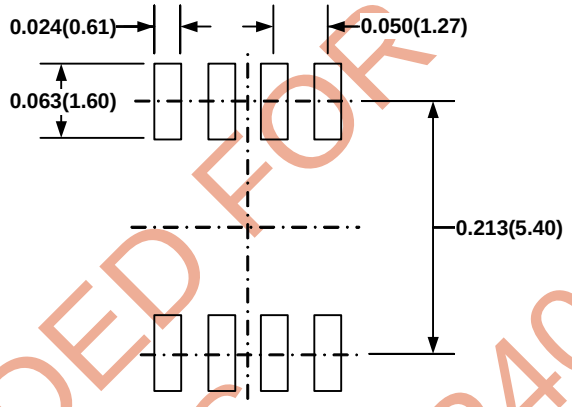
Figure 18—Universal Input, isolated Flyback Converter, Primary Constant Voltage Control, 30V/10W Output

PACKAGE INFORMATION

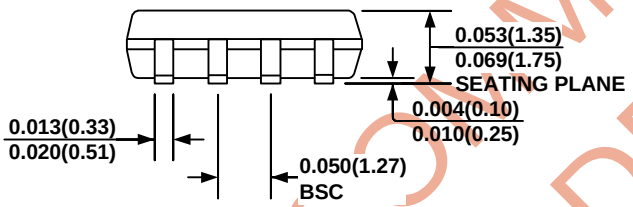
SOIC8



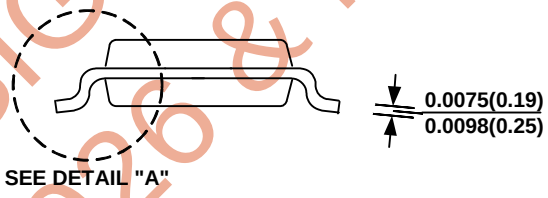
TOP VIEW



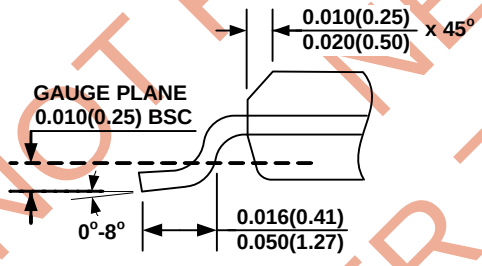
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.