MP3921

Single-Port, IEEE 802.3af/at PSE Controller for Power over Ethernet

DESCRIPTION

The MP3921 is a single-port power-sourcing equipment (PSE) power controller for IEEE 802.3af/at-compliant power over Ethernet (PoE) applications.

The MP3921 includes all the functions of IEEE 802.3af/at, including detection, single-event and two-event classification, current limiting, and disconnected load detection. All the functions can be configured to work in automatic mode or software configuration mode via the I²C.

The MP3921 features a 9-bit analog-to-digital converter (ADC) to monitor the current and voltage, a special I²C interface for isolated controller communication, adjustable current limits, and configurable system functions. These features provide flexibility for PoE applications.

The MP3921 is available in a QFN-32 (5mmx5mm) package.

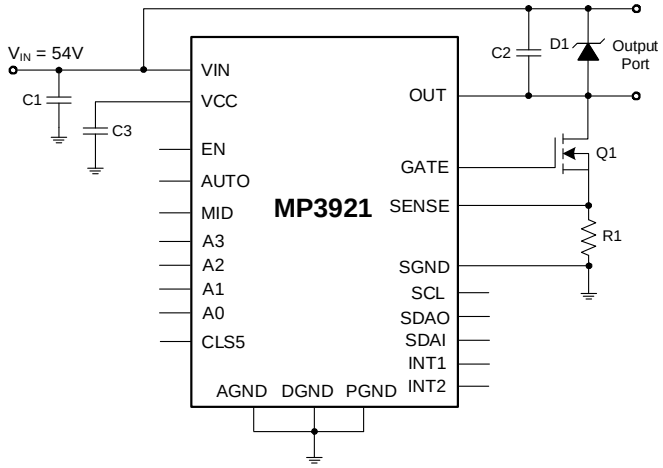
FEATURES

- IEEE802.3af/at Compliant
- 0.25Ω Current-Sense Resistor (R_{SENSE})
- Automatic Mode and I²C Command Control Mode
- Internal VCC Power Supply
- Three-Wire I²C Interface for Isolated Applications
- Two INT Pins for Interrupt Priority Selection
- Disconnected DC Load Detection
- Instantaneous Current/Voltage Readout
- Configurable I²C Address
- Thermal Protection
- Available in a QFN-32 (5mmx5mm) Package

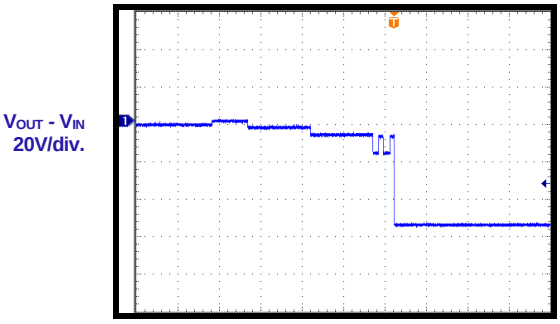
APPLICATIONS

- Power-Sourcing Equipment (PSE) Switches/Routers
- PSE Midspan Power Injectors
- Surveillance Network Video Recorders (NVRs) and Digital Video Recorders (DVRs)

TYPICAL APPLICATION



Start-Up for Class 4 PD



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP3921GU*	QFN-32 (5mmx5mm)	*See Below*	2

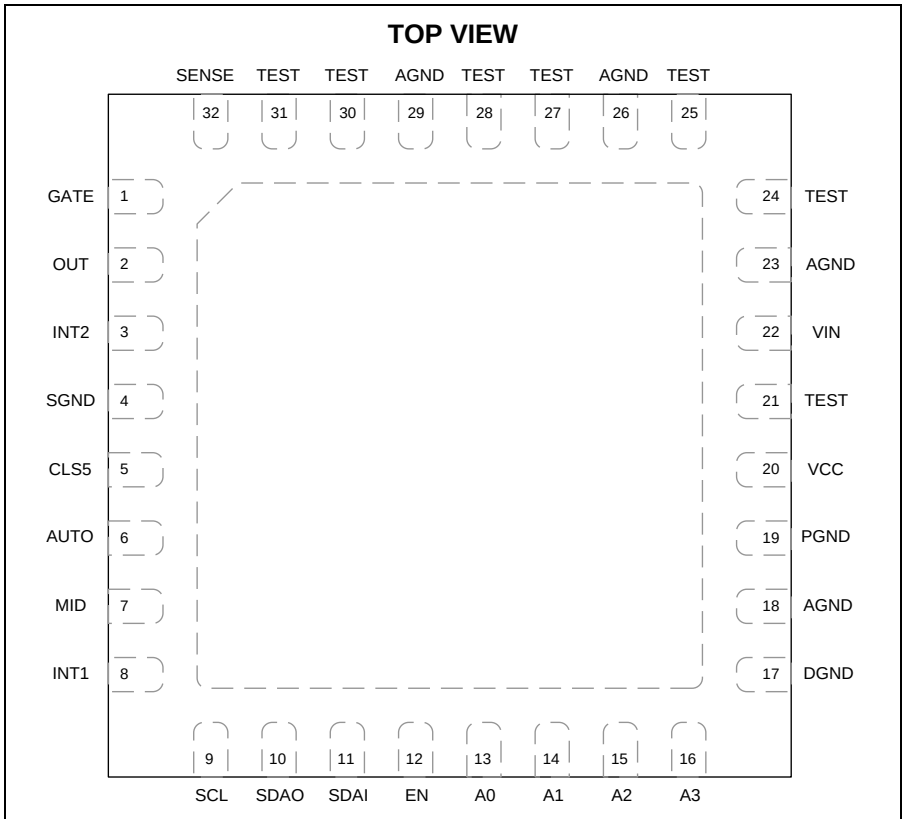
* For Tape & Reel, add suffix -Z (e.g. MP3921GU-Z).

TOP MARKING

MPSYYWW
MP3921
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP3921: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE



QFN-32 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	GATE	**MOSFET gate driver.**
2	OUT	**Output voltage sense.** Connect the OUT pin to the output interface return for detecting, classifying, voltage sensing, and current-limit foldback control.
3	INT2	**High-priority interrupt request.** The INT2 pin pulls low when the selected high-priority interrupt source register is set and the interrupt is enabled. INT2 is an open-drain output. Connect INT2 to DGND if the interrupt function is not used.
4	SGND	**Current-sense negative input.** Connect the SGND pin to the low-side terminal of the sense resistor. For accurate current sense, Kelvin connect SGND to the PCB.
5	CLS5	**Class 5 enable input.** The CLS5 pin is pulled down internally to DGND through a 50kΩ resistor. Leave CLS5 disconnected to disable the classification for Class 5 devices (IEEE 802.3at-compliant mode). Connect CLS5 to VCC to enable the classification of Class 5 devices. CLS5's status is latched when the device starts up, or after a reset condition. If CLS5's status changes after start-up, then there is no effect.
6	AUTO	**Automatic mode setting.** The AUTO pin is pulled up internally to VCC through a 50kΩ resistor (an external 10kΩ resistor can be added). Float AUTO to set automatic mode as the default. Connect AUTO to DGND to set shutdown mode as the default. AUTO's status is latched when the device starts up, or after a reset condition. If AUTO's status changes after start-up, then there is no effect.
7	MID	**Midspan mode setting.** The MID pin is pulled up internally to VCC through a 50kΩ resistor (an external 10kΩ resistor can be added). Float MID to enter midspan mode, then wait 2.8s to reinitiate detection. Connect MID to DGND to disable midspan mode. MID's status is latched when the device starts up, or after a reset condition. If MID's status changes after start-up, then there is no effect.
8	INT1	**Interrupt request for all interrupt source events.** The INT1 pin pulls low when the interrupt register is set and the interrupt function is enabled. INT1 is an open-drain output. Connect INT1 to DGND if the interrupt function is not used.
9	SCL	**I^2C clock input.** Connect the SCL pin to VCC using an external pull-up resistor (typically 4.7kΩ). Connect SCL to VCC if the I^2C interface is not used.
10	SDAO	**I^2C serial data output.** The SDAO pin is an open-drain output. Connect SDAO to VCC using an external pull-up resistor (typically 4.7kΩ). Connect SDAO to SDAI for non-isolated applications. Connect SDAO to DGND if the I^2C interface is not used.
11	SDAI	**I^2C serial data input.** Connect the SDAI pin to VCC using an external pull-up resistor (typically 4.7kΩ). Connect SDAI to SDAO for non-isolated applications. Connect SDAI to DGND if the I^2C interface is not used.
12	EN	**Enable input.** The EN pin turns all internal circuits and the port (except the VCC regulator) on and off. To turn on the device automatically, externally connect EN to VCC.
13	A0	**Address setting 0 for the MP3921.** Connect the A0 pin to VCC or DGND to set the lower 4-bit address bits (address = 010 A3 A2 A1 A0). The address signal is latched when the device starts up or is reset. A0 is pulled up internally to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added).
14	A1	**Address setting 1 for the MP3921.** Connect the A1 pin to VCC or DGND to set the lower 4-bit address bits (address = 010 A3 A2 A1 A0). The address signal is latched when the device starts up or is reset. A1 is pulled up internally to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added).

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
15	A2	**Address setting 2 for the MP3921.** Connect the A2 pin to VCC or DGND to set the lower 4-bit address bits (address = 010 A3 A2 A1 A0). The address signal is latched when the device starts up or is reset. A2 is pulled up internally to VCC through a 50kΩ resistor (an external 10kΩ resistor can be added).
16	A3	**Address setting 3 for the MP3921.** Connect the A3 pin to VCC or DGND to set the lower 4-bit address bits (address = 010 A3 A2 A1 A0). The address signal is latched when the device starts up or is reset. A3 is pulled up internally to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added).
17	DGND	**Ground of the internal digital and analog circuit.**
18, 23, 26, 29	AGND	**Analog ground.** The AGND pin must be connected to DGND in application.
19	PGND	**Ground of the input power supply.**
20	VCC	**3.3V internal regulator output for the analog and digital circuit supply.** A minimum 1µF ceramic capacitor must be placed between the VCC and DGND pins.
21, 24, 25, 27, 28, 30, 31	TEST	**Test pin for factory.** The TEST pin must be floated in application.
22	VIN	**Power supply input for VCC and the output.** Bypass the VIN pin with a minimum of one ceramic capacitor (0.1µF/100V) placed between VIN and PGND.
32	SENSE	**Current sense from the high-side sense resistor terminal.** It is recommended to use a 0.25Ω sense resistor for all applications. For accurate current sense, Kelvin connect the SENSE pin during PCB layout.

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +80V
OUT .....-0.3V to V_{IN} + 0.3V
GATE, SENSE.....-0.3V to +22V
DGND, AGND, SGND.....-0.3V to +0.3V
All other pins except TEST .....-0.3V to +6.5V
INT1, INT2, SDAO maximum sink current……..
……..20mA
Continuous power dissipation (T_A = 25°C)
……..2.7W (2) (4)
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±1000V
Charged-device model (CBM) ..... ±2000V

Recommended Operating Conditions (3)

V_{IN}……44V to 57V
INT1, INT2, SDAO maximum sink current……..
……5mA
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}
EV3921-U-00A (4)	46	2 .. °C/W
JESD51-7 (5)	36	8 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV3921-U-00A, a 2-layer PCB (51mmx51mm).
5) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 54V, PGND, DGND, AGND, and SGND are connected together, R_{SENSE} = 0.25Ω, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input under-voltage lockout (UVLO)	V_{IN_UVLO}	V_{IN} rising	28	29.5	31	V
Input UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			2.7		V
Input over-voltage lockout (OVLO)	V_{IN_OVLO}	V_{IN} rising	62	65	68	V
Input OVLO hysteresis	$V_{IN\_OVLO\_HYS}$			2.8		V
Input OVP lockout delay (7)				100		µs
Input power okay threshold	V_{IN_OK}	V_{IN} rising	38	40	42	V
Input power okay hysteresis	$V_{IN\_OK\_HYS}$			0.7		V
EN logic high voltage	V_{EN_HI}		2.5			V
EN logic low voltage	V_{EN_LOW}				0.4	V
EN input current		Pull EN to 0V, 3.3V		0		µA
EN turn-on/-off delay	t_{EN_ON}	EN pin high pulse duration for start-up or low-pulse duration for shutdown		150		µs
	t_{EN_OFF}			120		
Supply current	I_{IN}	Float the logic pin, no connection for the output, AUTO = low		2	4	mA
Shutdown current	I_{SD}	EN = 0V		150		µA
VCC regulation	V_{CC}	Load = 0mA		3.3		V
		Load = 15mA		3.2		
V_{CC} UVLO	V_{CC_UVLO}	V_{CC} rising	2.3	2.5	2.7	V
V_{CC} UVLO hysteresis	$V_{CC\_UV\_HYS}$			170		mV
VCC current limit		VCC = DGND		17		mA
Power-on reset (POR) delay	t_{POR}	From VCC on to detection		0.5		ms
Detection						
First detection voltage	V_{DET1}	Test the VIN to OUT pins	3.6	4		V
Second detection voltage	V_{DET2}	Test the VIN to OUT pins	7.2	8		V
Detection voltage slew rate	V_{SLEW}	C_{DET} = 0.1µF			0.02	V/µs
Detection current limit	I_{DET_LIMIT}	Short VIN to OUT	1	1.2	1.5	mA
Short-circuit detection threshold	V_{SC}	V_{DET1}	1	1.5	1.8	V
Open-circuit current threshold	I_{OPEN}		10	30	55	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 54V, PGND, DGND, AGND, and SGND are connected together, R_{SENSE} = 0.25Ω, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum valid detection resistance	R_{GOODL}		15	17	19	kΩ
Maximum valid detection resistance	R_{GOODH}		26.5	30	33	kΩ
Maximum valid capacitance	C_{GOOD_MAX}		1		9	µF
Detection time	t_{DET}	Second detection phase		280	310	ms
Detection reset time	t_{RESET}	The port is reset by internal discharge between VIN and OUT before detection starts		80	100	ms
Midspan mode detection delay	t_{MID_DLY}	Re-detection interval, MID = 1		2.8		sec
Power removal detection delay	t_{REM_DLY}	Re-detection after a power removal event due to error condition (ICUT, ILIM, INRUSH), fault timer = 60ms MID = 0, automatic and semi-automatic mode	0.8	0.96	1.12	sec
Classification						
Classification output voltage	V_{CLS}	Test VIN to OUT pins during classification, load < 60mA	16	18	20	V
Classification current limit	I_{CLS_ILIM}	Short VIN to OUT		70		mA
Class event time	t_{CLE}		8	15	22	ms
Mark event voltage	V_{MARK}	Test VIN to OUT pins	7.6	8.8	9.8	V
Mark event current limit	I_{MARK_ILIM}	Short VIN to OUT	6	10	14	mA
Mark event time	t_{ME}		6.5	9	11	ms
Classification current threshold	I_{CLS}	Class 0 to 1	5.5	6.5	7.5	mA
		Class 1 to 2	13.5	14.5	15.5	mA
		Class 2 to 3	21.5	23	24.5	mA
		Class 3 to 4	31.5	33	34.5	mA
		Class 4 to over-current (OC) condition (or Class 5 (8))	45.5	48	50.5	mA
Port start-up delay	t_{PON}	Automatic mode, from detection ending to the power port exceeding 21V			100	ms
		Manual mode, from the command to output port exceeding 21V			3	ms
Port shutdown delay		From command off to gate < 1V			0.5	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 54V, PGND, DGND, AGND, and SGND are connected together, R_{SENSE} = 0.25Ω, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate Driver						
GATE source capability	I_{SOURCE}	Port start-up, V_{GATE} = PGND		-43		µA
GATE sink capability	I_{SINK}	Port shutdown, V_{GATE} = 10V		60		µA
		Port shutdown, V_{GATE} < 1V		9		mA
		Trigger short-circuit protection (SCP), V_{SENSE} = 450mV, V_{GATE} = 5V (7)		100		mA
GATE clamp voltage	V_{GS_MAX}	Float the GATE pin		10		V
OUT Pin						
OUT pin resistance	R_{OUT}	Between VIN and OUT, pull OUT high in idle state (detection/classification off, port shutdown)		0.2		MΩ
OUT pin bias current	I_{OUT_BIAS}	OUT = 0V		-270		µA
		OUT = 54V			1	µA
Protection						
Output power good (PG) rising threshold	V_{PG}	The OUT pin voltage decreases	1.5	2	2.5	V
Output PG hysteresis	V_{PG_HYS}			400		mV
PG delay		Low to high deglitch		3		ms
		High to low deglitch		10		µs
Current-limit threshold	V_{ILIM}	Class 0 to Class 3, ILIM bit = 0	101	106.25	111.5	mV
		Class 4, ILIM bit = 1	201	212.5	224	mV
		Class 5, ILIM bit = 1	251.75	265	278.25	mV
Over-current (OC) detection threshold	V_{CUT}	Class 0 to Class 3 (ICUT = 000)	89.06	93.75	98.44	mV
		Class 4 (ICUT = 100)	154.38	162.5	170.63	mV
		Class 5 (ICUT = 101)	218.5	230	241.5	mV
Current-limit timer	t_{ILIM}	TILIM = 11	50	60	70	ms
OC timer	t_{ICUT}	TCUT = 10	50	60	70	ms
Start-up inrush current limit timer	t_{INRUSH}	TINRUSH = 10	50	60	70	ms
Foldback initial voltage	V_{FOLD_ST}	The OUT pin voltage when ILIM decreases, ILIM bit = 0		32		V
		The OUT pin voltage when ILIM decreases, ILIM bit = 1		18		V
Foldback end voltage	V_{FOLD_END}	The OUT pin voltage when ILIM decreases to the minimum value		46		V
Foldback minimum current limit	V_{LIM_MIN}	Short VIN to OUT, FBLIMT bit = 1, Class 4		40		mV
		Short VIN to OUT, FBLIMT bit = 0, Class 4		22		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 54V, PGND, DGND, AGND, and SGND are connected together, R_{SENSE} = 0.25Ω, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Short-circuit fast-off threshold	V_{SCP}	ILIM bit = 0		212		mV
		ILIM bit = 1		425		mV
SENSE pin bias current			-1		+1	µA
Thermal shutdown (7)				150		°C
Thermal shutdown hysteresis (7)				25		°C
DC Load Disconnection						
DC disconnect hold threshold	V_{DC_HOLD}	Decreases the output load until the output port shuts down	1.25	1.875	2.5	mV
DC connect power time	t_{DCON}	Load time to reset the t_{DCOFF} timer	37.5	43.75	50	ms
DC disconnect power remove time	t_{DCOFF}	Time from load < V_{DC_HOLD} to gate off	300	350	400	ms
Analog-to-Digital Converter (ADC)						
ADC resolution				9		bits
Maximum ADC current range		ADC results = 1 1111 1111 (2.4mA/count)		1.216		A
Maximum ADC voltage range		ADC results = 1 1111 1111 (0.15V/count)		76.65		V
ADC junction temperature range		ADC results = 0 0000 0000 to 1 1111 1111 (0.4°C/count)	-40		+164.4	°C
Current conversion		I_{ADC} = 600mA		254		count
Voltage conversion		V_{ADC} = 44V		293		count
		V_{ADC} = 57V		380		count
Temperature conversion (7)		T_J = 25°C		163		count
		T_J = 125°C		413		count
Logic Interface (SCL, SDAI, SDAO, INT1, INT2, MID, A0, A1, A2, A3, AUTO, CLS5)						
Input logic low voltage	V_{LI}				0.4	V
Input logic high voltage	V_{HI}		2			V
Logic input current		For SCL or SDAI	-1		+1	µA
Open-drain output logic low voltage	V_{LO}	Sink current = 3mA, SDAO, INT1, INT2			0.4	V
Open-drain output logic high leakage		Open drain to 3.3V			1	µA
Internal pull-up/-down resistance	R_{UP}	A0, A1, A2, A3, AUTO, MID to VCC, and CLS5 to DGND		50		kΩ

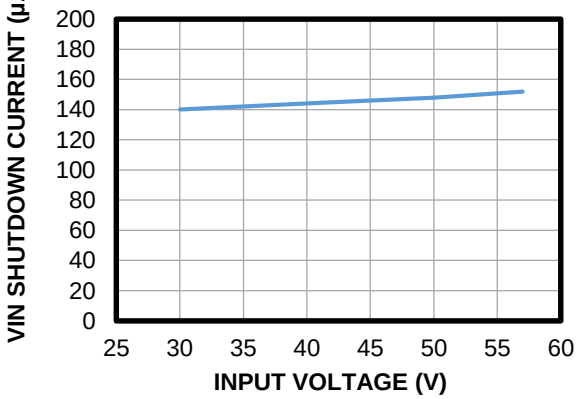
Notes:

6) Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.
8) If CLS5 is enabled, the MP3921 treats the upper current range classification from Class 4 as the classification current limit for Class 5.

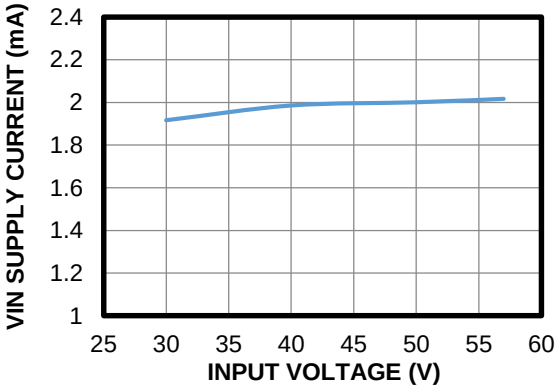
TYPICAL CHARACTERISTICS

V_{IN} = 54V, T_A = 25°C, unless otherwise noted.

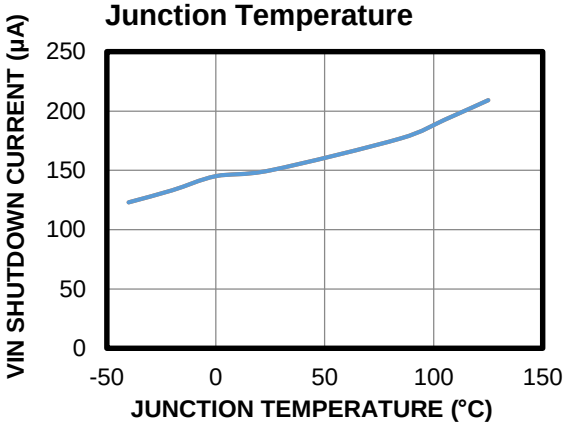
VIN Shutdown Current vs. Input Voltage



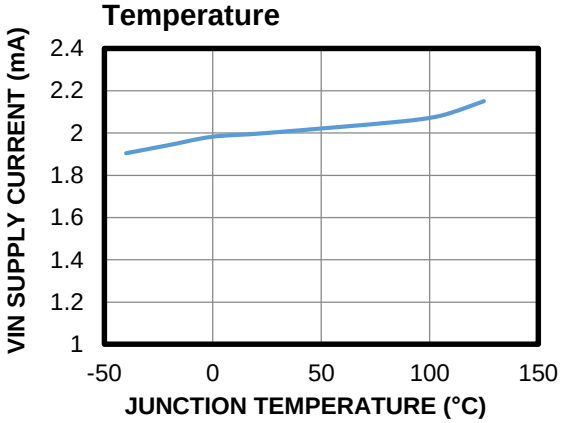
VIN Supply Current vs. Input Voltage



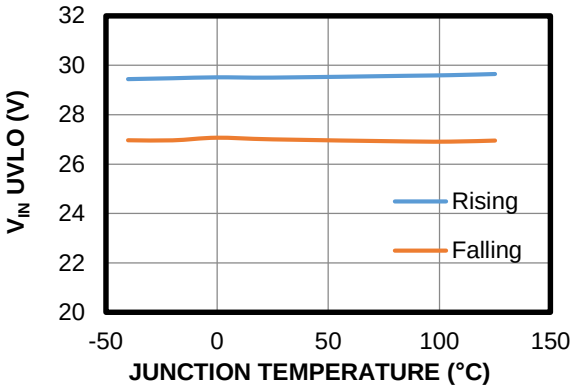
VIN Shutdown Current vs. Junction Temperature



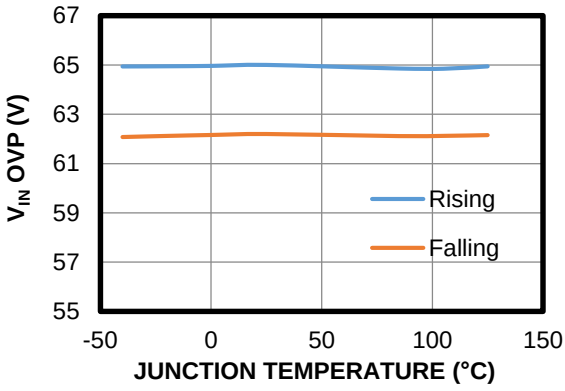
VIN Supply Current vs. Junction Temperature



V_{IN} UVLO vs. Junction Temperature



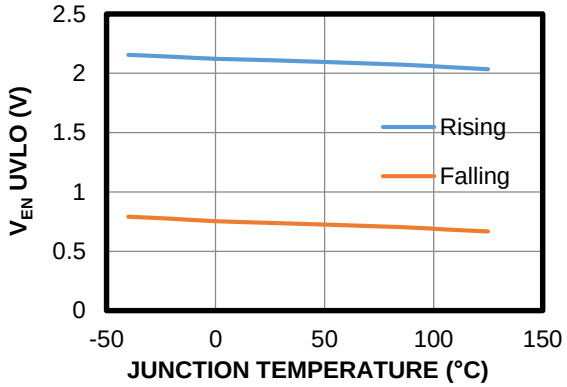
V_{IN} OVP vs. Junction Temperature



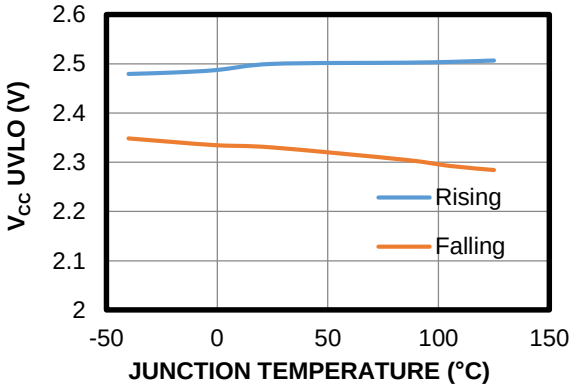
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 54V, T_A = 25°C, unless otherwise noted.

V_{EN} UVLO vs. Junction Temperature

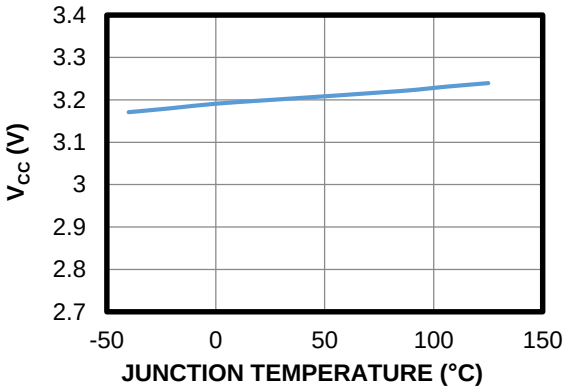


V_{CC} UVLO vs. Junction Temperature

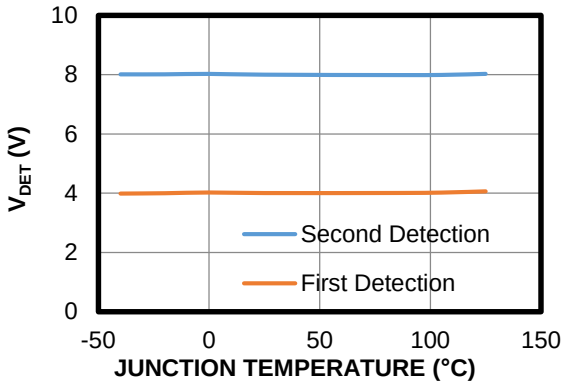


VCC Voltage vs. Junction Temperature

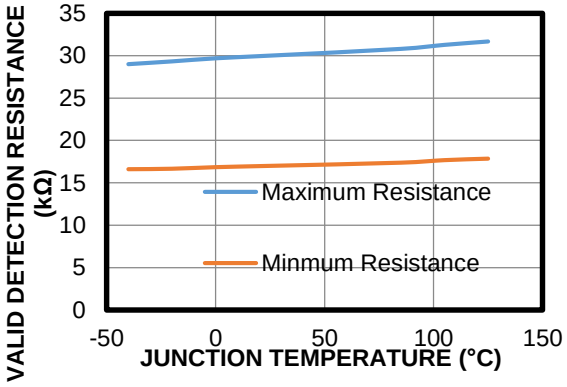
VCC load = 15mA



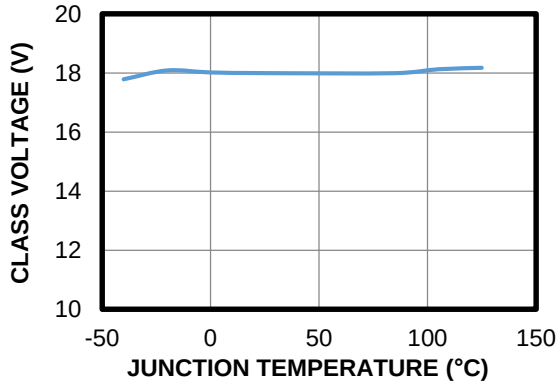
Detection Voltage vs. Junction Temperature



Valid Detection Resistance vs. Junction Temperature



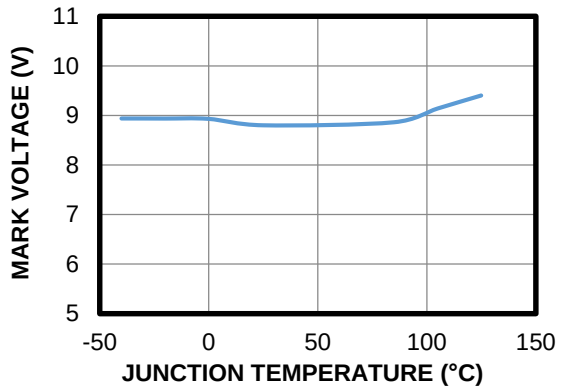
Class Voltage vs. Junction Temperature



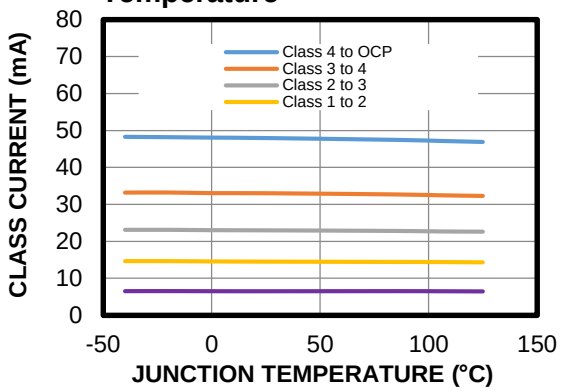
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 54V, T_A = 25°C, unless otherwise noted.

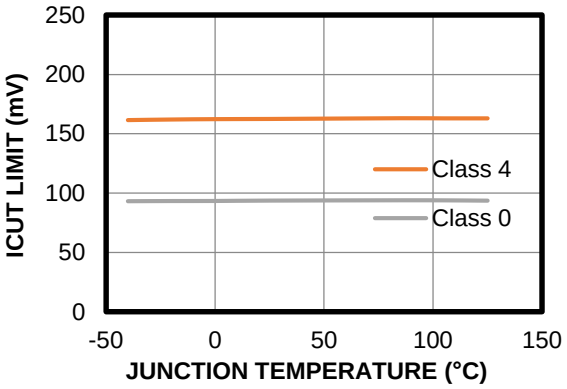
Mark Voltage vs. Junction Temperature



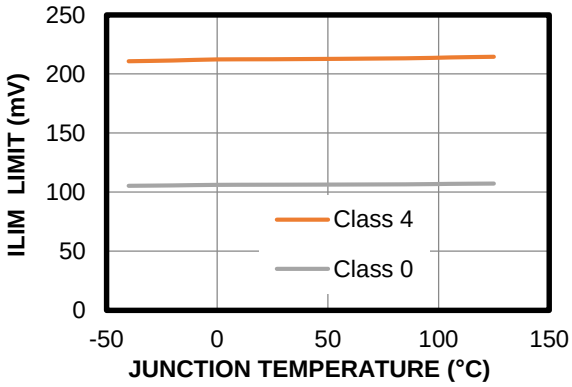
Class Current vs. Junction Temperature



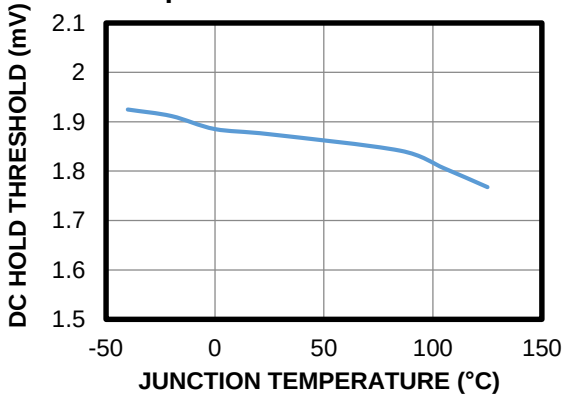
ICUT Limit vs. Junction Temperature



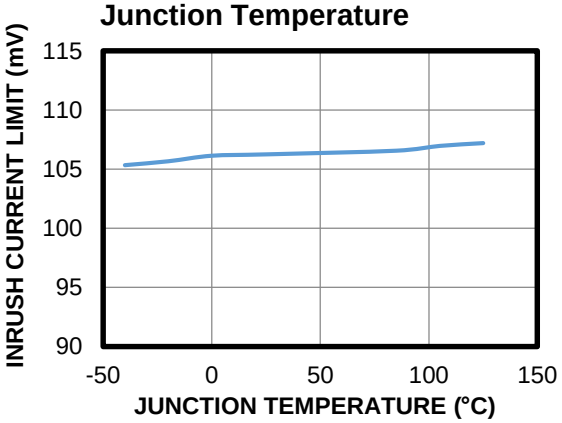
ILIM Limit vs. Junction Temperature



DC Hold Threshold vs. Junction Temperature



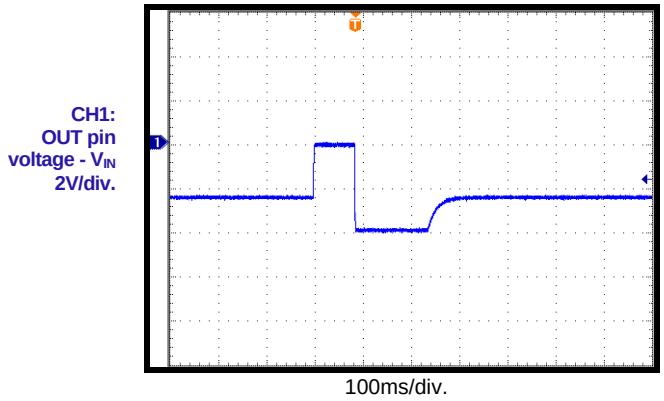
Inrush Current Limit vs. Junction Temperature



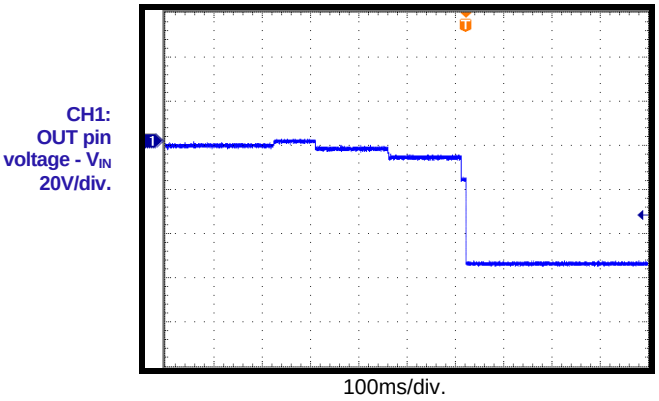
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 54V, set with a Class 4 PD load, T_A = 25°C, unless otherwise noted.

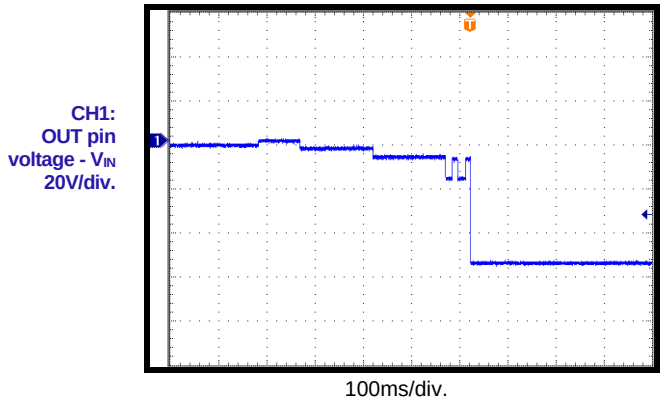
No PD Connection



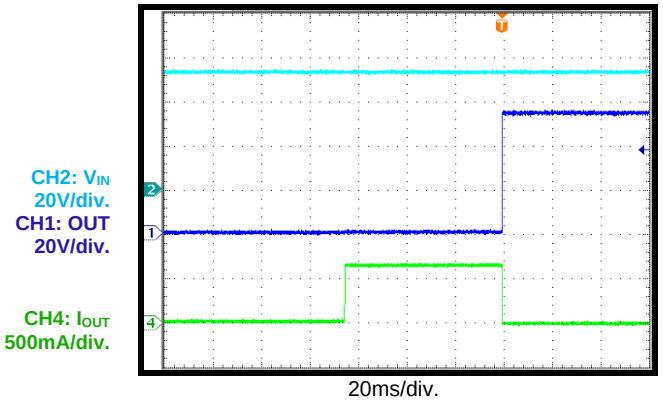
Class 0 to Class 3 PD Connection



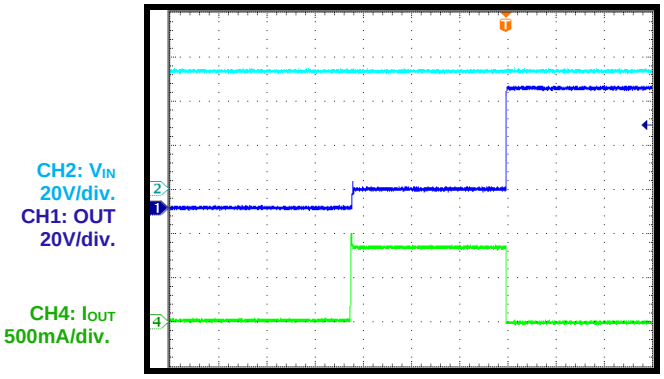
Class 4 PD Connection



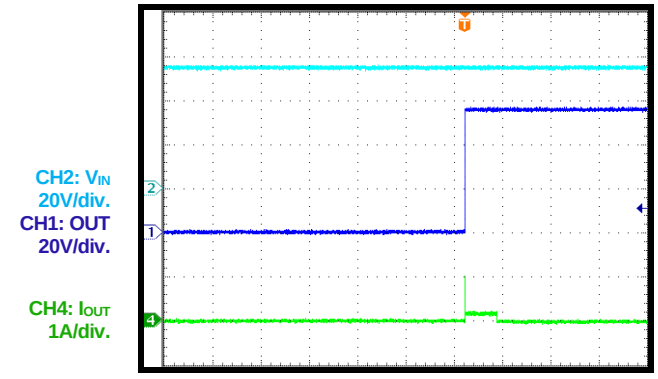
ICUT Triggered



ILIM Triggered



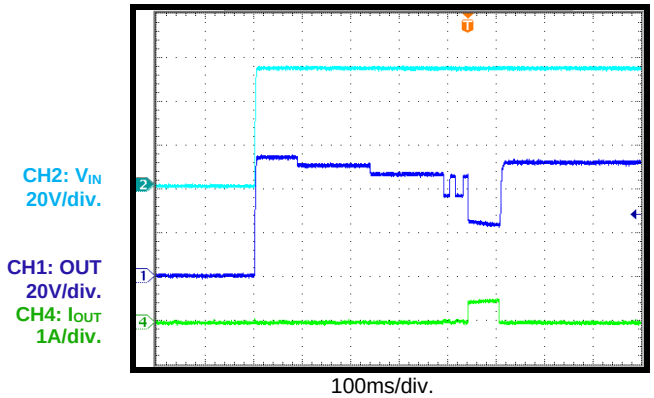
Output SCP Triggered



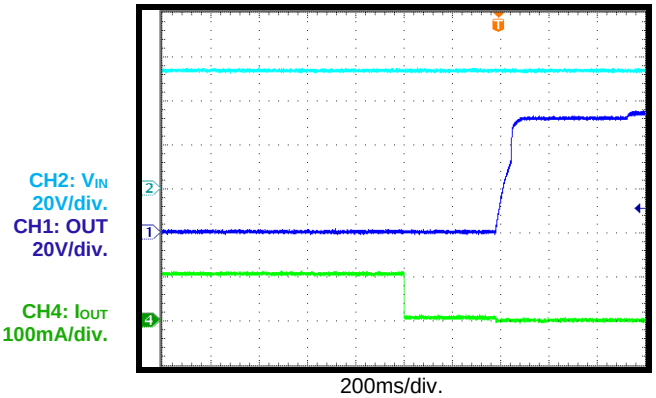
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 54V, set with a Class 4 PD load, T_A = 25°C, unless otherwise noted.

Inrush Current Limit Triggered



Output Disconnection Triggered



FUNCTIONAL BLOCK DIAGRAM

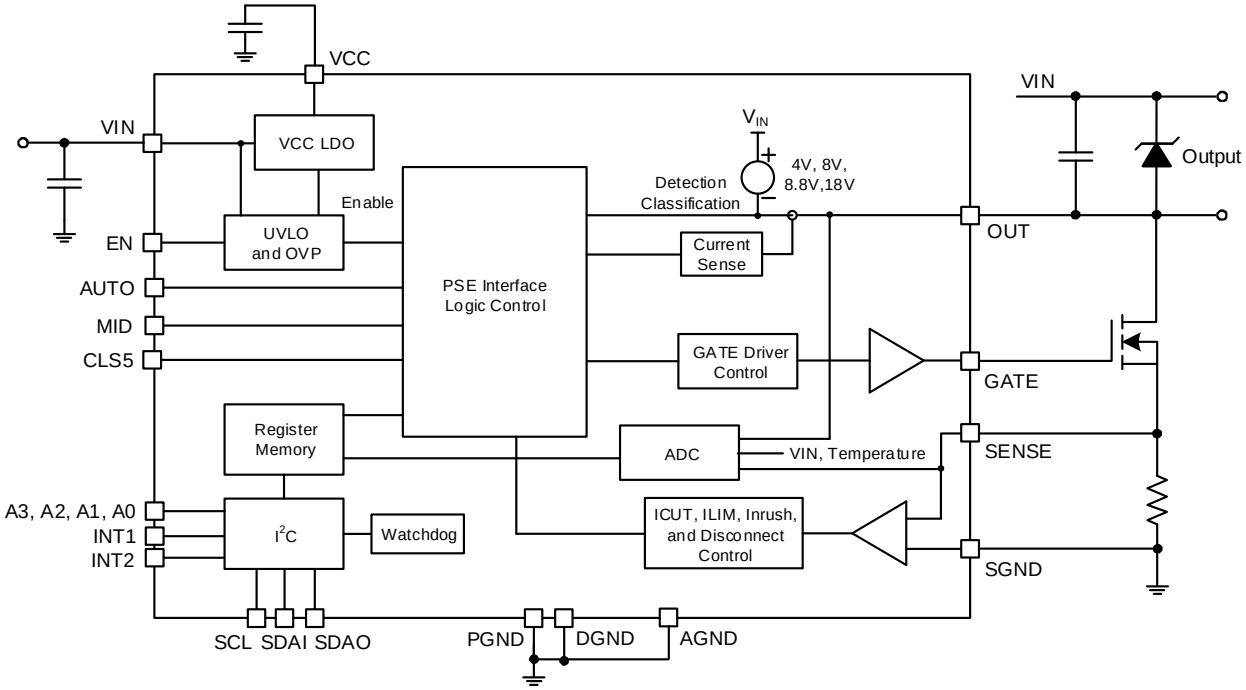


Figure 1: Functional Block Diagram

OPERATION

The MP3921 is a single-output power-sourcing equipment (PSE) power controller for IEEE 802.3af/at-compliant power over Ethernet (PoE) applications. The device establishes a method of communication between the powered device (PD) and PSE with detection, classification, and marked events. The MP3921 also provides functions for current and voltage protections in automatic mode as well as I^2C command control mode.

Power Supply

The MP3921 is designed for PoE applications that require a 44V to 57V input voltage (V_{IN}). The device powers the output port from this input source, then generates an internal 3.3V for the digital and analog circuits. The VCC regulator is enabled after VIN starts up. When V_{IN} exceeds its under-voltage lockout (V_{IN_UVLO}), the part is enabled after the power-on reset (POR) delay (t_{POR}). All functions can be enabled or disabled by the VCC voltage (V_{CC}) and EN voltage (V_{EN}) exceeding or dropping below their UVLO thresholds (V_{CC_UVLO} and V_{EN_UVLO}, respectively).

The MP3921 uses the PORT_ENABLE (05h) command to disable port. PORT_ENABLE does not include V_{IN}, V_{CC}, or V_{EN} UVLO.

The device can be reset by any of the below conditions:

- V_{IN} or V_{CC} UVLO
- EN turning off
- Writing 0 to ENAL (05h, bit[4])

After the MP3921 resets, all internal registers are set to their default values. The following pins are read and latched to the internal registers:

- AUTO
- MID
- CLS5
- A3 to A0

During normal operation, changes to these pins do not affect the registers.

The MP3921 includes a V_{IN} over-voltage protection (OVP) threshold at about 65V. The port shuts down if input OVP is triggered. The MP3921's outputs can restart with a new detection cycle after OVP recovery.

Powered Device (PD) Detection

In normal idle operation, the MP3921 detects the output port for a valid PD connection, which typically has a 24.9kΩ resistance (see Figure 2).

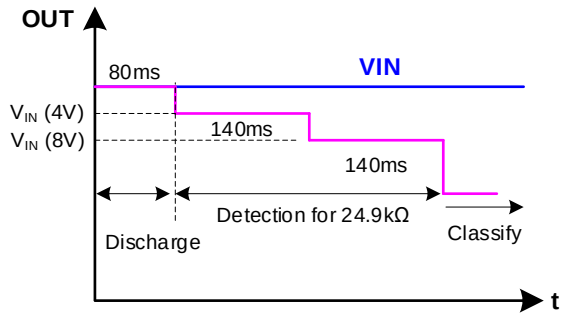


Figure 2: PD Detection Process

During this detection process, the MP3921 generates a two-phase voltage (4V/8V) through the OUT pin (see Figure 3).

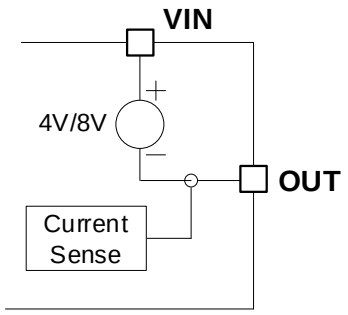


Figure 3: PD Detection Block Diagram

The OUT pin sinking current capability is limited to about 1.2mA. The current and voltage through OUT are measured. If the effective resistance with the two-point test is valid, then this means that a PD is connected to the PSE port. The MP3921 integrates a filter to avoid 50Hz/60Hz power-line noise.

After the detection cycle, DETC (00h, bit[3]) is set and an interrupt signal is generated to report that detection has completed. The host can read the DET/CLS_RESULT (26h) command to obtain the detection results.

After one detection cycle, the MP3921 enters classification mode if the PD connection is valid.

If the output port is shorted or the detected capacitance is too high, OUT limits the sink current to about 1.2mA. Then the detection cycle ends.

If the output port has an open circuit in the first phase detection period, then the MP3921 ends the detection cycle. If OUT has a low impedance to PGND, then detection ends immediately.

For other invalid resistance signatures, the MP3921 ends detection after two-phase detection. After an invalid detection result, the MP3921 re-enables detection within an 80ms port reset time. In midspan mode, there is a delay time (about 2.8s) before the 80ms reset time.

Midspan Mode

If the port is set to midspan mode, then the device waits about 2.8s before attempting to detect a PD connection. This can avoid detection collision. Midspan mode can be set or reset by the MID pin before the MP3921 starts up. Midspan mode can also be configured via MID (04h, bit[0]) using the I^2C interface during normal operation. If the detection is valid, then the device exits midspan mode.

Powered Device (PD) Classification

If the PD detection resistance is valid, then the device enters classification mode to measure the power level of the connected PD. Different classifications support 4W, 7W, 15.4W, or 30W of power to the port. Based on the IEEE802.3af/at standard, the MP3921 provides an additional class with Class 5.

Class 5 classification has a 40W load capability, which is valid when CLS5_EN (0Ch, bit[4]) is enabled and the classification current exceeds the Class 4 upper current threshold. If Class 5 is not enabled, then a classification current that exceeds 50.5mA results in an over-current (OC) condition and a classification failure. If Class 5 is enabled, then a classification current that exceeds 50.5mA results in a Class 5 classification level. In this scenario, an OC condition refers to when the current has triggered the current-limit threshold (V_{ILIM}). OC conditions can occur with all classes.

The CLS5 pin is pulled down internally to DGND to disable Class 5 classification. Pull CLS5 high during POR to enable Class 5 classification. Another method to enable Class 5 is to enable the CLS5_EN bit on the port.

During classification, the MP3921 outputs 18V on OUT (see Figure 4).

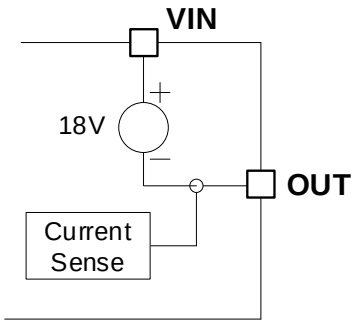


Figure 4: Classification Block Diagram

The device then measures the current though OUT to determine the classification level. After classification is complete, the status bit (CLSC) (00h, bit[4]) and interrupt are set. The classification result is stored in DET/CLS_RESULT.

Classification is based on the IEEE802.3at standards. If a classification result is in Class 0 to Class 3, then the MP3921 only performs one-time classification in accordance with IEEE 802.3af. If Class 4 or Class 5 is detected in the first classification event, then the MP3921 performs a second classification event when the voltages on VIN and OUT are the same. Two-event classification can be enabled by 2EVNTEN (0Ch, bit[0]) (see Figure 5).

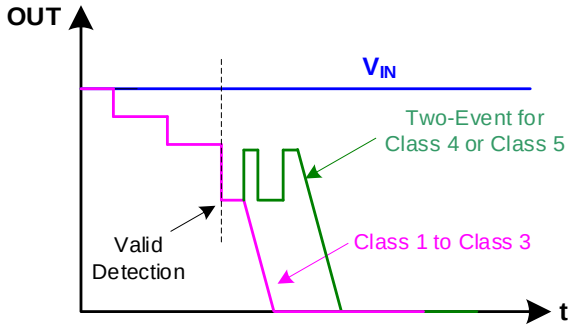


Figure 5: Single-Event and Two-Event Classification

Between the two classifications, the MP3921 performs two time mark events between VIN and OUT with an 8.8V mark voltage. The second classification result must be equal to the first classification result, or the classification is considered invalid.

After each two-event classification, the output port generates 8.8V to perform the mark event. During a classification mark event, the OUT pins have sink and source current capability. This means that the output port voltage can use a 0.1µF capacitor to follow OUT's regulated voltage.

The classification circuit is disabled when the classification result is valid, and the port output starts up.

Start-Up

If the detection and classification results are valid, then the MP3921 ramps up the port's output power. This power is delivered to the PD circuit. PEN (2Ah, bit[0]) and PEC (00h, bit[0]) are then set to indicate the port status. When V_{IN} is between 44V and 57V, the MP3921 can operate from 31V and report over-voltage (OV) conditions at 65V. If the OUT pin voltage drops below 2V, then PG (2Ah, bit[4]) and PGC (00h, bit[1]) are set to indicate the power good (PG) result.

If the detection is valid but the port does not start up within 400ms in automatic or semi-automatic mode, then the port initializes a new detection cycle.

Over-Current Protection (OCP)

When the port is powered up, the MP3921 controls the inrush current (I_{INRUSH}). As a result, the output port voltage ramps up smoothly until the connected PD capacitor charges up to the power source voltage. In this scenario, the GATE pin voltage (V_{GATE}) is controlled to limit the input current (I_{IN}) below 106.25mV / R_{SENSE}.

If the PD capacitance is too large or the output port is shorted, then I_{INRUSH} lasts for the start-up inrush current limit time (t_{INRUSH}). After t_{INRUSH}, the port output power turns off. t_{INRUSH} can be configured via TINRUSH (08h, bits[5:4]).

If 106.25mV / R_{SENSE} exceeds the port's OC threshold (I_{CUT}) during the inrush period, the ICUT OC timer (t_{ICUT}) begins counting. After t_{ICUT}, the output turns off. It is recommended for R_{SENSE} to be 0.25Ω for all applications. If the port shuts down due to the start-up inrush current, then STF (00h, bit[6]) is set to indicate a start-up failure event.

After start-up, the PG bit is set high to indicate the port's output power status. If the load current exceeds V_{CUT} / R_{SENSE} (where V_{CUT} is controlled by the ICUT bit), then t_{ICUT} is enabled to record the OC condition.

The port turns off once this timer finishes counting. If the load current exceeds V_{CUT} and triggers V_{ILIM} / R_{SENSE}, then the GATE pin regulates the load at the current limit. The current-limit timer (t_{ILIM}) is enabled to record the current limit event. t_{ILIM} is counted even if the MP3921 is in current foldback mode.

The OC detection threshold (V_{CUT}) is below V_{ILIM}. t_{ICUT} starts counting when the OC condition begins. If the load current drops below V_{CUT}, then t_{ICUT} does not reset immediately. Instead, t_{ICUT} counts down at 1/16 of the rising rate. t_{ICUT} records for a total of 60ms for every 0.96s + 0.06s detection window.

If the port shuts down due to an OC condition, then the port can be re-enabled only after t_{ICUT} counts down to 0ms. This logic can detect a short or repeated OC condition. The logic also protects the external MOSFET from overheating. t_{ILIM} and t_{INRUSH} operate with the same logic.

The over-current protection (OCP) timer does not reset even if the device shuts down or EN (05h, bit[0]) turns off. This means that the port cannot be re-enabled until the timer counts down to 0ms again. In manual mode, the host should read the read and clear (R/C) command register address continuously until the register is reset to 0. Then the port is re-enabled. In automatic mode, the MP3921 automatically restarts after the timer counts down to 0ms.

When t_{ICUT} is completed, the related OUT port shuts down (see Figure 6 on page 18). At the same time, the POWER_STATUS (2Ah) and OVER_LOAD_STATUS (2Dh and 2Eh) commands are set to indicate the power condition.

The default V_{CUT} is different for Class 0 to Class 3 compared to Class 4 and Class 5. V_{CUT} can also be configured. V_{ILIM} has three fixed values for Class 0 to Class 3, Class 4, and Class 5.

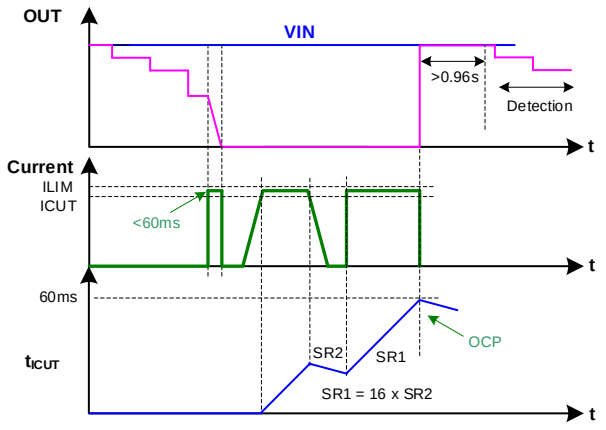


Figure 6: I_{CUT} Over-Current Detection

The GATE pin typically has a 43μA source current capability for current-limit regulation, which means that the output voltage (V_{OUT}) maximum start-up slew rate can be controlled by I_{GATE} / C_{GD} (where C_{GD} is the capacitance between the external MOSFET's gate and drain). When V_{GATE} is pulled down to 1V by a weak discharge current, V_{GATE} is latched to 0V with a strong pull-down current until the next start-up event. If the load current ramps up quickly and triggers the short-circuit fast-off threshold (V_{SCP}), then the MP3921 shuts down the port power quickly to protect the MOSFET. The load at the current limit is regulated until t_{ILIM} counts down.

The MP3921 shuts down the output port if an I_{CUT} or over-current limit (I_{LIM}) event occurs, and the related fault bits are set. The following registers are also affected:

- The PG and PEN bits in the POWER_STATUS command are cleared.
- The DET/CLS_RESULT, PORT_VOLTAGE (42h and 43h), and PORT_CURRENT (40h and 41h) commands are cleared.
- The PGC and PEC bits in the POWER_STATUS_CHANGE (2Bh and 2Ch) command are set.
- The ICUT and ILIM bits are cleared.

Current Foldback

During an overload or short-circuit condition, the MP3921 limits the current through the sense resistor by controlling the external MOSFET. The MOSFET loses power due to the rising drain voltage. To reduce power loss and protect the MOSFET, the current limit must be reduced when the drain voltage rises.

For Class 0 to Class 3 applications, the current limit drops when the OUT pin voltage exceeds 32V. Meanwhile, V_{ILIM} falls linearly to 40mV when the OUT pin voltage rises to 46V. For Class 4 and Class 5 applications, the current limit drops when the OUT pin voltage exceeds 18V. The current limit eventually falls to 40mV when the OUT pin voltage rises to 46V.

Figure 7 shows current-limit foldback. The current limit is calculated using a 0.25Ω sense resistor.

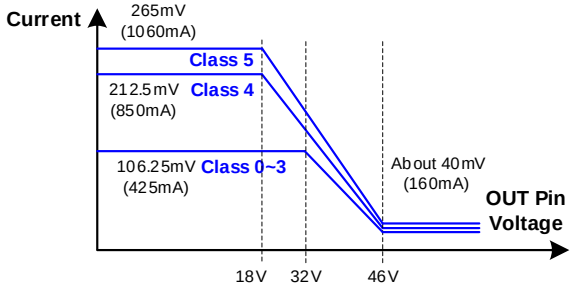


Figure 7: Current-Limit Foldback

DC Disconnect Detection

The MP3921 monitors the load current after the port is powered up. If the port load current drops below 7.5mA (assuming R_{SENSE} = 0.25Ω) for longer than 350ms, then the MP3921 considers the load disconnected and turns off the port's output power. The MP3921 considers the load connected to the port if the current exceeds 7.5mA (assuming R_{SENSE} = 0.25Ω), or exceeds the current load from the PSE output, for longer than 43.75ms in every 393.75ms window.

The DC disconnect detection function is enabled by default after the device starts up in automatic mode. If the AUTO pin is low during start-up or after the IC resets, then the DC disconnect detection function is disabled by default. The port can enable/disable the DC disconnect detection function via DISEN (07h, bit[0]). After shutdown occurs due to DC

disconnect detection, DCDIS (00h, bit[2]) is set to indicate the status. The following registers are also affected:

- The PG and PEN bits in the POWER_STATUS command are cleared.
- The DET/CLS_RESULT, PORT_VOLTAGE, and PORT_CURRENT commands are cleared.
- The PGC and PEC bits in the POWER_STATUS_CHANGE command are set.
- The ICUT and ILIM bits are cleared.

Interrupt Control

The MP3921 features two interrupt pins (IN1 and INT2) that can be used for different priority interrupt sources. The priority can be configured via the INTERRUPT_PRIORITY (02h) command. The INT2 pin responds to the selected interrupt sources, while the INT1 pin responds to all interrupt sources. By default, INT2 responds to V_{IN} power failures and OC events.

The MP3921 pulls INT1 and INT2 low if a fault condition occurs in the INTERRUPT_PRIORITY command while the interrupt is not masked. The interrupt signal is asserted to notify the host controller that certain fault conditions have been detected. If the interrupt source is masked, the interrupt event bits are set, but INT1 and INT2 do not respond to the fault event.

INT1 and INT2 go low if a fault occurs. If a second fault occurs before the host resets the interrupt signal, then the MP3921 keeps INT1 and INT2 low until the host controller resets the fault condition (see Figure 8).

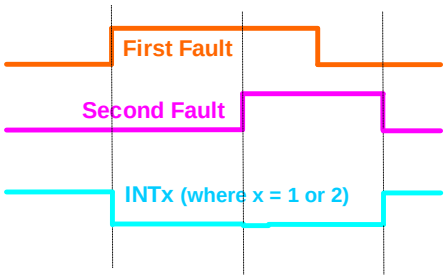


Figure 8: Interrupt Sequence

After the host controller receives the interrupt signal, it can check the status register to diagnose the issues. The host can read the R/C address to reset the interrupt event register, as well as INT1 and INT2. If the host controller reads the status register through the read-only address, then neither the interrupt event register nor INT1 and INT2 are reset. For more details, see the Register Map section on page 25.

INT1 and INT2 can be reset by CLRAINT (0Eh, bit[1]) or the interrupt disable bit, INTEN (0Eh, bit[0]) (see Figure 9).

The INTx pin (where x = 1 or 2) should be triggered at the fault event's edge. If two fault events occur simultaneously, then INTx does not reset until all fault events are cleared.

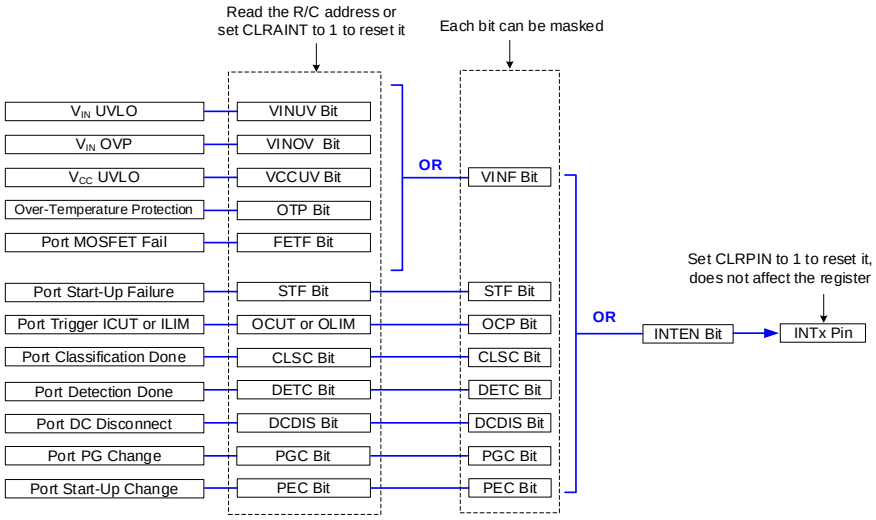


Figure 9: Interrupt Logic Diagram

Legacy Detection

If the detection capacitor (C_{DET}) exceeds 5µF and the cable is connected to a legacy PD with a high input capacitor (C_{IN}), then the DET/CLS_RESULT command returns to 010. LEGEN (12h, bits[1:0]) enable legacy detection mode. By default, the LEGEN bits are set to 00 to disable legacy detection. Table 1 shows the detection parameters.

Table 1: Legacy Detection Measurements

Parameter	Value	Units
Minimum measurable capacitance	5	µF
Maximum measurable capacitance	100	µF
Capacitance test charge current	500	µA
Nominal measurement time	150	ms
Maximum voltage before starting measurement	2.4	V
Duration of first port discharge period	250	ms
Duration of second port discharge period	500	ms
Maximum voltage during measurement	18.5	V

Legacy detection returns the results of the LEGACY_DETECT_RESULT1 (35h) command.

The MP3921 starts legacy detection after the PD input voltage is discharged below 2.4V. If the PD input voltage is high, then a 250ms discharge timer works with a 100kΩ load between the OUT and VIN pins. If the PD input voltage exceeds 2.4V, then a secondary 500ms discharge timer begins. If the PD input voltage does not fall below 2.4V after the two discharge times, then the MP3921 is set to 0010 in the LEGACY_DETECT_RESULT1 command.

After legacy detection starts, a fixed current is charged to the PD input. The voltage difference between the VIN and OUT pins is used to calculate the effective capacitance.

If the capacitance is too great and the measured voltage difference is below 0.5V, then the MP3921 reports 0110. If the capacitance is too low and the measured voltage reaches 18.5V, then the MP3921 reports 0100 or 0101. All these results are invalid in legacy detection.

If legacy detection is enabled and a legacy device is detected in automatic mode, then the detection status is reported in the LEGACY_DETECT_RESULT1 command. However, the device does not start up immediately, as it requires a host command through the I^2C.

If the LEGEN bits are set to 01 or 10 in automatic or semi-automatic mode, then there is initially one standard detecting cycle. If the standard resistance detection result is valid, then the MP3921 does not continue legacy detection and the classification process begins instead. If the standard resistance detection result is not valid and legacy detection is valid, then the MP3921 does not start the classification process, even if CLSEN (06h, bit[4]) is set. In this scenario, a software command is required to trigger the classification process.

If the following conditions are met, then PON (11h, bit[0]) automatically starts up the port regardless of whether the classification result matches or if an OC condition is present.

- The PON bit is enabled by the software after the legacy detection is determined to be valid.
- The MP3921 is in automatic or semi-automatic mode.

If the LEGEN bits are enabled in automatic or semi-automatic mode, then the legacy detection result repeats and refreshes the LEGACY_DETECT_RESULT1 command. This process repeats until the LEGEN bits are disabled. In manual mode, legacy detection occurs once, then the LEGEN bits reset automatically. It is recommended to use manual mode.

Mode Selection

The MP3921 provides four modes to flexibly control PoE communication and start-up: automatic mode, semi-automatic mode, manual mode, and shutdown mode. The AUTO pin and MODE (03h, bits[1:0]) set the different modes, which are described in greater detail on page 21.

Automatic Mode

In automatic mode, the MP3921 automatically controls and responds to all detection, classification, and start-up functions. The MP3921 handles these processes without external I²C control. Float the AUTO pin to force the MP3921 to work in automatic mode.

In automatic mode, the MODE bits are set to 11 when device turns on. The AUTO pin status is only read once when the device turns on or the MP3921 is reset. If a master is connected to the MP3921 via the I²C, then the master can change the MODE bits to change the mode. If there is no valid PD on the port in automatic mode, then the MP3921 repeats the detection cycle until a valid PD is connected.

If the MP3921 runs in automatic mode after start-up or reset, then DETEN (06h, bit[0]) and the CLSEN bit are set high based on the AUTO pin. If port is set to automatic mode via the I²C, then the DETEN and CLSEN bits do not change.

Semi-Automatic Mode

In semi-automatic mode, the MP3921 automatically detects and classifies the connected PD. However, the port does not start up until an I²C command is issued. Set the MODE bits to 10 to force the MP3921 to operate in semi-automatic mode.

When the port is set to semi-automatic mode, the DETEN and CLSEN bits do not change. If the DETEN and CLSEN bits are high in semi-automatic mode, then the port repeats the detection (and classification if the PD detection result is valid) continuously. However, the port does not start up until an I²C command is issued. If the detection and classification are valid, then the port power can be turned on by a PON bit. If the port is powered off in semi-automatic mode, then the DETEN and CLSEN bits are reset to 0.

If detection is valid and the port does not turn on within 400ms in automatic or semi-automatic mode, then the port initiates a new detection sequence. If the final detection and classification sequences are determined to be invalid before the start-up command is received, then the device fails to turn on. At the same time, the STF bits are set and the MP3921 resets the command. If the detection and classification sequences are valid but a start-up command is not issued after 400ms, then the STF bits are set.

Manual Mode

In manual mode, all functions are controlled via the I²C interface. Manual mode is recommended for system diagnostics. Set the MODE bits to 01 to force the port to operate in manual mode.

In manual mode, the DETEN and CLSEN bits are set to 0. Set these bits to 1 to enable one-time detection or classification. These bits reset to 0 automatically.

The PON bit powers the port in manual mode. The port turns on any time the PON bit is set. If the DETEN, CLSEN, and PON bits are set simultaneously, then the MP3921 executes a detection cycle first. If the DETEN and CLSEN bits are set after the port starts up, then the MP3921 ignores the DETEN and CLSEN bits. RDET (10h, bit[0]) and RCLS (10h, bit[4]) follow the same logic.

If a PON bit is received while the device recovers from a protection, then the MP3921 does not turn on and the failure is reported to the STF bits.

Shutdown Mode

In shutdown mode, all detection, classification, and port power output functions are off. To force the MP3921 to operate in shutdown mode, pull the AUTO pin to DGND before the device starts up or resets. Set the MODE bits to 00 to set the port to shutdown mode.

Once the port is in shutdown mode, the power turns off and the port event/status registers are cleared, except for the PEC and PGC bits. The I²C interface still operates in shutdown mode, but the port does not respond to any detection, classification, or port start-up commands.

In certain AUTO pin configurations, the MODE bits are set to 00 or 11 after start-up (or after a reset). After start-up, the port can switch between the four modes. The registers and port states are not changed by these bits unless shutdown mode is selected.

9-Bit Analog-to-Digital Converter (ADC)

The MP3921 integrates a 9-bit analog-to-digital converter (ADC) to continuously measure V_{IN} and V_{OUT}, as well as the load current and junction temperature (T_J). When any ADC information is required, the host controller can read the data registers. ADC conversion only works when the port is enabled, and there is no data update when the port is shut down. The register cannot be updated while it is read, even if ADC conversion is complete for that segment of data.

I²C Interface

The MP3921 features an I²C interface. The 7-bit device address is defined as 010 xxxx, where the lower 4 bits are set by the A3 to A0 pins. When the master sends an 8-bit address value, the 7-bit I²C address should be followed by a 0 or 1 to indicate a write or read operation, respectively. The MP3921 works as a slave and supports standard mode (100kbps) and fast mode (400kbps) communication.

The I²C is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled externally to a bus voltage when they are idle. When connected to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. To support communication with an isolated host controller, the data interface is split into two ports: SDAI and SDAO. For non-isolated applications, SDAI and SDAO can be connected to one another.

The MP3921 includes an alert response address for MP3921 devices that are connected through the address 0x0C (000 1100). If the bus master controller sends the alert response address when INT1 is low during an interrupt event, then the MP3921 with the interrupt request responds with its device address on the SDAI line before releasing the INT1 line.

If two MP3921 devices respond simultaneously, then the device with the lower address succeeds in transmitting to the master via the SDAI and SDAO lines. The device that attempts to send a 1 but detects a 0 on the SDAI line does not respond. After this, the MP3921 with the higher address finishes responding. The INT1 pin remains low until it receives the host controller's next alert response address read.

The MP3921 has a global address: 0110000. This means that the host controller can write to multiple MP3921 devices through the address 0x60 (01100000). If the host controller reads multiple MP3921 through the address 0x61 (01100001), then it works as an alert response address.

While reading or writing, the MP3921 register address is determined by the host command. After each read/write (R/W) data byte operation, the register address automatically increases by 1 byte, and the host can read/write the next byte without the new address command information. If the system works with several host controllers, and host 1 does not have data to read/write in the address set by itself, then this address can respond to host 2. If different registers must be read or written, then the address information is required to set the correct register address.

I²C Data Validity

A clock pulse is generated for each transferred data bit. The data on the SDA line must be stable during the clock's high period. The data line's high or low state can only change when the clock signal on the SCL line is low (see Figure 10).

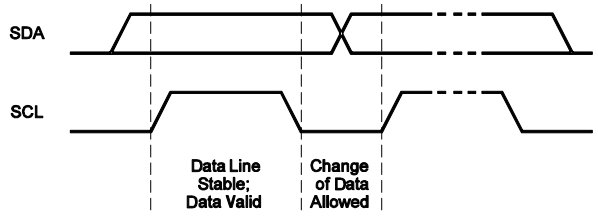


Figure 10: Bit Transfer on the I²C Bus

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start command is defined as the SDA signal transitioning from high to low while the SCL signal is high. A stop command is defined as the SDA signal transitioning from low to high while the SCL signal is high (see Figure 11 on page 23).

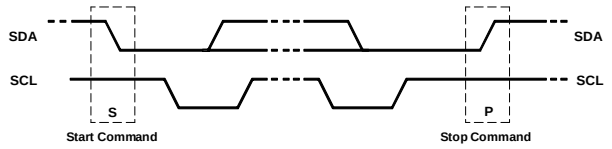


Figure 11: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after a start command. The bus is considered free again a minimum of 4.7µs after the stop command. The bus remains busy if a repeated start (Sr) command is generated instead of a stop command. The start and repeated start commands are functionally identical.

I²C Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledgement clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, allowing it to remain low during this clock pulse's high period.

Figure 12 shows the data transfer sequence.

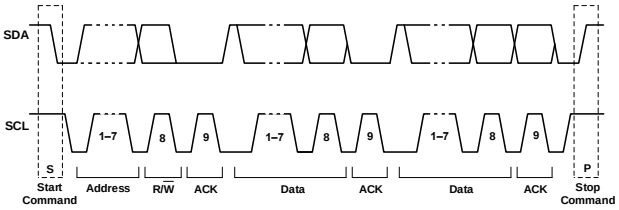


Figure 12: Complete Data Transfer

After the start command, a slave address is sent. This address is 7 bits long followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), while a 1 indicates a request for data (read). A data transfer is always terminated by a stop command generated by the master. However, if a master must communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

The MP3921 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements. It requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. The MP3921 acknowledges that it has received each byte by pulling the SDA line low during a single clock pulse's high period. A valid I²C address selects the MP3921. The MP3921 performs an update on the least significant bit (LSB) byte's falling edge.

Figure 13, Figure 14, and Figure 15 on page 24 shows an I²C write example, I²C read example, and the 0x0C address's different read command from the standard I²C, respectively.

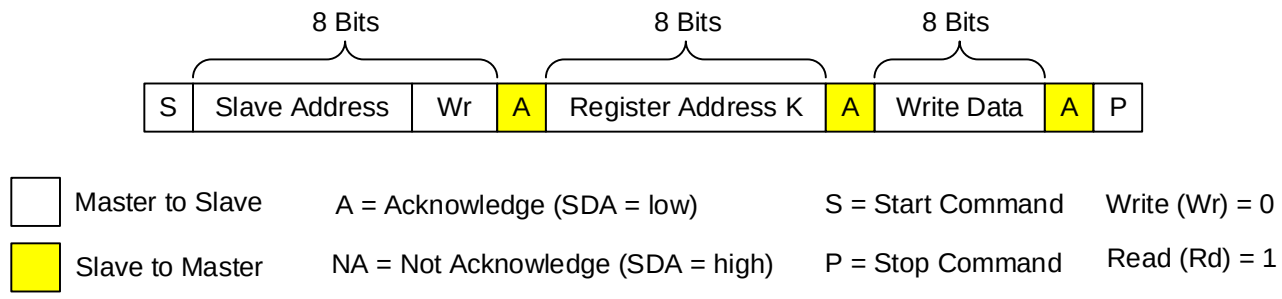


Figure 13: I²C Write Example

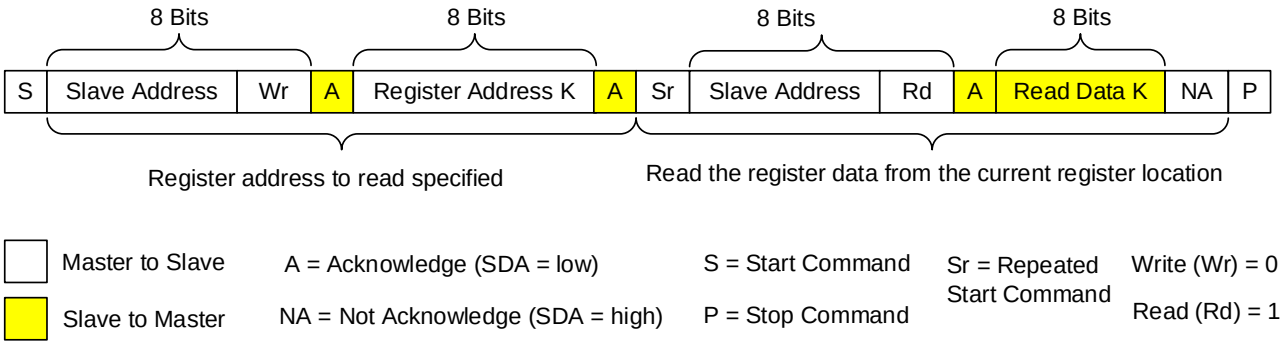


Figure 14: I²C Read Example

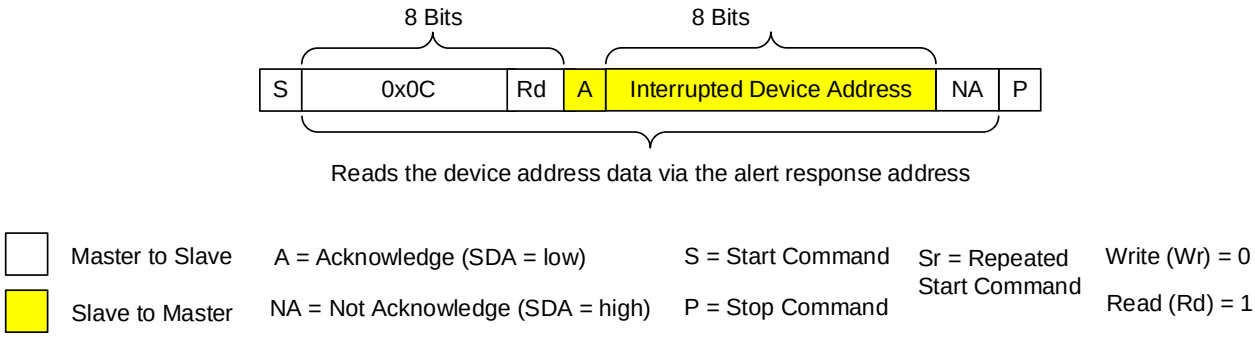


Figure 15: 0x0C Read Example

Watchdog

The MP3921 implements a watchdog to monitor the SCL line for I²C activity. If there is no transition on the SCL line for about 2.5s during I²C communication, then the I²C port and output port shut down. WDS (33h, bit[0]) is set to 1 to indicate the error condition. The WDS bit must be reset before the port can be re-enabled. After watchdog protection is triggered, the port shuts down until the host re-enables the EN bit.

By default, the watchdog is off after start-up. To enable the watchdog function, set WDEN (0Fh, bit[0]) to 1.

Over-Temperature Protection (OTP)

Over-temperature protection (OTP) is implemented to prevent the chip from thermal runaway. When T_J exceeds its upper threshold, the MP3921 shuts down the port (the I²C and registers still work). Once the temperature drops below its recovery threshold, the port is enabled again with a new detection cycle. OTP (20h and 21h, bit[2]) is set to 1 after OTP recovery.

REGISTER MAP

Addr	Command	Type	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Reset State
Interrupt Commands											
00h	INTERRUPT	R	VINF	STF	OCP	CLSC	DETC	DCDIS	PGC	PEC	1000 0000
01h	INTERRUPT_ MASK	R/W	VINF _M	STF_ M	OCP_ M	CLSC _M	DETC _M	DCDIS _M	PGC_ M	PEC_ M	1A A0 0A00 (9)
02h	INTERRUPT_ PRIORITY	R/W	VINF _P	STF_ P	OCP_ P	CLSC _P	DETC _P	DCDIS _P	PGC_ P	PEC_P	1010 0000
Configuration Commands											
03h	MODE_ SETTING	R/W	RESERVED (11)		RESERVED (11)		RESERVED (11)		MODE		AAAA AAAA (9)
04h	MIDSPAN_ SETTING	R/W	-	-	-	-	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	MID	0000 MMMM (9)
05h	PORT_ ENABLE	R/W	-	-	-	ENAL	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	EN	0001 1111
06h	DET/CLS_ ENABLE	R/W	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	CLSE N	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	DE TEN	AAAA AAAA (9)
07h	DISCONNECT _ENABLE	R/W	-	-	-	-	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	DISEN	0000 AAAA (9)
08h	FAULT_ TIMER	R/W	RESERVED (11)		TINRUSH		TILIM		TCUT		1010 1110
09h to 0Ah	RESERVED (11)	-	-	-	-	-	-	-	-	-	0000 0000
0Bh	FOLDBACK_ ILIM	R/W	-	-	-	-	-	-	-	FB LIMT	0000 0001
0Ch	2-EVENT_ CLASS_ 5_ENABLE	R/W	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	CLS5 _EN	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	2EVNT EN	CCCC AAAA (9)
0Dh	RESERVED (11)	-	-	-	-	-	-	-	-	-	1110 0100
0Eh	INTERRUPT_ ENABLE	R/W	-	-	-	-	-	CLR PIN	CLR AINT	INTEN	0000 0001
0Fh	GENERAL_ CONTROL	R/W	-	-	-	-	-	RESE RVED (11)	AD CEN	WDEN	0000 0A 10 (9)
Manual Control Commands											
10h	DET/CLS_ TRIGGER	R/W	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	RCLS	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	RDET	0000 0000
11h	POWER_ON/ OFF_ TRIGGER	R/W	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	POFF	RESE RVED (11)	RESE RVED (11)	RESE RVED (11)	PON	0000 0000
12h	LEGACY_ ENABLE	R/W	RESERVED (11)		RESERVED (11)		RESERVED (11)		LEGEN		0000 0000
Current Limit Configuration Commands											
13h	ICUT_ THRESHOLD	R/W	-	-	-	-	-	ICUT			0000 0000
14h to 16h	RESERVED (11)	-	-	-	-	-	-	-	-	-	0000 0000
17h	ILIM_ THRESHOLD	R/W	-	-	-	-	-	-	-	ILIM	0000 0000
18h to 1Ah	RESERVED (11)	-	-	-	-	-	-	-	-	-	0000 0000

Addr	Command	Type	D7	D6	D5	D4	D3	D2	D1	D0	Reset State
Status Commands											
20h	POWER_ SOURCE_ STATUS1	R	RESERVED (11)	RESERVED (11)	RESERVED (11)	FETF	VCC UV	OTP	VINOV	VINUV	0000 1001
21h		R/C (10)									
22h	POWER_ SOURCE_ STATUS2	R	-	-	-	-	-	-	VINOK	-	0000 0000
23h		R/C (10)									
24h	DET/CLS_ COMPLETE_ STATUS	R	RESERVED (11)	RESERVED (11)	RESERVED (11)	CLSC	RESERVED (11)	RESERVED (11)	RESERVED (11)	DETC	0000 0000
25h		R/C (10)									
26h	DET/CLS_ RESULT	R	CLSR				2EVNTC	DETR			0000 0000
27h to 29h	RESERVED (11)	-	-	-	-	-	-	-	-	-	0000 0000
2Ah	POWER_ STATUS	R	RESERVED (11)	RESERVED (11)	RESERVED (11)	PG	RESERVED (11)	RESERVED (11)	RESERVED (11)	PEN	0000 0000
2Bh	POWER_ STATUS_ CHANGE	R	RESERVED (11)	RESERVED (11)	RESERVED (11)	PGC	RESERVED (11)	RESERVED (11)	RESERVED (11)	PEC	0000 0000
2Ch		R/C (10)									
2Dh	OVER_LOAD_ STATUS	R	RESERVED (11)	RESERVED (11)	RESERVED (11)	OCUT	RESERVED (11)	RESERVED (11)	RESERVED (11)	STF	0000 0000
2Eh		R/C (10)									
2Fh	CURRENT_ LIMIT_ STATUS	R	-	-	-	-	RESERVED (11)	RESERVED (11)	RESERVED (11)	OLIM	0000 0000
30h		R/C (10)									
31h	DISCONNECT _STATUS	R	-	-	-	-	RESERVED (11)	RESERVED (11)	RESERVED (11)	DCDIS	0000 0000
32h		R/C (10)									
33h	WATCHDOG_ STATUS	R	-	-	-	-	-	-	-	WDS	0000 0000
34h	PIN_STATUS	R	-	-	-	AUTO	A3	A2	A1	A0	000A DDDD (9)
35h	LEGACY_ DETECT_ RESULT	R	RESERVED (11)				LEGDET				0000 0000
36h	RESERVED (11)	-	-	-	-	-	-	-	-	-	0000 0000
ADC Results Commands											
40h	PORT_ CURRENT	R	-	-	-	-	-	-	-	Bit[0]	0000 0000
41h		R	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	0000 0000
42h	OUT_PIN_ VOLTAGE	R	-	-	-	-	-	-	-	Bit[0]	0000 0000
43h		R	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	0000 0000
44h to 4Fh	RESERVED (11)	-	-	-	-	-	-	-	-	-	0000 0000
50h	INPUT_ VOLTAGE	R	-	-	-	-	-	-	-	Bit[0]	0000 0000
51h		R	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	0000 0000
52h	JUNCTION_ TEMPERATURE	R	-	-	-	-	-	-	-	Bit[0]	0000 0000
53h		R	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	0000 0000

Addr	Command	Type	D7	D6	D5	D4	D3	D2	D1	D0	Reset State
54h	RESERVED (11)	-	-	-	-	-	-	-	-	-	0000 0001
55h	RESERVED (11)	-	-	-	-	-	-	-	-	-	1111 1111
60h	DIE_ID	R	FAB		MAJOR_REV		MINOR_REV		VENDOR_ID		0000 0000

Notes:

9) "A" represents the AUTO pin's status during start-up. "M" represents the MID pin's status during start-up. "C" represents the CLS5 pin's status during start-up. "D" represents the A3 to A0 address pin statuses during start-up.
10) R/C is a read and clear address. Reading R/C clears the bit status after reading is complete.
11) Do not change the reserved register; otherwise, it may work abnormally.

INTERRUPT COMMANDS

INTERRUPT (00h)

Access: Read-only

The INTERRUPT command reads certain interrupt signals. Read the register address with a read and clear (R/C) byte, or write 1 to CLRAINT to reset the bit. The IN1 and INT2 pins go low to report if an interrupt bit is set to 1. These pins do not go low if the interrupt signal is masked.

Bits	Bit Name	Default	Description
7	VINF	1	Reads the interrupt signal for the input voltage (V_{IN}) power failure. If this bit is set to 1, this indicates that one of the following scenarios has occurred: • The start-up VIN is below 29.5V • V_{IN} over-voltage protection (OVP) • The VCC voltage (V_{CC}) is below the under-voltage lockout (UVLO) threshold • Thermal shutdown • A power MOSFET failure has occurred
6	STF	0	Reads the interrupt signal for a start-up failure. If this bit is set to 1 or if a port shuts down due to the start-up inrush current, then the output port has experienced a start-up failure.
5	OCP	0	Reads the interrupt signal for over-current (OC) conditions. If this bit is set to 1, then the output port has met the current-limit timer (t_{ILIM}) or the ICUT bit current (I_{CUT}) OC timeout condition.
4	CLSC	0	Reads the interrupt signal for classification completion. This bit is set to 1 if the output port has completed its classification process.
3	DETC	0	Reads the interrupt signal for detection completion. This bit is set to 1 if the output port has completed its detection process.
2	DCDIS	0	Reads the interrupt signal for a disconnected DC load. This bit is set to 1 if the output port has its DC load disconnected (load < 7.5mA).
1	PGC	0	Reads the interrupt signal for the power good (PG) status change. This bit is set to 1 if the output port has a new PG status.
0	PEC	0	Reads the interrupt signal for the power enable status change. This bit is set to 1 if the output port has changed its enable or disable status.

INTERRUPT_MASK (01h)

Access: Read/write

The INTERRUPT_MASK command configures certain interrupt signals. Write 1 to enable the interrupt function; write 0 to disable the interrupt function. “A” is 1 if the AUTO pin is set high during start-up or a reset. “A” is 0 if the AUTO pin is set low.

These bits only disable the response from the INT1 and INT2 pins. INTERRUPT (00h) always changes. The device cannot mask certain interruptions during start-up or a reset event, including V_{IN} and V_{CC} UVLO.

Bits	Bit Name	Default	Description
7	VINF_M	1	Masks the interrupt signal for V_{IN} power failures. Set this bit to 0 to disable the interrupt function.
6	STF_M	A	Masks the interrupt signal for start-up failures. Set this bit to 0 to disable the interrupt function.
5	OCP_M	A	Masks the interrupt signal for OC conditions. Set this bit to 0 to disable the interrupt function.

4	CLSC_M	0	Masks the interrupt signal for classification completion. Set this bit to 0 to disable the interrupt function.
3	DETC_M	0	Masks the interrupt signal for detection completion. Set this bit to 0 to disable the interrupt function.
2	DCDIS_M	A	Masks the interrupt signal for DC load disconnection. Set this bit to 0 to disable the interrupt function.
1	PGC_M	0	Masks the interrupt signal for the PG status change interrupt. Set this bit to 0 to disable the interrupt function.
0	PEC_M	0	Masks the interrupt signal for the power enable status change interrupt. Set this bit to 0 to disable the interrupt function.

INTERRUPT_PRIORITY (02h)

Access: Read/write

The INTERRUPT_PRIORITY command configures certain interrupt signals. If a bit is set to 1, the INT2 pin pulls low in response to the corresponding interrupt signal. The INT1 pin responds to all interrupt sources as long as they are not masked. INT2 only responds to the interrupt sources that are not masked.

Bits	Bit Name	Default	Description
7	VINF_P	1	This bit is selected if the INT2 pin responds to a V_{IN} power failure interrupt signal.
6	STF_P	0	This bit is selected if the INT2 pin responds to a start-up failure interrupt signal.
5	OCP_P	1	This bit is selected if the INT2 pin responds to an OC interrupt signal.
4	CLSC_P	0	This bit is selected if the INT2 pin responds to a classification completion interrupt signal.
3	DETC_P	0	This bit is selected if the INT2 pin responds to a detection completion interrupt signal.
2	DCDIS_P	0	This bit is selected if the INT2 pin responds to a DC load disconnect interrupt signal.
1	PGC_P	0	This bit is selected if the INT2 pin responds to a PG status change interrupt signal.
0	PEC_P	0	This bit is selected if the INT2 pin responds to a power enable status change interrupt signal.

CONFIGURATION AND CONTROL COMMANDS

OPERATION_MODE_SETTING (03h)

Access: Read/write

The OPERATION_MODE_SETTING command configures the modes.

Bits	Bit Name	Default	Description
7:2	RESERVED	-	Reserved.
1:0	MODE	AA	Sets the mode. “A” is 1 if the AUTO pin is set high during start-up or a reset. “A” is 0 if the AUTO pin is set low. The status is latched only during start-up or a reset. This can be changed via the I^2C. 00: Shutdown mode. The port is off, and there is no detection or classification process 01: Manual mode. There is no automatic state change 10: Semi-automatic mode. The detection and classification processes are automated, but the port does not turn on automatically 11: Automatic mode. The start-up, detection, and classification processes are automated

MIDSPAN_SETTING (04h)

Access: Read/write

The MIDSPAN_SETTING command configures midspan mode.

Bits	Bit Name	Default	Description
7:1	RESERVED	-	Reserved.
0	MID	M	Sets midspan mode. “M” is 1 if the MID pin is set high during start-up or a reset. “M” is 0 if the MID pin is set low. These changes can be configured by writing to the I^2C. Set this bit to 1 to enable midspan mode.

PORT_ENABLE (05h)

Access: Read/write

The PORT_ENABLE command configures port enable signals.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	ENAL	1	Enables the MP3921. If this bit is set to 1, all internal IC circuits are enabled. The Port is enabled if the ENAL and EN bits are set to 1. If ENAL is disabled, the I^2C continues to operate, but the port shuts down.
3:1	RESERVED	-	Reserved.
0	EN	1	Enables the port. This bit can disable the port, which includes detection and classification processes, resets the port and status registers, and shuts down the port. If the port is already turned off and this bit is set to 0, then there is no change. 1: Enabled 0: Disabled

DET/CLS_ENABLE (06h)

Access: Read/write

The DET/CLS_ENABLE command configures the detection and classification process enable signals. “A” is 1 if the AUTO pin is set high during start-up or a reset. “A” is 0 if the AUTO pin is set low. In automatic and semi-automatic mode, the detection and classification processes are enabled when the bit is set to 1. In manual made, set the bit to 1 for one-time detection or classification. Then the bit is reset to 0.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	CLSEN	A	Enables the classification process for the port. Set this bit to 1 to enable classification.
3:1	RESERVED	-	Reserved.
0	DETEN	A	Enables the detection process for the port. Set this bit to 1 to enable detection.

DISCONNECT_ENABLE (07h)

Access: Read/write

The DISCONNECT_ENABLE command configures the DC load disconnection function enable signal.

Bits	Bit Name	Default	Description
7:1	RESERVED	-	Reserved.
0	DISEN	A	Enables DC load disconnection. “A” is 1 if the AUTO pin is set high during start-up or a reset. “A” is 0 if the AUTO pin is set low. If this bit set to 1, the DC load disconnection function is enabled.

FAULT_TIMER (08h)

Access: Read/write

The FAULT_TIMER command configures certain timers. The timer begins counting up after a load triggers the threshold. If the current drops below the threshold, then the timer begins counting down at 1/16 of the rising rate. If it times out, the port shuts down. The port cannot be redetected once the timer counts down to 0ms.

Bits	Bit Name	Default	Description
7:6	RESERVED	-	Reserved.
5:4	TINRUSH	10	Sets the start-up inrush current timer. 00: 15ms 01: 30ms 10: 60ms 11: 120ms
3:2	TILIM	11	Sets the current-limit trigger timer after start-up. 00: 7.5ms 01: 15ms 10: 30ms 11: 60ms
1:0	TCUT	10	Set the OC timer after start-up. 00: 15ms 01: 30ms 10: 60ms 11: 120ms

FOLDBACK_ILIM (0Bh)

Access: Read/write

The FOLDBACK_ILIM command configures the foldback OC threshold.

Bits	Bit Name	Default	Description
7:1	RESERVED	-	Reserved.
0	FBLIMT	1	Sets the foldback OC threshold when the OUT pin exceeds 46V. 0: The foldback current limit is 22mV (88mA if R_{SENSE} = 0.25Ω) 1: The foldback current limit is 40mV (160mA R_{SENSE} = 0.25Ω)

2-EVENT_AND_CLASS_5_ENABLE (0Ch)

Access: Read/write

The 2-EVENT_AND_CLASS_5_ENABLE command configures two-event and Class 5 classification enable signals.

“A” is 1 if the AUTO pin is set high during start-up or a reset. “A” is 0 if the AUTO pin is set low. “C” is 1 if the CLS5 pin is set high during start-up or a reset. “C” is 0 if the CLS5 pin is set low. The CLS5 pin has a high power level under the IEEE802.3 at classification, but it is not a standard class level that is compatible with IEEE802.3.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	CLS5_EN	C	Enables Class 5 classification. If this bit set to 1, Class 5 classification is enabled, and the default current limit can support up to 40W of power.
3:1	RESERVED	-	Reserved.
0	2EVNTEN	A	Enables two-event classification. If this bit is set to 1, two-event classification is enabled when the first classification result on the port is Class 4 or Class 5.

INTERRUPT_ENABLE_CONTROL (0Eh)

Access: Read/write

The INTERRUPT_ENABLE_CONTROL command configures the interrupt enable control signals.

Bits	Bit Name	Default	Description
7:3	RESERVED	-	Reserved.
2	CLRPIN	0	Controls the reset function for the INT1 and INT2 pins. If this bit is set to 1, resetting the INT1 and INT2 pins does not affect the registers. This bit is automatically set to 0 after the INT1 and INT2 pins are reset.
1	CLRAINT	0	Controls the reset function for the interrupt source. If this bit is set to 1, all registers as well as the INT1 and INT2 pins are reset. This bit is automatically set to 0 after the INT1 and INT2 pins are reset.
0	INTEN	1	Enables the interrupt function. This bit does not affect the event register. If this bit is set to 1, the interrupt function is enabled.

GENERAL_ENABLE_CONTROL (0Fh)

Access: Read/write

The GENERAL_ENABLE_CONTROL command configures the I²C watchdog and analog-to-digital converter (ADC) enable signals. “A” is 1 if the AUTO pin is set high during start-up or a reset. “A” is 0 if the AUTO pin is set low.

Bits	Bit Name	Default	Description
7:2	RSVD	-	Reserved.
1	ADCEN	1	Enables the ADC. If this bit is set to 1, the ADC is enabled.
0	WDEN	0	Enables the I²C watchdog. If this bit is set to 0, the watchdog is disabled.

MANUAL MODE AND LEGACY DETECTION CONTROL COMMANDS

DET/CLS_TRIGGER (10h)

Access: Read/write

The DET/CLS_TRIGGER command configures the detection and classification trigger signals. In manual mode, one-time detection or classification occurs after the bit is set. In semi-automatic or automatic mode, detection and classification are controlled by the DETEN and CLSEN bits from the DET/CLS_ENABLE (06h) command. These processes are repeated once they are enabled.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	RCLS	0	Re-enables the classification function. If this bit is set to 1, a one-time classification event is enabled. This bit is reset after classification is complete.
3:1	RESERVED	-	Reserved.
0	RDET	0	Re-enables the detection function. If this bit is set to 1, a one-time detection event is enabled. This bit is reset after detection is complete.

POWER_ON/OFF_TRIGGER (11h)

Access: Read/write

The POWER_ON/OFF_TRIGGER command configures power-on/-off trigger signals.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	POFF	0	Triggers a shutdown on the port. If this bit is set to 1, the port shuts down. The bit automatically resets afterward.
3:1	RESERVED	-	Reserved.
0	PON	0	Triggers start-up on the port. If this bit is set to 1, the port starts up. This bit is reset after start-up is complete. The device performs a detection cycle first if the DETEN bit from the DET/CLS_ENABLE (06h) command and this bit are set simultaneously. This bit is operational in manual mode. If the port is powered on or in shutdown mode, then the port does not respond to this bit. This bit is operational in semi-automatic mode. If the detection and classification results are valid, then the port responds to this bit. This bit is only functional during legacy detection if the device is set to automatic mode. For all modes, this bit may be cleared by detection, classification, and legacy detection (DET/CLS/LEGACY_DET) failures, start-up failures, or if the PON signal lasts for 400ms when the port is operational.

LEGACY_ENABLE (12h)

Access: Read/write

The LEGACY_ENABLE command configures the enable signals in legacy detection mode.

Bits	Bit Name	Default	Description
7:2	RESERVED	-	Reserved.
1:0	LEGEN	00	Enables legacy detection mode. 00: Legacy detection is disabled 01: Legacy detection is enabled while standard detection is disabled 10: Legacy detection is enabled after standard detection is complete 11: Reserved

CURRENT LIMIT CONFIGURATION COMMANDS

ICUT_THRESHOLD (13h)

Access: Read/write

The ICUT_THRESHOLD command configures the port's OC threshold.

Bits	Bit Name	Default	Description
7:3	RESERVED	-	Reserved.
2:0	ICUT	000	Sets the port's OC threshold. The default value is 000. In automatic mode, the bits are set to 000 for Class 0 to Class 3 results, 100 for Class 4 results, and 101 for Class 5 results. In semi-automatic mode or manual mode, the bits do not change unless changes are made via the I^2C. 000 = 93.75mV (375mA with R_{SENSE} = 0.25Ω) 001 = 27.5mV (110mA with R_{SENSE} = 0.25Ω) 010 = 47mV (188mA with R_{SENSE} = 0.25Ω) 011 = 93.75mV (375mA with R_{SENSE} = 0.25Ω) 100 = 162.5mV (650mA with R_{SENSE} = 0.25Ω) 101 = 230mV (920mA with R_{SENSE} = 0.25Ω) 110 = 125mV (500mA with R_{SENSE} = 0.25Ω) 111 = 156.25mV (625mA with R_{SENSE} = 0.25Ω)

ILIM_THRESHOLD (17h)

Access: Read/write

The ILIM_THRESHOLD command configures port's over-current limit (OCL).

Bits	Bit Name	Default	Description
7:1	RESERVED	-	Reserved.
0	ILIM	0	Sets the port's OCL. The default value is 0. In automatic mode, the bit is set to 0 for Class 0 to Class 3, and set to 1 for Class 4 or Class 5 results. In semi-automatic mode and manual mode, the bit does not change unless changes are made via the I^2C. 0: 106.25mV (425mA if R_{SENSE} = 0.25Ω) 1: 212.5mV. The current limit is 265mV under Class 5 conditions

STATUS COMMANDS

POWER_SOURCE_STATUS1 (20h and 21h)

Access: Read-only (20h), read and clear (21h)

The POWER_SOURCE_STATUS1 command reads certain power source status signals. Read and clear (21h) means that the bit is reset after a read operation. If read on 20h, the bits are not cleared.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	FETF	0	Indicates whether an external power MOSFET failure has occurred. This bit is set to 1 if the external MOSFET has failed. If this occurs, the current limit cannot be reached, or the OUT pin is high after start-up.
3	VCCUV	1	Indicates whether a V_{CC} under-voltage (UV) condition has occurred. This bit is set to 1 if VCC has recovered from a shutdown or reset condition.
2	OTP	0	Indicates whether an over-temperature (OT) condition has occurred. This bit is set to 1 if the junction temperature (T_J) exceeds 150°C. For more details, see the Over-Temperature Protection (OTP) section on page 24.
1	VINOV	0	Indicates whether a V_{IN} over-voltage (OV) condition has occurred. This bit is set to 1 if V_{IN} exceeds 65V.
0	VINUV	1	Indicates whether a V_{IN} UV condition has occurred. This bit is set to 1 if V_{IN} drops below 29.5V.

POWER_SOURCE_STATUS2 (22h and 23h)

Access: Read-only (22h), read and clear (23h)

The POWER_SOURCE_STATUS2 command reads certain power source status signals.

Bits	Bit Name	Default	Description
7:2	RESERVED	-	Reserved.
1	VINOK	0	Indicates whether the V_{IN} source power is working normally. This bit is set to 1 if V_{IN} exceeds 40V.
0	RESERVED	-	Reserved.

DET/CLS_COMPLETE_STATUS (24h and 25h)

Access: Read-only (24h), read and clear (25h)

The DET/CLS_COMPLETE_STATUS command reads the detection and classification process complete status signals.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	CLSC	0	Indicates whether a port has completed its classification process. This bit set to 1 if classification has completed.
3:1	RESERVED	-	Reserved.
0	DETC	0	Indicates whether a port has completed its detection process. This bit set to 1 if detection has completed.

DET/CLS_RESULT (26h)

Access: Read-only

The DET/CLS_RESULT command reads the detection and classification result signals.

Bits	Bit Name	Default	Description
7:4	CLSR	0000	Returns the classification result. 0000: Classification is not done 0001: Class 1 0010: Class 2 0011: Class 3 0100: Class 4 0101: Class 5 0110: Class 0 0111: OC condition 1000: The first and secondary class results do not match If Class 5 is enabled, any current that exceeds Class 4's upper limit is considered a Class 5 result. An OC condition triggers a current limit. If Class 5 is disabled, any current exceeding Class 4's upper limit is considered an OC condition.
3	2EVNTC	0	Indicates whether two-event classification has been completed. This bit is set to 1 if two-event classification has been completed. This bit is only set once Class 4 and Class 5 are successfully detected.
2:0	DETR	000	Indicates detection result. 000: Detection has not completed (default after a power-on reset) 001: The port is shorted (VIN - OUT < 1.5V) 010: The detection capacitance (C_{DET}) is too high (exceeds 5μF) 011: The detection resistance (R_{DET}) is too low (below 19kΩ) 100: Detection is valid (19kΩ < R_{DET} < 26.5kΩ) 101: R_{DET} is too high (exceeds 26.5kΩ) 110: The port is open (<30μA load current) 111: Low impedance to PGND (OUT - PGND < 2V)

POWER_STATUS (2Ah)

Access: Read-only

The POWER_STATUS command reads certain power status signals.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	PG	0	Indicates the PG status. This bit is set to 1 if the port's power is on and the OUT pin voltage is below the PG voltage (V_{PG}). This bit resets once the OUT pin voltage exceeds the V_{PG} threshold with a short deglitch time.
3:1	RESERVED	-	Reserved.
0	PEN	0	Indicates whether power has been enabled. This bit set to 1 if the port starts up.

POWER_STATUS_CHANGE (2Bh and 2Ch)

Access: Read-only (2Bh), read and clear (2Ch)

The POWER_STATUS_CHANGE command reads certain power status change signals.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	PGC	0	Indicates whether the PG status has changed. This bit is set to 1 if the PG status changes.
3:1	RESERVED	-	Reserved.
0	PEC	0	Indicates whether the power status has been enabled or disabled. This bit is set to 1 if the power status changes (disabled or enabled).

OVER_LOAD_STATUS (2Dh and 2Eh)

Access: Read-only (2Ch), read and clear (2Eh)

The OVER_LOAD_STATUS command reads certain over-load status signals.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	OCUT	0	Indicates whether the ICUT timer (t_{ICUT}) has finished counting after I_{CUT} exceeds the OC threshold.
3:1	RESERVED	-	Reserved.
0	STF	0	Indicates a start-up failure. This bit is set to 1 if the start-up inrush timer times out, or if there is a start-up command failure.

CURRENT_LIMIT_STATUS (2Fh and 30h)

Access: Read-only (2Fh), read and clear (30h)

The CURRENT_LIMIT_STATUS command reads the current limit status signals.

Bits	Bit Name	Default	Description
7:1	RESERVED	-	Reserved.
0	OLIM	0	Indicates whether a hardware current limit has been triggered. This bit is set to 1 if a current limit is triggered.

DISCONNECT_STATUS (31h and 32h)

Access: Read-only (31h), read and clear (32h)

The DISCONNECT_STATUS command reads the disconnect status signals.

Bits	Bit Name	Default	Description
7:1	RESERVED	-	Reserved.
0	DCDIS	0	Indicates whether a disconnected DC load event has occurred. This bit is set to 1 if a disconnected DC load event occurs.

WATCHDOG_STATUS (33h)

Access: Read-only

The WATCHDOG_STATUS command reads the watchdog status signals.

Bits	Bit Name	Default	Description
7:1	RESERVED	-	Reserved.
0	WDS	0	Indicates the watchdog status. This bit is set to 0 if the watchdog times out without an active I^2C clock signal from the SCL line monitored for I^2C activity.

PIN_STATUS (34h)

Access: Read-only

The PIN_STATUS command reads the status signals of certain pins.

Bits	Bit Name	Default	Description
7:5	RESERVED	-	Reserved.
4	AUTO	A	Returns the AUTO pin's status during start-up. "A" is 1 if the AUTO pin is set high during start-up or a reset. "A" is 0 if the AUTO pin is set low. This bit is set to 1 if the AUTO pin is pulled high.
3	A3	D	Returns the A3 to A0 pins' statuses during start-up. "D" is 1 if the corresponding pin is set high during start-up or a reset. "D" is 0 if the corresponding pin is set low. These bits are set to 1 if the corresponding pin's voltage is high.
2	A2	D	
1	A1	D	
0	A0	D	

LEGACY_DETECT_RESULT1 (35h)

Access: Read-only

The LEGACY_DETECT_RESULT1 command reads the legacy detection results signals.

Bits	Bit Name	Default	Description
7:4	RESERVED	-	Reserved.
3:0	LEGDET	0000	Returns the legacy detection results. 0000: No legacy detection 0001: Valid (5μF < PD input capacitor < 100μF) 0010: Unable to discharge the PD input capacitance to 2.4V 0100: The first measurement exceeds the 18.5V maximum voltage 0101: The second measurement exceeds the 18.5V maximum voltage 0110: The difference between the measured voltages is below 0.5V

ADC RESULT COMMANDS

PORT_CURRENT (40h and 41h)

Access: Read-only

The PORT_CURRENT command reads the port's ADC current result.

Bits	Bit Name	Default	Description
(40h) 0	PORT_CURRENT_DATA	0	Returns the lower bit of the port's ADC current result.
(41h) 7:0		0000 0000	Returns the higher bits of the port's ADC current result. The output current (I_{OUT}) can be calculated with the following equation: I_{OUT} = 2.4mA x COUNT - 10mA Where COUNT is the unsigned binary integer of the ADC result.

PORT_VOLTAGE (42h and 43h)

Access: Read-only

The PORT_VOLTAGE command reads the port's ADC voltage result.

Bits	Bit Name	Default	Description
(42h) 0	OUT_PIN_VOLTAGE_DATA	0	Returns the lower bit of the port's ADC voltage result.
(43h) 7:0		0000 0000	Returns the higher bits of the port's ADC voltage result. The sum of these two registers is the OUT pin voltage. The port's output voltage (V_{OUT}) can be calculated with the following equation: V_{OUT} = 0.15V x (V_{IN} COUNT - OUT COUNT) Where COUNT is the unsigned binary integer of the ADC result.

INPUT_VOLTAGE (50h and 51h)

Access: Read-only

The INPUT_VOLTAGE command reads the port's ADC V_{IN} result.

Bits	Bit Name	Default	Description
(50h) 0	INPUT_VOLTAGE_DATA	0	Returns the lower bit of the ADC V_{IN} result.
(51h) 7:0		0000 0000	Returns the higher bits of the ADC V_{IN} result. V_{IN} can be calculated with the following equation: V_{IN} = 0.15V x COUNT Where COUNT is the unsigned binary integer of the ADC result.

JUNCTION_TEMPERATURE (52h and 53h)

Access: Read-only

The JUNCTION_TEMPERATURE command reads the port's die temperature result.

Bits	Bit Name	Default	Description
(52h) 0	JUNCTION_TEMPERATURE_DATA	0	Returns the lower bit of the ADC die temperature result.
(53h) 7:0		0000 0000	Returns the higher bits of the ADC die temperature result. T_J can be calculated with the following equation: T_J = 0.4°C x COUNT - 40°C Where COUNT is the unsigned binary integer of the ADC result.

DIE_ID (60h)

Access: Read-only

The DIE_ID command reads the die ID information.

Bits	Bit Name	Default	Description
7:6	FAB	00	Returns the fab location.
5:4	MAJOR_REV	00	Returns the major revision.
3:2	MINOR_REV	00	Returns the minor revision.
1:0	VENDOR_ID	00	Returns the vendor ID.

APPLICATION INFORMATION

Selecting the Input Capacitor

V_{IN} must be between 44V and 57V. C_{IN} maintains the DC input voltage. The system C_{IN} must be rated for 100V and can be aluminum electrolytic capacitors. Place a 0.1µF decoupling ceramic capacitor close to VIN and PGND to bypass VIN.

Selecting the VCC Capacitor

The MP3921 integrates the VCC pin (about 3.3V) to power the internal control circuit. The internal regulator requires a minimum 1µF ceramic bypass capacitor to be connected between the VCC and DGND pins. The VCC current limit is typically 17mA. Do not connect a heavy external load to VCC, as V_{CC} may drop. This can result in a high VIN to VCC low-dropout (LDO) power loss.

Selecting the Output Capacitor

An output capacitor (C_{OUT}) must be placed between the VIN and OUT pins for the MP3921's output. It is recommended to use a 0.1µF, 100V ceramic capacitor.

Output Transient Voltage Suppression (TVS)

The port's transient voltage suppression (TVS) should be rated for the expected port surge environment. TVS devices should have a minimum reverse standoff voltage of 58V, as well as a maximum clamping voltage of 95V at the expected peak surge current.

Selecting the Output MOSFET

The port's MOSFET can be a small, inexpensive device with average performance characteristics, provided the following conditions are met:

- The voltage rating should be a minimum of 100V for high-voltage surge environments.
- The on resistance ($R_{DS(ON)}$) should be below 150mΩ for power dissipation.
- The power dissipation for the power MOSFET (Q1) when $R_{DS(ON)}$ = 100mΩ at the maximum I_{CUT} is about 85mW.
- The gate charge (Q_G) when V_{GATE} = 10V should be below 50nC to satisfy faster response times under overload conditions.
- V_{GATE} should be 20V to establish a sufficient margin while GATE is about 10V.

The FDMC3612 is recommended for most applications.

Selecting the SENSE Resistor

The load current in the PSE port is sensed as the voltage across a current-sense resistor (R_{SENSE}, which is about 250mΩ). For more accurate current sensing, a Kelvin sense is provided through the SGND and SENSE pins.

Figure 16 shows the typical output components.

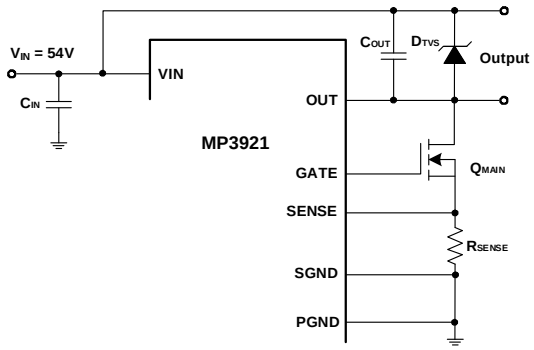


Figure 16: Typical Output Components

Selecting the Digital I/O Pull-Up Resistors

EN

EN is the enable input pin that can turn all internal circuits and the port on and off (except for the VCC regulator). Connect EN to VCC through a 100kΩ resistor to automatically turn on the MP3921.

AUTO

The AUTO pin sets automatic mode. AUTO is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added). Float the AUTO pin for automatic mode. Connect AUTO to DGND for shutdown mode.

MID

The MID pin sets midspan mode. MID is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added). Float the MID pin for midspan mode and wait 2.8s before reinitiating detection. Connect MID to DGND to disable midspan mode.

A0 to A3

The A0 to A3 pins set the MP3921's address. These pins are internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added). Connect these pins to VCC or DGND to set the lower 4 bits of the address (address = 010 A3 A2 A1 A0).

CLS5

The CLS5 pin enables Class 5. CLS5 is internally pulled down to DGND through a 50kΩ resistor. Leave CLS5 disconnected to disable the classification for Class 5 devices. (This is a high power level with the same classification as IEEE802.3at, which is not the standard class level that is compatible with IEEE802.3.) Connect CLS5 to VCC to enable the classification of Class 5 devices.

SCL and SDAI

SCL and SDAI are the I^2C input pins. They must be connected to VCC through an external pull-up resistor (typically 4.7kΩ). If the I^2C interface is not used, then connect the SCL pin to VCC, and connect the SDAI pin to DGND.

SDAO

SDAO is open-drain output pin as well as the I^2C serial data output pin. Connect SDAO to VCC through an external pull-up resistor (typically 4.7kΩ). Connect SDAO to SDAI for non-isolated applications. If the I^2C interface is not used, connect SDAO to DGND.

INT1 and INT2

INT1 and INT2 are open-drain outputs that act as the interrupt request pins for all interrupt source events. These pins are set low when the interrupt register is set and the interrupt function is enabled. Connect these pins to VCC through an external pull-up resistor (typically 4.7kΩ). If the interrupt function is not used, connect these pins to DGND.

Over-Current Protection (OCP) and Overload Protection (OLP)

Inrush Current Limit

The MP3921 provides a 425mA I_{INRUSH} limit for inrush protection. When the external MOSFET begins to operate, I_{INRUSH} protection is enabled. This protection allows the PD's C_{IN} to charge to the full V_{IN} on the power interface. It also ensures the pass MOSFET remains within its safe operating range.

If I_{INRUSH} exceeds I_{CUT} during the inrush, then t_{ICUT} begins working. If t_{ICUT} times out, then the output turns off.

ICUT

Following the end of start-up, a two-level current-limit protection scheme is applied to the port. The first level is I_{CUT}, which includes t_{ICUT}. If t_{ICUT} times out because the load current exceeds the I_{CUT} threshold, then the port shuts down. The I_{CUT} threshold is configured by ICUT (13h, bits[2:0]) (see Table 2).

Table 2: ICUT Threshold

ICUT Register Value	I_{CUT} (mA)
000	375
001	110
010	188
011	375
100	650
101	920
110	500
111	625

In automatic mode, the bits are automatically set to 000 for Class 0 to Class 3 results, set to 100 for the Class 4 result, and set to 101 for the Class 5 result, based on the classification result.

ILIM

The second level of current-limit protection is I_{LIM}, which is a hard limit. The GATE pin regulates the load at the current limit, and an additional timer (t_{ILIM}) is enabled to record the current limit event. When t_{ILIM} completes, the port shuts down. The I_{LIM} threshold can be configured via the ILIM_THRESHOLD (17h) command (see Table 3).

Table 3: ILIM Threshold

ILIM Register Value	I_{CUT} (mA)
0	425
1	850 for Class 4
	1060 for Class 5

In automatic mode, the bit is set to 0 for Class 0 to Class 3 results, or they are set to 1 for Class 4 and Class 5 based on the classification result.

Design Example

Table 4 shows a design example following the application guidelines.

Table 4: Design Example

V_{IN}	V_{OUT}	P_{OUT}
44V to 57V	0V to 57V	0W to 30W

Figure 18 on page 46 shows the detailed typical application schematic. The Typical Performance Characteristics section on page 12 shows the typical performance and circuit waveforms. For more device applications, refer to the related evaluation board datasheet(s).

PCB Layout Guidelines

Efficient PCB layout is critical, as poor layout can result in reduced performance, resistive loss, and system instability. For the best results, refer to Figure 17 and follow the guidelines below:

1. Place R_{SENSE} close to the IC. To optimize accuracy, place the SENSE and SGND pins close to R_{SENSE}. This minimizes the impact of the PCB trace resistance.
2. Kelvin connect the top of R1 to the SENSE pin.
3. Kelvin connect the bottom of R1 to the SGND pin.
4. Place C_{IN} (C1B) as close to the VIN and PGND pins as possible.
5. Place the VCC capacitor (C3) as close to the VCC and DGND pins as possible.
6. Place a sufficient number of PGND vias under the MP3921 to provide good thermal dissipation. This also lowers the PCB trace resistance from the bottom of R_{SENSE} to PGND.
7. Use a separate DGND and PGND layout that is connected under the IC package between the DGND and PGND pins.

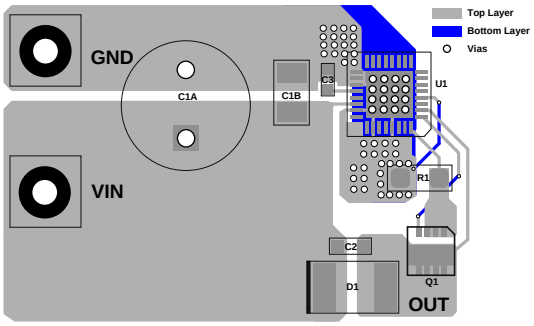


Figure 17: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

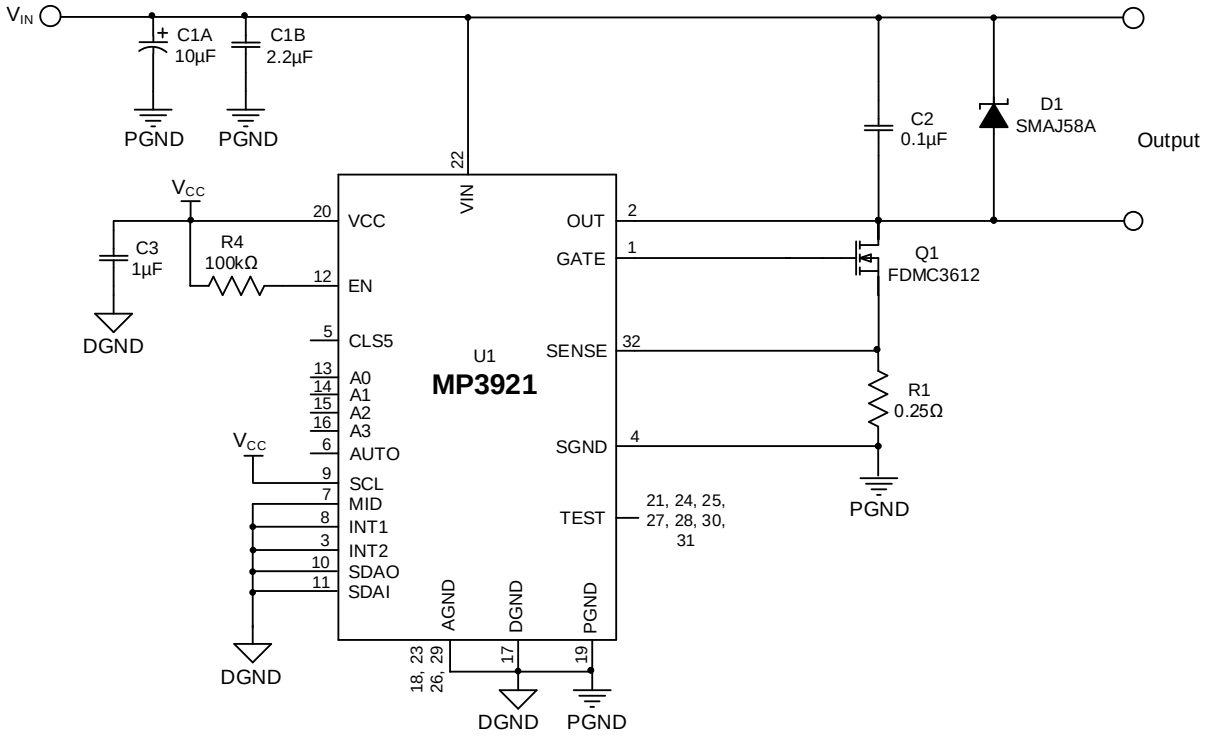
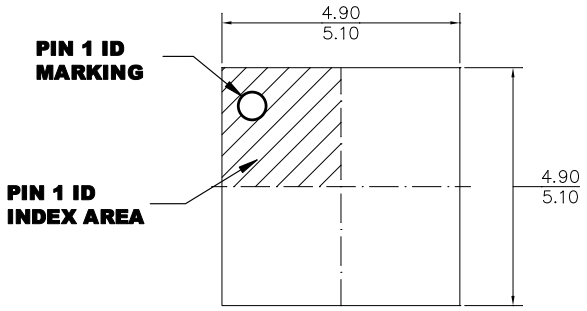


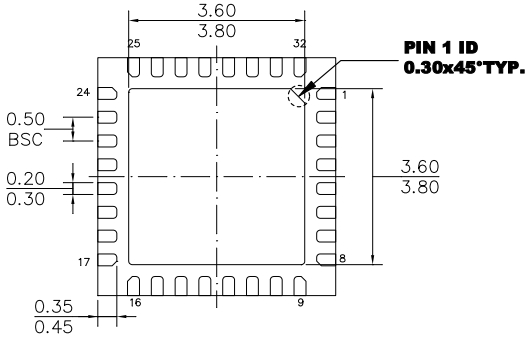
Figure 18: Typical Application Circuit (without I²C Control)

PACKAGE INFORMATION

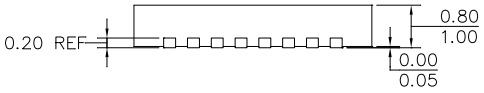
QFN-32 (5mmx5mm)



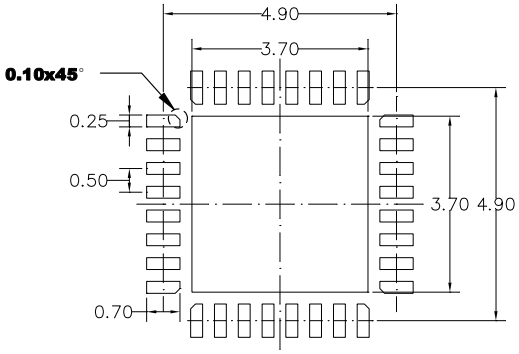
TOP VIEW



BOTTOM VIEW



SIDE VIEW

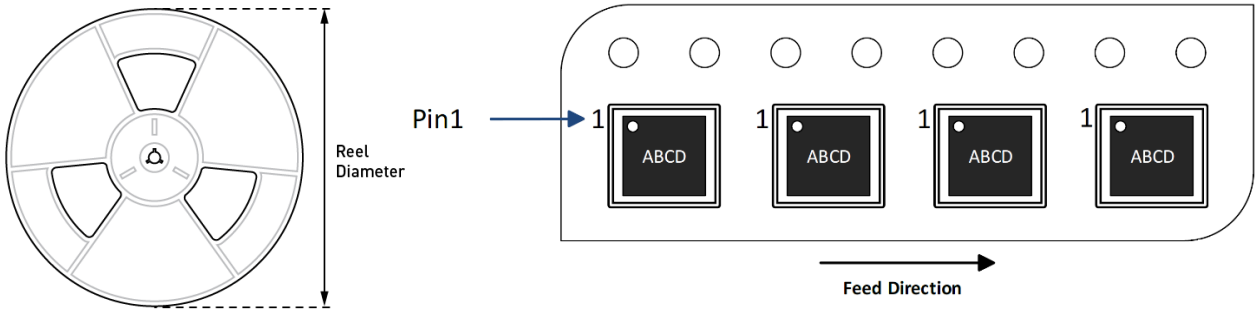


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION WHHE-1.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3921GU-Z	QFN-32 (5mmx5mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/19/2024	Initial Release	-