MP38875

15A, 16V, 800kHz Step-Down Converter with Synchronous Gate Driver

The Future of Analog IC Technology

DESCRIPTION

The MP38875 is a monolithic step-down switch mode converter with a built in internal power MOSFET. It achieves 15A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP38875 requires a minimum number of readily available standard external components and is available in a 20-pin 3mm x 4mm QFN package.

The MP38875 is ideal for a wide range of applications including distributed power systems, pre-regulator for linear regulators, compact DC-DC regulators for PCB space limited platforms.

FEATURES

- Wide 4.5V to 16V Operating Input Range
- 15A Output Current
- 25mΩ Internal Power MOSFET Switch
- Synchronous Gate Driver
- Synch from 300KHz to > 1MHz External Clock or 800KHz Fixed Switching Frequency
- Synch Output to Drive Another Regulator in Phase-Shift Operation
- Feedback Voltage Accuracy: 2%
- Programmable Soft-Start
- Startup Tracking
- EN and Power Good for Power Sequencing
- Cycle-by-Cycle Over Current Protection
- Thermal Shutdown
- Output Adjustable from 0.8V to 12V
- Stable with Low ESR Output Ceramic Capacitors
- Available in a 3mm x 4mm QFN Package

APPLICATIONS

- Distributed Power Systems
- Pre-Regulator for Linear Regulators
- Compact DC-DC Regulator for PCB Space Limited Platforms

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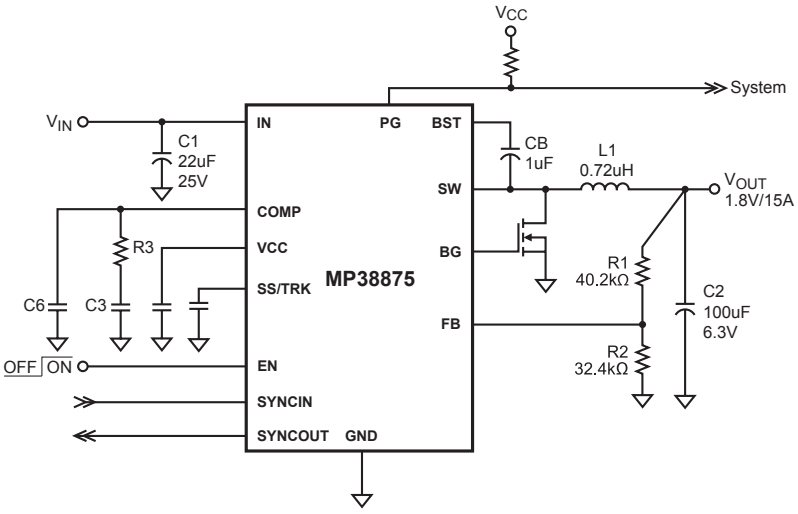
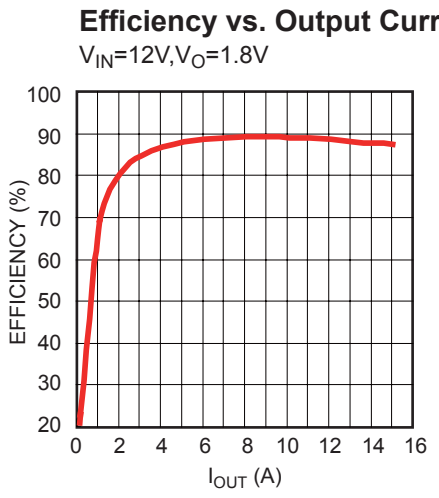
TYPICAL APPLICATION





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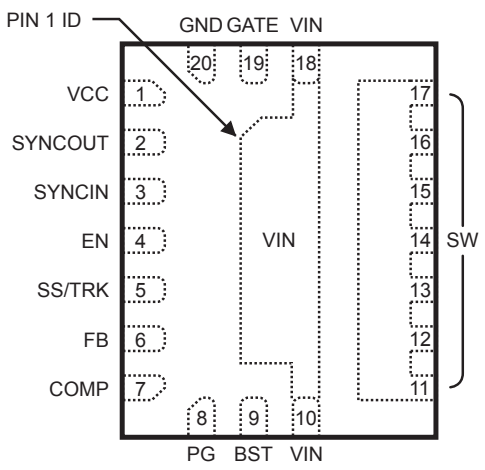
PACKAGE REFERENCE



Part Number*	Package
MP38875DL	3mm x 4mm QFN
Temperature	**Top Marking**
–40°C to +85°C	3887

* For Tape & Reel, add suffix –Z (e.g. MP38875DL–Z)
For RoHS compliant packaging, add suffix –LF
(e.g. MP38875DL–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 18V
V_{SW} ..... –0.3V (-5V for < 10ns) to 19V
V_{BS} ..... V_{SW} + 6V
All Other Pins ..... –0.3V to +6V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (2)

Supply Voltage V_{IN} ..... 4.5V to 16V
Output Voltage V_{OUT} ..... 0.8V to V_{IN} -4V
Operating Temperature ..... –40°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
QFN (3mm x 4mm)	48	11	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 16V	0.794	0.810	0.826	V
Feedback Current	I_{FB}	V_{FB} = 0.8V		10		nA
Switch On Resistance (4)	$R_{DS(ON)}$			25		mΩ
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0.1	10	μA
Current Limit (4)				21		A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V, $SYNC_{IN}$ = 0V		800		KHz
Fold-back Frequency		V_{FB} = 0V		200		KHz
Maximum Duty Cycle		V_{FB} = 0.6V		90		%
Minimum On Time(4)	t_{ON}			100		ns
Soft-Start Charging Current	I_{SS}	V_{SS} = 0V		8		μA
Maximum COMP Level	V_{COMP_MAX}	V_{FB} = 0.6V		4.4		V
Gain of Error Amplifier	G_{EA}	V_{COMP} = 1.5V		2		mA/V
Error Amplifier Sink Current		V_{COMP} = 1.5V		–270		μA
Error Amplifier Source Current		V_{COMP} = 1.5V		+270		μA
Power Good Ramp Up Threshold				90		%
Power Good Ramp Down Threshold				85		%

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Good Delay				20		µs
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V		10		nA
V_{CC} Tolerance	V_{CC}	I_{CC} = 0mA		5.3		V
V_{CC} Regulation		I_{CC} = 0~20mA		5		%
Sync Frequency	F_{SYNC}		0.3		1	MHz
SYNCIN Bias Current	I_{SYNCIN}			10		nA
SYNCIN Logic High Voltage			2			V
SYNCIN Logic Low Voltage					0.4	V
SYNCHOUT High Level		V_{CC} = 5V, Source 5mA		4.6		V
SYNCHOUT Low Level		V_{CC} = 5V, Sink 5mA		0.4		V
Under Voltage Lockout Threshold Rising			3.85	4.1	4.35	V
Under Voltage Lockout Threshold Hysteresis				900		mV
EN Input Low Voltage					0.4	V
En Input High Voltage			2			V
EN Input Current		V_{EN} = 2V		2		µA
		V_{EN} = 0V		0.1		
Supply Current (Shutdown)		V_{EN} = 0V		0.1		µA
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 1V		1.0		mA
Thermal Shutdown				150		°C
Gate Driver Sink Impedance	R_{SINK}			1		Ω
Gate Driver Source Impedance	R_{SOURCE}			4		Ω
Gate Drive Current Sense Trip Threshold				20		mV
Gate Drive Non-Overlap Time (see Figure 1) (4)	T_{d1}	From BG low to SW high		10		ns
	T_{d2}	From SW low to BG high		10		ns

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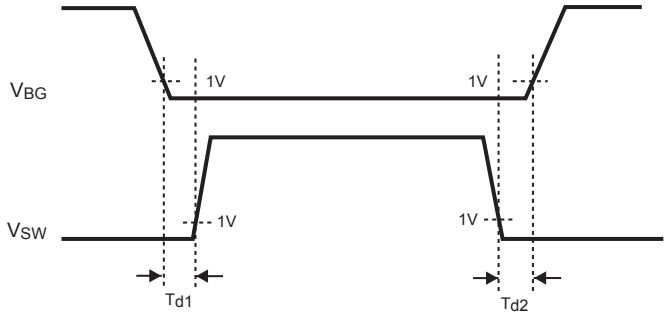

Figure 1—Gate Drive Non-Overlap Time Diagram

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PIN FUNCTIONS

Pin #	Name	Description
1	VCC	BG Driver Bias Supply. Decouple with a 1µF ceramic capacitor.
2	SYNCOUT	Timing output to drive another MP38875 (or similar device) SYNCIN for phase-shift operation.
3	SYNCIN	External Frequency Synchronization. Connect to GND if not used.
4	EN	On/Off Control.
5	SS/TRK	Soft-Start/Track Input. Connect a capacitor to ground.
6	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV.
7	COMP	Compensation. Connect R/C network to ground.
8	PG	Power Good Indicator. Connect this pin to V_{CC} or V_{OUT} by a 100kΩ pull-up resistor. The output of this pin is an open drain if the output voltage is within 10% of the nominal voltage, otherwise it is LOW. If PG is initially at open drain, there is a 20µs delay to pull PG if the output voltage is less than 10% regulation window.
9	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BS pins to form a floating supply across the power switch driver.
10, 18, Exposed Pad	VIN	Supply Voltage. The MP38875 operates from a +4.5V to +16V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
11-17	SW	Switch Output. These pins are fused together.
19	GATE	Gate Driver Output. Connect this pin to the synchronous MOSFET.
20	GND	Ground.

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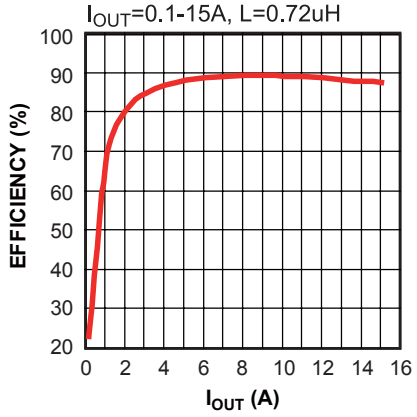
TYPICAL PERFORMANCE CHARACTERISTICS

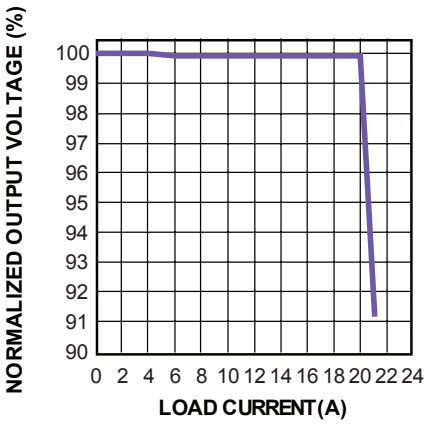
V_{IN}=12V, V_{OUT}=1.8V, L=0.72uF, T_A = +25ºC, unless otherwise noted.

Efficiency vs. Output Current

I_{OUT}=0.1-15A, L=0.72uH

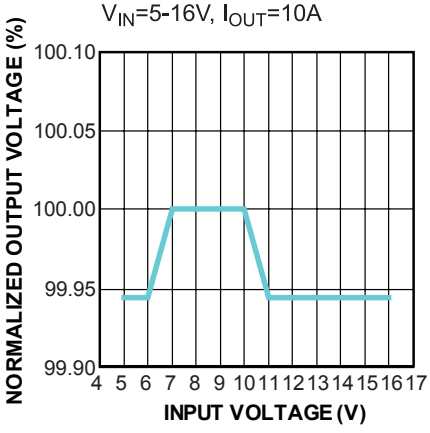


Load Regulation

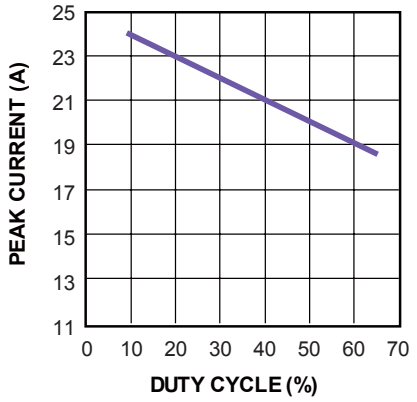


Line Regulation

V_{IN}=5-16V, I_{OUT}=10A

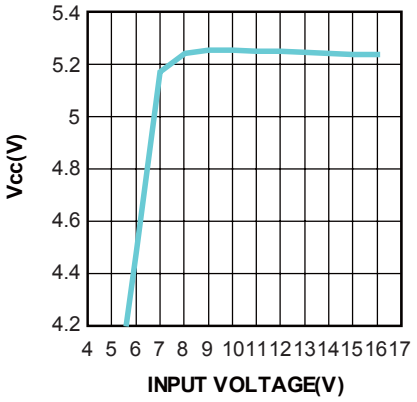


Peak Current vs. Duty Cycle



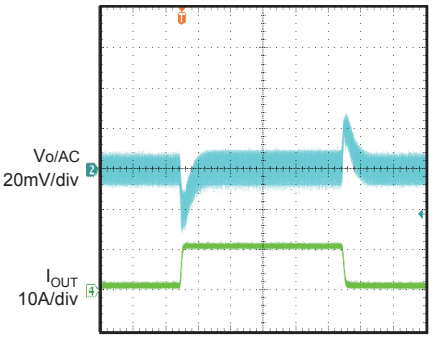
Vcc Regulator Line Regulation

V_{IN}= 5-16V, V_{OUT}=1.8V, I_{OUT}=0A



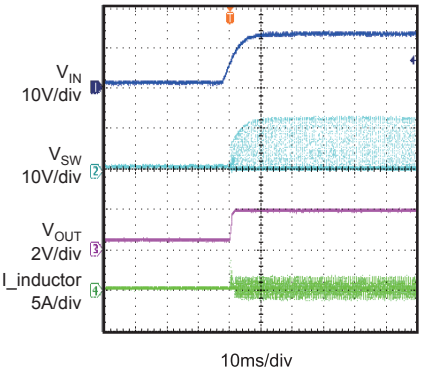
Transient Response

V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=0-10A, 1A/us



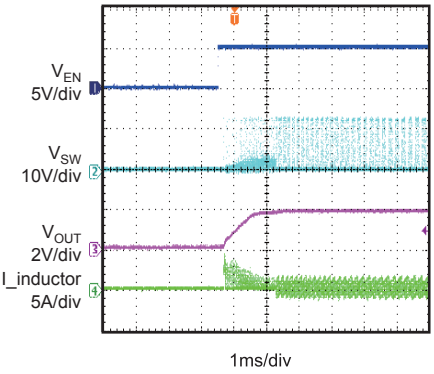
Power up

V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=0A



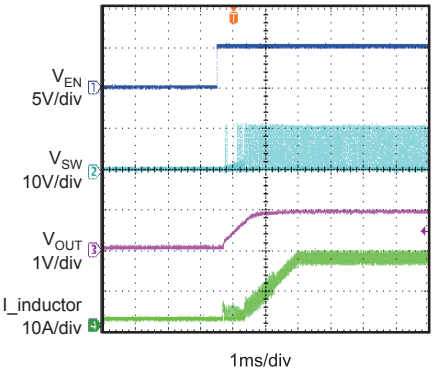
Startup through Enable

V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=0A



Startup through Enable

V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=15A



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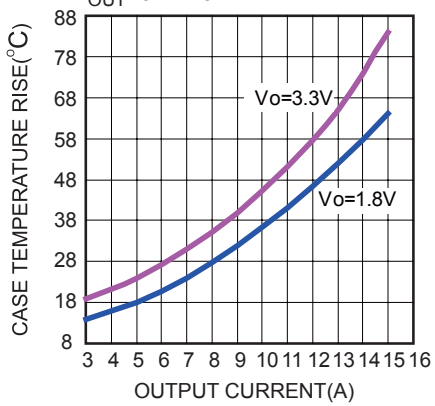
TYPICAL PERFORMANCE CHARACTERISTICS (*CONTINUED*)

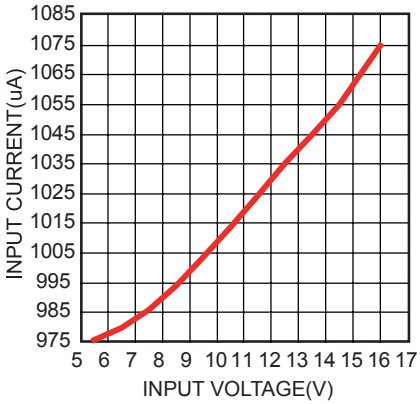
V_{IN}=12V, V_{OUT}=1.8V, L=0.72uF, T_A = +25°C, unless otherwise noted.

Case Temperature Rise vs. Output Current

I_{OUT}=3A - 15A

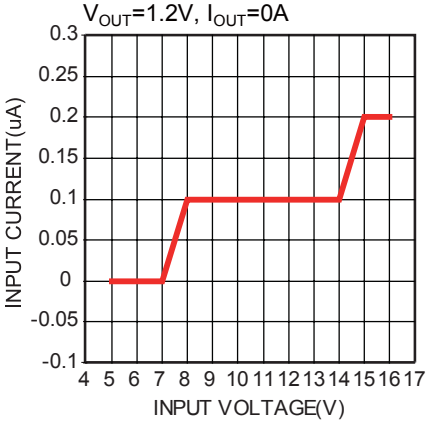


Enabled Supply Current vs. Input Voltage



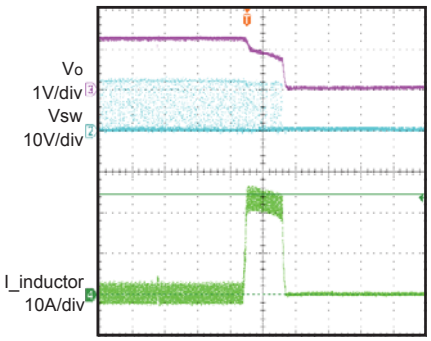
Disabled Supply Current vs. Input Voltage

V_{OUT}=1.2V, I_{OUT}=0A



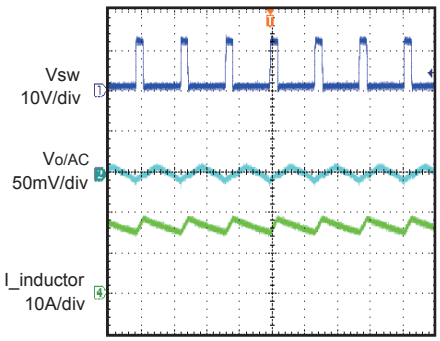
Output Short Circuit

I_{OUT}=0A



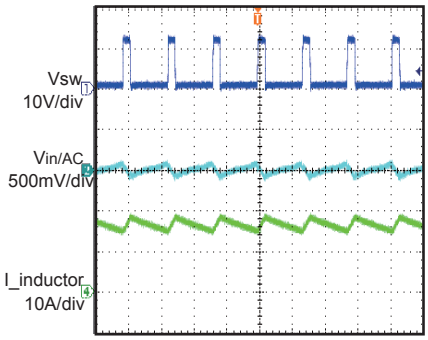
Output Ripple

V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=15A



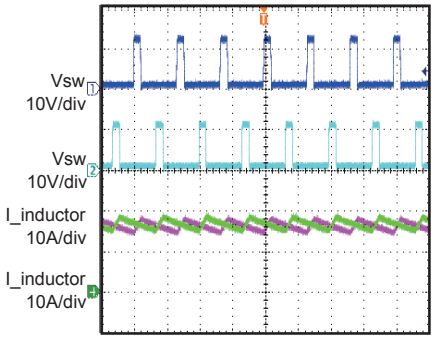
Input Ripple

V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=15A



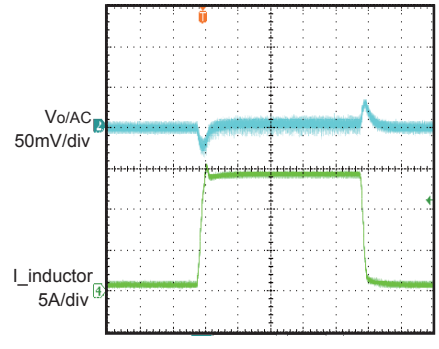
Two Phase Steady State Waveform

I_{OUT}=30A



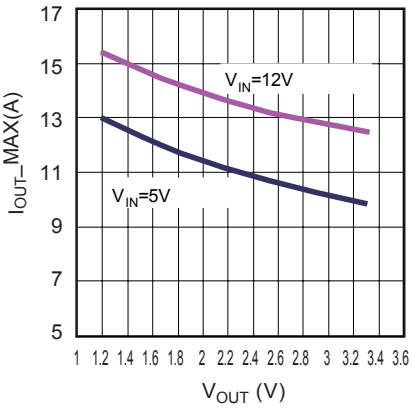
Two Phase Transient Response

I_{OUT}=1A - 20A, 1A/us



Current Derating Curves

$T_{_RISE}$=65°C



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FUNCTION BLOCK DIAGRAM

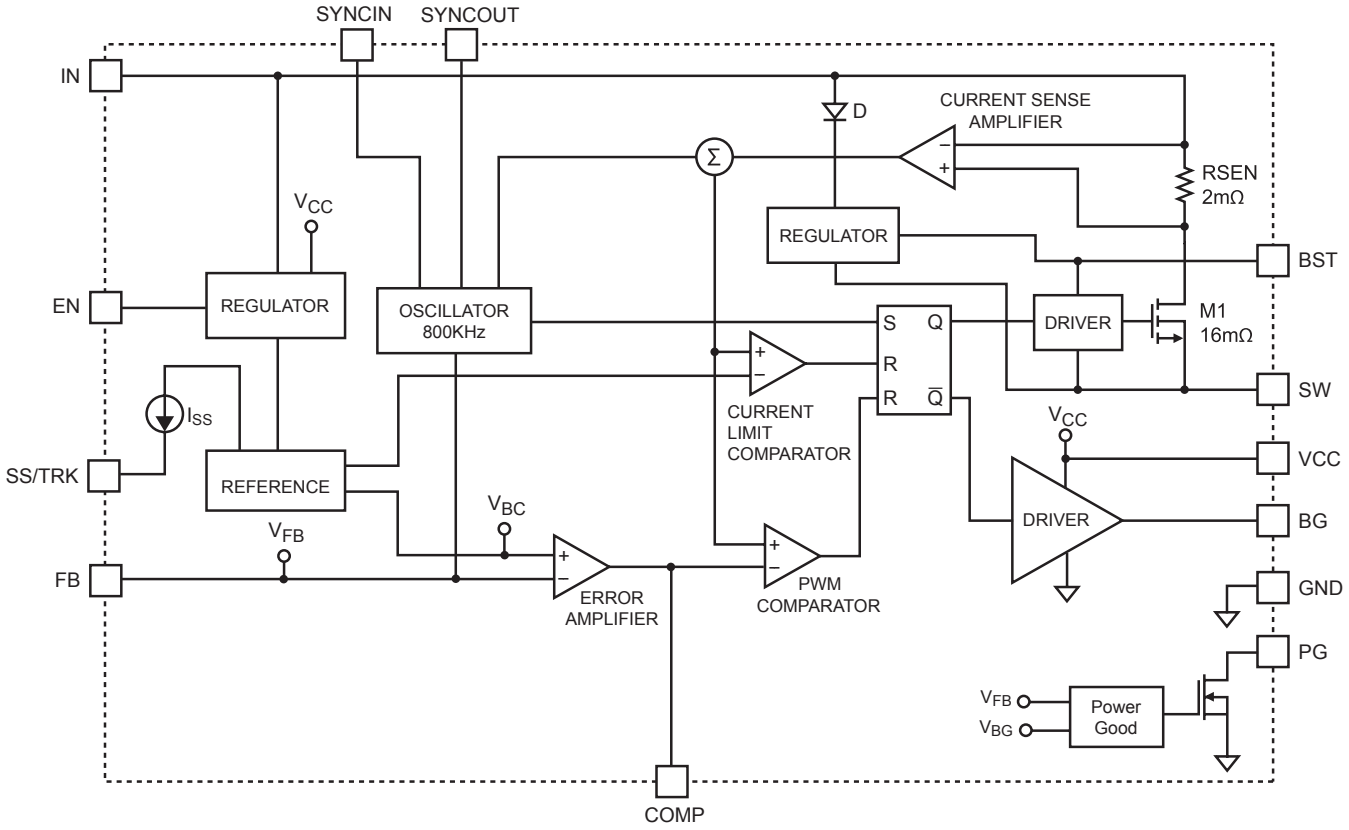

Figure 2—Functional Block Diagram

OPERATION

The MP38875 is a fixed frequency, synchronous, step-down switching regulator with an integrated high-side power MOSFET and a gate driver for a low-side external MOSFET. It achieves 15A continuous output current over a wide input supply range with excellent load and line regulation. It provides a single highly efficient solution with current mode control for fast loop response and easy compensation.

The MP38875 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the external compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized external compensation network minimizes the external component counts and simplifies the control loop design. See Application Information for compensation network design.

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Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases. Since this internal regulator provides the bias current for the bottom gate driver that requires significant amount of current depending upon the external MOSFET selection, a 1µF ceramic capacitor for decoupling purpose is required.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP38875 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is a consistent 3.2V.

Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal current source (10µA) charges up an external soft start capacitor C_{SS} from 0V t o 1.2V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

Over-Current-Protection and Latch off

The MP38875 has cycle-by-cycle over current limit. If the soft start Voltage is greater than 1.2V, and inductor current exceeds the current limit threshold, and FB voltage drops below 50% of reference Voltage, then the MP38875 goes into latch off until En or IN is recycled. This protection mode is especially useful when the output is dead-short to ground.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M3, C4, L1 and C2 (Figure 3). If (V_{IN}-V_{SW}) is more than 5V, U2 will regulate M3 to maintain a 5V BST voltage across C4.

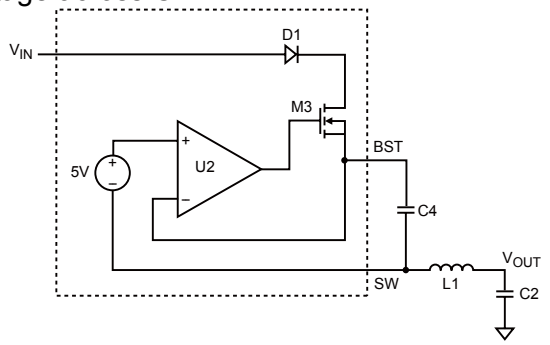

Figure 3—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Synchin/Synchout Control

The MP38875 has a dedicated synchin control pin (SYNCIN) that allows MP38875 be synchronized to external clock ranging from 300KHz up to 1 MHz. the MP38875 also has a synchout pin (SYNCOUT) generating a 50% duty cycle, 180° out of phase logic signal. The Synchout signal can be used to synchronize a slave phase by connecting the SYNCOUT pin of the master MP38875 with the SYNCIN pin of the slave MP38875. The 180° interleaving operation greatly reduces the requirement of the input decoupling capacitors.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the Typical Application Circuit on the front page). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). Choose R1 to be around 40.2kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	40.2 (1%)	32.4 (1%)
2.5	40.2 (1%)	19.1 (1%)
3.3	40.2 (1%)	13 (1%)
5	40.2 (1%)	7.68 (1%)

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 7mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current, 15A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 200mA, larger inductance is recommended for improved efficiency

Synchronous MOSFET

The external synchronous MOSFET is used to supply current to the inductor when the internal high-side switch is off. It reduces the power loss significantly when compared against a Schottky rectifier.

Table 2 lists example synchronous MOSFETs and manufacturers.

Table 2—Synchronous MOSFETSelection Guide

Manufacture	Part No.
Siliconix	si7336ADP
IR	1RFH7932P6F

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$I_{C1} = \frac{I_{LOAD}}{2}$ For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low.

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The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP38875 can be optimized for a wide range of capacitance and ESR values.

Compensation Components

MP38875 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where A_{VEA} is the error amplifier voltage gain, 9600V/V; G_{CS} is the current sense transconductance, 12.8A/V; R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C3), the output resistor of error amplifier. The other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where, G_{EA} is the error amplifier transconductance, 2.4mA/V.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case (as shown in Figure 3), a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system unstable. A good rule of thumb is to set the crossover frequency to approximately one-tenth of the switching frequency. The Table 3 lists the typical values of compensation components for some standard output voltages with various output capacitors and inductors. The values of the compensation components have been optimized for fast transient.

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Table 3—Compensation Values for Typical Output Voltage / Capacitor

V_{OUT} (V)	L1 (µH)	C2, Ceramic (µF)	C2, Poscap (µF)/ESR(mΩ)	R3 (kΩ)	C3 (nF)	C6 (pF)
1.2	0.82	100X2	None	2.2	10	100
1.2	0.82	47	330/ 9/ 6.3V	5.49	3.3	560
1.8	0.82	47	330/ 9/ 6.3V	8.25	2.2	390
2.5	1.2	47	330/ 9/ 6.3V	11.5	1.5	270
3.3	1.3	47	220/ 18/ 6.3V	8.06	2.7	680
5	1.8	47	220/ 18/ 6.3V	16	1	100

To optimize the compensation components , the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency. Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, below one forth of the crossover frequency provides sufficient phase margin. Determine the C3 value by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

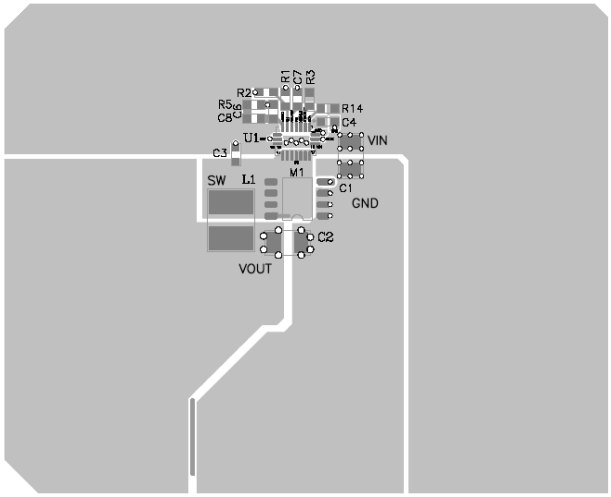
If this is the case, then add the second compensation capacitor (C6) to set the pole f_{P3} at the location of the ESR zero. Determine the C6 value by the equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure 4 for references.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side and low-side MOSFETs.
2) Keep the connection of low-side MOSFET between SW pin and input power ground as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



Top Layer

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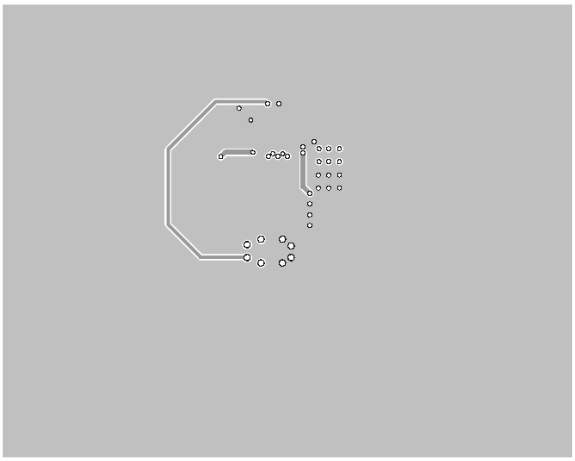

Bottom Layer

Figure 4—PCB Layout

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator. The applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: D= $\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Figure.5

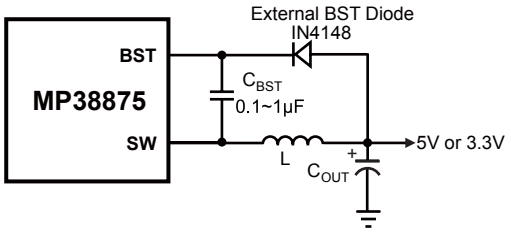

Figure 5—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

Output Voltage Tracking and Sequencing

The MP38875 allows the user to program how its output voltage ramps during startup by means of the SS pin. Through this pin, the output voltage can be set to either coincidentally or rationally track another output voltage, as shown below.

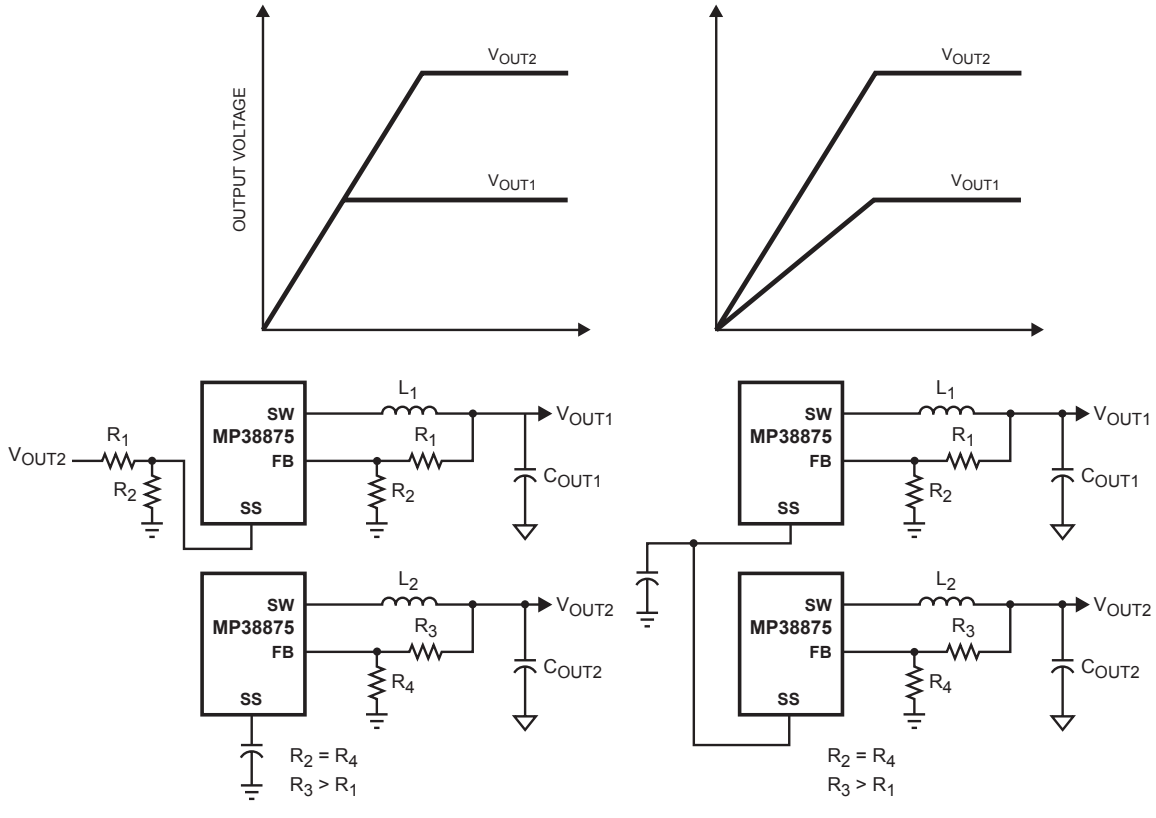

Figure 6—Output Voltage Tracking

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Two Phase Operation

The MP38875 can be configured as a two-phase interleaving regulator to provide up to 30A load current. The current balance is automatically achieved by connecting the two COMP pins together. See Figure 7 for detail configurations.

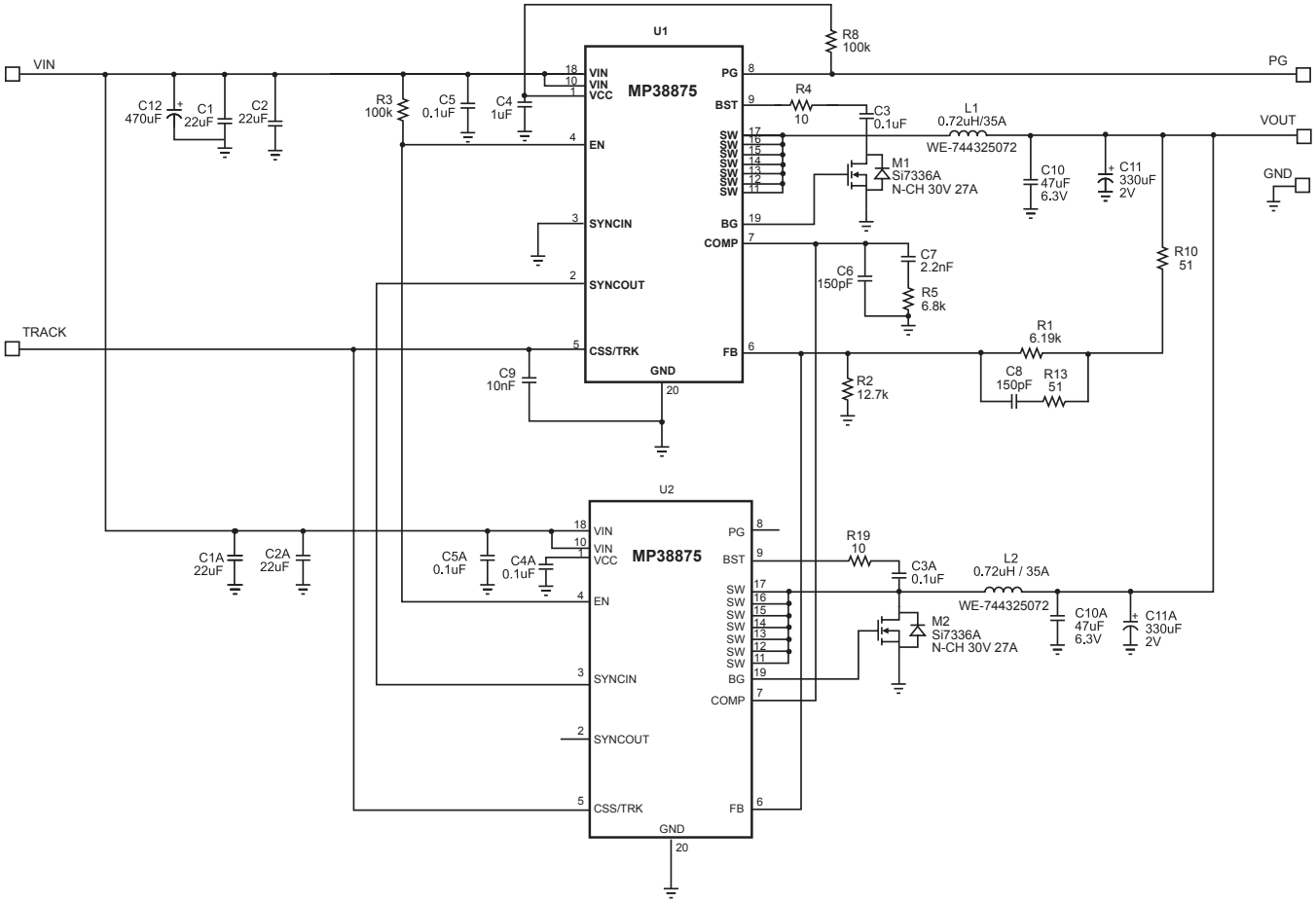

Figure 7—Two Phase Operation

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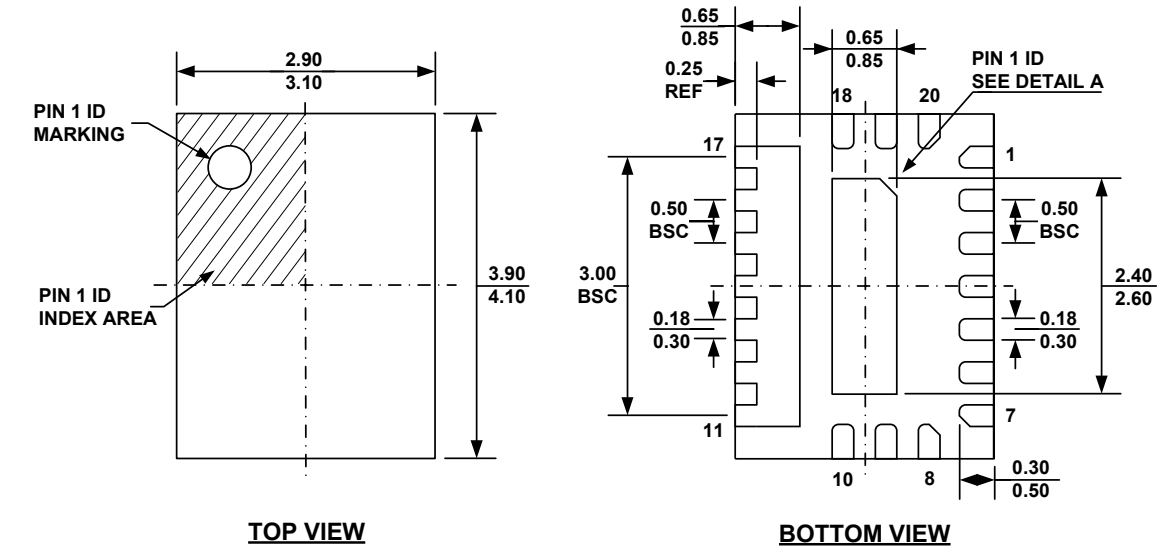
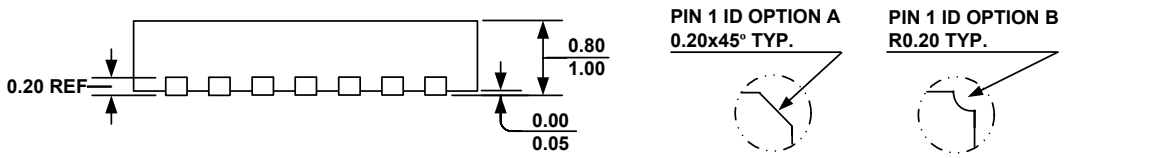
PACKAGE INFORMATION

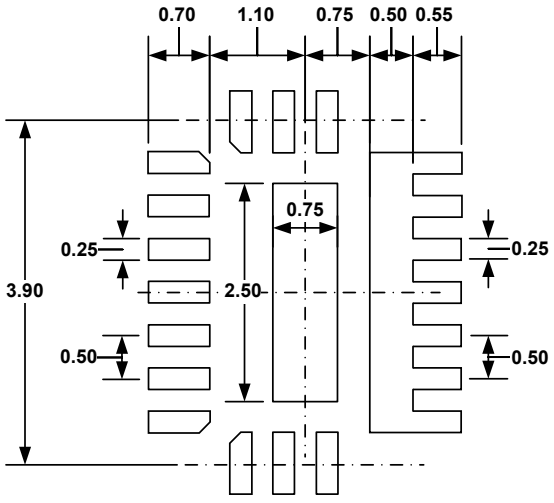
QFN20 (3mm x 4mm)



TOP VIEW **BOTTOM VIEW**



SIDE VIEW **DETAIL A**



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VGED.
5) DRAWING IS NOT TO SCALE.

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