MP3415

3.6A, 1MHz, Synchronous, Step-Up Converter with Output Disconnect

The Future of Analog IC Technology®

DESCRIPTION

The MP3415 is a high-efficiency, synchronous, current-mode, step-up converter with output disconnect.

The MP3415 can start up with an input voltage as low as 1.8V while providing inrush current limiting and output short-circuit protection (SCP). The integrated, P-channel, synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode. The P-channel MOSFET disconnects the output from the input when the MP3415 shuts down. Output disconnect discharges the output completely, allowing the MP3415 to draw a supply current below 1μA in shutdown mode.

The 1MHz switching frequency allows small external components while internal compensation and soft start minimize the external component count, making the MP3415 a compact solution for a wide current load range.

The MP3415 features an integrated power MOSFET that supports an output up to 5.5V and a peak switching current above 3.6A.

The MP3415 is available in a small QFN-12 (2mmx2mm) package.

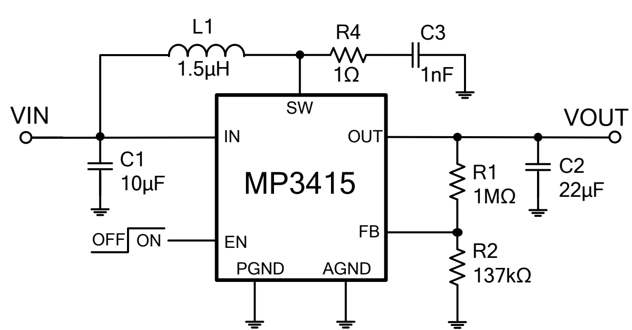
FEATURES

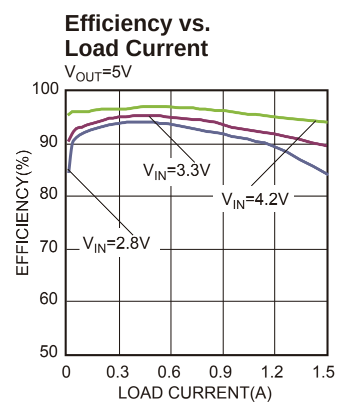
- 1.8V to 5.5V Input Voltage Range
- Output Voltage up to 5.5V
- Supports 5V/1.5A at 2.8V Input
- Internal Synchronous Rectifier
- 1MHz Fixed Switching Frequency
- 22μA Quiescent Current
- <1μA Shutdown Current
- True Output Disconnect from the Input
- Efficiency up to 97%
- Internal Compensation, Inrush Current Limiting, and Internal Soft Start
- Small External Components
- Protection Features Include OVP, SCP, and OTP
- Small QFN-12 (2mmx2mm) Package

APPLICATIONS

- Two-Cell and Three-Cell Alkaline, NiCd or NiMH, or Single-Cell Li Battery Consumer Products
- Personal Medical Devices
- Portable Media Players
- Wireless Peripherals
- Gaming Accessories

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3415GG	QFN-12 (2mmx2mm)	*See Below*

* FOR TAPE & REEL, ADD SUFFIX –Z (E.G. MP3415GG–Z)

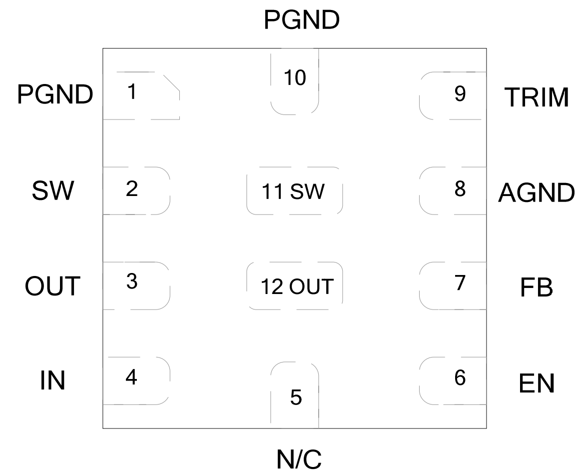
TOP MARKING

EAY
LLL

EA: Product code of MP3415GG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-12 (2mmx2mm)

ABSOLUTE MAXIMUM RATINGS (1)

SW, OUT ....-0.3V to +6.5V
SW (<5ns) ....-0.3V to +9.5V
All other pins ....-0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2)
.... 1.56W
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature................ -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....1.8V to 5.5V
V_{OUT}.............................V_{IN-MAX} x 110% to 5.5V (4)
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-12 (2mmx2mm)...............80 ..... 16... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) If V_{IN} is close to V_{OUT}, the boost converter may trigger the minimum on time. When V_{IN} is higher than V_{OUT}, the boost converter switches between boost mode and linear charge mode. Both conditions result in a $V_{OUT-RIPPLE}$ that is too high and are therefore not recommended.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, T_J = -40°C to 125°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Voltage Range						
Quiescent current	I_Q	V_{EN} = V_{IN} = 3.3V, V_{OUT} = 5V, no load, V_{FB} = 0.65V, measured on OUT, T_J = 25°C		22	30	μA
		V_{EN} = V_{IN} = 3.3V, V_{OUT} = 5V, no load, V_{FB} = 0.65V, measured on IN, T_J = 25°C		8	12	μA
Shutdown current	I_{SD}	V_{EN} = V_{OUT} = 0V, measured on IN, T_J = 25°C		0.1	1	μA
IN under-voltage lockout	V_{IN_UVLO}	V_{IN} rising, T_J = 25°C		1.65	1.7	V
IN under-voltage lockout hysteresis				100		mV
Step-Up Converter						
Operation frequency	F_{SW}		0.8	1.0	1.2	MHz
Feedback voltage reference	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to 125°C	591	600	609	mV
Feedback input current	I_{FB}	V_{FB} = 0.63V		1	50	nA
NMOS on resistance	R_{NDS_ON}			70		mΩ
NMOS leakage current	I_{N_LK}	V_{SW} = 6.5V, T_J = 25°C		0.1	1	μA
PMOS on resistance	R_{PDS_ON}			90		mΩ
PMOS leakage current	I_{P_LK}	V_{SW} = 6.5V, V_{OUT} = 0V, T_J = 25°C		0.1	1	μA
Maximum duty cycle	D_{MAX}		85	95		%
Start-up current limit	I_{ST_LIMIT}	V_{IN} = 4V, V_{OUT} = 0V		0.3		A
		V_{IN} = 4V, $V_{OUT-setting}$ = 3.6V, pull V_{OUT} to 3.3V		0.8		A
NMOS current limit	I_{SW_LIMIT}	Duty = 40%	3.6	4.2	5	A
Logic Interface						
EN input high-level voltage	V_{EN_H}		1.2			V
EN input low-level voltage	V_{EN_L}				0.4	V
EN input current	I_{EN}	Connect to V_{IN}		10		nA
Protection						
Thermal shutdown(6)				155		°C
Over-temperature hysteresis(6)				25		°C

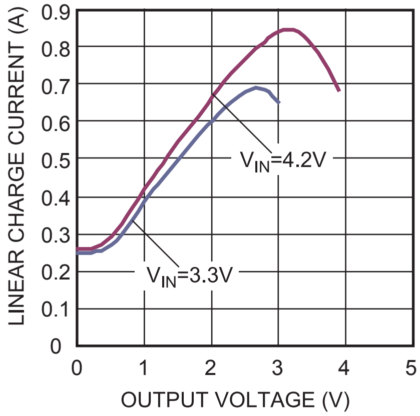
NOTE:

6) Guaranteed by characterization, not tested in production.

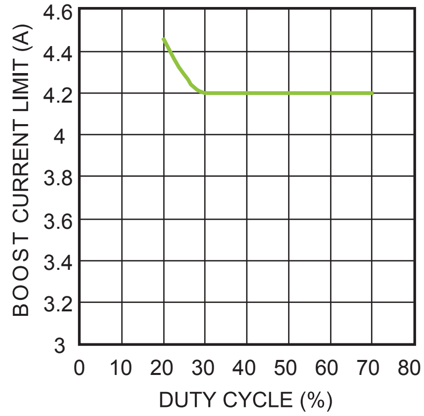
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

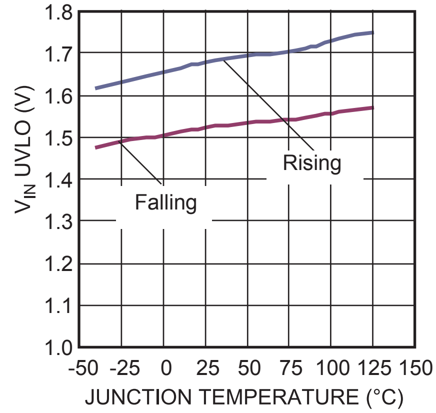
Linear Charge Current vs. Output Voltage



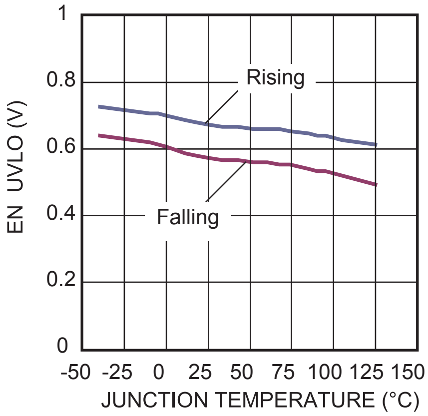
Boost Current Limit vs. Duty Cycle



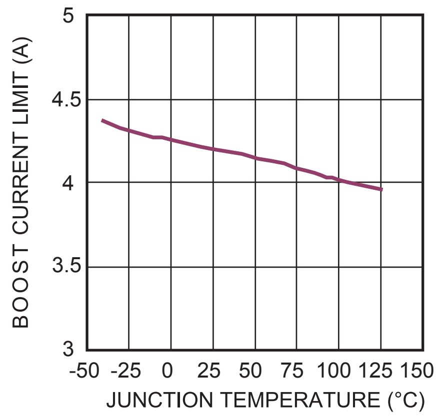
V_{IN} UVLO vs. Junction Temperature



EN UVLO vs. Junction Temperature

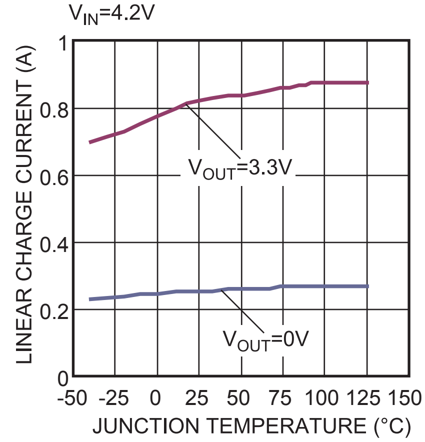


Boost Current Limit vs. Junction Temperature

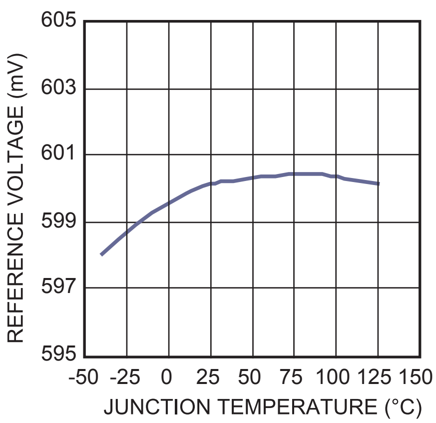


Linear Charge Current vs. Junction Temperature

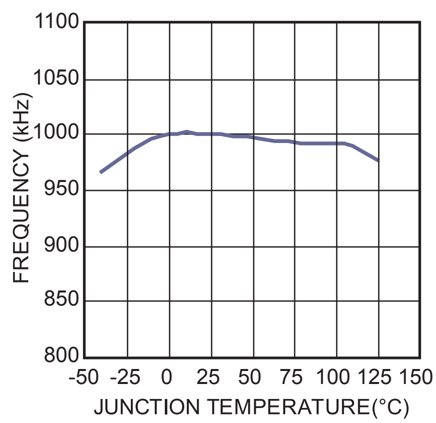
V_{IN}=4.2V



Reference Voltage vs. Junction Temperature

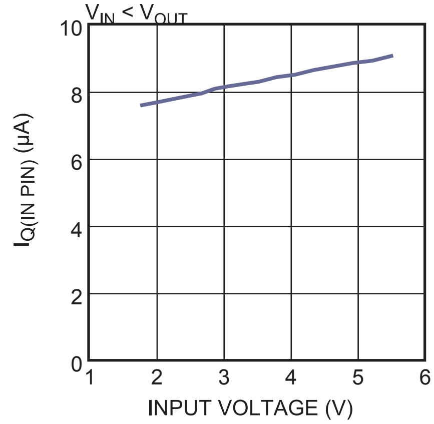


Frequency vs. Junction Temperature



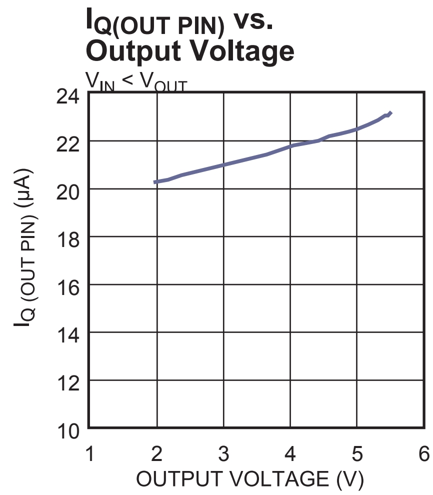
$I_{Q(IN\ PIN)}$ vs. Input Voltage

V_{IN} < V_{OUT}



Typical Performance Characteristics *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

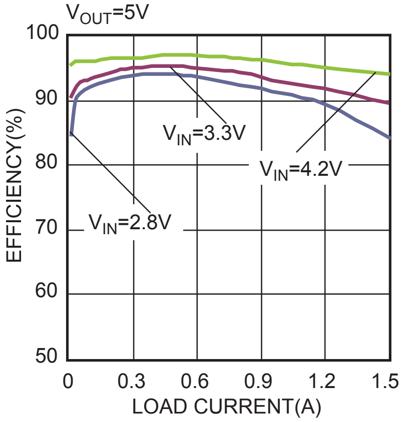


TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

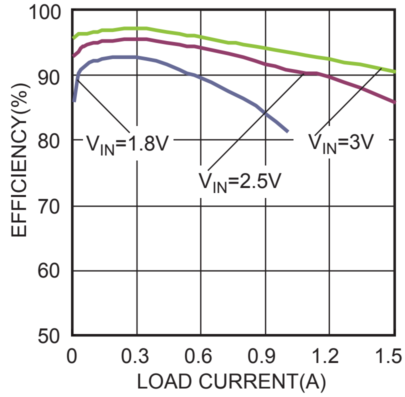
Efficiency vs. Load Current

V_{OUT}=5V



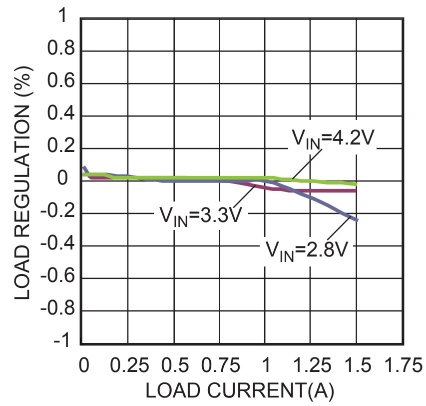
Efficiency vs. Load Current

V_{OUT}=3.3V



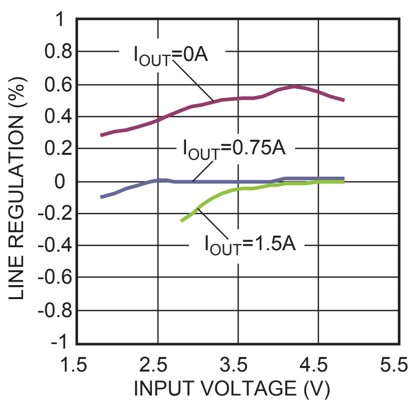
Load Regulation

V_{OUT}=5V



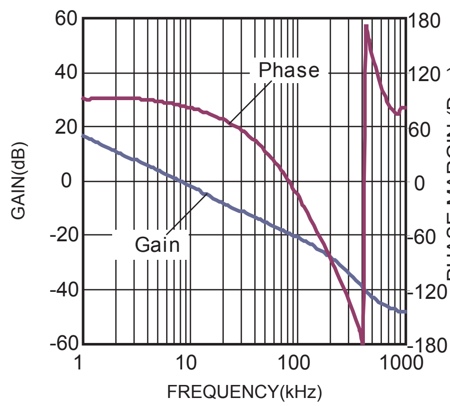
Line Regulation

V_{OUT}=5V



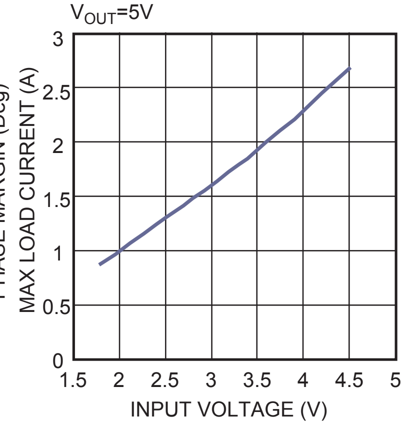
Bode Plot

V_{IN}=3.3V, V_{OUT}=5V, I_{OUT}=1.5A



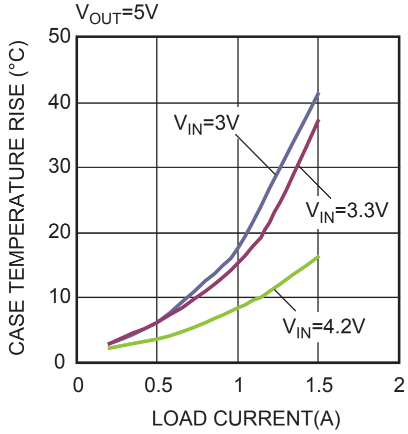
Load Capability vs. Input Voltage (7)

V_{OUT}=5V



Case Temperature Rise vs. Load Current

V_{OUT}=5V



NOTE:

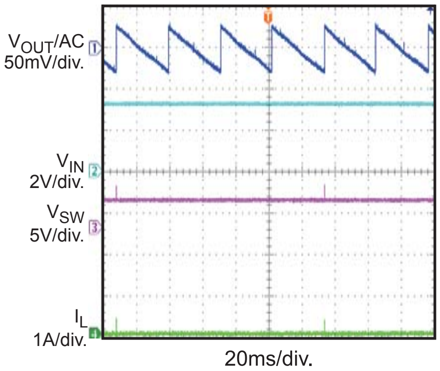
7) Tested with a 3.6A inductor peak current with the schematic shown in Figure 3. The maximum load current may decrease if the temperature rising is limited on the real application board.

TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

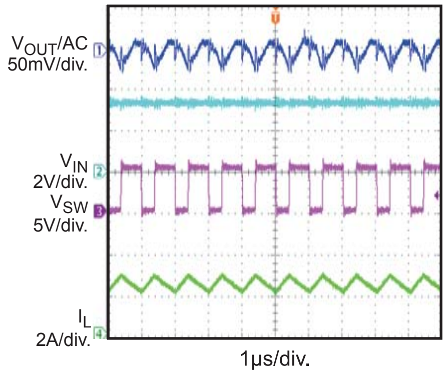
Steady State

I_{OUT} = 0A



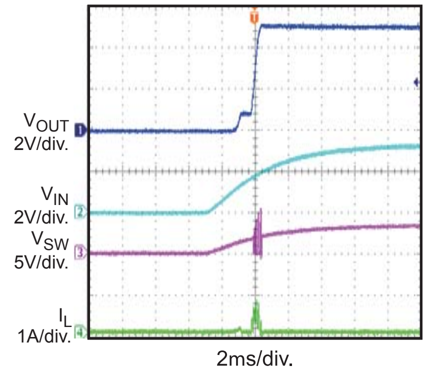
Steady State

I_{OUT} = 1.5A



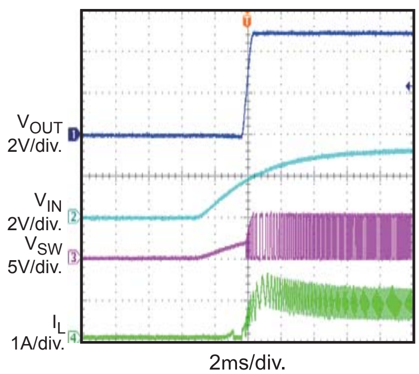
V_{IN} Start-Up

I_{OUT} = 0A



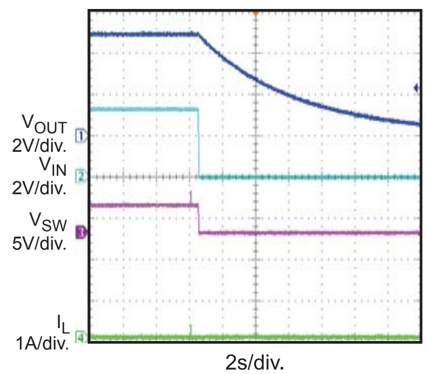
V_{IN} Start-Up

R_{LOAD} = 10Ω



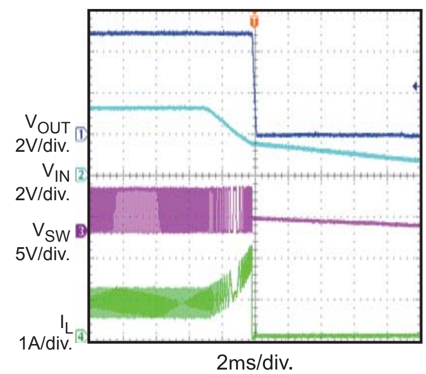
V_{IN} Shutdown

I_{OUT} = 0A



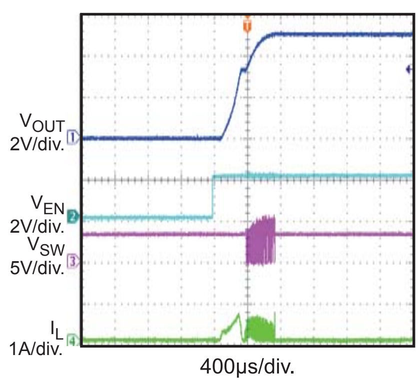
V_{IN} Shutdown

R_{LOAD} = 10Ω



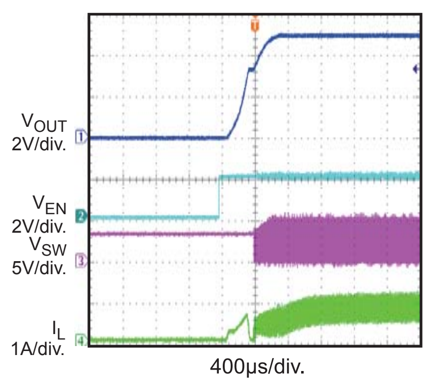
EN Start-Up

I_{OUT} = 0A



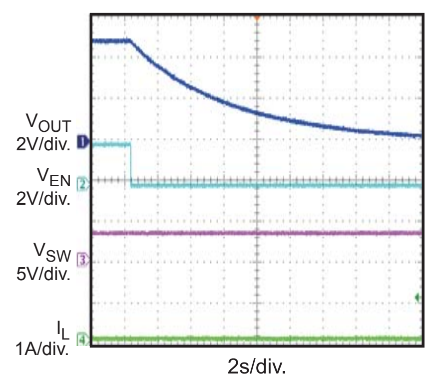
EN Start-Up

R_{LOAD} = 10Ω



EN Shutdown

I_{OUT} = 0A

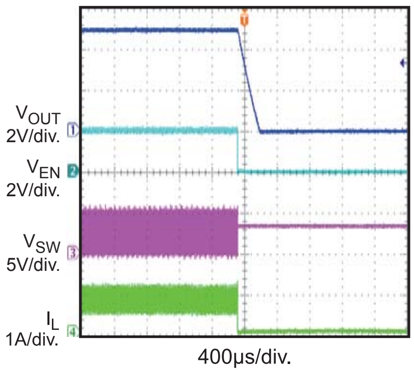


TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

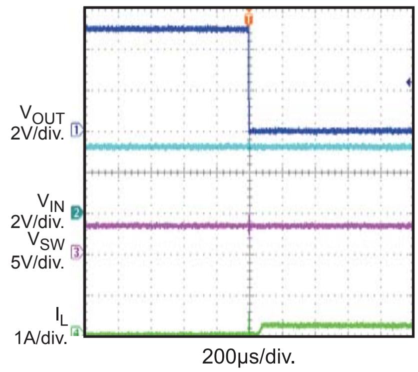
EN Shutdown

R_{LOAD} = 10Ω



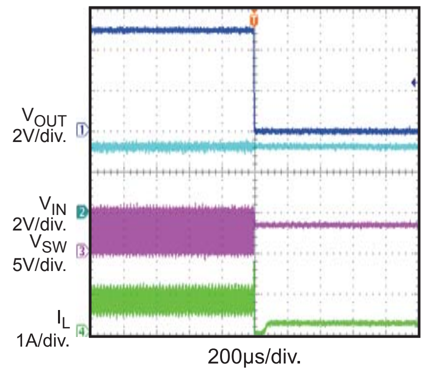
SCP Entry

I_{OUT} = 0A to Short



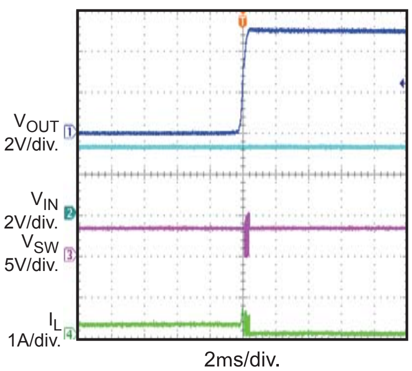
SCP Entry

R_{LOAD} = 10Ω to Short



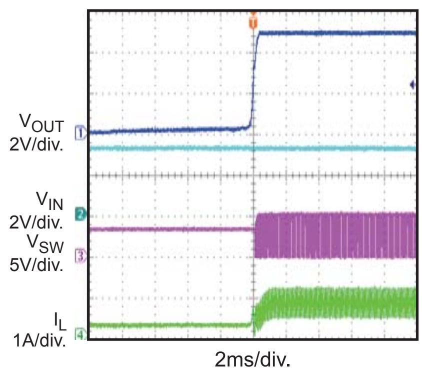
SCP Recovery

I_{OUT} = Short to 0A



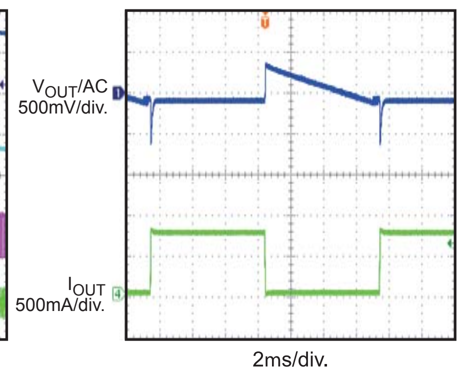
SCP Recovery

R_{LOAD} = Short to 10Ω



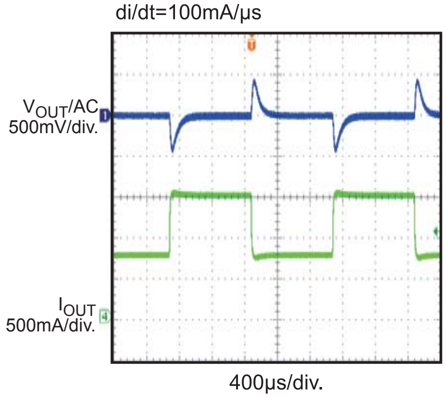
Load Transient

I_{OUT}= 0A to 0.75A
di/dt=100mA/µs



Load Transient

I_{OUT}= 0.75A to 1.5A
di/dt=100mA/µs



PIN FUNCTIONS

Pin #	Name	Description
1, 10	PGND	**Power Ground.**
2, 11	SW	**Power Switch Output.** SW is the connection node of the internal low-side MOSFET and synchronous MOSFET. Connect the power inductor between SW and the input power. Keep the PCB trace length as short and wide as possible to reduce EMI and voltage spikes.
3, 12	OUT	**Output.** OUT is the drain of the internal synchronous rectifier MOSFET. Bias power is derived from OUT once V_{OUT} exceeds V_{IN}. PCB trace length from OUT to the output filter capacitor(s) should be as short and wide as possible. The output disconnect feature allows OUT to be completely disconnected from IN when EN is low.
4	IN	**Power Supply Input.** The start-up bias is derived from IN and must be bypassed locally. The bias power is derived from OUT once V_{OUT} exceeds V_{IN}.
5	N/C	**No Connection.**
6	EN	**Chip Enable Control Input.** Set EN higher than 1.2V to turn on the regulator. Set EN lower than 0.4V to turn off the regulator.
7	FB	**Feedback.** Connect FB to the tap of an external resistive voltage divider from the output to set the output voltage.
8	AGND	**Analog Ground.**
9	TRIM	**Test Pin for Factory Use Only.** Connect TRIM to GND during application.

BLOCK DIAGRAM

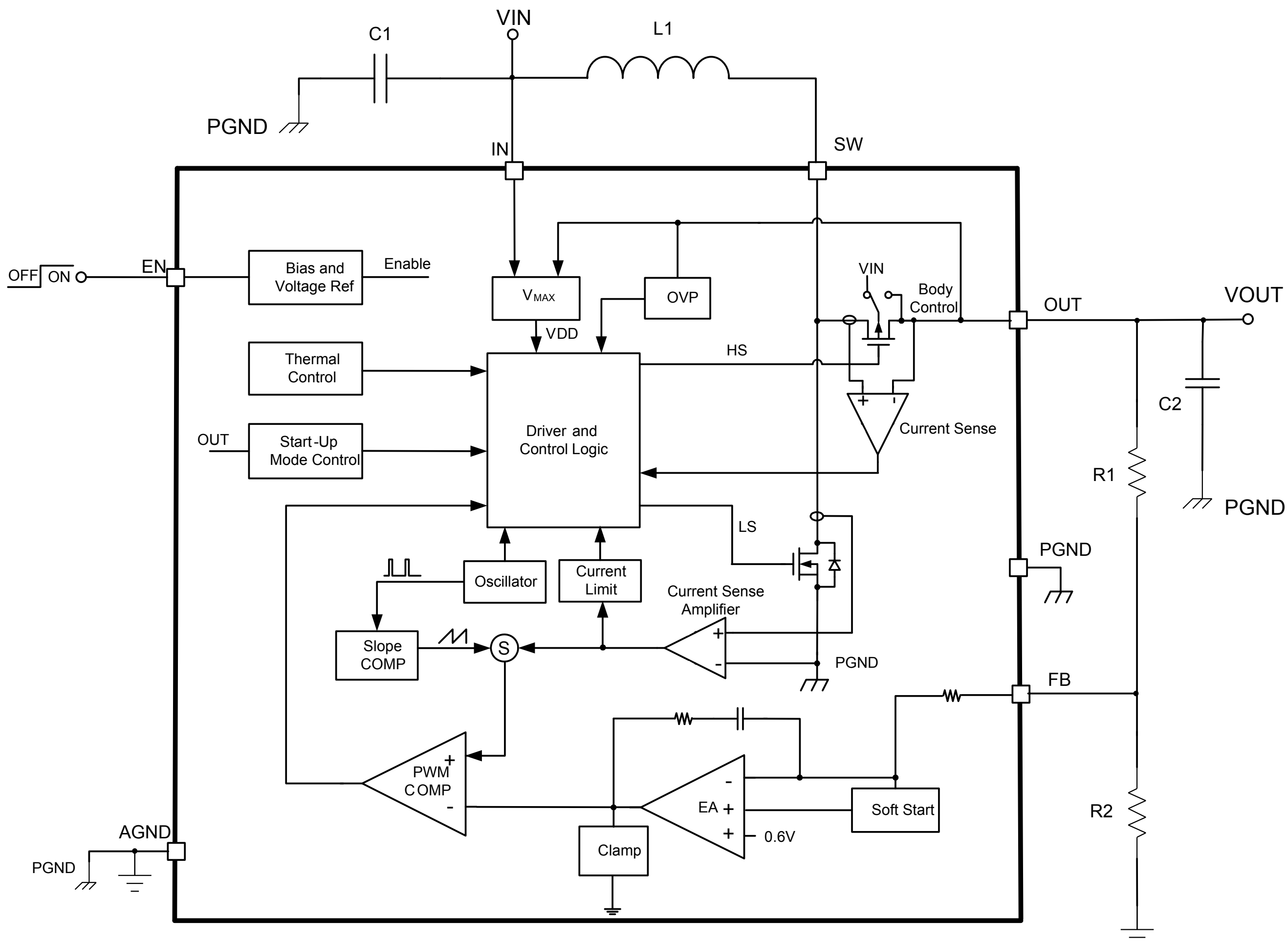


Figure 1: Functional Block Diagram

OPERATION

The MP3415 is a 1MHz, synchronous, step-up converter with true output disconnect. The device features a fixed-frequency, current-mode, PWM control for ideal line and load regulation. The internal soft start and loop compensation simplify the design process and minimize external components. The internal low-$R_{DS(ON)}$ MOSFETs combined with frequency stretching allow the MP3415 to achieve high efficiency over a wide load range.

Start-Up

When enabled, the MP3415 starts up in linear charge mode. During the linear charge, the rectified P-channel MOSFET (PMOS) turns on until the output voltage (V_{OUT}) is charged close to the input voltage (V_{IN}). To prevent inrush current, the PMOS current is limited to about 0.3A when V_{OUT} is 0V. The PMOS linear charge current limit is increased to about 0.8A while V_{OUT} rises to 3.3V (if V_{IN} is higher than 3.3V). This circuit helps to limit the output current under short-circuit conditions. Once the output voltage reaches $V_{IN,}$ the linear charging period elapses, and the device begins switching. V_{OUT} begins rising under internal soft-start (SS) control. In boost switching condition, the current limit is 4.2A, typically.

When V_{OUT} is higher than V_{IN}, the MP3415 powers its internal circuits from V_{OUT} instead of V_{IN}. This allows for strong driving capability and high efficiency, even if V_{IN} drops to as low as 1.8V.

Soft Start (SS)

The MP3415 provides a soft start (SS) by charging an internal capacitor with a current source. During the linear charge period, the SS signal continues rising, following FB. Once the linear charge elapses, the voltage on the SS capacitor is charged and ramps up to the reference voltage based on the internal fixed slew rate. The SS capacitor is discharged completely during a forced shutdown, thermal shutdown, or output short circuit.

Device Enable (EN)

The device begins operating if EN is higher than 1.2V and enters shutdown mode if EN is lower than 0.4V. In shutdown mode, all internal control circuits switch off, and the output disconnects from the input completely.

Power-Save Mode (PSM)

The MP3415 enters power-save mode (PSM) automatically when the load decreases and switches back to PWM mode when the load increases. In PSM, the converter stretches the frequency down to reduce switching and driver loss. The switch frequency is also stretched down when the input voltage is close to the output voltage, which triggers the minimum on time if kept at a 1MHz frequency. This helps decrease the output ripple by avoiding group pulse mode. Under very light-load conditions, the MP3415 runs in group-pulse mode to regulate the output voltage and save more power.

Error Amplifier (EA)

The error amplifier (EA) is an internally compensated amplifier. The EA compares the internal 0.6V reference voltage against V_{FB} to generate an EA signal, which controls V_{OUT}. The output voltage of the MP3415 is adjusted via FB by an external resistor divider and can be calculated with Equation (1):

$$V_{OUT} = 0.6V \times (1 + \frac{R1}{R2}) \tag{1}$$

Setting a high value for R1 and R2 can achieve a low quiescent current. However, a resistance that is too high is sensitive to noise and leads to a low loop bandwidth. Set the R1 value between 499kΩ and 1MΩ for good leakage, stability, and transient balance.

Current Sensing

In a linear charge condition, the high-side, P-channel MOSFET current is sensed and compared with the current limit threshold. The compared output manages the linear charge current.

In boost switching condition, lossless current sensing converts the N-channel MOSFET switch current signal to a voltage that is summed with the internal slope compensation. The summed signal is compared with the EA output to provide a peak-current control command for PWM. The peak switch current is limited to approximately 4.2A. The switch-current signal is blanked internally for 60ns to enhance noise immunity.

Output Disconnect

The MP3415 is designed to allow for true output disconnect by eliminating body diode conduction of the internal P-channel MOSFET rectifier. This allows V_{OUT} to reach 0V during shutdown, drawing zero current from the input source. This also allows for inrush current limiting at start-up, which minimizes the surge current seen by the input supply. To obtain the advantages of the output disconnect, there *cannot* be an external Schottky diode connected between SW and VOUT.

Overload (OLP) and Short-Circuit (SCP) Protections

When an overload or a short circuit occurs, the output voltage drops. If V_{OUT} drops below V_{IN} - 0.3V, the MP3415 stops for about 50μs and then runs in a linear charge mode. If the overload or short circuit is removed, the MP3415 restarts under SS control automatically.

Over-Voltage Protection (OVP)

If V_{OUT} is higher than the typical 6V threshold, the boost switching stops. After the output drops to about 5.7V, the switching recovers automatically. This protects the internal power MOSFET from over-voltage stress.

Thermal Shutdown (TSD)

The device has an internal temperature monitor. If the die temperature exceeds 155°C, the converter turns off. Once the temperature drops below 130°C, the converter restarts.

APPLICATION INFORMATION

Selecting the Input Capacitor

Low equivalent series resistance (ESR) input capacitors reduce input switching noise and peak current drawn from the input power. Ceramic capacitors are recommended for input decoupling and should be placed as close to the device as possible. Use a ceramic capacitor larger than 10µF to limit the V_{IN} ripple.

Output Capacitor Selection

To ensure stability over the full operating range, the output capacitor requires a minimum capacitance value of 22µF at the programmed output voltage. A higher capacitance value may be required to lower the output and transient ripple. X5R or X7R capacitors are recommended for their low ESR values. Supposing the ESR is zero, calculate the minimum output capacitor value needed to support the ripple in PWM mode with Equation (2):

$$C_O \geq \frac{I_O \times (V_{OUT(MAX)} - V_{IN(MIN)})}{f_S \times V_{OUT(MAX)} \times \Delta V} \quad (2)$$

Where $V_{OUT(MAX)}$ is the maximum output voltage, $V_{IN(MIN)}$ is the minimum input voltage, I_O is the output current, f_S is the switching frequency, and ΔV is the acceptable output ripple.

A 1µF ceramic capacitor is recommended to be placed between V_{OUT} and PGND with a short loop to reduce spikes on the SW node and improve EMI performance.

Selecting the Inductor

The MP3415 utilizes small, surface-mounted chip inductors for their 1MHz switching frequencies. Inductor values between 1µH and 2.2µH are suitable for most applications. Inductors with larger values allow for slightly greater output current capabilities by reducing the inductor ripple current. However, a larger inductance value increases component size. The minimum inductance value can be calculated with Equation (3):

$$L \geq \frac{V_{IN(MIN)} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{V_{OUT(MAX)} \times \Delta I_L \times f_S} \quad (3)$$

Where ΔI_L is the acceptable inductor current ripple.

Typically, the inductor current ripple is set to 30% to 50% of the maximum inductor current. Maintain a low series resistance of the inductor (DCR) to reduce resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

SW RC Snubber

When the MP3415 is used to generate an output of 4V or higher, an RC snubber should be added to protect the internal MOSFET from over-voltage caused by the SW spike. The recommended RC snubber parameters are 1Ω and 1nF (see Figure 3).

PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. Poor layout can result in reduced performance, excessive EMI, resistive loss, system instability, and even over-voltage stress. For best results, refer to Figure 2 and follow the guidelines below:

1. Place the output capacitor as close to OUT as possible with minimal distance to PGND.
2. Place a small decoupling capacitor in parallel with the bulk output capacitor and with smaller loop than bulk output capacitor. This is very important for reducing spikes on SW and improving EMI performance.
3. Place the input capacitor and inductor as close to IN and SW as possible.
4. Keep the trace between the inductor and SW as wide and short as possible.
5. Keep the feedback loop far away from all noise sources, such as SW.
6. Place the feedback divider resistors as close to FB and AGND as possible.
7. Tie the ground return of the input/output capacitors as close to PGND as possible.
8. Use a large copper GND area. Vias around GND are recommended to lower the die temperature.
9. Add an RC snubber circuit from SW to PGND to reduce the SW spike when the output is higher than 4V.

See Figure 2 for layout recommendations.

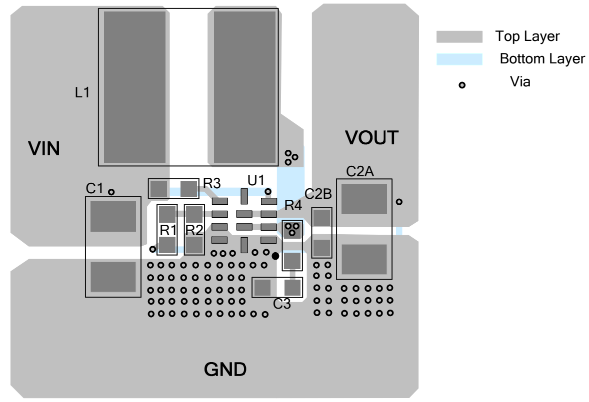


Figure 2: Layout Recommendation

Design Example

Table 1 shows a design example following the application guidelines for the following specifications:

Table 1: Design Example

V_{IN}	2.8V - 4.5V
V_{OUT}	5V
I_{OUT}	0A - 1.5A

The typical application circuit in Figure 3 is for 5V V_{OUT}. It shows the detailed application schematic and the basis for the typical performance waveforms. For additional detailed device applications, please refer to the related evaluation board datasheet (EVB).

TYPICAL APPLICATION CIRCUITS

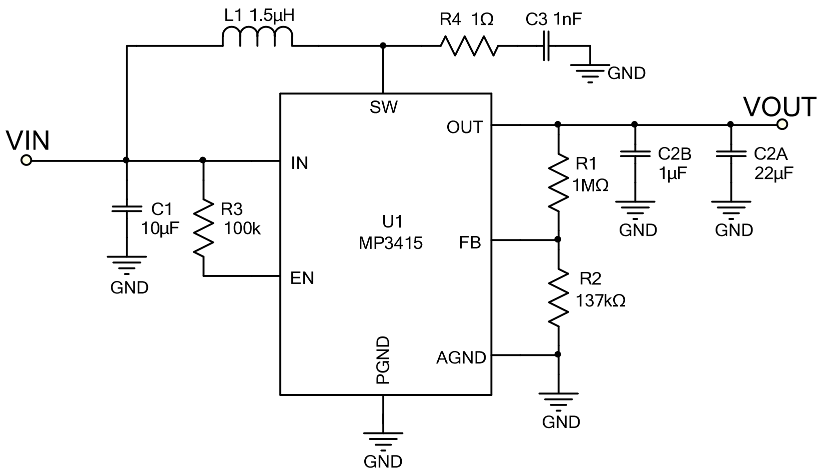


Figure 3: Typical Boost Application Circuit, V_{IN} = 2.8V to 4.5 V, V_{OUT} = 5V, I_{OUT} = 0A - 1.5A

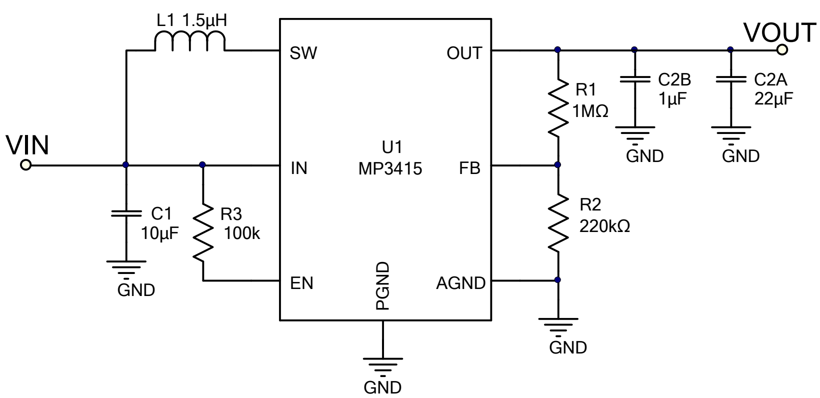
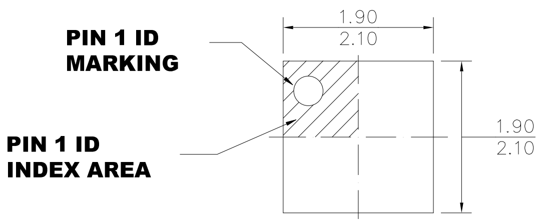


Figure 4: Typical Boost Application Circuit, V_{IN} = 1.8V to 3V, V_{OUT} = 3.3V, I_{OUT} = 0A - 1.5A[(8)]

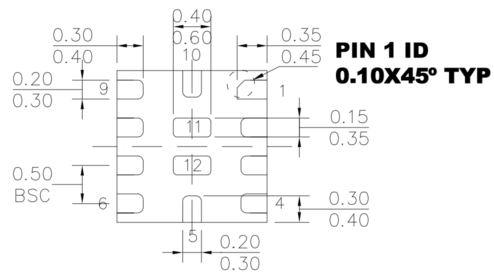
8) Tested with a 3.6A inductor peak current with the schematic shown in Figure 4. The maximum load current may decrease if VIN drops to lower than 2.1V.

PACKAGE INFORMATION

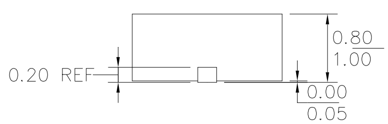
QFN-12 (2MMX2MM)



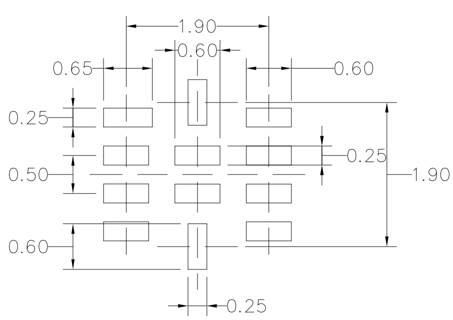
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.