MP3326A

16-Channel, 80mA/Channel, LED Driver with Separate PWM/Analog Dimming and Digital Interface

DSESCRIPTION

The MP3326A is a 16-channel LED driver that can operate from a wide 4.5V to 16V input voltage (V_{IN}) range. The MP3326A applies 16 internal current sources in each LED string terminal. The LED current (I_{LED}) of each channel is set by an external current-setting resistor. The maximum current for each channel is 80mA.

The MP3326A integrates a digital interface with up to 10 configurable digital interface addresses via an external resistor. This means that the MP3326A can support up to 10 cascaded ICs to drive the LED array. Each channel can be enabled or disabled via the digital interface.

The MP3326A employs both separate pulse-width modulation (PWM) dimming and analog dimming for each LED channel, as well as 12-bit PWM dimming and 6-bit analog dimming for each channel. The I_{LED} ramp rate and phase shift can be configured to reduce EMI.

The MP3326A can output a refresh signal from the RFSH/FLT pin, where the refresh signal frequency ($f_{REFRESH}$) can be set via the digital interface.

Full protection features include LED open protection, LED short protection, and over-temperature protection (OTP). The device also features a fault indicator. If a protection is triggered, then the RFSH/FLT pin is pulled low and the corresponding fault register is set.

The MP3326A is available in a QFN-24 (4mmx4mm) package.

FEATURES

- Wide 4.5V to 16V Input Voltage (V_{IN}) Range
- 16 Channels, Max 80mA/Channel
- LED Current (I_{LED}) Configured via an External Resistor
- 6-Bit Analog Dimming for Each Channel
- 12-Bit Pulse-Width Modulation (PWM) Dimming for Each Channel
- Selectable 220Hz, 250Hz, 280Hz, or 330Hz PWM Dimming Frequency (f_{PWM})
- Refresh Signal Output
- Digital Interface
- 10 Addresses Configurable via an External Resistor
- Configurable I_{LED} Slew Rate
- 40μs Phase Shift
- Fault Indicator
- LED Open Protection
- LED Short Protection with Configurable Threshold
- Under-Voltage Lockout (UVLO) Protection
- Over-Temperature Protection (OTP)
- Available in a QFN-24 (4mmx4mm) Package
- Available in a Wettable Flank Package

APPLICATIONS

- RGB Drivers
- LED Indicators
- Instruments Clusters
- General Displays
- LED Backlighting

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TYPICAL APPLICATION

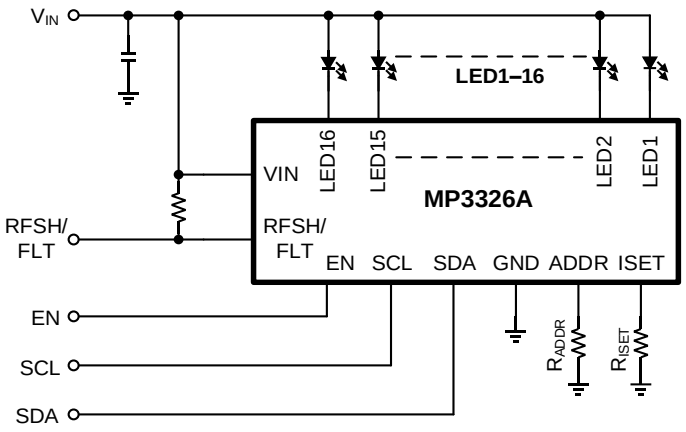

Figure 1: Typical Application Circuit

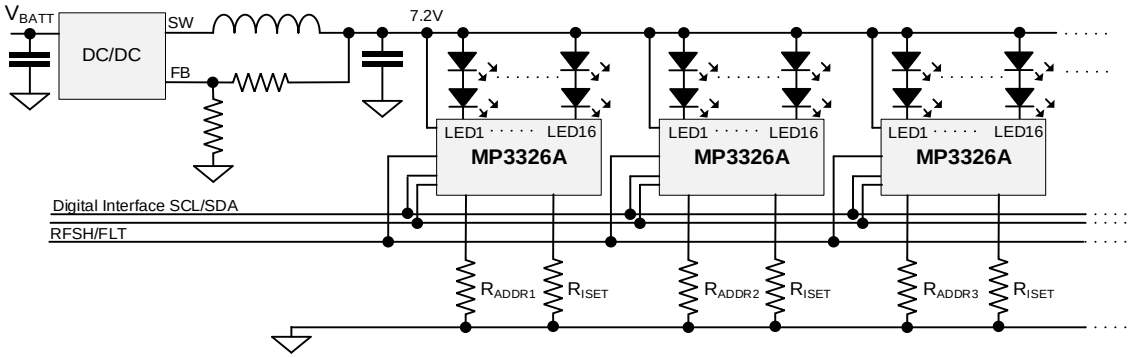

Figure 2: System Application Circuit with 2 LEDs in Series

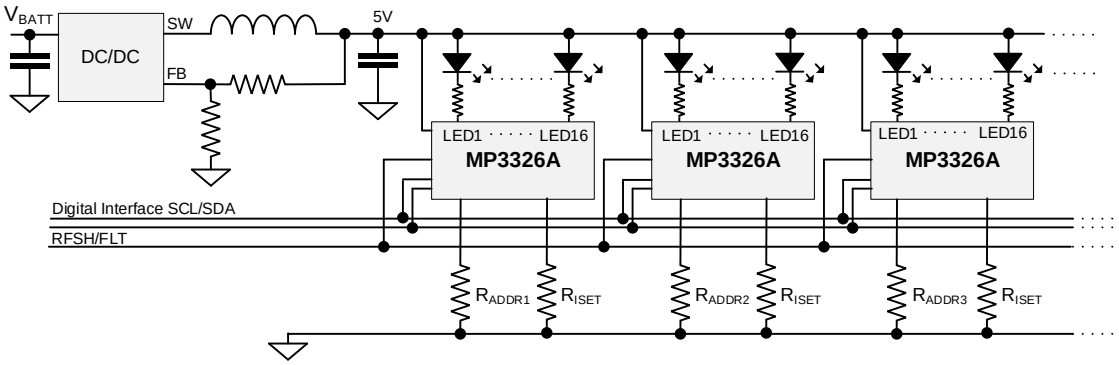

Figure 3: System Application Circuit with 1 LED and 1 Resistor in Series

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Level**
MP3326AGRE***	QFN-24 (4mmx4mm)	*See Below*	1

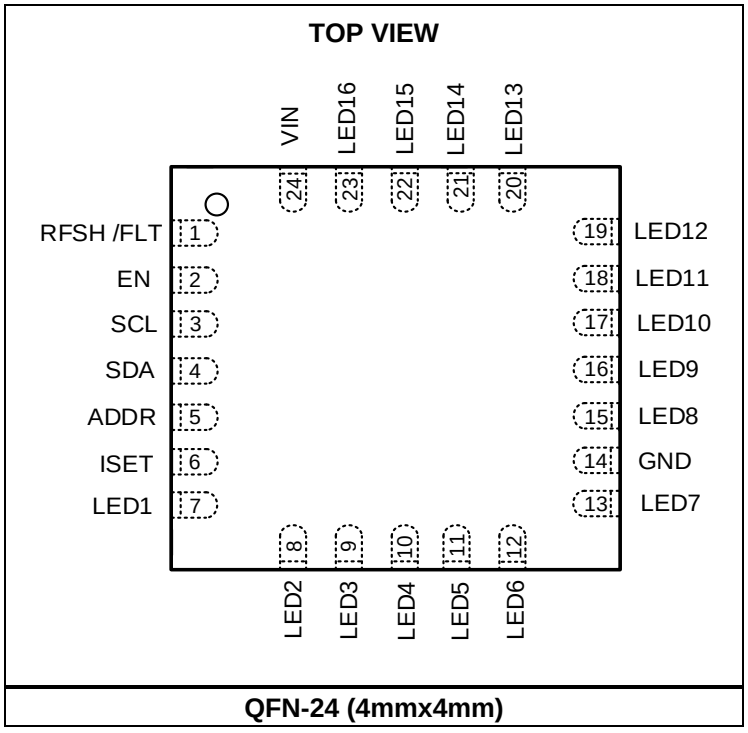
* For Tape & Reel, add suffix -Z (e.g. MP3326AGRE-Z).
** Moisture Sensitivity Level Rating
*** Wettable Flank

TOP MARKING

MPSYWW
M3326A
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M3326A: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	RFSH/FLT	**Refresh signal output or fault flag.** If the FLTEN bit = 0, then the RFSH/FLT pin outputs a synchronized signal that is set by the FRFSH[9:0] register. If FLTEN = 1, then RFSH/FLT indicates whether a fault occurs, in which case it is pulled low.
2	EN	**Enable control.** Pull the EN pin high to turn the LED driver on; pull EN low to turn it off.
3	SCL	**Digital interface clock input.**
4	SDA	**Digital interface data input.**
5	ADDR	**Digital interface address setting.** Configure the digital interface addresses by connecting different resistors from ADDR to GND. ADDR can set the 4 least significant bits (LSB) of the digital interface address. There are 10 configurable addresses.
6	ISET	**LED current setting.** Connect a current-setting resistor from ISET to GND to configure the current in each LED string.
7	LED1	**LED channel 1 current input.** Connect the LED channel 1 cathode to this pin.
8	LED2	**LED channel 2 current input.** Connect the LED channel 2 cathode to this pin.
9	LED3	**LED channel 3 current input.** Connect the LED channel 3 cathode to this pin.
10	LED4	**LED channel 4 current input.** Connect the LED channel 4 cathode to this pin.
11	LED5	**LED channel 5 current input.** Connect the LED channel 5 cathode to this pin.
12	LED6	**LED channel 6 current input.** Connect the LED channel 6 cathode to this pin.
13	LED7	**LED channel 7 current input.** Connect the LED channel 7 cathode to this pin.
14	GND	**Ground.**
15	LED8	**LED channel 8 current input.** Connect the LED channel 8 cathode to this pin.
16	LED9	**LED channel 9 current input.** Connect the LED channel 9 cathode to this pin.
17	LED10	**LED channel 10 current input.** Connect the LED channel 10 cathode to this pin.
18	LED11	**LED channel 11 current input.** Connect the LED channel 11 cathode to this pin.
19	LED12	**LED channel 12 current input.** Connect the LED channel 12 cathode to this pin.
20	LED13	**LED channel 13 current input.** Connect the LED channel 13 cathode to this pin.
21	LED14	**LED channel 14 current input.** Connect the LED channel 14 cathode to this pin.
22	LED15	**LED channel 15 current input.** Connect the LED channel 15 cathode to this pin.
23	LED16	**LED channel 16 current input.** Connect the LED channel 16 cathode to this pin.
24	VIN	**Power supply input.** The VIN pin supplies power to the IC. Connect a capacitor between VIN and GND.

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ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +22V
V_{LED1} to V_{LED16} .....-0.5V to +22V
All other pins .....-0.3V to +5V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (4mmx4mm)..... 2.97W

ESD Ratings

Human body model (HBM)…… ±1.5kV
Charged-device model (CDM).....±2kV

Recommended Operating Conditions

Input voltage (V_{IN}) .....4.5V to 16V
Operating junction temp (T_J) (3)……
..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-24 (4mmx4mm)			
JESD51-7 (4)	42	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Operating devices at a junction temperature up to 150°C is possible. Contact MPS for details.
4) Measured on a JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value indicates the thermal resistance from the junction-to-case bottom.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 5V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
Input voltage (V_{IN}) range	V_{IN}		4.5		16	V
Quiescent supply current	I_Q				5	mA
Shutdown supply current	I_{ST}	V_{EN} = 0V, V_{IN} = 16V			2	μA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$	Rising edge	3.6	3.8	4.2	V
V_{IN} UVLO falling threshold	$V_{IN_UVLO_FALLING}$	Falling edge	3.3	3.5	3.7	V
Enable (EN)						
EN rising threshold	V_{EN_RISING}	V_{EN} rising	2.1			V
EN falling threshold	$V_{EN_FALLING}$	V_{EN} falling			0.8	V
EN pull-down resistance	R_{EN}			1		MΩ
RFSH/FLT						
Refresh signal frequency	$f_{REFRESH}$	FRFSH[9:0] = 0x1A9, FPWM[1:0] = 01	285	300	315	Hz
RFSH/FLT pull-down resistance	$R_{RFSH/FLT}$	FLTEN = 1, fault is triggered			100	Ω
LED Regulator						
ISET voltage	V_{ISET}		1.176	1.2	1.224	V
LED current	I_{LED}	R_{ISET} = 24kΩ, ICHx[5:0] = 0x3F	-3%	50	+3%	mA
		R_{ISET} = 15kΩ, ICHx[5:0] = 0x3F	-3%	80	+3%	mA
Current sink headroom	V_{LEDx}	I_{LED} = 50mA		200	300	mV
		I_{LED} = 80mA		350	400	mV
Dimming						
Pulse-width modulation (PWM) frequency	f_{PWM}	FPWM[1:0] = 01	240	250	260	Hz
PWM duty step	t_{PWM}	12-bit resolution, f_{PWM} = 250Hz		1		μs
Phase shift	t_{DELAY}	PS_EN = 1		40		μs
LED current step		I_{LED} = 80mA, analog dimming step		1.25		mA
LED current slew rate in PWM dimming		SLEW[1:0] = 01, rising edge		5		μs
		SLEW[1:0] = 11, rising edge		20		μs
Protection						
LED short string protection threshold	V_{SLP}	STH[1:0] = 01	2.85	3	3.15	V
LED short string protection time	t_{SLP}	V_{LEDx} > STH[1:0]		4		ms
LED short string protection hiccup time	t_{SLP_HICCUP}			1		ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 5V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED short string protection hiccup detection time	t_{SLP_DET}			32		µs
LED open string protection threshold	V_{OLP}			100	150	mV
LED open string protection time	t_{OLP}	V_{LEDx} < 100mV		4		ms
LED open string protection hiccup time	t_{OLP_HICCUP}			1		ms
LED open string protection hiccup detection time	t_{OLP_DET}			32		µs
Thermal shutdown threshold (5)	T_{SD}			170		°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}			20		°C
Digital Interface						
Logic-low input voltage	V_{IN_LOW}		0		0.4	V
Logic-high input voltage	V_{IN_HIGH}		1.3			V
Logic-low output voltage (5)	V_{OUT_LOW}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency (5)	f_{SCL}		10		1000	kHz
Bus free time (5)	t_{BUF_FREE}	Between a stop and start condition	0.5			µs
Hold time after a start or repeated start command (5)	t_{HOLD_START}	After this period, the first clock is generated	0.26			µs
Repeated start command set-up time (5)	t_{SU_START}		0.26			µs
Stop command set-up time (5)	t_{SU_STOP}		0.26			µs
Data hold time (5)	t_{HOLD_DATA}		0			ns
Data set-up time (5)	t_{SU_DATA}		50			ns
Clock low timeout (5)	$t_{TIMEOUT}$		25		35	ms
Clock low time (5)	t_{LOW}		0.5			µs
Clock high time (5)	t_{HIGH}		0.26			µs
Clock/data falling time (5)	$t_{FALLING}$				120	ns
Clock/data rising time (5)	t_{RISING}				120	ns

Note:

5) Guaranteed by characterization. Not tested in production.

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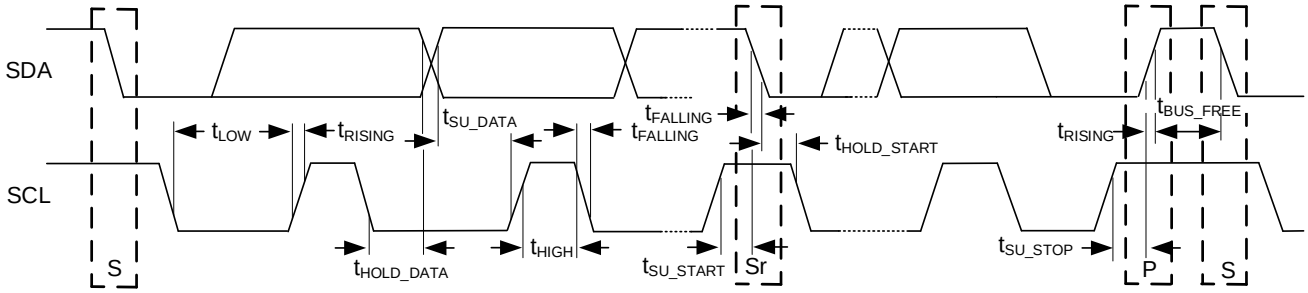
DIGITAL INTERFACE TIMING DIAGRAM



S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

Figure 4: Digital Interface Timing Diagram

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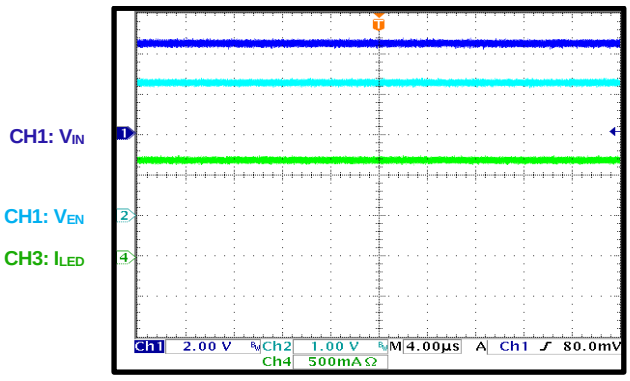
TYPICAL PERFORMANCE CHARACTERISTICS

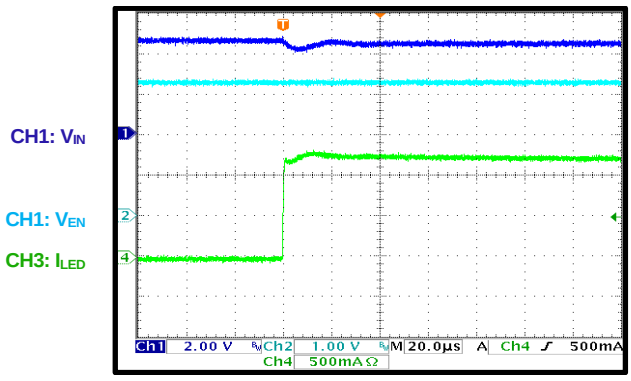
V_{IN} = 4.5V, I_{LED} = 80mA per string, LED = 16P1S, T_A = 25°C, unless otherwise noted.

Steady State

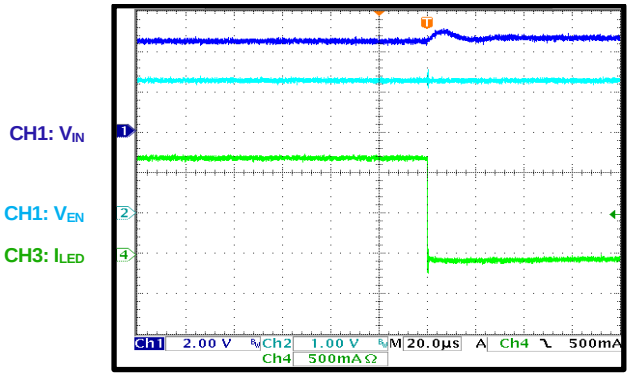
V_{IN} = 4.5V, 16P1S, 80mA/string



Start-Up via the EN Bit

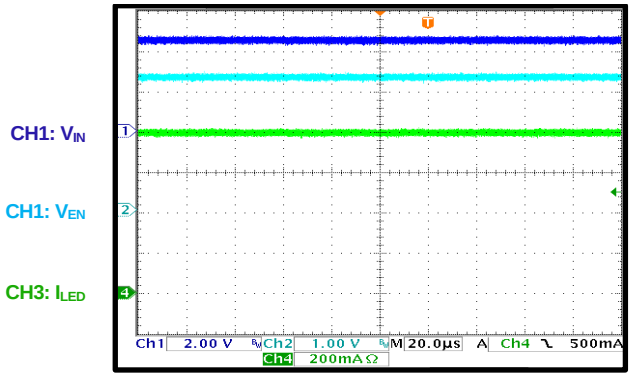


Shutdown via the EN Bit



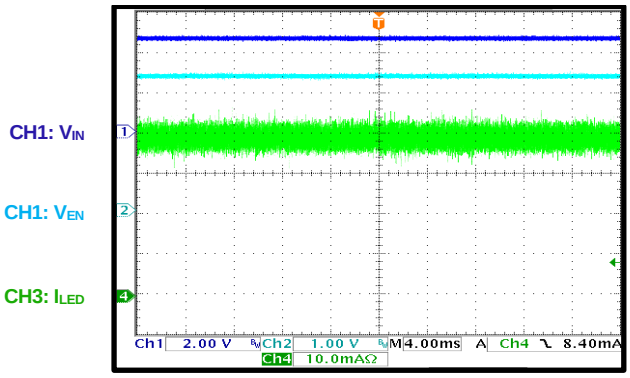
Analog Dimming

50mA/string



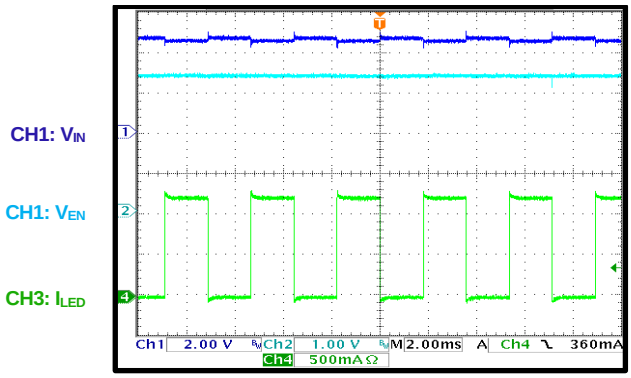
Analog Dimming

2.5mA/string



PWM Dimming

PWM duty = 50%



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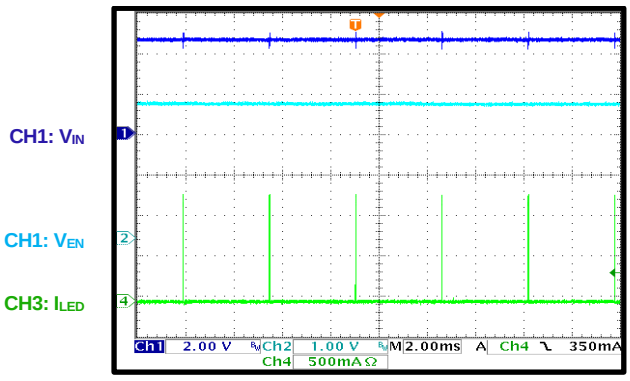
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 4.5V, I_{LED} = 80mA per string, LED = 16P1S, T_A = 25°C, unless otherwise noted.

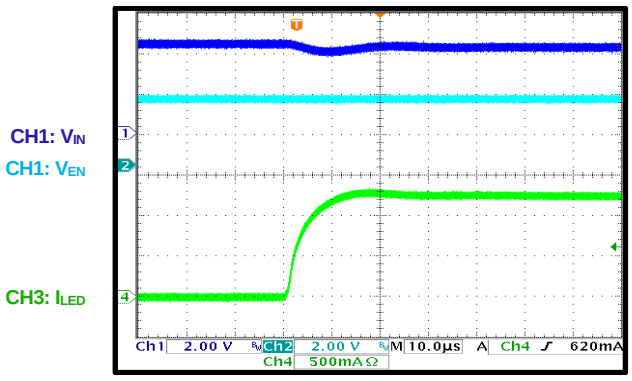
PWM Dimming

PWM duty = 0.5%



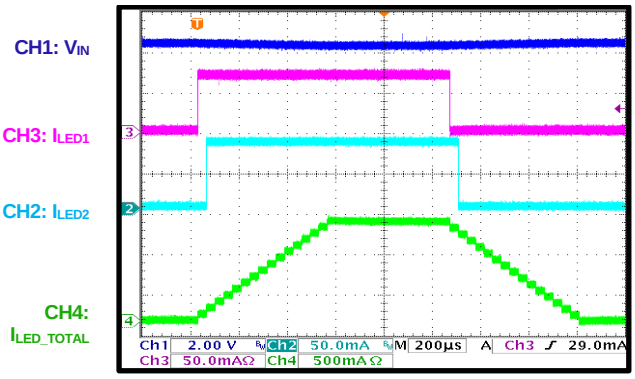
Slew Rate

PWM dimming slew rate = 5µs



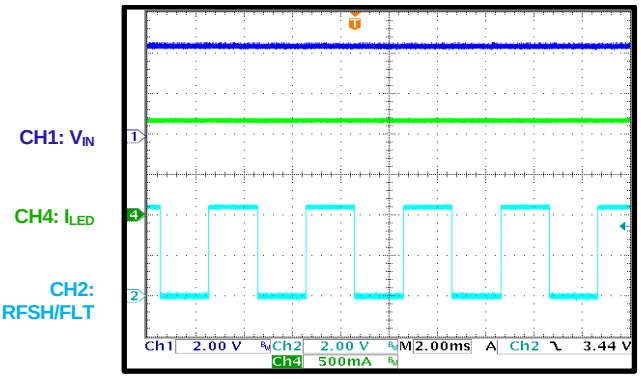
Phase Shift

PWM dimming duty = 20%



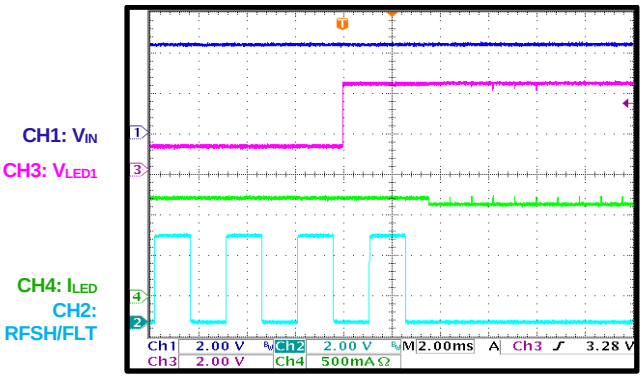
Refresh Function

f_{PWM} = 250Hz, RFRSH[9:0] = 0x1FF



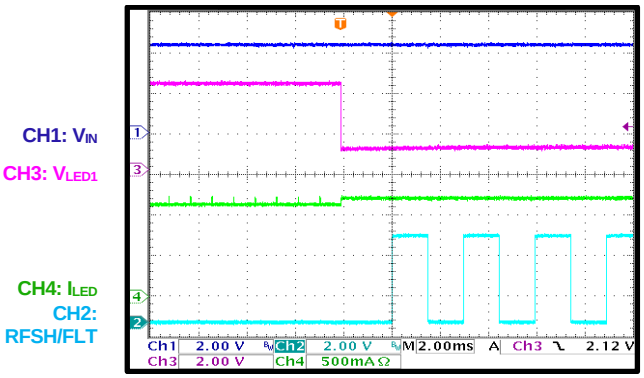
LEDx Short Entry

RFSH/FLT fault enabled, f_{PWM} = 330Hz, RFRSH[9:0] = 0x1FF



LEDx Short Recovery

RFSH/FLT fault enabled, f_{PWM} = 330Hz, RFRSH[9:0] = 0x1FF



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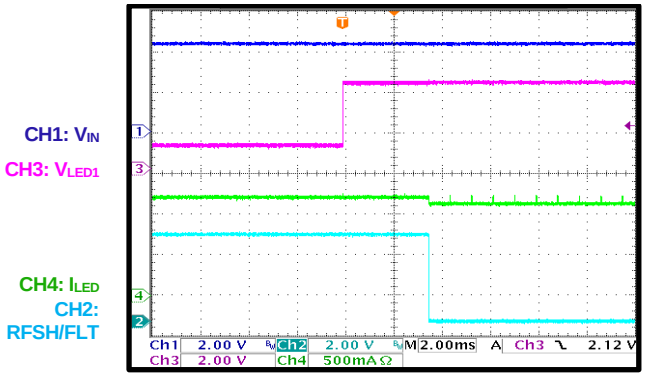
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 4.5V, I_{LED} = 80mA per string, LED = 16P1S, T_A = 25°C, unless otherwise noted.

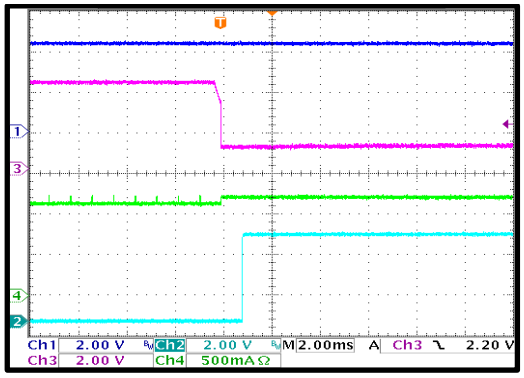
LEDx Short Entry

RFSH/FLT fault enabled, f_{PWM} = 250Hz, RFRSH[9:0] = 0x000



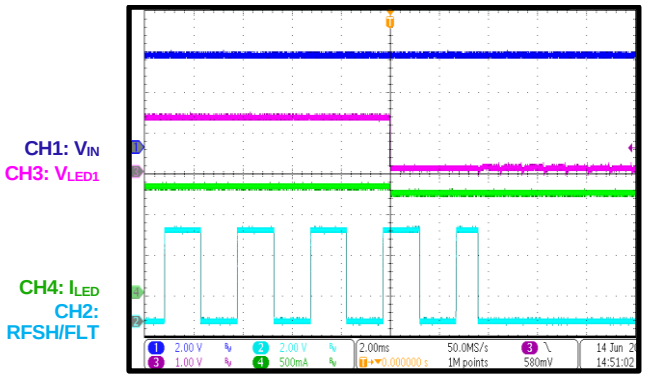
LEDx Short Recovery

RFSH/FLT fault enabled, f_{PWM} = 250Hz, RFRSH[9:0] = 0x000



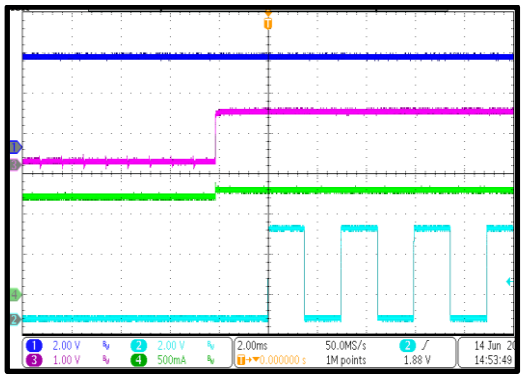
LEDx Open Entry

RFSH/FLT fault enabled, f_{PWM} = 330Hz, RFRSH[9:0] = 0x1FF



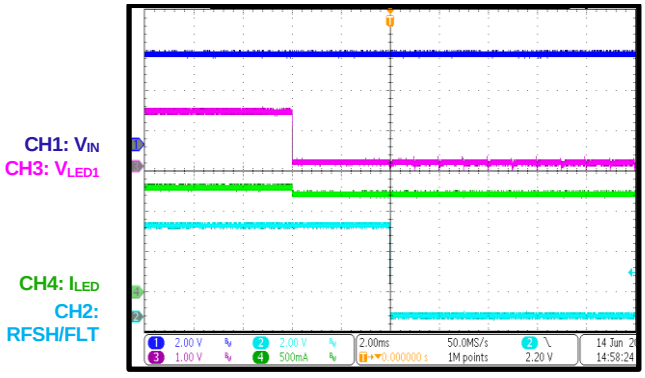
LEDx Open Recovery

RFSH/FLT fault enabled, f_{PWM} = 330Hz, RFRSH[9:0] = 0x1FF



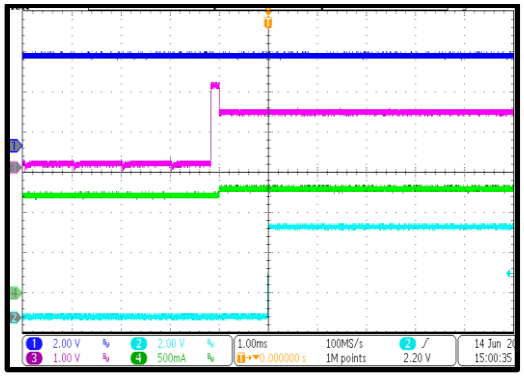
LEDx Open Entry

RFSH/FLT fault enabled, f_{PWM} = 250Hz, RFRSH[9:0] = 0x000



LEDx Open Recovery

RFSH/FLT fault enabled, f_{PWM} = 250Hz, RFRSH[9:0] = 0x000



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FUNCTIONAL BLOCK DIAGRAM

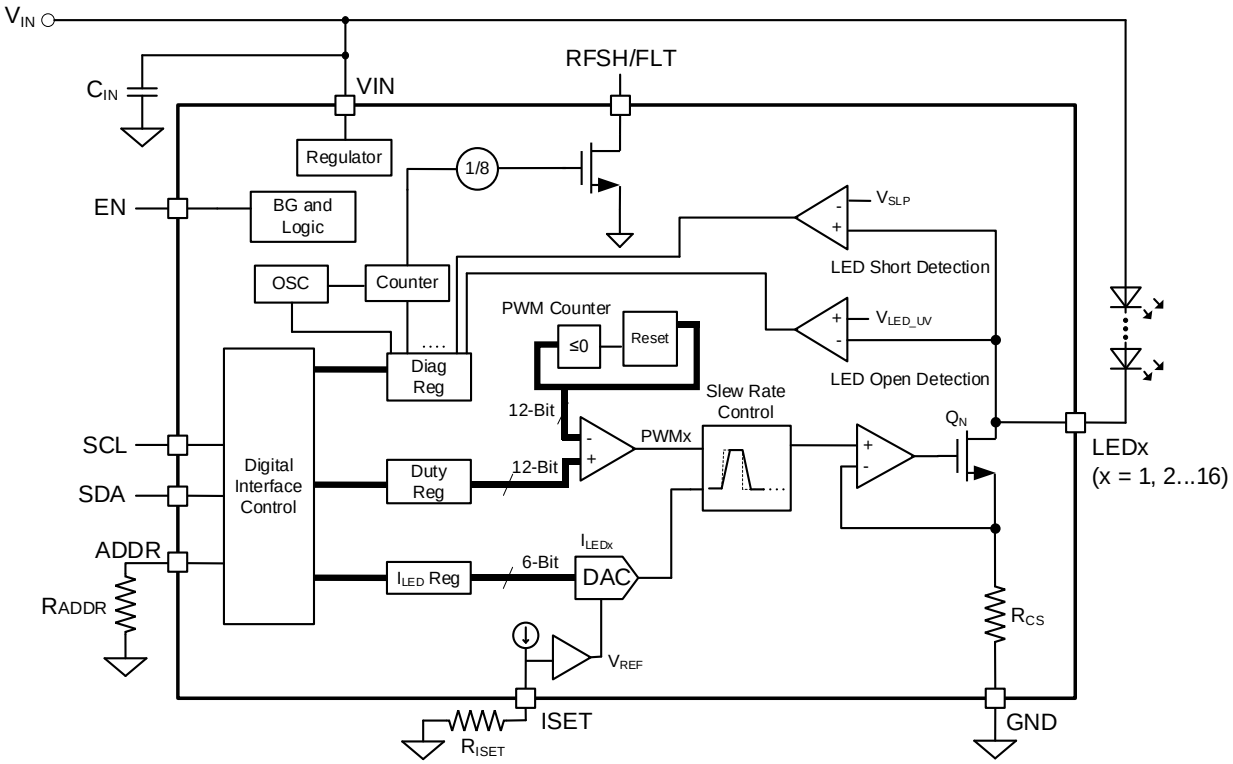

Figure 5: Functional Block Diagram

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OPERATION

The MP3326A applies 16 internal current sources in each LED string terminal. The LED current (I_{LED}) of all channels is set via an external current-setting resistor, with a maximum current up to 80mA per channel.

Enable (EN) and Start-Up

Once the input voltage (V_{IN}) exceeds its under-voltage lockout (UVLO) rising threshold ($V_{IN_UVLO_RISING}$) and the EN pin's voltage (V_{EN}) exceeds its rising threshold (V_{EN_RISING}), the MP3326A enters standby mode and the digital interface is active. After setting the digital interface register, set the EN bit high to start up the system. The start-up sequence is as follows:

1. V_{IN}
2. V_{EN}
3. Digital interface setting
4. Set the EN bit

Channel Selection

The channels can be disabled by pulling the corresponding CHxEN bit (where x = 1, 2…16) low.

Dimming

Each channel includes a separate 6-bit analog dimming register and 12-bit pulse-width modulation (PWM) dimming register. The MP3326A can support analog dimming and PWM dimming for each channel.

In analog dimming, the I_{LED} amplitude changes when the analog dimming register changes. Change the code in the ICHx register to apply analog dimming for the corresponding channel. I_{LED} can be estimated with Equation (1):

$$I_{LED} = \frac{ICHx}{63} \times I_{SET} \quad (1)$$

Where ICHx is the analog dimming code for channel x (where x = 1, 2…16).

If ICHx is set to 0, then the corresponding I_{LED} is 0A.

In PWM dimming, I_{LED} is a PWM waveform, the I_{LED} amplitude remains the same and the I_{LED} duty varies with the PWM dimming register.

The PWM dimming duty (D_{PWM}) is set by the PWMx register, and can be calculated with Equation (2):

$$D_{PWM} = \frac{PWMx}{4095} \quad (2)$$

Where PWMx is the D_{PWM} code for channel x (where x = 1, 2…16).

The duty only changes when the PWM duty register's 8 most significant bits (MSB) are written. If PWMx is set to 0, then the corresponding I_{LED} is 0A.

The PWM dimming frequency (f_{PWM}) can be selected via register FPWM[1:0]. Table 1 shows the FPWM[1:0] register settings for different PWM frequencies.

Table 1: PWM Frequency Setting

FPWM[1:0]	f_{PWM}
00	220Hz
01	250Hz (default)
10	280Hz
11	330Hz

To avoid glitches during normal operation, follow the guidelines below:

1. Change the FPWM[1:0] value only when the EN bit is set 0.
2. Write the FPWM register, then allow a 10μs delay before writing to other registers.

Phase Shift

Enable channel-by-channel phase shift by setting the PS_EN bit high.

When the phase shift function is enabled, the rising edge of each channel occurs 40μs after the previous channel. This means that the rising edge of the channel x + 1 (where x = 1, 2…15) I_{LED} occurs 40μs after the rising edge of channel x's I_{LED}.

Synchronized Output for LCD Refresh Frequency

Enable the fault indicator function via the FLTEN bit.

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If FLTEN = 0, fault indication is disabled and the RFSH/FLT pin maintains the output refresh signal, even if a protection is triggered.

If FLTEN = 1, fault indication is enabled and RFSH/FLT is pulled low if a fault occurs.

Table 2 shows the RFSH/FLT output status, which depends on the fault status.

Table 2: RFSH/FLT Output Status

FLTEN	FRFSH[9:0] = 0x000		FRFSH[9:0] = 0x001 to 0x3FF	
	No Fault	Fault	No Fault	Fault
1	Pull high externally	Low	Rectangular signal	Low
0	Pull high externally		Rectangular signal	

The refresh signal frequency ($f_{REFRESH}$) is set via FRFSH[9:0]. If FRFSH[9:0] = 0x000, then RFSH/FLT outputs high. If FRFSH[9:0] = 0x001~0x3FF, then RFSH/FLT outputs a rectangular signal. $f_{REFRESH}$ can be calculated with Equation (3):

$$f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} \text{ (Hz)} \quad (3)$$

Where FRFSH is the FRFSH[9:0] value (>0), and f_{PWM} is set via register FPWM[1:0]. f_{PWM} can be set to 220Hz, 250Hz, 280Hz, or 330Hz.

Note that all values in Equation (3) are decimal-based and $f_{REFRESH}$ does not change until the 8MSB are written.

The internal oscillator is divided by 8. As the clock refreshes the frequency generation, the FRFSH[9:0] register sets the counter number (see Figure 6).

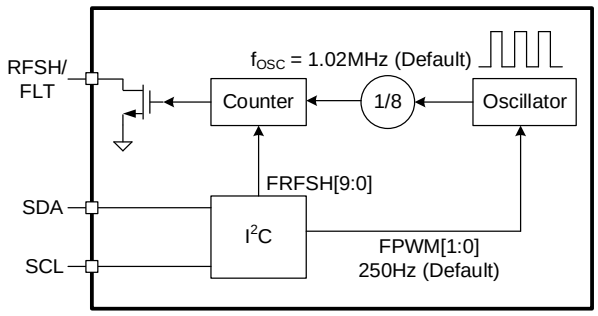

Figure 6: Refresh Frequency Generation

LED Current Slew Rate Control

To reduce EMI, change the I_{LED} rising and falling slew rate for PWM dimming. The I_{LED} rising and falling slew rate is controlled by the SLEW[1:0] register. Table 3 shows the SLEW[1:0] register settings for different slew rates.

Table 3: Slew Rate Setting

SLEW[1:0]	Slew Rate
00	No slew rate
01	5μs
10	10μs
11	20μs

Protections

The MP3326A employs V_{IN} UVLO protection, LED short protection, LED open protection, and thermal shutdown.

The RFSH/FLT pin is an active-low, open-drain output that is pulled high to an external voltage source. If a fault occurs, the corresponding fault bit is set and RFSH/FLT is pulled low.

For LED open and short protection, hiccup mode or latch-off mode can be selected via the LATCH bit in the digital interface.

If LATCH = 1 and a fault occurs, the MP3326A enters latch-off mode. The fault channel remains off until either VIN or EN turns off and resets. After the fault bit is read, FRSH/FLT is pulled high and the fault bit is set. If the fault bit is read again, then the fault bit resets.

If LATCH = 0 and a fault occurs, the MP3326A enters hiccup mode, during which the fault channel tries to conduct for 32μs every 1ms to detect whether the fault has been cleared. Once the fault condition is no longer present, FRSH/FLT is automatically pulled high and the fault bit resets when it is read.

V_{IN} Under-Voltage Lockout (UVLO) Protection

If V_{IN} reaches its UVLO threshold, the IC shuts down and all digital interface registers are reset.

LED Open Protection

If an LED is open, the LEDx (where x = 1, 2…16) voltage (V_{LEDx}) drops. If V_{LEDx} drops below the protection threshold (about 100mV) for 4ms, then LED open protection is triggered. In this scenario, the fault channel turns off, the corresponding open fault bit (CHxO, where x = 1, 2…16) is set, and RFSH/FLT is pulled low.

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LED Short Protection

If there is an LED short condition and V_{LEDx} exceeds the voltage set by STH[1:0] for 4ms, then LED short protection is triggered. Once this protection is triggered, the short channel turns off, the corresponding fault bit (CHxS, where x = 1, 2…16) is set, and RFSH/FLT is pulled low.

The LED short protection threshold (V_{SLP}) is configured via the STH[1:0] register. Table 4 shows the STH[1:0] register setting for different LED short protection thresholds.

Table 4: LED Short Protection Threshold Setting

STH[1:0]	V_{SLP}
00	2V
01	3V
10	4V
11	5V

Over-Temperature Protection (OTP)

If the IC temperature exceeds 170°C, then over-temperature protection (OTP) is triggered, all channels turn off, RFSH/FLT is pulled low, and FT_OTP is set. Once the temperature drops by about 150°C, all channels turn on again and the IC resumes normal operation.

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DIGITAL INTERFACE

Digital Interface Chip Address

The device address is 0x30~0x39, which can be configured via the ADDR resistor (R_{ADDR}). The internal current source flows to R_{ADDR}, and the ADDR voltage (V_{ADDR}) determines the digital interface address. Ten different addresses can be configured via R_{ADDR}.

Table 5 shows the various resistor ratio (R_{ADDR} / R_{ISET}) configurations to set the digital interface address.

Table 5: Digital Interface Address Setting

R_{ADDR} / R_{ISET} Ratio	Digital Interface Address (A3, A2, A1, A0)
<0.05	0000
>0.05, <0.15	0001
>0.15, <0.25	0010
>0.25, <0.35	0011
>0.35, <0.45	0100
>0.45, <0.55	0101
>0.55, <0.65	0110
>0.65, <0.75	0111
>0.75, <0.85	1000
>0.85, <0.95	1001

At start-up, the IC checks the digital interface address first. This address remains the same during operation until the IC's power is reset.

After a start (S) command is sent, the digital interface compatible master sends a 7-bit address, followed by an 8th data direction bit (where 1 = read and 0 = write). The 8th bit indicates the register address to/from which the data is written/read (see Figure 7).

0	1	1	A3	A2	A1	A0	R/W

Figure 7: Digital Interface Compatible Device Address

To avoid glitches during normal operation, follow the steps below:

1. Change the FPWM[1:0] value only when the EN bit is set to 0.
2. Write the FPWM[1:0] register, then allow a 10μs delay before writing to other registers.

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DIGITAL INTERFACE REGISTER MAP

Register Short Name	R/W	Add.	Default	D7	D6	D5	D4	D3	D2	D1	D0
ILED_FRE	R/W	00h	01	RESERVED						FPWM[1:0]	
DEV_CON	R/W	01h	00	FLTEN	LATCH	STH[1:0]		SLEW[1:0]		PS_EN	EN
REFRESH_1	R/W	02h	01	RESERVED					FT_OTP	FRFSH[1:0]	
REFRESH_2	R/W	03h	6A	FRFSH[9:2]							
CHN_EN1	R/W	04h	FF	CH16EN	CH15EN	CH14EN	CH13EN	CH12EN	CH11EN	CH10EN	CH9EN
CHN_EN2	R/W	05h	FF	CH8EN	CH7EN	CH6EN	CH5EN	CH4EN	CH3EN	CH2EN	CH1EN
FAU_OP1	R	06h	00	CH16O	CH15O	CH14O	CH13O	CH12O	CH11O	CH10O	CH9O
FAU_OP2	R	07h	00	CH8O	CH7O	CH6O	CH5O	CH4O	CH3O	CH2O	CH1O
FAU_SH1	R	08h	00	CH16S	CH15S	CH14S	CH13S	CH12S	CH11S	CH10S	CH9S
FAU_SH2	R	09h	00	CH8S	CH7S	CH6S	CH5S	CH4S	CH3S	CH2S	CH1S
ILED_CH1	R/W	0Ah	3F	RESERVED		ICH1[5:0]					
DPWM_CH1_1	R/W	0Bh	0F	RESERVED				PWM1[3:0]			
DPWM_CH1_2	R/W	0Ch	FF	PWM1[11:4]							
ILED_CH2	R/W	0Dh	3F	RESERVED		ICH2[5:0]					
DPWM_CH2_1	R/W	0Eh	0F	RESERVED				PWM2[3:0]			
DPWM_CH2_2	R/W	0Fh	FF	PWM2[11:4]							
ILED_CH3	R/W	10h	3F	RESERVED		ICH3[5:0]					
DPWM_CH3_1	R/W	11h	0F	RESERVED				PWM3[3:0]			
DPWM_CH3_2	R/W	12h	FF	PWM3[11:4]							
ILED_CH4	R/W	13h	3F	RESERVED		ICH4[5:0]					
DPWM_CH4_1	R/W	14h	0F	RESERVED				PWM4[3:0]			
DPWM_CH4_2	R/W	15h	FF	PWM4[11:4]							
ILED_CH5	R/W	16h	3F	RESERVED		ICH5[5:0]					
DPWM_CH5_1	R/W	17h	0F	RESERVED				PWM5[3:0]			
DPWM_CH5_2	R/W	18h	FF	PWM5[11:4]							
ILED_CH6	R/W	19h	3F	RESERVED		ICH6[5:0]					
DPWM_CH6_1	R/W	1Ah	0F	RESERVED				PWM6[3:0]			
DPWM_CH6_2	R/W	1Bh	FF	PWM6[11:4]							
ILED_CH7	R/W	1Ch	3F	RESERVED		ICH7[5:0]					
DPWM_CH7_1	R/W	1Dh	0F	RESERVED				PWM7[3:0]			
DPWM_CH7_2	R/W	1Eh	FF	PWM7[11:4]							
ILED_CH8	R/W	1Fh	3F	RESERVED		ICH8[5:0]					
DPWM_CH8_1	R/W	20h	0F	RESERVED				PWM8[3:0]			
DPWM_CH8_2	R/W	21h	FF	PWM8[11:4]							

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DIGITAL INTERFACE REGISTER MAP *(continued)*

Register Short Name	R/W	Add.	Default	D7	D6	D5	D4	D3	D2	D1	D0
ILED_CH9	R/W	22h	3F	RESERVED		ICH9[5:0]					
DPWM_CH9_1	R/W	23h	0F	RESERVED				PWM9[3:0]			
DPWM_CH9_2	R/W	24h	FF	PWM9[11:4]							
ILED_CH10	R/W	25h	3F	RESERVED		ICH10[5:0]					
DPWM_CH10_1	R/W	26h	0F	RESERVED				PWM10[3:0]			
DPWM_CH10_2	R/W	27h	FF	PWM10[11:4]							
ILED_CH11	R/W	28h	3F	RESERVED		ICH11[5:0]					
DPWM_CH11_1	R/W	29h	0F	RESERVED				PWM11[3:0]			
DPWM_CH11_2	R/W	2Ah	FF	PWM11[11:4]							
ILED_CH12	R/W	2Bh	3F	RESERVED		ICH12[5:0]					
DPWM_CH12_1	R/W	2Ch	0F	RESERVED					PWM12[3:0]		
DPWM_CH12_2	R/W	2Dh	FF	PWM12[11:4]							
ILED_CH13	R/W	2Eh	3F	RESERVED		ICH13[5:0]					
DPWM_CH13_1	R/W	2Fh	0F	RESERVED					PWM13[3:0]		
DPWM_CH13_2	R/W	30h	FF	PWM13[11:4]							
ILED_CH14	R/W	31h	3F	RESERVED		ICH14[5:0]					
DPWM_CH14_1	R/W	32h	0F	RESERVED					PWM14[3:0]		
DPWM_CH14_2	R/W	33h	FF	PWM14[11:4]							
ILED_CH15	R/W	34h	3F	RESERVED		ICH15[5:0]					
DPWM_CH15_1	R/W	35h	0F	RESERVED					PWM15[3:0]		
DPWM_CH15_2	R/W	36h	FF	PWM15[11:4]							
ILED_CH16	R/W	37h	3F	RESERVED		ICH16[5:0]					
DPWM_CH16_1	R/W	38h	0F	RESERVED					PWM16[3:0]		
DPWM_CH16_2	R/W	39h	FF	PWM16[11:4]							

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REGISTER MAP

All registers are in unsigned binary format.

ILED_FRE (0x00)

The ILED_FRE command sets the PWM frequency (f_{PWM}).

Bits	Access	Bit Name	Default	Description
7:2	R	RESERVED	N/A	Reserved.
1:0	R/W	FPWM[1:0]	2'b 01	Sets the LED current pulse-width modulation (PWM) dimming frequency (f_{PWM}). 00: 220Hz 01: 250Hz 10: 280Hz 11: 330Hz To avoid any glitches during normal operation, ensure that the following conditions are met: • FPWM[1:0] can only be changed once the EN bit is set to 0 • Write the FPWM[1:0] register, then wait 10µs before writing any other registers

DEV_CON (0x01)

The DEV_CON command controls the fault indication, latch-off mode, phase-shift functions, as well as the short string protection and slew rate thresholds.

Bits	Access	Bit Name	Default	Description
7	R/W	FLTEN	1'b0	Enables the FRSH/FLT pin's fault indication. 0: Disabled. The RFSH/FLT pin refreshes the signal output 1: Enabled. The RFSH/FLT pin indicates whether a fault has occurred
6	R/W	LATCH	1'b0	Enables latch-off mode. 0: Disabled. The part operates in hiccup mode if a fault occurs 1: Enabled. The part latches off if a fault occurs
5:4	R/W	STH[1:0]	2'b 00	Sets the LED short-load protection (SLP) threshold (V_{SLP}). 00: 2V 01: 3V 10: 4V 11: 5V
3:2	R/W	SLEW[1:0]	2'b 00	Sets the LED current (I_{LED}) slew rate. 00: No slew rate 01: 5µs 10:10µs 11: 20µs
1	R/W	PS_EN	1'b0	Enables the phase shift function. 0: Disabled 1: Enabled, the rising edge of LEDx + 1 occurs 40µs after LEDx (x = 1, 2…15)
0	R/W	EN	1'b0	Enables the IC. 0: Disabled 1: Enabled

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REFRESH_1 (0x02)

The FERRESH_1 command sets the RFSH/FLT pin refresh frequency (2LSB).

Bits	Access	Bit Name	Default	Description
7:3	R	RESERVED	N/A	Reserved.
2	R	FT_OTP	1'b0	Indicates whether an over-temperature (OT) fault has occurred. 0: An OT fault has not occurred 1: An OT fault has occurred
1:0	R/W	FRFSH[1:0]	2'b 01	Sets the 2LSB of the refresh frequency ($f_{REFRESH}$). FRFSH[9:0] = 0x000: Output a high-level voltage FRFSH[9:0] > 0: $f_{REFRESH}$ can be calculated with the following equation: $f_{REFRESH} = \frac{127500}{FRFSH} x \frac{f_{PWM}}{250}$ (Hz) All of the numbers in this equation have a decimal base. $f_{REFRESH}$ does not change until the 8MSB are written.

REFRESH_2 (0x03)

The FERRESH_2 command sets the RFSH/FLT pin refresh frequency (8MSB).

Bits	Access	Bit Name	Default	Description
7:3	R/W	FRFSH[9:2]	8'b 01101010	Sets the 8MSB of $f_{REFRESH}$. FRFSH[9:0] = 0x000: Output a high-level voltage FRFSH[9:0] > 0: $f_{REFRESH}$ can be calculated with the following equation: $f_{REFRESH} = \frac{127500}{FRFSH} x \frac{f_{PWM}}{250}$ (Hz) All of the numbers in this equation have a decimal base. $f_{REFRESH}$ does not change until the 8MSB are written.

CHN_EN1 (0x04)

The CHN_EN1 command sets the enable bits for channels 9 through 16.

Bits	Access	Bit Name	Default	Description
7	RW	CH16EN	1'b1	0: Disable channel 16 1: Enable channel 16
6	RW	CH15EN	1'b1	0: Disable channel 15 1: Enable channel 15
5	RW	CH14EN	1'b1	0: Disable channel 14 1: Enable channel 14
4	RW	CH13EN	1'b1	0: Disable channel 13 1: Enable channel 13
3	RW	CH12EN	1'b1	0: Disable channel 12 1: Enable channel 12
2	RW	CH11EN	1'b1	0: Disable channel 11 1: Enable channel 11
1	RW	CH10EN	1'b1	0: Disable channel 10 1: Enable channel 10
0	RW	CH9EN	1'b1	0: Disable channel 9 1: Enable channel 9

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CHN_EN2 (0x05)

The CHN_EN2 command sets the enable bits for channels 1 through 8.

Bits	Access	Bit Name	Default	Description
7	RW	CH8EN	1’b1	0: Disable channel 8 1: Enable channel 8
6	RW	CH7EN	1’b1	0: Disable channel 7 1: Enable channel 7
5	RW	CH6EN	1’b1	0: Disable channel 6 1: Enable channel 6
4	RW	CH5EN	1’b1	0: Disable channel 5 1: Enable channel 5
3	RW	CH4EN	1’b1	0: Disable channel 4 1: Enable channel 4
2	RW	CH3EN	1’b1	0: Disable channel 3 1: Enable channel 3
1	RW	CH2EN	1’b1	0: Disable channel 2 1: Enable channel 2
0	RW	CH1EN	1’b1	0: Disable channel 1 1: Enable channel 1

FAU_OP1 (0x06)

The FAU_OP1 command reads the open fault bits for channels 9 through 16.

Bits	Access	Bit Name	Default	Description
7	R	CH16O	1’b0	0: No open fault has occurred on channel 16 1: An open fault has occurred on channel 16
6	R	CH15O	1’b0	0: No open fault has occurred on channel 15 1: An open fault has occurred on channel 15
5	R	CH14O	1’b0	0: No open fault has occurred on channel 14 1: An open fault has occurred on channel 14
4	R	CH13O	1’b0	0: No open fault has occurred on channel 13 1: An open fault has occurred on channel 13
3	R	CH12O	1’b0	0: No open fault has occurred on channel 12 1: An open fault has occurred on channel 12
2	R	CH11O	1’b0	0: No open fault has occurred on channel 11 1: An open fault has occurred on channel 11
1	R	CH10O	1’b0	0: No open fault has occurred on channel 10 1: An open fault has occurred on channel 10
0	R	CH9O	1’b0	0: No open fault has occurred on channel 9 1: An open fault has occurred on channel 9

FAU_OP2 (0x07)

The FAU_OP2 command reads the open fault bits for channels 1 through 8.

Bits	Access	Bit Name	Default	Description
7	R	CH8O	1’b0	0: No open fault has occurred on channel 8 1: An open fault has occurred on channel 8
6	R	CH7O	1’b0	0: No open fault has occurred on channel 7 1: An open fault has occurred on channel 7

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5	R	CH6O	1’b0	0: No open fault has occurred on channel 6 1: An open fault has occurred on channel 6
4	R	CH5O	1’b0	0: No open fault has occurred on channel 5 1: An open fault has occurred on channel 5
3	R	CH4O	1’b0	0: No open fault has occurred on channel 4 1: An open fault has occurred on channel 4
2	R	CH3O	1’b0	0: No open fault has occurred on channel 3 1: An open fault has occurred on channel 3
1	R	CH2O	1’b0	0: No open fault has occurred on channel 2 1: An open fault has occurred on channel 2
0	R	CH1O	1’b0	0: No open fault has occurred on channel 1 1: An open fault has occurred on channel 1

FAU_SH1 (0x08)

The FAU_SH1 command reads the short fault bits for channels 9 through 16.

Bits	Access	Bit Name	Default	Description
7	R	CH16S	1’b0	0: No short fault has occurred on channel 16 1: A short fault has occurred on channel 16
6	R	CH15S	1’b0	0: No short fault has occurred on channel 15 1: A short fault has occurred on channel 15
5	R	CH14S	1’b0	0: No short fault has occurred on channel 14 1: A short fault has occurred on channel 14
4	R	CH13S	1’b0	0: No short fault has occurred on channel 13 1: A short fault has occurred on channel 13
3	R	CH12S	1’b0	0: No short fault has occurred on channel 12 1: A short fault has occurred on channel 12
2	R	CH11S	1’b0	0: No short fault has occurred on channel 11 1: A short fault has occurred on channel 11
1	R	CH10S	1’b0	0: No short fault has occurred on channel 10 1: A short fault has occurred on channel 10
0	R	CH9S	1’b0	0: No short fault has occurred on channel 9 1: A short fault has occurred on channel 9

FAU_SH2 (0x09)

The FAU_SH2 command reads the short fault bits for channels 1 through 8.

Bits	Access	Bit Name	Default	Description
7	R	CH8S	1’b0	0: No short fault has occurred on channel 8 1: A short fault has occurred on channel 8
6	R	CH7S	1’b0	0: No short fault has occurred on channel 7 1: A short fault has occurred on channel 7
5	R	CH6S	1’b0	0: No short fault has occurred on channel 6 1: A short fault has occurred on channel 6
4	R	CH5S	1’b0	0: No short fault has occurred on channel 5 1: A short fault has occurred on channel 5
3	R	CH4S	1’b0	0: No short fault has occurred on channel 4 1: A short fault has occurred on channel 4
2	R	CH3S	1’b0	0: No short fault has occurred on channel 3 1: A short fault has occurred on channel 3

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1	R	CH2S	1’b0	0: No short fault has occurred on channel 2 1: A short fault has occurred on channel 2
0	R	CH1S	1’b0	0: No short fault has occurred on channel 1 1: A short fault has occurred on channel 1

ILED_CH1 (0x0A)

The ILED_CH1 command sets the LED1 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH1[5:0]	6’b 111111	Sets the LED channel 1 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH1_1 (0x0B)

The DPWM_CH1_1 command sets the PWM dimming duty’s 4LSB for the channel 1 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM1[3:0]	4’b 1111	Sets the PWM dimming duty’s 4LSB for the channel 1 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH1_2 (0x0C)

The DPWM_CH1_2 command sets the PWM dimming duty’s 8MSB for the channel 1 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM1[11:4]	8’b 11111111	Sets the PWM dimming duty’s 8MSB for the channel 1 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH2 (0x0D)

The ILED_CH2 command sets the LED2 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH2[5:0]	6’b 111111	Sets the LED channel 2 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH2_1 (0x0E)

The DPWM_CH2_1 command sets the PWM dimming duty’s 4LSB for the channel 2 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM2[3:0]	4’b 1111	Sets the PWM dimming duty’s 4LSB for the channel 2 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH2_2 (0x0F)

The DPWM_CH2_2 command sets the PWM dimming duty’s 8MSB for the channel 2 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM2[11:4]	8’b 11111111	Sets the PWM dimming duty’s 8MSB for the channel 2 I_{LED}. The dimming duty only changes once the 8MSB are written.

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ILED_CH3 (0x10)

The ILED_CH3 command sets the LED3 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH3[5:0]	6’b 111111	Sets the LED channel 3 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH3_1 (0x11)

The DPWM_CH3_1 command sets the PWM dimming duty’s 4LSB for the channel 3 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM3[3:0]	4’b 1111	Sets the PWM dimming duty’s 4LSB for the channel 4 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH3_2 (0x12)

The DPWM_CH3_2 command sets the PWM dimming duty’s 8MSB for the channel 3 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM3[11:4]	8’b 11111111	Sets the PWM dimming duty’s 8MSB for the channel 3 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH4 (0x13)

The ILED_CH4 command sets the LED4 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH4[5:0]	6’b 111111	Sets the LED channel 4 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH4_1 (0x14)

The DPWM_CH4_1 command sets the PWM dimming duty’s 4LSB for the channel 4 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM4[3:0]	4’b 1111	Sets the PWM dimming duty’s 4LSB for the channel 4 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH4_2 (0x15)

The DPWM_CH4_2 command sets the PWM dimming duty’s 8MSB for the channel 4 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM4[11:4]	8’b 11111111	Sets the PWM dimming duty’s 8MSB for the channel 4 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH5 (0x16)

The ILED_CH5 command sets the LED5 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH5[5:0]	6’b 111111	Sets the LED channel 5 current for analog dimming. See Equation (1) on page 13 for details.

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DPWM_CH5_1 (0x17)

The DPWM_CH5_1 command sets the PWM dimming duty's 4LSB for the channel 5 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM5[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 5 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH5_2 (0x18)

The DPWM_CH5_2 command sets the PWM dimming duty's 8MSB for the channel 5 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM5[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 5 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH6 (0x19)

The ILED_CH6 command sets the LED6 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH6[5:0]	6'b 111111	Sets the LED channel 6 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH6_1 (0x1A)

The DPWM_CH6_1 command sets the PWM dimming duty's 4LSB for the channel 6 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM6[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 6 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH6_2 (0x1B)

The DPWM_CH6_2 command sets the PWM dimming duty's 8MSB for the channel 6 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM6[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 6 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH7 (0x1C)

The ILED_CH7 command sets the LED7 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH7[5:0]	6'b 111111	Sets the LED channel 7 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH7_1 (0x1D)

The DPWM_CH7_1 command sets the PWM dimming duty's 4LSB for the channel 7 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM7[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 7 I_{LED}. The dimming duty only changes once the 8MSB are written.

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DPWM_CH7_2 (0x1E)

The DPWM_CH7_2 command sets the PWM dimming duty's 8MSB for the channel 7 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM7[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 7 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH8 (0x1F)

The ILED_CH8 command sets the LED8 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH8[5:0]	6'b 111111	Sets the LED channel 8 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH8_1 (0x20)

The DPWM_CH8_1 command sets the PWM dimming duty's 4LSB for the channel 8 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM8[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 8 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH8_2 (0x21)

The DPWM_CH8_2 command sets the PWM dimming duty's 8MSB for the channel 8 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM8[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 8 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH9 (0x22)

The ILED_CH9 command sets the LED9 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH9[5:0]	6'b 111111	Sets the LED channel 9 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH9_1 (0x23)

The DPWM_CH9_1 command sets the PWM dimming duty's 4LSB for the channel 9 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM9[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 9 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH9_2 (0x24)

The DPWM_CH9_2 command sets the PWM dimming duty's 8MSB for the channel 9 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM9[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 9 I_{LED}. The dimming duty only changes once the 8MSB are written.

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ILED_CH10 (0x25)

The ILED_CH10 command sets the LED10 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH10[5:0]	6’b 111111	Sets the LED channel 10 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH10_1 (0x26)

The DPWM_CH10_1 command sets the PWM dimming duty’s 4LSB for the channel 10 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM10[3:0]	4’b 1111	Sets the PWM dimming duty’s 4LSB for the channel 10 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH10_2 (0x27)

The DPWM_CH10_2 command sets the PWM dimming duty’s 8MSB for the channel 10 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM10[11:4]	8’b 11111111	Sets the PWM dimming duty’s 8MSB for the channel 10 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH11 (0x28)

The ILED_CH11 command sets the LED11 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH11[5:0]	6’b 111111	Sets the LED channel 11 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH11_1 (0x29)

The DPWM_CH11_1 command sets the PWM dimming duty’s 4LSB for the channel 11 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM11[3:0]	4’b 1111	Sets the PWM dimming duty’s 4LSB for the channel 11 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH11_2 (0x2A)

The DPWM_CH11_2 command sets the PWM dimming duty’s 8MSB for the channel 11 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM11[11:4]	8’b 11111111	Sets the PWM dimming duty’s 8MSB for the channel 11 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH12 (0x2B)

The ILED_CH12 command sets the LED12 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH12[5:0]	6’b 111111	Sets the LED channel 12 current for analog dimming. See Equation (1) on page 13 for details.

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DPWM_CH12_1 (0x2C)

The DPWM_CH12_1 command sets the PWM dimming duty's 4LSB for the channel 12 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM12[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 12 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH12_2 (0x2D)

The DPWM_CH12_2 command sets the PWM dimming duty's 8MSB for the channel 12 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM12[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 12 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH13 (0x2E)

The ILED_CH13 command sets the LED13 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH13[5:0]	6'b 111111	Sets the LED channel 13 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH13_1 (0x2F)

The DPWM_CH13_1 command sets the PWM dimming duty's 4LSB for the channel 13 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM13[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 13 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH13_2 (0x30)

The DPWM_CH13_2 command sets the PWM dimming duty's 8MSB for the channel 13 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM13[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 13 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH14 (0x31)

The ILED_CH14 command sets the LED14 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH14[5:0]	6'b 111111	Sets the LED channel 14 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH14_1 (0x32)

The DPWM_CH14_1 command sets the PWM dimming duty's 4LSB for the channel 14 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM14[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 14 I_{LED}. The dimming duty only changes once the 8MSB are written.

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DPWM_CH14_2 (0x33)

The DPWM_CH14_2 command sets the PWM dimming duty's 8MSB for the channel 14 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM14[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 14 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH15 (0x34)

The ILED_CH15 command sets the LED15 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH15[5:0]	6'b 111111	Sets the LED channel 15 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH15_1 (0x35)

The DPWM_CH15_1 command sets the PWM dimming duty's 4LSB for the channel 15 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM15[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 15 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH15_2 (0x36)

The DPWM_CH15_2 command sets the PWM dimming duty's 8MSB for the channel 15 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM15[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 15 I_{LED}. The dimming duty only changes once the 8MSB are written.

ILED_CH16 (0x37)

The ILED_CH16 command sets the LED16 current amplitude.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ICH16[5:0]	6'b 111111	Sets the LED channel 16 current for analog dimming. See Equation (1) on page 13 for details.

DPWM_CH16_1 (0x38)

The DPWM_CH16_1 command sets the PWM dimming duty's 4LSB for the channel 16 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM16[3:0]	4'b 1111	Sets the PWM dimming duty's 4LSB for the channel 16 I_{LED}. The dimming duty only changes once the 8MSB are written.

DPWM_CH16_2 (0x39)

The DPWM_CH16_2 command sets the PWM dimming duty's 8MSB for the channel 16 I_{LED}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM16[11:4]	8'b 11111111	Sets the PWM dimming duty's 8MSB for the channel 16 I_{LED}. The dimming duty only changes once the 8MSB are written.

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APPLICATION INFORMATION

LED Current Setting

Connect a resistor from the ISET pin to GND to set I_{LED} for all 16 channels. I_{LED} can be calculated with Equation (4):

$$I_{LED}(mA)=\frac{1200}{R_{ISET}(k\Omega)} \quad (4)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 8 and following the guidelines below:

1. Place the VIN capacitor as close as possible to the VIN pin.
2. Add at least 3 vias near the VIN capacitor's ground point.
3. Ensure that the traces from the LED anode to the LEDx pins are wide enough to support the set current (up to 80mA).

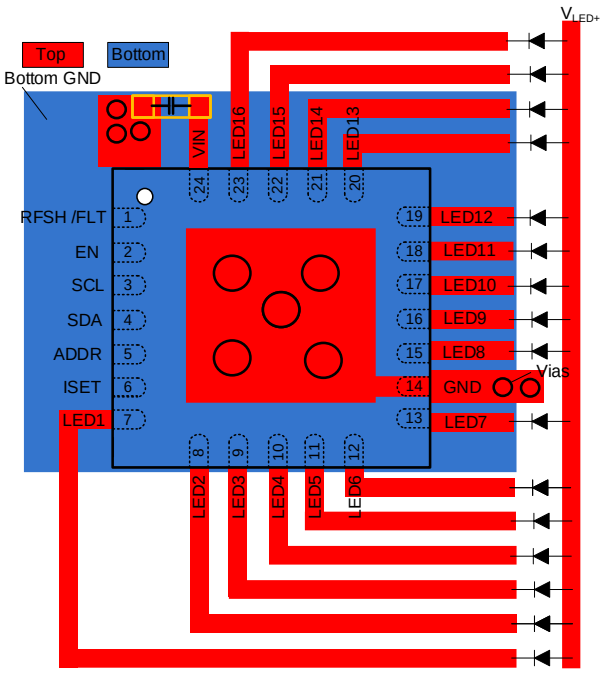

Figure 8: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

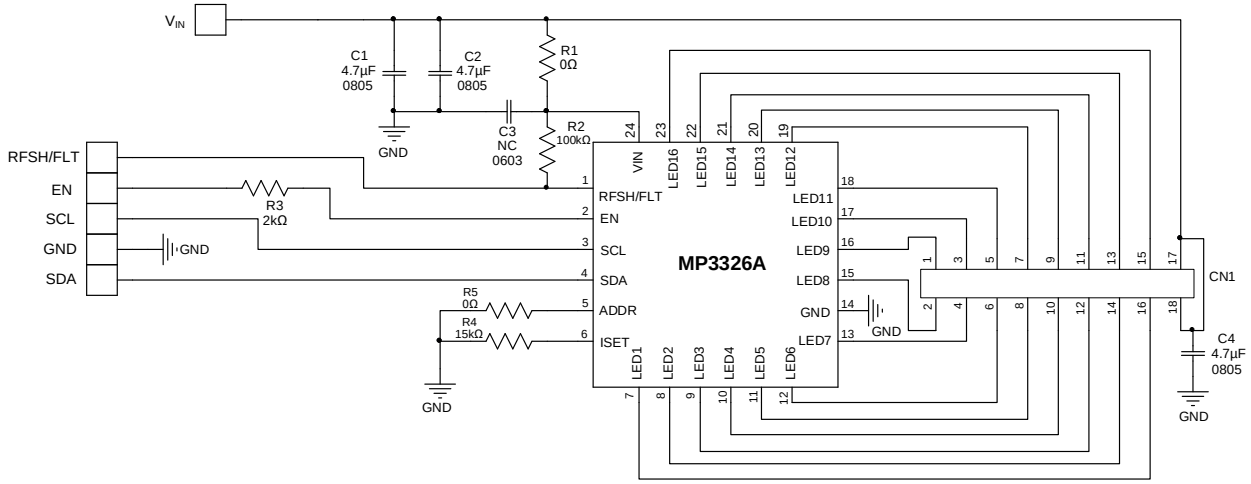

Figure 9: Typical Application Circuit (I_{LED} = 80mA/Channel)

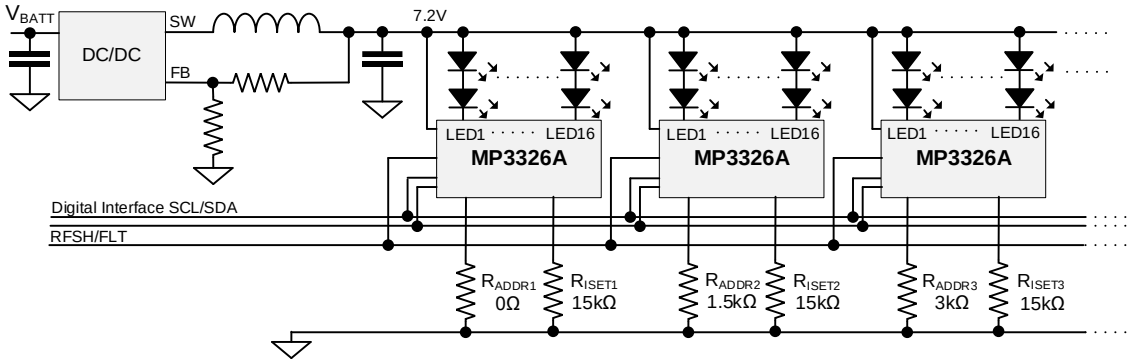

Figure 10: Typical System Application Circuit (2 LED in Series, I_{LED} = 80mA/Channel)

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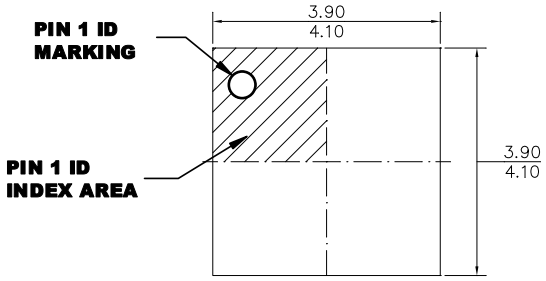
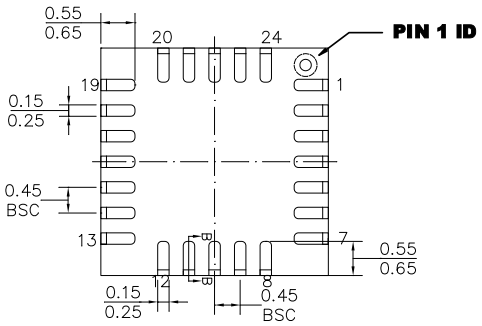
PACKAGE INFORMATION

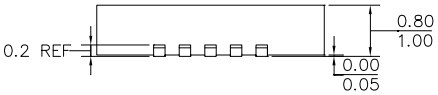
QFN-24 (4mmx4mm)
Wettable Flank



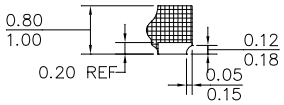
TOP VIEW



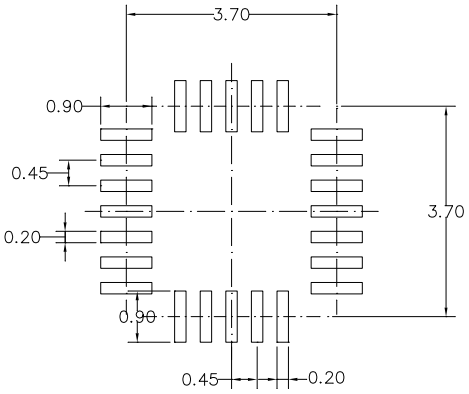
BOTTOM VIEW



SIDE VIEW



SECTION B-B



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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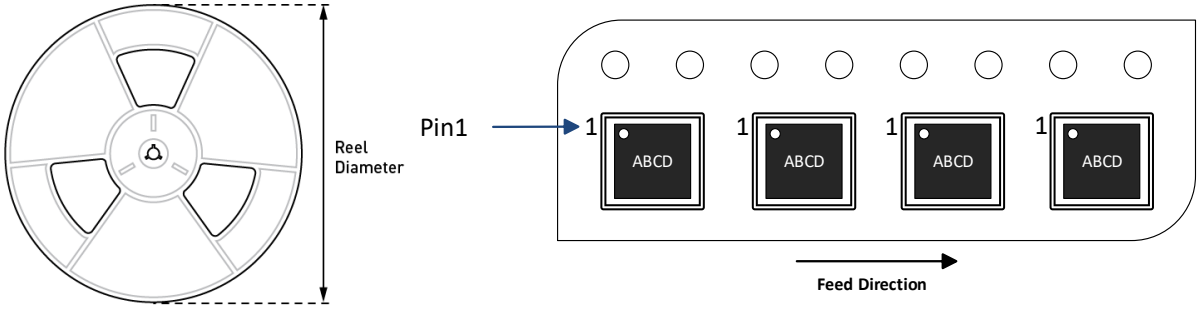
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3326AGRE-Z	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/8/2023	Initial Release	-

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