MP3312

2.7V-5.5V Input , 38V OVP, Dual-Channel White LED Driver

The Future of Analog IC Technology

DESCRIPTION

The MP3312 is a dual-channel step-up WLED driver with integrated 40V MOSFET, and supports 2.7V to 5.5V power supply input. It uses peak current mode to regulate the LED current which is set by external resistor.

The MP3312 employs 1.2MHz fixed switching frequency. It features supporting both PWM input analog dimming and digital analog dimming to accurately regulate the dimming current.

The MP3312 integrates current source to balance LED current, which leads good ILED matching and accuracy performance.

In addition, the MP3312 has LED open and short protection, cycle by cycle current limit protection, and thermal shutdown protection. It is available in tiny WLCSP1.35x1.35-9 package.

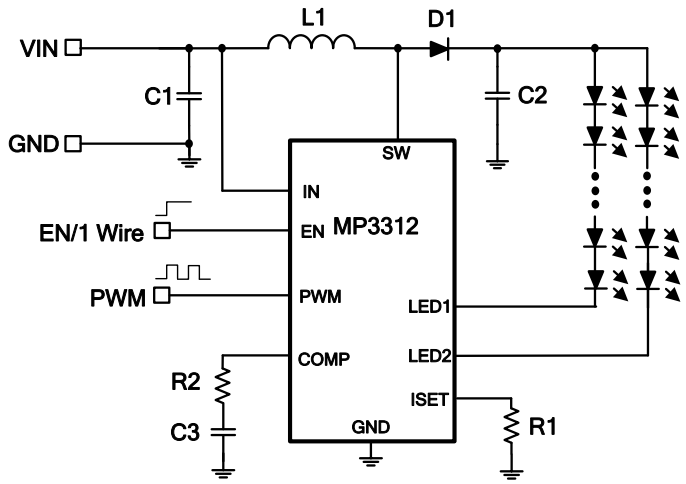
FEATURES

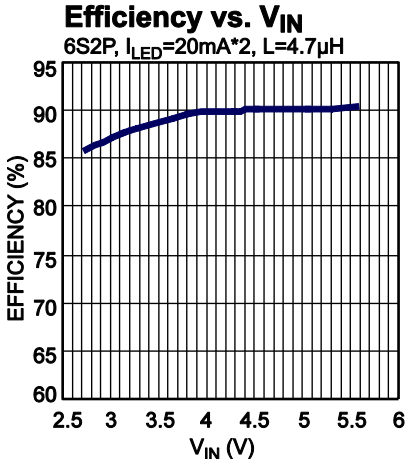
- 2.7V~5.5V Input Voltage
- 1.2MHz Switching Frequency
- Dual Channels Support up to 30mA/String
- 1% Current Matching Between LED Channels
- +/-2% Current Accuracy
- 38V OVP Protection
- PWM Input Analog Dimming Mode
- 5kHz to100kHz PWM Input Analog Dimming
- 1-Wire Interface for Digital Dimming
- 9-bit Dimming Resolution
- Internal Soft Start to Reduce Inrush Current
- Available in WLCSP1.35x1.35-9 Package

APPLICATIONS

- Feature Phone and Smart Phones
- Tablets
- GPS Receivers
- <10 inch LCD video displays with one-cell Li-ion battery

TYPICAL APPLICATION



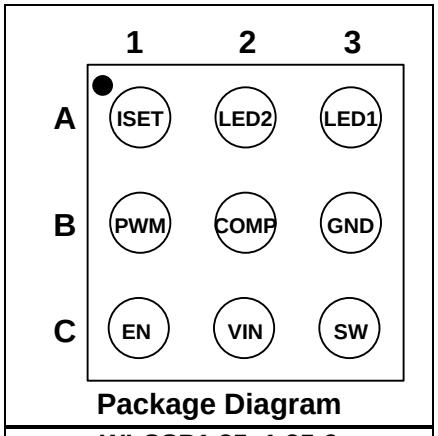


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3312GC	WLCSP1.35x1.35-9	BU

* For Tape & Reel, add suffix –Z (e.g. MP3312GC–Z);

PACKAGE REFERENCE



Package Diagram

WLCSP1.35x1.35-9

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +6V
V_{SW} ..... -1V to +40V
V_{LED1}, V_{LED2} ..... -0.3V to +40V
All Other Pins ..... –0.3V to +6V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Continuous Power Dissipation (T_A = 25°C) (2)
WLCSP1.35x1.35-9 ..... 1.04W

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.7V to 5.5V
Operating Junction Temp. ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

WLCSP1.35x1.35-9 ..... 120 ..... 12 ..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} =3.7V, V_{EN} = V_{PWM}= HIGH, Typical Values are at T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Power Supply						
Operating Input Voltage	V_{IN}		2.7		5.5	V
Supply Current (Quiescent)	I_Q	V_{IN}=3.7V, V_{EN}= V_{PWM}= High, no load with switching		1	2	mA
Supply Current (Shutdown)	I_{ST}	V_{EN}=0V, V_{IN}=3.7V			1	μA
Input UVLO Threshold	V_{IN_UVLO}	Rising Edge		2.4	2.6	V
Input UVLO Hysteresis				200		mV
OSCILLATOR						
Switching Frequency	f_{SW}		1	1.2	1.4	MHz
Maximum Duty Cycle	D_{MAX}		93	95		%
Minimum On Time(5)	T_{ON_MIN}			100		ns
Power Switch						
Main Switch On-Resistance	R_{DSON_M}	VIN=3.7V		0.2		Ω
Error Amplifier						
Error Amplifier Transconductance	gm			370		uS
Max Sink/Source Current				42		μA
Current Regulation						
VLEDx Regulation Voltage	V_{REG}	ILED1=ILED2=20mA		240		mV
ISET Pin Voltage	V_{ISET}		1.207	1.232	1.247	V
Current Multiplier	K_{ISET}			1020		
Current Accuracy		I_{ISET} =20uA, ($\|I_{MIN}$-$I_{ISET}\|$/I_{ISET},$\|I_{MAX}$-$I_{ISET}\|$/ I_{ISET})	-2		2	%
Current Matching		I_{ISET} =20uA, (I_{MAX} –I_{MIN}) /I_{AVG}		1	2	%
Current Sink Max Output Current			30			mA
EN & PWM Logic						
PWM Input High Threshold	V_{PWM_HI}	V_{PWM} Falling	1.2			V
PWM Input Low Threshold	V_{PWM_LO}	V_{PWM} Rising			0.4	V
EN High Voltage	V_{EN_HIGH}	V_{EN} Rising	1.2			V
EN Low Voltage	V_{EN_LOW}	V_{EN} Falling			0.4	V
EN & PWM Pull Down Resistor	R_{PD}			800		kΩ
EN Low Logic To Shutdown Time	T_{SD_EN}	EN High to Low	2.5			ms
PWM Low Logic To Shutdown Time	T_{SD_PWM}	PWM High to Low	20			ms
Minimum PWM On Time	T_{PO_MIN}			200		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} =3.7V, V_{EN} = V_{PWM}= HIGH, Typical Values are at T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Protection						
OVP Voltage	V_{OVP}		37	38	39.5	V
Cycle-Cycle Current Limit	I_{LIM}	Max Duty Cycle	1.2	1.8		A
Startup Current Limits(5)	I_{LIM_START}	Max Duty Cycle		1		A
Time Step for Half Current Limit(5)	T_{LIM_HALF}			6		ms
LEDx Threshold when No Switching				560		mV
LEDx Over Voltage Threshold	V_{OVP_LED}		4.5	5	5.5	V
Thermal Shutdown Threshold	T_{ST}			150		°C
Thermal Shutdown Hysteresis				25		°C
1-Wire Interface						
1-Wire Detection Delay Time	t_{DELAY}		100			µs
1-Wire Detection Time	$t_{DETECTION}$		260			µs
1-Wire Detection Window	t_{WIN}		1			ms
Start Time of Program Stream	t_{START}		2			µs
End Time of Program Stream	t_{EOS}		2		360	µs
High Time of Logic 0 Bit	t_{H_LB}		5		180	µs
Low Time of Logic 0 Bit	t_{L_LB}		3* t_{H_LB}		360	µs
High Time of Logic 1 Bit	t_{H_HB}		3* t_{L_HB}		360	µs
Low Time of Logic 1 Bit	t_{L_HB}		5		180	µs
Acknowledge Valid Time	t_{ACKval}				2	µs
Duration of Acknowledge Signal	t_{ACK}				512	µs
Acknowledge Output Voltage Low(6)	V_{ACKL}	Open drain, R_{PULLUP}= 15 kΩ to V_{IN}			0.4	V

Notes:

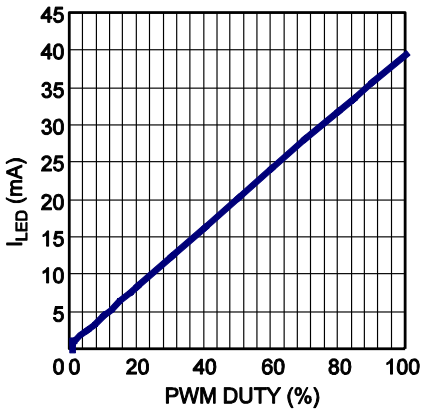
5) guarantee by design and characterization

6) ACK signal is active 0 (when ACK signal is true , data line is pulled down by chip),and this signal only reply when RFA bit is set to 1.If you want use ACK signal, the master should have an open-drain output, and data line should be pulled high by master with a resistor load.

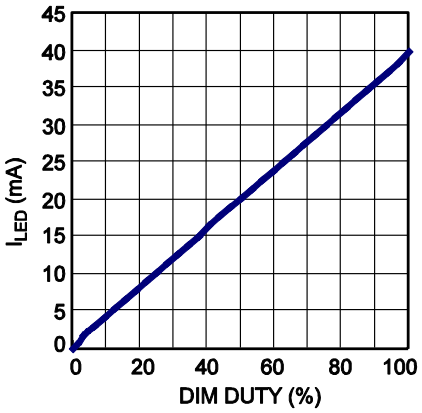
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.7V, 6*LEDs/string, ILED1=ILED2=20mA, L = 4.7μH, T_A = 25°C, unless otherwise noted.

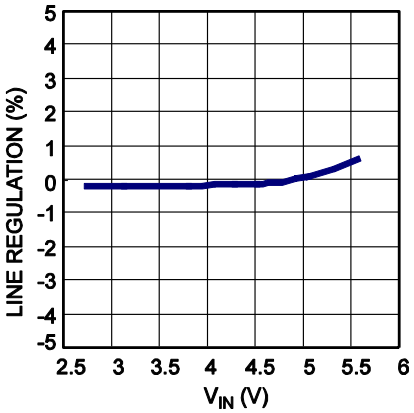
Analog Dimming Curve



1 Wire Dimming Curve



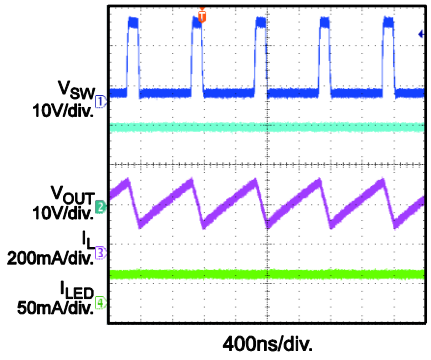
Line Regulation



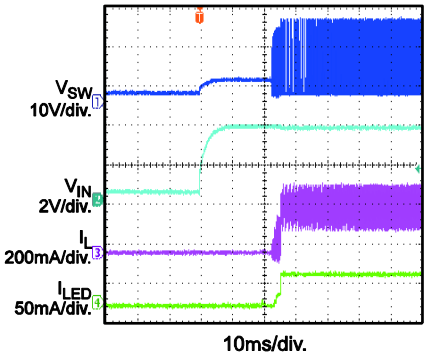
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, 6*LEDs/string, ILED1=ILED2=20mA, L = 4.7μH, T_A = 25°C, unless otherwise noted.

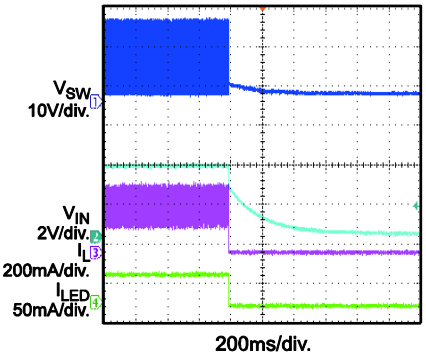
Steady State



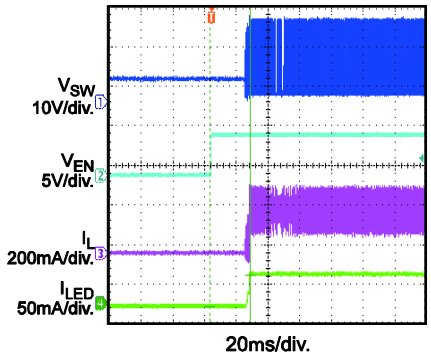
V_{IN} Power On



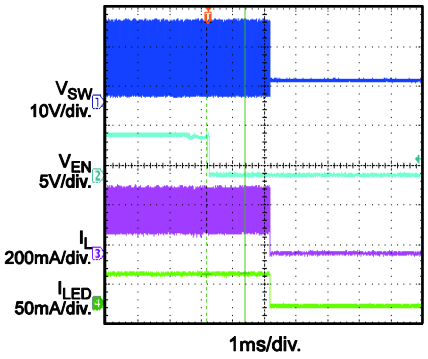
V_{IN} Power Off



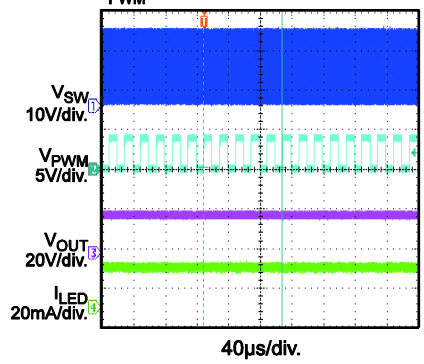
En Power On



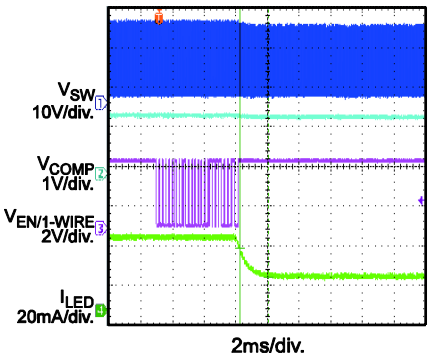
En Power Off



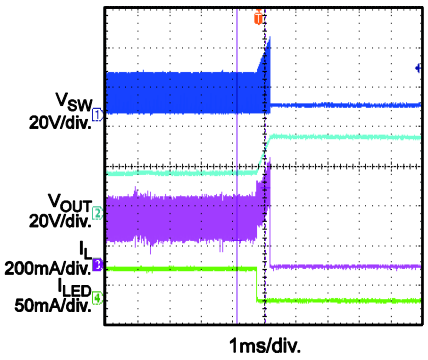
PWM Input Analog Dimming
f_{PWM}=50kHz



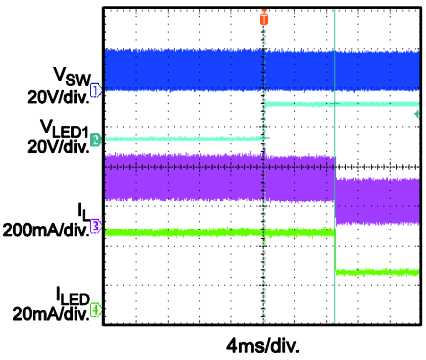
1-Wire Dimming (01FF to 0100)



Open Load Protection



Short 1 String Protection



PIN FUNCTIONS

Pin #	Name	Description
A1	ISET	Full scale LED current set pin. Connecting a resistor between this pin and GND sets the full scale current.
A2	LED2	LED2 current sink pin.
A3	LED1	LED1 current sink pin.
B1	PWM	PWM signal input pin. 5kHz to 100kHz PWM Signal is recommended to this pin to do the analog current dimming. Low logic for >20ms shuts down the IC.
B2	COMP	Internal error amplifier output pin. Connect a capacitor to compensate the system.
B3	GND	GND pin.
C1	EN	Enable and 1wire input pin. High logic enables the IC and low logic >2.5ms shuts down the IC.
C2	VIN	Power supply input pin. Connect a ceramic capacitor nearby this pin to bypass the IC.
C3	SW	Drain connection of the internal N-CH power MOSFET.

FUNCTIONAL BLOCK DIAGRAM

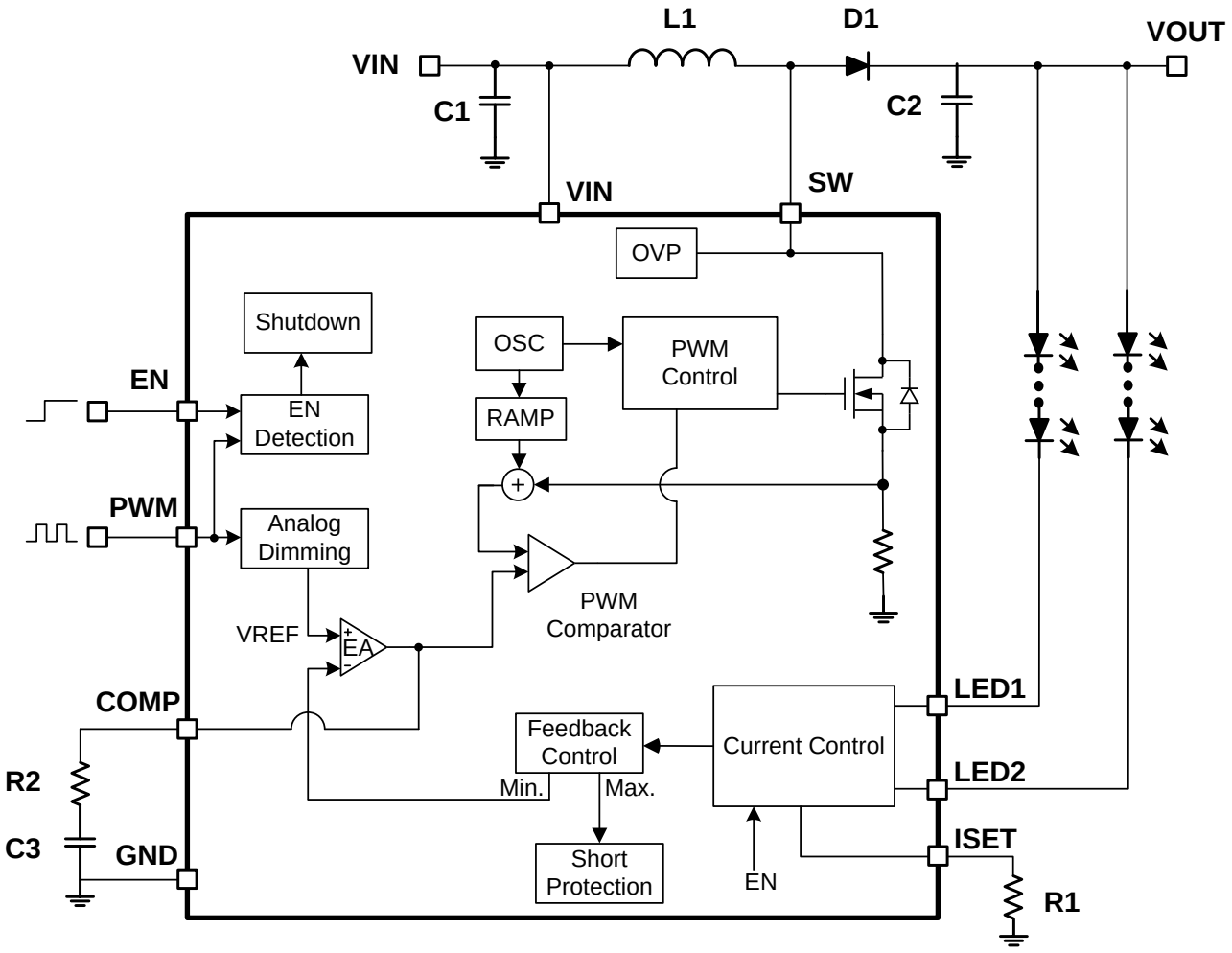


Figure 1— Functional Block Diagram

OPERATION

The MP3312 employs the fixed switching frequency, peak current mode control architecture and 2 regulated current sinks to power the LED array. The operation of the MP3312 can be understood by referring to the below function block diagram.

System Startup

Either pulling EN or PWM to high enables the IC operation while pulling EN to GND for >2.5ms or pulling PWM to GND for >20ms shuts down the IC.

When enabled, the MP3312 checks the topology connection first. The MP3312 also checks other safety limits, including UVLO and over-temperature protection (OTP). If all the protections pass, the chip then starts boosting the step-up converter with an internal soft-start.

It is recommended that the enable signal occurs after the establishment of the input voltage and PWM dimming signal during the start-up sequence to avoid large inrush current.

Switching Operation

At the start of each oscillator cycle the main low side FET (M1) is turned on through the control circuitry. To prevent sub-harmonic oscillation at duty cycle greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the positive input of the PWM generation comparator. When this voltage equals the output voltage of the error amplifier the main power FET is turned off. Then the inductor current flows through the free-wheeling diode, which forces the inductor current to decrease. The output voltage of the internal error amplifier is an amplified signal of the difference between the reference voltage and the feedback voltage. The converter automatically chooses the lowest active LEDX pin voltage to provide a high-enough bus voltage to power all the LED arrays.

If the feedback voltage drops below the reference, the output of the error amplifier increases. It results in more current flowing through the MOSFET, thus increasing the power delivered to the output. This forms a closed loop that regulates the output voltage.

Dimming Control

MP3312 supports analog dimming and 1-wire digital set dimming mode to regulate the WLED current.

To do analog dimming, apply a PWM signal to PWM pin by adjusting the LED current amplitude. The internal filter is integrated and the PWM signal with 5k~100kHz range is supported. Internal dimming signal duty detection circuit automatically changes the internal reference lineally to regulate the current.

In addition, the EN pin supports 1-wire interface to do current dimming control. The 1-wire description and protocol details are as follow.

1-wire Interface

1-wire interface is based on master-slave structure which is designed for digital dimming. The EN pin is multipurpose as single port to receive LED brightness data. The rate to detect the bit can automatically range from 1.39kBit/sec to 50kBit/sec.

The command sent to chip (slave) contains 24 bits, 9-bit dimming data, 8-bit device address and RFA bit are included. Chip detects the bit in series and it transmits the LSB first and MSB finally.

The control bits description is as below and Figure 2 shows the command bytes structure in detail.

- D0-D8 are the dimming data bits which achieve 9-bit dimming resolution
- Bit9 and bit11-bit15 is reserved. Set to 0
- RFA bit indicates master needs Request of Acknowledge or not.
- Device address byte is DA0-DA7. The device address byte is set to 0x8F.

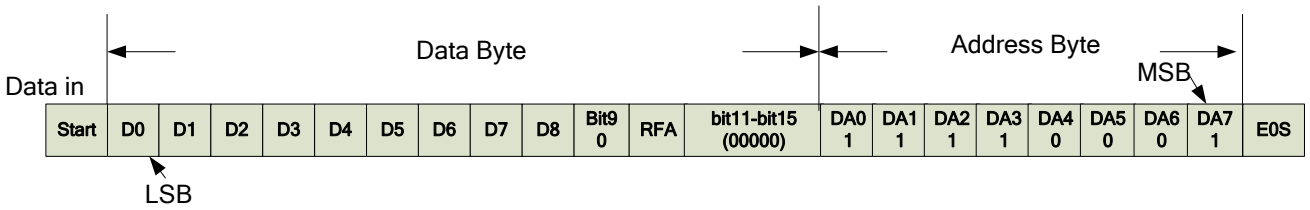


Figure 2—1-wire command structure

1-wire interface defines logic 0 and logic 1 by comparing the time of the signal low level and high level, 1 cycle means 1 logic bit. The bit detection starts with a falling edge on the EN pin and ends with the next falling edge. Shown as Figure 3

Low logic (logic 0): $t_{LOW} \geq 3^* t_{HIGH}$

High logic (logic 1): $t_{HIGH} \geq 3^* t_{LOW}$

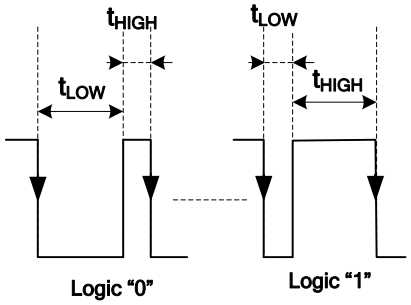


Figure 3—1-Wire Bit Definition

The EN pin needs to distinguish EN signal and digital dimming signal when set up boost driver. Chip only receives 1-wire signal when EN pin signal matches 1-wire protocol during 1ms 1-wire detection window. 1-wire dimming sequence is described as below, and shown in Figure 4.

1. Pulling VIN and PWM to high.
2. Pulling data line from low to high for t_{DELAY} (1-wire detection delay time, 100us) and this rising edge is the start of 1-wire detection window.
3. After 1-wire detection delay time, pulling data line to low for more than $t_{DETECTION}$ (1-wire detection time, 260us). Then pulling data line to high.
4. The sum of 1-wire detection delay time and 1-wire detection time should be less than t_{WIN}. (The time of 1-wire detection window,1ms).

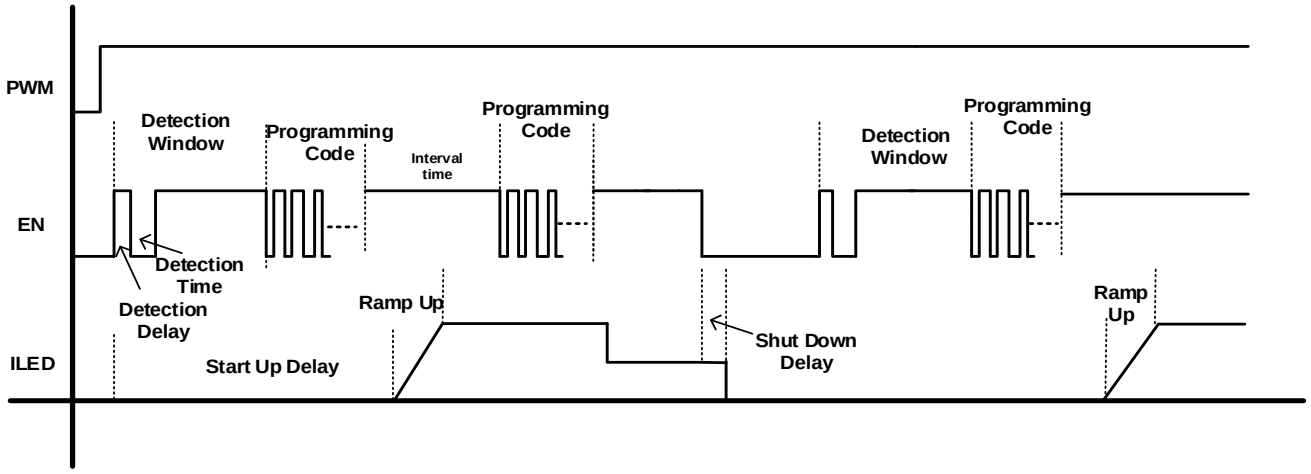


Figure 4—1-Wire Dimming Sequence

In addition, before chip starts to receive each command with first falling edge, data line should keep high level for t_{START} (min. 2us) time. which The transmission of each command is completed with low level for t_{EOS} (min. 2us).Shown in Figure 5.

There is a counter (typical: 2MHz/13bits) to measure the time of the high/low level in 1-Wire *interface*. The counter keeps work in the interval time between 2 commands, and it will recount after time out in single level. For preventing the mis-trigger, the counter of the interval time should result at the value larger than 5, otherwise the first bit of the next command will be missed. If bit-missed happens, the bit-malposition will happen in later communication process, and it will cause 1-Wire communication fail (1-Wire digital set dimming fail) since for the wrong address byte. Increasing the t_{EOS} will do help for MP3312 to recover from communication failure (when t_{EOS}=300us, the communication fail will recover soon)

The ACK signal feedback to master or not is dependent on RFA bit. If ACK is needed, the master should have an open-drain output, and data line should be pulled high by master with a resistor load.

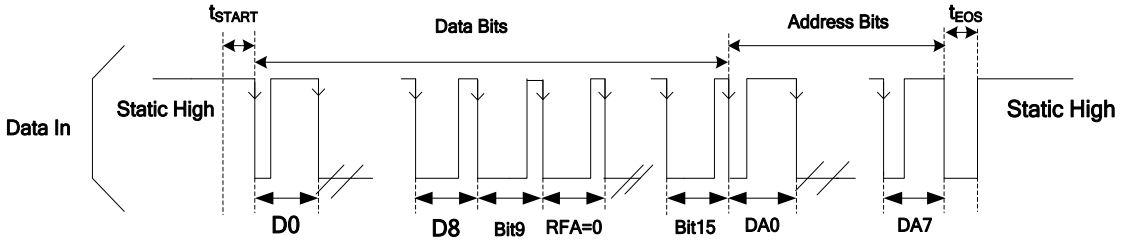


Figure 5— Data-line Timing when RFA=0

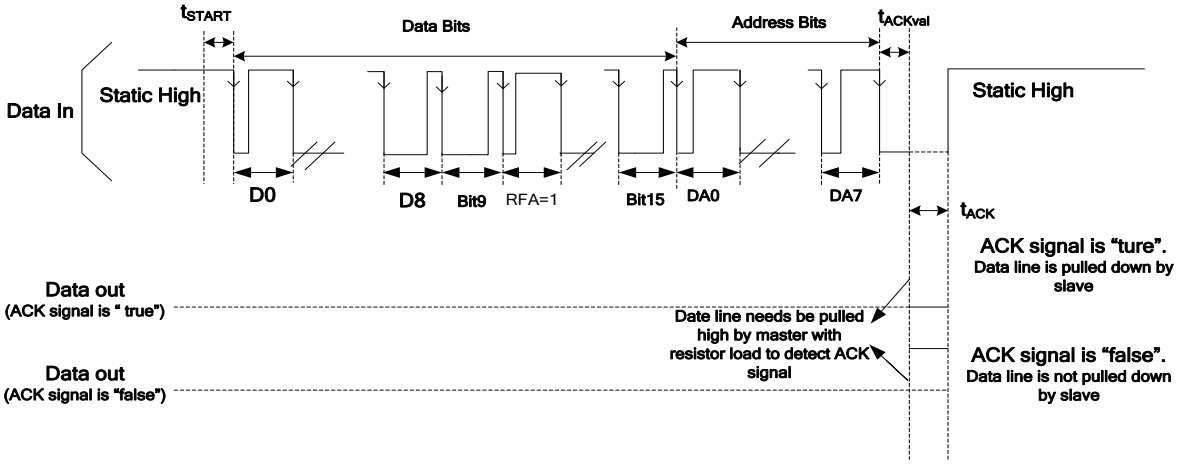


Figure 6—Data-line Timing when RFA=1

If RFA=0, No ACK signal feedback. After all 24 bits data is transferred, data line keeps low for

t_{EOS} (min. 2us) delay, and then it is pulled to static high. Shown as Figure 5.

If RFA=1, ACK signal feedback to master. After all 24 bits data is transferred, the data line keeps low for t_{ACKval} (max. 2us) time ,then data line should be released to output high impedance and master is ready to detect the ACK signal from slave . After t_{ACKval}, if ACK "false" (1-wire data is not received successfully), the data line will be pulled to high directly. After t_{ACKval}, if ACK "ture" (1-wire data is received successfully), data line will be continuously pulled to low V_{ACKL} (max. 0.4V) by slave for t_{ACK} (max. 512us) time. The master reads this low logic, it means chip received 1-wire data successfully. Then the data line is pulled to static high. Shown as Figure 6.

MP3312 has a 9-bit DAC for digital dimming control and the dimming resolution is 1/511. The default code value of D0 (LSB)-D8(MSB) is "111111111" when the device is first enabled. The LED current is dependent on the internal register value D0-D8 according to below formula:

$$ILED = ILED_{full} \times \frac{code}{511}$$

$ILED_{full}$ is the full scale output current set by R_{ISET} to ISET pin. Code is the DEC value of resolution bit (D0-D8).

Cycle-by-Cycle Current Limit Protection

MP3312 provides cycle-by-cycle current limit protection to avoid any damage due to too large current rating. During startup, the current limit is clamped to 1A for around 6ms to avoid output overshoot and inrush current. After that, the current limit returns back to normal 1.8A.

Open String Protection

Open string protection is achieved by detecting the VOUT pin. If the LED string is open, the feedback voltage is lower than the reference voltage, thus the COMP rises up and keeps charge the output capacitor until VOUT pin hits the protection point VOVP. Then the IC stops switching and shuts down till VIN and EN is reset for enable again.

Unused LED Channel

In some cases, if one LED current channel is not used, connect the corresponding LEDx to GND to remove it from the control loop.

Short String Protection

The MP3312 monitors the LEDX pin voltage to judge if the short string occurs. If one string is short, the respective LEDX pin will be pulled up to the boost output and tolerate high voltage stress. If the LEDX pin voltage is higher than 5 V and LED current is larger than 8% full-scale setting current, the short string condition is detected and if such condition lasts longer than 8ms, the fault string current source is disabled till VIN and EN is reset for enable again.

Thermal Shutdown Protection

To prevent the IC operate at exceedingly high temperature, thermal shutdown is implemented in this chip by detecting the silicon die temperature. When the die temperature exceeds the upper threshold 150℃, the IC shutdowns and recovers to normal operation when die temperature drops below lower threshold. Typically, the hysteresis value is 25°C.

APPLICATION INFORMATION

Setting the LED Current

The full scale LED current can be set through the current setting resistor on the FB pin.

$$ILED(mA) = \frac{V_{ISET}(V)}{R_{ISET}(k\Omega)} * 1020$$

For V_{ISET}=1.232V, R_{ISET}=63.4kΩ, the LED current is set to 20mA. Please do not leave ISET pin open.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be much less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. For most applications, a 1uF~4.7μF ceramic capacitor is ok.

Selecting the Inductor

The MP3312 requires an inductor to supply a higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current, resulting in lower peak inductor current and reducing stress on the internal N-channel MOSFET. However, the larger value inductor has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode with high efficiency and good EMI performance.
Calculate the required inductance value using the equation:

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

Where V_{IN} and V_{OUT} are the input and output voltages, f_{SW} is the switching frequency, I_{LOAD} is the total LED load current, and η is the efficiency. The switching current is used for the peak current mode control. In order to avoid hitting the current limit, the worst-case inductor peak current should be less than 80% of the current-limit I_{LIM}. Generally, a 4.7uH~10uH inductor is ok to cover most of the applications. Note that the system efficiency is dependent on the DC resistance of inductor, and larger DC resistance causes larger power loss.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. Care must be taken that ceramic capacitance is also dependent on the voltage rating; DC bias voltage and the value can loss as much as 50% of its capacitance at its rated voltage rating. Please leave enough voltage rating margin when select the component. In addition, too low capacitance will cause the loop instability. For most applications, a 1μF~4.7μF ceramic capacitor is ok.

Selecting the External Schottky Diode

To optimize the efficiency, a high-speed and low reverse recovery current schottky diode is recommended. Make sure the diode's average and peak current rating exceeds the output average LED current and the peak inductor current. In addition, the diode's break-down voltage rating should be large than the maximum voltage across the diode. Usually, unexpected high frequency spike voltage can be seen across the diode when the diode turns off. So, leaving some voltage rating margin is always needed to guarantee normal long term operation when selecting a diode.

Layout Considerations

Careful attention must be paid to the PCB board layout and components placement. Proper layout of the high frequency switching path is critical to prevent noise and electromagnetic interference problems. The loop of MP3312's internal low side MOSFET, schottky diode, and output capacitor is flowing with high frequency ripple current, it must be minimized. So the input and output capacitor should be placed to IC as close as possible.

TYPICAL APPLICATION CIRCUITS

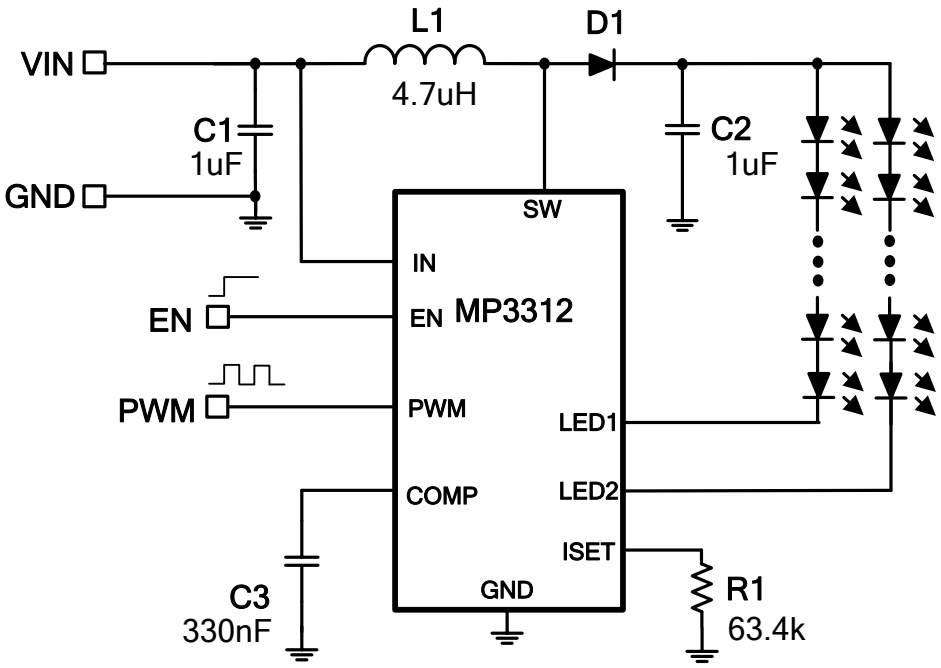
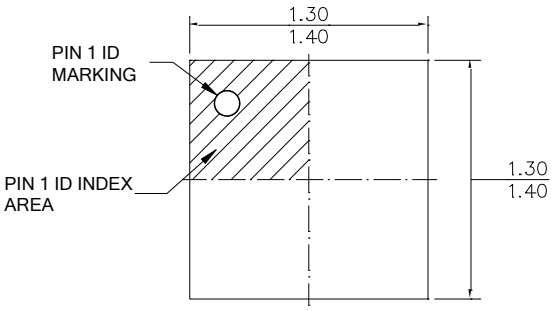


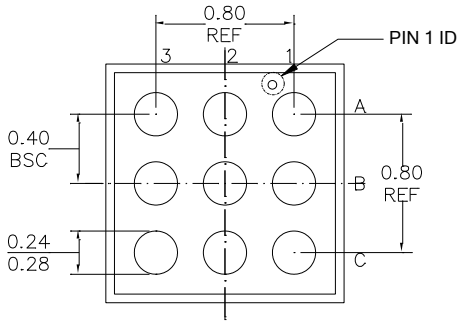
Figure 7— Typical Application for dual string 6LEDs, 20mA/string

PACKAGE INFORMATION

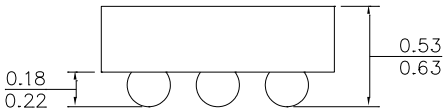
WLCSP1.35X1.35-9



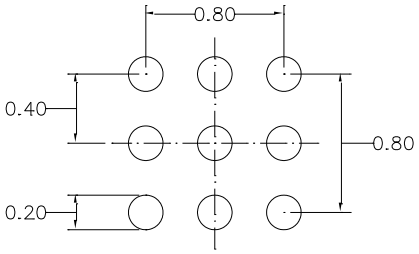
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211, VARIATION BC.
4) DRAWING IS NOT TO SCALE.

Revision History

Revision #	Revision date	Description	Pages Updated
1.1	12/7/2020	add the explanation on the failure issue of 1-wire communication	11