MP2927

Triple-Loop, Digital, Multi-Phase Controller with PMBus Interface for AVSBus

DESCRIPTION

The MP2927 is a triple-loop, digital, multi-phase controller that provides power for the memory and system-on-chip (SoC). The MP2927 can work with MPS's Intelli-Phase™ products to complete the multi-phase voltage regulator (VR) solution with a minimal number of external components. The MP2927 can be configured for up to 8-phase operation on rail 1, 1-phase operation on rail 2, and 1-phase operation on rail 3.

The MP2927 provides an on-chip non-volatile memory (NVM) to store and restore device configurations. Device configurations and fault parameters can be easily configured or monitored via the PMBus/I²C interface. The device can monitor and report the output current (I_{OUT}) through the current-sense (CS) output from Intelli-Phase™ devices.

The MP2927 is based on unique, digital, multi-phase control to provide fast transient response to the load transient with minimal output capacitors. With only one power loop control method for both steady state and load transient response, the power loop compensation is simple to configure.

The MP2927 is available in a TQFN-40 (5mmx5mm) package.

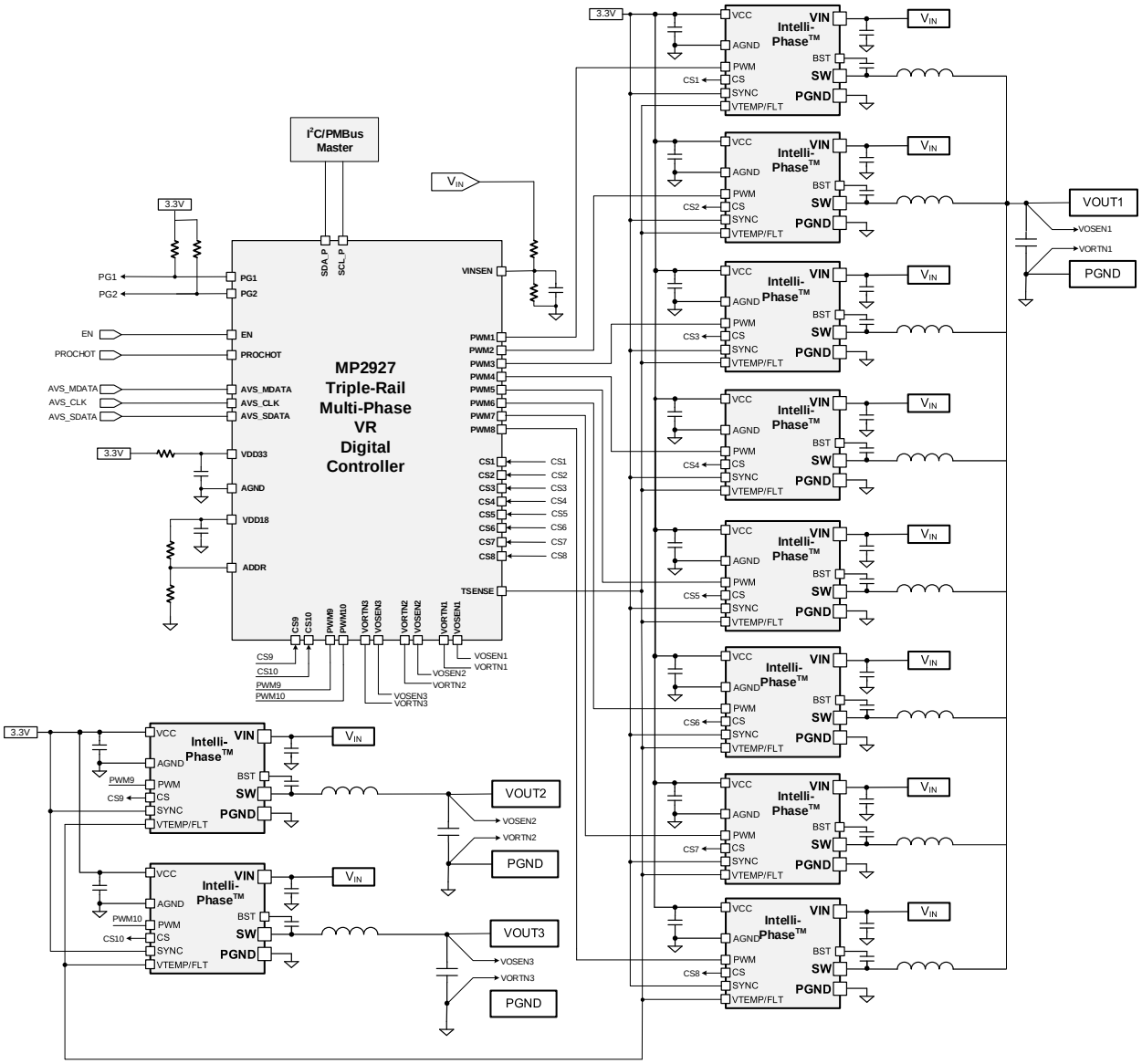
FEATURES

- Multi-Phase, Triple-Output, Digital Controller
- PMBus/I²C-Compliant (1MHz Bus Speed)
- AVSBus Mode Available
- Built-In Non-Volatile Memory (NVM) to Store Custom Configurations
- 200kHz to 3MHz Switching Frequency (f_{SW}) Range
- Coupled Inductor Mode for Rail 1
- Automatic Loop Compensation
- Fewer External Components than a Conventional Analog Controller
- Best Transient Performance with Digital Control
- Flexible Phase Assignment for Triple Rails
- Automatic Phase-Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current-Balancing with Configurable Offsets for Thermal Balance
- Input and Output Voltage, Current, and Power Monitoring
- Regulator Temperature Monitoring
- V_{IN} UVLO, Output OVP/UVP, OCP, OTP with No Action, Latch, or Hiccup Options
- Intelli-Phase™ Fault Diagnosis
- Auto-Records the VR Fault Type to the NVM
- Digital Load-Line Regulation
- Overclocking Mode by Adding an Offset to the Output Voltage (V_{OUT})
- Available in a TQFN-40 (5mmx5mm) Package

APPLICATIONS

- SoC Power
- DDR Memory Power
- Telecom and Networking Systems
- Base Stations

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2927GUT-xxxx**	TQFN-40 (5mmx5mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MP2927GUT-xxxx-Z).

** "xxxx" is the configuration code identifier for the register settings stored in NVM. Each "x" can be a hexadecimal value between 0 & F. Work with an MPS FAE to create this unique number.

TOP MARKING

MPSYYWW

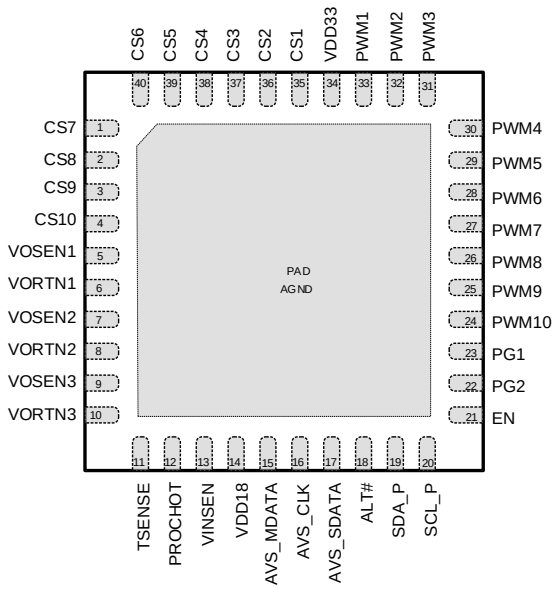
MP2927

LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2927: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



TQFN-40 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Type	Description
1	CS7	A [I]	**Phase 7 current-sense input.**
2	CS8	A [I]	**Phase 8 current-sense input.**
3	CS9	A [I]	**Phase 9 current-sense input.**
4	CS10	A [I]	**Phase 10 current sense input.**
5	VOSEN1	A [I]	**Positive remote voltage-sense input.** VOSEN1 is connected directly to the voltage regulator (VR) output voltage (V_{OUT}) at the load. VOSEN1 should be routed differentially with VORTN1.
6	VORTN1	A [I]	**Remote voltage-sense return input.** VORTN1 is connected directly to ground at the load. VORTN1 should be routed differentially with VOSEN1.
7	VOSEN2	A [I]	**Positive remote voltage-sense input.** VOSEN2 is connected directly to the VR V_{OUT} at the load. VOSEN2 should be routed differentially with VORTN2.
8	VORTN2	A [I]	**Remote voltage-sense return input.** VORTN2 is connected directly to ground at the load. VORTN2 should be routed differentially with VOSEN2.
9	VOSEN3	A [I]	**Positive remote voltage-sense input.** VOSEN3 is connected directly to the VR V_{OUT} at the load. VOSEN3 should be routed differentially with VORTN3.
10	VORTN3	A [I]	**Remote voltage-sense return input.** VORTN3 is connected directly to ground at the load. VORTN3 should be routed differentially with VOSEN3.
11	TSENSE	A [I]	**Temperature-sense input.** TSENSE can be configured to protect rails 1, 2, and 3. It can also be used for general-purpose analog voltage sensing, and includes optional fault detection.
12	PROCHOT	D [I]	**Digital input to indicate a processor hot event.**
13	VINSEN	A [I]	**Input voltage sense.** Connect VINSEN to a 1/16 divider from the input voltage (V_{IN}).
14	VDD18	Power	**1.8V LDO output.** VDD18 provides a power supply for the internal digital circuit. Connect a 1µF bypass capacitor to AGND.
15	AVS_MDATA	D [I]	**Data line from the SoC/CPU (AVSBus communication).**
16	AVS_CLK	D [I/O]	**Clock from the SoC/CPU (AVSBus communication).**
17	AVS_SDATA	D [I/O]	**Data line from the MP2927 to the SoC/CPU (AVSBus communication).**
18	ALT_P#	D [O]	**Open-drain output that asserts low when a warning has occurred.**
19	SDA_P	D [I/O]	**PMBus/I^{2}C data pin.**
20	SCL_P	D [I]	**PMBus/I^{2}C clock pin.**
21	EN	D[I]	**Enable pin for the controller.**
22	PG2	D[I/O]	**Power good (PG) output 2.**
23	PG1	D[I/O]	**Power good (PG) output 1.**
24	PWM10	D [O]	**Tri-state logic-level PWM output for phase 1 on rail 3.** Each output is connected to the PWM input of the Intelli-Phase™.
25	PWM9	D[O]	**Tri-state logic-level PWM output for phase 1 on rail 2.** Each output is connected to the PWM input of the Intelli-Phase™.
26	PWM8	D [O]	**Tri-state logic-level PWM output for phase 8 on rail 1.** Each output is connected to the PWM input of the Intelli-Phase™.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
27	PWM7	D [O]	**Tri-state logic-level PWM output for phase 7 on rail 1.** Each output is connected to the PWM input of the Intelli-Phase™.
28	PWM6	D [O]	**Tri-state logic-level PWM output for phase 6 on rail 1.** Each output is connected to the PWM input of the Intelli-Phase™.
29	PWM5	D [O]	**Tri-state logic-level PWM output for phase 5 on rail 1.** Each output is connected to the PWM input of the Intelli-Phase™.
30	PWM4	D [O]	**Tri-state logic-level PWM output for phase 4 on rail 1.** Each output is connected to the PWM input of the Intelli-Phase™.
31	PWM3	D [O]	**Tri-state logic-level PWM output for phase 3 on rail 1.** Each output is connected to the PWM input of the Intelli-Phase™.
32	PWM2	D [O]	**Tri-state logic-level PWM output for phase 2 on rail 1.** Each output is connected to the PWM input of the Intelli-Phase™.
33	PWM1	D [O]	**Tri-state logic-level PWM output for phase 1 on rail 1.** Each output is connected to the PWM input of the Intelli-Phase™.
34	VDD33	Power	**3.3V power supply input.** Connect a 1µF bypass capacitor from VDD33 to AGND.
35	CS1	A [I]	**Phase 1 current-sense input.**
36	CS2	A [I]	**Phase 2 current-sense input.**
37	CS3	A [I]	**Phase 4 current-sense input.**
38	CS4	A [I]	**Phase 4 current-sense input.**
39	CS5	A [I]	**Phase 5 current-sense input.**
40	CS6	A [I]	**Phase 6 current-sense input.**
PAD	AGND	Power	**Analog ground.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD33 .....-0.3V to +4V
VDD18 .....-0.3V to +2.2V
VORTN1/2/3..... -0.3V to +0.3V
CS1/2/3/4/5/67/8/9/10, PWM1/2/3/4/5/6/7/8/9/10, VOSEN1/2/3, SCL_P, SDA_P, EN, TSENSE, PG1, PG2……
.....-0.3V to +4V
VINSEN, AVS_MDATA, AVS_SDATA, AVS_CLK,.....-0.3V to +2.2V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (2) 3.47W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (VDD33) .....3.15V to 3.45V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TQFN-40 (5mmx5mm) ..... 36 ..... 5.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 6-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Remote-Sense Amplifier (Rails 1/2/3)						
Bandwidth (5)	$GBW_{(RSA)}$			20		MHz
VORTN1/2/3 current	$I_{RTN1/2/3}$	EN = 3.3V, VOSEN1/2/3 = 3V, VORTN1/2/3 = 0V	-80	-40		µA
VOSEN1/2/3 current	$I_{VOSEN1/2/3}$	EN = 3.3V, VOSEN1/2/3 = 3V, VORTN1/2/3 = 0V		40	80	µA
System Interface Control Inputs						
EN						
Input low voltage	$VIL_{(EN)}$				0.8	V
Input high voltage	$VIH_{(EN)}$		2			V
Enable high leakage	$IIH_{(EN)}$	EN = 3.3V		3.3		µA
Enable delay (regular power mode) (5)		EN Hi to PWM switching ready		10		us
Enable delay (low-power mode) (5)		EN Hi to PWM switching ready		2		ms
PG1, PG2						
Output low voltage		Sink 4mA	0		0.2	V
Open-drain leakage current	I_{PGLKG}	V_{PG} = 3.3V			3	µA
Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP) Comparator (Rails 1/2/3)						
Relative under-voltage threshold (V_{VID_UV})	Range	Relative to the DAC reference voltage	-425		-75	mV
	Resolution/LSB	3-bit DAC		50		mV
Relative over-voltage threshold (V_{VID_OV})	Range	Relative to the DAC reference voltage	200		450	mV
	Resolution/LSB	2-bit DAC		125		mV

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Absolute over-voltage threshold (V_{OVP_ABS})	Range	Absolute under-voltage (UV) threshold	0.5		2.3	V
	Resolution/LSB	8-bit register		10		mV
CS Fault Comparator (Rails 1/2/3, CS1~10 Protection)						
CS fault threshold	V_{CS_TH}			160		mV
TSENSE Fault Comparator (Protection)						
TSENSE fault threshold	$V_{TH(VTEMP\_FLT)}$			2.2	2.4	V
PROCHOT Threshold Digital-to-Analog Converter (DAC)						
Maximum threshold			0.5		2.3	V
Resolution/LSB (5)	$\Delta_{DAC\_PROCHOT}$	6-bit DAC		40		mV
PWM Outputs (PWM1~10)						
Output low voltage	$V_{OL\ (PWM)}$	$I_{PWM(SINK)}$ = 400µA		10	200	mV
Output high voltage	$V_{OH\ (PWM)}$	$I_{PWM(SOURCE)}$ = -400µA	3.0	VDD33 - 0.02		V
Rise and fall time (5)		C = 10pF		10		ns
PWM tri-state leakage		PWM = 1.5V, EN = 0V	-1		+1	µA
PWM middle-state voltage				1.50		V
VDD33 Supply						
Supply voltage range	VDD33		3.15	3.3	3.45	V
Supply current	I_{VDD33}	EN = 0 or 1, configured for normal power mode		40	55	mA
		EN = 0, configured for low-power mode		150		µA
Under-voltage lockout (UVLO) threshold voltage		VDD33 is rising		2.85	2.99	V
UVLO threshold voltage		VDD33 is falling	2.6	2.75		V
UVLO hysteresis		VDD33 is falling		130		mV
1.8V Regulator						
1.8V regulator output voltage	VDD18	I_{VDD18} = 0mA, T_J = 25°C	1.782	1.8	1.818	V
1.8V load regulation		VDD18 sources 30mA		VDD18 - 0.04		V
Analog-to-Digital Converter (ADC) (General, VIMON Dedicated, Rails 1/2/3)						
ADC reference voltage		T_J = 25°C	1.592	1.600	1.608	V
Resolution/LSB		10-bit ADC		1.5625		mV
DNL (5)		T_J = 25°C		1		LSB
Sample rate (5)				780		kHz

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VID DAC (Reference Voltage for Rails 1/2/3)						
DAC reference voltage		T_J = 25°C	1.592	1.6	1.608	V
Maximum voltage (5)				1.55		V
Resolution/LSB	Δ_{DAC}	10-bit ADC		1.5625		mV
Maximum V_{OUT} slew rate (5)				50		mV/µs
VOUT DC Loop DAC (V_{OUT} Calibration for Rails 1/2/3) (5)						
Range				240		mV
Resolution/LSB	Δ_{DAC}			0.9375		mV
OCP-SPIKE DAC (Rails 1/2/3, OCP_SPIKE Protection)						
Range		Adjustable via the PMBus	0.3		1.5	V
Resolution/LSB (5)	Δ_{DAC_OC}	8-bit DAC		6.25		mV
OCP-Phase DAC (Rails 1/2/3, OCP-Phase Protection)						
Range		Adjustable via the PMBus	1.35		2.35	V
Resolution/LSB (5)		8-bit DAC		5		mV
OVP-ABS DAC (Rails 1/2/3, Absolute OV Protection)						
Range	FS_{DAC_OVP}	Adjustable via the PMBus	0.5		2.3	V
Resolution/LSB (5)	Δ_{DAC_OVP}	8-bit DAC		10		mV
PMBus DC Characteristics (SDA_P, SCL_P)						
Input high voltage	V_{IH}	SCL_P, SDA_P for VBUS = 3.3V, Page 2, 2Dh = 0x0D53	2.2			V
		SCL_P, SDA_P for VBUS = 1.8V, Page 2, 2Dh = 0x0D53 (5)	1.26			V
Input low voltage	V_{IL}	SCL_P, SDA_P for VBUS = 3.3V, Page 2, 2Dh = 0x0D53			0.7	V
		SCL_P, SDA_P for VBUS = 1.8V, Page 2, 2Dh = 0x0D53 (5)			0.4	V
Input leakage current		SCL_P, SDA_P	-10		+10	µA
Output low voltage	V_{OL}	SDA_P sinks 2mA			400	mV
Maximum voltage (5)	V_{MAX}	Transient voltage (including ringing)	-0.3	3.3	+3.6	V
Pin capacitance (5)	C_{PIN}				10	pF
PMBus Timing Characteristics (1MHz) (5) (6)						
Operating frequency range			10		1000	kHz

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Bus free time		Between stop and start condition	0.5			µs
Holding time			0.26			µs
Repeated start condition set-up time			0.26			µs
Stop condition set-up time			0.26			µs
Data hold time			0			ns
Data set-up time			50			ns
Clock low timeout			25		35	ms
Clock low period			0.5			µs
Clock high period			0.26		50	µs
Clock/data falling time					120	ns
Clock/data rising time					120	ns
AVSBus Interface						
AVS_CLK, AVS_MDATA	V_{IL}	Logic low, Page 2, 2Eh = 0x378A			0.33	V
	V_{IH}	Logic high, Page 2, 2Eh = 0x378A	1.32			V
	V_{HYST}	Hysteresis		50		mV
Leakage current (AVS_CLK, AVS_MDATA, AVS_SDATA)	I_L	0V to 1.8V	-10		+10	µA
Pin capacitance (AVS_CLK, AVS_MDATA, AVS_SDATA) (5)	C_{PIN}				5	pF
Buffer on resistance (AVS_SDATA)	R_{ON}			14		Ω
Maximum voltage (AVS_CLK, AVS_MDATA, AVS_SDATA) (5)	V_{MAX}	Transient voltage (including ringing)	-0.3		+2.1	V
Slew rate (5) (AVS_CLK, AVS_MDATA, AVS_SDATA)		2nH, 10pF load	0.5		2	V/ns
VR clock to data delay (5)			4		8.3	ns
Set-up time (5)				7		ns
Hold time (5)				14		ns

Notice:

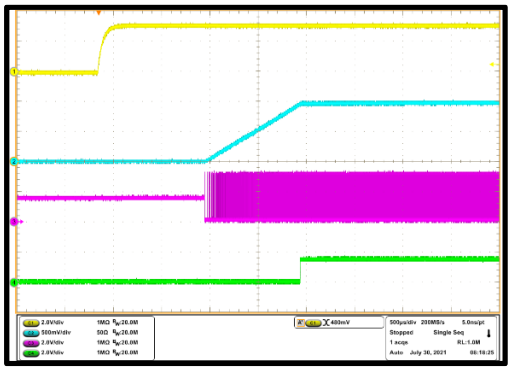
5) Guaranteed by design or characterization data. Not tested in production.
6) The device supports 100kHz, 400kHz, and 1MHz bus speeds. The PMBus timing parameters in this table are for operation at 1MHz. If the PMBus operating frequency is 100kHz or 400kHz, refer to the SMBus specification for timing parameters.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = V_{OUT3} = 1V, f_{SW1} = f_{SW2} = f_{SW3} = 800kHz, VDD33 = 3.3V, 8 + 1 + 1 phase mode, T_A = 25°C, unless otherwise noted.

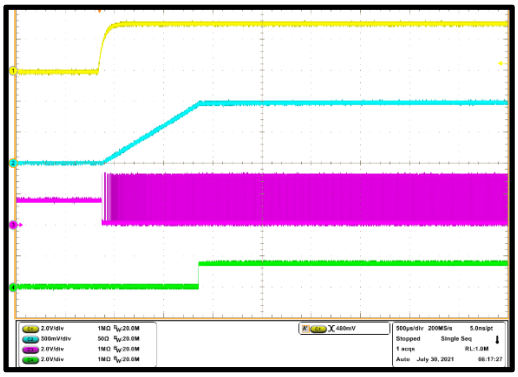
Rail 1 Enable On

Low-power mode, t_{ON} delay = 0



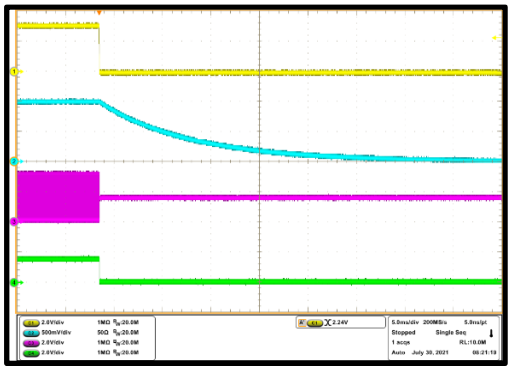
Rail 1 Enable On

Regular power mode, t_{ON} delay = 0



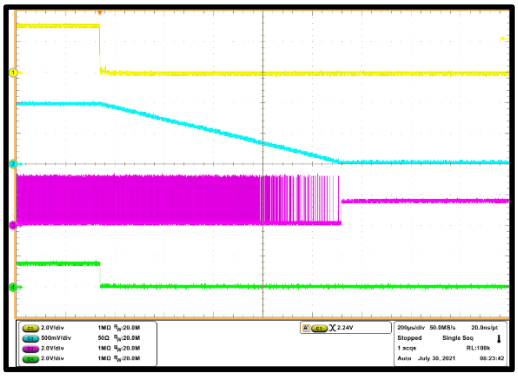
Rail1 Enable Off

Hi-Z off

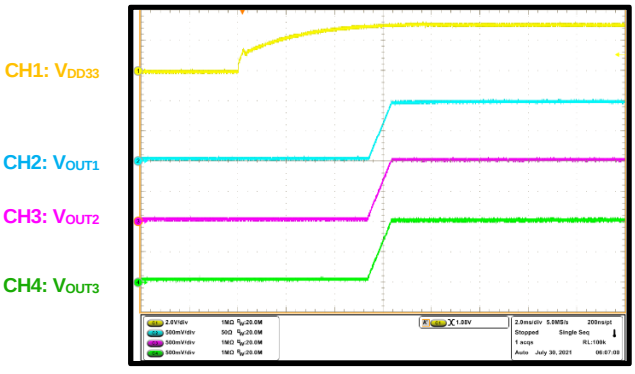


Rail1 Enable Off

Soft shutdown with 1mV/µs

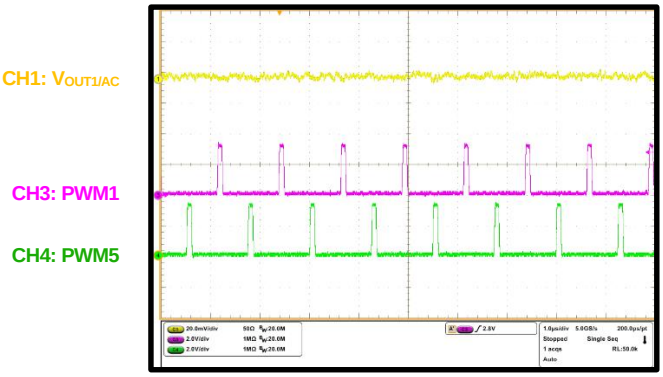


VDD33 On



Steady State

8-phase CCM, I_{OUT1} = 0A

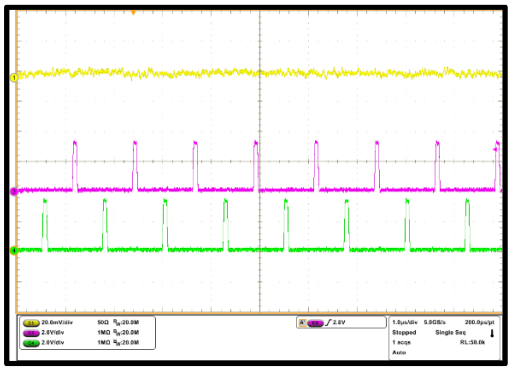


TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = V_{OUT3} = 1V, f_{SW1} = f_{SW2} = f_{SW3} = 800kHz, VDD33 = 3.3V, 8 + 1 + 1 phase mode, T_A = 25°C, unless otherwise noted.

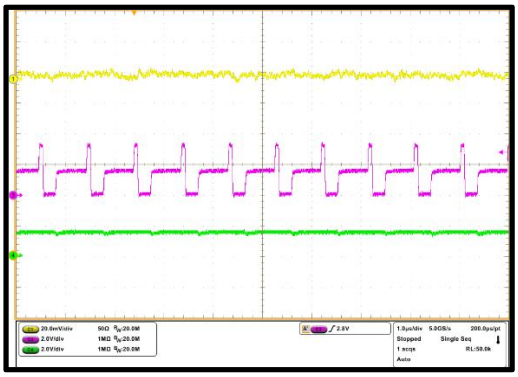
Steady State

8-phase CCM, I_{OUT1} = 120A



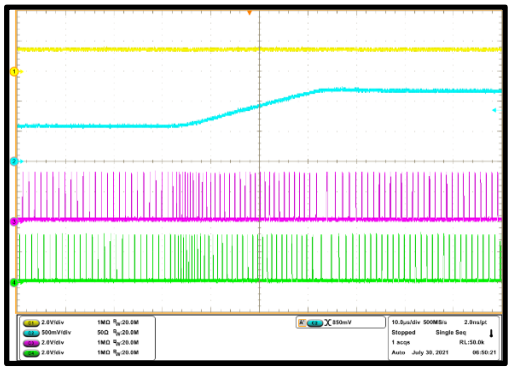
Steady State

1-phase DCM, I_{OUT1} = 2A



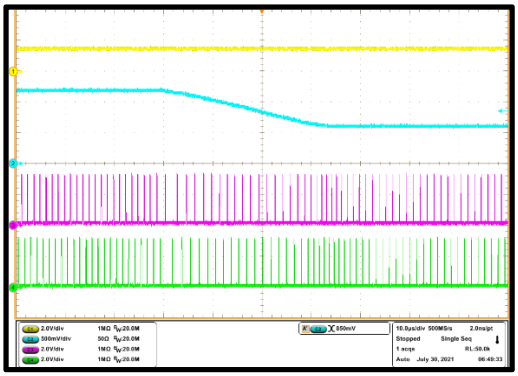
DVID Up

DVID from 0.6V to 1.2V, SR = 20mV/µs



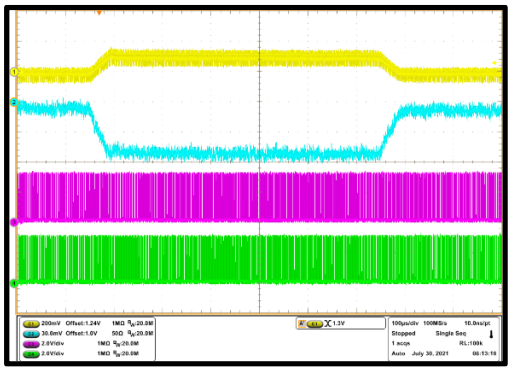
DVID Down

DVID from 1.2V to 0.6V, SR = 20mV/µs



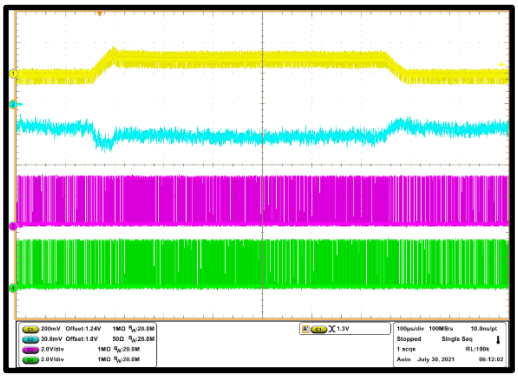
Load Transient with DC Load Line

R_{LL} = 0.4Ω, 0A to 100A at 5A/µs



Load Transient with AC Load Line

R_{LL} = 0Ω, 0A to 100A at 5A/µs

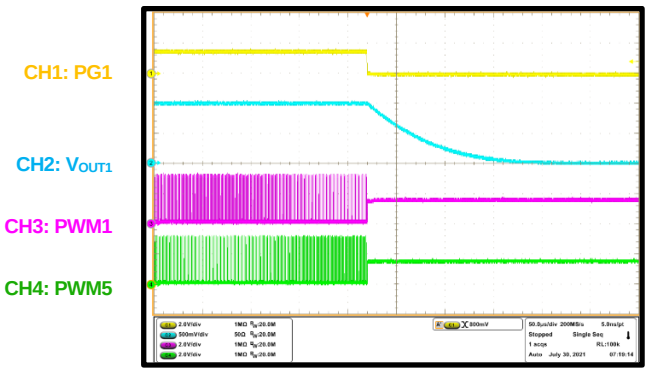


TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = V_{OUT3} = 1V, f_{SW1} = f_{SW2} = f_{SW3} = 800kHz, VDD33 = 3.3V, 8 + 1 + 1 phase mode, T_A = 25°C, unless otherwise noted.

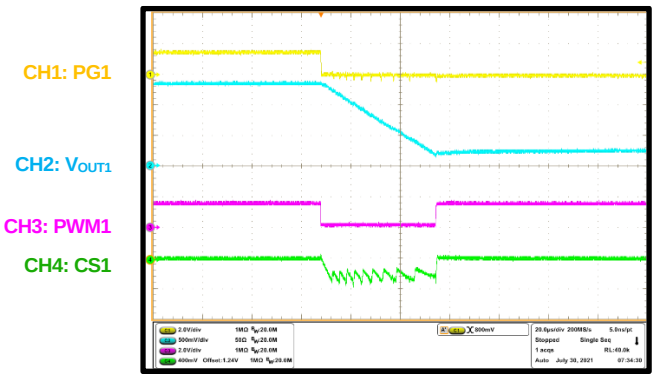
OCP

OCP_TDC = 120A, latch-off mode,
OCP_TDC action delay = 18µs



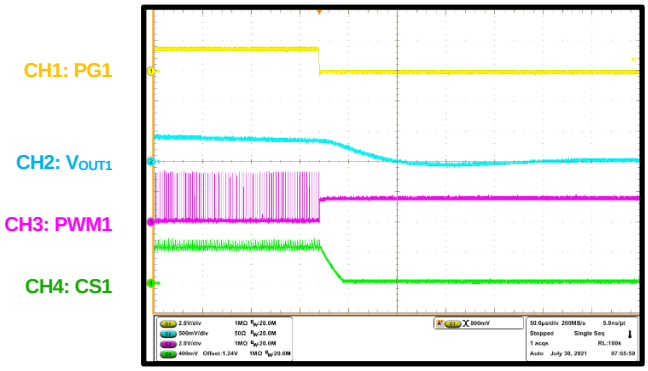
OVP

OVP VID delay = 0.5µs, latch-off mode



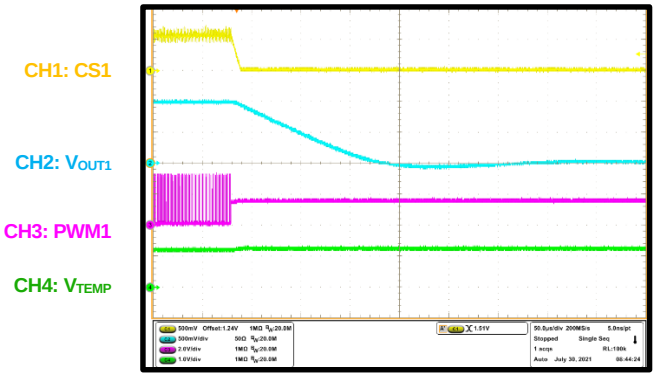
UVP

UVP delay = 500µs, latch-off mode



OTP

T_J = 100°C x V_{TEMP} + 10°C, latch-off mode,
OTP threshold = 130°C



FUNCTIONAL BLOCK DIAGRAM

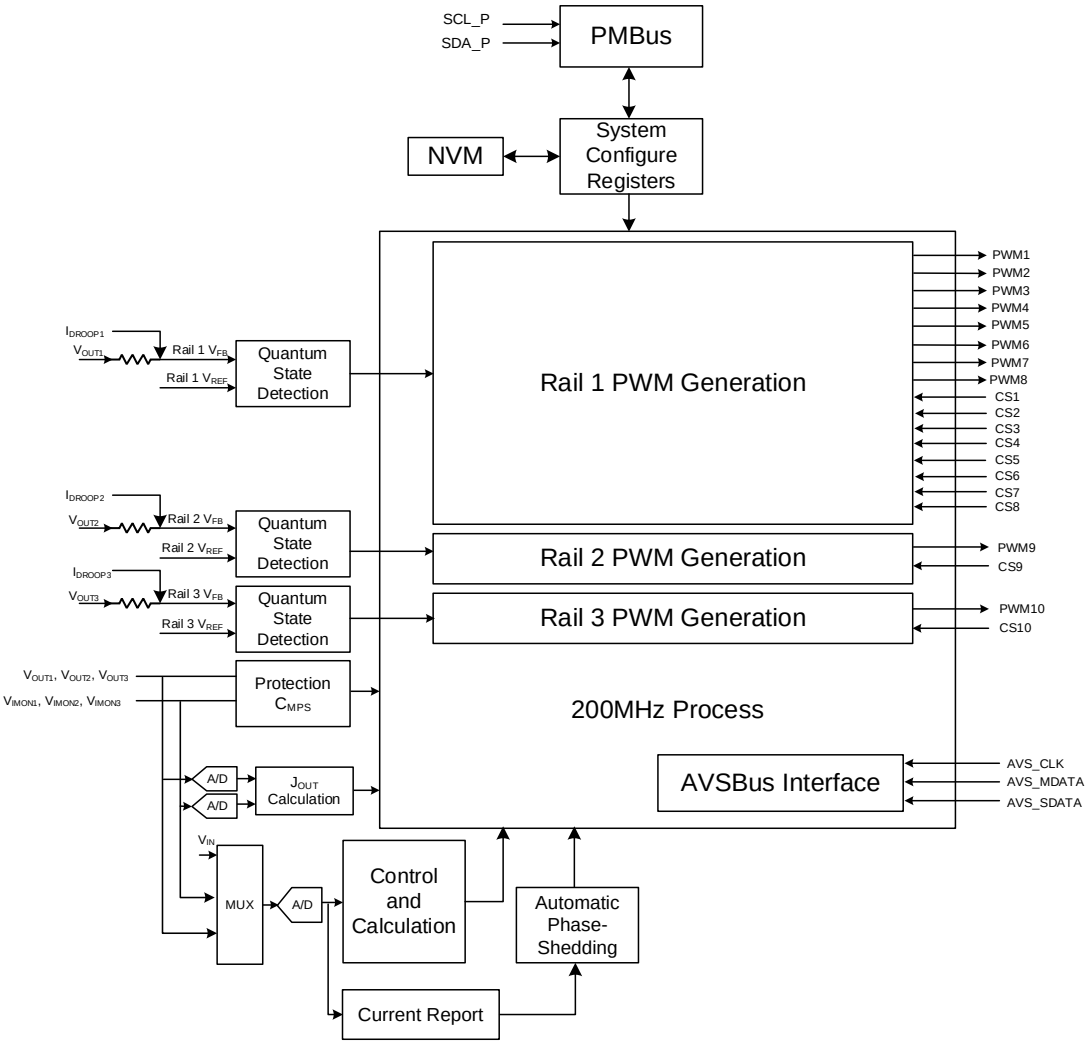


Figure 1: System Functional Block Diagram

OPERATION

The MP2927 is a triple-output, digital, multi-phase voltage regulator (VR) controller for general-purpose, multi-phase VRs. The device can implement adaptive phase-shedding and phase-adding according to the load current to improve overall VR efficiency. The MP2927 contains a precision digital-to-analog converter (DAC) and analog-to-digital converter (ADC), a differential remote voltage-sense amplifier, fast comparators, current sense, internal slope compensation, digital load-line setting, PGOOD monitoring, temperature monitoring, a PMBus/I^2C interface, an AVSBus interface, and a non-volatile memory (NVM) for custom configurations.

Fault protection features include input voltage (V_{IN}) under-voltage lockout (UVLO), over-current protection based on TDC (OCP_TDC), over-current protection based on ICCSPIKE/EDC/ICCMAX (OCP_SPIKE), cycle-by-cycle phase current limiting for over-current conditions (OVP_PHASE), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP). The MP2927 can detect the Intelli-Phase™ fault type if a protection occurs. The MP2927 automatically records all faults to the NVM in the event that the power supply shuts off when a fault occurs.

PWM Control and Switching Frequency

The MP2927 applies MPS's unique digital pulse-width modulation (PWM) control to provide fast load transient response and simple loop compensation. The switching frequency (f_{SW}) can be set with the related PMBus command FREQUENCY_SWITCH (33h).

The PWM on time (t_{ON}) of each phase updates in real time according to V_{IN}, the output voltage (V_{OUT}), and adaptive phase f_{SW}. t_{ON} can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

Where V_{OUT} is the real-time output voltage, V_{IN} is the input voltage, and f_{SW} is the switching frequency set by FREQUENCY_SWITCH (33h).

System Configuration

The MP2927 provides V_{IN} sense and differential V_{OUT} sense. It can work with Intelli-Phase™ (MPS's DrMOS) devices to sense the phase current, total load current, and the maximum temperature among the Intelli-Phase™ devices with a minimal number of external components. To achieve pre-biased functions, the MP2927's PWM outputs Hi-Z middle-state signals before outputting power to the load.

The PMBus slave address can be set up by the register via the PMBus.

The MP2927 provides a maximum of 8 rails for rail 1. The device can be configured for different phase number applications via the PMBus.

Any unused PWM enters tri-state. The active phase is interleaved automatically. Float any unused PWM and CS pins.

Non-Volatile Memory (NVM) Operation

The MP2927 uses non-volatile memory (NVM) to store application configuration parameters. The default values are preconfigured at the factory. The data can be configured again using the STORE_USER_ALL command (15h) via the PMBus.

Configurations are restored from the NVM during the power-on sequence, or if the device receives the RESTORE_USER_ALL command (16h) from the PMBus. Figure 2 on page 15 shows the MP2927 state machine.

The STORE_USER_CODE (17h) command can reconfigure the data, except for the trim registers. It is recommended to use STORE_USER_CODE (17h) to save the current configurations to the NVM. The RESTORE_USER_CODE (18h) command can load all data (except the trim registers) from the NVM to the operating memory.

NVM operation can be easily accomplished with MPS's GUI software. The NVM can be subjected to more than 1,000 erase/write cycles.

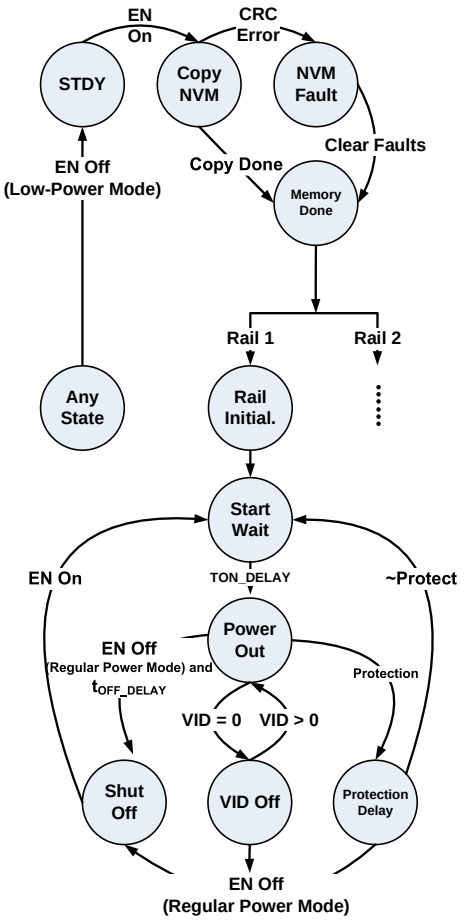


Figure 2: System State Machine

Power-On Configuration

The MP2927 is supplied by a 3.3V voltage. The internal low-dropout regulator (LDO) produces a 1.8V voltage for the digital circuit. The system is reset by the internal power-on reset (POR) signal. After the system exits POR, the data in the NVM is restored to the operating registers to initialize the VR operation. This restoration and initialization process takes about 1.1ms.

NVM Fault

If the data in the NVM is determined to be invalid by the cyclic redundancy check (CRC) during the system initialization process, then the system enters an NVM fault state without PWM switching. The MP2927 waits for the clear faults command, and the NVM configurations are ignored.

There are two ways to clear an NVM fault and reinitiate start-up with the default values in the register:

1. Clear the NVM fault via the PMBus.
2. Store the configurations to the NVM and restart the device.

Low Power Mode

The MP2927 can be configured to low-power mode or regular power mode.

In low-power mode, PMBus communication is disabled and the quiescent current (I_Q) drops to 150μA when EN goes low.

In regular power mode, PMBus communication is available when EN is low.

Wait State

After system initialization, the MP2927 begins the t_{ON} delay period and the soft start (SS) process. If any of the following conditions occur, the MP2927 enters the corresponding wait state:

1. A protection is triggered (such as if the sensed V_{IN} falls below the VIN_UVLO_ON threshold), or the sensed temperature exceeds the OTP threshold. The MP2927 enters the set protection mode (hiccup or retry mode) and waits for the fault to clear. Then the device enters the protection delay state for about 12.5ms before the next start-up/restart cycle.
2. The OPERATION off command is received via the PMBus. The MP2927 shuts down until it receives the on command from the PMBus master.
3. VID is commanded off. The MP2927 enters the VID off state, and there is no PWM output until the VID command exceeds the off level. The SS process begins immediately after exiting the VID off state.
4. EN turning off shuts down the MP2927.

Start-Up Sequence

The MP2927 is supplied by a 3.3V voltage at VDD33. VDD33 provides the biased supply for the analog circuit and internal 1.8V LDO. The 1.8V LDO supplies power to the digital circuit. The system is reset by the internal POR signal after the VDD33 supply is ready. After the system exits POR, the data in the NVM is loaded into the operating registers to configure the VR's operation.

Figure 3 shows the start-up sequence in regular power mode. Note that EN1, EN2, and EN3 can be interchangeably used for the start-up sequences of rail 1, rail 2, and rail 3.

t0 to t1: At t0, VDD33 is supplied by a 3.3V voltage. VDD33 reaches the UVLO threshold at t1. VDD18 reaches 1.8V when the VDD33 pin exceeds 1.8V.

t1 to t2: At t1, the data in the NVM starts loading into the operating registers. The entire NVM copying process takes about 1.5ms.

t2 to t3: At t2, the MP2927 waits for the EN pin to be pulled high once NVM copying is finished. The PMBus is available at this stage.

t3 to t4: After the EN pin pulls high, rail 1 stops and waits for an on command if the PMBus OPERATION (01h on Page 0) command is preset to off. If OPERATION is set to on, then the turn-on delay time (t_{ON} delay) starts counting. The delay time can be configured to be between 0ms and 6553.5ms via PMBus command TON_DELAY (60h on Page 0).

t4 to t5: When the t_{ON} delay expires, the rail VID DAC starts ramping up the reference voltage (V_{REF}) to the boot-up voltage with the configured slew rate. During SS, OCP_TDC, OVP, and UVP are masked until V_{REF} reaches the target value. The rail start-up sequence is complete at t5. Then the rail is ready to output power, and the start-up sequence for all rails is complete.

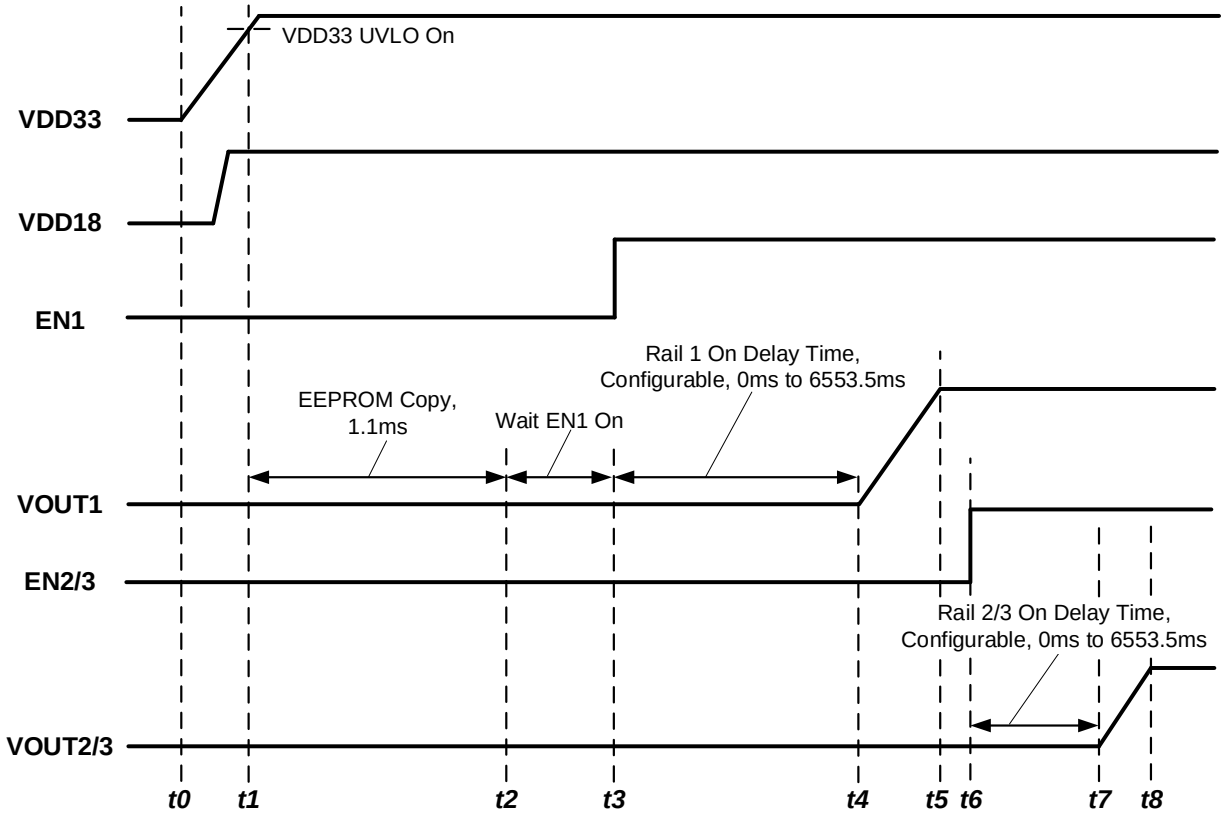


Figure 3: Start-Up Sequence in Regular Power Mode

Figure 4 on page 16 shows the start-up sequence in low-power mode. EN1, EN2, and EN3 can be exchanged. This means that the rails do not need to start up in a particular order.

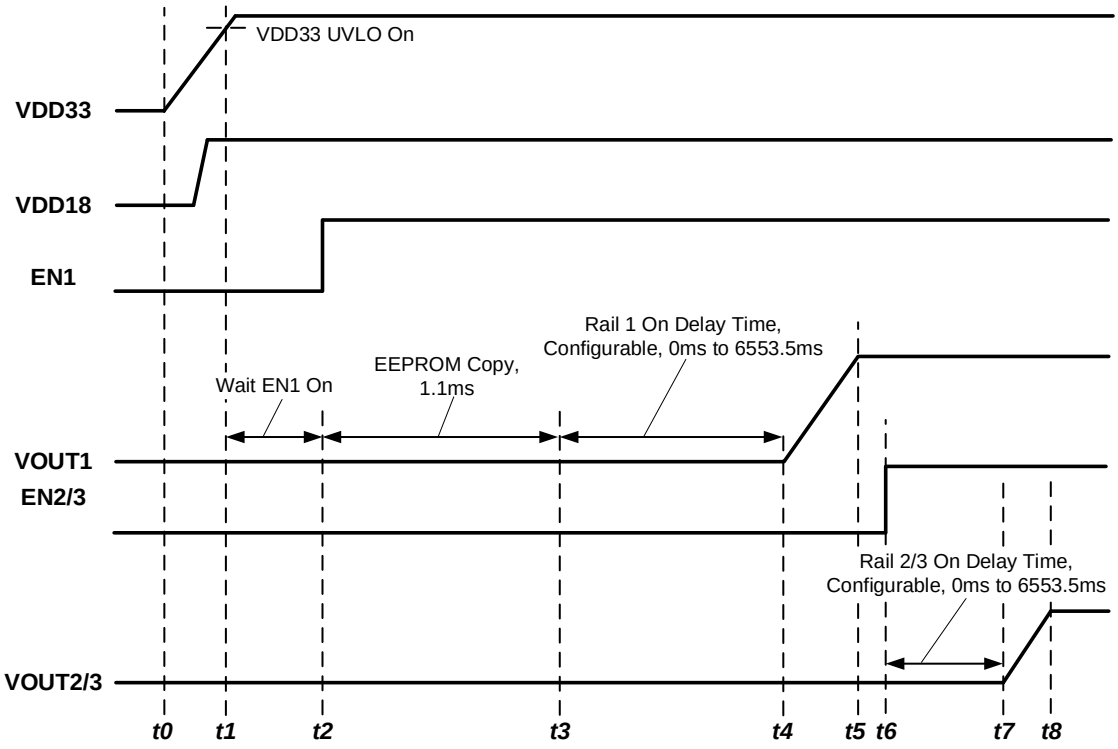


Figure 4: Start-Up Sequence in Low-Power Mode

Shutdown

The MP2927 can be shut down by VDD33 UVLO, the EN pin, the OPERATION command, or a protection. These shutdown methods are described below:

1. VDD33 shutdown: If the power supply on the VDD33 pin falls below the VDD33 UVLO falling threshold, the MP2927 shuts down immediately.
2. EN pin off: The MP2927 provides Hi-Z and soft shutdown with a selectable slew rate when the EN pin goes low in regular power mode. During soft shutdown, V_{OUT} ramps down with the selected slew rate until V_{REF} falls to the VID shutdown level set by register MFR_SD_VID (23h), bits[7:0]. Then all PWMs enter tri-state. A turn-off delay time can be added via register TOFF_DELAY (64h).

   If the EN pins go low in low-power mode, then the MP2927 initiates Hi-Z off immediately without a turn-off delay. The device enters standby mode with the smallest possible power consumption. The PMBus is unavailable until an EN pin is pulled high.
3. OPERATION command off: The MP2927 provides Hi-Z off and soft shutdown after receiving an OPERATION off command. When the OPERATION command is set to Hi-Z, all PWMs enter tri-state after an off command is received. Then V_{OUT} is discharged by the load current. When OPERATION commands a soft shutdown, V_{OUT} initiates the shutdown with the slow slew rate until V_{REF} reaches the VID shutdown level. Then all PWMs enter tri-state. A turn-off delay time can be added via register TOFF_DELAY (64h).
4. Protection shutdown: If V_{IN} OVP, V_{IN} UVLO, V_{OUT} UVP, OCP_SPIKE or OCP_TDC, OTP, a CS fault, or a VTEMP fault from the Intelli-Phase™ is triggered, then the VR enters Hi-Z off immediately.

   Once the V_{OUT} OVP threshold is triggered, the VR turns on all the active low-side MOSFETs (LS-FETs) to discharge C_{OUT}, then immediately shuts down until V_{OUT} falls below the reverse voltage protection (RVP) threshold (about 160mV).

Figure 6 shows the EN pin soft shutdown power sequence in regular power mode.

Figure 7 shows the EN pin Hi-Z off power sequence in low-power mode. When the EN pins are pulled low, the VR shuts down immediately with a t_{OFF} delay.

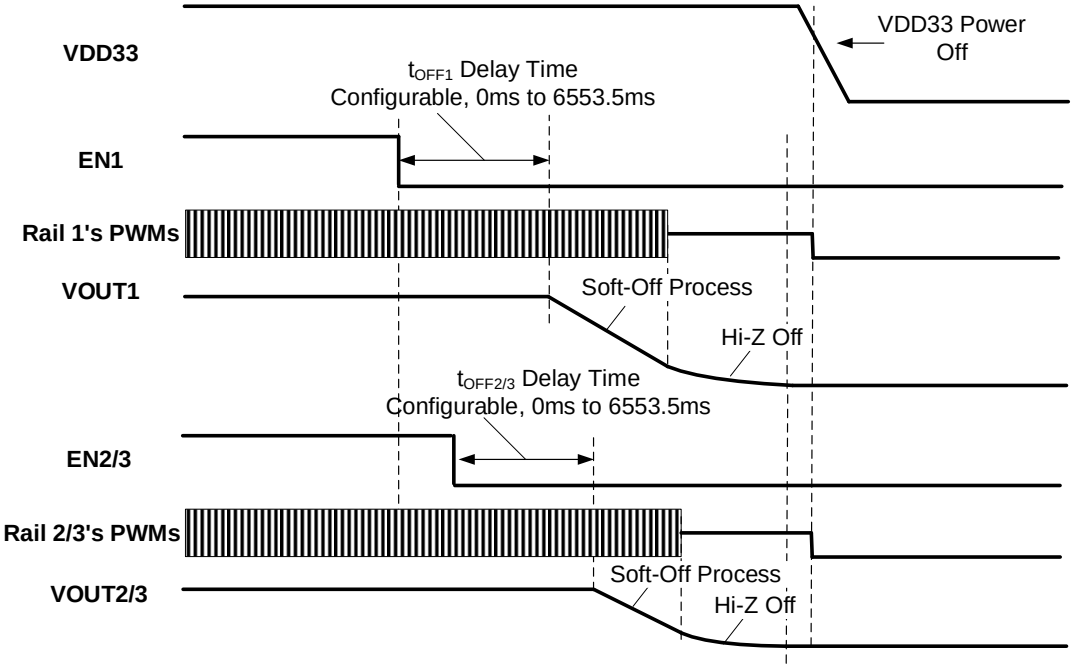


Figure 5: Shutdown Sequence in Regular Power Mode with Soft Shutdown

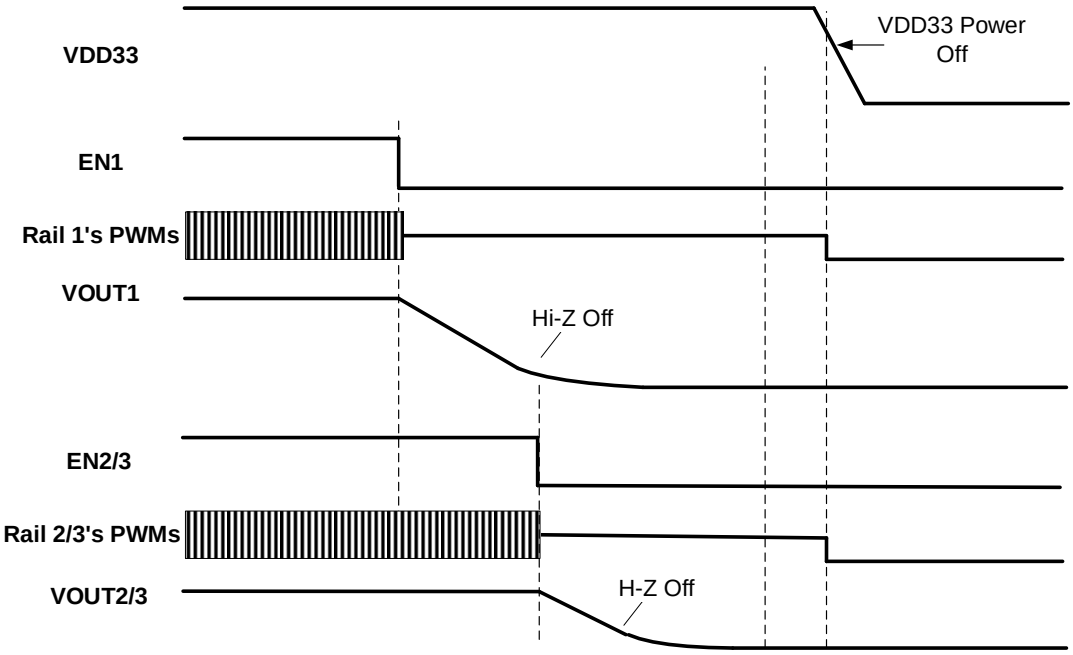


Figure 6: Shutdown Sequence in Low-Power Mode with Hi-Z Off

Power Good (PG) Indication

The MP2927 indicates power good (PG) with the PG1 and PG2 pins. These pins can be configured the following ways:

- PG1, PG2, and PG3
- PG1 and PG2
- PG1 and PG3
- PG2 and PG3

This function can be selected via GPIO_SEL_GROUP1 (66h on Page 0).

When V_{REF} reaches the VID value during soft start, the MP2927 starts the delay time counter and asserts PG when the delay time ends. The delay time can be configured via MFR_PG_DELAY (5Fh).

If the MP2927 is in Hi-Z off or soft shutdown due to a protection, OPERATION off command, or if an EN pin is pulled low, then the PG pins de-assert after a configurable delay time. This value can be configured via MFR_PG_DELAY (5Fh).

Figure 7 shows the PG indication process in regular power mode.

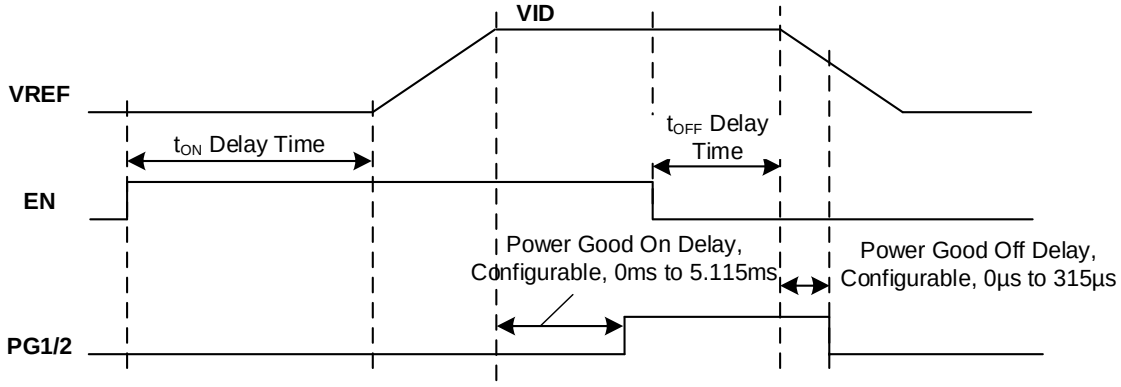


Figure 7: Shutdown On-/Off-Sequence in Regular Power Mode and EN Soft Shutdown

Voltage Reference

The MP2927 has three 8-bit VID DACs that provide the reference voltage (V_{REF}) for the individual output. V_{REF} is in VID format with 6.25mV per step, and ranges from 0V to 1.55V.

The MP2927 provides two different VID control modes: PMBus mode and AVSBus mode.

Output Voltage Setting and Sensing

The voltage at the load is sensed with a differential voltage-sense amplifier for each rail. This type of sensing improves load regulation. The sensed output voltages are used for loop compensation and V_{OUT} monitoring via the PMBus. With unity gain, V_{REF} is equal to VID, and the maximum VID voltage is limited to 1.55V, which is also the maximum VID DAC V_{OUT}.

With half-gain, V_{REF} is equal to half of the VID value, and the maximum VID voltage is 3V. Half-gain can be used to support overclocking applications or point-of-load (POL) applications with a V_{OUT} between 1.55V and 3V.

When V_{OUT} ≤ 3V, connect the remote-sense amplifier input pins (VOSEN and VORTN) directly to the output at the load.

When V_{OUT} > 3V, V_{OUT} must be divided to V_{REF} within 1.55V. Figure 8 shows the typical connections for an application where V_{OUT} > 3V and remote sensing is applied.

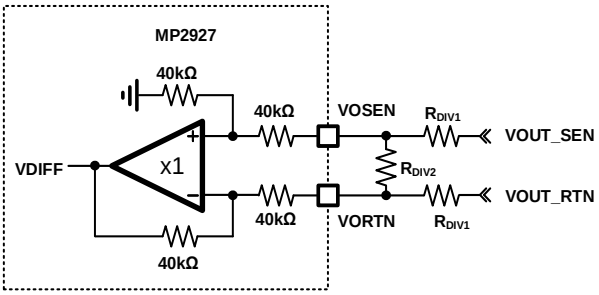


Figure 8: Output Divider Connections when Remote Sense is Applied

VOUT_SENP and VOUT_SENN are from the load, and must be routed as a differential pair on quiet areas.

Calculate the voltage divider ratio with Equation (2):

$$K_R = \frac{V_{OUT}}{V_{REF}} = \left(\frac{1}{R_{DIV1}} + \frac{2}{R_{DIV2}} + \frac{1}{40k\Omega} \right) \times R_{DIV1} \quad (2)$$

Where K_R can be configured via VOUT_SCALE_LOOP (29h).

VOUT_SCALE_LOOP can be estimated with Equation (3):

$$VOUT\_SCALE\_LOOP = 2^5 \times K_R \quad (3)$$

The controller uses this value to determine the reference voltage. V_{REF} can be calculated with Equation (4):

$$V_{REF} = \frac{2^5}{VOUT\_SCALE\_LOOP} \times V_{OUT} \quad (4)$$

Note that V_{REF} is in 6.25mV per step. Any value outside the step is ignored.

To minimize the V_{OUT} DC setting error, match the real output divider ratio from R_{DIV1} and R_{DIV2} to the ratio set by VOUT_SCALE_LOOP (29h). Design V_{REF} to be close to multiples of 6.25mV. See the VOUT_SCALE_LOOP (29h) section on page 40 for more details.

To prevent V_{OUT} from going out of regulation, ensure that the voltage on the VOSEN pin is below the maximum allowed sensing voltage (VDD33 - 0.3V) at any time.

Connect the output divider in a particular way if V_{OUT} exceeds the VOSEN pin's specification (see Figure 9). VORTN is directly connected to AGND to disable remote sensing.

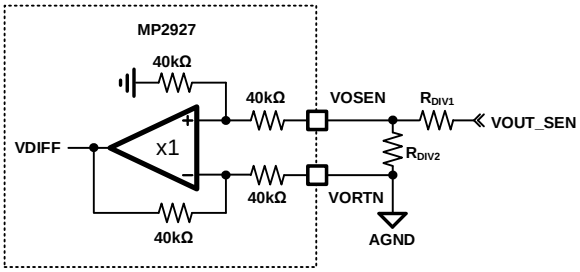


Figure 9: Output Divider Connections when Remote Sense is Not Applied

Use Equation (5) to calculate the voltage divider ratio in Figure 6:

$$K_R = \frac{V_{OUT}}{V_{REF}} = \left(\frac{1}{R_{DIV1}} + \frac{2}{R_{DIV2}} + \frac{1}{80k\Omega} \right) \times R_{DIV1} \quad (5)$$

Input Voltage Sense

The input power supply voltage is sampled at VINSEN and used for V_{OUT} regulation as the feed-forward control, V_{IN} UVLO and V_{IN} OVP fault protection, and V_{IN} monitoring via the PMBus.

An external resistor divider network is connected to VINSEN (see Figure 10). It is recommended to place a minimum 10nF filtering capacitor at VINSEN.

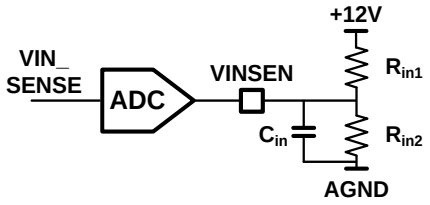


Figure 10: V_{IN} Sense Network

There is a register in the NVM to set the divider ratio of the V_{IN} divider network. This can be used to calculate V_{IN} for monitoring and protection.

Inductor Current Sense

The MP2927 works with MPS's Intelli-Phase™ to sense the phase inductor current (I_L) and the total current. The cycle-by-cycle current information is used for phase-current balancing, thermal balancing, over-current protection (OCP), and adaptive voltage positioning (V_{OUT} droop).

To enable current sensing, connect the MP2927's CSx pin directly to the Intelli-Phase™ CS pin. The MP2927's CSx pin can take either current or voltage information from the Intelli-Phase™ CS, which indicates the phase I_L. VCS_REF (typically 1.24V) can be connected to the Intelli-Phase™ to act as a CS reference voltage if required.

Total Current Sense

The total current is summed from each CS pin and converted into an IMON voltage via the internal resistors (see Figure 11 on page 21).

The IMON resistors of both rails are internal. The resistance and IMON current mirror gain are configurable (see Figure 13 on page 27). These combinations cover the I_{BASE} range, which is between 36.5A and 1167A (assuming that the current-sense gain = 8.5μA/A).

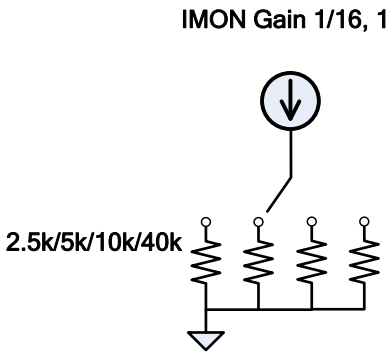


Figure 11: IMON Setting

If automatic phase-shedding (APS) is enabled via the PMBus, the total current report determines whether to enter or exit phase-shedding. This flattens the overall efficiency across the operating current range.

Intelli-Phase™ Temperature Sense

The MP2927 measures the temperature of the power stage by connecting all Intelli-Phase™ VTEMP pins together (see Figure 12). The voltage of the TSENSE pin indicates the highest junction temperature ($T_{JUNCTION}$) of all Intelli-Phase™ devices in the VR power system. The sensed temperature is used for over-temperature fault protection.

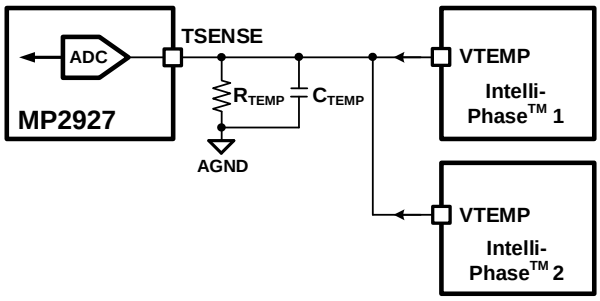


Figure 12: External Temperature Sense

The Intelli-Phases's™ V_{TEMP} is a voltage output proportional to $T_{JUNCTION}$. $T_{JUNCTION}$ can be calculated with Equation (6):

$$T_{JUNCTION}\ (°C)=a\times V_{TEMP}+b \qquad (6)$$

Where V_{TEMP} is the VTEMP voltage, *a* is the temperature gain, and *b* is the temperature offset.

Refer to the Intelli-Phase™ datasheet for details regarding the *a* and *b* values.

Die Temperature Sense

The MP2927 senses the die temperature. A thermal sensor converts the die temperature to a voltage (see Figure 13). This voltage is saved to DIE_TEMP_SENSE (D5h on Page 1). This register value can be read via the PMBus.

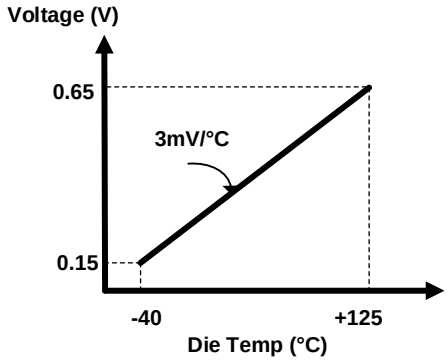


Figure 13: Die Temperature Sense

Dynamic Voltage Identification (DVID)

The MP2927 supports dynamic V_{OUT} transitions by changing the VID code via the PMBus interface and AVSBus interface.

In PMBus override control mode and AVSBus control mode, the DVID slew rate is set by VOUT_TRANSITION_RATE (27h) with 0.1mV/µs/LSB or 0.01mV/µs/LSB, which is determined by MFR_VR_CONFIG3 (C3h), bit[15]. The maximum slew rate is 60mV/µs.

The MP2927 applies an advanced digital control method to improve V_{OUT} performance while VID ramps up and down.

Ramping Up

When V_{OUT} is ramping up, I_L rises to charge the output capacitors. This current introduces a large, positive droop voltage, and lowers V_{OUT}.

When V_{REF} stops ramping, V_{OUT} may be below the minimum regulation tolerance budget (TOB). The MP2927 can automatically ramp up more VID steps than the target VID, then fall back to allow V_{OUT} to rise to the regulation TOB.

Ramping Down

When V_{OUT} ramps down, I_L decreases to discharge the output capacitors. The output capacitors continue to discharge when ramping ends, which may lead to V_{OUT} undershoot.

The MP2927 applies a low-pass filter for VID DAC to smooth out V_{REF} when V_{OUT} is ramping down.

Figure 14 shows V_{OUT} when VID ramps up after the previous VID finishes ramping downward.

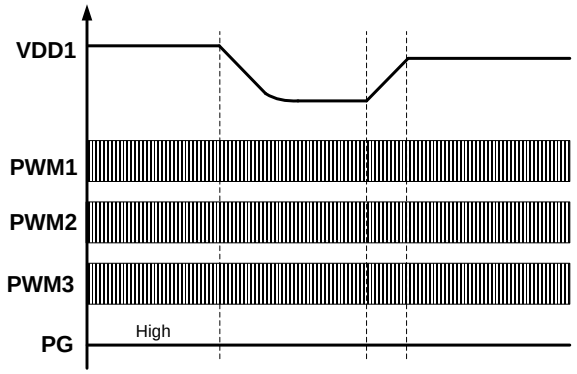


Figure 14: VID Ramping Down to VID Ramping Up

Automatic Phase-Shedding (APS)

The MP2927 provides APS to improve efficiency when there are no forced power state indicators. Figure 15 shows how the VR works in 2-phase CCM under heavy loads, or 1-phase CCM under light loads to optimize efficiency. The device enters 1-phase DCM under extremely light loads to further reduce switching loss.

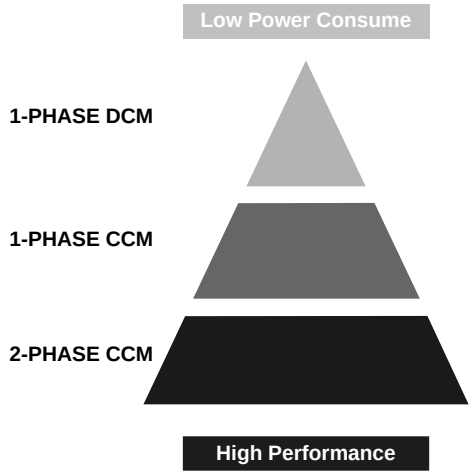


Figure 15: APS Function Diagram in 2-Phase Mode

APS is implemented by comparing the sensed load current with each power state's current threshold. The MP2927 provides two types of registers to configure APS functionality. All three rails use MFR_APS_LEVEL_12P (4Dh) to set the phase-shedding level. MFR_APS_CTRL2 (53h), bits[4:0] configure the hysteresis value to prevent the converter from changing power states under a steady load current. Figure 16 shows the APS current thresholds setting from 2-phase CCM to 1-phase CCM. See the MFR_APS_CTR2 (53h) section on page 57 and the MFR_APS_LEVEL12P (4Dh) section on page 54 for more details.

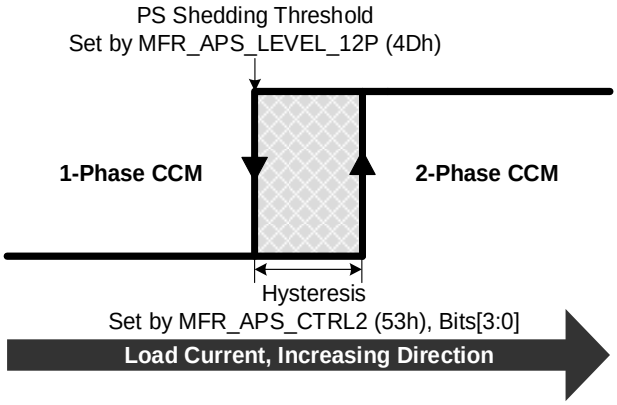


Figure 16: APS Threshold Setting

In addition to the sensed I_{OUT} comparison, the MP2927 provides three conditions that force the device to exit APS immediately and run with full-phase CCM, which accelerates the load transient response and reduces V_{OUT} undershoot:

1. The DVID process makes the controller run with full-phase CCM. After V_{OUT} settles to the target value, the new power state is determined by the load current.
2. Load step-up causes VFB- window tripping, which triggers full-phase CCM to reduce V_{OUT} undershoot.
3. Once the phase current exceeds the per-phase over-current limit, the MP2927 runs with the full-phase number.

Phase Current Balancing/Thermal Balancing

The phase current is sensed and calculated with the current reference in the current loop. Each zone's PWM on time is adjusted individually to balance the currents.

The MP2927 applies sigma-delta (Σ-Δ) modulation and delay line-loop (DLL) technology in the current balance modulation to increase the resolution of the current balance modulation and greatly reduce PWM jittering. The time resolution of the digital system is 5ns.

By applying Σ-Δ modulation and DLL technology, the digital PWM resolution can be increased to 0.08ns.

Each current balance loop can include a configurable phase current offset to achieve thermal balance between the phases. The phase with the greatest cooling capability is closest to the airflow, which allows it to take more phase current by increasing the phase current reference with the offset. This improves thermal balance between the phases. The bandwidth of the current proportional integral (PI) loop is relatively low compared to the V_{OUT} feedback loop, meaning it does not impact V_{OUT}.

Digital Load Line

The droop current mirror gains for all three rails can be configured to be 1/16, 1/8, 1/4, and 1/2.

The rail 1 internal droop resistors include sixty-four 25Ω resistors placed in series. The resistors can be configured to be between 25Ω and 1.6kΩ.

The rail 2 internal droop resistors include sixty-four 100Ω resistors placed in series. The resistors can be configured to be between 100Ω and 6.4kΩ.

The rail 3 internal droop resistors include sixty-four 100Ω resistors placed in series. The resistors can be configured to be between 100Ω and 6.4kΩ.

Figure 17 shows a set percentage of the current mirror gains.

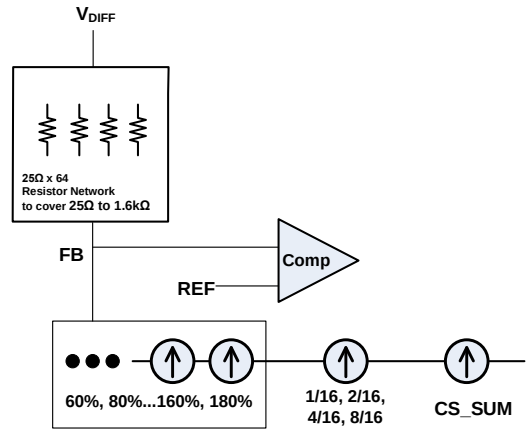


Figure 17: Digital Load Line for Rail One

Fault Monitoring and Protections

The MP2927 supports various fault monitoring and protections, described below.

V_{IN} Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)

If the sensed V_{IN} drops below the VIN_OFF threshold, the VR shuts off immediately by forcing PWM signals to tri-state. Once the sensed V_{IN} exceeds VIN_ON threshold, it restarts again. The V_{IN} UVLO threshold can be configured via registers VIN_ON (35h) and VIN_OFF (36h), with 31.25mV/LSB.

If V_{IN} exceeds the V_{IN} OVP threshold (set via VIN_OV_FAULT_LIMIT (55h)), then the VR shuts off. V_{IN} OVP can be set to either latch-off or auto-retry mode.

Over-Current Protection (OCP)

The OCP function applies to two OCP mechanisms, with two types of thresholds. IOUT_OC_FAULT_LIMIT (46h) bits[7:0]. If the sensed average I_{OUT} exceeds the OCP_TDC threshold for a preset time (the OCP_TDC blanking time), then OCP_TDC is triggered.

The second type is a current-only based threshold (OCP_SPIKE). The OCP_SPIKE threshold can be configured via PMBus command IOUT_OC_FAULT_LIMIT (46h), bits[15:8]. If the cycle-by-cycle total sensed average I_{OUT} exceeds the OCP_SPIKE threshold, then OCP_SPIKE is triggered.

If either mechanism is triggered on either rail, the MP2927 asserts OCP_L and delays any further action. This delay is called an action delay. If the current has not dropped below the threshold after the action delay has expired, then the MP2927 shuts down the VR to protect the power MOSFETs.

OCP_TDC and OCP_SPIKE can be configured to no action, hiccup, retry 6 times, or latch-off mode via the PMBus.

In no action mode, the controller takes no action and continues switching until other protections are tripped. If no action mode is selected, the fault indication bits in registers STATUS_IOUT (7Bh) and STATUS_WORD (79h) are not set.

In hiccup mode, the controller forces the PWM signals to tri-state to disable the output, and attempts to restart after a set protection delay time. This time can be configured via MFR_VR_CONFIG2 (C2h on Page 0), bits[14:13].

In retry 6 times mode, the VR restarts six times at most. If the fault is removed within these six restarts, then the VR resumes normal operation. If the fault remains, then the VR shuts down until a PMBus OPERATION on command is received, the power is cycled on VDD33, or EN is toggled.

In latch-off mode, the VR shuts down until a PMBus OPERATION off command is received followed by an on command, the power is cycled on VDD33, or EN is toggled.

The above four protection modes are available for OCP_TDC, OCP_SPIKE, V_{OUT} under-voltage protection (UVP), V_{OUT} over-voltage protection (OVP), VID OVP, and V_{OUT} absolute OVP.

In addition to the dual OCP mechanism described above, the MP2927 utilizes an extra current-based limitation protection called OCP_PHASE. The MP2927 monitors the phase current cycle by cycle. If the phase current exceeds the OCP_PHASE threshold during the PWM off time, the PWM remains low to discharge the inductor current below the set threshold.

If the present phase PWM on signal is blocked for more than 80ns, then the PWM on signal is skipped for this cycle and the next phase turns on to directly regulate V_{OUT}. Per-phase OCP typically works with UVP to protect the regulator. The OCP_PHASE threshold is PMBus-configurable via MFR_OCP_PHASE_LIMIT (49h).

Under-Voltage Protection (UVP)

The MP2927 provides UVP by monitoring V_{DIFF}.

If V_{DIFF} drops below the UVP threshold for a set time (known as the UVP blanking time), the controller forces the PWMs to tri-state to disable the output power (see Figure 18).

The VOUT_UV_FAULT_RESPONSE (45h) register determines the UVP mode. Similar to the OCP_TDC protection scheme, the UVP scheme also provides also provides no action, hiccup, retry 6 times, and latch-off options.

The UVP threshold can be configured with PMBus command VOUT_UV_FAULT_LIMIT (44h) (see page 50 for more details).

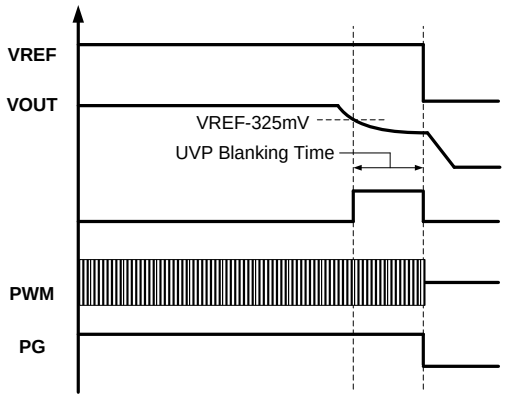


Figure 18: Under-Voltage Protection

UVP is typically triggered when the per-phase OCP current limit is reached, and the PWM signals are blocked by the per-phase OC signals (see Figure 19).

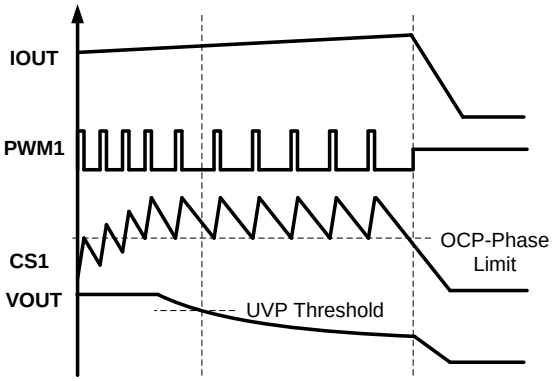


Figure 19: UVP Triggered when the Per-Phase Current is Limited by OCP_PHASE

Over-Voltage Protection (OVP)

The MP2927 provides two types of OVP VID_OVP and ABS_OVP by monitoring V_{DIFF}. If either OVP is triggered, the MP2927 turns on all LS-FETs to discharge C_{OUT} until V_{OUT} falls below 160mV. Then the devices initiates Hi-Z off.

VID_OVP is the OVP type that refers to V_{REF}. If V_{DIFF} exceeds the VID_OVP threshold for a set blanking time, then VID_OVP is triggered. The VID_OVP threshold can be configured via

PMBus command VOUT_OV_FAULT_LIMIT (40h), bits[10:8].

Similar to the UVP scheme, the VID_OVP scheme also provides also provides no action, hiccup, retry 6 times, and latch-off options.

The second type is called ABS_OVP. If V_{DIFF} exceeds the ABS_OVP threshold without a trigger delay time, then ABS_OVP is triggered. The ABS_OVP threshold is determined by VOUT_MAX (24h) and VOUT_OV_FAULT_LIMIT (40h), bits[7:0]. An ABS_OVP fault always initiates latch-off mode.

Figure 20 shows the OVP waveforms.

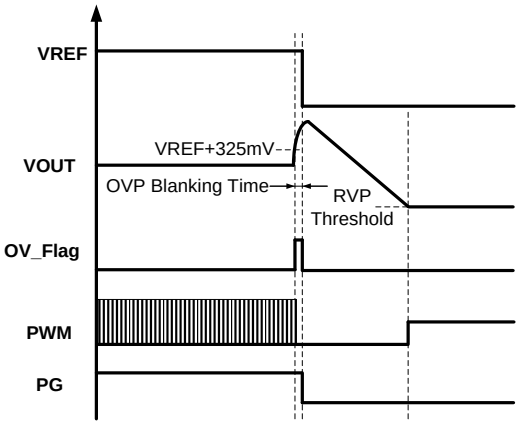


Figure 20: OVP Waveform

Reverse-Voltage Protection (RVP)

A large reverse I_L may cause negative output voltages that can harm the processor and other output components. The MP2927 provides reverse-voltage protection (RVP) with no additional system cost.

If OVP occurs, all LS-FETs are forced on to quickly discharge the voltage of the output capacitors. I_L becomes very negative, which can discharge the voltage of the output capacitors until they are negative enough to destroy the load without RVP.

If the VOSEN voltage falls below 160mV after OVP, and if RVP is enabled, then the MP2927 triggers RVP by latching all PWM outputs to tri-state. The reverse inductor current can quickly be reset to 0A by dissipating the energy in the inductor to the input DC voltage source through the forward-biased body diode of the high-side MOSFETs (HS-FETs). Figure 20 shows the RVP function after OVP.

Over-Temperature Protection (OTP)

Over-temperature protection (OTP) is triggered if the sensed power stage temperature exceeds the maximum temperature threshold. The MP2927 can be configured to latch-off mode or hiccup mode when OTP is triggered.

The MP2927 monitors the junction temperature of the Intelli-Phase™ by connecting the power stage's VTEMP (T_{OUT}) to the controller's TSENSE pin (see Figure 12 on page 21).

PROCHOT

The MP2927 senses the voltage on the PROCHOT pin with the internal analog-to-digital converter (ADC). If the PROCHOT voltage exceeds or falls bellows the threshold set by MFR_PROCHOT_SET (36h on Page 1), bits[13:8], then a PROCHOT fault occurs. The MP2927 shuts down rail 1 (or all rails). The rails that are shut down are determined by MFR_PROCHOT_SET (36h on Page 1), bit[15]. The PROCHOT sense fault direction is determined by MFR_PROCHOT_SET, bit[1].

The PROCHOT fault action mode can be set to latch-off or hiccup mode, which is determined by MFR_PROCHOT_SET, bit[0]. If latch-off mode is selected, the device remains off, even if the PROCHOT voltage changes. In hiccup mode, the system attempts to restart after a set protection delay time. This time can be configured via MFR_VR_CONFIG2 (C2h on Page 0), bits[14:13].

Line-Float Detection

The MP2927 supports remote sensing line-float detection (VOSEN, VORTN) during system initialization, after VDD33 powers on, and after EN powers on from low-power mode. The MP2927 latches off if a line float is detected, and reports the fault via PMBus command STATUS_VOUT (7Ah), bit[1]. Line-float detection can be enabled via MFR_VR_CONFIG4 (C4h on Page 0).

CS Fault and TEMP Fault

The MP2927 supports TEMP fault and CS fault protections to provide fast protections if any phase's DrMOS experiences a fault. If the TSENSE pin's voltage exceeds 2.2V, a TEMP fault occurs and the output is shut off. If the CS pin is pulled below 150mV, a CS fault occurs, and the output is shut off.

NVM Fault

If the data in the non-volatile memory (NVM) is invalid after the CRC during the NVM start-up process, the VR does not start until the fault is cleared.

Communication Failure

A data transmission fault occurs when information is not properly transferred between the devices. Several data transmission faults can occur:

- Sending too little data
- Reading too little data
- Host sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The data transmission faults assert ALT_P#. The CLEAR_FAULTS command de-asserts ALT_P#. If the faults is still present after this process, ALT_P# asserts again.

Intelli-Phase™ Fault Detection

The MP2927 supports Intelli-Phase™ fault type detection. Several types of Intelli-Phase™ faults can occur:

- Current-limit fault
- Over-temperature fault
- LS-FET shorted fault
- HS-FET shorted fault

This fault detection function only works when the Intelli-Phase™ supports fault type indication. Refer to the Intelli-Phase™ datasheet for more details.

If the fault protection and PWM fault detection function are both enabled, then the MP2927 scans the PWM fault if any of the following faults occur: V_{IN} UVLO, V_{IN} OVP, OTP, V_{OUT} UVP, V_{OUT} OVP, OCP, a VTEMP fault, or a CS fault.

If any of the above faults are triggered, the MP2927 executes the following steps (see Figure 21):

1. Shuts off the associated rail(s).
2. Starts the Intelli-Phase™ fault type scan for related rail(s) by sensing the impedance on the PWM pins.
3. Faults are reported to the Page 0 FAULTS_REPORT (E0~E5h) registers.
4. Faults are recorded to the NVM (registers F0h~F5h) when fault recording to the NVM is enabled. The last fault event is stored. To store faults to the NVM, the EN signal should remain high for at least 20ms after fault occurs.

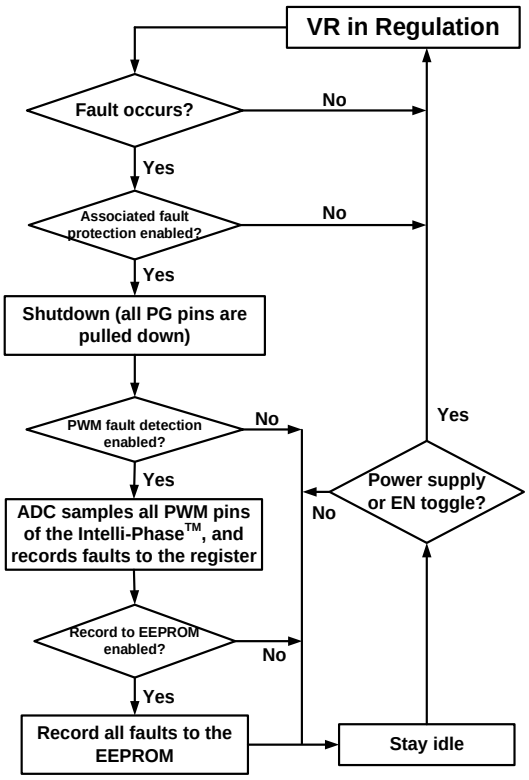


Figure 21: Intelli-Phase™ Fault Detection Flowchart

Configure the Intelli-Phase™ behaviors for fault detection and recording by enabling the following:

1. The fault protections using the related registers.
2. The ADC to sample the fault type from the Intelli-Phase's™ PWM pins.
3. Faults to be recorded to the NVM.

If a TSENSE or CS fault occurs, the MP2927 shuts down all rails. The faults are reported to the E0h~E5h registers on Page 1. If faults can be stored to the NVM, the faults (as well as the details related to the fault) are recorded to the F0h~F5h registers on Page 1. To record faults, the EN signal should remain high for at least 20ms after a fault occurs.

To clear the recorded fault in the NVM registers, send a FEh command.

PMBus Communication

The MP2927 supports real-time monitoring for the VR operation parameters and statuses with the PMBus interface. Table 3 lists the monitored parameters.

Table 3: PMBus Monitored Parameters

Parameter	PMBus
Output voltage	6.25mV/LSB
Output current	0.25A/LSB or 0.5A/LSB
Temperature	1°C
Input voltage	31.25mV/LSB
OVP	✓
UVP	✓
OCP	✓
OTP	✓
V_{IN} UVLO	✓
V_{IN} OVP	✓
Line float	✓
CML	✓

PMBus/I²C Interface

To support multiple VR devices used with the same PMBus/I²C interface, the MFR_ADDR_PMBUS register can configure the PMBus address.

Figure 22 on page 28 shows the supported PMBus/I²C transmission structure without packet error checking (PEC).

Figure 23 on page 28 shows the supported PMBus/I²C transmission structure with PEC.

There are six kinds of transmission structures:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word
6. Block read

To read or write the registers of the MP2927, the PMBus or I²C command must be compliant with the byte number of the register in the PMBus command table.

PMBus/I²C communication speed can support 1MHz.

VID Offset for Overclocking

The MP2927 can add an offset to the VID command, which is set by MFR_OFFSET_SET (22h). The target V_{OUT} is the sum of the VID value and the offset. Note that the maximum V_{OUT} is limited by VOUT_MAX.

With a 1x V_{DIFF} gain (the default), the maximum V_{OUT} is 1.6V. If the V_{OUT} range exceeds 1.6V, then the 1/2x V_{DIFF} gain must be enabled to support voltages above 1.6V, with a 3.2V maximum. Changing the offset value on the fly acts similarly to DVID operation, as the ramping up/down voltage slew rate is same as the DVID voltage slew rate.

AVSBus Mode

The MP2927 supports the following AVSBus protocol specified commands:

- Voltage read/write
- V_{OUT} transition rate read/write
- Current read
- Temperature read
- Voltage reset
- Power mode read/write
- AVSBus status read/write
- AVSBus version read

The MP2927 also supports slave interrupt functionality.

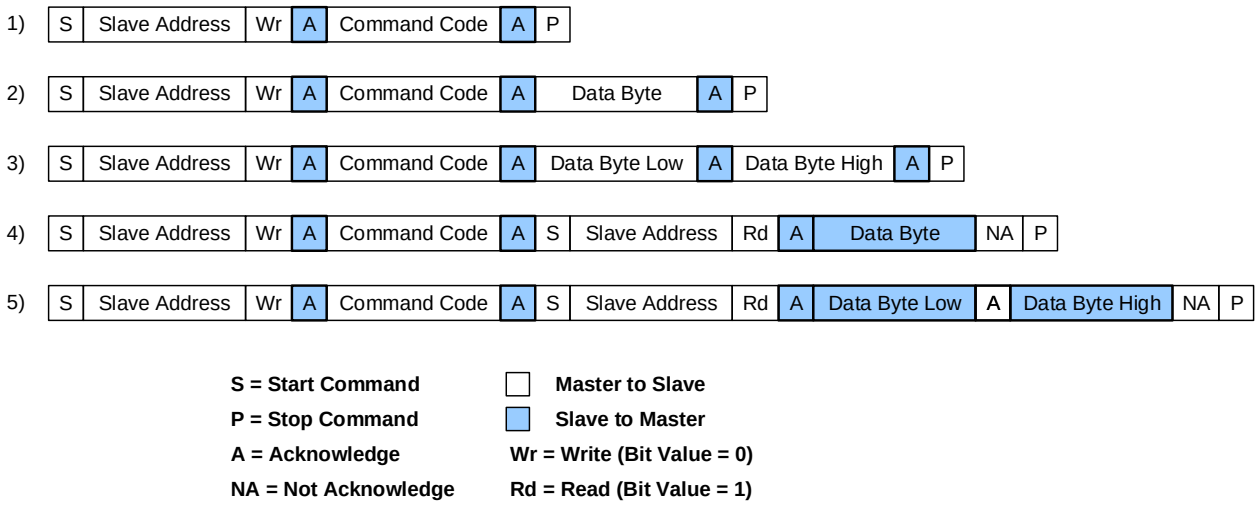


Figure 22: Supported PMBus/I²C Transmission Structure without PEC

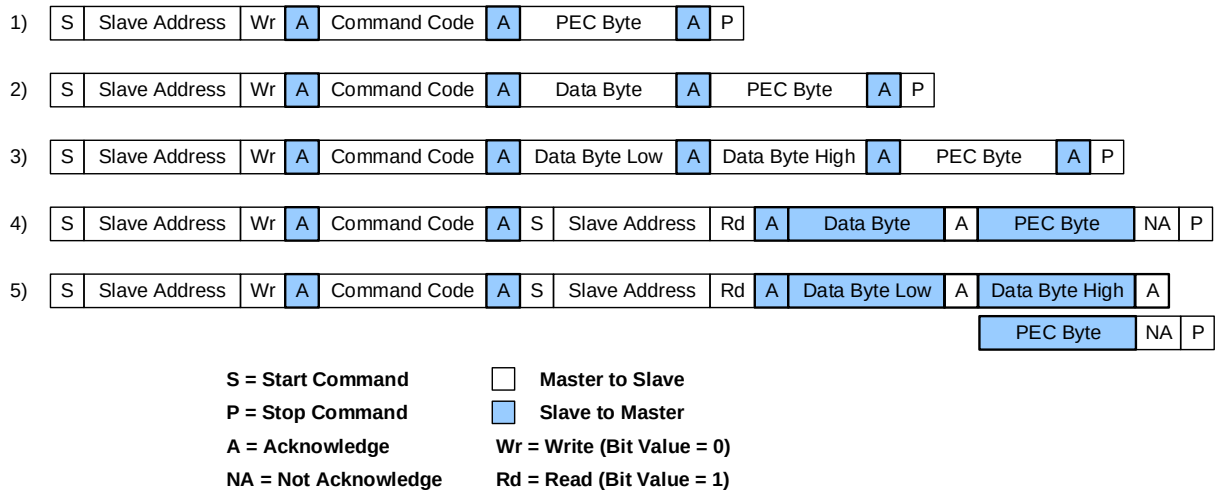


Figure 23: Supported PMBus/I²C Transmission Structure with PEC

PMBUS COMMANDS

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
00h	PAGE	R/W	1	✓	✓	✓
01h	OPERATION	R/W	1	✓	✓	✓
03h	CLEAR_FAULTS	Send	0	✓	✓	✓
10h	WRITE_PROTECT	R/W	1	✓	-	-
15h	STORE_ALL_CODE	Send	0	✓	✓	✓
16h	RESTORE_ALL_CODE	Send	0	✓	✓	✓
17h	STORE_USER_CODE	Send	0	✓	✓	✓
18h	RESTORE_USER_CODE	Send	0	✓	✓	✓
20h	VOUT_MODE	R/W	2	✓	-	-
21h	VOUT_COMMAND	R/W	2	✓	✓	✓
22h	MFR_VOUT_TRIM	R/W	2	✓	✓	✓
23h	MFR_SD_VID_SET	R/W	2	✓	-	-
	VDIFF1_SNAPSHOT	R/W	2	-	-	✓
24h	VOUT_MAX	R/W	2	✓	✓	✓
25h	MFR_JOUT_LONG_TERM	R/W	2	✓	✓	✓
26h	MFR_JOUT_SHORT_TERM	R/W	2	✓	✓	✓
27h	VOUT_TRANSITION_RATE	R/W	2	✓	✓	✓
28h	VOUT_DROOP	R/W	2	✓	✓	✓
29h	VOUT_SCALE_LOOP	R/W	2	✓	✓	✓
2Ah	MFR_SETTLE_CTRL	R/W	2	✓	✓	✓
2Bh	VOUT_MIN	R/W	2	✓	✓	✓
2Ch	MFR_TRIM_DCM_1P_2P_R1	R/W	2	✓	✓	✓
2Dh	MFR_TRIM_3P_4P_5P_R1	R/W	2	✓	-	-
	MFR_RESERVED	R/W	2	-	✓	-
	MFR_PMBUS_VTH	R/W	2	-	-	✓
2Eh	MFR_TRIM_6P_7P_8P_R1	R/W	2	✓	-	
	MFR_AVS_SET2	R/W	2	-	-	✓
2Fh	MFR_BLANK_LV1_R1	R/W	2	✓	-	-
	MFR_BLANK_LV1_R2	R/W	2	-	✓	-
	MFR_CP_SET	R/W	2	-	-	✓
30h	MFR_BLANK_LV2_R1	R/W	2	✓	-	✓
	MFR_PMBUS_TIMEOUT2	R/W	2	-	✓	
31h	MFR_BLANK_TIME1	R/W	2	✓	✓	✓
32h	MFR_PRT_CONFIG	R/W	2	✓	-	-
	VIN_SCALE_LOOP	R/W	2	-	✓	-
	MFR_PI_LOOP	R/W	2	-	-	✓
33h	FREQUENCY_SWITCH	R/W	2	✓	✓	✓
34h	MFR_OSR_SET	R/W	2	✓	✓	✓
35h	VIN_ON	R/W	2	✓	-	
	MFR_AVS_SET	R/W	2	-	-	✓
36h	VIN_OFF	R/W	2	✓	-	-
	MFR_PROCHOT_SET	R/W	2	-	✓	-

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
36h	MFR_AVS_WARN_MASK	R/W	2	-	-	✓
37h	MFR_SLOPE_SW_INI	R/W	2	✓	✓	✓
38h	MFR_SLOPE_SR_DCM	R/W	2	✓	✓	✓
39h	MFR_SLOPE_SR_1P	R/W	2	✓	✓	✓
3Ah	MFR_SLOPE_SR_2P	R/W	2	✓	✓	✓
3Bh	MFR_SLOPE_SR_3P_R1	R/W	2	✓	-	-
	MFR_SLOPE_SR_8P_R1	R/W	2	-	✓	-
	SR_LIMIT_1mV	R/W	2	-	-	✓
3Ch	MFR_SLOPE_SR_4P_R1	R/W	2	✓	-	-
	MFR_SLOPE_SR_7P_R1	R/W	2	-	✓	-
	MFR_TRIM_SEL	R/W	2	-	-	✓
3Dh	MFR_SLOPE_SR_5P_R1	R/W	2	✓	-	-
	MFR_SLOPE_SR_6P_R1	R/W	2	-	✓	-
	MFR_TRIM_SEL_R3	R/W	2	-	-	✓
3Eh	MFR_VRHOT_SET	R/W	2	✓	✓	✓
3Fh	MFR_IDRP_AC_SET	R/W	2	✓	✓	✓
40h	VOUT_OV_FAULT_LIMIT	R/W	2	✓	✓	✓
41h	VOUT_OV_FAULT_RESPONSE	R/W	2	✓	✓	✓
42h	VOUT_MAX_ALERT	R/W	2	✓	✓	✓
43h	VOUT_MIN_ALERT	R/W	2	✓	✓	✓
44h	VOUT_UV_FAULT_LIMIT	R/W	2	✓	✓	✓
45h	VOUT_UV_FAULT_RESPONSE	R/W	2	✓	✓	✓
46h	IOUT_OC_FAULT_LIMIT	R/W	2	✓	✓	✓
47h	IOUT_OC_FAULT_RESPONSE	R/W	2	✓	✓	✓
48h	IOUT_OC_SPIKE_RESPONSE	R/W	2	✓	✓	✓
49h	MFR_OCP_PHASE_LIMIT	R/W	2	✓	✓	✓
4Ah	IOUT_MAX_ALERT	R/W	2	✓	✓	✓
4Bh	MFR_FS_LIMIT_12P	R/W	2	✓	✓	✓
4Ch	MFR_FS_LIMIT_34P_R1	R/W	2	✓	-	✓
	MFR_FS_LIMIT_78P_R1	R/W	2	-	✓	-
	MFR_FS_LIMIT_56P_R1	R/W	2	-	-	✓
4Dh	MFR_APS_LEVEL_12P	R/W	2	✓	✓	✓
4Eh	MFR_APS_LEVEL_23P_R1	R/W	2	✓	-	-
	MFR_APS_LEVEL_67P_R1	R/W	2	-	✓	-
	MFR_APS_LEVEL_45P_R1	R/W	2	-	-	✓
4Fh	OT_FAULT_LIMIT	R/W	2	✓	✓	✓
50h	MFR_CORE_OTP_SET	R/W	2	✓	-	-
	MFR_NVM_WP	R/W	2	-	✓	-
	MFR_SMBALERT_MASK	R/W	2	-	-	✓
51h	MFR_FS_DETECT	R/W	2	✓	✓	✓
52h	MFR_APS_CTRL	R/W	2	✓	✓	✓
53h	MFR_APS_CTRL2	R/W	2	✓	✓	✓

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
54h	MFR_APS_CTRL3	R/W	2	✓	✓	✓
55h	VIN_OV_FAULT_LIMIT	R/W	2	✓	-	-
	MFR_CUSTOMER_ID	R/W	2	-	✓	-
	MFR_NVM_CTRL	R/W	2	-	-	✓
56h	MFR_FSCB_LOOP_CTRL	R/W	2	✓	✓	✓
57h	MFR_VOUT_LOOP_CTRL	R/W	2	✓	✓	✓
58h	JOUT_PK_SHORT	R/W	2	✓	✓	✓
59h	JOUT_PK_LONG	R/W	2	✓	✓	✓
5Ah	MFR_SLOPE_CNT_1P	R/W	2	✓	✓	✓
5Bh	MFR_SLOPE_CNT_23P	R/W	2	✓	✓	✓
5Ch	MFR_SLOPE_CNT_45P_R1	R/W	2	✓	-	-
	MFR_SLOPE_CNT_8P_R1	R/W	2	-	✓	
	VDIFF2_SNAPSHOT	R/W	2	-	-	✓
5Dh	MFR_SLOPE_CNT_67P_R1	R/W	2	✓	-	-
	VDIFF3_SNAPSHOT	R/W	2	-	-	✓
5Eh	MFR_SLOPE_CNT_DCM	R/W	2	✓	✓	✓
5Fh	MFR_PG_DELAY	R/W	2	✓	✓	✓
60h	TON_DELAY	R/W	2	✓	✓	✓
61h	TON_RISE	R/W	2	✓	✓	✓
62h	MFR_PWM_MIN_TIME1	R/W	2	✓	✓	✓
63h	MFR_PWM_MIN_TIME2	R/W	2	✓	✓	✓
64h	TOFF_DELAY	R/W	2	✓	✓	✓
65h	TOFF_FALL	R/W	2	✓	✓	✓
66h	GPIO_SEL_GROUP1	R/W	2	✓	-	-
	GPIO_SEL_GROUP3	R/W	2	-	✓	-
	(MFR_RESERVED)	R/W	2	-	-	✓
67h	GPIO_SEL_GROUP2	R/W	2	✓	-	
	GPIO_SEL_GROUP4/6	R/W	2	-	✓	✓
68h	GPIO_MODE	R/W	2	✓	-	-
	GPIO_ACTIVE	R/W	2	-	✓	-
	MFR_EN_SEL	R/W	2	-	-	✓
69h	MFR_VR_TEMP_CAL	R/W	2	✓	✓	✓
6Ah	MFR_VOUT_CALC	R/W	2	✓	✓	✓
6Bh	MFR_IOUT_CALC_AVS	R/W	2	✓	✓	✓
6Ch	IOUT_CAL_GAIN_PMBUS	R/W	2	✓	✓	✓
6Dh	IOUT_CAL_OS_PMBUS	R/W	2	✓	✓	✓
6Eh	MFR_IMON_SET	R/W	2	✓	✓	✓
6Fh	IOUT_MIN_ALERT	R/W	2	✓	✓	✓
70h	MFR_PHASE_CFG	R/W	2	✓	-	-
	MFR_CONFIG_ID	R/W	2	-	✓	-
	MFR_PSI_SET	R/W	2	-	-	✓
71h	MFR_PVID01	R/W	2	✓	✓	✓

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
72h	MFR_PVID23_R1	R/W	2	✓	✓	✓
73h	MFR_PVID45_R1/2	R/W	2	✓	✓	✓
74h	MFR_PVID67_R1	R/W	2	✓	✓	✓
75h	SAMPLE_INTERVAL_12P	R/W	2	✓	✓	✓
76h	SAMPLE_INTERVAL_34P_R1	R/W	2	✓	-	-
	MFR_RESERVED	R/W	2	-	✓	-
	CRC_USER_LAST	R/W	2	-	-	✓
77h	MFR_ADDR_PMBUS	R/W	2	✓	-	-
	MFR_RESERVED	R/W	2	-	✓	✓
78h	STATUS_BYTE	R	1	✓	✓	✓
79h	STATUS_WORD	R	2	✓	✓	✓
7Ah	STATUS_VOUT	R	1	✓	✓	✓
7Bh	STATUS_IOUT	R	1	✓	✓	✓
7Ch	STATUS_INPUT	R	1	✓	✓	✓
7Dh	STATUS_TEMPERATURE	R	1	✓	✓	✓
7Eh	STATUS_CML	R	1	✓	✓	✓
81h	READ_ADC_SUM	R	2	✓	✓	✓
82h	READ_VFB_SENSE	R	2	✓	✓	✓
83h	READ_TSENSE_SENSE	R	2	✓	-	-
84h	READ_CS1	R	2	✓	-	-
	READ_CS5	R	2	-	✓	-
85h	READ_CS2	R	2	✓	-	-
	READ_CS6	R	2	-	✓	-
	READ_CS9	R	2	-	-	✓
86h	READ_CS3	R	2	✓	-	-
	READ_CS7	R	2		✓	-
87h	READ_CS4	R	2	✓	-	-
	READ_CS8	R	2	-	✓	-
	READ_CS10	R	2	-	-	✓
88h	READ_VIN	R	2	✓	✓	✓
8Bh	READ_VOUT	R	2	✓	✓	✓
8Ch	READ_IOUT	R	2	✓	✓	✓
8Dh	READ_TEMPERATURE	R	2	✓	✓	✓
8Eh	READ_ADC_RESULT	R	2	-	✓	✓
8Fh	READ_VCOMP	R	2	✓	✓	✓
96h	READ_POUT	R	2	✓	✓	✓
98h	PMBUS_REVISION	R	2	✓	-	-
99h	MFR_ID	R	Block	✓	-	-
9Ah	MFR_MODEL	R	Block	✓	-	-
9Bh	MFR_REVISION	R	Block	✓	-	-
9Dh	MFR_DATE	R	Block	✓	-	-
9Fh	MFR_PRODUCT_ID	R/W	2	✓	-	-

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
C0h	MFR_PRODUCT_REV	R	1	✓	-	-
	RESERVED	R/W	2	-	✓	-
C1h	MFR_VR_CONFIG1	R/W	2	✓	-	-
C2h	MFR_VR_CONFIG2	R/W	2	✓	-	-
C3h	MFR_VR_CONFIG3	R/W	2	✓	-	-
C4h	MFR_VR_CONFIG4	R/W	2	✓	-	-
C5h	MFR_VR_CONFIG5	R/W	2	✓	-	-
C6h	MFR_VR_CONFIG6	R/W	2	✓	-	-
C7h	MFR_VR_CONFIG7	R/W	2	✓	-	-
C8h	MFR_TIMEOUT	R/W	2	✓	-	-
D0h	CAPABILITY	R	2	✓	✓	✓
D1h	JOUT_SHORT_TERM	R	2	✓	✓	✓
D2h	JOUT_LONG_TERM	R	2	✓	✓	✓
D3h	IMON_FAST_SENSE	R	2	✓	✓	✓
D4h	VDIFF_FAST_SENSE	R	2	✓	✓	✓
D5h	DIE_TEMP_SENSE	R	2	-	✓	-
E0h	FAULTS_REPORT1	R	2	-	✓	-
E1h	FAULTS_REPORT2	R	2	-	✓	-
E2h	FAULTS_REPORT3	R	2	-	✓	-
E3h	FAULTS_REPORT4	R	2	-	✓	-
E4h	FAULTS_REPORT5	R	2	-	✓	-
E5h	FAULTS_REPORT6	R	2	-	✓	-
F0h	FAULTS_RECORD1	R	2	-	✓	-
F1h	FAULTS_RECORD2	R	2	-	✓	-
F2h	FAULTS_RECORD3	R	2	-	✓	-
F3h	FAULTS_RECORD4	R	2	-	✓	-
F4h	FAULTS_RECORD5	R	2	-	✓	-
F5h	FAULTS_RECORD6	R	2	-	✓	-
FBh	ADC_SUM_RESET	Send	0	✓	✓	✓
FCh	CLEAR_CRC_FAULT	Send	0	✓	✓	✓
FEh	CLEAR_STORED_FAULTS	Send	0	✓	✓	✓
FFh	CLEAR_NVM_FAULTS	Send	0	✓	✓	✓

PAGE 0 REGISTER MAP

PAGE (00h)

The PAGE command on Page 0 provides the ability to configure, control, and monitor all registers, including test mode and the NVM, through only one physical address.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
7:2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1:0	PAGE	0x00: Page 0. All PMBus commands address the operating registers on Page 0 0x01: Page 1. All PMBus commands address the operating registers on Page 1 0x02: Page 2. All PMBus commands address the operating registers on Page 1 0x03: Page 4. All PMBus commands address the test mode registers 0x28: Page 28. All PMBus commands address the NVM registers that are mapped to the operating registers on Page 0 0x29: Page 29. All PMBus commands address the NVM registers that are mapped to the operating registers on Page 1 0x29: Page 2A. All PMBus commands address the NVM registers that are mapped to the operating registers on Page 2

OPERATION_R1 (01h)

The OPERATION_R1 command on Page 0 turns the rail 1 output on and off in conjunction with the input from EN pin, and sets V_{OUT} to the upper or lower margin voltages. The controller stays in the OPERATION command setting mode until a subsequent OPERATION command is received, or a change to EN sets rail 1 to another mode.

Command	OPERATION_R1							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								

Bits	Bit Name	Description
7:0	OPERATION_R1	Sets the operation mode for rail 1. 8’b 00xx xxxx: Hi-Z off 8’b 01xx xxxx: Soft shutdown 8’b 1000 xxxx: Normal on 8’b 1001 xxxx: Margin low 8’b 1010 xxxx: Margin high 8’b 1011 xxxx: AVSBus mode Others: Invalid commands “x” means not applicable.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page 0 clears any fault bits in the following registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), and STATUS_CML (7Eh).

This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

The WRITE_PROTECT command on Page 0 controls writing to the PMBus device. This command provides protection against accidental changes. This command is not intended to provide protection against deliberate changes to the device's configuration or operation.

All support commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Command	WRITE_PROTECT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	WRITE_PROTECT							

Bits	Bit Name	Description
7:0	WRITE_PROTECT	0x80: Disable all writes except to the WRITE_PROTECT command 0x40: Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 0x20: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND commands 0x00: Enable writes to all commands Others: Invalid commands

STORE_ALL_CODE (15h)

The STORE_ALL_CODE command on Page 0 instructs the PMBus device to copy all the Page 0, Page 1, and Page 2 contents, including the internal trim registers, of the operating memory to the matching locations in the NVM. Any items in operating memory that do not have matching locations in the NVM are ignored.

This command is controlled by 50h (Page 1), bits[7:0]. Register 50h, bits[7:0] must be set to 0x63 to write to the NVM. If it is any other value, the NVM is write-protected.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command on Page 0 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents, including the internal trim registers, from the NVM, and overwrite the matching locations in the operating memory. Any items in the user store that do not have matching locations in the operating memory are ignored.

This command cannot be used while the device is outputting power, and is ignored if attempted.

This command is write-only. There is no data byte for this command.

STORE_USER_CODE (17h)

The STORE_ALL_CODE command on Page 0 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents of the operating memory to the matching locations in the NVM (excluding the trim registers). Any items in operating memory that do not have matching locations in the NVM are ignored.

This command is controlled by 50h (Page 1), bits[7:0]. 50h, bits[7:0] must be set to 0x63 to write to the NVM. If it is any other value, the NVM is write-protected.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_USER_CODE (18h)

The RESTORE_USER_CODE command on Page 0 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the NVM, and overwrite the matching locations in the operating memory. Any items in user store that do not have matching locations in the operating memory are ignored. Trim registers are not overwritten by this command.

This command cannot be used while the device is outputting power, and is ignored if attempted.

This command is write-only. There is no data byte for this command.

VOUT_MODE (20h)

The VOUT_MODE command on Page 0 to returns the key VID features that the MP2927 can support.

Command	VOUT_MODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DEVICE_VOUT_MODE			EXPONENT				

Bits	Bit Name	Description
7:5	DEVICE_VOUT_MODE	3'b000: Linear mode 3'b010: Direct mode
4:0	EXPONENT	Linear mode: Sets the 5-bit, two's complement exponent for the mantissa, which is delivered as the data bytes for an output voltage related command. If EXP = 5'b 10111, the resolution is 2mV. Direct mode: Always set to 5'b 00000.

VOUT_COMMAND_R1 (21h)

The VOUT_COMMAND_R1 command on Page 0 sets the rail 1 V_{REF} VID in PMBus override mode.

Command	VOUT_COMMAND_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_COMMAND_R1										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_COMMAND_R1	Sets the rail 1 V_{REF} (VID_DAC V_{OUT}) in PMBus VID mode. 1 VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits [15:14].

VOUT_TRIM_R1 (22h)

The VOUT_TRIM_R1 command on Page 0 applies a fixed offset voltage to the commanded rail 1 V_{OUT}.

Command	VOUT_TRIM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	VOUT_TRIM_R1								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRIM_R1	Sets the V_{OUT} offset voltage on rail 1. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits [15:14].

MFR_SD_VID_SET (23h)

MFR_SD_VID command on Page 0 sets the Hi-Z shutdown voltage threshold. It is only effective when VID is slewing down to 0V.

Command	MFR_SD_VID_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	MFR_VID_OFF					MFR_SD_VID							

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:8	MFR_VID_OFF	Sets the minimum operating V_{REF} for all three rails. If the target VID is below the value set by MFR_VID_OFF, the associated rail will DVID down to 0V and de-assert the PG signal. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits[15:14].
7:0	MFR_SD_VID	Sets the PWM Hi-Z shut down voltage threshold. Once the VID-DAC output is below the Hi-Z shut down threshold, the output enters PWM Hi-Z shutdown mode. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits[15:14].

VOUT_MAX_R1 (24h)

The VOUT_MAX_R1 command on Page 0 sets the maximum V_{REF} for rail 1 VID-DAC, which sets the maximum V_{OUT}. When an external resistor divider is applied, the maximum voltage is clamped to VOUT_MAX / K_R. K_R is the dividing ratio for the external resistor divider. This command is effective in PMBus mode.

Command	VOUT_MAX_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_MAX_R1										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MAX_R1	Set the rail 1 maximum VID + offset voltage. This limits the sum of VID + the VOUT_TRIM offset. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits [15:14].

MFR_JOUT_LONG_TERM_R1 (25h)

The MFR_JOUT_LONG_TERM_R1 command on Page 0 sets the rail 1 long-term value to calculate J_{OUT}.

Command	MFR_JOUT_LONG_TERM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	JOUT_LONG_TERM									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	JOUT_LONG_TERM	Sets the long-term value for the J_{OUT} calculation, calculated with the following equation: LONG_TIME = JOUT_LONG_TERM x SHORT_TIME

MFR_JOUT_SHORT_TERM_R1 (26h)

The MFR_JOUT_SHORT_TERM_R1 command on Page 0 sets the rail 1 short-term value to calculate J_{OUT}.

Command	MFR_JOUT_SHORT_TERM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		X														

Bits	Bit Name	Description
15	JOUT_METHOD_SEL	Selects the J_{OUT} calculation method. 1'b1: Fixed frequency. Sample the current and voltage with a fixed frequency 1'b0: Adjustable frequency. Sample the current and voltage after a delay time at the PWM1 falling edge
14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	JOUT_EN	Enables the J_{OUT} function. 1'b1: Enabled 1'b0: Disabled
12:7	JOUT_SHORT_TERM_FIX_FREQ	Bits[12:7] are fixed to 0 in fixed frequency mode.
6:0		Bits[6:0] set JOUT_SHORT_TERM in fixed-frequency mode. ADC_TIME/LSB. The short-term value can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_FIX_FREQ x ADC_TIME
12:1	JOUT_SHORT_TERM_ADAPTIVE_FREQ	50ns/LSB in adjustable-frequency mode. The short-term value can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_ADAPTIVE_FREQ x 50ns
0		Bit[0] is fixed to 0 in adjustable-frequency mode.

VOUT_TRANSITION_RATE_R1 (27h)

The VOUT_TRANSITION_RATE_R1 command on Page 0 sets the rail 1 dynamic VID (DVID) transition slew rate and EN soft shutdown slew rate in PMBus mode.

Command	VOUT_TRANSITION_RATE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	VOUT_TRANSITION_RATE_R1												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	VOUT_TRANSITION_ RATE_R1	Sets the rail 1 DVID transition slew rate and the EN soft shutdown slew rate in PMBus mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h), bit[15].

VOUT_DROOP_R1 (28h)

The VOUT_DROOP_R1 command on Page 0 sets the load-line parameters for rail 1.

Command	VOUT_DROOP_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function											RDROOP_SET_R1					

Bits	Bit Name	Description
15	IACDROOP_BW_ SET_R1	Enables the device to reduce the BW of the AC droop by reducing the bias current. This is for rail 1 only. 1’b0: Disabled 1’b1: Enabled
14	IACDROOP_BW_ SET_R1	Enables the device to reduce the BW of the AC droop by increasing the compensation capacitor. This is for rail 1 only. 1’b0: Disabled 1’b1: Enabled
13	IACDROOP_ GAIN2_SET_R1	Set the PMBus load line slope (AC droop) level; active when bit[12] of this command = 1. 1’b0:1 x IDROOP_INI 1’b1:1/2 x IDROOP_INI
12	MFR_ACLL_EN_R1	Selects the AC or DC load line. 1’b0: DC load line 1’b1: AC load line
11:9	PMBUS_LL_LEVEL_R1	Sets the PMBus load line slope (DC droop) level; active when bit[12] of this command = 1. The MP2927 provides 8 levels for DC droop. 3’b000: 0 3’b001: 3/4 x IDROOP_INI 3’b010: 4/4 x IDROOP_INI 3’b011: 5/4 x IDROOP_INI 3’b100: 6/4 x IDROOP_INI 3’b101: 7/4 x IDROOP_INI 3’b110: 8/4 x IDROOP_INI 3’b111: 9/4 x IDROOP_INI

8:7	IDROOP_GAIN1_ SET_R1	Sets the I_{DROOP} gain for rail 1. 2'b00: 1/16 x IDROOP_INI 2'b01: 1/8 x IDROOP_INI 2'b10: 1/4 x IDROOP_INI 2'b11: 1/2 x IDROOP_INI
6	SHORT_FIRST_ HALF_R1	Set this bit to 1 if R_{DROOP} is below 800Ω. 1'b0: Do not short the first half of the rail 1 resistors 1'b1: Short the first half of the rail 1 resistors
5:0	RDROOP_SET_R1	Sets the R_{DROOP} for rail 1. 25Ω/LSB. 1.6kΩ maximum.

VOUT_SCALE_LOOP_R1 (29h)

The VOUT_SCALE_LOOP_R1 command on Page 0 sets the rail 1 output voltage (V_{OUT}) to reference voltage (V_{REF}) dividing ratio when an external output divider is applied.

Command	VOUT_SCALE_LOOP_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	VOUT_SCALE_LOOP_R1							

Bits	**Bit Name**	**Description**
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VOUT_SCALE_LOOP_ R1	Sets the rail 1 V_{OUT} to V_{REF} dividing ratio. V_{REF} ranges from 0V to 1.6V.

MFR_SETTLE_CTRL_R1 (2Ah)

The MFR_SETTLE_CTRL_R1 command on Page 0 sets the DVID parameters.

Command	MFR_SETTLE_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_DROOPFALL_DELAY_R1					MFR_RISE_STEP_R1										

Bits	**Bit Name**	**Description**
15:11	MFR_DROOPFALL_ DELAY_R1	Sets the delay time between V_{REF} reaching the target (VID + DROOP_VID) and V_{REF} falling back to VID. 50ns/LSB.
10:6	MFR_RISE_STEP_R1	Sets the extra VID steps count for rail 1 when DVID goes up. The extra VID steps are used to compensate the droop created when the output capacitor charges during DVID up. 1 step/LSB.
5:0	RESERVED	Fixed to 0.

VOUT_MIN_R1 (2Bh)

The VOUT_MIN_R1 command on Page 0 instructs the device to limit the rail 1 minimum V_{OUT} in PMBus mode. When the V_{OUT} decoded from PMBus interface is below the value set by VOUT_MIN (2Bh), V_{OUT} is clamped to VOUT_MIN. When an external resistor divider is applied on VOSEN, the minimum V_{OUT} is clamped to VOUT_MIN / K_R. Where K_R is the dividing ratio of the divider.

Command	VOUT_MIN_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_MIN_R1										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MIN_R1	Sets the minimum VID under PMBus mode for rail 1. Any VID below this value is clamped to VOUT_MIN. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits[15:14].

MFR_TRIM_DCM_1P_2P_R1 (2Ch)

The MFR_TRIM_DCM_1P_2P_R1 command on Page 0 trims V_{OUT} at 2-phase CCM and 1-phase CCM or DCM. This is for the rail 1 power state.

Command	MFR_TRIM_DCM_1P_2P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	MFR_TRIM_2PS_R1					MFR_TRIM_1PS_R1					MFR_TRIM_DCM_R1				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	MFR_TRIM_2PS_R1	Set the V_{OUT} trim for 2-phase CCM on rail 1. 2.3mV/LSB.
9:5	MFR_TRIM_1PS_R1	Set the V_{OUT} trim for 1-phase CCM on rail 1. 2.3mV/LSB.
4:0	MFR_TRIM_DCM_R1	Set the V_{OUT} trim for 1-phase DCM on rail 1. 2.3mV/LSB.

MFR_TRIM_3P_4P_5P_R1 (2Dh)

The MFR_TRIM_3P_4P_5P_R1 command on Page 0 trims V_{OUT} at 3-phase, 4-phase, and 5-phase CCM. This is for the rail 1 power state.

Command	MFR_TRIM_3P_4P_5P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	MFR_TRIM_5PS_R1					MFR_TRIM_4PS_R1					MFR_TRIM_3PS_R1				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	MFR_TRIM_5PS_R1	Set the V_{OUT} trim for 5-phase CCM on rail 1. 2.3mV/LSB.
9:5	MFR_TRIM_4PS_R1	Set the V_{OUT} trim for 4-phase CCM on rail 1. 2.3mV/LSB.
4:0	MFR_TRIM_3PS_R1	Set the V_{OUT} trim for 3-phase CCM on rail 1. 2.3mV/LSB.

MFR_TRIM_6P_7P_8P_R1 (2Eh)

The MFR_TRIM_6P_7P_8P_R1 command on Page 0 trims V_{OUT} at 6-phase, 7-phase, and 8-phase CCM. This is for the rail 1 power state.

Command	MFR_TRIM_6P_7P_8P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	MFR_TRIM_8PS_R1					MFR_TRIM_7PS_R1					MFR_TRIM_6PS_R1				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	MFR_TRIM_8PS_R1	Set the V_{OUT} trim for 8-phase CCM on rail 1. 2.3mV/LSB.
9:5	MFR_TRIM_7PS_R1	Set the V_{OUT} trim for 7-phase CCM on rail 1. 2.3mV/LSB.
4:0	MFR_TRIM_6PS_R1	Set the V_{OUT} trim for 6-phase CCM on rail 1. 2.3mV/LSB.

MFR_BLANK_LV1_R1 (2Fh)

The MFR_LV1_TIME_R1 command on Page 0 sets the signal blanking time between two consecutive phases in multi-phase operation.

Command	MFR_BLANK_LV1_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PHS_NUM_LVL1				SLOPE_RESET_TIME2						MFR_BLANK_TIME2					

Bits	Bit Name	Description
15:12	PHS_NUM_LVL1	Sets the phase number threshold that triggers the slope compensation reset time and PWM blanking time.
11:6	SLOPE_RESET_TIME2	Configures the second set of slope compensation reset times. Note that the slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME (MFR_BLANK_TIME1 (2Fh on Page 0), bits[5:0]). 5ns/LSB.
5:0	MFR_BLANK_TIME2	Configures the second set of PWM blanking times between two consecutive phases. 5ns/LSB.

MFR_BLANK_LV2_R1 (30h)

The MFR_LV2_TIME_R1 command on Page 0 sets the signal blanking time between two consecutive phases in multi-phase operation.

Command	MFR_BLANK_LV2_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PHS_NUM_LVL2				SLOPE_RESET_TIME3						MFR_BLANK_TIME3					

Bits	Bit Name	Description
15:12	PHS_NUM_LVL2	Sets the phase number threshold that triggers the slope compensation reset time and PWM blanking time.
11:6	SLOPE_RESET_TIME3	Configures the third set of slope compensation reset times. Note that the slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME (MFR_BLANK_TIME1 (30h on Page 0), bits[5:0]). 5ns/LSB.

5:0	MFR_BLANK_TIME3	Configures the third set of PWM blanking times between two consecutive phases. 5ns/LSB.

MFR_BLANK_TIME1_R1 (31h)

The MFR_BLANK_TIME1_R1 command on Page 0 configures the slope compensation reset time and PWM blanking time between two consecutive phases.

Command	MFR_BLANK_TIME1_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					MFR_SLOPE_BLANK_TIME1_R1						MFR_PHASE_BLANK_TIME1_R1					

Bits	Bit Name	Description
15:12	RESERVED	Fixed to 0.
11:6	MFR_SLOPE_BLANK_ TIME1_R1	Configures the slope compensation reset time. Note that the slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME (MFR_BLANK_TIME1 (31h on Page 0), bits[5:0]). 5ns/LSB. The blank time can be calculated with the following equation: MFR_SLOPE_BLANK_TIME1_R1 = (bits[11:6] x 5 + 25) ns
5:0	MFR_PHASE_BLANK_ TIME1_R1	Configures the PWM blanking times between two consecutive phases. 5ns/LSB. The PWM blanking time can be calculated with the following equation: MFR_PHASE_BLANK_TIME1_R1 = (bits[5:0] x 5 + 25) ns

MFR_PRT_CONFIG (32h)

The MFR_PRT_CONFIG command on Page 0 sets certain configurations for the MP2927.

Command	MFR_PRT_CONFIG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	OT_WARN_EN	Enables the over-temperature (OT) warning function for all rails. If an OT warning occurs, ALT_P# asserts. 1'b0: Disabled 1'b1: Enabled
14	OC_WARN_EN	Enables the over-current (OC) warning function for all rails. If an OC warning occurs, ALT_P# asserts. 1'b0: Disabled 1'b1: Enabled
13	UV_WARN_EN	Enables the under-voltage (UV) warning function for all rails. If a UV warning occurs, ALT_P# asserts. 1'b0: Disabled 1'b1: Enabled
12	OV_WARN_EN	Enables the over-voltage (OV) warning function for all rails. If an OV warning occurs, ALT_P# asserts. 1'b0: Disabled 1'b1: Enabled

11:10	MFR_VIN_UVP_MODE	Sets the V_{IN} UVP mode. 2'b00: No action 2'b01: Latch-off mode 2'b1x: Retry
9	MFR_VIN_OVP_MODE	Sets the V_{IN} OVP mode. 1'b0: Retry 1'b1: Latch-off mode
8	MFR_VINUV_WARN_EN	Enables the V_{IN} UV warning function. If a V_{IN} UV warning occurs, ALT_P# asserts. 1'b0: Disabled 1'b1: Enabled
7	MFR_VIN_FLT_EN	Enables all V_{IN} fault functions. 1'b0: Disabled 1'b1: Enabled
6	MFR_CORE_OTP_EN	Enables chip OTP. If chip OTP occurs, ALT_P# asserts. 1'b0: Disabled 1'b1: Enabled
5	MFR_OTP_EN_R3	Enables rail 3 OTP. 1'b0: Disabled 1'b1: Enabled
4	MFR_OTP_EN_R2	Enables rail 2 OTP. 1'b0: Disabled 1'b1: Enabled
3	MFR_OTP_EN_R1	Enables rail 1 OTP in independent mode. This bit controls all rails in merge mode. 1'b0: Disable DrMOS OTP 1'b1: Enable DrMOS OTP
2	MFR_CSPIN_FAULT_EN	Enables the CS pin to act as a DrMOS fault indicator and record the fault type to the NVM. The MP2927 monitors the CS pin voltage; if the voltage drops below 160mV, a DrMOS fault has occurred. 1'b0: Disabled 1'b1: Enabled
1	MFR_PROTECT_ ALL_SHUTDOWN	Enable all rails to shut down if a protection occurs. 1b'0: Disabled 1b'1: Enabled
0	MFR_PROTECT_ALL_ DIS	1'b0: Enables all protections 1'b1: If bit[0] = 1, bit[2] = 1, bit[3] = 1, and bit[4] of this command = 0, all protections are disabled

FREQUENCY_SWITCH_R1 (33h)

The FREQUENCY_SWITCH_R1 command on Page 0 sets the rail 1 switching frequency (f_{SW}). f_{SW} can be set between 200kHz and 5.11MHz, with 10kHz per step.

Command	FREQUENCY_SWITCH_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	FREQUENCY_SWITCH_R1								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	FREQUENCY_SWITCH_R1	Sets the switching frequency (f_{SW}) in direct format. 10kHz/LSB.

MFR_OSR_SET_R1 (34h)

The MFR_OSR_SET_R1 command on Page 0 sets the overshoot reduction (OSR) parameters for rail 1.

Command	MFR_OSR_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				MFR_OSR_FILTER_R1						MFR_OSR_BLANKTIME_R1						

Bits	Bit Name	Description
15	DBG_WD	Fixed to 1.
14	RESERVED	Fixed to 0.
13	MFR_OSR_EN_R1	Enables overshoot reduction (OSR). This function can reduce the V_{OUT} overshoot when the load is released. 1'b0: Disabled 1'b1: Enabled
12:7	MFR_OSR_FILTER_R1	Sets the minimum OSR duration time. 5ns/LSB.
6:0	MFR_OSR_ BLANKTIME_R1	Sets the blanking time between two effective OSR events. 10ns/LSB.

VIN_ON (35h)

The VIN_ON command on Page 0 sets the V_{IN} under-voltage lockout (UVLO) rising threshold.

Command	VIN_ON															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	VIN_ON									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VIN_ON	Sets the V_{IN} under-voltage lockout (UVLO) rising threshold. 31.25mV/LSB.

VIN_OFF (36h)

The VIN_OFF command on Page 0 sets the V_{IN} under-voltage lockout (UVLO) falling threshold.

Command	VIN_OFF															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	VIN_OFF									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VIN_OFF	Sets the V_{IN} under-voltage lockout (UVLO) falling threshold. 31.25mV/LSB.

MFR_SLOPE_SW_INI_R1 (37h)

The MFR_SLOPE_SW_INI_R1 command on Page 0 sets rail 1's initial ramp for soft start.

Command	MFR_SLOPE_SW_INI_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	MFR_VOUT_FINE_TUNE_R1						MFR_SLOPE_SW_INI_R1						

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	MFR_VOUT_FINE_TUNE_R1	Sets the V_{OUT} fine-tune value. The trim value is per step. Bit[12] is the signed bit. 0.64mV/LSB when V_{DIFF} gain = 1 0.96mV/LSB when V_{DIFF} gain = 1/2
6:0	MFR_SLOPE_SW_INI_R1	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_DCM_R1 (38h)

The MFR_SLOPE_SR_DCM_R1 command on Page 0 sets the rail 1 slope compensation slew rate in 1-phase DCM. Slope compensation provides noise immunity for PWM generation stabilizes the PWM switches on the MP2927. Slope compensation is generated by a PMBus-configurable current source and a PMBus-configurable capacitor. The MP2927 provides slope voltage configurations for all phases.

Command	MFR_SLOPE_SR_DCM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_1P_R1 (39h)

The MFR_SLOPE_SR_1P_R1 command on Page 0 provides 2 bytes to configure slope compensation for 1-phase CCM. It is for rail 1 only.

Command	MFR_SLOPE_SR_1P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_2P_R1 (3Ah)

The MFR_SLOPE_SR_2P_R1 command on Page 0 provides 2 bytes to configure slope compensation for 2-phase CCM. It is for rail 1 only.

Command	MFR_SLOPE_SR_2P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_3P_R1 (3Bh)

The MFR_SLOPE_SR_3P_R1 command on Page 0 provides 2 bytes to configure slope compensation for 3-phase CCM. It is for rail 1 only.

Command	MFR_SLOPE_SR_3P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_4P_R1 (3Ch)

The MFR_SLOPE_SR_4P_R1 command on Page 0 provides 2 bytes to configure slope compensation for 4-phase CCM. It is for rail 1 only.

Command	MFR_SLOPE_SR_4P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_5P_R1 (3Dh)

The MFR_SLOPE_SR_5P_R1 command on Page 0 provides 2 bytes to configure slope compensation for 5-phase CCM. It is for rail 1 only.

Command	MFR_SLOPE_SR_5P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_VRHOT_SET_R1 (3Eh)

The MFR_VRHOT_SET_R1 command on Page 0 sets the parameters of VRHOT.

Command	MFR_VRHOT_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X			MFR_VRHOT_LIMIT_R1							

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	MFR_VRHOT_MODE	Fixed to 1.
8	MFR_VRHOT_EN_R1	Enables VR HOT. 1'b0: Disabled 1'b1: Enabled
7:0	MFR_VRHOT_LIMIT_R1	Set the VR over-temperature (OT) alert threshold. If the sensed temperature via the TSENSE pin exceeds this threshold, OCP_L from the GPIO pins asserts to alert the system. 1°C/LSB.

MFR_IDRP_AC_SET (3Fh)

The MFR_IDRP_AC_SET command on Page 0 sets the AC droop parameters.

Command	MFR_IDRP_AC_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					RCDROOP					TAU1				TAU2		

Bits	Bit Name	Description
15:12	RESERVED	Fixed to 0.
11:8	RCDROOP	Set the rail 1 R_{CDROOP}. 100Ω/LSB.
7	FILTER_SIGN_BIT	Selects the filter 1 type. The detailed parameter is determined by bits[6:4] of this command. 1'b0: Fast filter 1'b1: Slow filter

6:4	TAU1	If bit[7] = 0: Tau = (7 - bits[6:4]) x 20ns If bit[7] = 1: Tau= (7 - bits[6:4]) x 4μs
3	FILTER_SIGN_BIT	Selects the filter 2 type. The detailed parameter is determined by bits[2:0] of this command. 1'b0: Fast filter 1'b1: Slow filter
2:0	TAU2	If bit[3] = 0: Tau = (7 - bits[2:0]) x 20ns If bit[3] = 1: Tau= (7 - bits[2:0]) x 4μs

VOUT_OV_FAULT_LIMIT_R1 (40h)

The VOUT_OV_FAULT_LIMIT_R1 command on Page 0 sets the V_{OUT} over-voltage protection (OVP) threshold.

Command	VOUT_OV_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X				OVP_ABS_SET_R1							

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	OVP_VID_SET_R1	Sets the over-voltage protection (OVP) VID threshold. 3'b001: V_{REF} + 200mV 3'b010: V_{REF} + 325mV 3'b100: V_{REF} + 450mV Others: Invalid
7:0	OVP_ABS_SET_R1	Sets an absolute OVP threshold. If V_{OUT} exceeds this value, OVP occurs. 10mV/LSB.

VOUT_OV_FAULT_RESPONSE_R1 (41h)

The VOUT_OV_FAULT_RESPONSE_R1 command on Page 0 sets the protection mode and delay time if a V_{OUT} over-voltage (OV) fault occurs.

Command	VOUT_OV_FAULT_RESPONSE_R1															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X				MFR_OVP_VID_DELAYTIME_R1					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OVP_ABS_EN_R1	1'b0: Disabled 1'b1: Enabled
7:6	MFR_OVP_VID_MODE_R1	Set the over-voltage (OV) fault mode. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	MFR_OVP_VID_ DELAYTIME_R1	Sets the VID OVP blanking time. If a VID OVP condition stays for more than the OVP_VID blanking time, a VID OVP fault occurs. 100ns/LSB.

VOUT_MAX_ALERT_R1 (42h)

The VOUT_MAX_ALERT_R1 command on Page 0 sets the V_{OUT} over-voltage (OV) warning threshold or returns the maximum V_{OUT} for rail 1. The function is determined by GPIO_ACTIVE (68h), bit[13].

Command	VOUT_MAX_ALERT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_MAX_ALERT_R1															

Bits	Bit Name	Description
15:0	VOUT_MAX_ALERT_R1	If GPIO_ACTIVE (68h) bit[13] set to 0, this command sets the V_{OUT} over-voltage (OV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] set to 1, this command returns the maximum V_{OUT}. The maximum value can be written with a lower value, and if a higher V_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x0000 to reset this command. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 0), bit[10].

VOUT_MIN_ALERT_R1 (43h)

The VOUT_MIN_ALERT_R1 command on Page 0 sets the V_{OUT} under-voltage (UV) warning threshold or returns the minimum V_{OUT} for rail 1. The function is determined by GPIO_ACTIVE (68h), bit[13].

Command	VOUT_MIN_ALERT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_MIN_ALERT_R1															

Bits	Bit Name	Description
15:0	VOUT_MIN_ALERT_R1	If GPIO_ACTIVE (68h) bit[13] set to 0, this command sets the V_{OUT} under-voltage (UV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] set to 1, this command returns the minimum V_{OUT}. This command can be written with a higher value, and if a lower V_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x03FF to reset this command. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 0), bit[10].

VOUT_UV_FAULT_LIMIT_R1 (44h)

The VOUT_UV_FAULT_LIMIT_R1 command on Page 0 sets the V_{OUT} under-voltage (UV) fault threshold.

Command	VOUT_UV_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

10:8	UVP_VID_SET_R1	Sets the under-voltage protection (UVP) threshold. 3'b000: V_{REF} - 425mV 3'b001: V_{REF} - 375mV 3'b010: V_{REF} - 325mV 3'b011: V_{REF} - 275mV 3'b100: V_{REF} - 225mV 3'b101: V_{REF} - 175mV 3'b110: V_{REF} - 125mV 3'b111: V_{REF} - 75mV
7:0	RESERVED	Fixed to 0.

VOUT_UV_FAULT_RESPONSE_R1 (45h)

The VOUT_UV_FAULT_RESPONSE_R1 on Page 0 sets the V_{OUT} under-voltage (UV) fault response.

Command	VOUT_UV_FAULT_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_UV_VID_EN_R1	Enables VID under-voltage protection (UVP). 1'b0: Disabled 1'b1: Enabled
7:6	MFR_UVP_MODE_R1	Sets the V_{OUT} UVP mode. 2'b00: No action 2'b01: Latch off mode 2'b10: Hiccup mode 2'b11: Retry 6 times
5:0	MFR_UVP_ DELAYTIME_R1	Sets the V_{OUT} UVP blanking time. A UVP fault occurs if the sensed V_{DIFF} falls below the UVP threshold for the UVP blanking time. 100ns/LSB.

IOUT_OC_FAULT_LIMIT_R1(46h)

The IOUT_OC_FAULT_LIMIT_R1 command on Page 0 sets the I_{OUT} over-current (OC) fault threshold.

Command	IOUT_OC_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	OCP_SPIKE_SET_R1	Sets the rail 1 OCP_SPIKE_TOTAL current-level DAC value. 6.25mV/LSB. OVP_SPIKE_TOTAL can be calculated with the following equation: $OCP\_SPIKE\_TOTAL = OCP\_SPIKE \times K_{CS} \times G_{IMON} \times R_{IMON} / 6.25$
7:0	OCP_TDC_SET_R1	Sets the rail 1 OCP_TDC_TOTAL current level. The high 8MSB of the IMON ADC result IMON1_SENSE, bits[9:0] is compared to this value. OCP_TDC_TOTAL can be calculated with the following equation: $OCP\_TDC\_TOTAL = OCP\_TDC \times K_{CS} \times G_{IMON} \times R_{IMON} / 6.25$

IOUT_OC_FAULT_RESPONSE_R1 (47h)

The IOUT_OC_FUALT_RESPONSE_R1 command on Page 1 sets the rail 1 over-current protection (OCP) options and values.

Command	IOUT_OC_FAULT_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									MFR_OCPTDC_TRIG_DELAY_R1							

Bits	Bit Name	Description
15:14	MFR_OCP_MODE_R1	Selects the over-current protection (OCP) mode for both OCP_TDC and OCP_SPIKE. 2'b00: No action 2'b01: Latch off mode 2'b10: Hiccup mode 2'b11: Retry six times
13	MFR_OCP_TDC_EN_R1	Enables OCP_TDC. 1'b0: Disabled 1'b1: Enabled
12:8	MFR_OCPTDC_ ACTION_DELAY_R1	Sets the OCP_TDC fault action time. This is the delay between OCP_L signal assertion and current limiting, hiccup mode entry, or shutdown. 1µs/LSB.
7:0	MFR_OCPTDC_ TRIG_DELAY_R1	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for the OCP_TDC blanking time. 20µs/LSB.

IOUT_OC_SPIKE_RESPONSE_R1 (48h)

The IOUT_OC_SPIKE_RESPONSE_R1 command on Page 0 sets the over-current (OC) spike options and values.

Command	IOUT_OC_SPIKE_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	MFR_OCCMP_SEL	Selects the over-current protection (OCP) mode. 1'b0: OCP_TDC used the digital comparator for OCP_TDC 1'b1: OCP_TDC uses the analog comparator for OCP_SPIKE. In this mode, OCP_SPIKE should be disabled.
8	MFR_OCP_SPIKE_EN_R1	Enables OCP_SPIKE. 1'b0: Disabled 1'b1: Enabled
7:4	MFR_OCPSPIKE_ ACTIONDELAY_R1	Sets the OCP_SPIKE fault action delay time. This is time is between OCP_L assertion (after exceeding current threshold relative to IDDSpike) and current limiting, hiccup mode entry, or shutdown. 1µs/LSB.
3:0	MFR_OCPSPIKE_ TRIGDELAY_R1	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for an OCP_SPIKE blanking time. 200ns/LSB.

MFR_OCP_PHASE_LIMIT_R1 (49h)

The MFR_OCP_PHASE_LIMIT_R1 command on Page 0 sets the rail 1 per-phase valley current limit. The MP2927 provides OCP_PHASE protection to limit the per-phase valley current. OCP_PHASE is implemented by monitoring and comparing the cycle-by-cycle sensed CS current with a current reference.

Command	MFR_OCP_PHASE_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									OCP_DAC_SET_R1							

Bits	Bit Name	Description
15:8	RESERVED	Unused. Fixed to 0.
7:0	OCP_DAC_SET_R1	Sets the per-phase valley current limit DAC value. 5mV/LSB.

IOUT_MAX_ALERT_R1 (4Ah)

The IOUT_MAX_ALERT_R1 command on Page 0 sets the I_{OUT} over-current (OC) warning threshold or returns the peak value of I_{OUT}. It is for rail 1 only. It is determined by GPIO_ACTIVE (68h), bit[13].

Command	IOUT_MAX_ALERT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IOUT_MAX_ALERT_R1															

Bits	Bit Name	Description
15:0	IOUT_MAX_ALERT_R1	If GPIO_ACTIVE (68h) bit[13] set to 0, this command sets the DAC value for the I_{OUT} over-current (OC) warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h) bit[13] set to 1, this command returns the peak I_{OUT} value. I_{OUT} can be written with a lower value, and if a higher I_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x0000 to reset the command. Convert the read value to the actual I_{OUT} (in A) with the following equation: $$I_{OUT}(A) = \frac{4Ah,bits[9:0]}{6Ch,bits[9:0] \times 1024} \times 6Eh,bits[10:0] \times 2^{(6\text{-GAIN\_SEL})}$$ Where GAIN_SEL is set by 6Ch, bits[11:10].

MFR_FS_LIMIT_12P_R1 (4Bh)

The MFR_FS_LIMIT_12P_R1 command on Page 0 sets the rail 1 FS_LIMIT threshold for 1-phase and 2-phase operation to detect fast load insertion and exit phase-shedding.

Command	MFR_FS_LIMIT_12P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_FS_LIMIT_2P_R1								MFR_FS_LIMIT_1P_R1							

Bits	Bit Name	Description
15:8	MFR_FS_LIMIT_2P_R1	Sets the exit phase-shedding PWM interval time for 2-phase operation. If the time interval between two phases is shorter than FS_LIMIT_2P, add + 1 to the interval. 5ns/LSB.
7:0	MFR_FS_LIMIT_1P_R1	Set the PWM1 off-time threshold to exit phase-shedding. If the PWM1 off time (after excluding MIN_OFF_TIME) is shorter than FS_LIMIT_1P, add + 1 to the count. It is effective both for DCM and CCM. 10ns/LSB.

MFR_FS_LIMIT_34P_R1 (4Ch)

The MFR_FS_LIMIT_34P_R1 command on Page 0 sets the rail 1 FS_LIMIT threshold for 3-phase and 4-phase operation to detect fast load insertion and exit phase-shedding.

Command	MFR_FS_LIMIT_34P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_FS_LIMIT_4P_R1								MFR_FS_LIMIT_3P_R1							

Bits	Bit Name	Description
15:8	MFR_FS_LIMIT_4P_R1	Sets the exit phase-shedding PWM interval time for 4-phase operation. If the time interval between two phases is shorter than FS_LIMIT_4P, add + 1 to the interval. 5ns/LSB.
7:0	MFR_FS_LIMIT_3P_R1	Sets the exit phase-shedding PWM interval time for 3-phase operation. If the time interval between two phases is shorter than FS_LIMIT_3P, add + 1 to the interval. 5ns/LSB.

MFR_APS_LEVEL_12P_R1 (4Dh)

The MFR_APS_LEVEL_12P_R1command on Page 0 sets the rail 1 automatic phase-shedding (APS) current threshold for 1-phase CCM and 1-phase DCM operation.

Command	MFR_APS_LEVEL_12P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_LEVEL_1P_CCM_R1								DROP_LEVEL_1P_DCM_R1							

Bits	Bit Name	Description
15:8	DROP_LEVEL_1P_CCM_R1	Sets the rail 1 automatic phase-shedding (APS) current threshold for 1-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_1P_DCM_R1	Sets the rail 1 APS current threshold for 1-phase DCM. 1A/LSB.

MFR_APS_LEVEL_23P_R1 (4Eh)

The MFR_APS_LEVEL_23P_R1 command on Page 0 sets the rail 1 automatic phase-shedding (APS) current threshold for 2-phase CCM and 3-phase CCM.

Command	MFR_APS_LEVEL_23P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	DROP_LEVEL_3P	Sets the rail 1 automatic phase-shedding (APS) current threshold for 3-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_2P	Sets the rail 1 APS current threshold for 2-phase CCM. 1A/LSB.

OT_FAULT_LIMIT_R1 (4Fh)

The OT_FAULT_LIMIT_R1 command on Page 0 sets the over-temperature protection (OTP) fault operation and values.

Command	OT_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X		MFR_OTP_HYS						MFR_OTP_LIMIT_R1							

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	MFR_OTP_MODE	Sets the over-temperature protection (OTP) mode. 1'b0: Latch-off mode 1'b1: Retry
13:8	MFR_OTP_HYS	Sets the temperature hysteresis for the OTP threshold. If the junction temperature monitored on the TSENS pin drops below OTP_LIMIT-OTP_HYS, the PWM initiates a soft starts as it would start a normal start-up sequence. 1°C/LSB.
7:0	MFR_OTP_LIMIT_R1	Sets the VR OTP fault limit. When the junction temperature monitored on the TSENSE pin exceeds OTP_LIMIT, the VR shuts off the disabled output. 1°C/LSB.

MFR_CORE_OTP_SET (50h)

The MFR_CORE_OTP_SET command on Page 0 sets the chip's over-temperature protection (OTP) fault operation and values.

Command	MFR_CORE_OTP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			MFR_CORE_OTP_HYS						MFR_CORE_OTP_LIMIT							

Bits	Bit Name	Description
15	MFR_CORE_OTP_RES	Fixed to 0.
14	MFR_CORE_OTP_ MODE	Sets the chip over-temperature protection (OTP) mode. 1'b0: Latch off 1'b1: Retry
13:8	MFR_CORE_OTP_HYS	Set the temperature hysteresis for the OTP threshold. If the junction temperature monitored on the TSENS pin drops below OTP_LIMIT-OTP_HYS, the PWM initiates a soft start as it would start a normal start-up sequence. 1°C/LSB.
7:0	MFR_CORE_OTP_LIMIT	Controller OTP fault limit setting. When the junction temperature monitored on TSENS pin exceeds OTP_LIMIT, the VR shuts off the disabled output. 1°C/LSB.

MFR_FS_DETECT_R1 (51h)

The MFR_FS_DETECT_R1 command on Page 0 sets rail 1 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_FS_DETECT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables the device to exit phase-shedding according to the PWM1 off time. The PWM minimum off time is excluded from PWM off time (see Figure 24). 1'b0: Disabled 1'b1: Enabled
10	FS_EXIT_APS_EN_NP	Enables the device to exit phase-shedding according to the multi-phase PWM interval time between consecutive phases. The time threshold is set by 4Bh on Page 0. The PWM blanking time is excluded from the PWM interval time (see Figure 25). 1'b0: Disabled 1'b1: Enabled
9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count for the PWM1 off-time condition to exit phase-shedding. Once the PWM off-time condition reaches the counting threshold, the controller exits APS immediately.
6:3	RETURN_APS_DELAY	Sets the minimum full-phase runtime after exiting APS due to an FS limit event. 20μs/LSB.
2:0	FS_EXIT_APS_CNT_NP	Sets the continuous count of the multi-phase PWMs interval time to exit phase-shedding. Once the PWMs interval condition reaches the counting threshold, the controller exits APS immediately.

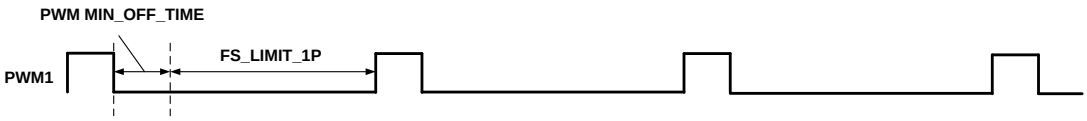


Figure 24: FS_LIMIT_1P Condition during 1-Phase Operation

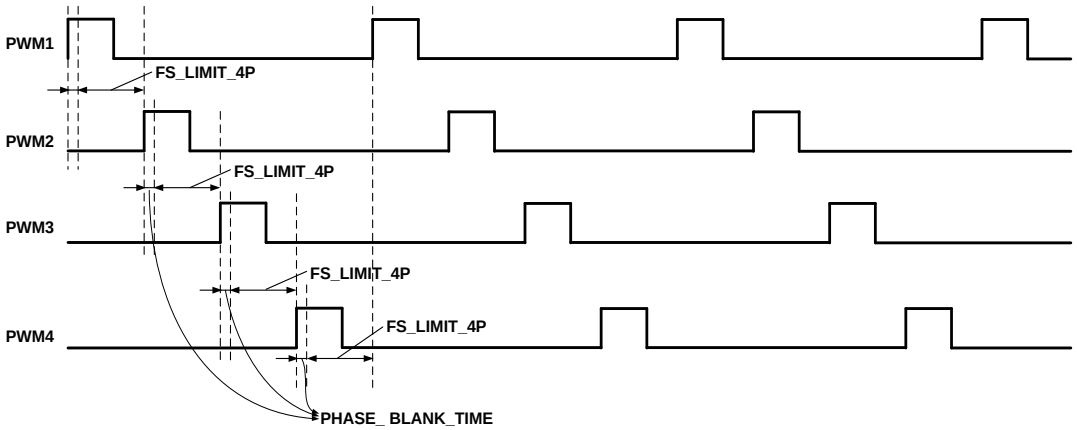


Figure 25: FS_LIMIT_NP Condition during N-Phase Operation (N = 4)

MFR_APS_CTRL_R1 (52h)

The MFR_APS_CTRL_R1 command on Page 0 sets rail 1 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									MFR_PS_ENTER_TIME_R1							

Bits	Bit Name	Description
15:12	MFR_ADP_OC_nPS_ EXIT_CNT_R1	Sets the period delay count from when OCP_PHASE is triggered to when the device exits automatic phase-shedding (APS). 100ns/LSB.
11	MFR_ADP_OC_ nPS_EXIT_EN_R1	Enables OCP_PHASE protection to make the device exit APS at any power state. 1'b0: Disabled 1'b1: Enabled
10	MFR_ADP_PFM_ EXIT_EN_R1	Enables the device to exit APS under a rail 1 increasing frequency condition. 1'b0: Disabled 1'b1: Enabled
9	MFR_ADP_OC_ 1PS_EXIT_EN_R1	Enables OCP_PHASE protection to force the device to exit APS during 1-phase DCM/CCM only. Then the device runs with full-phase operation. 1'b0: Disabled 1'b1: Enabled
8	MFR_ADP_UV_ EXIT_EN_R1	Sets rail 1 to enter full-phase operation if V_{FB} < VID - 25mV. 1'b0: Disabled 1'b1: Enabled
7:2	MFR_PS_ENTER_TIME_R1	Sets the phase-shedding delay time. When the reported load current is consecutively below the APS threshold for a time calculated with APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE, the controller enters APS mode and automatically sheds phases according to the load current.
1	MFR_PHASHED_ EXIT_MOD_R1	Set the phase dropping mode for phase-shedding. Phase-shedding may be caused by APS. 1'b0: Drop to the target phase count immediately 1'b1: Shed phases one by one with a configured delay time. The delay time is set by MFR_PS_INTERVAL_R1 (54h), bits[10:7]
0	MFR_AUTO_PS_EN_R1	Enables rail 1 APS mode. 1'b0: Disabled 1'b1: Enabled

MFR_APS_CTRL2_R1 (53h)

The MFR_APS_CTRL2_R1 command on Page 0 sets rail 1 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL2_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	APS_COMP_CNT						APS_COMP_LEVEL				MFR_APS_HYS			

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:9	APS_COMP_CNT	The MP2927 provides positive compensation on V_{REF} during phase-shedding to reduce undershoot. Phase-shedding may be due to APS. V_{REF} compensation is implemented by adding a PMBus-configurable positive voltage on COMP of the DC loop. After phase-shedding starts, the voltage returns 0V step by step with a set time interval. The time interval between each step is set by APS_COMP_CNT. 50ns/LSB.
8	DECAY_COMP_EN	Enables V_{REF} compensation while exiting decay. The compensation voltage level and slew rate are the same as during APS compensation. 1'b0: Disabled 1'b1: Enabled
7:4	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce undershoot. Compensation is added to V_{REF} when phase-shedding begins. 1.37mV/LSB
3:0	MFR_APS_HYS	Sets the current hysteresis between phase-shedding and phase-adding. This prevents back-and-forth phase-shedding when APS is enabled. 1A/LSB.

MFR_APS_CTRL3_R1 (54h)

The MFR_APS_CTRL3_R1 command on Page 0 sets rail 1 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL3_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X					MFR_PRD_EXIT_APS_TIME_R1						

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:7	MFR_PS_INTERVAL_R1	Sets the phase-by-phase dropping time intervals. It is only effective when register 52h, bit[1] is set to 1. 2.5µs/LSB.
6:0	MFR_PRD_EXIT_APS_TIME_R1	Sets the period condition for the DC loop and current balance loop hold. If the absolute error between the set switching period and the real switching period ($\|t_S - t_{SET}\|$) is longer than MFR_PRD_EXIT_APS_TIME x 80ns, then the device holds the DC loop and current-balancing time for a given time. 80ns/LSB.

VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command on Page 0 sets the V_{IN} over-voltage protection (OVP) threshold. This register is in linear format. If the sensed V_{IN} exceeds the VIN_OV fault limit, the device shuts down immediately.

Command	VIN_OV_FAULT_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	VIN_OV_FAULT_LIMIT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VIN_OV_FAULT_LIMIT	Sets the V_{IN} over-voltage protection (OVP) threshold. 31.25mV/LSB.

MFR_FSCB_LOOP_CTRL_R1 (56h)

The MFR_FSCB_LOOP_CTRL_R1 command on Page 0 sets the rail 1 f_{SW} and current balance loop.

Command	MFR_FSCB_LOOP_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	FS_LOOP_EN_R1	Enables the f_{SW} loop. The frequency loop keeps f_{SW} constant, and ensures it equals the set value different V_{IN} and load current values. This bit active for all rails. 1'b0: Disabled 1'b1: Enabled
14	TRANS_HOLD_ FS_EN_R1	Enables the device to maintain frequency loop and CB loop regulation when a load transient event is detected (e.g. V_{FB} exceeds the VFB+ window or VFB- window). 1'b0: Disabled 1'b1: Enabled
13	PS_HOLD_FS_EN_R1	Enables the device to hold frequency loop regulation when the phase count changes. 1'b0: Disabled 1'b1: Enabled
12	DVID_HOLD_FS_ EN_R1	Enables the device to hold frequency loop regulation when DVID occurs. 1'b0: Disabled 1'b1: Enabled
11:8	MFR_FS_LOOP_CNT_ R1	Sets the minimum hold time for the frequency loop when any of load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set. 100μs/LSB.
7	MFR_CB_EN_R1	Enables the current balance loop. 1'b1: Enabled 1'b0: Disabled
6	PRD_HOLD_CB_EN_R1	Enables the device to hold the current balance loop when the PWM period meets the PWM switching period condition set via PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disabled 1'b1: Enabled
5	PS_HOLD_CB_EN_R1	Enables the device to hold the current balance loop when the phase number changes. 1'b0: Disabled 1'b1: Enabled
4	DVID_HOLD_CB_EN_R1	Enables the device to hold the current balance loop when DVID occurs. 1'b0: Disabled 1'b1: Enabled
3:0	MFR_DYM_FLT_CNT_ R1	Sets the current balance loop hold time. When any load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set, the current balance loop stops regulating for a time set via CB_LOOP_THOLD. 100μs/LSB.

MFR_VOUT_LOOP_CTRL_R1 (57h)

The MFR_VOUT_LOOP_CTRL_R1 command on Page 0 set the rail 1 V_{OUT} loop parameters.

Command	MFR_VOUT_LOOP_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	MFR_VDIFF_GAIN_SEL_R1	Selects the V_{DIFF} gain. When V_{OUT} exceeds 1.6V (the maximum sampling range of the internal ADC), select 1/2x gain so that V_{OUT} can be as high as 3.2V. 1'b0: 1x 1'b1: 1/2x
9	MFR_DC_REF_SEL_R1	Sets the V_{OUT} DC loop sensing point. 1'b0: V_{FB} 1'b1: V_{DIFF}
8	MFR_VCAL_PS2_EN_R1	Enables DC loop calibration in DCM. 1'b0: Disabled 1'b1: Enabled
7	MFR_VCAL_EN_R1	Enables DC loop calibration for DCM and CCM. 1'b0: Disabled 1'b1: Enabled
6	PRD_HOLD_DC_EN_R1	Enables the device to hold the DC loop when the PWM time interval meets PWM switching period condition set via PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disabled 1'b1: Enabled
5	PS_HOLD_DC_EN_R1	Enables the device to hold the DC loop when the phase count changes. 1'b0: Disabled 1'b1: Enabled
4	TRANS_HOLD_DC_EN_R1	Enables the device to hold DC loop regulation when a load transient event is detected (e.g. V_{FB} exceeds the VFB+ window or VFB- window). 1'b0: Disabled 1'b1: Enabled
3:0	MFR_DC_LOOP_CNT_R1	Sets the DC loop's minimum hold time in direct format. 200μs/LSB with a +100μs offset.

JOUT_SHORT_PK_R1 (58h)

The JOUT_SHORT_PK_R1 command on Page 0 returns the peak J_{OUT} value in every SHORT_TERM period.

Command	JOUT_SHORT_PK_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	JOUT_SHORT_PK_R1															

Bits	Bit Name	Description
15:0	JOUT_SHORT_PK_R1	Returns the peak J_{OUT} value in every SHORT_TERM when J_{OUT} is enabled and GPIO_ACTIVE (68h), bit[13] is set to1. If J_{OUT} is disabled or GPIO_ACTIVE (68h), bit[13] is set to 0, this command returns the preset value.

JOUT_LONG_PK_R1(59h)

The JOUT_LONG_PK_R1 command on Page 0 returns the peak J_{OUT} value in every LONG_TERM period.

Command	JOUT_LONG_PK_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	JOUT_LONG_PK_R1															

Bits	Bit Name	Description
15:0	JOUT_LONG_PK_R1	Returns the peak J_{OUT} value in every LONG_TERM when J_{OUT} is enabled and GPIO_ACTIVE (68h), bit[13] is set to1. If J_{OUT} is disabled or GPIO_ACTIVE (68h), bit[13] is set to 0, this command returns the preset value.

MFR_SLOPE_CNT_1P_R1 (5Ah)

The MFR_SLOPE_CNT_1P_R1 command on Page 0 sets the rail 1 slope voltage clamp time in 1-phase operation.

Command	MFR_SLOPE_CNT_1P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_1P_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	MFR_SLOPE_CNT_1P_R1	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_23P_R1 (5Bh)

The MFR_SLOPE_CNT_23P_R1 command on Page 0 sets the rail 1 slope voltage clamp time in 2-phase and 3-phase operation.

Command	MFR_SLOPE_CNT_23P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_SLOPE_CNT_3P_R1								MFR_SLOPE_CNT_2P_R1							

Bits	Bit Name	Description
15:8	MFR_SLOPE_CNT_3P_R1	Sets the slope voltage clamp time. 5ns/LSB.
7:0	MFR_SLOPE_CNT_2P_R1	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_45P_R1 (5Ch)

The MFR_SLOPE_CNT_45P_R1 command on Page 0 sets the rail 1 slope voltage clamp time in 4-phase and 5-phase operation.

Command	MFR_SLOPE_CNT_45P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_SLOPE_CNT_5P_R1								MFR_SLOPE_CNT_4P_R1							

Bits	Bit Name	Description
15:8	MFR_SLOPE_CNT_5P_R1	Sets the slope voltage clamp time. 5ns/LSB.
7:0	MFR_SLOPE_CNT_4P_R1	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_67P_R1 (5Dh)

The MFR_SLOPE_CNT_67P_R1 command on Page 0 sets the rail 1 slope voltage clamp time in 6-phase and 7-phase operation.

Command	MFR_SLOPE_CNT_67P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_SLOPE_CNT_7P_R1								MFR_SLOPE_CNT_6P_R1							

Bits	Bit Name	Description
15:8	MFR_SLOPE_CNT_7P_R1	Sets the slope voltage clamp time. 5ns/LSB.
7:0	MFR_SLOPE_CNT_6P_R1	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_DCM_R1 (5Eh)

The MFR_SLOPE_CNT_DCM_R1 command on Page 0 sets the rail 1 slope voltage clamp time in DCM.

Command	MFR_SLOPE_CNT_DCM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X		MFR_SLOPE_CNT_DCM_R1										

Bits	Bit Name	Description
15	RESERVED	Fixed to 0.
14	5P_CNT_MSB	The MSB for the 5-phase operation slope count.
13	4P_CNT_MSB	The MSB for the 4-phase operation slope count.
12	3P_CNT_MSB	The MSB for the 3-phase operation slope count.
11:10	2P_CNT_MSB	The MSB for the 2-phase operation slope count.
9:0	MFR_SLOPE_CNT_DCM_R1	Sets the slope voltage clamp time in DCM. 5ns/LSB.

MFR_PG_DELAY_R1 (5Fh)

The MFR_PG_DELAY_R1 command on Page 0 sets the delay time for power good (PG) on and off.

Command	MFR_PG_DELAY_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PGOFF_DELAY_R1						MFR_PGON_DELAY_R1									

Bits	Bit Name	Description
15:10	MFR_PGOFF_DELAY_R1	Sets the power good (PG) off delay time. 5µs/LSB.
9:0	MFR_PGON_DELAY_R1	Sets the PG on delay time. 5µs/LSB.

TON_DELAY_R1 (60h)

The TON_DELAY_R1 command on Page 0 sets the delay time from when system initialization ends to when rail 1 V_{REF} starts to boot up.

Command	TON_DELAY_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TON_DELAY_R1															

Bits	Bit Name	Description
15:0	TON_DELAY_R1	Sets the delay time from when system initialization ends to when V_{REF} boots up. 100µs/LSB.

TON_RISE_R1 (61h)

The TON_RISE_R1 command on Page 0 sets the rail 1 V_{REF} boot-up slew rate.

Command	TON_RISE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	TON_RISE_R1												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TON_RISE_R1	Sets the rail 1 boot-up slew rate in PMBus mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h), bit[15].

MFR_PWM_MIN_TIME1_R1 (62h)

The MFR_PWM_MIN_TIME1_R1 command on Page 0 sets the minimum pulse width when PWM is high, low, or in tri-state. It is for rail 1 only.

Command	MFR_PWM_MIN_TIME1_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	MFR_MIN_LOW_TIME_R1									MFR_MIN_HIZ_TIME_R1					

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	MFR_MIN_LOW_TIME_R1	Sets the minimum PWM low time. 10ns/LSB with a -5ns offset. The minimum PWM low time can be calculated with the following equation: (PWM_MIN_LOW_TIME x 10) ns
8:6	MFR_MINON_TIME_R1	Sets the minimum PWM high time. 10ns/LSB with a -5ns offset. The minimum PWM high time can be calculated with the following equation: (PWM_MIN_HIGH_TIME x 10) ns
5:0	MFR_MIN_HIZ_TIME_R1	Sets the minimum PWM tri-state time. 10ns/LSB with a -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: (PWM_MIN_TRI_TIME x 10) ns

MFR_PWM_MIN_TIME2_R1 (63h)

The MFR_PWM_MIN_TIME2_R1 command on Page 0 sets the PWM minimum off time and PWM on-pulse width when under-current protection (UCP) is triggered. It is for rail 1 only.

Command	MFR_PWM_MIN_TIME2_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	TON_LIMIT_TO_VCAL					X	X	X	X	MFR_MINOFF_TIME_R1				

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	TON_LIMIT_TO_VCAL	The DC loop can be held if the PWM period meets the condition set in MFR_FS (33h on Page 0). If the calculated PWM on time is shorter than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	MFR_ZCD_EN_R1	Enables rail 1 zero-current detection (ZCD). 1'b0: Disabled 1'b1: Enabled
8:5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4:0	MFR_MINOFF_TIME_R1	Sets the PWM minimum off time. 20ns/LSB with a 15ns offset. The PWM minimum off time can be calculated with the following equation: (PWM_MIN_OFF_TIME x 20 + 15) ns

TOFF_DELAY_R1 (64h)

The TOFF_DELAY_R1 command on Page 0 sets the rail 1 delay time from EN going low to V_{REF} starting the shutdown process on rail 1.

Command	TOFF_DELAY_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TOFF_DELAY_R1															

Bits	Bit Name	Description
15:0	TOFF_DELAY_R1	Sets the delay time from when EN goes low to V_{REF} shutdown. 100µs/LSB.

TOFF_FALL_R1 (65h)

The TOFF_FALL_R1 command on Page 0 sets the V_{REF} transition down slew rate after the device receives an OPERATION soft shutdown command for rail 1.

Command	TOFF_FALL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	TOFF_FALL_R1												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TOFF_FALL_R1	Sets the rail 1 OPERATION command soft shutdown slew rate in PMBus mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h), bit[15].

GPIO_SEL_GROUP1 (66h)

The GPIO_SEL_GROUP1 command on Page 0 selects different signals from the inputs of the mux for the PG pins.

Command	GPIO_SEL_GROUP1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		GPIO_PG1_SEL			GPIO_PG2_SEL											

Bits	Bit Name	Description
15	RESERVED	Fixed to 0.
14:12	GPIO_PG1_SEL	3’b000: PG1 is set to be PG1, PG2, and PG3 3’b001: PG1 is set to be PG2 and PG3 3’b010: PG1 is set to be PG1 and PG3 3’b011: PG1 is set to be PG3 3’b100: PG1 is set to be PG1 and PG2 3’b101: PG1 is set to be PG2 3’b110: PG1 is set to be PG1 3’b111: PG1 is set to be open-drain high
11:9	GPIO_PG2_SEL	3’b000: PG2 is set to be PG1, PG2, and PG3 3’b001: PG2 is set to be PG2 and PG3 3’b010: PG2 is set to be PG1 and PG3 3’b011: PG2 is set to be PG3 3’b100: PG2 is set to be PG1 and PG2 3’b101: PG2 is set to be PG2 3’b110: PG2 is set to be PG1 3’b111: PG2 is set to be open-drain high
8:0	RESERVED	Fixed to 0.

GPIO_SEL_GROUP2 (67h)

The GPIO_SEL_GROUP2 command on Page 0 sets the GPIO pin's function.

Command	GPIO_SEL_GROUP2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	RESERVED	Fixed to 0.
14:12	GPIO_PWM6_SEL	3'b000: The PWM6 pin is set to be PWM 3'b001: The PWM6 pin is set to be GND 3'b010: The PWM6 pin is set to be J_{OUT} short-term alert 3'b011: The PWM6 pin is set to be J_{OUT} long-term alert 3'b100: The PWM6 pin is set to be I_{OUT} max alert 3'b101: The PWM6 pin is set to be I_{OUT} min alert 3'b110: The PWM6 pin is set to be V_{OUT} max alert 3'b111: The PWM6 pin is set to be V_{OUT} min alert
11:0	RESERVED	Fixed to 0.

GPIO_MODE (68h)

The GPIO_MODE command on Page 0 sets the GPIO pin's output mode.

Command	GPIO_MODE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:7	RESERVED	Fixed to 0.
6	PWM8_TRI_STATE	Selects the PWM8 pin's output mode. 1'b0: Push-pull output 1'b1: Open-drain output
5	PWM7_TRI_STATE	Selects the PWM7 pin's output mode. 1'b0: Push-pull output 1'b1: Open-drain output
4	PWM6_TRI_STATE	Selects the PWM6 pin's output mode. 1'b0: Push-pull output 1'b1: Open-drain output
3:0	RESERVED	Fixed to 0.

MFR_TEMP_CAL_R1 (69h)

The MFR_TEMP_CAL_R1 command on Page 0 sets the TSENSE pin temperature-sense gain and offset.

Command	MFR_TEMP_CAL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_TEMP_GAIN_R1								MFR_TEMP_OFFSET_R1							

Bits	Bit Name	Description
15:8	MFR_TEMP_GAIN_R1	Sets the temperature-sense gain to transfer the voltage on the TSENSE pin to a direct temperature (in °C).
7:0	MFR_TEMP_OFFSET_R1	Sets the temperature-sense offset to convert the voltage on the TSENSE pin to a direct temperature (in °C). 1°C/LSB. Bit[7] is signed bit.

MFR_VOUT_CALC_R1 (6Ah)

The MFR_VOUT_CALC_R1 command on Page 0 sets the rail 1 gain and offset for the V_{OUT} calculation.

Command	MFR_VOUT_CALC_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	MFR_VOUT_CALC_OFFSET_R1						MFR_VOUT_CALC_GAIN_R1							

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:8	MFR_VOUT_CALC_OFFSET_R1	Adds an offset to the V_{OUT} report in register READ_VOUT (8Bh). This bit is for the rail 1 V_{OUT} report only. This bit is in two's complement format. Bit[13] is the signed bit. VID_STEP/LSB. When the VID_STEP is 6.25mV, the voltage list below shows the direct values and real-world values. 6'b00 0000: 0mV 6'b00 0001: +6.25mV 6'b01 1111: +193.75mV 6'b10 0000: -200mV 6'b10 0001: -193.75mV 6'b11 1111: -6.25mV
7:0	MFR_VOUT_CALC_GAIN_R1	Sets the gain from the ADC-sensed VOSEN - VORTN voltage to the PMBUS V_{OUT} report in register READ_VOUT (8Bh). This bit is for the rail 1 V_{OUT} report only.

MFR_IOUT_CAL_AVSBUS_R1 (6Bh)

The MFR_IOUT_CALC_AVSBUS_R1 command on Page 0 sets the rail 1 gain and offset for the AVSBus I_{OUT} report.

Command	MFR_IOUT_CAL_AVSBUS_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_IOUT_AVS_OS_R1					MFR_IOUT_AVS_GAIN_R1										

Bits	Bit Name	Description
15:11	MFR_IOUT_AVS_OS_R1	Bit[15] is the signed bit. 160mA/LSB.
10:0	MFR_IOUT_AVS_GAIN_R1	Sets the current-sense gain for the PMBus report. The gain can be calculated with the following equation: $$GAIN = \frac{1.6 \times 32 \times 10^{-3}}{1024 \times K_{CS} \times G_{IMON} \times R_{IMON}}$$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the internal IMON resistor (in Ω).

IOUT_CAL_GAIN_PMBUS_R1 (6Ch)

The IOUT_CAL_GAIN_PMBUS_R1 command on Page 0 sets the rail 1 gain for I_{OUT} reporting in PMBus mode. The MP2927 senses I_{OUT} by sensing the voltage of IMON. The reported I_{OUT} is returned with PMBus command READ_IOUT (8Ch on Page 0).

Command	IOUT_CAL_GAIN_PMBUS_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	GAIN_SEL		IOUT_CALC_GAIN_R1									

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:10	GAIN_SEL	Sets the exponent value for the IOUT_CAL_GAIN calculation equation in this command.
9:0	IOUT_CALC_GAIN_R1	Sets the current-sense gain for the PMBus report. The gain can be calculated with the following equation: $$IOUT\_CAL\_GAIN = \frac{1023}{1.6} \times K_{CS} \times G_{IMON} \times R_{IMON} \times 2^{(6-GAIN\_SEL)}$$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bits[11:10] of this command.

IOUT_CAL_OS_PMBUS_R1 (6Dh)

The IOUT_CAL_OS_PMBUS_R1 command on Page 0 sets the rail 1 offset for I_{OUT} reporting in PMBus mode. The MP2927 senses I_{OUT} by sensing the IMON voltage. The reported I_{OUT} is returned with PMBus command READ_IOUT (8Ch on Page 0).

Command	IOUT_CAL_OS_PMBUS_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	IOUT_CAL_PH_OFS_R1							IOUT_CALC_OFFSET_R1					

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:6	IOUT_CAL_PH_OFS_R1	Adds an offset according the phase number, where larger n corresponds with a larger offset. Bit[12] is signed bit.
5:0	IOUT_CALC_OFFSET_R1	Adds a current report offset to READ_IOUT (8Ch).

MFR_IMON_SET_R1 (6Eh)

The MFR_IMON_SET_R1 command on Page 0 sets certain configurations for the internal IMON sense in PMBus mode. It is rail 1 only.

Command	MFR_IMON_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						MFR_TRIM_IMON_DIGI_GAIN_R1										

Bits	Bit Name	Description
15:13	MFR_IMON_RES_SET_R1	Sets the rail 1 IMON resistor. 3'b 000: 2.5kΩ 3'b 001: 5kΩ 3'b 010: 10kΩ 3'b 011: 40kΩ 3'b1xx: No connection
12	MFR_IMON_GAIN_SET_R1	1'b0: The IMON1 current mirror gain is 1/8 1'b1: The IMON1 current mirror gain is 1/16
11	RESERVED	Fixed to 0.
10:0	MFR_TRIM_IMON_DIGI_GAIN_R1	Set the digital calculation gain for I_{OUT} reporting. The gain is multiplied by the IMON ADC-sensed valued and forms the final IMON digital-sense value. The IMON digital-sense value is used for PMBus I_{OUT} reporting. The final sensed IMON value can be calculated with the following equation: $IOUT\_PMBUS\_REPORT = 1023 \times \frac{I_{OUT} \times K_{CS} \times G_{IMON} \times R_{IMON}}{1.6} \times \frac{TRIM\_DIGI\_GAIN}{1024} \times \frac{2^{(6-GAIN\_SEL)}}{GAIN}$ Where I_{OUT} is the output current (in A), K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and TRIM_DIGI_GAIN is a decimal value.

IOUT_MIN_ALERT_R1 (6Fh)

The IOUT_MIN_ALERT_R1 command on Page 0 returns the minimum I_{OUT} or its preset value. This function is determined by GPIO_ACTIVE (68h), bit[13]. It is for rail 1 only.

Command	IOUT_MIN_ALERT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	IOUT_MIN_ALERT_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

9:0	IOUT_MIN_ALERT_R1	If GPIO_ACTIVE (68h), bit[13] is set to 0, then 6Fh sets the DAC value for the I_{OUT} OC warn threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h), bit[13] is set to 1, then 6Fh returns the minimum value of I_{OUT}. In this mode, it also can be written with a higher value. If a higher I_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x03FF to reset this command. Convert the read value to actual I_{OUT} (in A) with the following equation: $$I_{OUT}(A) = \frac{6Fh, bits[9:0]}{6Ch, bits[9:0] \times 1024} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$$ Where GAIN_SEL: 6Ch, bits[11:10].

MFR_PHASE_CFG (70h)

The MFR_PHASE_CFG command on Page 0 sets the phase configurations.

Command	MFR_PHASE_CFG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X						PHASE_NUM_CFG_R1			

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:7	PHASE_NUM_CFG_R3	Sets the rail 3 phase number.
6:4	PHASE_NUM_CFG_R2	Sets the rail 2 phase number.
3:0	PHASE_NUM_CFG_R1	Sets the rail 1 phase number.

MFR_PVID01_R1 (71h)

The MFR_PVID01_R1 command on Page 0 sets the rail 1 V_{BOOT}.

Command	MFR_PVID01_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID1_R1								MFR_PVID0_R1							

Bits	Bit Name	Description
15:8	MFR_PVID1_R1	Reserved.
7:0	MFR_PVID0_R1	Sets the rail 1 V_{BOOT}, when MFR_VR_CONFIG1 (C1h on Page 0), bit[13] is 1. It is VID format. VID_STEP/LSB.

MFR_PVID23_R1 (72h)

The MFR_PVID23_R1 command on Page 0 is reserved.

Command	MFR_PVID23_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID3_R1								MFR_PVID2_R1							

Bits	Bit Name	Description
15:8	MFR_PVID3_R1	Reserved.
7:0	MFR_PVID2_R1	Reserved.

MFR_PVID45_R1 (73h)

The MFR_PVID45_R1 command on Page 0 is reserved.

Command	MFR_PVID45_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID5_R1								MFR_PVID4_R1							

Bits	Bit Name	Description
15:8	MFR_PVID5_R1	Reserved.
7:0	MFR_PVID4_R1	Reserved.

MFR_PVID67_R1 (74h)

The MFR_PVID67_R1 command on Page 0 is reserved.

Command	MFR_PVID67_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID7_R1								MFR_PVID6_R1							

Bits	Bit Name	Description
15:8	MFR_PVID7_R1	Reserved.
7:0	MFR_PVID6_R1	Reserved.

SAMPLE_INTERVAL_12PH_R1 (75h)

The SAMPLE_INTERVAL_12P_R1 command on Page 0 sets the sample interval for 1-phase and 2-phase operation on rail 1.

Command	SAMPLE_INTERVAL_12PH_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			SAMPLE_INTERVAL_2PH_R1							SAMPLE_INTERVAL_1PH_R1						

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13:7	SAMPLE_INTERVAL_2PH_R1	Sets the 2-phase sample interval. 50ns/LSB.
6:0	SAMPLE_INTERVAL_1PH_R1	Sets the 1-phase sample interval. 50ns/LSB.

SAMPLE_INTERVAL_34PH_R1 (76h)

The SAMPLE_INTERVAL_34PH_R1 command Page 0 sets the sample interval for 3-phase and 4-phase operation on rail 1.

Command	SAMPLE_INTERVAL_34PH_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			SAMPLE_INTERVAL_4PH_R1							SAMPLE_INTERVAL_3PH_R1						

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13:7	SAMPLE_INTERVAL_4PH_R1	Sets the 2-phase sample interval. 50ns/LSB.
6:0	SAMPLE_INTERVAL_3PH_R1	Sets the 1-phase sample interval. 50ns/LSB.

MFR_ADDR_PMBUS (77h)

The MFR_ADDR_PMBUS command on Page 0 sets PMBus address.

Command	MFR_ADDR_PMBUS															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X		ADDR_MSB			ADDR_LSB			

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7	ADDR_CONFIG_MODE	Fixed to 1.
6:4	ADDR_MSB	Sets the 3MSB for the PMBus address. This value ranges between 0 and 7.
3:0	ADDR_LSB	Set the 4LSB for the PMBus address.

STATUS_BYTE (78h)

The STATUS_BYTE command on Page 0 returns 1 byte of information with a summary of the most critical statuses and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								X

Bits	Bit Name	Behavior	Description
7	NVM_BUSY	Live	Reports the live status of the NVM. 1'b0: The NVM is idle. NVM write and read with a PMBus command is available 1'b1: The NVM is busy. NVM write and read with a PMBus command is unavailable

6	OFF	Live	Indicates whether the rail 1 output is off. It asserts if the rail 1 output is off. The output may turn off if a protection occurs, EN goes low, or VID = 0. 1'b0: V_{OUT1} is on 1'b1: V_{OUT1} is off
5	VOUT_OV_FAULT	Latch	Indicates whether a rail 1 V_{OUT} over-voltage (OV) faul has occurred. If rail 1 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. This is for VID_OVP and ABS_OVP. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	Indicates whether a rail 1 I_{OUT} over-current (OC) fault has occurred. If rail 1 OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. This is for OCP_TDC and OCP_SPIKE. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
3	VIN_UV_FAULT	Latch	Indicates whether a V_{IN} under-voltage (UV) fault has occurred. If a V_{IN} UV fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	TEMPERATURE	Latch	Indicates whether an over-temperature (OT) fault or warning has occurred. If a TSENSE-related OTP or OT warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Latch	Indicates whether a PMBus communication fault has occurred. If a PMBus communications related fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	PROCHOT_FAULT	Latch	Indicates whether a PROCHOT fault has occurred. If the PROCHOT voltage exceeds or falls below the level set by MFR_PROCHOT_SET (36h on Page 1), bits[13:8], then a PROCHOT fault occurs and this bit is set and latched. The PROCHOT fault direction is determined by MFR_PROCHOT_SET (36h on Page 1), bit[1]. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No PROCHOT fault has occurred 1'b1: A PROCHOT fault has occurred

STATUS_WORD (79h)

The STATUS_WORD (79h) command on Page 0 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher byte gives more detailed information of the fault conditions. The lower byte shares the information with register STATUS_BYTE (78h).

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function						X	X		STATUS_BYTE (78h)							

Bits	Bit Name	Behavior	Description
15	VOUT	Live	Indicates whether a V_{OUT} over-voltage (OV) or under-voltage (UV) fault has occurred. If V_{OUT} OVP or UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} fault or warning has occurred 1'b1: A V_{OUT} fault or warning has occurred
14	IOUT	Live	Indicates whether a rail 1 I_{OUT} warning or a fault has occurred. If a rail 1 I_{OUT} fault or warning occurs, or if an output power (P_{OUT}) warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} fault or warning has occurred 1'b1: An I_{OUT} fault or warning has occurred
13	INPUT	Latch	Indicates whether a V_{IN} or I_{IN} fault or warning has occurred. If a V_{IN} or I_{IN} protection or warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} or I_{IN} fault or warning has occurred 1'b1: A V_{IN} or I_{IN} fault or warning has occurred
12	TEMP FAULT	Latch	Indicates whether a temperature-related fault has occurred. If the TSENSE pin voltage exceeds 2.2V or another temperature fault occurs, then this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No temp fault has occurred 1'b1: A temp fault has occurred
11	PG_NOT_ACTIVE	Live	1'b0: PG is active 1'b1: PG is not active
10:9	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
8	WATCH_DOG_OVF	Latch	Indicates whether the watchdog monitor block timer has overflowed. The monitor value calculation has a watchdog timer. If the timer overflows, then the monitor value calculation state machine and the timer are reset, and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 0 returns 1 byte of information with the detailed V_{OUT} fault and warning statuses on rail 1.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function						X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Indicates whether a rail 1 V_{OUT} has an over-voltage (OV) fault has occurred. If rail 1 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred

6	VOUT_OV_WARNING	Live	Indicates whether a rail 1 V_{OUT} over-voltage (OV) warning has occurred. If rail 1 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} OV warning has occurred 1'b1: A V_{OUT} OV warning has occurred
5	VOUT_UV_WARNING	Live	Indicates whether a rail 1 V_{OUT} has an under-voltage (UV) warning has occurred. If rail 1 UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} UV warning has occurred 1'b1: A V_{OUT} UV warning has occurred
4	VOUT_UV_FAULT	Latch	Indicates whether a rail 1 V_{OUT} has an under-voltage (UV) fault has occurred. If rail 1 UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN_ WARNING	Latch	Indicates whether a rail 1 V_{OUT} reaches VOUT_MAX or VOUT_MIN has occurred. If the VID value exceeds the value set by VOUT_MAX (24h on Page 0) and VOUT_MIN (2Bh on Page 0), then this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID exceeds VOUT_MAX or is below VOUT_MIN
2	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
1	LINE_FLOAT	Latch	Indicates whether rail 1 line-float protection has occurred. If a line-float fault is detected, the device shuts down the associated rails and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No line-float fault has occurred 1'b1: A line-float fault has occurred
0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 0 returns 1 byte of information with the detailed I_{OUT} fault and warning statuses on rail 1.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function				X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Indicates whether the rail 1 I_{OUT} has an over-current (OC) fault. If rail 1 OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. This is for OCP_TDC and OCP_SPIKE. 1'b0: No output OC fault 1'b1: An output OC fault has occurred

6	TDC_OCP_UV_FAULT	Latch	Indicates whether the rail 1 I_{OUT} has dual OC and under-voltage (UV) fault. If rail 1 OCP occurs while the UV comparator is set, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No dual OC and UV fault has occurred 1'b1: A dual OC and UV fault has occurred
5:0	RESERVED	/	Unused. X indicates that reads are always 0.

STATUS_INPUT (7Ch)

The STATUS_INPUT command on Page 0 returns 1 byte of information with detailed input fault and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	VIN_OVP	X	X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	VIN_OVP	Latch	Indicates whether a V_{IN} over-voltage (OV) fault has occurred. If V_{IN} exceeds the VIN_OV limit, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6:0	RESERVED	/	Unused. X indicates that reads are always 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command on Page 0 returns 1 byte of information with temperature-related fault and warning conditions.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		VRHOT	X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Indicates whether an over-temperature (OT) fault has occurred. If the temperature sensed via TSENSE exceeds the OT fault limit set by OT_FAULT_LIMIT (4F on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
6	VRHOT	Live	Indicates whether a VRHOT event has occurred. If the temperature sensed via TSENSE exceeds the OT warning limit set by MFR_VRHOT_SET (3Eh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No VRHOT event has occurred 1'b1: A VRHOT event has occurred
5:0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_CML (7Eh)

The STATUS_CML command on Page 0 returns 1 byte of information with PMBus communication related faults.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function					X			

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	Indicates whether the device received an invalid PMBus command. If the MP2927 receives an unsupported command code, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	INVALID_DATA	Latch	Indicates whether invalid PMBus data has been received. If the MP2927 receives unsupported data, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received
5	PEC_ERROR	Latch	Indicates whether a PMBus packet error checking (PEC) fault has occurred. The PMBus interface supports the use of the PEC byte that is defined in the SMBus standard. The PEC byte is transmitted by the MP2927 during a read transaction or sent to the MP2927 during a write transaction. If the PEC byte sent to the controller during a write is incorrect, then the command is not executed and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4	NVM_CRC_ERROR	Latch	Indicates whether a cyclic redundancy check (CRC) fault has occurred. While storing the operating memory data to the NVM, the MP2927 calculates a CRC code for each bit and saves the final CRC code to the NVM. While restoring the NVM data to the operating memory, the MP2927 recalculates the CRC code with each bit. The MP2927 checks the CRC results when the restoration process is done. If the CRC result does not match what is stored , the VR shuts down and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
3	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
2	CML_FLT_TRG	Latch	If NVM operation is blocked while the controller records a fault into the NVM, then this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No NVM operation is blocked 1'b1: NVM operation has been blocked while the controller records a fault to the NVM

1	CML_OTHER_FAULTS	Latch	If any of the faults listed below occur during PMBus communication, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1) Sending too few bits 2) Reading too few bits 3) Host sends or reads too few bytes 4) Reading too many bytes
0	NVM_SIG_FAULTS	Latch	While restoring data from the NVM to the memory, the device checks the signature register in address 00h of the NVM first. If the signature register is 0x1234, then the restoration process halts and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to clear the bit. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

READ_ADC_SUM (81h)

The READ_ADC_SUM command on Page 0 returns the sum of 16 consecutive ADC-sensed results.

Command	READ_ADC_SUM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X		ADC_SUM													

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	ADC_SUM_READY	Indicates whether 16 consecutive ADC-sensed results are ready. 1'b0: Not ready 1'b1: Ready
13:0	ADC_SUM	Stores the sum of 16 consecutive ADC-sensed results. Send FBh (0 byte) to start the ADC summing action.

READ_VFB1_SENSE (82h)

The READ_VFB1_SENSE command on Page 0 returns the ADC-sensed VFB1 voltage.

Command	READ_VFB1_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_VFB_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_VFB1_SENSE	Returns the ADC-sensed VFB1 voltage in direct format. 1.56mV/LSB.

READ_TSENSE_SENSE (83h)

The READ_TSENSE_SENSE command on Page 0 reads the TSENSE pin voltage.

Command	READ_TSENSE_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_TSENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_TSENSE	Return the ADC-sensed voltage on TSENSE in direct format. 1.56mV/LSB.

READ_CS1 (84h)

The READ_CS1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS1 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function							READ_CS1									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS1	Returns the ADC-sensed voltage on rail 1's CS1 in direct format. 3.125mV/LSB.

READ_CS2 (85h)

The READ_CS2 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS2 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function							READ_CS2									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS2	Returns the ADC-sensed voltage on rail 1's CS2 in direct format. 3.125mV/LSB.

READ_CS3 (86h)

The READ_CS3 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS3 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function							READ_CS3									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS3	Returns the ADC-sensed voltage on rail 1's CS3 in direct format. 3.125mV/LSB.

READ_CS4 (87h)

The READ_CS4 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS4 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function							READ_CS4									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS4	Returns the ADC-sensed voltage on rail 1's CS4 in direct format. 3.125mV/LSB.

READ_VIN (88h)

The READ_VIN command on Page 0 provides 2 bytes to return the sensed V_{IN} based on the VINSEN1 pin. In VID mode, the returned value must ignore the exponent value set by bits[15:11].

Command	READ_VIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	1	1	0	1	1	X	READ_VIN									

Bits	Bit Name	Description
15:11	EXP	Unused. Fixed to 11011.
10	RESERVED	Fixed to 0.
9:0	READ_VIN	Return the sensed input voltage in Linear11 format. 31.25mV/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 0 returns the sensed rail 1 VOSEN - VORTN voltage. Where K_R is the dividing ratio of the divider.

Command	READ_VOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	READ_VOUT											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT	Returns the V_{OUT} value. Linear mode: 2mV/LSB. V_{OUT} can be calculated with the following equation: V_{OUT} = READ_VOUT x 2 x K_R K_R is the dividing ratio of the divider. Direct mode: VID_STEP/LSB. V_{OUT} can be calculated with the following equation: V_{OUT} = READ_VOUT x VID_STEP x K_R. Where VID_STEP is determined by C1h, bits[15:14], and K_R is the dividing ratio of the divider.

READ_IOUT (8Ch)

The READ_IOUT command on Page 0 returns the sensed rail 1 I_{OUT}.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP					READ_IOUT										

Bits	Bit Name	Description
15:11	EXP	This value is determined by VR_CONFIG1 (C1h), bit[3]. 1: Select 5'b11110 0: Select 5'b11111
10:0	READ_IOUT	Returns the sensed I_{OUT}. Determined by VR_CONFIG1 (C1h), bit[3]. 1: 0.25A/LSB 0: 0.5A/LSB

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 0 returns the temperature sensed on the TSENSE pin.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	X	X	X	READ_TEMP							

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_TEMP	Returns the temperature sensed on the TSENSE pin. 1°C/LSB.

READ_VCOMP (8Fh)

The READ_VCOMP command on Page 0 returns the COMP value.

Command	READ_VCOMP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_VCOMP							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_VCOMP	Return the COMP value.

READ_POUT (96h)

The READ_POUT command on Page 0 returns the rail 1 output power (P_{OUT}).

Command	READ_POUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_POUT															

Bits	Bit Name	Description
15:0	READ_POUT	Returns the rail 1 P_{OUT}. The ADC read value is the same as the value from D1h. Convert the read value to actual power (in W) with the following equation: $P_{OUT}(W) = \frac{\frac{READ\_POUT \times 8}{6Ch, bits[9:0] \times 1000} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}}{t_{SHORT\_TERM}}$ Where GAIN_SEL is 6Ch, bits[11:10], and: G_{VIDFF} is the VDIFF gain setting by 57h, bit[10]. 57h, bit[10] = 0: G_{VDIFF} = 1 57h, bit[10] = 1: G_{VDIFF} = 0.5 t_{SHORT_TERM} is the short term (in µs): 26h, bit[15] = 0: t_{SHORT_TERM} = 26h, bits[12:1] x 0.05µs 26h, bit[15] = 1: t_{SHORT_TERM} = (26h, bits[6:0] + 1) x 4Eh (on Page 1), bits[13:8] x 0.05µs

PMBUS_REVISION (98h)

The PMBUS_REVISION command on Page 0 returns the revision of the PMBus to which the device is compliant.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	PMBUS_REVISION							

Byte	Byte Name	Byte
7:0	PMBUS_REVISION	Always returns 0x33. This means that theMP2927 supports PMBus revisions up to 1.3.

MFR_ID (99h)

The MFR_ID command on Page 0 returns the uniquely identifies for VR vendor. It is block read only.

Byte	Byte Name	Description
3	Character 3	Reads are always 0x4D. This represents “M.”
2	Character 2	Reads are always 0x50. This represents “P.”
1	Character 1	Reads are always 0x53. This represents “S.”

MFR_MODEL (9Ah)

The MFR_MODEL command on Page 0 returns the unique product identification. It is block read only.

Byte	Byte Name	Description
6	Character 6	Reads are always 0x4D, this represents “M”.
5	Character 5	Reads are always 0x50, this represents “P”.
4	Character 4	Reads are always 0x32, this represents “2”.
3	Character 3	Reads are always 0x39, this represents “9”.
2:1	Characters 2,1	XX. Defined by the 9Fh value.

MFR_REVISION (9Bh)

The MFR_REVISION command on Page 0 returns the silicon revision track number. It is block read only.

Byte	Byte Name	Description
1	Character 1	Returns the MP2927 product silicon revision tracking number.

MFR_DATE (9Dh)

The MFR_DATE command on Page 0 returns the part’s date of manufacture with ASCII format, i.e. “DDMMYY.” For example, if the date of manufacture is 2018-06-15, then the MFR_DATE is 0x31 35 30 36 31 38. It is block read only.

Byte	Byte Name	Description
6	Character 6	DD. Identifies the day that the part was manufactured.
5	Character 5	
4	Character 4	MM. Identifies the month that the part was manufactured.
3	Character 3	
2	Character 2	YY. Identifies the year that the part was manufactured.
1	Character 1	

MFR_PRODUCT_ID (9Fh)

MFR_PRODUCT_ID command on Page 0 returns the product ID.

Command	MFR_PRODUCT_ID															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PRODUCT_ID2								PRODUCT_ID1							

Byte	Byte Name	Description
2	PRODUCT_ID2	Always returns 0x32, which represents 2.
1	PRODUCT_ID1	Always returns 0x37, which represents 7.

MFR_VR_CONFIG1 (C1h)

The MFR_VR_CONFIG1 command on Page 0 sets basic functions for the MP2927.

Command	MFR_VR_CONFIG1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					0	0	0	0	1	0						

Bits	Bit Name	Description
15:14	VID_STEP	Sets the VID resolution. VID_STEP can be set to 6.25mV, 5mV, or 2mV in PMBus mode. 2'b00: 6.25mV 2'b01: 5mV 2'b1x: 2mV
13	VBOOT_SEL	Sets the boot-up voltage (V_{BOOT}). 1'b0: In PMBus mode, V_{BOOT} is set by VOUT_COMMAND (21h) 1'b1: In PMBus mode, V_{BOOT} is set by MFR_PVID (71h)
12	PG_FOR_VID=0V	Selects the PG state when DVID goes to 0V. 1'b0: High 1'b1: Low
11	PVID_PIN_EN	Fixed to 0.
10	PVID_EN_R3	Fixed to 0.
9	PVID_EN_R2	Fixed to 0.
8	PVID_EN_R1	Fixed to 0.
7	DBG_CRC	Sets the function for CRC_USER_LAST (76h on Page 2) (see page 189). 0: Option 1 1: Option 2
6	DEBUG_MODE_EN	Fixed to 0.
5	IOUT_REPORT_SEL_R3	Sets the PMBus report resolution for rail 3. 1'b0: 0.5A/LSB 1'b1: 0.25A/LSB
4	IOUT_REPORT_SEL_R2	Sets the PMBus report resolution for rail 2. 1'b0: 0.5A/LSB 1'b1: 0.25A/LSB
3	IOUT_REPORT_SEL_R1	Sets the PMBus report resolution for rail 1. 1'b0: 0.5A/LSB 1'b1: 0.25A/LSB
2	VIN_TON_CAL_MODE	Selects how the V_{IN} value is obtained to calculate t_{ON}. 1'b0: Update t_{ON} with READ_VIN (88h) 1'b1: Update t_{ON} with READ_VN (88h) exceeds 0.75V. If the V_{IN} changes but is below 0.75V, t_{ON} does not update
1	EN_OFF_MODE_SEL	Seta the EN shutdown mode. It is only effective in regular power mode. In low-power mode, EN always shuts the converter down with Hi-Z. 1'b 0: Hi-Z off 1'b 1: Soft shutdown
0	RESERVED	Fixed to 0.

MFR_VR_CONFIG2 (C2h)

The MFR_VR_CONFIG2 command on Page 0 sets some basic functions for the MP2927.

Command	MFR_VR_CONFIG2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	DRMOS_TYPE	Selects the DrMOS type. 1'b0: Voltage-sense DrMOS 1'b1: Current-sense DrMOS
14:13	HICCUP_TIME	Sets the hiccup time in retry mode if a protection occurs. 2'b00: 12.5ms 2'b01: 6ms 2'b10: 2ms 2'b11: 0.5ms
12	VR_TEMPER_ MERGE_EN	Selects the TSENS pin function. Fixed to 1.
11	DRMOS_FLT_ DETECT_EN_R3	Enables the PWM pin to act as a DrMOS fault type indicator and record the fault type to the EEPROM. It is for rail 3 only. For certain Intelli-Phase™ products, PWM can report the DrMOS fault type. When this function is enabled, the MP2927 monitors the voltage on the PWM pin to detect the fault type after the VR shuts down. 1'b0: Disabled 1'b1: Enabled
10	DRMOS_FLT_ DETECT_EN_R2	Enables the PWM pin to act as a DrMOS fault type indicator and record the fault type to the EEPROM. It is for rail 2 only. For certain Intelli-Phase™ products, PWM can report the DrMOS fault type. When this function is enabled, the MP2927 monitors the voltage on the PWM pin to detect the fault type after the VR shuts down. 1'b0: Disabled 1'b1: Enabled
9	DRMOS_FLT_ DETECT_EN_R1	Enables the PWM pin to act as a DrMOS fault type indicator and record the fault type to the EEPROM. It is for rail 1 only. For certain Intelli-Phase™ products, PWM can report the DrMOS fault type. When this function is enabled, the MP2927 monitors the voltage on the PWM pin to detect the fault type after the VR shuts down. 1'b0: Disabled 1'b1: Enabled
8	OVP_DVID_BLOCK_EN	Enables the device to block V_{OUT} over-voltage protection (OVP) during DVID. 1'b0: Disabled 1'b1: Enabled
7	OVP_DISCHARGE_ MODE	Sets the PWM behavior after OVP occurs. 1'b0: If OVP occurs, all PWMs are pulled low until V_{OUT} drops below the RVP threshold. Then all PWMs stay at tri-state, even if V_{OUT} rises above the RVP threshold again 1'b1: If OVP occurs, all PWMs are pulled low as long as V_{OUT} exceeds the RVP threshold.
6	RESERVED	Fixed to 0.
5	MFR_VRMON_LPF	Sets the filter parameter for the V_{OUT} report. 1'b0: No V_{OUT} report filter 1'b1: 2 points moving the average filter
4	MFR_IOUT_LPF	Set filter parameter of the I_{OUT} report. 1'b0: No I_{OUT} report filter 1'b1: 2 points moving the average filter

3	OCP_PHASE_SS_ BLOCK_EN	Enables the device to block over-current protection (OCP) phase limit protection during soft start. 1'b0: Disabled 1'b1: Enabled
2	LOW_PWR_MODE_ EN	Enables low-power mode. In low-power mode, the analog and digital blocks are off, and the controller consumes very little quiescent current when EN is off. In regular power mode, when EN is low, only the output power is disabled and the analog and NVM are still active. This is effective after VDD33 power reset. 1'b0: Disabled 1'b1: Enabled
1	CS_RESISTOR	Selects the IC's internal current-sense resistor. 1'b0: 1kΩ 1'b1: 2kΩ
0	SDM_FRAC	Enables the decimal fraction for sigma-delta (Σ-Δ) modulation. 1'b0: Disabled 1'b1: Enabled

MFR_VR_CONFIG3 (C3h)

The MFR_VR_CONFIG3 command on Page 0 sets some basic functions for the MP2927.

Command	MFR_VR_CONFIG3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						1										

Bits	Bit Name	Description
15	VOUT_SLEWRATE_ RES	Selects the V_{OUT} DVID, boot-up, and soft shutdown slew rate resolution. 1'b0: 1mV/μs/LSB 1'b1: 0.01mV/μs/LSB
14	VRMON_SEL_R3	Selects the analog-to-digital converter (ADC) speed when V_{OUT} is reported. For rail 3 only. 1'b0: Slow ADC 1'b1: Fast ADC
13	VRMON_SEL_R2	Selects the ADC speed when V_{OUT} is reported. For rail 2 only. 1'b0: Slow ADC 1'b1: Fast ADC
12	VRMON_SEL_R1	Selects the ADC speed when V_{OUT} is reported. For rail 1 only. 1'b0: Slow ADC 1'b1: Fast ADC
11	AVSBUS_PREFIX_ MODE	Selects when the MP2927 issues a status response frame to the CPU for a dynamic VID transition. It is only effective in AVSBus override mode. 1'b0: The MP2927 issues a status response frame when any rail's VR is settles 1'b1: The MP2927 issues a status response frame when all rails' VRs settle
10	RESERVED	Fixed to 1.

9	DIS_PREFIX_MODE	Select the status response frame behavior mode in AVSBus mode when VID is controlled by the PMBus interface. 1'b0: A status response frame is issued from the VR to the CPU when any of the AVSBus status bit flags (OCW, UVW, OTW, and OPW) change 1'b1: No status response frame is issued from the VR to the CPU when any of the AVSBus status bit flags (OCW, UVW, OTW, and OPW) change
8	HIZ_HIGH_BLOCK_EN	Enables a minimum tri-state time constraint when PWM goes from tri-state to a high state. The minimum tri-state time is set by PWM_MIN_TIME1 (62h on Page 0 and Page 1), bits[5:0]. 1'b0: Disabled 1'b1: Enabled
7	SETTLE_PREFIX_ MODE	Selects the behavior when issuing a status response frame during AVSBus DVID. 1'b0: Only the slave issues status response frame after receiving a Get Status command from the corresponding rail 1'b1: In addition to the Get Status command, the slave also issues a status response frame if the VDONE flag of the status response frame is 1
6	HIGHFREQ_DEBUG	Enables the PWM signal to precede 5ns in high-frequency (>1MHz) events in debug mode. 1'b0: Disabled 1'b1: Enabled
5	WATCH_DOG_EN	Enables the watchdog. 1'b0: Disabled 1'b1: Enabled
4	DELAY_LINE_EN	Enables the delay-line loop to sharply reduce the PWM jitter when the frequency loop is applied. 1'b0: Disabled 1'b1: Enabled
3	VIN2TON_EN	Enables V_{IN} influence on t_{ON}. 1'b0: V_{IN} sense does not influence the PWM on time 1'b1: V_{IN} sense influences the PWM on time
2:1	BG_CHOP_MODE	Selects the frequency for the bandgap chop. 2'b00: Disabled 2'b01: 125kHz 2'b10: 250kHz 2'b11: 500kHz
0	PWM_TRI_MODE	Set the tri-state voltage level. 1'b0: Hi-Z 1'b1: Middle voltage

MFR_VR_CONFIG4 (C4h)

The MFR_VR_CONFIG4 command on Page 0 sets some basic functions for the MP2927.

Command	MFR_VR_CONFIG4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	0			0												

Bits	Bit Name	Description
15	COMP_HYS_EN	Fixed to 0.
14	REFIN_EN	Enables the device to provide a 1.23V reference voltage on the GPIO pins with a sourcing capability. A 1µF external capacitor is required. The GPIO pin's function is selected via GPIO_SEL1 (66h), bits[3:0]. 1'b0: Disable REFIN 1'b1: Enable REFIN
13	COMP_DAC_ ENLARGE_EN	Enables the device to enlarge the COMP DAC value in the DC loop. 1'b0: Disabled 1'b1: Enabled
12	TSENS2_FLT_EN	Fixed to 0.
11	TSENSE_FLT_EN	Enables the TSENSE fault pin to act as DrMOS fault type indicator and record the fault type to the EEPROM. The MP2927 monitors the voltage level on the TSENSE pin. If the TSENSE voltage exceeds 2.2V, a DrMOS fault has occurred. 1'b0: Disabled 1'b1: Enabled
10	VORTN_LINE_ FLOAT_EN	Enables the device to detect whether the VORTN pins are floating on all rails. 1'b0: Disabled 1'b1: Enabled
9	VOSEN_LINE_ FLOAT_EN	Enables the device to detect whether the VOSEN pin are floating on all rails. 1'b0: Disabled 1'b1: Enabled
8:7	PVID3V3_1V8	Sets the PVID power logic. 2'b10: 3V3 logic 2'b01: 1V8 logic Others: Invalid
6	TON_REDUCTION_ DCM_EN_R3	Enables t_{ON} 1/4 reduction under DCM for rail 3. When t_{ON} reduction is enabled, the on time is reduced by 1/4 in 1-phase DCM to reduce the V_{OUT} ripple. 1'b0: Disabled 1'b1: Enabled
5	TON_REDUCTION_ DCM_EN_R2	Enables t_{ON} 1/4 reduction under DCM for rail 2. When t_{ON} reduction is enabled, the on time is reduced by 1/4 in 1-phase DCM to reduce the V_{OUT} ripple. 1'b0: Disabled 1'b1: Enabled
4	TON_REDUCTION_ DCM_EN_R1	Enables t_{ON} 1/4 reduction under DCM for rail 1. When t_{ON} reduction is enabled, the on time is reduced by 1/4 in 1-phase DCM to reduce the V_{OUT} ripple. 1'b0: Disabled 1'b1: Enabled
3	DAC_CMP_EN_R3	Enables a smooth transition when a DVID down event is preempted by a DVID up event. It is for rail 3 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: Disable the rail 3 V_{REF} filter function during continuous DVID down and up 1'b1: Enable the rail 3 V_{REF} filter function during continuous DVID down and up
2	DAC_CMP_EN_R2	Enables a smooth transition when a DVID down event is preempted by a DVID up event. It is for rail 2 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: Disable the rail 2 V_{REF} filter function during continuous DVID down and up 1'b1: Enable the rail 2 V_{REF} filter function during continuous DVID down and up

1	DAC_CMP_EN_R1	Enables a smooth transition when a DVID down event is preempted by a DVID up event. It is for rail 1 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: Disable the rail 1 V_{REF} filter function during continuous DVID down and up 1'b1: Enable the rail 1 V_{REF} filter function during continuous DVID down and up
0	SLOPE_LEAKAGE	Enables the device to turn off the low-leakage switch after the current source in DCM to avoid leakage from the current source via the high-leakage switch during slope compensation. 1'b0: Disabled 1'b1: Enabled

MFR_VR_CONFIG5 (C5h)

The MFR_VR_CONFIG5 command on Page 0 sets some basic functions for the MP2927.

Command	MFR_VR_CONFIG5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function							1									

Bits	Bit Name	Description
15	OV_UV_1/2_EN_R3	Enables the 1/2 divider for the V_{OUT} VID_OVP and VID_UVP thresholds on rail 3. 1'b0: Disabled 1'b1: Enabled
14	OV_UV_1/2_EN_R2	Enables the 1/2 divider for the V_{OUT} VID_OVP and VID_UVP thresholds on rail 2. 1'b0: Disabled 1'b1: Enabled
13	OV_UV_1/2_EN_R1	Enables the 1/2 divider for the V_{OUT} VID_OVP and VID_UVP thresholds on rail 1. 1'b0: Disabled 1'b1: Enabled
12	RVP_1/2_SET_EN_R3	Enables the reverse-voltage protection (RVP) threshold 1/2 divider for rail 3. 1'b0: Disabled 1'b1: Enabled
11	RVP_1/2_SET_EN_R2	Enables the RVP threshold 1/2 divider for rail 2. 1'b0: Disabled 1'b1: Enabled
10	RVP_1/2_SET_EN_R1	Enables the RVP threshold 1/2 divider for rail 1. 1'b0: Disabled 1'b1: Enabled
9	MFR_DBG_FIX32	Always fixed to 1.
8:6	ZCD_SET_R3	Fine-tunes the rail 3 zero-current detection (ZCD) threshold. 3'b000: -10mV 3'b001: -5mV 3'b010: 0mV 3'b011: +5mV 3'b100: +10mV 3'b101: +15mV 3'b110: +20mV 3'b111: +25mV

5:3	ZCD_SET_R2	Fine-tunes the rail 2 ZCD threshold. 3'b000: -10mV 3'b001: -5mV 3'b010: 0mV 3'b011: +5mV 3'b100: +10mV 3'b101: +15mV 3'b110: +20mV 3'b111: +25mV
2:0	ZCD_SET_R1	Fine-tunes the rail 1 ZCD threshold. 3'b000: -10mV 3'b001: -5mV 3'b010: 0mV 3'b011: +5mV 3'b100: +10mV 3'b101: +15mV 3'b110: +20mV 3'b111: +25mV

MFR_VR_CONFIG6 (C6h)

The MFR_VR_CONFIG6 command on Page 0 sets some basic functions for the MP2927.

Command	MFR_VR_CONFIG6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	VID_DAC_FILTER_R3	Selects the filter for the rail 3 VID-DAC while VID is ramping down. 2'b00: 2.35µs filter 2'b01: 4.7µs filter 2'b10: 7.05µs filter 2'b11: 9.4µs filter
13	VID_DAC_FILTER_R3_EN	Enables the rail 3 VID-DAC filter when DVID ramps down to avoid V_{OUT} undershoot. 1'b0: Disabled 1'b1: Enabled
12:11	VID_DAC_FILTER_R2	Selects the filter for the rail 2 VID-DAC while VID is ramping down. 2'b00: 2.35µs filter 2'b01: 4.7µs filter 2'b10: 7.05µs filter 2'b11: 9.4µs filter
10	VID_DAC_FILTER_R2_EN	Enables the rail 2 VID-DAC filter when DVID ramps down to avoid V_{OUT} undershoot. 1'b0: Disabled 1'b1: Enabled
9:8	VID_DAC_FILTER_R1	Selects the filter for the rail 1 VID-DAC while VID is ramping down. 2'b00: 2.35µs filter 2'b01: 4.7µs filter 2'b10: 7.05µs filter 2'b11: 9.4µs filter

7	VID_DAC_FILTER_R1_EN	Enables the rail 1 VID-DAC filter when DVID ramps down to avoid V_{OUT} undershoot. 1'b0: Disabled 1'b1: Enabled
6	VOUT_SR_PLUS_EN	Fixed to 1.
5:4	FILTER_IMON3_JOUT	Sets the filter time constant for the IMON3 J_{OUT} buffer. 2'b00: 810ns 2'b01: 2μs 2'b10: 3.5μs 2'b11: 12.2μs
3:2	FILTER_IMON2_JOUT	Sets the filter time constant for the IMON2 J_{OUT} buffer. 2'b00: 810ns 2'b01: 2μs 2'b10: 3.5μs 2'b11: 12.2μs
1:0	FILTER_IMON1_JOUT	Sets the filter time constant for the IMON1 J_{OUT} buffer. 2'b00: 810ns 2'b01: 2μs 2'b10: 3.5μs 2'b11: 12.2μs

MFR_VR_CONFIG7 (C7h)

The MFR_VR_CONFIG7 command on Page 0 sets some basic functions for the MP2927.

Command	MFR_VR_CONFIG7															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				MFR_SW_BLOCK_SET				10			2			2		

Bits	Bit Name	Description
15	MFR_PAGE_EN	Enables the device to follow what is set by WRITE_PROTECT (10h). 1'b0: Disabled 1'b1: Enabled
14	MFR_BYTEWR_DEBUG	NVM byte write. This bit can be enabled when operating Page 28 and Page 29. 1'b0: Disabled 1'b1: Enabled
13	MFR_BYTEWR_DEBUG2	NVM byte write. This bit can be enabled when operating Page 28 and Page 29. 1'b0: Disabled 1'b1: Enabled
12:9	MFR_SW_BLOCK_SET	Sets the slope low leakage switch's turn-on time in DCM. The PWM set signal is blocked when turning on the low leakage switch. 10ns/LSB.
8:6	VID_DATA_UPDATE_R3	Fixed to 10.
5:3	VID_DATA_UPDATE_R2	Fixed to 2.
2:0	VID_DATA_UPDATE_R1	Fixed to 2.

MFR_TIMEOUT (C8h)

MFR_TIMEOUT command on Page 0 sets the timeout time in PMBus mode.

Command	MFR_TIMEOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_ADC_HOLD_TIME								PMBUS_TIMEOUT							

Bits	Bit Name	Description
15:9	MFR_ADC_HOLD_TIME	Sets the ADC hold time. 50ns/LSB.
8	PMBUS_FILTER_EN	1'b0: Disables the PMBus digital filter 1'b1: Enables the PMBus digital filter
7:4	PMBUS_TIMEOUT	Sets the PMBUS timeout time, calculated with the following equation: PMBUS_TIMEOUT x 1.6ms + 1.5ms
3	PMBUS_SDA_DELAY_EN	1'b0: SCL and SDA have the same delay inside the IC 1'b1: SDA has delay that is 50ns longer than SCL inside the IC
2:0	RESERVED	Unused. Fixed to 0.

CAPABILITY (D0h)

The CAPABILITY command on Page 0 is read only.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7:0	CAPABILITY	Fixed to 0xC0.

JOUT1_SHORT_TERM (D1h)

The JOUT1_SHORT_TERM command on Page 0 returns the rail 1 real-time J_{OUT} in every short-term period.

Command	JOUT1_SHORT_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT1_SHORT_TERM															

Bits	Bit Name	Description
15:0	JOUT1_SHORT_TERM	Returns the real-time J_{OUT} value in every SHORT_TERM period. Convert the read value to actual output Joules (in µJ) with the following equation: $J_{OUT\_SHORT\_TERM}(\mu J) = \frac{D1h \times 8}{6Ch, bits[9:0] \times 1000} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch, bits[11:10], and: G_{VIDFF} is the VDIFF gain setting by 57h, bit[10]. 57h, bit[10] = 0: G_{VDIFF} = 1 57h, bit[10] = 1: G_{VDIFF} = 0.5

JOUT1_LONG_TERM (D2h)

The JOUT1_LONG_TERM command on Page 0 returns the rail 1 real-time J_{OUT} in every long-term period.

Command	JOUT1_LONG_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT1_LONG_TERM															

Bits	Bit Name	Description
15:0	JOUT1_LONG_TERM	Returns the real-time J_{OUT} value in every LONG_TERM period. Convert the read value to actual output Joules (in mJ) with the following equation: $J_{OUT\_LONG\_TERM}(mJ) = \frac{D2h \times 16.384}{6Ch, bits[9:0] \times 1000} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch, bits[11:10], and: G_{VIDFF} is the VDIFF gain setting by 57h, bit[10]. 57h, bit[10] = 0: G_{VDIFF} = 1 57h, bit[10] = 1: G_{VDIFF} = 0.5

IMON1_FAST_SENSE (D3h)

The IMON1_FAST_SENSE command on Page 0 returns one of the J_{OUT} ADC values.

Command	IMON1_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	IMON1_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	IMON1_FAST_SENSE	Returns the I_{OUT} ADC value in that J_{OUT} calculation. Convert the read value to the actual I_{OUT} (in A) with the following equation: $I_{OUT}(A) = \frac{D3h, bits[9:0]}{6Ch, bits[9:0] \times 1024} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$ Where GAIN_SEL is 6Ch, bits[11:10].

VDIFF1_FAST_SENSE (D4h)

The VDIFF1_FAST_SENSE command on Page 0 is returns an additional J_{OUT} ADC value.

Command	VDIFF1_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	VDIFF1_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.

9:0	VDIFF1_FAST_SENSE	Returns the V_{OUT} ADC value in the J_{OUT} calculation. 1.56mV/LSB when V_{DIFF} gain = 1 3.12mV/LSB when V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 0), bit[10].

ADC_SUM_RESET (FBh)

The ADC_SUM_RESET command on Page 0 resets the ADC_SUM count.

This command is write-only. There is no data byte for this command.

CLEAR_CRC_FAULT (FCh)

The CLEAR_CRC_FAULT command on Page 0 clears the CRC fault information that is stored in NVM Page 28.

This command is write-only. There is no data byte for this command.

CLEAR_STORED_FAULTS (FEh)

The CLEAR_STORED_FAULTS command on Page 0 clears the last fault information that is stored in NVM Page 28.

This command is write-only. There is no data byte for this command.

CLEAR_NVM_FAULTS (FFh)

The CLEAR_NVM_FAULTS command on Page 0 clears any NVM faults.

This command is write-only. There is no data byte for this command.

PAGE 1 REGISTER MAP

OPERATION_R2 (01h)

The OPERATION_R2 command on Page 1 turns the rail 2 output on and off in conjunction with the input from EN pin, and sets V_{OUT} to the upper or lower margin voltages. The controller remains in the OPERATION command setting mode until a subsequent OPERATION command is received, or a change to EN sets rail 2 to another mode.

Command	OPERATION_R2							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OPERATION_R2							

Bits	Bit Name	Description
7:0	OPERATION_R2	Sets the operation mode for rail 2. 8’b 00xx xxxx: Hi-Z off 8’b 01xx xxxx: Soft shutdown 8’b 1000 xxxx: Normal on 8’b 1001 xxxx: Margin low 8’b 1010 xxxx: Margin high 8’b 1011 xxxx: AVSBus mode Others: Invalid commands “x” means not applicable.

STORE_ALL_CODE (15h)

The STORE_ALL_CODE command on Page 1 instructs the PMBus device to copy all the Page 0, Page 1, and Page 2 contents, including the internal trim registers, from the operating memory to the matching locations in the NVM. Any items in the operating memory that do not have matching locations in the NVM are ignored.

This command is controlled by 50h (Page 1), bits[7:0]. 50h, bits[7:0] must be set to 0x63 to write to the NVM. If it is any other value, the NVM is write-protected.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command on Page 1 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents, including the internal trim registers, from the NVM and to overwrite the matching locations in the operating memory. Any items in the user store that do not have matching locations in the operating memory are ignored.

This command cannot be used while the device is outputting power, and is ignored if attempted.

This command is write-only. There is no data byte for this command.

STORE_USER_CODE (17h)

The STORE_USER_CODE command on Page 1 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the operating memory to the matching locations in the NVM (excluding the trim registers). Any items in the operating memory that do not have matching locations in the NVM are ignored.

This command is controlled by 50h (Page 1), bits[7:0]. 50h. Bits[7:0] must be set to 0x63 to write to the NVM. If it is any other value, the NVM is write-protected.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_USER_CODE (18h)

The RESTORE_USER_CODE command on Page 1 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the NVM and to overwrite the matching locations in the operating memory. Any items in the user store that do not have matching locations in the operating memory are ignored. Trim registers are not overwritten by this command.

This command cannot be used while the device is outputting power, and is ignored if attempted.

This command is write-only. There is no data byte for this command.

VOUT_COMMAND_R2 (21h)

The VOUT_COMMAND_R2 command on Page 1 sets the rail 2 V_{REF} VID in PMBus override mode.

Command	VOUT_COMMAND_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_COMMAND_R2										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_COMMAND_R2	Sets the rail 2 V_{REF} (VID_DAC V_{OUT}) in PMBus VID mode. 1 VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits[15:14].

VOUT_TRIM_R2 (22h)

The VOUT_TRIM_R2 command on Page 1 applies a fixed offset voltage to the commanded rail 2 V_{OUT}.

Command	VOUT_TRIM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	VOUT_TRIM_R2								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRIM_R2	Sets the V_{OUT} offset voltage on rail 2. VID_STEP/LSB.

VOUT_MAX_R2 (24h)

The VOUT_MAX_R2 command on Page 1 sets the maximum V_{REF} for rail 2 VID-DAC, which sets the maximum V_{OUT}. When an external resistor divider is applied, the maximum voltage is clamped to VOUT_MAX / K_R. Where K_R is the dividing ratio for the external resistor divider. This command is effective in PMBus mode.

Command	VOUT_MAX_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_MAX_R2										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MAX_R2	Sets the rail 2 maximum VID + offset voltage. This limits the sum of VID + the VOUT_TRIM offset. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits[15:14].

MFR_JOUT_LONG_TERM_R2 (25h)

The MFR_JOUT_LONG_TERM_R2 command on Page 1 sets the rail 2 long-term value to calculate J_{OUT}.

Command	MFR_JOUT_LONG_TERM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	JOUT_LONG_TERM									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	JOUT_LONG_TERM	Sets the long-term value for the J_{OUT} calculation, calculated with the following equation: LONG_TIME = JOUT_LONG_TERM x SHORT_TIME

MFR_JOUT_SHORT_TERM_R2 (26h)

The MFR_JOUT_SHORT_TERM_R2 command on Page 1 sets the rail 2 short-term value to calculate J_{OUT}.

Command	MFR_JOUT_SHORT_TERM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	JOUT_EN	Enables the J_{OUT} function. 1'b1: Enabled 1'b0: Disabled
12:7	JOUT_SHORT_TERM_FIX_FREQ	Bits[12:7] are fixed to 0 in fixed-frequency mode.
6:0		Bits[6:0] set JOUT_SHORT_TERM in the fixed-frequency mode. ADC_TIME/LSB. The short-term value can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_FIX_FREQ x ADC_TIME
12:1	JOUT_SHORT_TERM_ADAPTIVE_FREQ	50ns/LSB in adjustable-frequency mode. The short-term value can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_ADAPTIVE_FREQ x 50ns
0		Bit[0] is fixed to 0 in adjustable-frequency mode.

VOUT_TRANSITION_RATE_R2 (27h)

The VOUT_TRANSITION_RATE_R2 command on Page 1 sets the rail 2 dynamic VID (DVID) transition slew rate and EN soft-shutdown slew rate in PMBus mode.

Command	VOUT_TRANSITION_RATE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	VOUT_TRANSITION_RATE_R2												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	VOUT_TRANSITION_ RATE_R2	Sets the rail 2 DVID transition slew rate and the EN soft shutdown slew rate in PMBus mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h), bit[15].

VOUT_DROOP_R2 (28h)

The VOUT_DROOP_R2 on Page 1 sets the load-line parameters for rail 2.

Command	VOUT_DROOP_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function											RDROOP_SET_R2					

Bits	Bit Name	Description
15	IACDROOP_BW_SET_ R2	Enables the device to reduce the AC droop bandwidth (BW) by reducing the bias current. This is for rail 2 only. 1’b0: Disabled 1’b1: Enabled
14	IACDROOP_BW_SET_ R2	Enables the device to reduce the AC droop BW by increasing the compensation capacitor. This is for rail 2 only. 1’b0: Disabled 1’b1: Enabled
13	IACDROOP_GAIN2_SET_R2	Sets the PMBus load-line slope (AC droop) level; active when bit[12] of this command = 1. 1’b0:1 x IDROOP_INI 1’b1:1/2 x IDROOP_INI
12	MFR_ACLL_EN_R2	Selects the AC or DC load line. 1’b0: DC load line 1’b1: AC load line
11:9	PMBUS_LL_ LEVEL_R2	Sets the PMBus load line slope (DC droop) level; active when bit[12] of this command = 1. The MP2927 provides 8 levels for DC droop. 3’b000: 0 3’b001: 3/4 x IDROOP_INI 3’b010: 4/4 x IDROOP_INI 3’b011: 5/4 x IDROOP_INI 3’b100: 6/4 x IDROOP_INI 3’b101: 7/4 x IDROOP_INI 3’b110: 8/4 x IDROOP_INI 3’b111: 9/4 x IDROOP_INI

8:7	IDROOP_GAIN1_ SET_R2	Sets the IDROOP gain for rail 2. 2'b00: 1/16 x IDROOP_INI 2'b01: 1/8 x IDROOP_INI 2'b10: 1/4 x IDROOP_INI 2'b11: 1/2 x IDROOP_INI
6	SHORT_FIRST_ HALF_R2	Set this bit to 1 if R_{DROOP} is below 3.2Ω. 1'b0: Do not short the first half of the rail 2 resistors 1'b1: Short the first half of the rail 2 resistors
5:0	RDROOP_SET_R2	Sets the R_{DROOP} for rail 2. 100Ω/LSB. 6.4kΩ maximum.

VOUT_SCALE_LOOP_R2 (29h)

The VOUT_SCALE_LOOP_R2 command on Page 1 sets the rail 2 V_{OUT} to V_{REF} dividing ratio when an external output divider is applied.

Command	VOUT_SCALE_LOOP_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	VOUT_SCALE_LOOP_R2							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VOUT_SCALE_LOOP_ R2	Sets the rail 2 V_{OUT} to V_{REF} dividing ratio. V_{REF} ranges from 0V to 1.6V.

MFR_SETTLE_CTRL_R2 (2Ah)

The MFR_SETTLE_CTRL_R2 command on Page 1 sets the DVID parameters for rail 2.

Command	MFR_SETTLE_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_DROOPFALL_DELAY_R2					MFR_RISE_STEP_R2					RESERVED					

Bits	Bit Name	Description
15:11	MFR_DROOPFALL_ DELAY_R2	Sets the delay time between V_{REF} reaching the target (VID + DROOP_VID) and V_{REF} falling back to VID. 50ns/LSB.
10:6	MFR_RISE_STEP_R2	Sets the extra VID steps count for rail 2 when DVID goes up. The extra VID steps are used to compensate the droop created when the output capacitor charges during DVID up. 1 step/LSB.
5:0	RESERVED	Fixed to 0.

VOUT_MIN_R2 (2Bh)

The VOUT_MIN_R2 command on Page 1 instructs the device to limit the rail 2 minimum V_{OUT} in PMBus mode. If the V_{OUT} decoded from the PMBus interface is below the value set by VOUT_MIN (2Bh), V_{OUT} is clamped to VOUT_MIN. If an external resistor divider is applied on VOSEN, the minimum V_{OUT} is clamped to VOUT_MIN / K_R. Where K_R is the dividing ratio of the divider.

Command	VOUT_MIN_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_MIN_R2										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MIN_R2	Sets the minimum VID under PMBus mode for rail 2. Any VID below this value is clamped to VOUT_MIN. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits[15:14].

MFR_TRIM_DCM_1P_2P_R2 (2Ch)

The MFR_TRIM_DCM_1P_2P_R2 command on Page 1 trims the output voltage during 1-phase CCM or DCM. This is for the rail 2 power state.

Command	MFR_TRIM_DCM_1P_2P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X					MFR_TRIM_1PS_R2					MFR_TRIM_DCM_R2				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:5	MFR_TRIM_1PS_R2	Set the V_{OUT} trim for 1-phase CCM on rail 2. 2.3mV/LSB.
4:0	MFR_TRIM_DCM_R2	Sets the V_{OUT} trim for 1-phase DCM on rail 2. 2.3mV/LSB.

MFR_RESERVED (2Dh)

The MFR_RESERVED command on Page 1 is reserved.

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (2Fh)

The MFR_RESERVED command on Page 1 is reserved.

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_BLANK_TIME1_R2 (31h)

The MFR_BLANK_TIME1_R2 command on Page 1 configures the slope compensation reset time and PWM blanking time between two consecutive phases. It is for rail 2 only.

Command	MFR_BLANK_TIME1_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED				MFR_SLOPE_BLANK_TIME1_R2						MFR_PHASE_BLANK_TIME1_R2					

Bits	Bit Name	Description
15:12	RESERVED	Fixed to 0.
11:6	MFR_SLOPE_ BLANK_TIME1_R2	Configures the slope compensation reset time. Note that the slope compensation reset time should not be longer than the PWM blanking time, which is set by PWM_BLANK_TIME (MFR_BLANK_TIME1 (31h on Page 1), bits[5:0]). 5ns/LSB. The blank time can be calculated with the following equation: MFR_SLOPE_BLANK_TIME1_R2 = (bits[11:6] x 5 + 25) ns
5:0	MFR_PHASE_ BLANK_TIME1_R2	Configures the PWM blanking times between two consecutive phases. 5ns/LSB. The PWM blank time can be calculated with the following equation: MFR_PHASE_BLANK_TIME1_R2 = (bits[5:0] x 5 + 25) ns

MFR_VIN_SCALE_LOOP (32h)

The VIN_SCALE_LOOP command on Page 1 sets the resistor divider ratio for V_{IN} sensing.

Command	MFR_VIN_SCALE_LOOP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED								MFR_VIN_SCALE_LOOP							

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:0	MFR_VIN_SCALE_LOOP	Sets the VIN sensing scale, calculated with the following equation: $VIN\_SCALE\_LOOP = \frac{1280 \times V_{INSEN}}{V_{IN}} = \frac{1280 \times R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}}$ Where R_{TOP} and R_{BOTTOM} are the resistor dividers on the VINSEN pin.

FREQUENCY_SWITCH_R2 (33h)

The FREQUENCY_SWITCH_R2 command on Page 1 sets the rail 2 switching frequency (f_{SW}). f_{SW} can be set between 200kHz and 5.11MHz, with 10kHz per step.

Command	FREQUENCY_SWITCH_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	FREQUENCY_SWITCH_R2								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	FREQUENCY_SWITCH_R2	Sets the switching frequency (f_{SW}) in direct format. 10kHz/LSB.

MFR_OSR_SET_R1 (34h)

The MFR_OSR_SET_R2 command on Page 1 sets the overshoot reduction (OSR) parameters for rail 2.

Command	MFR_OSR_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				MFR_OSR_FILTER_R2						MFR_OSR_BLANKTIME_R2						

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	MFR_OSR_EN_R2	Enables overshoot reduction (OSR). This function can reduce the V_{OUT} overshoot when the load is released. 1'b0: Disabled 1'b1: Enabled
12:7	MFR_OSR_FILTER_R2	Sets the minimum OSR duration time. 5ns/LSB.
6:0	MFR_OSR_ BLANKTIME_R2	Sets the blanking time between two effective OSR events. 10ns/LSB.

MFR_PROCHOT_SET (36h)

The MFR_PROCHOT_SET command on Page 1 sets some configurations for PROCHOT faults.

Command	MFR_PROCHOT_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			PROCHOT_DAC_SET							PROCHOT_DELAY_TIME						

Bits	Bit Name	Description
15	PROCHOT_ SHUTDOWN_MODE	Selects the PROCHOT fault shutdown mode. 1'b0: All rails shut down 1'b1: Rail 1 shuts down

14	PROCHOT_FLT_EN	Enables PROCHOT fault. The MP2927 senses the voltage on the PROCHOT pin with the internal ADC. If the PROCHOT voltage exceeds or falls below the level set by MFR_PROCHOT_SET (36h on Page 1), bits[13:8], then a PROCHOT fault occurs and shuts down all rails immediately. The PROCHOT fault direction is determined by bit[1] of this command. 1'b0: Disabled 1'b1: Enabled
13:8	PROCHOT_DAC_SET	Sets the PROCHOT digital fault threshold. 4 ADC steps/LSB.
7	RESERVED	Fixed to 0.
6:2	PROCHOT_DELAY_ TIME	Sets the delay time for PROCHOT_DGTL_FAULT. 100ns/LSB.
1	PROCHOT_FLT_DIR	Selects the PROCHOT digital fault direction. 1'b0: Triggered when the PROCHOT voltage exceeds the threshold set by bits[13:8] in 36h (on Page 1) 1'b1: Triggered when the PROCHOT voltage falls below the threshold set by bits[13:8] in 36h (on Page 1)
0	PROCHOT_FLT_MODE	Selects the PROCHOT fault action mode. 1'b0: Auto-retry mode 1'b1: Latch-off mode

MFR_SLOPE_SW_INI_R2 (37h)

The MFR_SLOPE_SW_INI_R2 command on Page 1 sets rail 2's initial ramp for soft start.

Command	MFR_SLOPE_SW_INI_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	MFR_VOUT_FINE_TUNE_R2						MFR_SLOPE_SW_INI_R2						

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	MFR_VOUT_FINE_ TUNE_R2	Sets the V_{OUT} fine-tune value. The trim value is per step. Bit[12] is the signed bit. 0.64mV/LSB when V_{DIFF} gain = 1 0.96mV/LSB when V_{DIFF} gain = 1/2
6:0	MFR_SLOPE_SW_INI_ R2	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_DCM_R2 (38h)

The MFR_SLOPE_SR_DCM_R2 command on Page 1 sets the rail 2 slope compensation slew rate in 1-phase DCM.

Command	MFR_SLOPE_SR_DCM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_1P_R2 (39h)

The MFR_SLOPE_SR_1P_R2 command on Page 1 provides 2 bytes to configure slope compensation for 1-phase CCM. It is for rail 2 only.

Command	MFR_SLOPE_SR_1P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_8P_R1 (3Bh)

The MFR_SLOPE_SR_8P_R1 command on Page 0 provides 2 bytes to configure slope compensation for 8-phase CCM. It is for rail 1 only.

Command	MFR_SLOPE_SR_8P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED						CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_7P_R1 (3Ch)

The MFR_SLOPE_SR_7P_R1 command on Page 1 provides 2 bytes to configure slope compensation for 7-phase CCM. It is for rail 1 only.

Command	MFR_SLOPE_SR_7P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED						CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_6P_R1 (3Dh)

The MFR_SLOPE_SR_6P_R1 command on Page 1 provides 2 bytes to configure slope compensation for 6-phase CCM. It is for rail 1 only.

Command	MFR_SLOPE_SR_6P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED						CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_VRHOT_SET (3Eh)

The MFR_VRHOT_SET command on Page 1 is reserved.

Command	MFR_VRHOT_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X		MFR_VRHOT_LIMIT_R2							

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_VRHOT_EN_R2	Reserved.
7:0	MFR_VRHOT_LIMIT_R2	Reserved.

MFR_RESERVED (3Fh)

The MFR_RESERVED command on Page 1 is reserved.

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

VOUT_OV_FAULT_LIMIT_R2 (40h)

The VOUT_OV_FAULT_LIMIT_R2 command on Page 0 sets the V_{OUT} over-voltage protection (OVP) threshold.

Command	VOUT_OV_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	OVP_VID_SET_R2			OVP_ABS_SET_R2							

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	OVP_VID_SET_R2	Sets the over-voltage protection (OVP) VID threshold. 3'b001: V_{REF} + 200mV 3'b010: V_{REF} + 325mV 3'b100: V_{REF} + 450mV Others: Invalid
7:0	OVP_ABS_SET_R2	Sets an absolute OVP threshold. If V_{OUT} exceeds this value, OVP occurs. 10mV/LSB.

VOUT_OV_FAULT_RESPONSE_R2 (41h)

The VOUT_OV_FAULT_RESPONSE_R2 command on Page 1 sets protection mode and delay time if a V_{OUT} over-voltage (OV) fault occurs. It is for rail 2 only.

Command	VOUT_OV_FAULT_RESPONSE_R2															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X				MFR_OVP_VID_DELAYTIME_R2					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OVP_ABS_EN_R2	Enables absolute over-voltage protection (ABS_OVP) for rail 2. 1'b0: Disabled 1'b1: Enabled
7:6	MFR_OVP_VID_ MODE_R2	Set the over-voltage (OV) fault mode. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	MFR_OVP_VID_ DELAYTIME_R2	Sets the VID OVP blanking time. If a VID OVP condition lasts for longer than the OVP_VID blanking time, a VID OVP fault occurs. 100ns/LSB.

VOUT_MAX_ALERT_R2 (42h)

The VOUT_MAX_ALERT_R2 command on Page 1 sets the V_{OUT} over-voltage (OV) warning threshold or returns the maximum V_{OUT} for rail 2. The function is determined by GPIO_ACTIVE (68h), bit[13].

Command	VOUT_MAX_ALERT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_MAX_ALERT_R2															

Bits	Bit Name	Description
15:0	VOUT_MAX_ALERT_R2	If GPIO_ACTIVE (68h) bit[13] set to 0, this command sets the V_{OUT} over-voltage (OV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] set to 1, this command returns the maximum V_{OUT}. The maximum value can be written with a lower value, and if a higher V_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x0000 to reset this command. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 1), bit[10].

VOUT_MIN_ALERT_R2 (43h)

The VOUT_MIN_ALERT_R2 command on Page 1 sets the V_{OUT} under-voltage (UV) warning threshold or returns the minimum V_{OUT} for rail 2. The function is determined by GPIO_ACTIVE (68h), bit[13].

Command	VOUT_MIN_ALERT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_MIN_ALERT_R2															

Bits	Bit Name	Description
15:0	VOUT_MIN_ALERT_R2	If GPIO_ACTIVE (68h) bit[13] set to 0, this command sets the V_{OUT} under-voltage (UV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] set to 1, this command returns the minimum V_{OUT}. This command can be written with a higher value, and if a lower V_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x03FF to reset this command. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 0), bit[10].

VOUT_UV_FAULT_LIMIT_R2 (44h)

The VOUT_UV_FAULT_LIMIT_R2 command on Page 1 sets the V_{OUT} under-voltage (UV) fault threshold for rail 2.

Command	VOUT_UV_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	UVP_VID_SET_R2			RESERVED							

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	UVP_VID_SET_R2	Sets the under-voltage protection (UVP) threshold. 3'b000: V_{REF} - 425mV 3'b001: V_{REF} - 375mV 3'b010: V_{REF} - 325mV 3'b011: V_{REF} - 275mV 3'b100: V_{REF} - 225mV 3'b101: V_{REF} - 175mV 3'b110: V_{REF} - 125mV 3'b111: V_{REF} - 75mV
7:0	RESERVED	Fixed to 0.

VOUT_UV_FAULT_RESPONSE_R2 (45h)

The VOUT_UV_FAULT_RESPONSE_R2 on Page 1 sets the V_{OUT} under-voltage (UV) fault response for rail 2.

Command	VOUT_UV_FAULT_RESPONSE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X				MFR_UVP_DELAYTIME_R2					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_UV_VID_EN_R2	Enables VID under-voltage protection (UVP). 1'b0: Disabled 1'b1: Enabled
7:6	MFR_UVP_MODE_R2	Sets the V_{OUT} UVP mode. 2'b00: No action 2'b01: Latch off mode 2'b10: Hiccup mode 2'b11: Retry 6 times
5:0	MFR_UVP_ DELAYTIME_R2	Sets the V_{OUT} UVP blanking time. A UVP fault occurs if the sensed V_{DIFF} falls below the UVP threshold for the UVP blanking time. 100ns/LSB.

IOUT_OC_FAULT_LIMIT_R2 (46h)

The IOUT_OC_FAULT_LIMIT_R2 command on Page 1 sets the rail 2 I_{OUT} over-current (OC) fault threshold.

Command	IOUT_OC_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OCP_SPIKE_SET_R2								OCP_TDC_SET_R2							

Bits	Bit Name	Description
15:8	OCP_SPIKE_SET_R2	Sets the rail 2 OCP_SPIKE_TOTAL current-level DAC value. 6.25mV/LSB. OVP_SPIKE_TOTAL can be calculated with the following equation: $OCP\_SPIKE\_TOTAL = OCP\_SPIKE \times K_{CS} \times G_{IMON} \times R_{IMON} / 6.25$
7:0	OCP_TDC_SET_R2	Sets the rail 2 OCP_TDC_TOTAL current level. The high 8MSB of the IMON ADC result IMON1_SENSE, bits[9:0] is compared to this value. OCP_TDC_TOTAL can be calculated with the following equation: $OCP\_TDC\_TOTAL = OCP\_TDC \times K_{CS} \times G_{IMON} \times R_{IMON} / 6.25$

IOUT_OC_FAULT_RESPONSE_R2 (47h)

The IOUT_OC_FAULT_RESPONSE_R2 command on Page 1 sets the rail 2 over-current protection (OCP) options and values.

Command	IOUT_OC_FAULT_RESPONSE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									MFR_OCPTDC_TRIG_DELAY_R2							

Bits	Bit Name	Description
15:14	MFR_OCP_MODE_R2	Selects the over-current protection (OCP) mode for both OCP_TDC and OCP_SPIKE. 2'b00: No action 2'b01: Latch off mode 2'b10: Hiccup mode 2'b11: Retry 6 times
13	MFR_OCP_TDC_EN_R2	Enables OCP_TDC. 1'b0: Disabled 1'b1: Enabled
12:8	MFR_OCPTDC_ ACTION_DELAY_R2	Sets the OCP_TDC fault action time. This is the delay between OCP_L signal assertion and current limiting, hiccup mode entry, or shutdown. 1µs/LSB.
7:0	MFR_OCPTDC_ TRIG_DELAY_R2	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for the OCP_TDC blanking time. 20µs/LSB.

IOUT_OC_SPIKE_RESPONSE_R2 (48h)

The IOUT_OC_SPIKE_RESPONSE_R2 command on Page 1 sets the over-current (OC) spike options and values.

Command	IOUT_OC_SPIKE_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OCP_SPIKE_EN_R2	Enables OCP_SPIKE. 1'b0: Disabled 1'b1: Enabled
7:4	MFR_OCPSPIKE_ ACTIONDELAY_R2	Sets the OCP_SPIKE fault action delay time. This is time is between OCP_L assertion (after exceeding current threshold relative to IDDSpike) and current limiting, hiccup mode entry, or shutdown. 1µs/LSB.
3:0	MFR_OCPSPIKE_ TRIGDELAY_R2	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for an OCP_SPIKE blanking time. 200ns/LSB.

MFR_OCP_PHASE_LIMIT_R2 (49h)

The MFR_OCP_PHASE_LIMIT_R2 command on Page 1 sets the rail 2 per-phase valley current limit. The MP2927 provides OCP_PHASE protection to limit the per-phase valley current. OCP_PHASE is implemented by monitoring and comparing the cycle-by-cycle sensed CS current with a current reference.

Command	MFR_OCP_PHASE_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED								OCP_DAC_SET_R2							

Bits	Bit Name	Description
15:8	RESERVED	Unused. Fixed to 0.
7:0	OCP_DAC_SET_R2	Sets the per-phase valley current limit DAC value. 5mV/LSB.

IOUT_MAX_ALERT_R2 (4Ah)

The IOUT_MAX_ALERT_R2 command on Page 1 sets the I_{OUT} over-current (OC) warning threshold or returns the peak value of I_{OUT}. It is for rail 2 only. It is determined by GPIO_ACTIVE (68h), bit[13].

Command	IOUT_MAX_ALERT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IOUT_MAX_ALERT_R2															

Bits	Bit Name	Description
15:0	IOUT_MAX_ALERT_R2	If GPIO_ACTIVE (68h) bit[13] set to 0, then this command sets the DAC value for the I_{OUT} over-current (OC) warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h) bit[13] set to 1, then this command returns the peak I_{OUT}. I_{OUT} can be written with a lower value, and if a higher I_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x0000 to reset the command. Convert the read value to the actual I_{OUT} (in A) with the following equation: $$I_{OUT}(A) = \frac{4Ah, bits[9:0]}{6Ch, bits[9:0] \times 1024} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$$ Where GAIN_SEL is set by 6Ch, bits[11:10].

MFR_FS_LIMIT_12P_R1 (4Bh)

The MFR_FS_LIMIT_12P_R2 command on Page 1 sets the rail 2 FS_LIMIT threshold for 1-phase to detect fast load insertion and exit phase-shedding.

Command	MFR_FS_LIMIT_12P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED								MFR_FS_LIMIT_1P_R2							

Bits	Bit Name	Description
15:8	RESERVED	Unused. Fixed to 0.
7:0	MFR_FS_LIMIT_1P_R2	Set the PWM1 off-time threshold to exit phase-shedding. If the PWM1 off time (after excluding MIN_OFF_TIME) is shorter than FS_LIMIT_1P, add + 1 to the count. It is effective both for DCM and CCM. 10ns/LSB.

MFR_FS_LIMIT_78P_R1 (4Ch)

The MFR_FS_LIMIT_78P_R1 command on Page 1 sets the rail 1 FS_LIMIT threshold for 7-phase and 8-phase operation to detect fast load insertion and exit phase-shedding.

Command	MFR_FS_LIMIT_78P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_FS_LIMIT_8P_R1								MFR_FS_LIMIT_7P_R1							

Bits	Bit Name	Description
15:8	MFR_FS_LIMIT_8P_R1	Sets the exit phase-shedding PWM interval time for 8-phase operation. If the time interval between two phases is shorter than FS_LIMIT_8P, add + 1 to the interval. 5ns/LSB.
7:0	MFR_FS_LIMIT_7P_R1	Sets the exit phase-shedding PWM interval time for 7-phase operation. If the time interval between two phases is shorter than FS_LIMIT_7P, add + 1 to the interval. 5ns/LSB.

MFR_APS_LEVEL_12P_R2 (4Dh)

The MFR_APS_LEVEL_12P_R2 command on Page 1 sets the rail 2 automatic phase-shedding (APS) current threshold for 1-phase CCM and DCM.

Command	MFR_APS_LEVEL_12P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_APS_IIL_1P_CCM_R2								MFR_APS_IIL_1P_DCM_R2							

Bits	Bit Name	Description
15:8	MFR_APS_IIL_1P_CCM_R2	Sets the rail 2 automatic phase-shedding (APS) current threshold for 1-phase CCM. 1A/LSB.
7:0	MFR_APS_IIL_1P_DCM_R2	Sets the rail 2 APS current threshold for 1-phase DCM. 1A/LSB.

MFR_APS_LEVEL_67P_R1 (4Eh)

The MFR_APS_LEVEL_67P_R1 command on Page 1 sets the rail 1 automatic phase-shedding (APS) current threshold for 6-phase and 7-phase operation.

Command	MFR_APS_LEVEL_67P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_LEVEL_7P								DROP_LEVEL_6P							

Bits	Bit Name	Description
15:8	DROP_LEVEL_7P	Sets the rail 1 automatic phase-shedding (APS) current threshold for 7-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_6P	Sets the rail 1 APS current threshold for 6-phase DCM. 1A/LSB.

OT_FAULT_LIMIT_R2 (4Fh)

The OT_FAULT_LIMIT_R2 command on Page 1 is reserved.

Command	OT_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	MFR_OTP_LIMIT_R2							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	MFR_OTP_LIMIT_R2	Reserved.

MFR_NVM_WP (50h)

The MFR_NVM_WP command on Page 1 enables EEPROM write protection.

Command	MFR_NVM_WP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED								MFR_NVM_WP							

Bits	Bit Name	Description
15:8	RESERVED	Fixed to 0x85.
7:0	MFR_NVM_WP	Enables NVM write protection. This command is effective after a power cycle. 0x63: Enable writing to the NVM Others: Disable writing to the NVM

MFR_FS_DETECT_R2 (51h)

The MFR_FS_DETECT_R2 command on Page 1 sets some rail 2 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_FS_DETECT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X						RETURN_APS_DELAY						

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables the device to exit phase-shedding according to the PWM4 off time. The PWM minimum off time is excluded from PWM off time. 1’b0: Disabled 1’b1: Enabled
10	FS_EXIT_APS_EN_NP	Enables the device to exit phase-shedding according to the multi-phase PWM interval time between consecutive phases. The time threshold is set by register 4Bh. The PWM blanking time is excluded from the PWM interval time. 1’b0: Disabled 1’b1: Enabled

9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count for the PWM1 off-time condition to exit phase-shedding. Once the PWM off-time condition reaches the counting threshold, the controller exits APS immediately.
6:3	RETURN_APS_DELAY	Sets the minimum full-phase runtime after exiting APS due to an FS limit event. 20µs/LSB.
2:0	FS_EXIT_APS_CNT_NP	Sets the continuous count of the multi-phase PWMs interval time to exit phase-shedding. Once the PWM interval condition reaches the counting threshold, the controller exits APS immediately.

MFR_APS_CTRL_R2 (52h)

The MFR_APS_CTRL_R2 command on Page 1 sets some rail 2 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									MFR_PS_ENTER_TIME_R2							

Bits	Bit Name	Description
15:12	MFR_ADP_OC_NPS_ EXIT_CNT_R2	Sets the period delay count from when OCP_PHASE is triggered to when the device exits automatic phase-shedding (APS). 100ns/LSB.
11	MFR_ADP_OC_ NPS_EXIT_EN_R2	Enables OCP_PHASE to make the device exit APS at any power state. 1'b0: Disabled 1'b1: Enabled
10	MFR_ADP_PFM_ EXIT_EN_R2	Enables the device to exit APS under a rail 2 increasing frequency condition. 1'b0: Disabled 1'b1: Enabled
9	MFR_ADP_OC_ 1PS_EXIT_EN_R2	Enables OCP_PHASE to make the device exit APS during 1-phase DCM/CCM only. Then the device runs with full-phase operation. 1'b0: Disabled 1'b1: Enabled
8	MFR_ADP_UV_ EXIT_EN_R2	Sets rail 2 to enter full-phase operation if V_{FB} < VID - 25mV. 1'b0: Disabled 1'b1: Enabled
7:2	MFR_PS_ENTER_ TIME_R2	Sets the phase-shedding delay time. When the reported load current remains below the APS threshold for a set time, calculated with APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE, then the controller enters APS and automatically sheds phases according to the load current.
1	MFR_PHASHED_ EXIT_MOD_R2	Set the phase-dropping mode for phase-shedding. Phase-shedding may be due to APS. 1'b0: Drop to the target phase count immediately 1'b1: Shed phases one by one with a configured delay time. The delay time is set by DROP_PHASE_WAIT_TIME of this command
0	MFR_AUTO_PS_EN_R2	Enables rail 2 APS. 1'b0: Disabled 1'b1: Enabled

MFR_APS_CTRL2_R2 (53h)

The MFR_APS_CTRL2_R2 command on Page 1 sets some rail 2 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL2_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	APS_COMP_CNT						APS_COMP_LEVEL				MFR_APS_HYS			

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:9	APS_COMP_CNT	The MP2927 provides positive compensation on V_{REF} during phase-shedding to reduce undershoot. Phase-shedding may be due to APS. V_{REF} compensation is implemented by adding a PMBus-configurable positive voltage on the COMP of the DC loop. After phase-shedding starts, the voltage returns 0V step by step with a set time interval. The time interval between each step is set by APS_COMP_CNT. 50ns/LSB.
8	DECAY_COMP_EN	Enables V_{REF} compensation while exiting decay. The compensation voltage level and slew rate are the same as during APS. 1'b0: Disabled 1'b1: Enabled
7:4	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce the undershoot. The compensation is added to V_{REF} when phase-shedding begins. 1.37mV/LSB.
3:0	MFR_APS_HYS	Sets the current hysteresis between phase-shedding and phase-adding. This prevents back-and-forth phase-shedding when APS is enabled. 1A/LSB.

MFR_APS_CTRL3_R2 (54h)

The MFR_APS_CTRL3_R2 command on Page 1 sets some rail 2 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL3_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X					MFR_PRD_EXIT_APS_TIME_R2						

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:7	MFR_PS_INTERVAL_R2	Sets the phase-by-phase dropping time intervals. It is only effective when bit[1] of register 52h is set to 1. 2.5μs/LSB.
6:0	MFR_PRD_EXIT_ APS_TIME_R2	Sets the period condition for the DC loop and current balance loop hold. If the absolute error between the set switching period and the real switching period ($\|t_S - t_{SET}\|$) is longer than MFR_PRD_EXIT_APS_TIME x 80ns, then the device holds the DC loop and current balancing time for a given time. 80ns/LSB.

MFR_CUSTOMER_ID (55h)

The MFE_CUSTOMER_ID command on Page 1 sets the customer code revision.

Command	MFR_CUSTOMER_ID															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_CUSTOMER_ID															

Bits	Bit Name	Description
15:0	MFR_CUSTOMER_ID	Sets the customer code revision.

MFR_FSCB_LOOP_CTRL_R2 (56h)

The MFR_FSCB_LOOP_CTRL command on Page 1 sets the rail 2 f_{SW} and current balance loop.

Command	MFR_FSCB_LOOP_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function													CB_LOOP_HOLD_TIME			

Bits	Bit Name	Description
15	MFR_FS_LOOP_EN_R2	Enables the f_{SW} loop. The frequency loop keeps f_{SW} constant, and ensures it equals the set value, regardless of V_{IN} and the load current values. This bit active for all rails. 1'b0: Disabled 1'b1: Enabled
14	TRANS_HOLD_FS_EN_R2	Enables the device to maintain frequency loop and CB loop regulation when a load transient event is detected (e.g. V_{FB} exceeds VFB+ window or VFB- window). 1'b0: Disabled 1'b1: Enabled
13	PS_HOLD_FS_EN_R2	Enables the device to hold frequency loop regulation when the phase count changes. 1'b0: Disabled 1'b1: Enabled
12	DVID_HOLD_FS_EN_R2	Enables the device to hold frequency loop regulation when DVID occurs. 1'b0: Disabled 1'b1: Enabled
11:8	MFR_FS_LOOP_CNT_R2	Sets the minimum hold time for the frequency loop when any of load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set. 100μs/LSB.
7	MFR_CB_EN_R2	Enables the current balance loop. 1'b1: Enabled 1'b0: Disabled
6	PRD_HOLD_CB_EN_R2	Enables the device to hold the current balance loop when the PWM period meets the PWM switching period condition set via PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disabled 1'b1: Enabled

5	PS_HOLD_CB_EN_R2	Enables the device to hold the current balance loop when the phase number changes. 1'b0: Disabled 1'b1: Enabled
4	DVID_HOLD_CB_EN_R2	Enables the device to hold the current balance loop when DVID occurs. 1'b0: Disabled 1'b1: Enabled
3:0	CB_LOOP_HOLD_TIME	Sets the current balance loop holding time. If any load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set, then the current balance loop stops regulating for a time set via CB_LOOP_THOLD. 100μs/LSB.

MFR_VOUT_LOOP_CTRL_R2 (57h)

The MFR_VOUT_LOOP_CTRL_R2 command on Page 1 sets the rail 2 V_{OUT} loop parameters.

Command	MFR_VOUT_LOOP_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	MFR_VDIFF_GAIN_SEL_R2	Selects the V_{DIFF} gain. When V_{OUT} exceeds 1.6V (the maximum sampling range of the internal ADC), select 1/2x gain so that V_{OUT} can be as high as 3.2V. 1'b0: 1x 1'b1: 1/2x
9	MFR_DC_REF_SEL_R2	Sets the V_{OUT} DC loop sensing point. 1'b0: V_{FB} 1'b1: V_{DIFF}
8	MFR_VCAL_PS2_EN_R2	Enables DC loop calibration in DCM. 1'b0: Disabled 1'b1: Enabled
7	MFR_VCAL_EN_R1	Enables DC loop calibration for DCM and CCM. 1'b0: Disabled 1'b1: Enabled
6	PRD_HOLD_DC_EN_R1	Enables the device to hold the DC loop when the PWM time interval meets the PWM switching period condition set via PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disabled 1'b1: Enabled
5	PS_HOLD_DC_EN_R1	Enables the device to hold the DC loop when the phase count changes. 1'b0: Disabled 1'b1: Enabled
4	TRANS_HOLD_DC_EN_R1	Enables the device to hold DC loop regulation when a load transient event is detected (e.g. V_{FB} exceeds the VFB+ window or VFB- window). 1'b0: Disabled 1'b1: Enabled

3:0	MFR_DC_LOOP_CNT_R1	Sets the DC loop's minimum hold time in direct format. 200μs/LSB with a +100μs offset.

JOUT_SHORT_PK_R2 (58h)

The JOUT_SHORT_PK_R2 command on Page 1 returns the rail 2 peak J_{OUT} value in every short-term period.

Command	JOUT_SHORT_PK_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	JOUT_SHORT_PK_R2															

Bits	Bit Name	Description
15:0	JOUT_SHORT_PK_R2	Returns the peak value of J_{OUT} in every SHORT_TERM when J_{OUT} is enabled and GPIO_ACTIVE (68h), bit[13] is set to1. If J_{OUT} is disabled or GPIO_ACTIVE (68h), bit[13] is set to 0, this command returns the preset value.

JOUT_LONG_PK_R2 (59h)

The JOUT_LONG_PK_R2 command on Page 1 returns the rail 2 peak J_{OUT} value in every long-term period.

Command	JOUT_LONG_PK_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	JOUT_LONG_PK_R2															

Bits	Bit Name	Description
15:0	JOUT_LONG_PK_R2	Returns the peak value of J_{OUT} in every LONG_TERM when J_{OUT} is enabled and GPIO_ACTIVE (68h), bit[13] is set to 1. If J_{OUT} is disabled or GPIO_ACTIVE (68h), bit[13] is set to 0, this command returns the preset value.

MFR_SLOPE_CNT_1P_R2 (5Ah)

The MFR_SLOPE_CNT_1P_R2 command on Page 1 sets the rail 2 slope voltage clamp time in 1-phase operation.

Command	MFR_SLOPE_CNT_1P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_1P_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	MFR_SLOPE_CNT_1P_R2	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_2P_R2 (5Bh)

The MFR_SLOPE_CNT_2P_R2 command on Page 1 is reserved.

Command	MFR_SLOPE_CNT_2P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED								MFR_SLOPE_CNT_2P_R2							

Bits	Bit Name	Description
15:8	RESERVED	Fixed to 0.
7:0	MFR_SLOPE_CNT_2P_R2	Fixed to 0.

MFR_SLOPE_CNT_8P_R1 (5Ch)

The MFR_SLOPE_CNT_8P_R1 command on Page 1 sets the rail 1 slope voltage clamp time in 8-phase operation.

Command	MFR_SLOPE_CNT_8P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED								MFR_SLOPE_CNT_8P_R1							

Bits	Bit Name	Description
15:8	RESERVED	Fixed to 0.
7:0	MFR_SLOPE_CNT_8P_R1	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_DCM_R2 (5Eh)

The MFR_SLOPE_CNT_DCM_R2 command on Page 1 sets the rail 2 slope voltage clamp time in DCM.

Command	MFR_SLOPE_CNT_DCM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X		MFR_SLOPE_CNT_DCM_R2										

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:10	MFR_SLOPE_CNT_2P_PLUS_R2	Fixed to 0.
9:0	MFR_SLOPE_CNT_DCM_R2	Sets the slope voltage clamp time in DCM. 5ns/LSB.

MFR_PG_DELAY_R2 (5Fh)

The MFR_PG_DELAY_R2 command on Page 1 sets the rail 2 delay time for power good (PG) on and off.

Command	MFR_PG_DELAY_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PGOFF_DELAY_R2						MFR_PGON_DELAY_R2									

Bits	Bit Name	Description
15:10	MFR_PGOFF_DELAY_R2	Sets the power good (PG) off delay time. 5µs/LSB.
9:0	MFR_PGON_DELAY_R2	Sets the PG on delay time. 5µs/LSB.

TON_DELAY_R2 (60h)

The TON_DELAY_R2 command on Page 1 sets the rail 2 delay time from when system initialization ends to when the rail 2 V_{REF} starts to boot up.

Command	TON_DELAY_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TON_DELAY_R2															

Bits	Bit Name	Description
15:0	TON_DELAY_R2	Sets the delay time from when system initialization ends to when V_{REF} boots up. 100µs/LSB.

TON_RISE_R2 (61h)

The TON_RISE_R2 command on Page 1 sets the rail 2 V_{REF} boot-up slew rate.

Command	TON_RISE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	TON_RISE_R2												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TON_RISE_R2	Sets the rail 2 boot-up slew rate in PMBus mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h), bit[15].

MFR_PWM_MIN_TIME1_R2 (62h)

The MFR_PWM_MIN_TIME1_R2 command on Page 1 sets the minimum pulse width when PWM is high, low, or in tri-state. It is for rail 2 only.

Command	MFR_PWM_MIN_TIME1_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	MFR_MIN_LOW_TIME_R2									MFR_MIN_HIZ_TIME_R2					

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	MFR_MIN_LOW_TIME_R2	Sets the minimum PWM low time. 10ns/LSB with a -5ns offset. The minimum PWM low time can be calculated with the following equation: (PWM_MIN_LOW_TIME x 10) ns
8:6	MFR_MINON_TIME_R2	Sets the minimum PWM high time. 10ns/LSB with a -5ns offset. The minimum PWM high time can be calculated with the following equation: (PWM_MIN_HIGH_TIME x10) ns
5:0	MFR_MIN_HIZ_TIME_R2	Sets the minimum PWM tri-state time. 10ns/LSB with a -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: (PWM_MIN_TRI_TIME x 10) ns

MFR_PWM_MIN_TIME2_R2 (63h)

The MFR_PWM_MIN_TIME2_R2 command on Page 1 sets the PWM minimum off time and PWM on-pulse width when under-current protection (UCP) is triggered. It is for rail 2 only.

Command	MFR_PWM_MIN_TIME2_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	TON_LIMIT_TO_VCAL					X	X	X	X	MFR_MINOFF_TIME_R2				

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	TON_LIMIT_TO_VCAL	On the MP2927, the DC loop can be held if the PWM period meets the condition set by MFR_FS (33h on Page 0). If the calculated PWM on time is shorter than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	MFR_ZCD_EN_R2	Enables rail 2 zero-current detection (ZCD). 1'b0: Disabled 1'b1: Enabled
8:5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4:0	MFR_MINOFF_TIME_R2	Sets the PWM minimum off time. 20ns/LSB with a 15ns offset. The PWM minimum off time can be calculated with the following equation: (PWM_MIN_OFF_TIME x 20 + 15) ns

TOFF_DELAY_R2 (64h)

The TOFF_DELAY_R2 command on Page 1 sets the rail 2 delay time from EN going low to V_{REF} starting the shutdown process on rail 2.

Command	TOFF_DELAY_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TOFF_DELAY_R2															

Bits	Bit Name	Description
15:0	TOFF_DELAY_R2	Sets the delay time from when EN goes low to V_{REF} shutdown. 100µs/LSB.

TOFF_FALL_R2 (65h)

The TOFF_FALL_R2 command on Page 1 sets the V_{REF} transition down slew rate after the device receives an OPERATION soft shutdown command for rail 2.

Command	TOFF_FALL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	TOFF_FALL_R2												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TOFF_FALL_R2	Sets the rail 2 OPERATION command soft shutdown slew rate in PMBus mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h), bit[15].

GPIO_SEL_GROUP3 (66h)

The GPIO_SEL_GROUP3 command on Page 1 sets GPIO parameters.

Command	GPIO_SEL_GROUP3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		PWM8_SEL			PWM7_SEL											

Bits	Bit Name	Description
15	RESERVED	Fixed to 0.
14:12	PWM8_SEL	3’b000: The PWM8 pin is set to be PWM 3’b001: The PWM8 pin is set to be GND 3’b010: The PWM8 pin is set to be J_{OUT} short-term alert 3’b011: The PWM8 pin is set to be J_{OUT} long-term alert 3’b100: The PWM8 pin is set to be I_{OUT} max alert 3’b101: The PWM8 pin is set to be I_{OUT} min alert 3’b110: The PWM8 pin is set to be V_{OUT} max alert 3’b111: The PWM8 pin is set to be V_{OUT} min alert
11:0	PWM7_SEL	3’b000: The PWM7 pin is set to be PWM 3’b001: The PWM7 pin is set to be GND 3’b010: The PWM7 pin is set to be J_{OUT} short-term alert 3’b011: The PWM7 pin is set to be J_{OUT} long-term alert 3’b100: The PWM7 pin is set to be I_{OUT} max alert 3’b101: The PWM7 pin is set to be I_{OUT} min alert 3’b110: The PWM7 pin is set to be V_{OUT} max alert 3’b111: The PWM7 pin is set to be V_{OUT} min alert

GPIO_SEL_GROUP4 (67h)

Command	GPIO_SEL_GROUP4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:0	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

GPIO_ACTIVE (68h)

The GPIO_ACTIVE command on Page 1 selects the output active high/low GPIO.

Command	GPIO_ACTIVE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					RESERVED			RESERVED								

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	PK_LATCH_EN	1'b0: The related registers in the memory for Pages 0, 1, and 2 regarding the J_{OUT} short-term, J_{OUT} long-term, I_{OUT} max, I_{OUT} min, V_{OUT} max, and V_{OUT} min values can report the preset NVM values 1'b1: The related registers in the memory for Pages 0, 1, and 2 regarding the J_{OUT} short-term, J_{OUT} long-term, I_{OUT} max, I_{OUT} min, V_{OUT} max, and V_{OUT} min values can report the latched peak values
12	POUT_ALERT_NO_DELAY_EN	Enables a P_{OUT} alert delay. 1'b0: There is one term delay for a P_{OUT} alert 1'b1: No delay of for P_{OUT} altert
11:10	RESERVED	Fixed to 0.
9	OTWARN_SEL	1'b0: Selects VRHOT for the OT_WARN report 1'b1: Selects READ_TEMPERATURE (8Dh) > OT_WARN_LIMIT (51h) for the OT_WARN report
8:0	RESERVED	Fixed to 0.

MFR_VR_TEMP_CAL (69h)

The MFR_VR_TEMP_CAL command on Page 1 is reserved.

Command	MFR_VR_TEMP_CAL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_TEMP_GAIN_R2								MFR_TEMP_OFFSET_R2							

Bits	Bit Name	Description
15:8	MFR_TEMP_GAIN_R2	Reserved.
7:0	MFR_TEMP_OFFSET_R2	Reserved.

MFR_VOUT_CALC_R2 (6Ah)

The MFR_VOUT_CALC_R2 command on Page 1 sets the rail 2 gain and offset for the V_{OUT} calculation.

Command	MFR_VOUT_CALC_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	MFR_VOUT_CALC_OFFSET_R2						MFR_VOUT_CALC_GAIN_R2							

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:8	MFR_VOUT_CALC_ OFFSET_R2	Adds an offset to the V_{OUT} report in register READ_VOUT (8Bh). This bit is for the rail 2 V_{OUT} report only. This bit is in two's complement format. Bit[13] is the signed bit. VID_STEP/LSB. When the VID_STEP is 6.25mV, the voltage list below shows the direct values and real-world values. 6'b00 0000: 0mV 6'b00 0001: +6.25mV 6'b01 1111: +193.75mV 6'b10 0000: -200mV 6'b10 0001: -193.75mV 6'b11 1111: -6.25mV
7:0	MFR_VOUT_CALC_ GAIN_R2	Sets the gain from the ADC-sensed VOSEN - VORTN voltage to the PMBus V_{OUT} report in register READ_VOUT (8Bh). This bit is for the rail 2 V_{OUT} report only.

MFR_IOUT_CAL_AVSBUS_R2 (6Bh)

The MFR_IOUT_CALC_AVSBUS_R2 command on Page 1 sets the rail 2 gain and offset for the AVSBus I_{OUT} report.

Command	MFR_IOUT_CAL_AVSBUS_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IOUT_AVS_OS_R2					IOUT_AVS_GAIN_R2										

Bits	Bit Name	Description
15:11	IOUT_AVS_OS_R2	Bit[15] is the signed bit. 160mA/LSB.
10:0	IOUT_AVS_GAIN_R2	Sets the current-sense gain for the AVSBus report. The gain can be calculated with the following equation: $GAIN = \frac{1.6 \times 32 \times 10^4}{1024 \times K_{CS} \times G_{IMON} \times R_{IMON}}$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in μA/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the internal IMON resistor (in kΩ).

IOUT_CAL_GAIN_PMBUS_R2 (6Ch)

The IOUT_CAL_GAIN_PMBUS_R2 command on Page 1 sets the rail 2 gain for I_{OUT} reporting in PMBus mode. The MP2927 senses I_{OUT} by sensing the voltage of IMON. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch on Page 0).

Command	IOUT_CAL_GAIN_PMBUS_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	GAIN_SEL	MFR_IOUT_CALC_GAIN_R2										

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:10	GAIN_SEL	Sets the exponent value for the IOUT_CAL_GAIN calculation equation in this command.

9:0	MFR_IOUT_CALC_GAIN_R2	Sets the current-sense gain for the PMBus report. The gain can be calculated with the following equation: $IOUT\_CAL\_GAIN=\frac{1023}{1.6}\times K_{CS}\times G_{IMON}\times R_{IMON}\times 2^{(6-GAIN\_SEL)}$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bits[11:10] of this command.

IOUT_CAL_OS_PMBUS_R2 (6Dh)

The IOUT_CAL_OS_PMBUS_R2 command on Page 1 sets the rail 2 offset for I_{OUT} reporting in PMBus mode. The MP2927 senses I_{OUT} by sensing the voltage of IMON. The reported I_{OUT} is returned with PMBus command READ_IOUT (8Ch on Page 0).

Command	IOUT_CAL_OS_PMBUS_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	IOUT_CAL_PH_OFS_R2							MFR_IOUT_CALC_OFFSET_R2					

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:6	IOUT_CAL_PH_OFS_R2	Adds an offset according the phase number, where larger n corresponds with a larger offset. Bit[12] is signed bit.
5:0	MFR_IOUT_CALC_OFFSET_R2	Adds a current report offset to READ_IOUT (8Ch).

MFR_IMON_SET_R2 (6Eh)

The MFR_IMON_SET_R2 command on Page 1 sets certain configurations for the internal IMON sense in PMBus mode. It is rail 2 only.

Command	MFR_IMON_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						MFR_TRIM_IMON_DIGI_GAIN_R2										

Bits	Bit Name	Description
15:13	MFR_IMON_RES_SET_R2	Sets the rail 2 IMON resistor. 3'b 000: 2.5kΩ 3'b 001: 5kΩ 3'b 010: 10kΩ 3'b 011: 40kΩ 3'b1xx: No connection
12	MFR_IMON_GAIN_SET_R2	1'b0: The IMON2 current mirror gain is 1/8 1'b1: The IMON2 current mirror gain is 1/16
11	RESERVED	Fixed to 0.

10:0	MFR_TRIM_IMON_DIGI_GAIN_R2	Sets the digital calculation gain for I_{OUT} reporting. The gain is multiplied by the IMON ADC-sensed valued and forms the final IMON digital-sensed value. The IMON digital-sensed value is used for the PMBus I_{OUT} report. The final IMON-sensed value can be calculated with the following equation: $IOUT\_PMBUS\_REPORT=1024\times\frac{I_{OUT}\times K_{CS}\times G_{IMON}\times R_{IMON}}{1.6}\times\frac{TRIM\_DIGI\_GAIN}{1024}\times\frac{2^{(6\text{-}GAIN\_SEL)}}{GAIN}$ Where I_{OUT} is the output current (in A), K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and TRIM_DIGI_GAIN is a decimal value.

IOUT_MIN_ALERT_R2 (6Fh)

The IOUT_MIN_ALERT_R2 command on Page 1 returns the minimum I_{OUT} or its preset value. This function is determined by GPIO_ACTIVE (68h), bit[13]. It is for rail 2 only.

Command	IOUT_MIN_ALERT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	IOUT_MIN_ALERT_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IOUT_MIN_ALERT_R2	If GPIO_ACTIVE (68h), bit[13] is set to 0, then 6Fh sets the DAC value for the I_{OUT} OC warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h), bit[13] is set to 1, then 6Fh returns the minimum I_{OUT} value. In this mode, it also can be written with a higher value. If the higher I_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x03FF to reset this command. Convert the read value to the actual I_{OUT} (in A) with the following equation: $I_{OUT}(A)=\frac{6Fh[9:0]}{6Ch[9:0]\times 1024}\times 6Eh[10:0]\times 2^{(6\text{-}GAIN\_SEL)}$ Where GAIN_SEL: 6Ch, bits[11:10].

MFR_CONFIG_ID(70h)

The MFR_CONFIG_ID command in Page 1 configures the 4-digit part number suffix for the MP2927.

Command	MFR_CONFIG_ID															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_CONFIG_ID															

Bits	Bit Name	Description
15:0	MFR_CONFIG_ID	Sets the 4-digit part number suffix.

MFR_PVID01_R2 (71h)

The MFR_PVID01_R2 command on Page 1 sets the rail 2 V_{BOOT}.

Command	MFR_PVID01_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID1_R2								MFR_PVID0_R2							

Bits	Bit Name	Description
15:8	MFR_PVID1_R2	Reserved.
7:0	MFR_PVID0_R2	Sets the rail 2 V_{BOOT}, when MFR_VR_CONFIG1 (C1h on Page 0), bit[13] is 1. It is in VID format. VID_STEP/LSB.

MFR_PVID23_R2 (72h)

The MFR_PVID23_R2 command on Page 1 is reserved.

Command	MFR_PVID23_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID3_R2								MFR_PVID2_R2							

Bits	Bit Name	Description
15:8	MFR_PVID3_R2	Reserved.
7:0	MFR_PVID2_R2	Reserved.

MFR_PVID45_R2 (73h)

The MFR_PVID45_R2 command on Page 1 is reserved.

Command	MFR_PVID45_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID5_R2								MFR_PVID4_R2							

Bits	Bit Name	Description
15:8	MFR_PVID5_R2	Reserved.
7:0	MFR_PVID4_R2	Reserved.

MFR_PVID67_R1 (74h)

The MFR_PVID67_R1 command on Page 1 is reserved.

Command	MFR_PVID67_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID7_R1								MFR_PVID6_R1							

Bits	Bit Name	Description
15:8	MFR_PVID7_R1	Reserved.
7:0	MFR_PVID6_R1	Reserved.

SAMPLE_INTERVAL_12PH_R2 (75h)

The SAMPLE_INTERVAL_12P_R2 command on Page 1 sets the sample interval for 1-phase and 2-phase operation.

Command	SAMPLE_INTERVAL_12PH_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			SAMPLE_INTERVAL_2PH_R2							SAMPLE_INTERVAL_1PH_R2						

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13:7	SAMPLE_INTERVAL_2PH_R2	Sets the 2-phase sample interval. 50ns/LSB.
6:0	SAMPLE_INTERVAL_1PH_R2	Sets the 1-phase sample interval. 50ns/LSB.

MFR_RESERVED (76h)

The MFR_RESERVED command on Page 1 is reserved.

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (77h)

The MFR_RESERVED command on Page 1 is reserved.

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

STATUS_BYTE (78h)

The STATUS_BYTE command on Page 1 returns 1 byte of information with a summary of the most critical statuses and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		OFF					CML	X

Bits	Bit Name	Behavior	Description
7	NVM_BUSY	Live	Reports the live status of the NVM. 1'b0: The NVM is idle. NVM write and read with a PMBus command is available 1'b1: The NVM is busy. NVM write and read with a PMBus command is unavailable
6	OFF	Live	Indicates whether the rail 2 output is off. This bit is in live mode. It asserts if the rail 2 output is off. The output may turn off if there are protection, EN goes low, or VID = 0. 1'b0: VOUT2 is on 1'b1: VOUT2 is off
5	VOUT_OV_FAULT	Latch	Indicates whether a rail 2 V_{OUT} over-voltage (OV) fault has occurred. If rail 2 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. This is for VID_OVP and ABS_OVP. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	Indicates whether a rail 2 I_{OUT} over-current (OC) fault has occurred. If rail 2 OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. This is for OCP_TDC and OCP_SPIKE. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
3	VIN_UV_FAULT	Latch	Indicates whether a V_{IN} under-voltage UV fault has occurred. If a V_{IN} UV fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	TEMPERATURE	Latch	Indicates whether an over-temperature (OT) fault or warning has occurred. If a TSENSE-related OTP or OT warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Latch	Indicates whether a PMBus communication fault has occurred. If a PMBus communications related fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	PROCHOT_FAULT	Latch	Indicates whether a PROCHOT fault has occurred. If the PROCHOT voltage exceeds or falls below the level set by MFR_PROCHOT_SET (36h on Page 1), bits[13:8], then a PROCHOT fault occurs and this bit is set and latched. The PROCHOT fault direction is determined by MFR_PROCHOT_SET (36h on Page 1), bit[1]. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No PROCHOT fault has occurred 1'b1: A PROCHOT fault has occurred

STATUS_WORD (79h)

The STATUS_WORD (79h) command on Page 1 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher byte gives more detailed information of the fault conditions. The lower byte shares the information with register STATUS_BYTE (78h).

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function						X	X		STATUS_BYTE (78h)							

Bits	Bit Name	Behavior	Description
15	VOUT	Live	Indicates whether a rail 2 V_{OUT} over-voltage (OV) or under-voltage (UV) fault has occurred. If V_{OUT} OVP or UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} fault or warning has occurred 1'b1: A V_{OUT} fault or warning has occurred
14	IOUT	Live	Indicates whether a rail 2 I_{OUT} warning or a fault has occurred. If a rail 2 I_{OUT} fault or warning or a P_{OUT} warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} fault or warning has occurred 1'b1: An I_{OUT} fault or warning has occurred
13	INPUT	Latch	Indicates whether a V_{IN} or I_{IN} fault or warning has occurred. If any V_{IN} or I_{IN} protection or warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} or I_{IN} fault or warning has occurred 1'b1: A V_{IN} or I_{IN} fault or warning has occurred
12	RESERVED	Latch	Reserved.
11	PG_NOT_ACTIVE	Live	1'b0: PG is active. 1'b1: PG is not active
10:9	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
8	WATCH_DOG_OVF	Latch	Indicates whether the watchdog monitor block timer has overflowed. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 1 returns 1 byte of information with the detailed V_{OUT} fault and warning statuses for rail 1.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X			X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Indicates whether a rail 2 V_{OUT} over-voltage (OV) fault has occurred. If rail 2 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
6	VOUT_OV_WARNING	Live	Indicates whether a rail 2 V_{OUT} OV warning has occurred. If rail 2 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} OV warning has occurred 1'b1: A V_{OUT} OV warning has occurred
5	VOUT_UV_WARNING	Live	Indicates whether a rail 2 V_{OUT} under-voltage (UV) warning has occurred. If rail 2 UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} UV warning has occurred 1'b1: A V_{OUT} UV warning has occurred
4	VOUT_UV_FAULT	Latch	Indicates whether a rail 2 V_{OUT} UV fault has occurred. If rail 2 UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN_ WARNING	Latch	Indicates whether rail 2 V_{OUT} has reached VOUT_MAX or VOUT_MIN. If the VID value exceeds the value set by VOUT_MAX (24h on Page 0) and VOUT_MIN (2Bh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID exceeds VOUT_MAX or is below VOUT_MIN
2	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
1	LINE_FLOAT	Latch	Indicates whether rail 2 line-float protection has occurred. If a line-float fault is detected, the device shuts down the associated rails and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No line-float fault has occurred 1'b1: A line-float fault has occurred
0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 1 returns 1 byte of information with the detailed I_{OUT} fault and warning statuses for rail 2.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function				X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Indicates whether a rail 2 I_{OUT} over-current (OC) fault has occurred. If rail 2 OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. This is for OCP_TDC and OCP_SPIKE. 1'b0: No output OC fault 1'b1: An output OC fault has occurred
6	TDC_OCP_UV_FAULT	Latch	Indicates whether a rail 2 I_{OUT} dual over-current (OC) and under-voltage (UV) fault has occurred. If rail 2 OCP occurs while the UV comparator is set, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No dual OC and UV fault has occurred 1'b1: A dual OC and UV fault has occurred
5:0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_INPUT (7Ch)

The STATUS_INPUT command on Page 1 returns 1 byte of information with detailed input fault and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X	X		X	X	X

Bits	Bit Name	Behavior	Description
7	VIN_OVP	Latch	Indicates whether a V_{IN} over-voltage (OV) fault has occurred. If V_{IN} exceeds the VIN_OV limit, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
5	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
4	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
3	VIN_UVLO_LIVE	Live	Indicates whether V_{IN} under-voltage lockout (UVLO) has occurred in real time. If V_{IN} falls below the VIN_OFF threshold, this bit is set. The bit resets when V_{IN} exceeds the VIN_ON threshold. 1'b0: V_{IN} is below VIN_OFF (36h) 1'b1: V_{IN} exceeds VIN_ON (35h)
2:0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command on Page 0 returns 1 byte of information with temperature-related fault and warning conditions.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Indicates whether an over-temperature (OT) fault has occurred. If the temperature sensed via TSENSE exceeds the OT fault limit set by OT_FAULT_LIMIT (4Fh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
6	VRHOT	Live	Indicates whether a VRHOT event has occurred. If the temperature sensed via TSENSE exceeds the OT warning limit set by MFR_VRHOT_SET (3Eh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No VRHOT event has occurred 1'b1: A VRHOT event has occurred
5:0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_CML (7Eh)

The STATUS_CML command on Page 0 returns 1 byte of information with PMBus communication related faults.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function					X			

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	Indicates whether the device received an invalid PMBus command. If the MP2927 receives an unsupported command code, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	INVALID_DATA	Latch	Indicates whether invalid PMBus data has been received. If the MP2927 receives unsupported data, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received

5	PEC_ERROR	Latch	Indicates whether a PMBus PEC fault has occurred. The PMBus interface supports the use of the packet error checking (PEC) byte defined in the SMBus standard. The PEC byte is transmitted by the MP2927 during a read transaction or sent to the MP2927 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4	NVM_CRC_ERROR	Latch	Indicates whether a cyclic redundancy check (CRC) fault has occurred. While storing the operating memory data to the NVM, the MP2927 calculates a CRC code for each bit, and saves the final CRC code to the NVM. While restoring the NVM data to the operating memory, the MP2927 recalculates the CRC code and checks the CRC results when the restoration process is done. If the result does not match what is stored, the VR shuts down and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
3	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
2	CML_FLT_TRG	Latch	If NVM operation is blocked while the controller records a fault to the NVM, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No NVM operation is blocked 1'b1: NVM operation has been blocked while the controller records a fault to the NVM
1	CML_OTHER_FAULTS	Latch	If any of the faults listed below occur during PMBus communication, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. • Sending too few bits • Reading too few bits • Host sends or reads too few bytes • Reading too many bytes
0	NVM_SIG_FAULTS	Latch	While restoring data from the NVM to the operating memory, the device checks the signature register in address 00h of the NVM first. If the signature register is 0x1234, the restoration process halts and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to clear the bit. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

READ_ADC_SUM (81h)

The READ_ADC_SUM command on Page 1 returns the sum of 16 consecutive ADC-sensed results.

Command	READ_ADC_SUM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X		ADC_SUM													

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	ADC_SUM_READY	Indicates whether the 16 consecutive ADC-sensed results are ready. 1'b0: Not ready 1'b1: Ready
13:0	ADC_SUM	Stores the sum of 16 consecutive ADC-sensed results. Send FBh (0 byte) to start the ADC summing action.

READ_VFB2_SENSE (82h)

The READ_VFB2_SENSE command on Page 0 returns the ADC-sensed VFB2 voltage.

Command	READ_VFB2_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_VFB_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_VFB1_SENSE	Returns the ADC-sensed VFB2 voltage in direct format. 1.56mV/LSB.

READ_TSENSE_SENSE (83h)

The READ_TSENSE_SENSE on Page 1 reads the TSENSE pin voltage.

Command	READ_TSENSE_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_TSENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_TSENSE	Returns the ADC-sensed voltage on TSENSE in direct format. 1.56mV/LSB.

READ_CS5 (84h)

The READ_CS5 command on Page 1 returns the ADC-sensed average voltage on rail 1's CS5 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	RESERVED						READ_CS5									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS5	Returns the ADC-sensed voltage on rail 1's CS5 in direct format. 3.125mV/LSB.

READ_CS6 (85h)

The READ_CS6 command on Page 1 returns the ADC-sensed average voltage on rail 1's CS6 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	RESERVED						READ_CS6									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS6	Returns the ADC-sensed voltage on rail 1's CS6 in direct format. 3.125mV/LSB.

READ_CS7 (86h)

The READ_CS7 command on Page 1 returns the ADC-sensed average voltage on rail 1's CS7 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS7															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	RESERVED						READ_CS7									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS7	Returns the ADC-sensed voltage on rail 1's CS7 in direct format. 3.125mV/LSB.

READ_CS8 (86h)

The READ_CS8 command on Page 1 returns the ADC-sensed average voltage on rail 1's CS8 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS8															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	RESERVED						READ_CS8									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS8	Returns the ADC-sensed voltage on rail 1's CS8 in direct format. 3.125mV/LSB.

READ_VIN (88h)

The READ_VIN command on Page 1 provides 2 bytes to return the sensed V_{IN} based on the VINSEN1 pin. In VID mode, the returned value must ignore the exponent value set by bits[15:11].

Command	READ_VIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	1	1	0	1	1	X	READ_VIN									

Bits	Bit Name	Description
15:11	EXP	Unused. Fixed to 11011.
10	RESERVED	Fixed to 0.
9:0	READ_VIN	Returns the sensed V_{IN} in Linear11 format. 31.25mV/LSB

READ_VOUT (8Bh)

The READ_VOUT command on Page 1 returns the sensed rail 2 VOSEN - VORTN voltage. Where K_R is the dividing ratio of the divider.

Command	READ_VOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	READ_VOUT											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT	Returns the V_{OUT} value. Linear mode: 2mV/LSB. V_{OUT} can be calculated with the following equation: V_{OUT} = READ_VOUT x 2 x K_R Where K_R is the dividing ratio of the divider. Direct mode: VID_STEP/LSB. V_{OUT} can be calculated with the following equation: V_{OUT} = READ_VOUT x VID_STEP x K_R. Where VID_STEP is determined by C1h, bits[15:14], and K_R is the dividing ratio of the divider.

READ_IOUT (8Ch)

The READ_IOUT command on Page 0 returns the sensed rail 1 I_{OUT}.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP					READ_IOUT										

Bits	Bit Name	Description
15:11	EXP	This value is determined by VR_CONFIG1 (C1h), bit[3]. 1: Select 5'b11110 0: Select 5'b11111
10:0	READ_IOUT	Returns the sensed I_{OUT}, which is determined by VR_CONFIG1 (C1h), bit[3]. 1: 0.25A/LSB 0: 0.5A/LSB

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 1 is reserved.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP					X	X	X	READ_TEMP							

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_TEMP	Reserved.

READ_AD_RESULT (8Eh)

The READ_AD_RESULT command on Page 1 returns the ADC result.

Command	READ_AD_RESULT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_ADC									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_ADC	Returns the ADC value.

READ_VCOMP (8Fh)

The READ_VCOMP command on Page 1 returns the COMP value.

Command	READ_VCOMP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_VCOMP							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_VCOMP	Returns the COMP value.

READ_POUT (96h)

The READ_POUT command on Page 1 returns the rail 2 output power (P_{OUT}).

Command	READ_POUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_POUT															

Bits	Bit Name	Description
15:0	READ_POUT	Returns the rail 2 P_{OUT}. The ADC read value is the same as the value from D1h. Convert the read value to actual power (in W) with the following equation: $P_{OUT}(W) = \frac{\frac{READ\_POUT \times 8}{6Ch,bits[9:0] \times 1000} \times 6Eh,bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}}{t_{SHORT\_TERM}}$ Where GAIN_SEL is 6Ch, bits[11:10], and: G_{VIDFF} is the VDIFF gain setting by 57h, bit[10]. 57h, bit[10] = 0: G_{VDIFF} = 1 57h, bit[10] = 1: G_{VDIFF} = 0.5 t_{SHORT_TERM} is the short term (in µs): 26h, bit[15] = 0: t_{SHORT_TERM} = 26h, bits[12:1] x 0.05µs 26h, bit[15] = 1: t_{SHORT_TERM} = (26h, bits[6:0] + 1) x 4Eh (on Page 1), bits[13:8] x 0.05µs

CAPABILITY (D0h)

The CAPABILITY command on Page 1 is read-only.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	CAPABILITY							

Bits	Bit Name	Description
7:0	CAPABILITY	Fixed to 0xC0.

JOUT2_SHORT_TERM (D1h)

The JOUT2_SHORT_TERM command on Page 1 returns the real-time rail 2 J_{OUT} in every short-term period.

Command	JOUT2_SHORT_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT2_SHORT_TERM															

Bits	Bit Name	Description
15:0	JOUT2_SHORT_TERM	Returns the real-time J_{OUT} value in every SHORT_TERM period. Convert the read value to actual output Joule (in µJ) with the following equation: $J_{OUT\_SHORT\_TERM}(\mu J) = \frac{D1h \times 8}{6Ch,bits[9:0] \times 1000} \times 6Eh,bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch, bits[11:10], and: G_{VIDFF} is the VDIFF gain setting by 57h, bit[10]. 57h, bit[10] = 0: G_{VDIFF} = 1 57h, bit[10] = 1: G_{VDIFF} = 0.5

JOUT2_LONG_TERM (D2h)

The JOUT2_LONG_TERM command on Page 1 returns the real-time rail 2 J_{OUT} in every long-term period.

Command	JOUT2_LONG_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT2_LONG_TERM															

Bits	Bit Name	Description
15:0	JOUT2_LONG_TERM	Returns the real-time J_{OUT} value in every LONG_TERM period. Convert the read value to the actual output Joule (in mJ) with the following equation: $J_{OUT\_LONG\_TERM}(mJ) = \frac{D2h \times 16.384}{6Ch, bits[9:0] \times 1000} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch, bits[11:10], and: G_{VIDFF} is the VDIFF gain setting by 57h, bit[10]. 57h, bit[10] = 0: G_{VDIFF} = 1 57h, bit[10] = 1: G_{VDIFF} = 0.5

IMON2_FAST_SENSE (D3h)

The IMON2_FAST_SENSE command on Page 1 returns one of the J_{OUT} ADC values.

Command	IMON2_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	IMON2_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IMON2_FAST_SENSE	Returns the I_{OUT} ADC value in the J_{OUT} calculation. Convert the read value to the actual I_{OUT} (in A) with the following equation: $I_{OUT}(A) = \frac{D3h[9:0]}{6Ch, bits[9:0] \times 1024} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$ Where GAIN_SEL is 6Ch, bits[11:10].

VDIFF2_FAST_SENSE (D4h)

The VDIFF2_FAST_SENSE command on Page 1 returns an additional J_{OUT} ADC value.

Command	VDIFF2_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	VDIFF2_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

9:0	VDIFF2_FAST_SENSE	Returns the V_{OUT} ADC value in the J_{OUT} calculation. 1.56mV/LSB when V_{DIFF} gain = 1 3.12mV/LSB when V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 57h (on Page 0), bit[10].

DIE_TEMP_SENSE (D5h)

The DIE_TEMP_SENSE command on Page 1 returns the die temperature's ADC value.

Command	DIE_TEMP_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	DIE_TEMP_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	DIE_TEMP_SENSE	Returns the die temperature's ADC data. 1.5625mV/LSB. Convert the read value to the actual die temperature (in °C) with the following equation: $T_{DIE\_TEMP}(°C) = \frac{D5h, bits[9:0] \times 1.5625mV - 275mV}{3}$

FAULTS_REPORT1 (E0h)

The FAULTS_REPORT1 command on Page 1 returns some protection information for the MP2927. This information is lost when the device shuts down.

Command	FAULTS_REPORT1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X		X	X		X								

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	CS10_FAULT_FLAG	Indicates whether a CS10 fault has occurred. This bit is set to 1 when CS10 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
11:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	CS9_FAULT_FLAG	Indicates whether a CS9 fault has occurred. This bit is set to 1 when CS9 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7	CS8_FAULT_FLAG	Indicates whether a CS8 fault has occurred. This bit is set to 1 when CS8 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred

6	CS7_FAULT_FLAG	Indicates whether a CS7 fault has occurred. This bit is set to 1 when CS7 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
5	CS6_FAULT_FLAG	Indicates whether a CS6 fault has occurred. This bit is set to 1 when CS6 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
4	CS5_FAULT_FLAG	Indicates whether a CS5 fault has occurred. This bit is set to 1 when CS5 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
3	CS4_FAULT_FLAG	Indicates whether a CS4 fault has occurred. This bit is set to 1 when CS4 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
2	CS3_FAULT_FLAG	Indicates whether a CS3 fault has occurred. This bit is set to 1 when CS3 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
1	CS2_FAULT_FLAG	Indicates whether a CS2 fault has occurred. This bit is set to 1 when CS2 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
0	CS1_FAULT_FLAG	Indicates whether a CS1 fault has occurred. This bit is set to 1 when CS1 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred

FAULTS_REPORT2 (E1h)

The FAULTS_REPORT2 command on Page 1 returns some protection information for the MP2927. This information is lost when the device shuts down.

Command	FAULTS_REPORT2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	OTP_R2	Indicates whether rail 2 over-temperature protection (OTP) has occurred. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
12	OCP_TDC_R2	Indicates whether rail 2 OCP_TDC has occurred. 1'b0: No OCP_TDC fault has occurred 1'b1: An OCP_TDC fault has occurred

11	OCP_SPIKE_R2	Indicates whether rail 2 OCP_SPIKE has occurred. 1'b0: No OCP_SPIKE fault has occurred 1'b1: An OCP_SPIKE fault has occurred
10	UVP_R2	Indicates whether rail 2 V_{OUT} under-voltage protection (UVP) has occurred. 1'b0: No V_{OUT} UVP has occurred 1'b1: V_{OUT} UVP has occurred
9	VID_OVP_R2	Indicates whether rail 2 V_{OUT} VID over-voltage protection (OVP) has occurred. 1'b0: No V_{OUT} VID OVP has occurred 1'b1: V_{OUT} VID OVP has occurred
8	ABSOLUTE_OVP_R2	Indicates whether rail 2 V_{OUT} ABS OVP has occurred. 1'b0: No V_{OUT} ABS OVP has occurred 1'b1: V_{OUT} ABS OVP has occurred
7:6	RESERVED	Fixed to 0.
5	OTP_R1	Indicates whether rail 1 over-temperature protection (OTP) has occurred. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
4	OCP_TDC_R1	Indicates whether rail 1 OCP_TDC has occurred. 1'b0: No OCP_TDC fault has occurred 1'b1: An OCP_TDC fault has occurred
3	OCP_SPIKE_R1	Indicates whether rail 1 OCP_SPIKE has occurred. 1'b0: No OCP_SPIKE fault has occurred 1'b1: An OCP_SPIKE fault has occurred
2	UVP_R1	Indicates whether rail 1 V_{OUT} UVP has occurred. 1'b0: No V_{OUT} UVP has occurred 1'b1: V_{OUT} UVP has occurred
1	VID_OVP_R1	Indicates whether rail 1 V_{OUT} VID OVP has occurred. 1'b0: No V_{OUT} VID OVP has occurred 1'b1: V_{OUT} VID OVP has occurred
0	ABSOLUTE_OVP_R1	Indicates whether rail 1 V_{OUT} ABS OVP has occurred. 1'b0: No V_{OUT} ABS OVP has occurred 1'b1: V_{OUT} ABS OVP has occurred

FAULTS_REPORT3 (E2h)

The FAULTS_REPORT3 command on Page 1 returns some protection information for the MP2927. This information is lost when the device shuts down.

Command	FAULTS_REPORT3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM1_FAULTS				PWM2_FAULTS				PWM3_FAULTS				PWM4_FAULTS			

Bits	Bit Name	Description
15:12	PWM1_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 1-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM2_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 2-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM3_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 3-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over- temperature protection 4'b1000: SW-PGND short protection
3:0	PWM4_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 4-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over- temperature protection 4'b1000: SW-PGND short protection

FAULTS_REPORT4 (E3h)

The FAULTS_REPORT4 command on Page 1 returns some protection information for the MP2927. This information is lost when the device shuts down.

Command	FAULTS_REPORT4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM5_FAULTS				PWM6_FAULTS				PWM7_FAULTS				PWM8_FAULTS			

Bits	Bit Name	Description
15:12	PWM5_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 5-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

11:8	PWM6_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 6-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM7_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 7-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM8_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 8-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULTS_REPORT5 (E4h)

The FAULTS_REPORT5 command on Page 1 returns some protection information for the MP2927. This information is lost when the device shuts down.

Command	FAULTS_REPORT5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	RESERVED				PWM9_FAULTS				RESERVED				PWM10_FAULTS			

Bits	Bit Name	Description
15:12	RESERVED	Reserved.
11:8	PWM9_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 9-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	RESERVED	Reserved.
3:0	PWM10_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 10-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULTS_REPORT6 (E5h)

The FAULTS_REPORT5 command on Page 1 returns some protection information for the MP2927. This information is lost when the device shuts down.

Command	FAULTS_REPORT6															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	PMBUS_TIMEOUT2	Indicates whether a PMBus TIMEOUT2 event has occurred. 1'b0: No PMBus TIMEOUT2 event has occurred 1'b1: A PMBus TIMEOUT2 event has occurred
12	PROCHOT_FAULT	Indicates whether a PROCHOT fault has occurred. 1'b0: No PROCHOT fault has occurred 1'b1: A PROCHOT fault has occurred
11	CHIP_OTP_FLAG	Indicates whether chip over-temperature protection (OTP) has occurred. 1'b0: No chip OTP 1'b1: Chip OTP has occurred
10	VIN_UVP	Indicates whether V_{IN} under-voltage protection (UVP) has occurred. 1'b0: No V_{IN} UVP has occurred 1'b1: V_{IN} UVP has occurred
9	VIN_OVP	Indicates whether V_{IN} over-voltage protection (OVP) has occurred. 1'b0: No V_{IN} OVP has occurred 1'b1: V_{IN} OVP has occurred
8	VIN_UVLO	Indicates whether V_{IN} under-voltage lockout (UVLO) has occurred. 1'b0: No V_{IN} UVLO has occurred 1'b1: V_{IN} UVLO has occurred
7:6	RESERVED	Fixed to 0.
5	OTP_R3	Indicates whether rail 3 OTP has occurred. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
4	OCP_TDC_R3	Indicates whether rail 3 OCP_TDC has occurred. 1'b0: No OCP_TDC fault has occurred 1'b1: An OCP_TDC fault has occurred
3	OCP_SPIKE_R3	Indicates whether rail 3 OCP_SPIKE has occurred. 1'b0: No OCP_SPIKE fault has occurred 1'b1: An OCP_SPIKE fault has occurred
2	UVP_R3	Indicates whether rail 3 V_{OUT} UVP has occurred. 1'b0: No V_{OUT} UVP has occurred 1'b1: V_{OUT} UVP has occurred
1	VID_OVP_R3	Indicates whether rail 3 V_{OUT} VID OVP has occurred. 1'b0: No V_{OUT} VID OVP has occurred 1'b1: V_{OUT} VID OVP has occurred

0	ABSOLUTE_OVP_R3	Indicates whether rail 3 V_{OUT} ABS OVP has occurred. 1'b0: No V_{OUT} ABS OVP has occurred 1'b1: V_{OUT} ABS OVP has occurred

FAULTS_RECORD1 (F0h)

The FAULTS_RECORD1 command on Page 1 records the latest fault information for the MP2927.

Command	FAULTS_RECORD1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X		X	X		X								

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	CS10_FAULT_FLAG	Indicates whether a CS10 fault has occurred. This bit is set to 1 when CS10 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
11:10	RESERVED	X indicates that writes are ignored and reads are always 0.
9	CS9_FAULT_FLAG	Indicates whether a CS9 fault has occurred. This bit is set to 1 when CS9 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
8	RESERVED	X indicates that writes are ignored and reads are always 0.
7	CS8_FAULT_FLAG	Indicates whether a CS8 fault has occurred. This bit is set to 1 when CS8 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
6	CS7_FAULT_FLAG	Indicates whether a CS7 fault has occurred. This bit is set to 1 when CS7 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
5	CS6_FAULT_FLAG	Indicates whether a CS6 fault has occurred. This bit is set to 1 when CS6 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
4	CS5_FAULT_FLAG	Indicates whether a CS5 fault has occurred. This bit is set to 1 when CS5 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
3	CS4_FAULT_FLAG	Indicates whether a CS4 fault has occurred. This bit is set to 1 when CS4 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
2	CS3_FAULT_FLAG	Indicates whether a CS3 fault has occurred. This bit is set to 1 when CS3 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred

1	CS2_FAULT_FLAG	Indicates whether a CS2 fault has occurred. This bit is set to 1 when CS2 is pulled low. 1’b0: No CS fault has occurred 1’b1: A CS fault has occurred
0	CS1_FAULT_FLAG	Indicates whether a CS1 fault has occurred. This bit is set to 1 when CS1 is pulled low. 1’b0: No CS fault has occurred 1’b1: A CS fault has occurred

FAULTS_RECORD2 (F1h)

The FAULTS_RECORD2 command on Page 1 records the latest fault information for the MP2927.

Command	FAULTS_RECORD2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	OTP_R2	Indicates whether rail 2 over-temperature protection (OTP) has occurred. 1’b0: No OTP fault has occurred 1’b1: An OTP fault has occurred
12	OCP_TDC_R2	Indicates whether rail 2 OCP_TDC has occurred. 1’b0: No OCP_TDC fault has occurred 1’b1: An OCP_TDC fault has occurred
11	OCP_SPIKE_R2	Indicates whether rail 2 OCP_SPIKE has occurred. 1’b0: No OCP_SPIKE fault has occurred 1’b1: An OCP_SPIKE fault has occurred
10	UVP_R2	Indicates whether rail 2 V_{OUT} under-voltage protection (UVP) has occurred. 1’b0: No V_{OUT} UVP has occurred 1’b1: V_{OUT} UVP has occurred
9	VID_OVP_R2	Indicates whether rail 2 V_{OUT} VID over-voltage protection (OVP) has occurred. 1’b0: No V_{OUT} VID OVP has occurred 1’b1: V_{OUT} VID OVP has occurred
8	ABSOLUTE_OVP_R2	Indicates whether rail 2 V_{OUT} ABS OVP has occurred. 1’b0: No V_{OUT} ABS OVP has occurred 1’b1: V_{OUT} ABS OVP has occurred
7:6	RESERVED	Fixed to 0.
5	OTP_R1	Indicates whether rail 1 over-temperature protection (OTP) has occurred. 1’b0: No OTP fault has occurred 1’b1: An OTP fault has occurred
4	OCP_TDC_R1	Indicates whether rail 1 OCP_TDC has occurred. 1’b0: No OCP_TDC fault has occurred 1’b1: An OCP_TDC fault has occurred

3	OCP_SPIKE_R1	Indicates whether rail 1 OCP_SPIKE has occurred. 1'b0: No OCP_SPIKE fault has occurred 1'b1: An OCP_SPIKE fault has occurred
2	UVP_R1	Indicates whether rail 1 V_{OUT} UVP has occurred. 1'b0: No V_{OUT} UVP has occurred 1'b1: V_{OUT} UVP has occurred
1	VID_OVP_R1	Indicates whether rail 1 V_{OUT} VID OVP has occurred. 1'b0: No V_{OUT} VID OVP has occurred 1'b1: V_{OUT} VID OVP has occurred
0	ABSOLUTE_OVP_R1	Indicates whether rail 1 V_{OUT} ABS OVP has occurred. 1'b0: No V_{OUT} ABS OVP has occurred 1'b1: V_{OUT} ABS OVP has occurred

FAULTS_RECORD3 (F2h)

The FAULTS_RECORD3 command on Page 1 records the latest fault information for the MP2927.

Command	FAULTS_RECORD3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM1_FAULTS				PWM2_FAULTS				PWM3_FAULTS				PWM4_FAULTS			

Bits	Bit Name	Description
15:12	PWM1_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 1-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM2_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 2-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM3_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 3-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM4_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 4-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULTS_RECORD4 (F3h)

The FAULTS_RECORD4 command on Page 1 records the latest fault information for the MP2927.

Command	FAULTS_RECORD4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM5_FAULTS				PWM6_FAULTS				PWM7_FAULTS				PWM8_FAULTS			

Bits	Bit Name	Description
15:12	PWM5_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 5-phase operation. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
11:8	PWM6_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 6-phase operation. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
7:4	PWM7_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 7-phase operation. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
3:0	PWM8_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 8-phase operation. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current-limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection

FAULTS_RECORD5 (F4h)

The FAULTS_RECORD5 command on Page 1 records the latest fault information for the MP2927.

Command	FAULTS_RECORD5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	MFR_RESERVED				PWM9_FAULTS				MFR_RESERVED				PWM10_FAULTS			

Bits	Bit Name	Description
15:12	MFR_RESERVED	Reserved.

11:8	PWM9_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 9-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	MFR_RESERVED	Reserved.
3:0	PWM10_FAULTS	Indicates whether an Intelli-Phase™ fault (and its type) has occurred during 10-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULTS_RECORD6 (F5h)

The FAULTS_RECORD6 command on Page 1 records the latest fault information for the MP2927.

Command	FAULTS_RECORD6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:13	RESERVED	Fixed to 0.
12	PROCHOT_FAULT	Indicates whether a PROCHOT fault v. 1'b0: No PROCHOT fault has occurred 1'b1: A PROCHOT fault has occurred
11	CHIP_OTP_FLAG	Indicates whether chip over-temperature protection (OTP) has occurred. 1'b0: No chip OTP 1'b1: Chip OTP has occurred
10	VIN_UVP	Indicates whether V_{IN} under-voltage protection (UVP) has occurred. 1'b0: No V_{IN} UVP has occurred 1'b1: V_{IN} UVP has occurred
9	VIN_OVP	Indicates whether V_{IN} over-voltage protection (OVP) has occurred. 1'b0: No V_{IN} OVP has occurred 1'b1: V_{IN} OVP has occurred
8	VIN_UVLO	Indicates whether V_{IN} under-voltage lockout (UVLO) has occurred. 1'b0: No V_{IN} UVLO has occurred 1'b1: V_{IN} UVLO has occurred
7:6	RESERVED	Fixed to 0.
5	OTP_R3	Indicates whether rail 3 OTP has occurred. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred

4	OCP_TDC_R3	Indicates whether rail 3 OCP_TDC has occurred. 1'b0: No OCP_TDC fault has occurred 1'b1: An OCP_TDC fault has occurred
3	OCP_SPIKE_R3	Indicates whether rail 3 OCP_SPIKE has occurred. 1'b0: No OCP_SPIKE fault has occurred 1'b1: An OCP_SPIKE fault has occurred
2	UVP_R3	Indicates whether rail 3 V_{OUT} UVP has occurred. 1'b0: No V_{OUT} UVP has occurred 1'b1: V_{OUT} UVP has occurred
1	VID_OVP_R3	Indicates whether rail 3 V_{OUT} VID OVP has occurred. 1'b0: No V_{OUT} VID OVP has occurred 1'b1: V_{OUT} VID OVP has occurred
0	ABSOLUTE_OVP_R3	Indicates whether rail 3 V_{OUT} ABS OVP has occurred. 1'b0: No V_{OUT} ABS OVP has occurred 1'b1: V_{OUT} ABS OVP has occurred

ADC_SUM_RESET (FBh)

The ADC_SUM_RESET command on Page 1 resets the ADC_SUM count.

This command is write-only. There is no data byte for this command.

CLEAR_CRC_FAULT (FCh)

The CLEAR_CRC_FAULT command on Page 1 clears the CRC fault information that is stored in NVM Page 28.

This command is write-only. There is no data byte for this command.

CLEAR_STORED_FAULTS (FEh)

The CLEAR_STORED_FAULTS command on Page 1 clears the last fault information that is stored in NVM, Page 28.

This command is write-only. There is no data byte for this command.

CLEAR_NVM_FAULTS (FFh)

The CLEAR_NVM_FAULTS command on Page 1 clears any NVM faults.

This command is write-only. There is no data byte for this command.

PAGE 2 REGISTER MAP

OPERATION_R3 (01h)

The OPERATION_R3 command on Page 2 turns the rail 3 output on and off in conjunction with the input from EN pin, and sets V_{OUT} to the upper or lower margin voltages. The controller stays in the OPERATION command setting mode until a subsequent OPERATION command is received, or a change to EN sets rail 3 to another mode.

Command	OPERATION_R3							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OPERATION_R3							

Bits	Bit Name	Description
7:0	OPERATION_R3	Sets the operation mode for rail 3. 8’b 00xx xxxx: Hi-Z off 8’b 01xx xxxx: Soft shutdown 8’b 1000 xxxx: Normal on 8’b 1001 xxxx: Margin low 8’b 1010 xxxx: Margin high 8’b 1011 xxxx: AVSBus mode Others: Invalid commands “x” means not applicable.

STORE_ALL_CODE (15h)

The STORE_ALL_CODE command on Page 2 instructs the PMBus device to copy all the Page 0, Page 1, and Page 2 contents, including the internal trim registers, from the operating memory to the matching locations in the NVM. Any items in the operating memory that do not have matching locations in the NVM are ignored.

This command is controlled by 50h (Page 1), bits[7:0]. 50h, bits[7:0] must be set to 0x63 to write to the NVM. If it is any other value, the NVM is write-protected.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command on Page 2 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents, including the internal trim registers, from the NVM and overwrite the matching locations in the operating memory. Any items in the user store that do not have matching locations in the operating memory are ignored.

This command cannot be used while the device is outputting power, and is ignored if attempted.

This command is write-only. There is no data byte for this command.

STORE_USER_CODE (17h)

The STORE_USER_CODE command on Page 1 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the operating memory to the matching locations in the NVM (excluding the trim registers). Any items in the operating memory that do not have matching locations in the NVM are ignored.

This command is controlled by 50h (Page 1), bits[7:0]. Bits[7:0] must be set to 0x63 to write to the NVM. If it is any other value, the NVM is write-protected.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_USER_CODE (18h)

The RESTORE_USER_CODE command on Page 1 instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the NVM and to overwrite the matching locations in the operating memory. Any items in the user store that do not have matching locations in the operating memory are ignored. Trim registers are not overwritten by this command.

This command cannot be used while the device is outputting power, and is ignored if attempted.

This command is write-only. There is no data byte for this command.

VOUT_COMMAND_R3 (21h)

The VOUT_COMMAND_R3 command on Page 2 sets the rail 3 V_{REF} VID in PMBus override mode.

Command	VOUT_COMMAND_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_COMMAND_R3										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_COMMAND_R3	Sets the rail 3 V_{REF} (VID_DAC V_{OUT}) in PMBus VID mode. 1 VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits [15:14].

VOUT_TRIM_R3 (22h)

The VOUT_TRIM_R3 command on Page 2 applies a fixed offset voltage to the commanded rail 3 V_{OUT}.

Command	VOUT_TRIM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	VOUT_TRIM_R3								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRIM_R3	Sets the V_{OUT} offset voltage on rail 3. VID_STEP/LSB.

VDIFF1_SNAPSHOT (23h)

The VDIFF1_SNAPSHOT command on Page 2 returns the snapshot D4h value (on Page 0) when reading the D3h (on Page 0) value.

Command	VDIFF1_SNAPSHOT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	VDIFF1_SNAPSHOT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

9:0	VDIFF1_SNAPSHOT	Returns the snapshot V_{OUT} ADC value while reading D3h (on Page 0). This value is updated from D4h (on Page 0) while reading D3h (on Page 0). 1.56mV/LSB when V_{DIFF} gain = 1 3.12mV/LSB when V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 1), bit[10].

VOUT_MAX_R3 (24h)

The VOUT_MAX_R3 command on Page 2 sets the maximum V_{REF} for rail 3 VID-DAC, which sets the maximum V_{OUT}. When an external resistor divider is applied, the maximum voltage is clamped to VOUT_MAX / K_R. Where K_R is the dividing ratio for the external resistor divider. This command is effective in PMBus mode.

Command	VOUT_MAX_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_MAX_R3										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MAX_R3	Set the rail 3 maximum VID + offset voltage. This limits the sum of VID + the VOUT_TRIM offset. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits[15:14].

MFR_JOUT_LONG_TERM_R3 (25h)

The MFR_JOUT_LONG_TERM_R3 command on Page 2 sets the rail 3 long-term value to calculate J_{OUT}.

Command	MFR_JOUT_LONG_TERM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	JOUT_LONG_TERM									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	JOUT_LONG_TERM	Sets the long-term value for the J_{OUT} calculation, calculated with the following equation: LONG_TIME = JOUT_LONG_TERM x SHORT_TIME

MFR_JOUT_SHORT_TERM_R3 (26h)

The MFR_JOUT_SHORT_TERM_R3 command on Page 1 sets the rail 3 short-term value to calculate J_{OUT}.

Command	MFR_JOUT_SHORT_TERM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X		JOUT_SHORT_TERM_FIX_FREQ						JOUT_SHORT_TERM_ADAPTIVE_FREQ						

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	JOUT_EN	Enables the J_{OUT} function. 1'b1: Enabled 1'b0: Disabled
12:7	JOUT_SHORT_TERM_FIX_FREQ	Bits[12:7] are fixed to 0 in fixed-frequency mode.
6:0		Bits[6:0] set JOUT_SHORT_TERM in the fixed-frequency mode. ADC_TIME/LSB. The short-term value can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_FIX_FREQ x ADC_TIME
12:1	JOUT_SHORT_TERM_ADAPTIVE_FREQ	50ns/LSB in adjustable-frequency mode. The short-term value can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_ADAPTIVE_FREQ x 50ns
0		Bit[0] is fixed to 0 in adjustable-frequency mode.

VOUT_TRANSITION_RATE_R3 (27h)

The VOUT_TRANSITION_RATE_R3 command on Page 2 sets the rail 3 dynamic VID (DVID) transition slew rate and EN soft-shutdown slew rate in PMBus mode.

Command	VOUT_TRANSITION_RATE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	VOUT_TRANSITION_RATE_R3												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	VOUT_TRANSITION_RATE_R3	Set the rail 3 DVID transition slew rate and the EN soft-shutdown slew rate in PMBus mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h), bit[15].

VOUT_DROOP_R3 (28h)

The VOUT_DROOP_R3 on Page 1 sets the load-line parameters for rail 3.

Command	VOUT_DROOP_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function											RDROOP_SET_R3					

Bits	Bit Name	Description
15	IACDROOP_BW_SET_R3	Enables the device to reduce the AC droop bandwidth (BW) by reducing the bias current. This is for rail 3 only. 1'b0: Disabled 1'b1: Enabled
14	IACDROOP_BW_SET_R3	Enables the device to reduce the AC droop BW by increasing the compensation capacitor. This is for rail 3 only. 1'b0: Disabled 1'b1: Enabled

13	IACDROOP_GAIN2_SET_R3	Sets the PMBus load-line slope (AC droop) level; active when bit[12] of this command = 1. 1'b0: 1 x IDROOP_INI 1'b1: 1/2 x IDROOP_INI
12	MFR_ACLL_EN_R3	Selects the AC or DC load line. 1'b0: DC load line 1'b1: AC load line
11:9	PMBUS_LL_LEVEL_R3	Sets the PMBus load-line slope (DC droop) level; active when bit[12] of this command = 1. The MP2927 provides 8 levels for DC droop. 3'b000: 0 3'b001: 3/4 x IDROOP_INI 3'b010: 4/4 x IDROOP_INI 3'b011: 5/4 x IDROOP_INI 3'b100: 6/4 x IDROOP_INI 3'b101: 7/4 x IDROOP_INI 3'b110: 8/4 x IDROOP_INI 3'b111: 9/4 x IDROOP_INI
8:7	IDROOP_GAIN1_SET_R3	Sets the IDROOP gain for rail 3. 2'b00: 1/16 x IDROOP_INI 2'b01: 1/8 x IDROOP_INI 2'b10: 1/4 x IDROOP_INI 2'b11: 1/2 x IDROOP_INI
6	SHORT_FIRST_HALF_R3	Set this bit to 1 if R_{DROOP} is below 3.2Ω. 1'b0: Do not short the first half of the rail 3 resistors 1'b1: Short the first half of the rail 3 resistors
5:0	RDROOP_SET_R3	Sets the R_{DROOP} for rail 3. 100Ω/LSB. 6.4kΩ maximum.

VOUT_SCALE_LOOP_R3 (29h)

The VOUT_SCALE_LOOP_R3 command on Page 2 sets the rail 3 output voltage (V_{OUT}) to reference voltage (V_{REF}) dividing ratio when an external output divider is applied.

Command	VOUT_SCALE_LOOP_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	VOUT_SCALE_LOOP_R3							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VOUT_SCALE_LOOP_R3	Sets the rail 3 V_{OUT} to V_{REF} dividing ratio. V_{REF} ranges from 0V to 1.6V.

MFR_SETTLE_CTRL_R3 (2Ah)

The MFR_SETTLE_CTRL_R3 command on Page 2 sets the DVID parameters for rail 3.

Command	MFR_SETTLE_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_DROOPFALL_DELAY_R3					MFR_RISE_STEP_R3					RESERVED					

Bits	Bit Name	Description
15:11	MFR_DROOPFALL_ DELAY_R3	Sets the delay time between V_{REF} reaching the target (VID + DROOP_VID) and V_{REF} falling back to VID. 50ns/LSB.
10:6	MFR_RISE_STEP_R3	Sets the extra VID steps count for rail 3 when DVID goes up. The extra VID steps are used to compensate the droop created when the output capacitor charges during DVID up. 1 step/LSB.
5:0	RESERVED	Fixed to 0.

VOUT_MIN_R3 (2Bh)

The VOUT_MIN_R3 command on Page 2 instructs the device to limit the rail 3 minimum V_{OUT} in PMBus mode. When the V_{OUT} decoded from the PMBus interface is below the value set by VOUT_MIN (2Bh), V_{OUT} is clamped to VOUT_MIN. When an external resistor divider is applied on VOSEN, the minimum V_{OUT} is clamped to VOUT_MIN / K_R. Where K_R is the dividing ratio of the divider.

Command	VOUT_MIN_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_MIN_R3										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MIN_R3	Sets the minimum VID under PMBus mode for rail 3. Any VID below this value is clamped to VOUT_MIN. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h), bits [15:14].

MFR_TRIM_DCM_1P_2P_R3 (2Ch)

The MFR_TRIM_DCM_1P_2P_R3 command on Page 2 trims the output voltage in 1-phase CCM or DCM. This is for the rail 3 power state.

Command	MFR_TRIM_DCM_1P_2P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	MFR_TRIM_2PS_R3					MFR_TRIM_1PS_R3					MFR_TRIM_DCM_R3				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	MFR_TRIM_2PS_R3	Unused. fixed to 0.
9:5	MFR_TRIM_1PS_R3	Set the V_{OUT} trim for 1-phase CCM on rail 3. 2.3mV/LSB.
4:0	MFR_TRIM_DCM_R3	Sets the V_{OUT} trim for 1-phase DCM on rail 3. 2.3mV/LSB.

MFR_PMBUS_VTH (2Dh)

The MFR_PMBUS_VTH command on Page 2 sets the PMBus logic level.

Command	MFR_PMBUS_VTH															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	MFR_PMB_THH_SET						MFR_PMB_THL_SET					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	MFR_PMB_THH_SET	Sets the PMBus logic high threshold. 0V to 2.56V, 40mV/LSB.
5:0	MFR_PMB_THL_SET	Sets the PMBus logic low threshold. 0V to 2.56V. 40mV/LSB.

MFR_AVS_SET2 (2Eh)

The MFR_AVS_SET2 command on Page 2 sets AVSBus parameters.

Command	MFR_AVS_SET2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	AVSBUS_MODE	Enables AVSBus mode. 1’b0: Disabled 1’b1: Enabled
12	AVS_CMP_TH_SEL	Select the AVS CMP threshold. 1’b0: The VDDIO voltage and resistor divider 1’b1: The DACs
11:6	AVS_CMP_TH_HIGH	0V to 2.56V. 40mV/LSB.
5:0	AVS_CMP_TH_LOW	0V to 2.56V. 40mV/LSB.

MFR_CP_SET (2Fh)

The MFR_CP_SET command on Page 2 sets the parameters for the couple inductor.

Command	MFR_CP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:5	RESERVED	Fixed to 0.
4	MFR_PH1_CP_EN	Fixed to 1.
3	MFR_CP_82PART	Fixed to 1.
2	MFR_APS_SD_MODE_R3	Fixed to 0.
1	MFR_APS_SD_MODE_R2	Fixed to 0.
0	MFR_APS_SD_MODE_R1	Enables the rail 1 couple inductor. 1’b0: Disabled 1’b1: Enabled

MFR_PMBUS_TIMEOUT2 (30h)

The MFR_PMBUS_TIMEOUT2 command on Page 2 sets parameters for PMBus TIMEOUT2.

Command	MFR_PMBUS_TIMEOUT2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:9	RESERVED	Fixed to 0.
8	TIMEOUT2_PROTECT_EN	Enables PMBus pack-to-pack timeout protection. 1’b0: Disabled 1’b1: Enabled
7	MFR_PMBUS_TIMEOUT2_SEL	Sets the target data resolution for the PMBus-pack to-pack timeout protection counter. 1’b0: 100µs x 128 1’b1: 200ns x 128
6:0	MFR_PMBUS_TIMEOUT2_DATA	Sets the target data for the PMBus pack-to-pack timeout protection counter.

MFR_BLANK_TIME1_R3 (31h)

The MFR_BLANK_TIME1_R3 command on Page 2 configures the slope compensation reset time and PWM blanking time between two consecutive phases. It is for rail 3 only.

Command	MFR_BLANK_TIME1_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED				MFR_SLOPE_BLANK_TIME1_R3						MFR_PHASE_BLANK_TIME1_R3					

Bits	Bit Name	Description
15:12	RESERVED	Fixed to 0.
11:6	MFR_SLOPE_ BLANK_TIME1_R3	Configures the slope compensation reset time. Note that the slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME (MFR_BLANK_TIME1 (31h on Page 2), bits[5:0]). 5ns/LSB. The blank time can be calculated with the following equation: MFR_SLOPE_BLANK_TIME1_R3 = (bits[11:6] x 5 + 25) ns
5:0	MFR_PHASE_ BLANK_TIME1_R3	Configures the PWM blanking times between two consecutive phases. 5ns/LSB. The PWM blank time can be calculated with the following equation: MFR_PHASE_BLANK_TIME1_R3 = (bits[5:0] x 5 + 25) ns

MFR_PI_LOOP (32h)

The MFR_PI_LOOP command on Page 2 sets the integral parameter for the current balance loop and DC loop.

Command	MFR_PI_LOOP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X				CURRENT_SHARE_LOOP				VOUT_DC_LOOP						

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:11	FREQUENCY_LOOP	Sets the frequency loop parameters. The default value is 2.
10:7	CURRENT_SHARE_LOOP	Sets the current share loop parameters. The default value is 2.
6:0	VOUT_DC_LOOP	Sets the V_{OUT} DC loop parameters. The default value is 16.

FREQUENCY_SWITCH_R3 (33h)

The FREQUENCY_SWITCH_R3 command on Page 2 sets the rail 3 switching frequency (f_{SW}). f_{SW} can be set between 200kHz and 5.11MHz, with 10kHz per step.

Command	FREQUENCY_SWITCH_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	FREQUENCY_SWITCH_R3								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	FREQUENCY_SWITCH_R3	Sets the switching frequency (f_{SW}) in direct format. 10kHz/LSB.

MFR_OSR_SET_R3 (34h)

The MFR_OSR_SET_R3 command on Page 2 sets the overshoot reduction (OSR) parameters for rail 3.

Command	MFR_OSR_SET_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				MFR_OSR_FILTER_R3						MFR_OSR_BLANKTIME_R3						

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	MFR_OSR_EN_R3	Enables overshoot reduction (OSR). This function can reduce the V_{OUT} overshoot when the load is released. 1'b0: Disabled 1'b1: Enabled
12:7	MFR_OSR_FILTER_R3	Sets the minimum OSR duration time. 5ns/LSB.
6:0	MFR_OSR_ BLANKTIME_ R3	Sets the blanking time between two effective OSR events. 10ns/LSB.

MFR_AVD_SET (35h)

The MFR_AVS_SET command is used to set the AVSBUS parameters.

Command	MFR_AVS_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		MFR_AVS_ADDR_R3					MFR_AVS_ADDR_R2					MFR_AVS_ADDR_R1				

Bits	Bit Name	Description
15	MFR_AVS VDDIO_EN	1’b0: Set the AVS CMP threshold using DACs 1’b1: Set the AVS CMP threshold using the VDDIO voltage and resistor divider
14:11	MFR_AVS_ADDR_R3	Sets the AVSBus slave address for rail 3.
10	MFR_AVS_EN_R3	1’b0: Rail 3 does not follow AVSBus commands 1’b1: Rail 3 follows AVSBus commands when OPERATION_R3 is set to 0xB0
9:6	MFR_AVS_ADDR_R2	Sets the AVSBus slave address for rail 2.
5	MFR_AVS_EN_R2	1’b0: Rail 2 does not follow AVSBus commands 1’b1: Rail 2 follows AVSBus commands when OPERATION_R2 is set to 0xB0
4:1	MFR_AVS_ADDR_R1	Sets the AVSBus slave address for rail 1.
0	MFR_AVS_EN_R1	1’b0: Rail 1 does not follow AVSBus commands 1’b1: Rail 1 follows AVSBus commands when OPERATION_R1 is set to 0xB0

MFR_AVS_WARN_MASK (36h)

The MFR_AVS_WARN_MASK command on Page 2 sets some masks.

Command	MFR_AVS_WARN_MASK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:5	RESERVED	Fixed to 0.
4	AVS_VR_UNSETTLE_ MASK	Masks the VR unsettle flag that triggers a slave to issue a status response frame to the CPU. 1’b0: No mask 1’b1: Masked
3	AVS_OC_WARN_MASK	Masks the over-current (OC) warning flag that triggers a slave to issue a status response frame to the CPU. 1’b0: No mask 1’b1: Masked
2	AVS_UV_WARN_MASK	Masks the under-voltage (UV) warning flag that triggers a slave to issue a status response frame to the CPU. 1’b0: No mask 1’b1: Masked
1	AVS_OP_WARN_MASK	Masks the over-power (OP) warning flag that triggers a slave to issue a status response frame to the CPU. 1’b0: No mask 1’b1: Masked
0	AVS_OT_WARN_MASK	Mask the over-temperature (OT) warning flag that triggers a slave to issue a status response frame to the CPU. 1’b0: No mask 1’b1: Masked

MFR_SLOPE_SW_INI_R3 (37h)

The MFR_SLOPE_SW_INI_R3 command on Page 2 sets rail 3's initial ramp for soft start.

Command	MFR_SLOPE_SW_INI_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	MFR_VOUT_FINE_TUNE_R3						MFR_SLOPE_SW_INI_R3						

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	MFR_VOUT_FINE_TUNE_R3	Sets the V_{OUT} fine-tune value. The trim value is per step. Bit[12] is the signed bit. 0.64mV/LSB when V_{DIFF} gain = 1 0.96mV/LSB when V_{DIFF} gain = 1/2
6:0	MFR_SLOPE_SW_INI_R3	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_DCM_R3 (38h)

The MFR_SLOPE_SR_DCM_R3 command on Page 2 sets the rail 3 slope compensation slew rate in 1-phase DCM.

Command	MFR_SLOPE_SR_DCM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_1P_R3 (39h)

The MFR_SLOPE_SR_1P_R3 command on Page 2 provides 2 bytes to configure slope compensation for 1-phase CCM. It is for rail 3 only.

Command	MFR_SLOPE_SR_1P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_2P_R3 (3Ah)

The MFR_SLOPE_SR_2P_R3 command on Page 2 is reserved.

Command	MFR_SLOPE_SR_2P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Unused. Fixed to 0.
5:0	CURRENT_SOURCE	Unused. Fixed to 0.

SR_LIMIT_1MV (3Bh)

The SR_LIMIT_1MV command on Page 2 limits the AVSBus slew rate.

Command	SR_LIMIT_1MV															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED									AVS_SR_LIMIT_1MV						

Bits	Bit Name	Description
15:7	RESERVED	Fixed to 0.
6:0	AVS_SR_LIMIT_1MV	Sets the limit for the AVSBus DVID slew rate 1mV/µs/LSB.

MFR_TRIM_SEL (3Ch)

The MFR_TRIM_SEL command on Page 2 sets the trim selection.

Command	MFR_TRIM_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:12	MFR_DROP_TRIM_SEL_R2	Sets the C1h~CBh values in Page 1 and the 0Ah~0Dh values in Page 2. There are 16 backup trim registers (the I_{DROOP} trim registers) for rail 2.
11:8	MFR_DROP_TRIM_SEL_R1	Sets the C1h~CBh values in Page 1 and the 0Ah~0Dh values in Page 2. There are 16 backup trim registers (the I_{DROOP} trim registers) for rail 1.
7:4	MFR_IMON_TRIM_SEL_R2	Sets the C1h~CBh values in Page 1 and the 0Ah~0Dh values in Page 2. There are 16 backup trim registers (the IMON trim registers) for rail 2.
3:0	MFR_IMON_TRIM_SEL_R1	Sets the C1h~CBh values in Page 1 and the 0Ah~0Dh values in Page 2. There are 16 backup trim registers (the IMON trim registers) for rail 1.

MFR_TRIM_SEL_R3 (3Dh)

The MFR_TRIM_SEL_R3 command on Page 2 sets the trim selection.

Command	MFR_TRIM_SEL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:4	MFR_DROP_TRIM_SEL_R3	Sets the C1h~CBh values in Page 1 and the 0Ah~0Dh values in Page 2. There are 16 backup trim registers (the I_{DROOP} trim registers) for rail 3.
3:0	MFR_IMON_TRIM_SEL_R3	Sets the C1h~CBh values in Page 1 and the 0Ah~0Dh values in Page 2. There are 16 backup trim registers (the IMON trim registers) for rail 3.

MFR_RESERVED (3Eh)

The MFR_RESERVED command on Page 2 is reserved.

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X		MFR_VRHOT_LIMIT_R3							

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_VRHOT_EN_R3	Fixed to 0.
7:0	MFR_VRHOT_LIMIT_R3	Reserved.

MFR_RESERVED (3Fh)

The MFR_RESERVED command on Page 2 is reserved.

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED															

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

VOUT_OV_FAULT_LIMIT_R3 (40h)

The VOUT_OV_FAULT_LIMIT_R3 command on Page 1 sets the V_{OUT} over-voltage protection (OVP) threshold for rail 3.

Command	VOUT_OV_FAULT_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X				OVP_ABS_SET_R3							

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	OVP_VID_SET_R3	Sets the over-voltage protection (OVP) VID threshold. 3'b001: V_{REF} + 200mV 3'b010: V_{REF} + 325mV 3'b100: V_{REF} + 450mV Others: Invalid
7:0	OVP_ABS_SET_R3	Sets an absolute OVP threshold. If V_{OUT} exceeds this value, OVP occurs. 10mV/LSB.

VOUT_OV_FAULT_RESPONSE_R3 (41h)

The VOUT_OV_FAULT_RESPONSE_R3 command on Page 2 sets protection mode and delay time if a V_{OUT} over-voltage (OV) fault occurs. It is for rail 3 only.

Command	VOUT_OV_FAULT_RESPONSE_R3															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X				MFR_OVP_VID_DELAYTIME_R3					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OVP_ABS_EN_R3	Enabled absolutely over-voltage protection (ABS_OVP) for rail 3. 1'b0: Disabled 1'b1: Enabled
7:6	MFR_OVP_VID_ MODE_R3	Set the over-voltage (OV) fault mode. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	MFR_OVP_VID_ DELAYTIME_R3	Sets the VID OVP blanking time. If a VID OVP condition remains for longer than the OVP_VID blanking time, a VID OVP fault occurs. 100ns/LSB.

VOUT_MAX_ALERT_R3 (42h)

The VOUT_MAX_ALERT_R2 command on Page 2 sets the V_{OUT} over-voltage (OV) warning threshold or returns the maximum V_{OUT} for rail 3. The function is determined by GPIO_ACTIVE (68h), bit[13].

Command	VOUT_MAX_ALERT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_MAX_ALERT_R3															

Bits	Bit Name	Description
15:0	VOUT_MAX_ALERT_R3	If GPIO_ACTIVE (68h) bit[13] set to 0, this command sets the V_{OUT} over-voltage (OV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] set to 1, this command returns the maximum V_{OUT}. The maximum value can be written with a lower value, and if a higher V_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x0000 to reset this command. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 2), bit[10].

VOUT_MIN_ALERT_R3 (43h)

The VOUT_MIN_ALERT_R3 command on Page 2 sets the V_{OUT} under-voltage (UV) warning threshold or returns the minimum V_{OUT} for rail 3. The function is determined by GPIO_ACTIVE (68h), bit[13].

Command	VOUT_MIN_ALERT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_MIN_ALERT_R3															

Bits	Bit Name	Description
15:0	VOUT_MIN_ALERT_R3	If GPIO_ACTIVE (68h) bit[13] set to 0, this command sets the V_{OUT} under-voltage (UV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] set to 1, this command returns the minimum V_{OUT}. This command can be written with a higher value, and if a lower V_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x03FF to reset this command. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 1), bit[10].

VOUT_UV_FAULT_LIMIT_R3 (44h)

The VOUT_UV_FAULT_LIMIT_R3 command on Page 2 sets the V_{OUT} under-voltage (UV) fault threshold for rail 3.

Command	VOUT_UV_FAULT_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	UVP_VID_SET_R3			RESERVED							

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	UVP_VID_SET_R3	Sets the under-voltage protection (UVP) threshold. 3'b000: V_{REF} - 425mV 3'b001: V_{REF} - 375mV 3'b010: V_{REF} - 325mV 3'b011: V_{REF} - 275mV 3'b100: V_{REF} - 225mV 3'b101: V_{REF} - 175mV 3'b110: V_{REF} - 125mV 3'b111: V_{REF} - 75mV
7:0	RESERVED	Fixed to 0.

VOUT_UV_FAULT_RESPONSE_R3 (45h)

The VOUT_UV_FAULT_RESPONSE_R3 on Page 2 sets the V_{OUT} under-voltage (UV) fault response for rail 3.

Command	VOUT_UV_FAULT_RESPONSE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X				MFR_UVP_DELAYTIME_R3					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_UV_VID_EN_R3	Enables VID under-voltage protection (UVP). 1'b0: Disabled 1'b1: Enabled
7:6	MFR_UVP_MODE_R3	Sets the V_{OUT} UVP mode. 2'b00: No action 2'b01: Latch off mode 2'b10: Hiccup mode 2'b11: Retry 6 times
5:0	MFR_UVP_ DELAYTIME_R3	Sets the V_{OUT} UVP blanking time. A UVP fault occurs if the sensed V_{DIFF} falls below the UVP threshold for the UVP blanking time. 100ns/LSB.

IOUT_OC_FAULT_LIMIT_R2 (46h)

The IOUT_OC_FAULT_LIMIT_R3 command on Page 2 sets the rail 3 I_{OUT} over-current (OC) fault threshold.

Command	IOUT_OC_FAULT_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OCP_SPIKE_SET_R3								OCP_TDC_SET_R3							

Bits	Bit Name	Description
15:8	OCP_SPIKE_SET_R3	Sets the rail 3 OCP_SPIKE_TOTAL current level DAC value. 6.25mV/LSB. OVP_SPIKE_TOTAL can be calculated with the following equation: $OCP\_SPIKE\_TOTAL = OCP\_SPIKE \times K_{CS} \times G_{IMON} \times R_{IMON} / 6.25$
7:0	OCP_TDC_SET_R3	Sets the rail 3 OCP_TDC_TOTAL current level. The high 8MSB of the IMON ADC result via IMON1_SENSE, bits[9:0] is compared to this value. 6.25mV/LSB. OCP_TDC_TOTAL can be calculated with the following equation: $OCP\_TDC\_TOTAL = OCP\_TDC \times K_{CS} \times G_{IMON} \times R_{IMON} / 6.25$

IOUT_OC_FAULT_RESPONSE_R3 (47h)

The IOUT_OC_FAULT_RESPONSE_R3 command on Page 2 sets the rail 3 over-current protection (OCP) options and values.

Command	IOUT_OC_FAULT_RESPONSE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									MFR_OCPTDC_TRIG_DELAY_R3							

Bits	Bit Name	Description
15:14	MFR_OCP_MODE_R3	Selects the over-current protection (OCP) mode for both OCP_TDC and OCP_SPIKE. 2'b00: No action 2'b01: Latch off mode 2'b10: Hiccup mode 2'b11: Retry 6 times
13	MFR_OCP_TDC_EN_R3	Enables OCP_TDC. 1'b0: Disabled 1'b1: Enabled
12:8	MFR_OCPTDC_ACTION_DELAY_R3	Sets the OCP_TDC fault action time. This is the delay between OCP_L signal assertion and current limiting, hiccup mode entry, or shutdown. 1µs/LSB.
7:0	MFR_OCPTDC_TRIG_DELAY_R3	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for the OCP_TDC blanking time. 20µs/LSB.

IOUT_OC_SPIKE_RESPONSE_R3 (48h)

The IOUT_OC_SPIKE_RESPONSE_R3 command on Page 2 sets the over-current (OC) spike options and values.

Command	IOUT_OC_SPIKE_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OCP_SPIKE_EN_R3	Enables OCP_SPIKE. 1'b0: Disabled 1'b1: Enabled
7:4	MFR_OCPSPIKE_ ACTIONDELAY_R3	Sets the OCP_SPIKE fault action delay time. This is time is between OCP_L assertion (after exceeding current threshold relative to IDDSpike) and current limiting, hiccup mode entry, or shutdown. 1µs/LSB.
3:0	MFR_OCPSPIKE_ TRIGDELAY_R3	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for an OCP_SPIKE blanking time. 200ns/LSB.

MFR_OCP_PHASE_LIMIT_R3 (49h)

The MFR_OCP_PHASE_LIMIT_R3 command on Page 2 sets the rail 3 per-phase valley current limit. The MP2927 provides OCP_PHASE protection to limit the per-phase valley current. OCP_PHASE is implemented by monitoring and comparing the cycle-by-cycle sensed CS current with a current reference.

Command	MFR_OCP_PHASE_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED								OCP_DAC_SET_R3							

Bits	Bit Name	Description
15:8	RESERVED	Unused. Fixed to 0.
7:0	OCP_DAC_SET_R3	Sets the per-phase valley current limit DAC value. 5mV/LSB.

IOUT_MAX_ALERT_R3 (4Ah)

The IOUT_MAX_ALERT_R3 command on Page 2 sets the I_{OUT} over-current (OC) warning threshold or returns the peak value of I_{OUT}. It is for rail 3 only. It is determined by GPIO_ACTIVE (68h), bit[13].

Command	IOUT_MAX_ALERT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IOUT_MAX_ALERT_R3															

Bits	Bit Name	Description
15:0	IOUT_MAX_ALERT_R3	If GPIO_ACTIVE (68h) bit[13] set to 0, this command sets the DAC value for the I_{OUT} over-current (OC) warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h) bit[13] set to 1, this command returns the peak I_{OUT}. I_{OUT} can be written with a lower value, and if a higher I_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x0000 to reset the command. Convert the read value to the actual I_{OUT} (in A) with the following equation: $$I_{OUT}(A) = \frac{4Ah, bits[9:0]}{6Ch, bits[9:0] \times 1024} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$$ Where GAIN_SEL is set by 6Ch, bits[11:10].

MFR_FS_LIMIT_12P_R3 (4Bh)

The MFR_FS_LIMIT_12P_R3 command on Page 2 sets the rail 3 FS_LIMIT threshold for 1-phase to detect fast load insertion and exit phase-shedding.

Command	MFR_FS_LIMIT_12P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_FS_LIMIT_2P_R3								MFR_FS_LIMIT_1P_R3							

Bits	Bit Name	Description
15:8	MFR_FS_LIMIT_2P_R3	Unused. Fixed to 0.
7:0	MFR_FS_LIMIT_1P_R3	Set the PWM1 off-time threshold to exit phase-shedding. If the PWM1 off-time (after excluding MIN_OFF_TIME) is shorter than FS_LIMIT_1P, add + 1 to the count. It is effective both for DCM and CCM. 10ns/LSB.

MFR_FS_LIMIT_56P_R1 (4Ch)

The MFR_FS_LIMIT_56P_R1 command on Page 2 sets the rail 1 FS_LIMIT threshold for 5-phase and 6-phase operation to detect fast load insertion and exit phase-shedding.

Command	MFR_FS_LIMIT_56P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_FS_LIMIT_6P_R1								MFR_FS_LIMIT_5P_R1							

Bits	Bit Name	Description
15:8	MFR_FS_LIMIT_6P_R1	Sets the exit phase-shedding PWM interval time for 6-phase operation. If the time interval between two phases is shorter than FS_LIMIT_6P, add + 1 to the interval. 5ns/LSB.
7:0	MFR_FS_LIMIT_5P_R1	Sets the exit phase-shedding PWM interval time for 5-phase operation. If the time interval between two phases is shorter than FS_LIMIT_5P, add + 1 to the interval. 5ns/LSB.

MFR_APS_LEVEL_12P_R3 (4Dh)

The MFR_APS_LEVEL_12P_R3 command on Page 2 sets the rail 3 automatic phase-shedding (APS) current threshold for 1-phase CCM and DCM.

Command	MFR_APS_LEVEL_12P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_APS_IIL_1P_CCM_R3								MFR_APS_IIL_1P_DCM_R3							

Bits	Bit Name	Description
15:8	MFR_APS_IIL_1P_CCM_R3	Sets the rail 3 automatic phase-shedding (APS) current threshold for 1-phase CCM. 1A/LSB.
7:0	MFR_APS_IIL_1P_DCM_R3	Sets the rail 3 APS current threshold for 1-phase DCM. 1A/LSB.

MFR_APS_LEVEL_45P_R1 (4Eh)

The MFR_APS_LEVEL_45P_R1 command on Page 2 sets the rail 1 automatic phase-shedding (APS) current threshold for 4-phase and 5-phase operation.

Command	MFR_APS_LEVEL_45P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_LEVEL_5P								DROP_LEVEL_4P							

Bits	Bit Name	Description
15:8	DROP_LEVEL_5P	Sets the rail 1 automatic phase-shedding (APS) current threshold for 5-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_4P	Sets the rail 1 APS current threshold for 4-phase CCM. 1A/LSB.

OT_FAULT_LIMIT_R3 (4Fh)

Command	OT_FAULT_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	MFR_OTP_LIMIT_R3							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	MFR_OTP_LIMIT_R3	Reserved.

SMBALERT_MASK (50h)

The SMBALERT_MASK command on Page 2 masks faults to prevent the assertion of ALT_P#.

Command	SMBALERT_MASK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	OTP_MASK	1’b0: If over-temperature protection (OTP) occurs, ALT_P# does not assert 1’b1: No mask
14	OVP_MASK	1’b0: If over-voltage protection (OVP) occurs, ALT_P# does not assert 1’b1: No mask
13	UVP_MASK	1’b0: If under-voltage protection (UVP) occurs, ALT_P# does not assert 1’b1: No mask
12	VOUT>VMAX_ VOUT<VMIN	1’b0: If V_{OUT} exceeds V_{MAX} or drops below V_{MIN}, ALT_P# does not assert 1’b1: No mask
11	OCP_MASK	1’b0: If over-current protection (OCP) occurs, ALT_P# does not assert 1’b1: No mask
10	OC_UV(SCP)_MASK	1’b0: If dual OCP and UVP occur, ALT_P# does not assert 1’b1: No mask
9	CML_INVALID_CMD_ MASK	1’b0: If an invalid command in communication fault (see the STATUS_CML section on page 77) is triggered, ALT_P# does not assert 1’b1: No mask
8	CML_INVALID_DATA_ MASK	1’b0: If invalid data in a communication fault (see the STATUS_CML section on page 77) triggers, ALT_P# does not assert 1’b1: No mask
7	PEC_ERROR_MASK	1’b0: If a PEC error occurs, ALT_P# does not assert 1’b1: No mask
6	CRC_ERROR_MASK	1’b0: If a CRC error occurs, ALT_P# does not assert 1’b1: No mask

5	CMD_FLT_BLK_TRG_MASK	1’b0: If command fault block trig occurs, ALT_P# does not assert 1’b1: No mask
4	CML_OTHER_FAULT_MASK	1’b0: If an additional communication fault (see the STATUS_CML section on page 7) is triggered, ALT_P# does not assert 1’b1: No mask
3	EEPROM_FAULT_MASK	1’b0: If an EEPROM fault occurs, ALT_P# does not assert 1’b1: No mask
2	VIN_OVP_MASK	1’b0: If a V_{IN} over-voltage (OV) fault occurs, ALT_P# does not assert 1’b1: No mask
1	VIN_UV_WARN_MASK	1’b0: If a V_{IN} under-voltage (UV) warning occurs, ALT_P# does not assert 1’b1: No mask
0	VIN_UVP_MASK	1’b0: If a V_{IN} UV fault occurs, ALT_P# does not assert 1’b1: No mask

MFR_FS_DETECT_R3 (51h)

The MFR_FS_DETECT_R3 command on Page 2 sets some rail 3 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_FS_DETECT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X						RETURN_APS_DELAY						

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables the device to exit phase-shedding according to the PWM10 off time. The PWM minimum off time is excluded from PWM off time. 1’b0: Disabled 1’b1: Enabled
10	FS_EXIT_APS_EN_NP	Enables the device to exit phase-shedding according to the multi-phase PWM interval time between consecutive phases. The time threshold is set by register 4Bh. The PWM blanking time is excluded from the PWM interval time. 1’b0: Disabled 1’b1: Enabled
9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count for the PWM10 off-time condition to exit phase-shedding. Once the PWM off-time condition reaches the counting threshold, the controller exits APS immediately.
6:3	RETURN_APS_DELAY	Sets the minimum full-phase runtime after exiting APS due to an FS limit event. 20µs/LSB.
2:0	FS_EXIT_APS_CNT_NP	Sets the continuous count of the multi-phase PWMs interval time to exit phase-shedding. Once the PWMs interval condition reaches the counting threshold, the controller exits APS immediately.

MFR_APS_CTRL_R3 (52h)

The MFR_APS_CTRL_R3 command on Page 2 sets some rail 3 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									MFR_PS_ENTER_TIME_R3							

Bits	Bit Name	Description
15:12	MFR_ADP_OC_nPS_ EXIT_CNT_R3	Sets the period delay count from when OCP_PHASE is triggered to when the device exits automatic phase-shedding (APS). 100ns/LSB.
11	MFR_ADP_OC_nPS_ EXIT_EN_R3	Enables OCP_PHASE protection to make the device exit APS at any power state. 1'b0: Disabled 1'b1: Enabled
10	MFR_ADP_PFM_EXIT_ EN_R3	Enables the device to exit APS under a rail 3 increasing frequency condition. 1'b0: Disabled 1'b1: Enabled
9	MFR_ADP_OC_1PS_ EXIT_EN_R3	Enables OCP_PHASE protection to make the device exit APS during 1-phase DCM/CCM only. Then the device runs with full-phase operation. 1'b0: Disabled 1'b1: Enabled
8	MFR_ADP_UV_EXIT_EN_R3	Sets rail 3 to enter full-phase operation if V_{FB} < VID - 25mV. 1'b0: Disabled 1'b1: Enabled
7:2	MFR_PS_ENTER_TIME_R3	Sets the phase-shedding delay time. When the reported load current is consecutively below the APS threshold for a time calculated with APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE, the controller enters APS mode and automatically sheds phases according to the load current.
1	MFR_PHASHED_EXIT_MOD_R3	Set the phase dropping mode for phase-shedding. Phase-shedding may be due to APS. 1'b0: Drop to the target phase count immediately 1'b1: Shed phases one by one with a configured delay time. The delay time is set by DROP_PHASE_WAIT_TIME of this command
0	MFR_AUTO_PS_EN_R3	Enables rail 3 APS. 1'b0: Disabled 1'b1: Enabled

MFR_APS_CTRL2_R3 (53h)

The MFR_APS_CTRL2_R3 command on Page 2 sets some rail 3 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL2_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:9	APS_COMP_CNT	The MP2927 provides positive compensation on V_{REF} during phase-shedding to reduce undershoot. Phase-shedding may be due to APS. V_{REF} compensation is implemented by adding a PMBus-configurable positive voltage on COMP of the DC loop. After phase-shedding starts, the voltage returns 0V step by step with a set time interval. The time interval between each step is set by APS_COMP_CNT. 50ns/LSB.
8	DECAY_COMP_EN	Enables V_{REF} compensation while exiting decay. The compensation voltage level and slew rate are the same as during APS. 1'b0: Disabled 1'b1: Enabled
7:4	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce the undershoot. The compensation is added to V_{REF} when phase-shedding begins. 1.37mV/LSB.
3:0	MFR_APS_IHYS_R3	Sets the current hysteresis between phase-shedding and phase-adding. This prevents back-and-forth phase-shedding when APS is enabled. 1A/LSB.

MFR_APS_CTRL3_R3 (54h)

The MFR_APS_CTRL3_R3 command on Page 2 sets some rail 3 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL3_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	MFR_PS_INTERVAL_R3				MFR_PRD_EXIT_APS_TIME_R3						

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:7	MFR_PS_INTERVAL_R3	Sets the phase-by-phase dropping time intervals. It is only effective when register 52h, bit[1] is set to 1. 2.5µs/LSB.
6:0	MFR_PRD_EXIT_ APS_TIME_R3	Sets the period condition for the DC loop and current balance loop hold. If the absolute error between the set switching period and the real switching period ($\|t_S - t_{SET}\|$) is longer than MFR_PRD_EXIT_APS_TIME x 80ns, then the device holds the DC loop and current balancing time for a given time. 80ns/LSB.

MFR_NVM_CTRL (55h)

The MFR_NVM_CTRL command on Page 2 sets non-volatile memory (NVM) parameters.

Command	MFR_NVM_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			JOUT_ADC_TIME													

Bits	Bit Name	Description
15	PMBUS_TIMEOUT2_ MASK	1'b0: If a PMBUS timeout occurs, ALT_P# does not assert 1'b1: No mask
14	PROCHOT_MASK	1'b0: If a PROCHOT fault occurs, ALT_P# does not assert 1'b1: No mask

13:8	JOUT_ADC_TIME	Sets the J_{OUT} ADC time. 50ns/LSB.
7	TESTMODE_WRITE_EN	1'b0: Disabled. Cannot write to Page 3 1'b1: Enabled. Can write to Page 3
6	MEMORY_READ_EN	1'b0: Disabled. The read value is FFFF 1'b1: Enabled. The read value is the real value
5	MFR_BYTE_WORD	Enables NVM single-byte write or read via the PMBus. 1'b0: Disabled 1'b1: Enabled
4	OPERATION_ALL_CALL_EN	Enables command on/off control for all rails. 1'b0: Disabled 1'b1: Enabled
3	MFR_EEPROM_COPY_EN	This bit applies to the 16h and 18h registers. Set it to 0 in normal operation. 1'b0:Disabled 1'b1: Enabled
2	MFR_STORE_ALL_EN	This bit applies to the 15h register. 1'b0:Disabled 1'b1: Enabled
1	MFR_FAULT_SAVE_EN	Enables saving faults to the operating memory. 1'b0: Disabled 1'b1: Enabled
0	MFR_CRC_ERROR_EN	Enables CRC fault protection to shut down the device. 1'b0: Disabled 1'b1: Enabled

MFR_FSCB_LOOP_CTRL_R3 (56h)

The MFR_FSCB_LOOP_CTRL_R3 command on Page 2 sets the rail 3 f_{SW} and current balance loop.

Command	MFR_FSCB_LOOP_CTRL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function													CB_LOOP_HOLD_TIME			

Bits	Bit Name	Description
15	MFR_FS_LOOP_EN_R3	Enables the f_{SW} loop. The frequency loop keeps f_{SW} constant, and ensures it equals the set value, regardless of V_{IN} and the load current values. This bit active for all rails. 1'b0: Disabled 1'b1: Enabled
14	TRANS_HOLD_ FS_EN_R3	Enables the device to maintain frequency loop and CB loop regulation when a load transient event is detected (e.g. V_{FB} exceeds VFB+ window or VFB- window). 1'b0: Disabled 1'b1: Enabled
13	PS_HOLD_FS_EN_R3	Enables the device to hold frequency loop regulation when the phase count changes. 1'b0: Disabled 1'b1: Enabled

12	DVID_HOLD_FS_EN_R3	Enables the device to hold frequency loop regulation when DVID occurs. 1'b0: Disabled 1'b1: Enabled
11:8	MFR_FS_LOOP_CNT_R3	Sets the minimum hold time for the frequency loop when any load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set. 100μs/LSB.
7	MFR_CB_EN_R3	Enables the current balance loop. 1'b1: Enabled 1'b0: Disabled
6	PRD_HOLD_CB_EN_R3	Enables the device to hold the current balance loop when the PWM period meets the PWM switching period condition set via PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disabled 1'b1: Enabled
5	PS_HOLD_CB_EN_R3	Enables the device to hold the current balance loop when the phase number changes. 1'b0: Disabled 1'b1: Enabled
4	DVID_HOLD_CB_EN_R3	Enables the device to hold the current balance loop when DVID occurs. 1'b0: Disabled 1'b1: Enabled
3:0	CB_LOOP_HOLD_TIME	Sets the current balance loop hold time. When any load transient event, PWM switching period change event, phase count changing event, or DVID event is detected, and the corresponding enable bit is set, the current balance loop stops regulating for a time set via CB_LOOP_THOLD. 100μs/LSB.

MFR_VOUT_LOOP_CTRL_R3 (57h)

The MFR_VOUT_LOOP_CTRL_R3 command on Page 2 set the rail 3 V_{OUT} loop parameters.

Command	MFR_VOUT_LOOP_CTRL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	MFR_VDIFF_GAIN_SEL_R3	Selects the V_{DIFF} gain. When V_{OUT} exceeds 1.6V (the maximum sampling range of the internal ADC), select 1/2x gain so that V_{OUT} can be as high as 3.2V. 1'b0: 1x 1'b1: 1/2x
9	MFR_DC_REF_SEL_R3	Sets the V_{OUT} DC loop sensing point. 1'b0: V_{FB} 1'b1: V_{DIFF}
8	MFR_VCAL_PS2_EN_R3	Enables DC loop calibration in DCM. 1'b0: Disabled 1'b1: Enabled

7	MFR_VCAL_EN_R3	Enables DC loop calibration for DCM and CCM. 1'b0: Disabled 1'b1: Enabled
6	DC_LOOP_TSW_DIS_EN	Disables DC_LOOP when t_{SW} changes. 1'b0: Do not disable DC_LOOP 1'b1: Disable DC_LOOP
5	DC_LOOP_PH_DIS_EN	Disables DC_LOOP when a phase number changes. 1'b0: Do not disable DC_LOOP 1'b1: Disable DC_LOOP
4	DC_LOOP_TR_DIS_EN	Disables DC_LOOP when a load transient occurs. 1'b0: Do not disable DC_LOOP 1'b1: Disable DC_LOOP
3:0	MFR_DC_LOOP_CNT_R3	Sets the DC loop minimum hold time in direct format. 200μs/LSB with a +100μs offset.

JOUT_SHORT_PK_R3 (58h)

The JOUT_SHORT_PK_R3 command on Page 2 returns the rail 3 peak J_{OUT} value in every SHORT_TERM period.

Command	JOUT_SHORT_PK_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	JOUT_SHORT_PK_R3															

Bits	Bit Name	Description
15:0	JOUT_SHORT_PK_R3	Returns the peak value of J_{OUT} in every SHORT_TERM when J_{OUT} is enabled and GPIO_ACTIVE (68h), bit[13] is set to1. If J_{OUT} is disabled or GPIO_ACTIVE (68h), bit[13] is set to 0, this command returns the preset value.

JOUT_LONG_PK_R3 (59h)

The JOUT_LONG_PK_R3 command on Page 2 returns the rail 3 peak J_{OUT} value in every LONG_TERM period.

Command	JOUT_LONG_PK_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	JOUT_LONG_PK_R3															

Bits	Bit Name	Description
15:0	JOUT_LONG_PK_R3	Returns the peak value of J_{OUT} in every LONG_TERM when J_{OUT} is enabled and GPIO_ACTIVE (68h), bit[13] is set to 1. If J_{OUT} is disabled or GPIO_ACTIVE (68h), bit[13] is set to 0, this command returns the preset value.

MFR_SLOPE_CNT_1P_R3 (5Ah)

The MFR_SLOPE_CNT_1P_R3 command on Page 2 sets the rail 3 slope voltage clamp time in 1-phase operation.

Command	MFR_SLOPE_CNT_1P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_1P_R3									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	MFR_SLOPE_CNT_1P_R3	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_2P_R3 (5Bh)

The MFR_SLOPE_CNT_2P_R3 command on Page 2 is fixed to 0.

Command	MFR_SLOPE_CNT_2P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED								MFR_SLOPE_CNT_2P_R3							

Bits	Bit Name	Description
15:8	RESERVED	Fixed to 0.
7:0	MFR_SLOPE_CNT_2P_R3	Fixed to 0.

VDIFF2_SNAPSHOT (5Ch)

The VDIFF2_SNAPSHOT command on Page 2 returns the snapshot D4h value (on Page 1) when reading the D3h (on Page 1) value.

Command	VDIFF2_SNAPSHOT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	VDIFF2_SNAPSHOT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VDIFF2_SNAPSHOT	Returns the snapshot V_{OUT} ADC value while reading D3h (on Page 1). This value is updated from D4h (on Page 1) while reading D3h (on Page 1). 1.56mV/LSB when V_{DIFF} gain = 1 3.12mV/LSB when V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 1), bit[10].

VDIFF3_SNAPSHOT (5Dh)

The VDIFF3_SNAPSHOT command on Page 2 returns the snapshot D4h value (on Page 2) when reading the D3h (on Page 2) value.

Command	VDIFF3_SNAPSHOT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	VDIFF3_SNAPSHOT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VDIFF3_SNAPSHOT	Returns the snapshot V_{OUT} ADC value while reading D3h (on Page 2). This value is updated from D4h (on Page 2) while reading D3h (on Page 2). 1.56mV/LSB when V_{DIFF} gain = 1 3.12mV/LSB when V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 2), bit[10].

MFR_SLOPE_CNT_DCM_R3 (5Eh)

The MFR_SLOPE_CNT_DCM_R3 command on Page 2 sets the rail 3 slope voltage clamp time in DCM.

Command	MFR_SLOPE_CNT_DCM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_DCM_R3									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	MFR_SLOPE_CNT_ DCM_R3	Sets the slope voltage clamp time in DCM. 5ns/LSB.

MFR_PG_DELAY_R3 (5Fh)

The MFR_PG_DELAY_R3 command on Page 2 sets the rail 3 delay time for power good (PG) on and off.

Command	MFR_PG_DELAY_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PGOFF_DELAY_R3						MFR_PGON_DELAY_R3									

Bits	Bit Name	Description
15:10	MFR_PGOFF_DELAY_ R3	Sets the power good (PG) off delay time. 5µs/LSB.
9:0	MFR_PGON_DELAY_R3	Sets the PG on delay time. 5µs/LSB.

TON_DELAY_R3 (60h)

The TON_DELAY_R3 command on Page 2 sets the delay time from when system initialization ends to when the rail 3 V_{REF} starts to boot up.

Command	TON_DELAY_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TON_DELAY_R3															

Bits	Bit Name	Description
15:0	TON_DELAY_R3	Sets the delay time from when system initialization ends to when V_{REF} boots up. 100µs/LSB.

TON_RISE_R3 (61h)

The TON_RISE_R3 command on Page 2 sets the rail 3 V_{REF} boot-up slew rate.

Command	TON_RISE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	TON_RISE_R3												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TON_RISE_R3	Sets the rail 3 boot-up slew rate in PMBus mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h), bit[15].

MFR_PWM_MIN_TIME1_R3 (62h)

The MFR_PWM_MIN_TIME1_R3 command on Page 1 sets the minimum pulse width when PWM is high, low, or in tri-state. It is for rail 3 only.

Command	MFR_PWM_MIN_TIME1_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	MFR_MIN_LOW_TIME_R3									MFR_MIN_HIZ_TIME_R3					

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	MFR_MIN_LOW_TIME_R3	Sets the minimum PWM low time. 10ns/LSB with a -5ns offset. The minimum PWM low time can be calculated with the following equation: (PWM_MIN_LOW_TIME x 10) ns
8:6	MFR_MINON_TIME_R3	Sets the minimum PWM high time. 10ns/LSB with a -5ns offset. The minimum PWM high time can be calculated with the following equation: (PWM_MIN_HIGH_TIME x 10) ns
5:0	MFR_MIN_HIZ_ TIME_R3	Sets the minimum PWM tri-state time. 10ns/LSB with a -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: (PWM_MIN_TRI_TIME x 10) ns

MFR_PWM_MIN_TIME2_R3 (63h)

The MFR_PWM_MIN_TIME2_R3 command on Page 2 sets the PWM minimum off time and enables zero-current detection (ZCD). It is for rail 3 only.

Command	MFR_PWM_MIN_TIME2_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	TON_LIMIT_TO_VCAL				X	RESERVED				MFR_MINOFF_TIME_R3				

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	TON_LIMIT_TO_VCAL	On the MP2927, the DC loop can be held if the PWM period meets the condition set in MFR_FS (33h on Page 0). If the calculated PWM on time is shorter than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	MFR_ZCD_EN_R3	Enables rail 3 zero-current detection (ZCD). 1'b0: Disabled 1'b1: Enabled
8:5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4:0	MFR_MINOFF_TIME_R3	Sets the PWM minimum off time. 20ns/LSB with a 15ns offset. The PWM minimum off time can be calculated with the following equation: (PWM_MIN_OFF_TIME x 20 + 15) ns

TOFF_DELAY_R3 (64h)

The TOFF_DELAY_R3 command on Page 2 sets the rail 3 delay time from EN going low to V_{REF} starting the shutdown process on rail 3.

Command	TOFF_DELAY_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TOFF_DELAY_R3															

Bits	Bit Name	Description
15:0	TOFF_DELAY_R3	Sets the delay time from when EN goes low to V_{REF} shutdown. 100µs/LSB.

TOFF_FALL_R3 (65h)

The TOFF_FALL_R3 command on Page 2 sets the V_{REF} transition down slew rate after the device receives an OPERATION soft shutdown command for rail 3.

Command	TOFF_FALL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	TOFF_FALL_R3												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

[12:0]	TOFF_FALL_R3	Sets the rail 3 OPERATION command soft-shutdown slew rate in PMBus mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h), bit[15].

GPIO_SEL_GROUP5 (66h)

The GPIO_SEL_GROUP5 command on Page 2 sets GPIO parameters.

Command	GPIO_SEL_GROUP5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	RESERVED											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	RESERVED	Fixed to 0.

GPIO_SEL_GROUP6 (67h)

The GPIO_SEL_GROUP6 command on Page 2 sets GPIO parameters.

Command	GPIO_SEL_GROUP6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	RESERVED											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	RESERVED	Fixed to 0.

MFR_EN_SEL (68h)

The MFR_EN_SEL command on Page 2 sets the EN-related parameters.

Command	MFR_EN_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								MFR_EN3_SEL			MFR_EN2_SEL			MFR_EN1_SEL		

Bits	Bit Name	Description
15:14	MFR_PG2_EN_SEL_R3	Selects the internal power good (PG) combination for rail 3 internal enable (EN) signal (see bits[8:6] of this command). 2'b00: PGOOD_R1 2'b01: PGOOD_R2 2'b10: PGOOD_R1 and PGOOD_R2 2'b11: PGOOD_R1 and PGOOD_R2
13:12	MFR_PG2_EN_SEL_R2	Selects the internal PG combination for rail 2 internal EN signal (see bits[5:3] of this command). 2'b00: PGOOD_R1 2'b01: PGOOD_R3 2'b10: PGOOD_R1 and PGOOD_R3 2'b11: PGOOD_R1 and PGOOD_R3

11:10	MFR_PG2_EN_SEL_R1	Selects the internal PG combination for rail 1 internal EN signal (see bits[2:0] of this command). 2'b00: PGOOD_R2 2'b01: PGOOD_R3 2'b10: PGOOD_R2 and PGOOD_R3 2'b11: PGOOD_R2 and PGOOD_R3
9	EN_PIN_SEL	1'b0: All three rails share one EN signal from the EN pin 1'b1: All rails use different EN signals, determined by bits[8:0] of this command
8:6	MFR_EN3_SEL	Selects the internal ENABLE_R3. 3'b000: The EN pin 3'b001: The GPIO2 pin 3'b010: The GPIO3 pin 3'b011: The GPIO4 pin 3'b100: The PVID0 pin 3'b101: The PVID1 pin 3'b110: The PVID2 pin 3'b111: The internal PG combination (see bits[15:14] of this command)
5:3	MFR_EN2_SEL	Selects the internal ENABLE_R2. 3'b000: The EN pin 3'b001: The GPIO2 pin 3'b010: The GPIO3 pin 3'b011: The GPIO4 pin 3'b100: The PVID0 pin 3'b101: The PVID1 pin 3'b110: The PVID2 pin 3'b111: The internal PG combination (see bits[13:12] of this command)
2:0	MFR_EN1_SEL	Selects the internal ENABLE_R1. 3'b000: The EN pin 3'b001: The GPIO2 pin 3'b010: The GPIO3 pin 3'b011: The GPIO4 pin 3'b100: The PVID0 pin 3'b101: The PVID1 pin 3'b110: The PVID2 pin 3'b111: The internal PG combination (see bits[11:10] of this command)

MFR_VR_TEMP_CAL (69h)

Command	MFR_VR_TEMP_CAL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_TEMP_GAIN_R3								MFR_TEMP_OFFSET_R3							

Bits	**Bit Name**	**Description**
15:8	MFR_TEMP_GAIN_R3	Reserved.
7:0	MFR_TEMP_OFFSET_R3	Reserved.

MFR_VOUT_CALC_R3 (6Ah)

The MFR_VOUT_CALC_R3 command on Page 2 sets the rail 3 gain and offset for the V_{OUT} calculation.

Command	MFR_VOUT_CALC_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	MFR_VOUT_CALC_OFFSET_R3						MFR_VOUT_CALC_GAIN_R3							

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:8	MFR_VOUT_CALC_ OFFSET_R3	Adds an offset to V_{OUT} report in register READ_VOUT (8Bh). This bit is for the rail 3 V_{OUT} report only. This bit is in two's complement format. Bit[13] is the signed bit. VID_STEP/LSB. When the VID_STEP is 6.25mV, the voltage list below shows the direct values and real-world values. 6'b00 0000: 0mV 6'b00 0001: +6.25mV 6'b01 1111: +193.75mV 6'b10 0000: -200mV 6'b10 0001: -193.75mV 6'b11 1111: -6.25mV
7:0	MFR_VOUT_CALC_ GAIN_R3	Sets the gain from the ADC-sensed VOSEN - VORTN voltage to the PMBus V_{OUT} report in register READ_VOUT (8Bh). This bit is for the rail 3 V_{OUT} report only.

MFR_IOUT_CALC_AVS_R3 (6Bh)

The MFR_IOUT_CALC_AVS command on Page 2 sets the gain and offset for the rail 3 AVSBus I_{OUT} report.

Command	MFR_IOUT_CALC_AVS															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OUT_AVS_OS_R3					IOUT_AVS_GAIN_R3										

Bits	Bit Name	Description
15:11	OUT_AVS_OS_R3	Bit[15] is signed bit. 160mA/LSB.
10:0	IOUT_AVS_GAIN_R3	Sets the current-sense gain for the AVSBus report. The current-sense gain can be calculated with the following equation: $$GAIN = \frac{1.6 \times 32 \times 10^4}{1024 \times K_{CS} \times G_{IMON} \times R_{IMON}}$$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in µA/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the internal IMON resistor (in kΩ).

IOUT_CAL_GAIN_PMBUS_R3 (6Ch)

The IOUT_CAL_GAIN_PMBUS_R3 command on Page 2 sets the rail 3 gain for I_{OUT} reporting in PMBus mode. The MP2927 senses I_{OUT} by sensing the voltage of IMON. The reported I_{OUT} is returned with PMBus command READ_IOUT (8Ch on Page 2).

Command	IOUT_CAL_GAIN_PMBUS_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	GAIN_SEL		MFR_IOUT_CALC_GAIN_R3									

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:10	GAIN_SEL	Sets the exponent value for the IOUT_CAL_GAIN calculation equation in this command.
9:0	MFR_IOUT_CALC_GAIN_R3	Sets the current-sense gain for the PMBus report. The gain can be calculated with the following equation: $IOUT\_CAL\_GAIN=\frac{1023}{1.6}\times K_{CS}\times G_{IMON}\times R_{IMON}\times 2^{(6-GAIN\_SEL)}$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bits[11:10] of this command.

IOUT_CAL_OS_PMBUS_R3 (6Dh)

The IOUT_CAL_OS_PMBUS_R3 command on Page 2 sets the rail 3 offset for I_{OUT} reporting in PMBus mode. The MP2927 senses I_{OUT} by sensing the voltage of IMON. The reported I_{OUT} is returned with PMBus command READ_IOUT (8Ch on Page 0).

Command	IOUT_CAL_OS_PMBUS_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	IOUT_CAL_PH_OFS_R3							MFR_IOUT_CALC_OFFSET_R3					

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:6	IOUT_CAL_PH_OFS_R3	Adds an offset according the phase number, where a larger n corresponds with a larger offset. Bit[12] is the signed bit.
5:0	MFR_IOUT_CALC_OFFSET_R3	Adds a current report offset to READ_IOUT (8Ch).

MFR_IMON_SET_R3 (6Eh)

The MFR_IMON_SET_R3 command on Page 2 sets certain configurations for the internal IMON sense in PMBus mode. It is rail 3 only.

Command	MFR_IMON_SET_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						MFR_TRIM_IMON_DIGI_GAIN_R3										

Bits	Bit Name	Description
15:13	MFR_IMON_RES_SET_R3	Sets the rail 3 IMON resistor. 3'b000: 2.5kΩ 3'b001: 5kΩ 3'b010: 10kΩ 3'b011: 40kΩ 3'b1xx: No connection
12	MFR_IMON_GAIN_SET_R3	1'b0: The IMON3 current mirror gain is 1/8 1'b1: The IMON3 current mirror gain is 1/16
11	RESERVED	Fixed to 0.
10:0	MFR_TRIM_IMON_DIGI_GAIN_R3	Sets the digital calculation gain for I_{OUT} reporting. The gain is multiplied by the IMON ADC-sensed valued and forms the final IMON digital-sensed value. The IMON digital-sensed value is used for the PMBus I_{OUT} report. The final IMON-sensed value can be calculated with the following equation: $IOUT\_PMBUS\_REPORT=1024\times\frac{I_{OUT}\times K_{CS}\times G_{IMON}\times R_{IMON}}{1.6}\times\frac{TRIM\_DIGI\_GAIN}{1024}\times\frac{2^{(6\text{-}GAIN\_SEL)}}{GAIN}$ Where I_{OUT} is the output current (in A), K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and TRIM_DIGI_GAIN is a decimal value.

IOUT_MIN_ALERT_R3 (6Fh)

The IOUT_MIN_ALERT_R3 command on Page 2 returns the minimum I_{OUT} or its preset value. This function is determined by GPIO_ACTIVE (68h), bit[13]. It is for rail 3 only.

Command	IOUT_MIN_ALERT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	IOUT_MIN_ALERT_R3									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IOUT_MIN_ALERT_R3	If GPIO_ACTIVE (68h), bit[13] is set to 0, this command sets the DAC value for the I_{OUT} OC warn threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h), bit[13] is set to 1, this command returns the minimum I_{OUT}. In this mode, it also can be written with a higher value. If a higher I_{OUT} is detected, this register is overwritten. To start the new recording, write the value 0x03FF to reset this command. Convert the read value to the actual I_{OUT} (in A) with the following equation: $I_{OUT}(A)=\frac{6Fh,bits[9:0]}{6Ch,bits[9:0]\times 1024}\times 6Eh,bits[10:0]\times 2^{(6\text{-}GAIN\_SEL)}$ Where GAIN_SEL: 6Ch, bits[11:10].

MFR_PSI_SET (70h)

The MFR_PSI_SET command on Page 2 sets the phase configuration.

Command	MFR_PSI_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X									MFR_PSI_SET_R1			

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FORCE_PHASE_ NUM_EN_R3	Enables the device to force the power state following what is set by bits[10:9] of this command. 1'b0: Disable a forced power state 1'b1: Enable a forced power state. The system active phase number is determined by bits[10:9] of this command
10:9	MFR_PSI_SET_R3	Sets the forced phase number for rail 3. 2'b:00: DCM 2'b:01: 1-phase CCM 2'b:10: 2-phase CCM Others: Ineffective
8	FORCE_PHASE_ NUM_EN_R2	Enables the device to force the power state following what is set by bits[7:5] of this command. 1'b0: Disable a forced power state 1'b1: Enable a forced power state. The system active phase number is determined by bits[7:5] of this command
7:5	MFR_PSI_SET_R2	Set the forced phase number for rail 2. 3'b000: DCM 3'b001: 1-phase CCM 3'b010: 2-phase CCM Others: Ineffective
4	FORCE_PHASE_ NUM_EN_R1	Enables the device to force the power state following what is set by bits[3:0] of this command. 1'b0: Disable a forced power state 1'b1: Enable a forced power state. The system active phase number is determined by bits[3:0] of this command
3:0	MFR_PSI_SET_R1	Sets the forced phase number for rail 1. 4'b0000: DCM 4'b0001: 1-phase CCM 4'b0010: 2-phase CCM Others: Ineffective

MFR_PVID01_R3 (71h)

The MFR_PVID01_R2 command on Page 2 sets the rail 3 V_{BOOT}.

Command	MFR_PVID01_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID1_R3								MFR_PVID0_R3							

Bits	Bit Name	Description
15:8	MFR_PVID1_R3	Reserved.
7:0	MFR_PVID0_R3	Sets the rail 3 V_{BOOT}, when MFR_VR_CONFIG1 (C1h on Page 0), bit[13] is 1. It is in VID format. VID_STEP/LSB.

MFR_PVID23_R3 (72h)

The MFR_PVID23_R3 command on Page 2 is reserved.

Command	MFR_PVID23_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID3_R3								MFR_PVID2_R3							

Bits	Bit Name	Description
15:8	MFR_PVID3_R3	Reserved.
7:0	MFR_PVID2_R3	Reserved.

MFR_PVID45_R3 (72h)

The MFR_PVID45_R3 command on Page 2 is reserved.

Command	MFR_PVID45_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID5_R3								MFR_PVID4_R3							

Bits	Bit Name	Description
15:8	MFR_PVID5_R3	Reserved.
7:0	MFR_PVID4_R3	Reserved.

MFR_PVID67_R3 (72h)

The MFR_PVID67_R3 command on Page 2 is reserved.

Command	MFR_PVID67_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PVID7_R3								MFR_PVID6_R3							

Bits	Bit Name	Description
15:8	MFR_PVID7_R3	Reserved.
7:0	MFR_PVID6_R3	Reserved.

SAMPLE_INTERVAL_12PH_R3 (75h)

The SAMPLE_INTERVAL_12P_R3 command on Page 2 sets the rail 3 sample interval for 1-phase and 2-phase operation.

Command	SAMPLE_INTERVAL_12PH_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	SAMPLE_INTERVAL_2PH_R3								SAMPLE_INTERVAL_1PH_R3							

Bits	Bit Name	Description
15:8	SAMPLE_INTERVAL_2PH_R3	Sets the 2-phase sample interval. 50ns/LSB.
7:0	SAMPLE_INTERVAL_1PH_R3	Sets the 1-phase sample interval. 50ns/LSB.

CRC_USER_LAST (76h)

The CRC_USER_LAST command on Page 2 returns CRC result when the STORE_ALL or RESTORE_ALL command is received.

Command	CRC_USER_LAST															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CRC_USER_LAST															

Bits	Bit Name	Description
15:0	CRC_USER_LAST	The selection bit for the Mux is determined by MFR_VR_CONFIG1 (C1h on Page 0), bit[7]. If this bit is set to 0, option 1 is selected. In option 1, the CRC code is retrieved from the STORE_ALL process. The CRC is calculated based on the data flow from the register values to the MTP cell values. If this bit is set to 1, option 2 is selected. In option 2, the CRC code is retrieved from RESTORE_ALL (or the automatic restoration process after start-up). This value is calculated based on the data flow from the MTP cells to the registers. If the storing and restoring process are both successful, the results from both options will match the actual CRC code.

MFR_RESERVED (77h)

The MFR_RESERVED command on Page 2 is reserved.

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_RESERVED															

Bits	Bit Name	Description
15:0	RESERVED	RESERVED.

STATUS_BYTE (78h)

The STATUS_BYTE command on Page 2 returns 1 byte of information with a summary of the most critical statuses and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								X

Bits	Bit Name	Behavior	Description
7	NVM_BUSY	Live	Reports the live status of the NVM. 1'b0: The NVM is idle. NVM write and read with a PMBus command is available 1'b1: The NVM is busy. NVM write and read with a PMBus command is unavailable
6	OFF	Live	Indicates whether the rail 3 output is off. This bit is in live mode. It asserts if the rail 3 output is off. The output may turn off if there are protection, EN goes low, or VID = 0. 1'b0: VOUT3 is on 1'b1: VOUT3 is off
5	VOUT_OV_FAULT	Latch	Indicates whether a rail 3 V_{OUT} over-voltage (OV) fault has occurred. If rail 3 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. This is for VID_OVP and ABS_OVP. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	Indicates whether a rail 3 I_{OUT} over-current (OC) fault has occurred. If rail 3 OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. This is for OCP_TDC and OCP_SPIKE. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
3	VIN_UV_FAULT	Latch	Indicates whether a V_{IN} under-voltage UV fault has occurred. If a V_{IN} UV fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	TEMPERATURE	Latch	Indicates whether an over-temperature (OT) fault or warning has occurred. If a TSENSE-related OTP or OT warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Latch	Indicates whether a PMBus communication fault has occurred. If a PMBus communication related fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	PROCHOT_FAULT	Latch	Indicates whether a PROCHOT fault has occurred. If the PROCHOT voltage exceeds or falls below the level set by MFR_PROCHOT_SET (36h on Page 1), bits[13:8], then a PROCHOT fault occurs and this bit is set and latched. The PROCHOT fault direction is determined by MFR_PROCHOT_SET (36h on Page 1), bit[1]. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No PROCHOT fault has occurred 1'b1: A PROCHOT fault has occurred

STATUS_WORD (79h)

The STATUS_WORD (79h) command on Page 2 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher byte gives more detailed information of the fault conditions. The lower byte shares the information with register STATUS_BYTE (78h).

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function						X	X		STATUS_BYTE (78h)							

Bits	Bit Name	Behavior	Description
15	VOUT	Live	Indicates whether a rail 3 V_{OUT} over-voltage (OV) or under-voltage (UV) fault has occurred. If V_{OUT} OVP or UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} fault or warning has occurred 1'b1: A V_{OUT} fault or warning has occurred
14	IOUT	Live	Indicates whether a rail 3 I_{OUT} warning or fault has occurred. If a rail 3 I_{OUT} fault or warning or a P_{OUT} warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} fault or warning has occurred 1'b1: An I_{OUT} fault or warning has occurred
13	INPUT	Latch	Indicates whether a V_{IN} or I_{IN} fault or warning has occurred. If any V_{IN} or I_{IN} protection or warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} or I_{IN} fault or warning has occurred 1'b1: A V_{IN} or I_{IN} fault or warning has occurred
12	RESERVED	Latch	Reserved.
11	PG_NOT_ACTIVE	Live	1'b0: PG is active. 1'b1: PG is not active
10:9	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
8	WATCH_DOG_OVF	Latch	Indicates whether the watchdog monitor block timer has overflowed. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 2 returns 1 byte of information with the detailed V_{OUT} fault and warning statuses on rail 3.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X			X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Indicates whether a rail 3 V_{OUT} over-voltage (OV) fault has occurred. If rail 3 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
6	VOUT_OV_WARNING	Live	Indicates whether a rail 3 V_{OUT} OV warning has occurred. If rail 3 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} OV warning has occurred 1'b1: A V_{OUT} OV warning has occurred
5	VOUT_UV_WARNING	Live	Indicates whether a rail 3 V_{OUT} under-voltage (UV) warning has occurred. If rail 3 UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} UV warning has occurred 1'b1: A V_{OUT} UV warning has occurred
4	VOUT_UV_FAULT	Latch	Indicates whether a rail 3 V_{OUT} UV fault has occurred. If rail 3 UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN_ WARNING	Latch	Indicates whether rail 3 V_{OUT} has reached VOUT_MAX or VOUT_MIN. If the VID value exceeds the value set by VOUT_MAX (24h on Page 0) and VOUT_MIN (2Bh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID exceeds VOUT_MAX or is below VOUT_MIN
2	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.
1	LINE_FLOAT	Latch	Indicates whether rail 3 line-float protection has occurred. If a line-float fault is detected, the device shuts down the associated rails and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No line-float fault has occurred 1'b1: A line-float fault has occurred
0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 2 returns 1 byte of information with the detailed I_{OUT} fault and warning statuses on rail 3.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function				X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Indicates whether a rail 3 I_{OUT} over-current (OC) fault has occurred. If rail 3 OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. This is for OCP_TDC and OCP_SPIKE. 1'b0: No output OC fault 1'b1: An output OC fault has occurred
6	TDC_OCP_UV_FAULT	Latch	Indicates whether a rail 3 I_{OUT} dual OC and under-voltage (UV) fault has occurred. If rail 3 OCP occurs while the UV comparator is set, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No dual OC and UV fault has occurred 1'b1: A dual OC and UV fault has occurred
5:0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_INPUT (7Ch)

The STATUS_INPUT command on Page 2 returns 1 byte of information with detailed input fault and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	VIN_OVP	Latch	Indicates whether a V_{IN} over-voltage (OV) fault has occurred. If V_{IN} exceeds the VIN_OV limit, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6:0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command on Page 2 returns 1 byte of information with temperature-related fault and warning conditions.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		VRHOT	X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Indicates whether an over-temperature (OT) fault has occurred. If the temperature sensed via TSENSE exceeds the OT fault limit set by OT_FAULT_LIMIT (4Fh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred

6	VRHOT	Live	Indicates whether a VRHOT event has occurred. If the temperature sensed via TSENSE exceeds the OT warning limit set by MFR_VRHOT_SET (3Eh on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No VRHOT event has occurred 1'b1: A VRHOT event has occurred
5:0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_CML (7Eh)

The STATUS_CML command on Page 2 returns 1 byte of information with PMBus communication related faults.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function					X			

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	Indicates whether the device received an invalid PMBus command. If the MP2927 receives an unsupported command code, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	INVALID_DATA	Latch	Indicates whether invalid PMBus data has been received. If the MP2927 receives unsupported data, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received
5	PEC_ERROR	Latch	Indicates whether a PMBus packet error checking (PEC) fault has occurred. The PMBus interface supports the use of the PEC byte that is defined in the SMBus standard. The PEC byte is transmitted by the MP2927 during a read transaction or sent to the MP2927 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, then the command is not executed and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4	NVM_CRC_ERROR	Latch	Indicates whether a cyclic redundancy check (CR)C fault has occurred. While storing the operating memory data to the NVM, the MP2927 calculates a CRC code for each bit, and saves the final CRC code to the NVM. While restoring the NVM data to the operating memory, the MP2927 recalculates the CRC code and checks the CRC results when the restoration process is done. If the CRC result does not match what is stored, the VR shuts down and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
3	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

2	CML_FLT_TRG	Latch	If NVM operation is blocked while the controller records a fault to the NVM, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No NVM operation is blocked 1'b1: NVM operation has been blocked while the controller records a fault to the NVM
1	CML_OTHER_FAULTS	Latch	If any of the faults listed below occur during PMBus communication, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. • Sending too few bits • Reading too few bits • Host sends or reads too few bytes • Reading too many bytes
0	NVM_SIG_FAULTS	Latch	While restoring data from the NVM to the operating memory, the device checks the signature register in address 00h of the NVM first. If the signature register is 0x1234, the restoration process halts and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to clear this bit. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

READ_ADC_SUM (81h)

The READ_ADC_SUM command on Page 2 returns the sum of 16 consecutive ADC-sensed results.

Command	READ_ADC_SUM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X		ADC_SUM													

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	ADC_SUM_READY	Indicates whether the 16 consecutive ADC-sensed results are ready. 1'b0: Not ready 1'b1: Ready
13:0	ADC_SUM	Stores the sum of 16 consecutive ADC-sensed results. Send FBh (0 byte) to start the ADC summing action.

READ_VFB3_SENSE (82h)

The READ_VFB3_SENSE command on Page 0 returns the ADC-sensed VFB3 voltage.

Command	READ_VFB3_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_VFB3_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_VFB3_SENSE	Returns the ADC-sensed VFB3 voltage in direct format. 1.56mV/LSB.

READ_TSENSE_SENSE (83h)

The READ_TSENSE_SENSE on Page 2 reads the TSENSE pin voltage.

Command	READ_TSENSE_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_TSENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_TSENSE	Return the ADC-sensed voltage on TSENSE in direct format. 1.56mV/LSB.

READ_CS9 (85h)

The READ_CS9 command on Page 2 returns the ADC-sensed average voltage on rail 2's CS9 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS9															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	RESERVED						READ_CS9									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS9	Returns the ADC-sensed voltage on rail 2's CS9 in direct format. 3.125mV/LSB.

READ_CS10 (87h)

The READ_CS10 command on Page 2 returns the ADC-sensed average voltage on rail 3's CS10 in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS10															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	RESERVED						READ_CS10									

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS10	Returns the ADC-sensed voltage on rail 3's CS10 in direct format. 3.125mV/LSB.

READ_VIN (88h)

The READ_VIN command on Page 2 provides 2 bytes to return the sensed V_{IN} based on the VINSEN3 pin. In VID mode, the returned value must ignore the exponent value set by bits[15:11].

Command	READ_VIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP						READ_VIN									

Bits	Bit Name	Description
15:11	EXP	Unused. Fixed to 11011.
10	RESERVED	Fixed to 0.
9:0	READ_VIN	Returns the sensed V_{IN} in Linear11 format. 31.25mV/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 2 returns the sensed rail 3 VOSEN - VORTN voltage. Where K_R is the dividing ratio of the divider.

Command	READ_VOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	READ_VOUT											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT	Returns the V_{OUT} value. Linear mode: 2mV/LSB. V_{OUT} can be calculated with the following equation: V_{OUT} = READ_VOUT x 2 x K_R Where K_R is the dividing ratio of the divider. Direct mode: VID_STEP/LSB. V_{OUT} can be calculated with the following equation: V_{OUT} = READ_VOUT x VID_STEP x K_R. Where VID_STEP is determined by C1h, bits[15:14], and K_R is the dividing ratio of the divider.

READ_IOUT (8Ch)

The READ_IOUT command on Page 2 returns the sensed rail 3 I_{OUT} in direct format.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP					READ_IOUT										

Bits	Bit Name	Description
15:11	EXP	This value is determined by VR_CONFIG1 (C1h), bit[3]. 1: Select 5'b11110 0: Select 5'b11111
10:0	READ_IOUT	Returns the sensed I_{OUT}, which is determined by VR_CONFIG1 (C1h), bit[3]. 1: 0.25A/LSB 0: 0.5A/LSB

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 2 is reserved.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	X	X	X	READ_TEMP							

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_TEMP	Reserved.

READ_AD_RESULT (8Eh)

The READ_AD_RESULT command on Page 2 returns the ADC result.

Command	READ_AD_RESULT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_ADC									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_ADC	Returns the ADC value.

READ_VCOMP (8Fh)

The READ_VCOMP command on Page 2 returns the COMP value.

Command	READ_VCOMP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_VCOMP							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_VCOMP	Returns the COMP value.

READ_POUT (96h)

The READ_POUT command on Page 2 returns the rail 3 output power (P_{OUT}).

Command	READ_POUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_POUT															

Bits	Bit Name	Description
15:0	READ_POUT	Returns the rail 3 P_{OUT}. The ADC read value is the same as the value from D1h. Convert the read value to actual power (in W) with the following equation: $P_{OUT}(W) = \frac{\frac{READ\_POUT \times 8}{6Ch, bits[9:0] \times 1000} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}}{t_{SHORT\_TERM}}$ Where GAIN_SEL is 6Ch, bits[11:10], and: G_{VIDFF} is the VDIFF gain setting by 57h, bit[10]. 57h, bit[10] = 0: G_{VDIFF} = 1 57h, bit[10] = 1: G_{VDIFF} = 0.5 t_{SHORT_TERM} is the short term (in µs): 26h, bit[15] = 0: t_{SHORT_TERM} = 26h, bits[12:1] x 0.05µs 26h, bit[15] = 1: t_{SHORT_TERM} = (26h, bits[6:0] + 1) x 4Eh (on Page 1), bits[13:8] x 0.05µs

CAPABILITY (D0h)

The CAPABILITY command on Page 2 is read-only.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	CAPABILITY							

Bits	Bit Name	Description
7:0	CAPABILITY	Fixed to 0xC0.

JOUT3_SHORT_TERM (D1h)

The JOUT3_SHORT_TERM command on Page 2 returns the real-time rail 3 J_{OUT} in every short-term period.

Command	JOUT3_SHORT_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT3_SHORT_TERM															

Bits	Bit Name	Description
15:0	JOUT3_SHORT_TERM	Returns the real-time J_{OUT} value in every SHORT_TERM period. Convert the read value to actual output Joules (in µJ) with the following equation: $J_{OUT\_SHORT\_TERM}(\mu J) = \frac{D1h \times 8}{6Ch, bits[9:0] \times 1000} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch, bits[11:10], and: G_{VIDFF} is the VDIFF gain setting by 57h, bit[10]. 57h, bit[10] = 0: G_{VDIFF} = 1 57h, bit[10] = 1: G_{VDIFF} = 0.5

JOUT3_LONG_TERM (D2h)

The JOUT3_LONG_TERM command on Page 2 returns the real-time rail 3 J_{OUT} in every long-term period.

Command	JOUT3_LONG_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT3_LONG_TERM															

Bits	Bit Name	Description
15:0	JOUT3_LONG_TERM	Returns the real-time J_{OUT} value in every LONG_TERM period. Convert the read value to actual output Joules (in mJ) with the following equation: $J_{OUT\_LONG\_TERM}(mJ) = \frac{D2h \times 16.384}{6Ch, bits[9:0] \times 1000} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch, bits[11:10], and: G_{VIDFF} is the VDIFF gain setting by 57h, bit[10]. 57h, bit[10] = 0: G_{VDIFF} = 1 57h, bit[10] = 1: G_{VDIFF} = 0.5

IMON3_FAST_SENSE (D3h)

The IMON3_FAST_SENSE command on Page 2 returns one of the J_{OUT} ADC values.

Command	IMON3_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	IMON3_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IMON3_FAST_SENSE	Returns the I_{OUT} ADC value in the J_{OUT} calculation. Convert the read value to the actual I_{OUT} (in A) with the following equation: $I_{OUT}(A) = \frac{D3h, bits[9:0]}{6Ch, bits[9:0] \times 1024} \times 6Eh, bits[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$ Where GAIN_SEL is 6Ch, bits[11:10].

VDIFF3_FAST_SENSE (D4h)

The VDIFF3_FAST_SENSE command on Page 2 returns an additional J_{OUT} ADC value.

Command	VDIFF3_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	VDIFF3_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

9:0	VDIFF3_FAST_SENSE	Returns the V_{OUT} ADC value in the J_{OUT} calculation. 1.56mV/LSB when V_{DIFF} gain = 1 3.12mV/LSB when V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 57h (on Page 2), bit[10].

ADC_SUM_RESET (FBh)

The ADC_SUM_RESET command on Page 2 resets the ADC_SUM count.

This command is write-only. There is no data byte for this command.

CLEAR_CRC_FAULT (FCh)

The CLEAR_CRC_FAULT command on Page 2 clears the CRC fault information that is stored in NVM Page 28.

This command is write-only. There is no data byte for this command.

CLEAR_STORED_FAULTS (FEh)

The CLEAR_STORED_FAULTS command on Page 2 clears the last fault information that is stored in NVM Page 28.

This command is write-only. There is no data byte for this command.

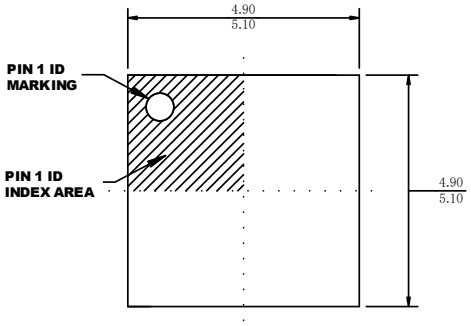
CLEAR_NVM_FAULTS (FFh)

The CLEAR_NVM_FAULTS command on Page 2 clears any NVM faults.

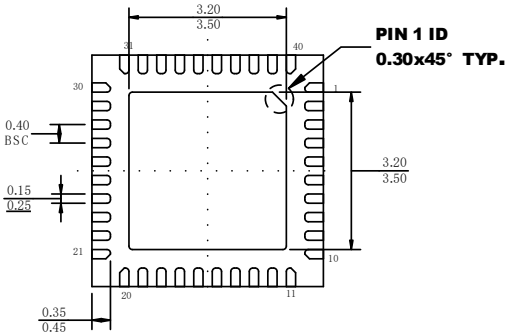
This command is write-only. There is no data byte for this command.

PACKAGE INFORMATION

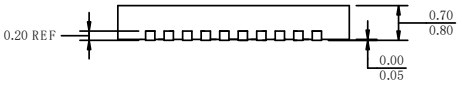
TQFN-40 (5mmx5mm)



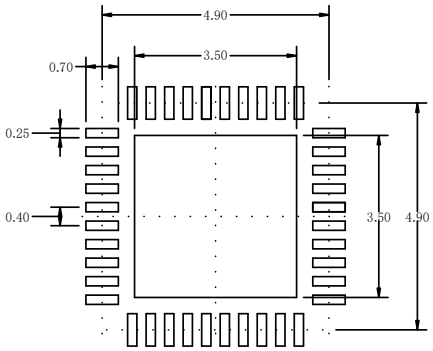
TOP VIEW



BOTTOM VIEW



SIDE VIEW

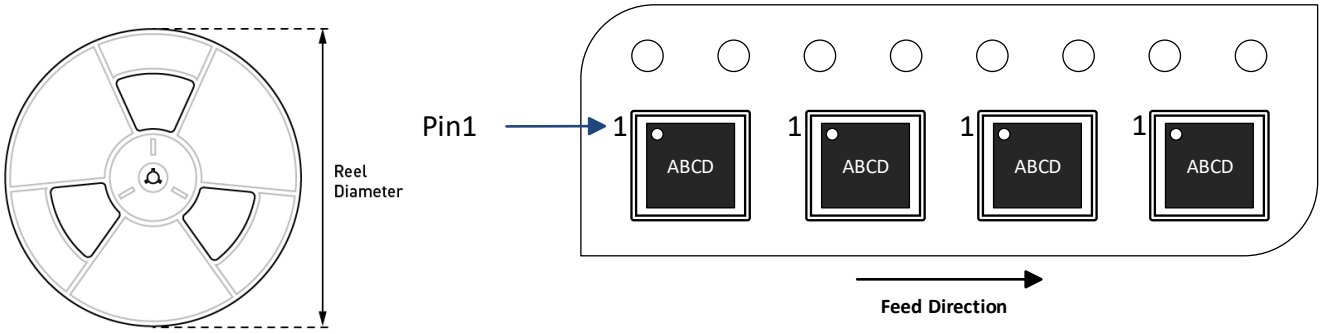


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION WHHE-1
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2927GUT	TQFN-40 (5mmx5mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/10/2022	Initial Release	-
1.1	4/24/2024	Updated all mentions of “MP2882” to “MP2927”	15, 17, 22, 24–27