MP2926

Triple-Loop, Digital, Multi-Phase Controller with PMBus Interface

DESCRIPTION

The MP2926 is a triple-loop, digital, multi-phase controller that provides power for the memory and SoC. The MP2926 can work with MPS's Intelli-Phase™ products to complete the multi-phase voltage regulator (VR) solution with minimal external components. The MP2926 can be configured with up to 2-phase operation for each rail.

The MP2926 provides an on-chip non-volatile memory (NVM) to store and restore device configurations. Device configurations and fault parameters can be easily programmed or monitored via the PMBus/I²C interface. The device can monitor and report output current through the current-sense (CS) output from Intelli-Phase™ devices.

The MP2926 is based on unique, digital, multi-phase, nonlinear control to provide a fast transient response to the load transient with minimal output capacitors. With only one power loop control method for both steady state and load transient, the power loop compensation is easy to configure.

The device is available in a QFN-40 (5mmx5mm) package.

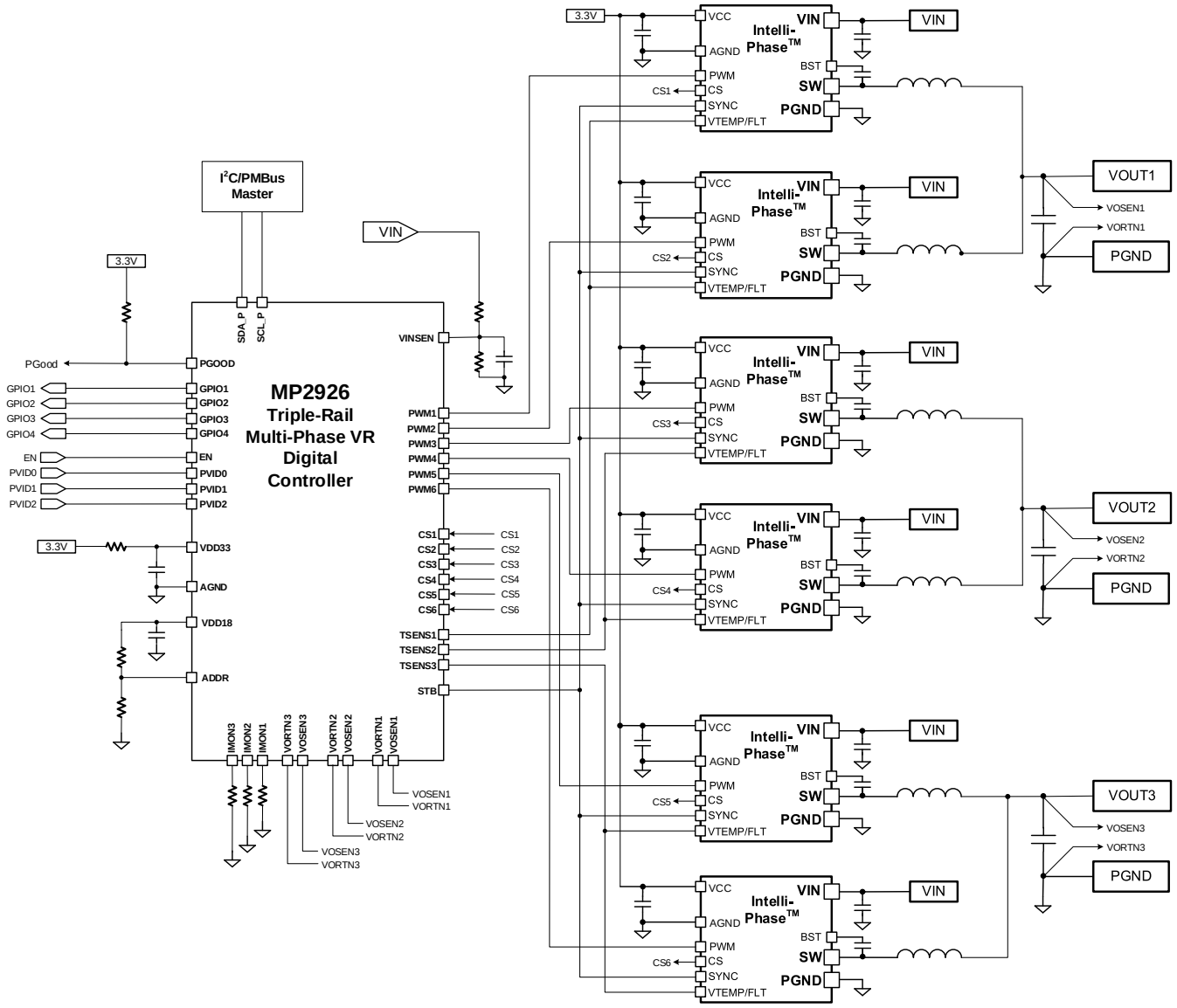
FEATURES

- Multi-Phase, Triple-Output, Digital Controller
- PMBus/I²C Compliant (1MHz Bus Speed)
- PVID Mode Available
- Pin Configurable for PMBus Address
- Built-In NVM to Store Custom Configurations
- Switching Frequency Range 200kHz to 3MHz
- Automatic Loop Compensation
- Fewer External Components than a Conventional Analog Controller
- Best Transient Performance with Nonlinear Digital Control
- Flexible Phase Assignment for Triple Rails
- Automatic Phase-Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing with Configurable Offsets for Thermal Balance
- Input and Output Voltage, Current, and Power Monitoring
- Regulator Temperature Monitoring
- V_{IN} UVLO, Output OVP/UVP, OCP, OTP with No Action, Latch, or Hiccup Mode
- Intelli-Phase™ Fault Diagnosis
- Auto-Records the VR Fault Type to the NVM
- Digital Load-Line Regulation
- Overclocking Mode by Adding Offset to Output Voltage
- RoHS-Compliant
- Available in a QFN-40 (5mmx5mm) Package

APPLICATIONS

- SoC Power
- DDR Memory Power
- Telecom and Networking Systems
- Base Stations

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2926GUT-xxxx**	TQFN-40 (5mmx5mm)	*See Below*	3

* For Tape & Reel, add suffix –Z (e.g. MP2926GUT-xxxx–Z).

** “xxxx” is the configuration code identifier for the register settings stored in NVM. Each “x” is a hexadecimal value between 0 & F. Work with the MPS FAE to create this unique number.

TOP MARKING

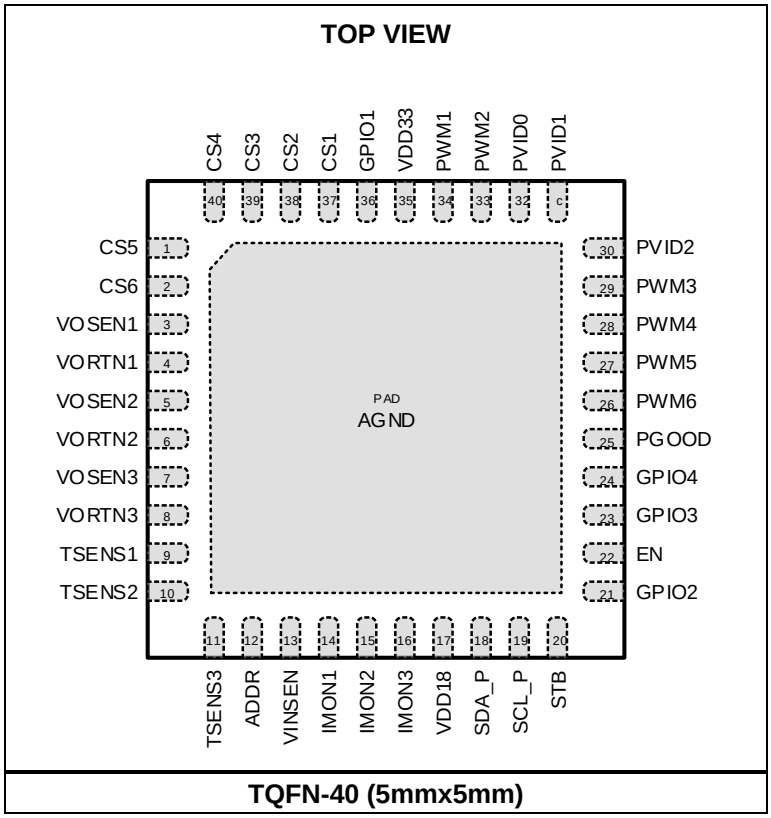
MPSYYWW

MP2926

LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2926: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE



TQFN-40 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Type	Description
1	CS5	A [I]	**Phase 5 current-sense input.**
2	CS6	A [I]	**Phase 6 current-sense input.**
3	VOSEN1	A [I]	**Positive remote voltage sense input.** VOSEN1 is connected to the VR output voltage directly at the load, and should be routed differentially with VORTN1.
4	VORTN1	A [I]	**Remote voltage sense return input.** VORTN1 is connected to ground directly at the load, and should be routed differentially with VOSEN1.
5	VOSEN2	A [I]	**Positive remote voltage sense input.** VOSEN2 is connected to the VR output voltage directly at the load, and should be routed differentially with VORTN2.
6	VORTN2	A [I]	**Remote voltage sense return input.** VORTN2 is connected to ground directly at the load, and should be routed differentially with VOSEN2.
7	VOSEN3	A [I]	**Positive remote voltage sense input.** VOSEN3 is connected to the VR output voltage directly at the load, and should be routed differentially with VORTN3.
8	VORTN3	A [I]	**Remote voltage sense return input.** VORTN3 is connected to ground directly at the load, and should be routed differentially with VOSEN3.
9	TSENS1	A [I]	**Temperature-sense input.** TSENS1 can be configured for either rail 1, rail 2, or rail 3 DrMOS V_{TEMP} sensing. It can also be used for general-purpose analog voltage sensing, or provide fault detection.
10	TSENS2	A [I]	**Temperature-sense input.** TSENS2 can be configured for either rail 1, rail 2, or rail 3 DrMOS V_{TEMP} sensing. It can also be used for general-purpose analog voltage sensing, or provide fault detection.
11	TSENS3	A [I]	**Temperature-sense input.** TSENS3 can be configured for either rail 1, rail 2, or rail 3 DrMOS V_{TEMP} sensing. It can be used for general-purpose analog voltage sensing, or be configured to protect rail 1, rail 2, or rail 3 with a configurable threshold.
12	ADDR	A [I]	**PMBus address setting.**
13	VINSEN	A [I]	**Input voltage sensing.** Connect VINSEN to a 1/16 divider from the input voltage.
14	IMON1	A[O]	**IMON1 current output.**
15	IMON2	A[O]	**IMON2 current output.**
16	IMON3	A[O]	**IMON3 current output.**
17	VDD18	Power	**1.8V LDO output.** VDD18 provides a power supply for the internal digital circuit. Connect a 1µF bypass capacitor to AGND.
18	SDA_P	D [I/O]	**PMBus/I²C data pin.**
19	SCL_P	D [I]	**PMBus/I²C clock pin.**
20	STB	D [O]	**Open-drain output to force the Intelli-Phase™ to enter standby mode**. Pull active high to enable the Intelli-Phase™. Connect it to the Intelli-Phase's™ SYNC pin.
21	GPIO2	D [I/O]	**General-purpose input/output.**
22	EN	D[I]	**Enable pin for the controller.**
23	GPIO3	D [I/O]	**General-purpose input/output.**
24	GPIO4	D [I/O]	**General-purpose input/output.**

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
25	PGOOD	D[I/O]	**Power good output.**
26	PWM6	D [O]	**Tri-state logic-level PWM outputs.** Each output is connected to the PWM input of the Intelli-Phase™. Phase 1 for rail 3.
27	PWM5	D [O]	**Tri-state logic-level PWM outputs.** Each output is connected to the PWM input of the Intelli-Phase™.
28	PWM4	D [O]	**Tri-state logic-level PWM outputs.** Each output is connected to the PWM input of the Intelli-Phase™. Phase 1 for rail 2.
29	PWM3	D [O]	**Tri-state logic-level PWM outputs**. Each output is connected to the PWM input of the Intelli-Phase™.
30	PVID2	A [I]	**PVID mode port 2.**
31	PVID1	A [I]	**PVID mode port 1.**
32	PVID0	A [I]	**PVID mode port 0.**
33	PWM2	D [O]	**Tri-state logic-level PWM outputs.** Each output is connected to the PWM input of the Intelli-Phase™.
34	PWM1	D [O]	**Tri-state logic-level PWM outputs.** Each output is connected to the PWM input of the Intelli-Phase™. Phase 1 for rail 1.
35	VDD33	Power	**3.3V power supply input.** Connect a 1µF bypass capacitor to AGND.
36	GPIO1	A [O]	**General-purpose output for analog signals.**
37	CS1	A [I]	**Phase 1 current-sense input.**
38	CS2	A [I]	**Phase 2 current-sense input.**
39	CS3	A [I]	**Phase 3 current-sense input.**
40	CS4	A [I]	**Phase 4 current-sense input.**
PAD	AGND	Power	**Analog ground.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD33 .....-0.3V to +4.0V
VDD18 .....-0.3V to +2.2V
VORTN1/2/3..... -0.3V to +0.3V
CS1/2/3/4/5/6, PWM1/2/3/4/5/6, VOSEN1/2/3, GPIO1/2/3/4, SCL_P, SDA_P, EN, PVID0, PVID1, PVID2, TSENS1/2/3, ADDR, STB, PGOOD .....-0.3V to +4.0V
VINSEN, IMON1/2/3 .....-0.3V to +2.2V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (2) 3.47W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (VDD33) .....3.15V to 3.45V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
TQFN-40 (5mmx5mm)	36	5 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 6-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Remote-Sense Amplifier (Rails 1/2/3)						
Bandwidth (5)	$GBW_{(RSA)}$			20		MHz
VORTN1/2/3 current	$I_{RTN1/2}$	EN = 3.3V, VOSEN1/2/3 = 3V, VORTN1,2,3 = 0V	-80	-40		µA
VOSEN1/2/3 current	$I_{VOSEN1/2}$	EN = 3.3V, VOSEN1/2/3 = 3V, VORTN1/2/3 = 0V		40	80	µA
System Interface Control Inputs						
EN						
Input low voltage	$VIL_{(EN)}$				0.8	V
Input high voltage	$VIH_{(EN)}$		2			V
Enable high leakage	$IIH_{(EN)}$	EN = 3.3V		3.3		µA
Enable delay (regular power mode) (5)		EN high to PWM switching ready		10		us
Enable delay (low-power mode) (5)		EN high to PWM switching ready		2		ms
PGOOD						
Output low voltage		Sink 4mA	0		0.2	V
Open-drain leakage current	I_{PGLKG}	V_{PGOOD} = 3.3V			3	µA
Over-Voltage (OV) and Under-Voltage (UV) Protection Comparator (Rail 1/2/3)						
Relative under-voltage threshold (V_{VID_UV})	Range	Relative to the DAC reference voltage	-425		-75	mV
	Resolution/LSB	3-bit DAC		50		mV
Relative over-voltage threshold (V_{VID_OV})	Range	Relative to the DAC reference voltage	200		450	mV
	Resolution/LSB	2-bit DAC		125		mV
CS Fault Comparator (Rail 1/2/3, CS# Protection)						
CS fault threshold	V_{CS_TH}			160		mV
TSENS1/2 Fault Comparator (Protection)						
TSENS1/2 fault threshold	V_{TH} ($V_{TEMP\ FLT}$)			2.2	2.4	V
TSENS3 Threshold DAC (5)						
Range			0.5		2.3	V
Resolution/LSB	Δ_{DAC_TSENS3}	6-bit DAC		40		mV

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM Outputs (PWM1/2/3/4/5/6)						
Output low voltage	$V_{OL\ (PWM)}$	$I_{PWM(SINK)}$ = 400µA		10	200	mV
Output high voltage	$V_{OH\ (PWM)}$	$I_{PWM(SOURCE)}$ = -400µA	3.0	VDD33 - 0.02		V
Rise and fall time (5)		C = 10pF		10		ns
PWM tri-state leakage		PWM = 1.5V, EN = 0V	-1		+1	µA
PWM middle state voltage				1.50		V
GPIO2/3/4						
Output low voltage	$V_{OL\ (GPIO2/3/4)}$	$I_{GPIO2/3/4(SINK)}$ = 400µA		10	200	mV
Output high voltage	$V_{OH\ (GPIO2/3/4)}$	$I_{GPIO2/3/4(SOURCE)}$ = -400µA	3.15	VDD33 - 0.02		V
Rise and fall time (5)		C = 10pF		10		ns
Open-drain output leakage		VGPIO2/3/4 = 3.3V	-1		+1	µA
STB						
Output low voltage	$V_{OL\ (STB)}$	$I_{STB(SINK)}$ = 4mA		90	300	mV
Output high voltage	$V_{OH\ (STB)}$	VDD33 = 3.3V, $I_{STB(SOURCE)}$ = -4mA	3	3.14		V
STB tri-state leakage		STB = 1.5V, EN = 0V	-1		+1	µA
VDD33 Supply						
Supply voltage range	VDD33		3.15	3.3	3.45	V
Supply current	I_{VDD33}	EN = 0 or 1, programmed as normal power mode		40	55	mA
		EN = 0, programmed as low-power mode		150		µA
UVLO threshold voltage		VDD33 is rising		2.85	2.99	V
UVLO threshold voltage		VDD33 is falling	2.6	2.75		V
UVLO hysteresis		VDD33 is falling		130		mV
1.8V Regulator						
1.8V regulator output voltage	VDD18	I_{VDD18} = 0mA, T_J = 25°C	1.782	1.8	1.818	V
1.8V load regulation		VDD18 source 30mA		VDD18 - 0.04		V
ADC (General, V_{IMON}, V_{DIFF} Dedicated, Rail 1/2/3)						
ADC reference voltage		T_J = 25°C	1.592	1.600	1.608	V
Resolution/LSB		10-bit ADC		1.5625		mV
DNL (5)		T_J = 25°C		1		LSB
Sample rate (5)				780		kHz

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VID DAC (Reference Voltage for Rail1/2/3)						
DAC reference voltage		T_J = 25°C	1.592	1.600	1.608	V
Maximum voltage (5)				1.55		V
Resolution/LSB	Δ_{DAC}	10-bit ADC		1.5625		mV
Maximum output voltage slew rate (5)				50		mV/µs
VOUT DC Loop DAC (VOUT Calibration for Rail1/2/3) (5)						
Range				240		mV
Resolution/LSB	Δ_{DAC}			0.9375		mV
OCP-SPIKE DAC (Rail1/2/3, OCP_SPIKE Protection)						
Range		Adjustable via the PMBus	0.3		1.5	V
Resolution/LSB (5)	Δ_{DAC_OC}	8-bit DAC		6.25		mV
OCP-Phase DAC (Rail1/2/3, OCP_PHASE Protection)						
Range		Adjustable via the PMBus	1.35		2.35	V
Resolution/LSB (5)		8-bit DAC		5		mV
OVP-ABS DAC (Rail1/2, Absolute OV Protection)						
Range	FS_{DAC_OVP}	Adjustable via the PMBus	0.5		2.3	V
Resolution/LSB (5)	Δ_{DAC_OVP}	8-bit DAC		10		mV
IMON1/2/3						
IMON gain accuracy		Gain = 1/16, T_J = 25°C	-1%		+1%	
IMON offset trim LSB		Gain = 1/16, I_{CS} = 0A		625		nA
VIMON1/2/3						
V_{IMON} gain		R_{IMON} = 40kΩ, T_J = 25°C IMON gain = 1/16, VIMON/IC	2475	2500	2525	Ω
V_{IMON} offset		R_{IMON} = 40kΩ, I_{CS} = 0A, IMON gain = 1/16		25		mV
PMBus DC Characteristics (SDA_P, SCL_P)						
Input high voltage	V_{IH}	SCL_P, SDA_P, Page 2, 2Dh = 0x0D53	2.2			V
Input low voltage	V_{IL}	SCL_P, SDA_P Page 2, 2Dh = 0x0D53			0.7	V
Input leakage current		SCL_P, SDA_P	-10		+10	µA
Output low voltage (5)	V_{OL}	SDA_P sinks 2mA			400	mV
Maximum voltage	V_{MAX}	Transient voltage including ringing	-0.3	3.3	+3.6	V
Pin capacitance	C_{PIN}				10	pF

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PMBus Timing Characteristics (1MHz) (5) (6)						
Operating frequency range			10		1000	kHz
Bus free time		Between stop and start condition	0.5			µs
Holding time			0.26			µs
Repeated start condition set-up time			0.26			µs
Stop condition set-up time			0.26			µs
Data hold time			0			ns
Data set-up time			50			ns
Clock low timeout			25		35	ms
Clock low period			0.5			µs
Clock high period			0.26		50	µs
Clock/data falling time					120	ns
Clock/data rising time					120	ns

Notes:

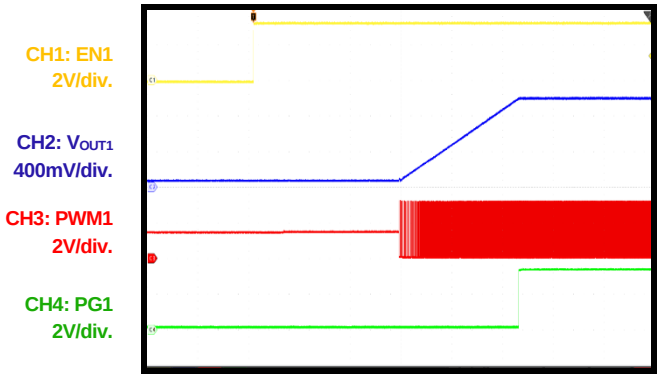
5) Guaranteed by design or characterization data. Not tested in production.
6) The device supports 100kHz, 400kHz, and 1MHz bus speeds. The PMBus timing parameters in this table are for operation at 1MHz. If the PMBus operating frequency is 100kHz or 400kHz, refer to the SMBus specifications for timing parameters.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = V_{OUT3} = 1V, f_{SW1} = f_{SW2} = f_{SW3} = 700kHz, VDD33 = 3.3V, 2 + 2 + 2 phase mode, T_A = 25°C, unless otherwise noted.

Rail 1 Enable On

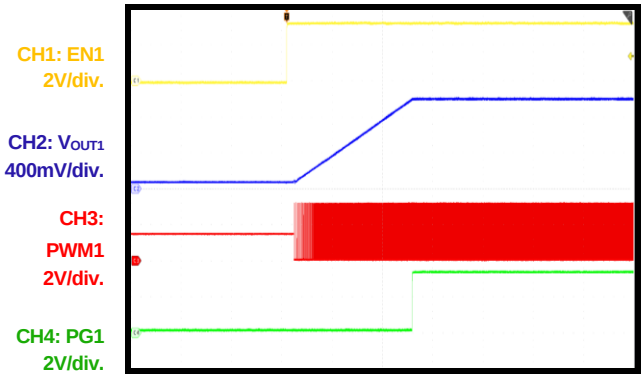
Low-power mode, t_{ON} delay = 0



400µs/div.

Rail 1 Enable On

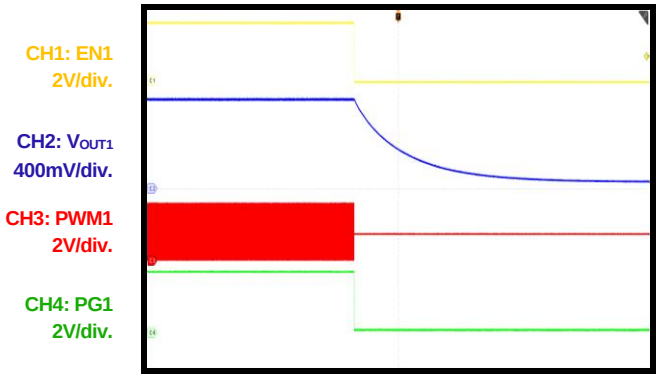
Regular power mode, t_{ON} delay = 0



400µs/div.

Rail 1 Enable Off

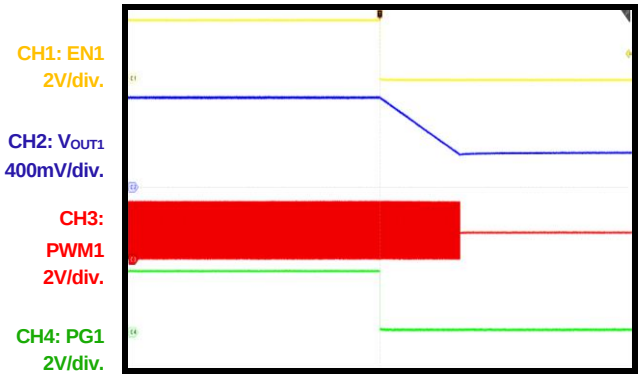
Hi-Z off



400ms/div.

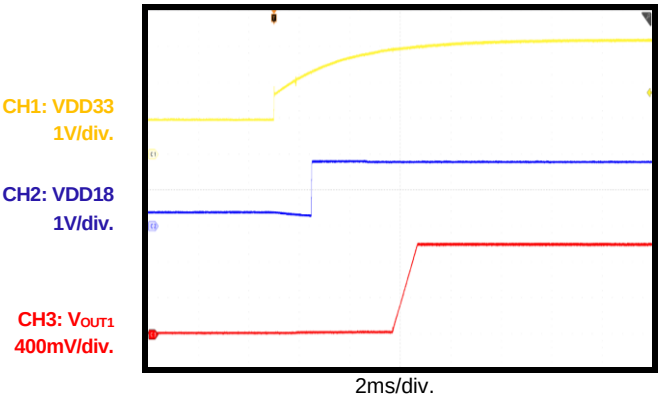
Rail 1 Enable Off

Soft-off with 1mV/µs



400µs/div.

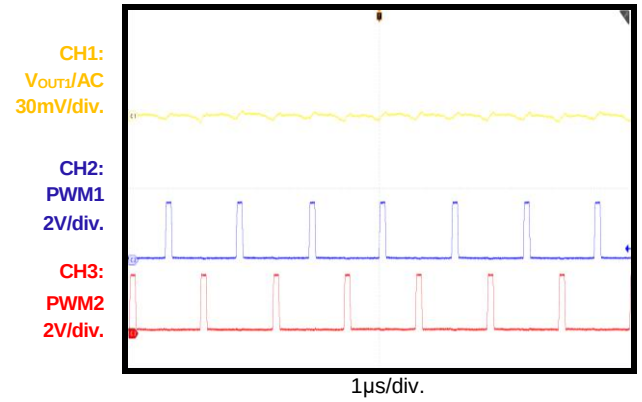
VDD33 On



2ms/div.

Steady State

2-phase CCM, I_{OUT1} = 0A



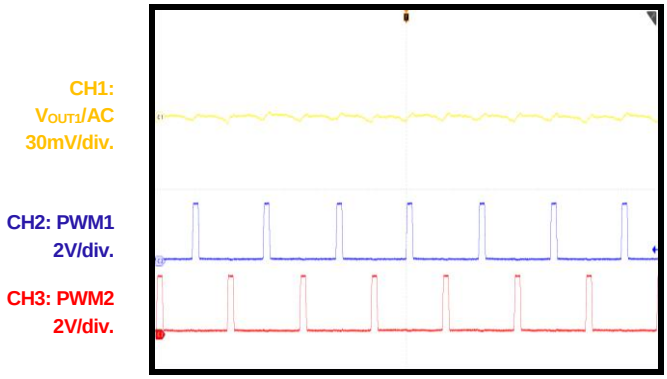
1µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = V_{OUT3} = 1V, f_{SW1} = f_{SW2} = f_{SW3} = 700kHz, VDD33 = 3.3V, 2 + 2 + 2 phase mode, T_A = 25°C, unless otherwise noted.

Steady State

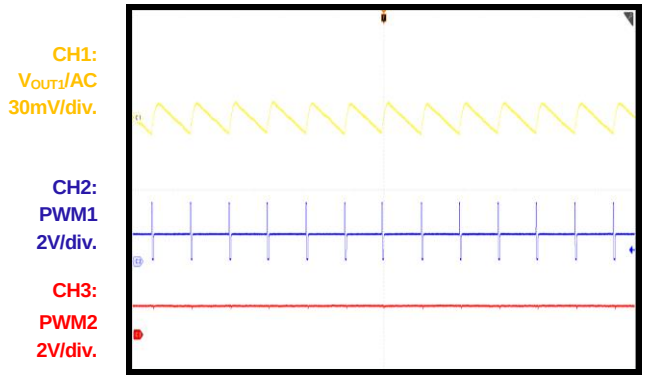
2-phase CCM, I_{OUT1} = 30A



1µs/div.

Steady State

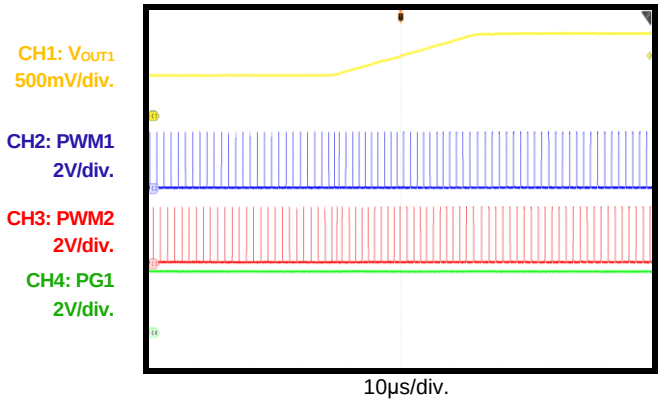
1-phase DCM, I_{OUT1} = 1A



10µs/div.

DVID Up

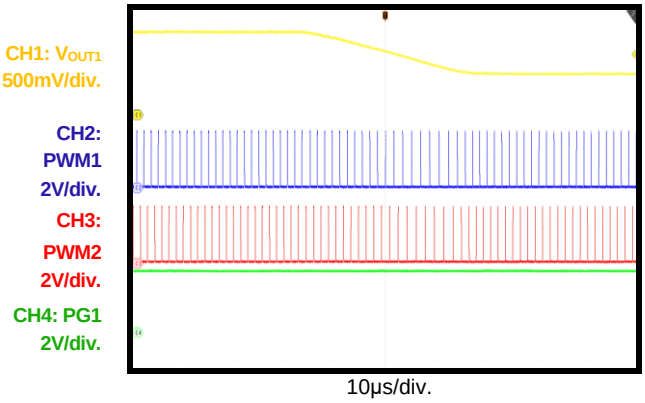
DVID from 0.6V to 1.2V, SR = 20mV/µs



10µs/div.

DVID Down

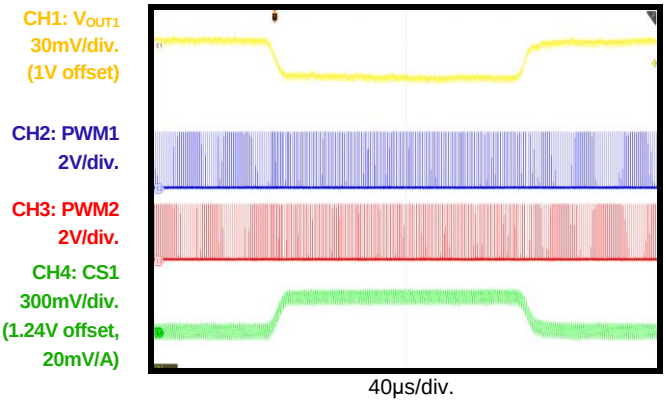
DVID from 1.2V to 0.6V, SR = 20mV/µs



10µs/div.

Load Transient with DC Load Line

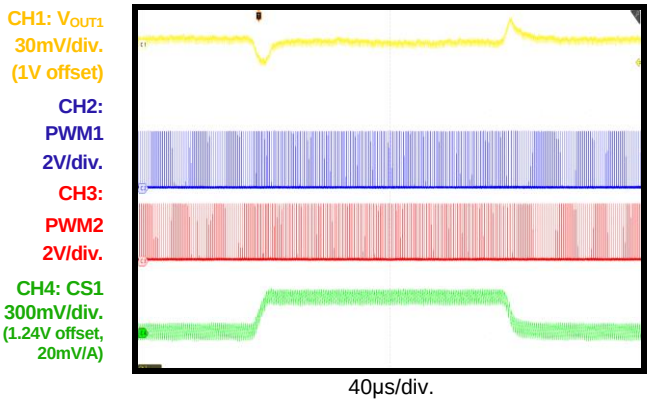
RLL = 1mΩ, 0A to 30A when 5A/µs



40µs/div.

Load Transient with AC Load Line

RLL = 0, 0A to 30A when 5A/µs



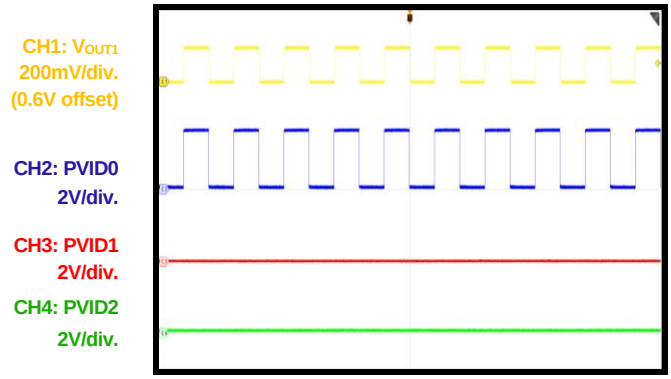
40µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = V_{OUT3} = 1V, f_{SW1} = f_{SW2} = f_{SW3} = 700kHz, VDD33 = 3.3V, 2 + 2 + 2 phase mode, T_A = 25°C, unless otherwise noted.

PVID Transient

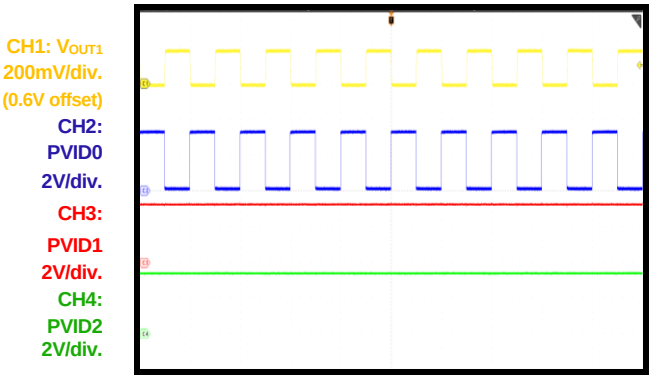
PVID_000 = 0.6V, PVID_001 = 0.8V



1ms/div.

PVID Transient

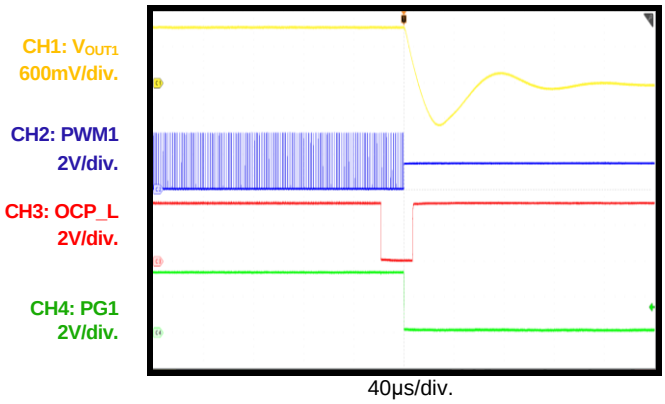
PVID_111 = 0.6V, PVID_110 = 0.8V



1ms/div.

OCP

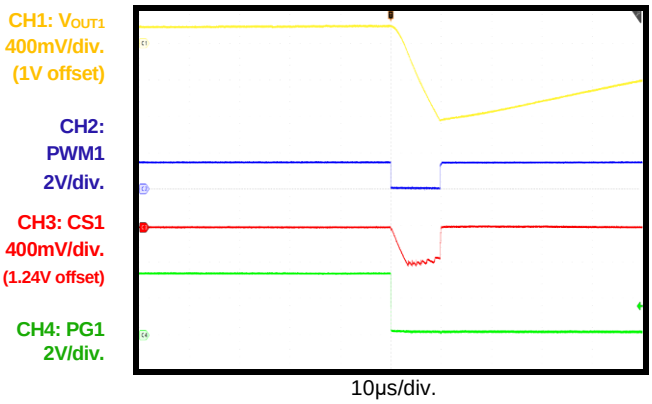
OCP_TDC = 30A,
OCP_TDC action delay = 18µs, latch-off mode



40µs/div.

OVP

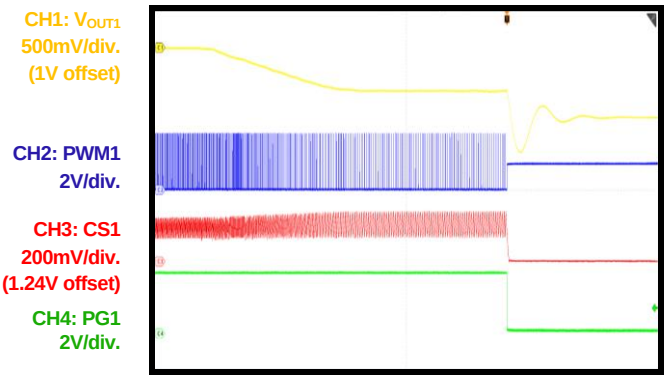
OVP VID delay = 0.5µs, latch-off mode



10µs/div.

UVP

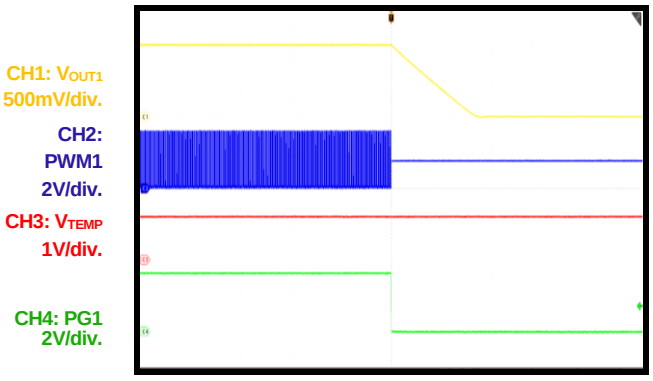
UVP delay = 500µs, latch-off mode



100µs/div.

OTP

T_J = 100°C x V_{TEMP} + 10°C, latch-off mode,
OTP threshold = 130°C



200µs/div.

FUNCTIONAL BLOCK DIAGRAM

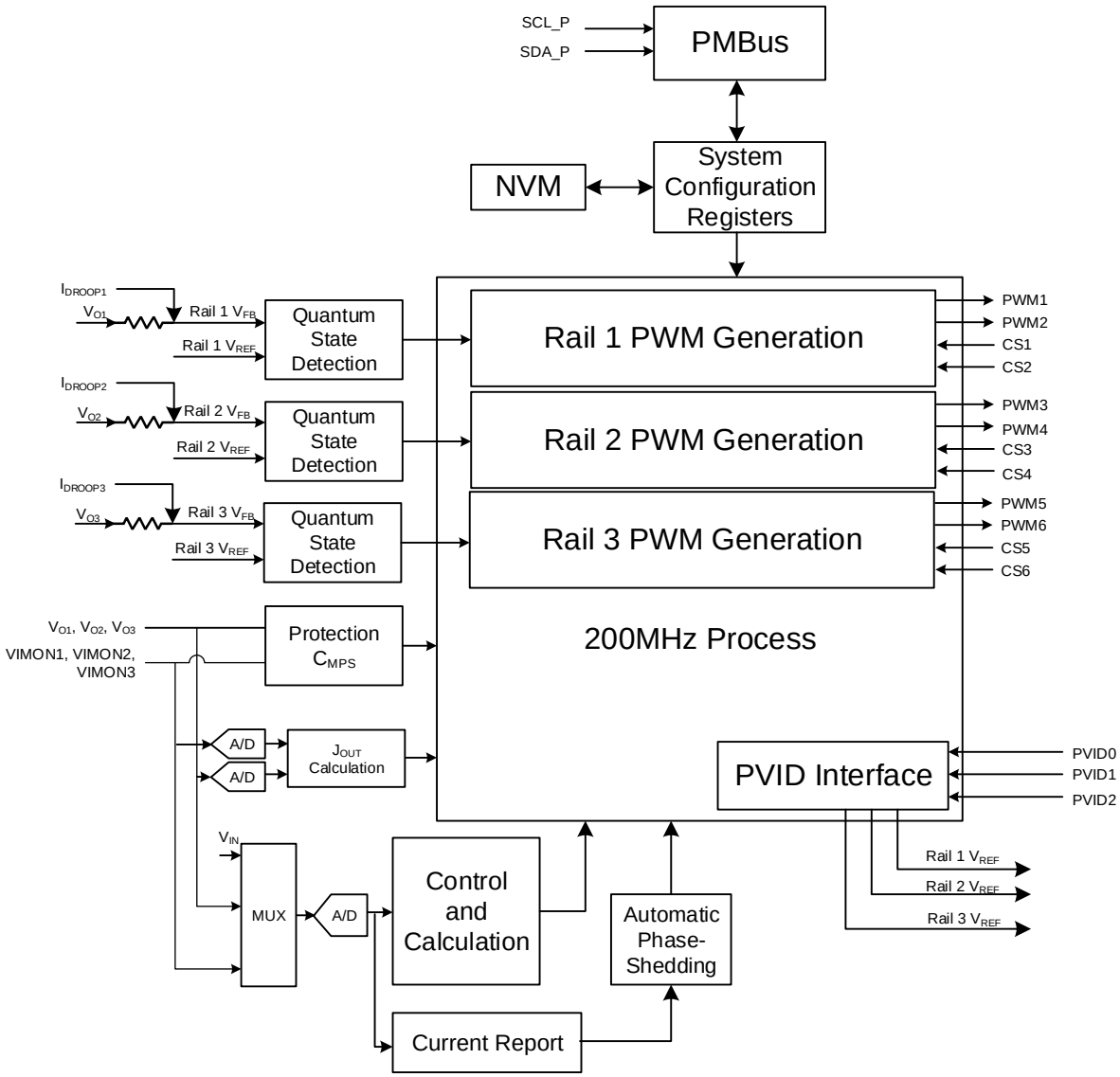


Figure 1: Functional Block Diagram

OPERATION

The MP2926 is a triple-output, digital, multi-phase VR controller for general-purpose multi-phase voltage regulators. The device can implement adaptive phase-shedding and phase-adding according to the load current to improve overall VR efficiency. The MP2926 contains a precision DAC and ADC, a differential remote voltage sense amplifier, fast comparators, current sense, internal slope compensation, digital load-line setting, PG and temperature monitoring, a PMBus/I²C and PVID interface, and a non-volatile memory (NVM) to store custom configurations.

Fault protection features include input under-voltage lockout (V_{IN} UVLO), over-current protection based on TDC (OCP_TDC), over-current protection based on $I_{CCSPIKE}$/EDC/I_{CCMAX} (OCP_SPIKE), cycle-by-cycle phase current limiting for over-current conditions (OCP_PHASE), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MP2926 can also detect the fault type of the Intelli-Phase™ if a protection occurs. The MP2926 can automatically record all the faults to the NVM in case the power supply shuts off while a fault occurs.

PWM Control and Switching Frequency

The MP2926 applies MPS's unique digital PWM control to provide fast load transient response and easy loop compensation. The switching frequency can be configured through the PMBus.

The PWM on time (t_{ON}) of each phase updates in real time according to the input voltage, output voltage, and adaptive phase switching frequency. t_{ON} can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

Where V_{OUT} is the real-time output voltage, V_{IN} is the input voltage, and f_{SW} is the switching frequency set by PMBus command FREQUENCY_SWITCH (33h).

System Configuration

The MP2926 provides input voltage sense and differential output voltage sense capabilities. The device can work with Intelli-Phase™ (MPS DrMOS) devices to sense the phase current, total load current, and the maximum temperature in the Intelli-Phase™ with a minimal number of external components. The PWM of the MP2926 outputs Hi-Z/middle state signals before outputting power to the load to achieve a pre-biased output condition before start-up.

The MP2926 can be configured up to 2-phase operation for each rail. It can be configured for different phase number applications via the PMBus. Table 1 shows phase setting examples. Applications include but are not limited to these examples.

Table 1: Phase Count Configuration and Active PWM Pins

MFR_PHASE_PSI_CFG (70h, Page 0)			Active PWM Pins		
Rail 1 70h bits[3:0]	Rail 2 70h bits[6:4]	Rail 3 70h bits[8:7]	Rail 1	Rail 2	Rail 3
4'b0010	3'b010	3'b010	1~2	4~3	6~5
4'b0001	3'b001	3'b001	1	4	6

Any unused PWM pin enters middle state, and the active phase interleaves automatically. Float the unused PWM and CS pins.

Non-Volatile Memory (NVM) Operation

The MP2926 uses an NVM to store the application configuration parameters. The default values are preconfigured at the factory. The data can be reconfigured using the STORE_USER_ALL command (15h) via the PMBus.

The configuration is restored from the NVM during the power-on sequence or by receiving the RESTORE_USER_ALL command (16h) from the PMBus. Figure 2 shows the MP2926's state machine.

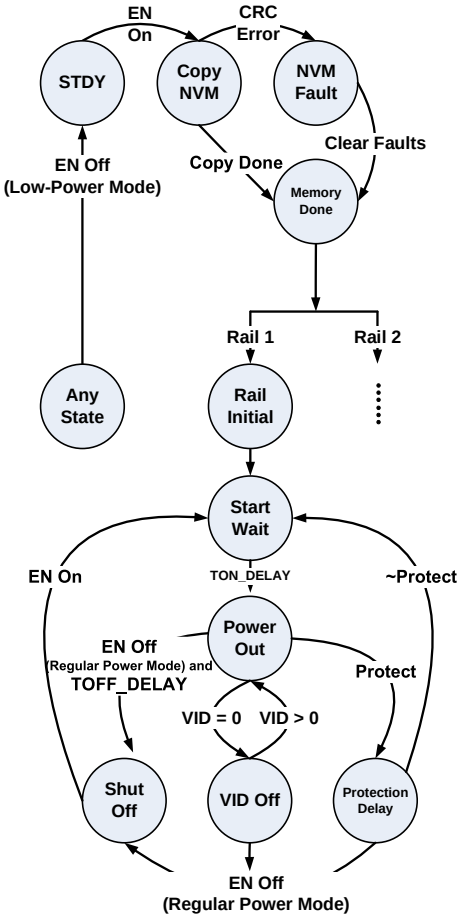


Figure 2: System State Machine

The PMBus STORE_USER_CODE (17h) command can reconfigure the data, except for the trim registers. It is recommended to use the STORE_USER_CODE (17h) command to save the current configuration to the NVM.

The RESTORE_USER_CODE (18h) command via the PMBus can load all the data from the NVM to the memory, except the trim registers.

NVM operation can be easily accomplished with MPS's GUI software. The NVM can be subject to more than 100,000 erase/write cycles.

NVM Fault

If the data from the NVM is determined to be invalid by the cyclic redundancy check (CRC) during the system initialization process, the system enters an NVM fault state without PWM switching. The system waits for the CLEAR_FAULTS command, and the NVM configuration is ignored.

There are two ways to clear the NVM fault and start up again with the default value in the register:

1. Clear the NVM fault via the PMBus.
2. Store the configuration to the NVM and restart the device.

Low-Power Mode

The MP2926 can be configured to low-power mode or regular power mode. If EN is low in low-power mode, PMBus communication is disabled and the I_Q is reduced to 150μA. In regular power mode, PMBus communication is available when EN is low.

Wait State

After system initialization, the MP2926 begins the t_{ON} delay period and the soft start process. The MP2926 enters the corresponding wait state if any of the following conditions occur:

1. A protection is triggered (e.g. the sensed input voltage drops below the under-voltage lockout threshold), or the sensed temperature exceeds the over-temperature protection (OTP) threshold. The MP2926 enters the protection state (hiccup or retry mode) until the fault clears. Then it enters the protection delay state (12.5ms) before the next restart cycle.
2. The device receives an off command via the PMBus. The MP2926 shuts off until it receives an on command from the PMBus master.
3. VID is commanded off. The MP2926 is in its VID off state, and there is no PWM output until the VID command exceeds the off level. The MP2926 immediately begins the soft start process after exiting the VID off state.
4. EN turns off and shuts down the MP2926.

Power-On Sequence

The MP2926 is supplied by a 3.3V voltage at VDD33. VDD33 provides the bias supply for the analog circuit and internal 1.8V LDO. The 1.8V LDO supplies the digital circuit. The system is reset by the internal power-on reset (POR) signal after the VDD33 supply is ready. After the system exits POR, the data in the NVM is loaded into the operating registers to configure the VR's operation.

Figure 3 shows the power-on sequence of the MP2926 in regular power mode. The steps are described in further detail below:

t0 to t1: At t0, VDD33 is supplied by a 3.3V voltage, and it reaches the VDD33 under-voltage lockout (UVLO) threshold at t1. VDD18 reaches 1.8V when the VDD33 pin is >1.8V.

t1 to t2: At t1, the data in the NVM starts loading into the operating registers. The entire NVM copying process typically takes about 2ms. If the user selects the voltage on the ADDR pin to set the PMBus address, the PMBus address is detected.

t2 to t3: After NVM copying is finished at t2, the MP2926 waits for the EN pin to pull high. The PMBus is available at this stage.

t3 to t4: If the PMBus OPERATION (01h, Page 0) command is preset to the off state after the EN pin pulls high, rail 1 halts at this stage, and waits for an OPERATION on command. If OPERATION (01h, Page 0) is preconfigured for the on state, the turn-on delay (t_{ON} delay) starts counting. The delay time is PMBus-configurable from 0ms to 6553.5ms via PMBus command TON_DELAY (60h, Page 0).

t4 to t5: When the t_{ON} delay expires, the rail VID DAC starts ramping up V_{REF} with the configured slew rate to the boot-up voltage. During soft start, OCP_TDC, OVP, and UVP are masked until V_{REF} reaches the target value. The rail's power-on sequence is complete at t5. When it is ready to output power, the power on-sequence of three rails is complete.

Figure 4 shows the MP2926's power-on sequence in low-power mode.

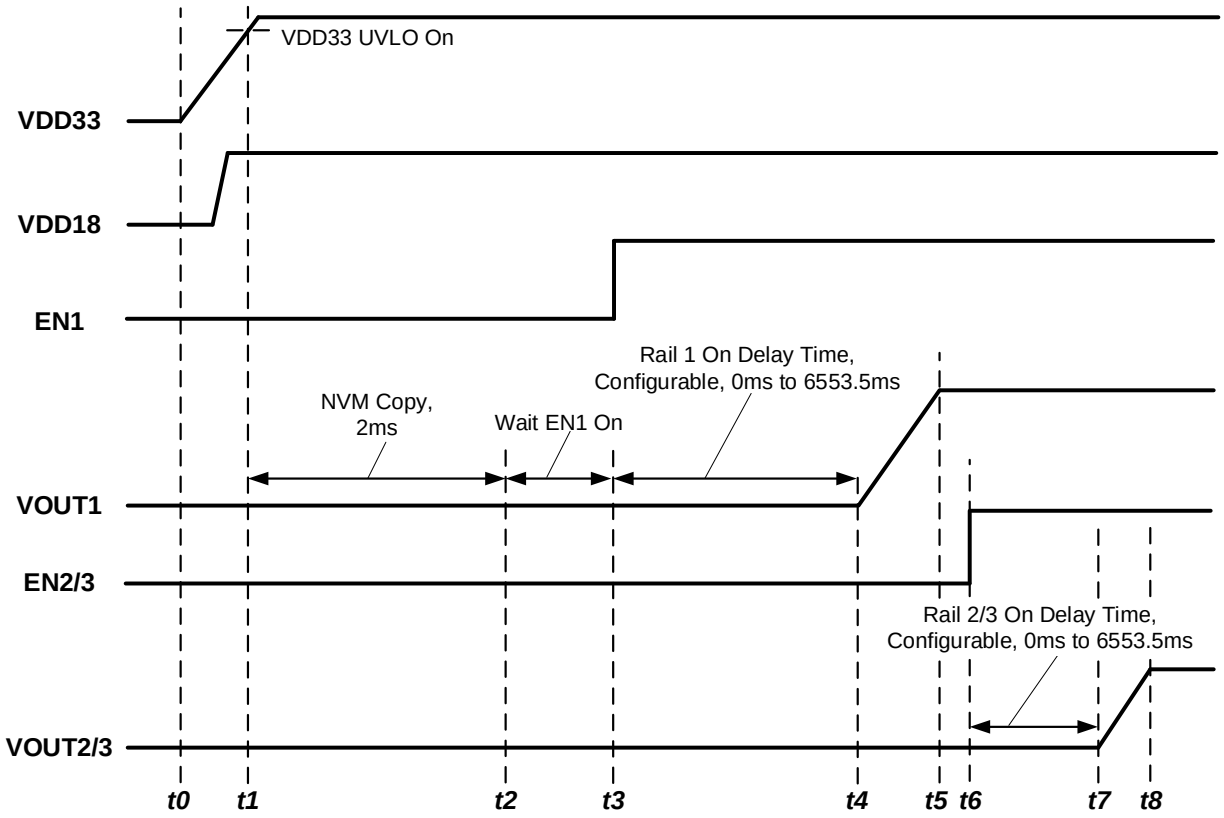


Figure 3: Power-On Sequence during Regular Power Mode

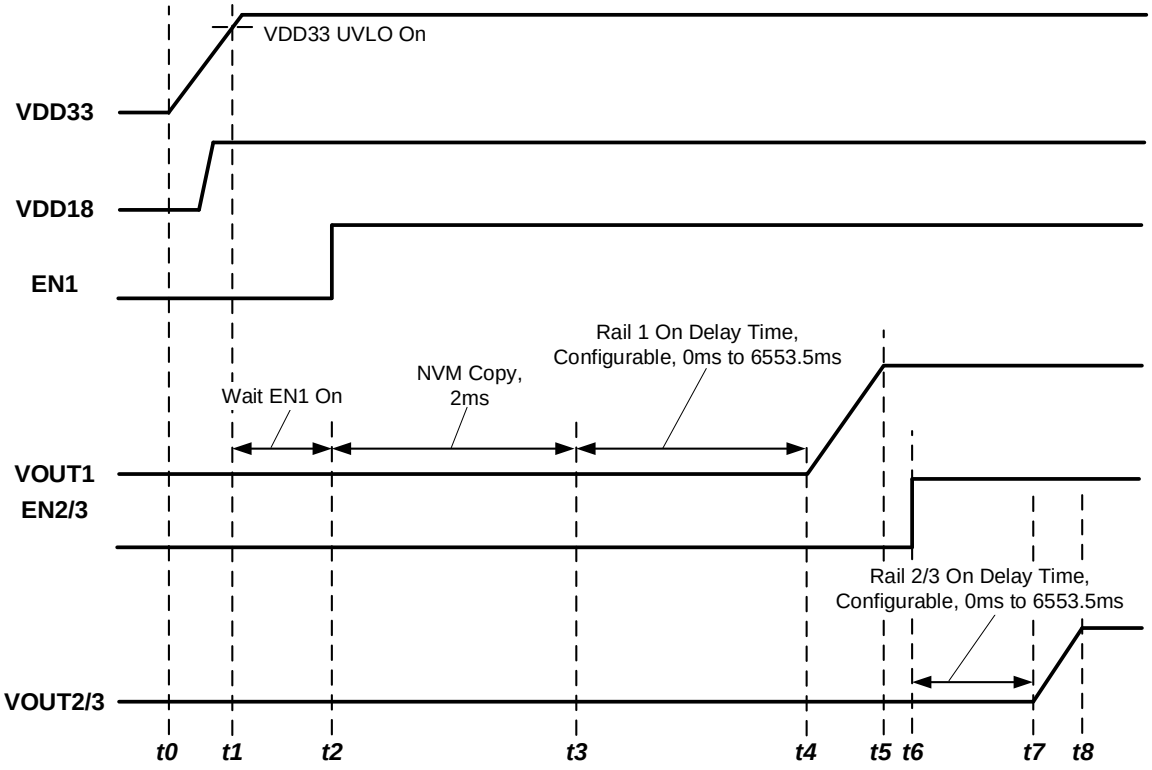


Figure 4: Power-On Sequence during Low-Power Mode

Power Off

The MP2926 can be powered off by the operation command, the EN pin turning off, VDD33 under-voltage lockout (UVLO), or a shutdown due to a protection. These conditions are described below:

1. VDD33 power-off: If the power supply on the VDD33 pin falls below the VDD33 under-voltage lockout (UVLO) falling threshold, the MP2926 powers off immediately.
2. EN pin off: The MP2926 provides Hi-Z and soft-off when the EN pin toggles low during regular power mode.

   During soft-off, V_{OUT} ramps down by the selected slew rate determined by register TON_RISE (61h) until V_{REF} reaches the VID shutdown level set by register MFR_SD_VID (23h), bits[7:0]. Then all PWMs enter tri-state. A turn-off delay time can be added via register TOFF_DELAY (64h).

   If both EN pins are off in low-power mode, the MP2926 initiates Hi-Z off immediately without a turn-off delay, and the device enters standby mode with low power consumption. The PMBus is unavailable until the EN pins are toggled high.
3. OPERATION command off: The MP2926 provides Hi-Z off and soft-off with the OPERATION command off. When the system receives a Hi-Z off command, all PWMs enter tri-state, and V_{OUT} is discharged by the load current.

   If the system receives a soft-off command, VOUT initiates a soft shutdown with the selected slew rate determined by TON_RISE (61h) until V_{REF} reaches the VID shutdown level. Then all PWMs enter tri-state. A turn-off delay time can be added to soft-off via TOFF_DELAY (64h).
4. Protection shutdown: If a V_{IN} over-voltage protection (OVP) or UVLO, V_{OUT} under-voltage protection (UVP), an over-current spike (OCP_SPIKE), an over-current condition on TDC (OCP_TDC), over-temperature protection (OTP), a CS fault, or a VTEMP fault from the Intelli-Phase™ are triggered, the VR initiates Hi-Z off immediately. If V_{OUT} OVP is triggered, the VR turns on all the active low-side MOSFETs (LS-FETs) to discharge C_{OUT}.

The device shuts down until V_{OUT} falls below the reverse-voltage protection (RVP) threshold (about 160mV).

Figure 5 shows the EN pin soft-off power sequence during regular power mode.

Figure 6 shows the EN pin Hi-Z off power sequence in low-power mode. When the EN pins are pulled low, the VR shuts down immediately without a t_{OFF} delay.

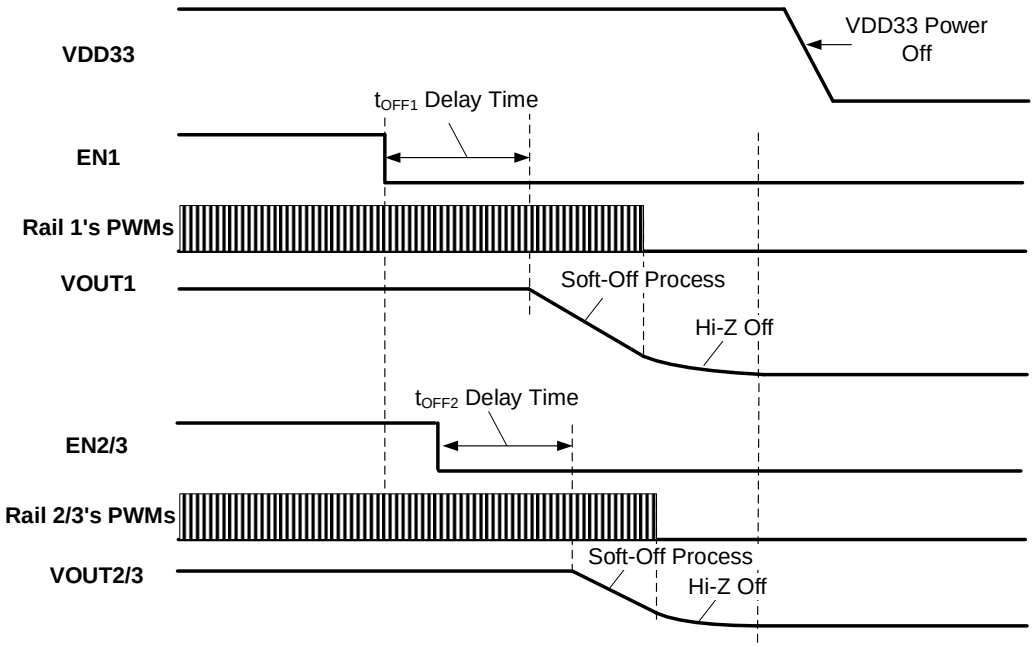


Figure 5: Power-Off Sequence During Regular Power Mode with Soft Off

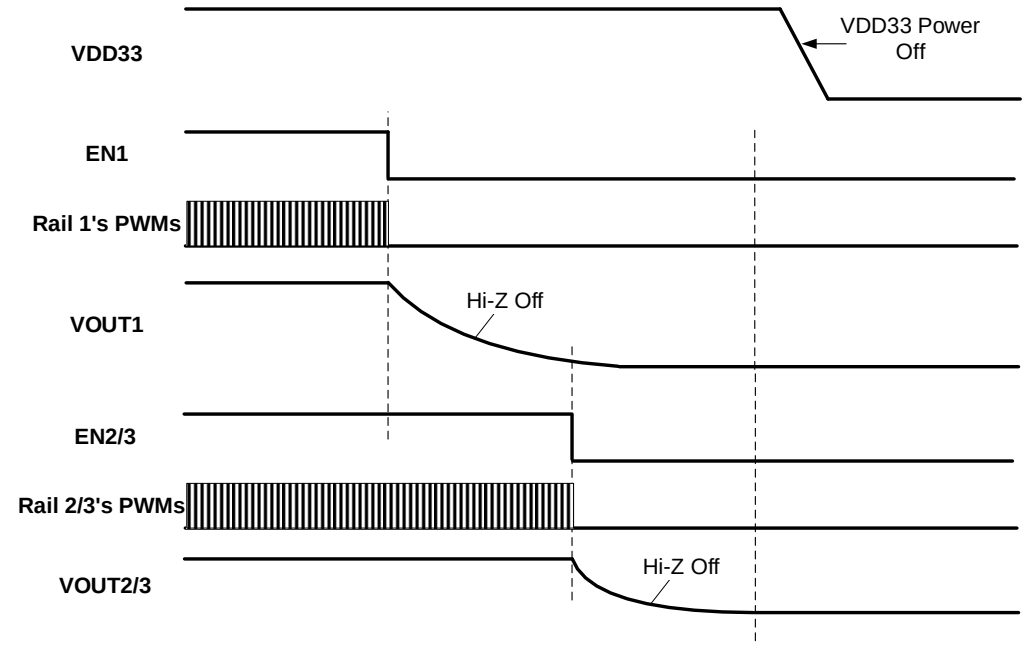


Figure 6: Power-Off Sequence During Low-Power Mode with Hi-Z Off

Voltage Reference

The MP2926 has two 10-bit VID DACs, which provide the reference voltage (V_{REF}) for the individual output. V_{REF} is in VID format with 6.25mV per step, and a 0V to 1.55V range.

The MP2926 provides two different VID control modes: PMBus VID mode and PVID mode.

Output Voltage Setting and Sensing

The voltage at the load is sensed with differential voltage sense amplifier for each rail. This type of sensing provides better load regulation. The sensed output voltages are used for loop compensation and output voltage monitoring via the PMBus. With unity gain, V_{REF} equals VID. The maximum VID voltage is limited to 1.55V, which is the maximum VID DAC output voltage.

With half gain, V_{REF} equals half of VID, and the maximum VID voltage is 3V. The half gain can be used to support overclocking applications and POL applications with a 1.55V to 3V output voltage.

When V_{OUT} ≤ 3V, connect the remote-sense amplifier input pins (VOSEN and VORTN) directly to the output at the load.

When V_{OUT} > 3V, the output voltage must be divided by the reference voltage within 1.55V. Figure 7 shows the typical connections for the remote sense when V_{OUT} exceeds 3V.

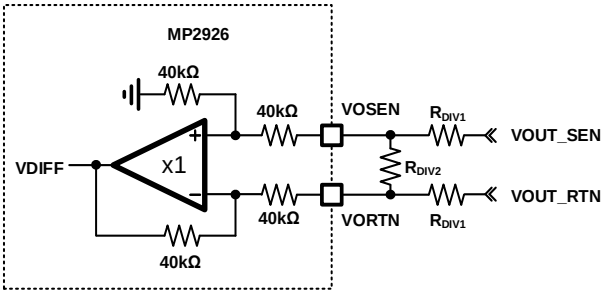


Figure 7: Output Divider Connections when Remote Sense Is Applied

VOUT_SENP and VOUT_SENN are from the load, and must be routed as a differential pair on quiet areas. Calculate the voltage divider ratio in Figure 7 with Equation (2):

$$K_R = \frac{V_{OUT}}{V_{DIFF}} = \left(\frac{1}{R_{DIV1}} + \frac{2}{R_{DIV2}} + \frac{1}{40k\Omega}\right) \times R_{DIV1} \quad (2)$$

K_R must be configured in the MP2926 by PMBus command VOUT_SCALE_LOOP (29h).

The controller uses this value to determine the reference voltage.

VOUT_SCALE_LOOP can be calculated with Equation (3):

$$VOUT\_SCALE\_LOOP = 2^5 \times K_R \quad (3)$$

Where VOUT_SCALE_LOOP is the configured value in register VOUT_SCALE_LOOP (29h).

The reference voltage can be calculated with Equation (4):

$$V_{REF} = \frac{2^5}{VOUT\_SCALE\_LOOP} \times V_{OUT} \quad (4)$$

The reference voltage is 6.25mV per step. Any other value is ignored. To minimize the output voltage DC setting error, match the real output divider ratio to R_{DIV1}, R_{DIV2}, and the PMBus set by the VOUT_SCALE_LOOP (29h) command. Design V_{REF} so that it is close to multiples of 6.25mV.

See the VOUT_SCALE_LOOP (29h) section on page 42 for more details.

To prevent the output voltage from going out of regulation, ensure the voltage on the VOSEN pin is below the maximum allowed sensing voltage (VDD33 - 0.3V) at all times.

For output voltage designs above the VOSEN pin specifications, connect the output divider carefully (see Figure 8). Connect VORTN directly to AGND to disable remote sensing.

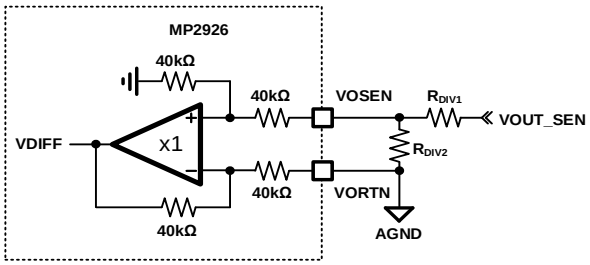


Figure 8: Output Divider Connections when Remote Sense Is Not Applied

Calculate the voltage divider ratio in Figure 8 with Equation (5):

$$K_R = \frac{V_{OUT}}{V_{DIFF}} = \left(\frac{1}{R_{DIV1}} + \frac{1}{R_{DIV2}} + \frac{1}{80k\Omega}\right) \times R_{DIV1} \quad (5)$$

VID Offset for Overclocking

The MP2926 supports adding an offset to the VID command. Set the offset with VOUT_TRIM (22h). The VID stop is decided by C1h (Page 0) bits[15:14], applied for PMBus or PVID mode. The target output voltage is the sum of the VID and the offset. The maximum output voltage is limited by the VOUT_MAX setting.

With a regular V_{DIFF} gain (1x, default value), the maximum output voltage is 1.55V. If the output voltage must exceed 1.55V, enable the 1/2x V_{DIFF} gain for a maximum of 3.0V.

Changing the offset value on the fly acts similarly to dynamic VID (DVID) operation, and the ramping up/down voltage slew rate is the same as the DVID voltage slew rate.

Input Voltage Sense

The input power supply voltage is sampled at VINSEN and used for output voltage regulation as the feed-forward control, V_{IN} under-voltage lockout (UVLO), V_{IN} over-voltage protection (OVP), and V_{IN} monitoring via the PMBus.

A resistor divider network outside the chip should be connected to VINSEN (see Figure 9). A 10nF or greater filtering capacitor is recommend at VINSEN.

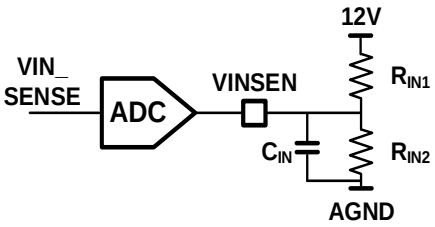


Figure 9: VIN Sense Network

There is a register in the NVM for setting up the divider ratio of the input voltage divider network. This can be used to calculate the input voltage for monitoring and protection.

Inductor Current Sense

The MP2926 works with MPS's Intelli-Phase™ to sense the phase inductor current and the total current. The cycle-by-cycle current information is used for phase-current balancing or thermal balancing, over-current protection, and adaptive voltage positioning (output voltage droop).

To achieve current sensing, connect the MP2926's CS pin directly to the Intelli-Phase™ CS pin. The MP2926's CS can take current or voltage information from the DrMOS CS to indicate the phase inductor current. If required, VCS_REF (1.24V) can be connected to the DrMOS as the CS reference voltage.

Total Current Sense

The total current is summed from each CS, and converted into an IMON voltage through internal resistors.

The IMON resistors of both rails are internal. The resistance and IMON current mirror gain are configurable (see Figure 10). These combinations cover the 36.5A to 1167A I_{BASE} range (assuming the current-sense gain = 8.5μA/A).

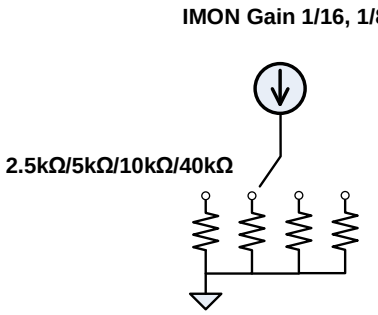


Figure 10: IMON Setting

If automatic phase-shedding is enabled via the PMBus, the total current report determines whether to enter or exit phase-shedding mode to flatten the overall efficiency across the operating current range.

Intelli-Phase™ Temperature Sense

The MP2926 measures the temperature of the power stage by connecting all Intelli-Phase™ VTEMP pins (see Figure 11). The voltage of the TSENS1 pin of the MP2926 indicates the highest junction temperature of all Intelli-Phase™ devices in the VR power system. The sensed temperature is used for over-temperature fault protection.

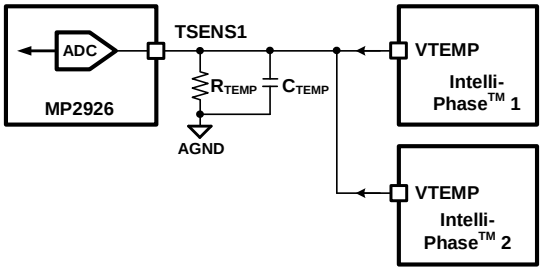


Figure 11: External Temperature Sense

The Intelli-Phase™ VTEMP pin has a voltage output proportional to the junction temperature. The junction temperature can be calculated with Equation (6):

$$T_J\ (°C) = a \times V_{TEMP} + b \quad (6)$$

Where V_{TEMP} is the VTEMP voltage, *a* is the analog temperature-sense gain, and *b* is the temperature-sense offset.

Refer to the Intelli-Phase™ datasheet for more information on the values of *a* and *b*.

Self-Temperature Sense

The MP2926 senses its temperature. A thermal sensor converts the die temperature to a voltage (see Figure 12). This voltage is saving into the register D5h (Page 1).

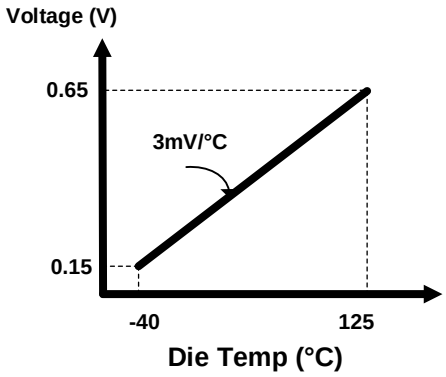


Figure 12: Die Temperature Sense

This register value can be read through the PMBus. The die temperature can be calculated with Equation (7):

$$T_{DIE\_TEMP}(°C) = \frac{DIE\_TEMP[9:0] \times 1.5625mV - 275mV}{3mV/°C} \quad (7)$$

Where DIE_TEMP is the read value from D5h (Page 1).

Dynamic Voltage Identification (DVID)

The MP2926 supports dynamic output voltage transition by changing the VID code with the PMBus interface and by toggling the PVID pins.

During PMBus override control mode and PVID control mode, the DVID slew rate is set by VOUT_TRANSITION_RATE (27h) with 0.1mV/μs/LSB or 0.01mV/μs/LS. That value is determined by MFR_VR_CONFIG3 (C3h) bit[15], and the maximum slew rate is 60mV/μs.

The MP2926 applies an advanced digital control method to improve output voltage performance while VID ramps up and down.

Ramping Up

When the output voltage ramps up, the inductor current rises to charge the output capacitors. This current introduces a large positive droop voltage, and lowers the output voltage.

When V_{REF} ramping ends, the output voltage may be below the minimum regulation tolerance budget (TOB).

The MP2926 automatically ramps up more VID steps than the target VID, and falls back to fasten the output voltage to rise to the regulation TOB.

Ramping Down

When the output voltage ramps down, the inductor current decreases to discharge the output capacitors. The output capacitors continue to discharge when ramping ends; this may lead to an output voltage undershoot.

The MP2926 applies a low-pass filter to the VID_DAC to smooth out the reference voltage when the output voltage is ramping down. Figure 13 shows the output voltage when VID ramps up after the previous VID finishes ramping down.

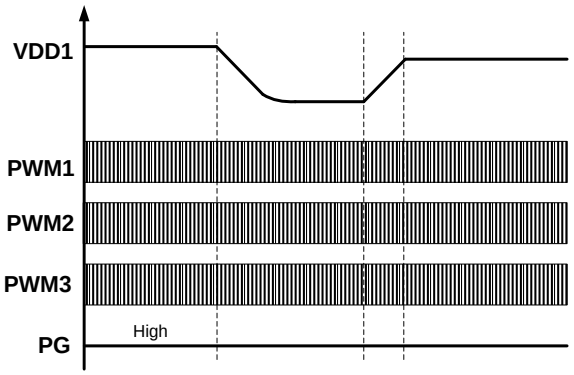


Figure 13: VID Ramping Down to VID Ramping Up

Automatic Phase-Shedding (APS)

The MP2926 provides an automatic phase-shedding (APS) function to improve the efficiency when there are no forced power state indicators. Figure 14 shows how the VR works in 2-phase CCM under heavy loads, and 1-phase DCM at extreme light loads to optimize efficiency. The VR enters 1-phase DCM under extremely light loads to further reduce the switching loss.

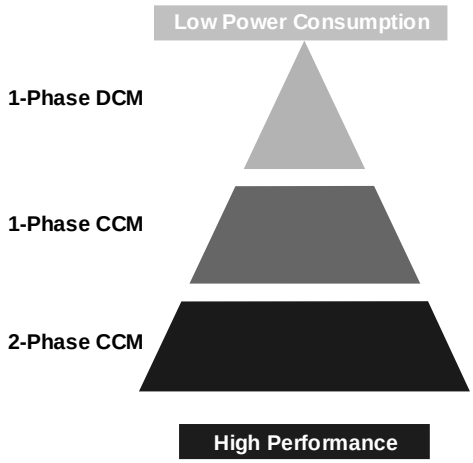


Figure 14: APS Function Diagram at 2-Phase Mode

The APS function is implemented by comparing the sensed load current with each power state current threshold. The MP2926 provides two types of registers to configure the APS function. All three rails have the MFR_APS_LEVEL_12P (4Dh) register to set the phase-shedding level, and 4 bits in register MFR_APS_CTRL2 (53h) to program the hysteresis value. This prevents the converter from changing the power state back and forth at a steady load current.

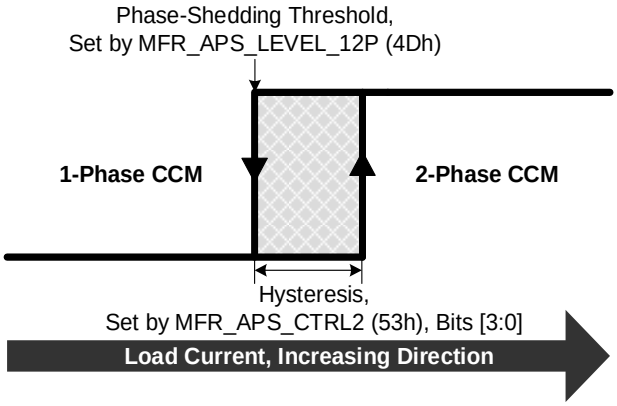


Figure 15: APS Threshold Setting

Figure 15 shows the APS current thresholds setting from 2-phase CCM to 1-phase CCM. See the MFR_APS_CTRL2 (53h) section on page 60, and the MFR_APS_LEVEL_12P (4Dh) section on page 57 for more information.

The MP2926 provides a sensed output current comparison as well as three conditions to immediately exit APS and run with full-phase CCM operation to accelerate the load transient response and reduce the output voltage undershoot. These conditions are described below:

1. The DVID process makes the controller run in full-phase CCM. After the output voltage is settled to the target value, the new power state is determined by the load current.
2. Load step-up causes VFB- window tripping, and triggers full-phase CCM to reduce output voltage undershoot.
3. Once the phase current exceeds the per-phase over-current limit, the MP2926 runs with a full phase number.

Phase Current Balancing/Thermal Balancing

The phase current is sensed and calculated with the current reference in the current loop. Each phase's PWM on time is adjusted individually to balance the currents accordingly.

The MP2926 applies sigma-delta (Σ-Δ) modulation and delay line loop (DLL) technology in the current balance modulation to increase the resolution of the current balance modulation and greatly reduce PWM jitter. The time resolution of the digital system is 5ns. By applying Σ-Δ modulation and DLL technology, the digital PWM resolution can be increased to 0.08ns.

Each current balance loop can also include the configurable phase current offset to achieve thermal balance among the phases. The phase with greater cooling capabilities due to better proximity to the airflow can take in more phase current. This can be accomplished by increasing the phase current reference with the offset to better balance the phase thermal. The current proportional integral (PI) loop bandwidth is lower than the output voltage feedback loop, so it does not significantly impact the output voltage.

Standby Mode for DrMOS

The STB signal can stand for the DrMOS. Once the part is in standby mode, the STB voltage can be configured to low, tri-state, or high for standby mode and for run mode.

Signal Mux

The multiplexor (mux) is flexible for debugging the versatile system.

If any of the following digital signals are pulled low, they remain low until POR or the PMBus commands a reset: OCP_SPIKE1, OCP_SPIKE2, OCP_SPIKE3, OCP_TDC1, OCP_TDC2, OCP_TDC3, and FAULT#.

VRHOT#1, VRHOT#2, VRHOT#3 is the Intelli-Phase™ over-temperature protection (OTP) warning signal.

PGOOD can be used for multiple configurations:

- PGOOD is configured to either PG1, PG2, or PG3
- PGOOD is configured for AND operation of PG1, PG2, and PG3
- PGOOD is configured for AND operation, and can operate any two of the three (e.g. PG1 and PG2, PG2 and PG3, or PG1 and PG3)

CSn means any signal among the CS1, CS2, CS3, CS4, CS5, and CS6 pins.

VCS_REF is the reference voltage for current sensing, such as CS_SUM for the MP2926. The resistor between CS_SUM and CSn is integrated into the MP2926. VCS_REF is for sensing purposes only.

By configuration, IOUT_ALT indicates any of the following signals:

- If rail 1's total current exceeds the threshold
- If rail 2's total current exceeds the threshold
- If rail 3's total current exceeds the threshold

VOUT_ALT indicates any of the following signals:

- If rail 1's voltage exceeds the threshold
- If rail 2's voltage exceeds the threshold
- If rail 3's voltage exceeds the threshold

The three rails can use one EN pin for control, or they can work with three enable signals:

- EN1 controls rail 1
- EN2 controls rail 2
- EN3 controls rail 3

When working independently, the EN pin should cooperate with GPIO2/3/4, PVID0/1/2, or the PG signal to select three enable signals. For example, if the EN pin is configured to EN1, then the PG1 pin is configured to EN2, and the PG2 pin is configured to EN3. Then after rail 1 works normally, rail 2 starts to work. After rail 2 works normally, rail 3 starts to work. This allows the power sequence to be controlled.

POUT_ALT is a signal that indicates any updates on the JOUT registers:

- JOUT_SHORT_TERM_PEAK_R1
- JOUT_LONG_TERM_PEAK_R1
- JOUT_SHORT_TERM_PEAK_R2
- JOUT_LONG_TERM_PEAK_R2
- JOUT_SHORT_TERM_PEAK_R3
- JOUT_LONG_TERM_PEAK_R3

Once the register updates, POUT_ALT pulls low for 1µs, then back to high level.

By configuration, POUT_ALT can indicate if JOUT exceeds a threshold.

Table 2 shows how the mux is distributed for each GPIO pin (see the GPIO register (66h, 67h, and 68h on page 69, page 123, and page 180 for more details).

Table 2: Mux Signals

MP2926 Pin Name	STB	ADDR	Input with Programmable Threshold	VCS_REF	CSn	TSENS1	TSENS2	TSENS3	VIMON1	VIMON2	VIMON3	EN = All EN	EN1	EN2	EN3	PG = All PGood	PG1	PG2	PG3	ALT_P# (OD/Low)	FAULT	OCP_L	OCP_SPIKE	OCP_TDC	VRHOT# (OD/Low)	obs_A (default:JOUT_short term)	obs_B (default:JOUT_Long term)	obs_C (default:Iout_max)	obs_D (default:Iout_min)	obs_E (default:Vout_max)	obs_F (default:Vout_min)
GPIO1				O					O	O	O																				
ADDR		D			O				O	O	O																				
STB	D																														
EN												D	O	O	O																
PGOOD																D	O	O	O												
TSENS1						D																									
TSENS2					O		D		O	O	O																				
TSENS3			D		O			D																							
GPIO2													O	O	O		D	O	O	O	O	O	O	O	O	O	O	O	O	O	O
GPIO3													O	O	O		O	D	O	O	O	O	O	O	O	O	O	O	O	O	O
GPIO4													O	O	O		O	O	D	O	O	O	O	O	O	O	O	O	O	O	O
PVID0													O	O	O																
PVID1													O	O	O																
PVID2													O	O	O																

Default	D
Optional	O
Not Applicable	

Digital Load Line

The droop current mirror has two gains for three rails. The first current mirror ratio (GAIN1) is configurable from 1/16, 1/8, 1/4, and 1/2 in register 28h bits[8:7].

The DC droop second current mirror ratio (GAIN2) can be configured to one of eight levels: 0, 3/4, 4/4, 5/4, 6/4, 7/4, 8/4, and 9/4 in register 28h bits[11:9].

The AC droop second current mirror ratio (GAIN2) can be configured to 1 or 1/2 in register 28h bit[13].

The load-line slope with the GAIN1 and GAIN2 current-sense gain, which is also referred to as the initial load-line slope (R_{LL_INI}), can be calculated with Equation (8):

$$R_{LL\_INI} = R_{DROOP} \times K_{CS} \times GAIN1 \times GAIN2 \quad (8)$$

Where R_{LL_INI} is the initial load-line slope (in Ω), K_{CS} is the current-sense gain of the Intelli-Phase™ (in A/A), and R_{DROOP} is the internal droop resistor (in Ω).

The 64 internal droop resistors for rail 1 are 25Ω resistors in series. They can be configured from 25Ω to 1.6kΩ (see Figure 16).

The 64 internal droop resistors for rail 2 are 100Ω resistors in series. They can be configured from 100Ω to 6.4kΩ.

The 64 internal droop resistors for rail 3 are 100Ω resistors in series. They can be configured from 100Ω to 6.4kΩ.

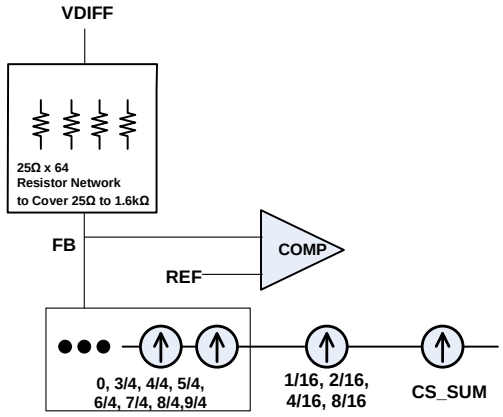


Figure 16: Digital Load Line for Rail 1

Fault Monitoring and Protections

The MP2926 supports various fault monitoring and protections. These protections are described below.

V_{IN} Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)

The VR shuts off immediately by forcing the PWM signals to tri-state if the sensed input voltage drops below the VIN_OFF threshold, and restarts again when the sensed input voltage exceeds the VIN_ON threshold. The V_{IN} under-voltage lockout (UVLO) threshold is configurable via registers VIN_ON (35h) and VIN_OFF (36h) with 31.25mV/LSB.

If the input voltage exceeds the V_{IN} over-voltage protection (OVP) threshold, set with register VIN_OV_FAULT_LIMIT (55h), the VR shuts off. VIN OVP can be selected to either latch-off or auto-retry mode.

Over-Current Protection (OCP)

Over-current protection (OCP) applies a dual-OCP mechanism with two types of thresholds:

The first type (OCP1) is a time-based and current-based threshold. The OCP1 limit is configured by the PMBus command IOUT_OC_FAULT_LIMIT (46h). OCP1 trips if the sensed average output current exceeds the setting threshold for a preset time (OCP1 blanking time).

The second type (OCP2) is only a current-based threshold. An optional OCP2 limit can be configured by the PMBus command IOUT_OC_FAULT_LIMIT (46h). If the cycle-by-cycle total sensed average output current exceeds the OCP2 threshold, OCP2 is triggered.

OCP1 and OCP2 can be programmed to no action, hiccup, retry 6 times, and latch-off mode via the PMBus.

The controller takes no action in no action mode and keeps switching until trips other protections. The fault indication bit in registers STATUS_IOUT (7Bh) and STATUS_WORD (79h) cannot be set to no action mode.

In hiccup mode, the controller forces the PWM signals to tri-state to disable the output, and attempt to restart after a 12.5ms protection delay time. This delay time can be configured by MFR_VR_CONFIG2 (C2h, Page 0) bits[14:13].

In retry 6 times mode, the VR restarts six times at most. If the fault is removed within six restarts, the VR resumes normal operation. If

the fault remains after the device retries six times, the VR shuts down. The VR does not turn on again until it receives a PMBus on command, EN is toggled, or power is cycled on VDD33.

In latch off mode, the VR shuts down until power is cycled on VDD33, EN is toggled, or the PMBus receives an on command again.

The above four protection modes are available for OCP1, OCP2, V_{OUT} under-voltage protection (UVP), V_{OUT} VID over-voltage protection (OVP), and V_{OUT} absolute over-voltage protection (OVP).

If either mechanism trips in any rail, then the MP2926 asserts OCP_L and delays any further action. This delay is called an action delay. If the current has not decreased below the threshold after the action delay has expired, the MP2926 can shut down the VR to protect the power MOSFETs.

In addition to the dual-OCP mechanism described above, the MP2926 utilizes an extra current-based limitation protection (OCP_PHASE). The MP2926 monitors the phase current cycle by cycle. If the phase current exceeds the OCP_PHASE threshold during the PWM off time, the PWM remains low to discharge the inductor current below the setting threshold.

If the present phase PWM on signal is blocked for longer than 80ns, the PWM on signal is skipped for this cycle, and the next phase turns on immediately to regulate the output voltage. Generally, per-phase OCP works with under-voltage protection (UVP) to protect the regulator system. The OCP_PHASE threshold is PMBus-configurable with register MFR_OCP_PHASE_LIMIT (49h).

Under-Voltage Protection (UVP)

The MP2926 provides under-voltage (UV) and over-voltage (OV) protection by monitoring V_{DIFF}.

If V_{DIFF} drops below the UVP threshold for a given time (the UVP blanking time), the controller forces the PWMs to tri-state to disable the output power (see Figure 17).

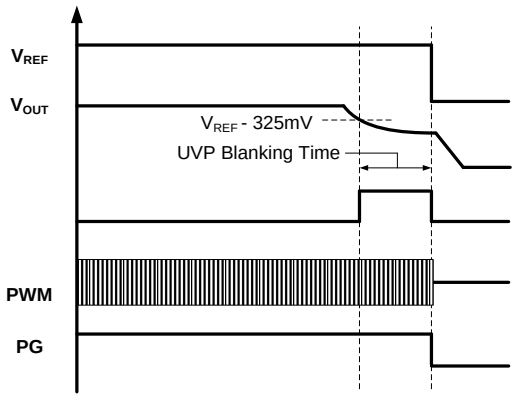


Figure 17: Under-Voltage Protection

The VOUT_UV_FAULT_RESPONSE (45h) register determines the UVP protection mode. Similar to the OCP1 protection scheme, the UVP scheme also provides no action, hiccup, retry 6 times, and latch-off mode.

The UVP threshold is configured via the PMBus command VOUT_UV_FAULT_LIMIT (44h).

Normally, UVP can be triggered when the per-phase OCP current limit is reached, and the PWM signals are blocked by the per-phase OC signals (see Figure 18).

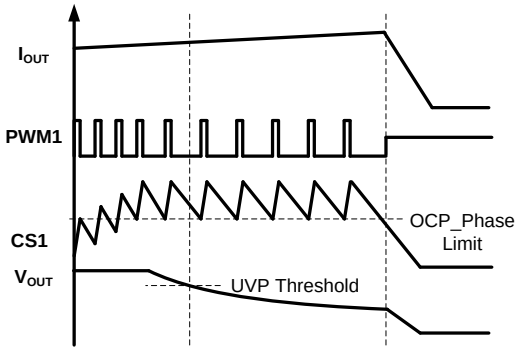


Figure 18: UVP Triggered when Per-Phase Current is Limited by OCP_PHASE

Over-Voltage Protection (OVP)

The MP2926 applies dual over-voltage protection (OVP) conditions: VID OVP and ABS OVP. If any OVP is tripped, the MP2926 turns on all LS-FETs to discharge C_{OUT} until V_{OUT} falls below 160mV, and then ends with Hi-Z off.

VID OVP is the OV protection type that refers to V_{REF}. It is tripped if V_{DIFF} exceeds the VID OVP threshold for the blanking time. The VID_OVP threshold is configured by PMBus command MFR_OV_FAULT_LIMIT (44h) bits[10:8].

Similar to UVP, the MP2926 provides no action, hiccup, retry 6 times, and latch off modes for VID OVP.

The second type is referred as ABS OVP, which is tripped if V_{DIFF} exceeds the ABS_OVP threshold without triggering the delay time. The ABS_OVP threshold is determined by VOUT_MAX (24h) and MFR_OV_FAULT_LIMIT (44h), bits[7:0]. The ABS_OVP fault response is always latch off mode.

Figure 19 shows the OVP waveforms of the MP2926.

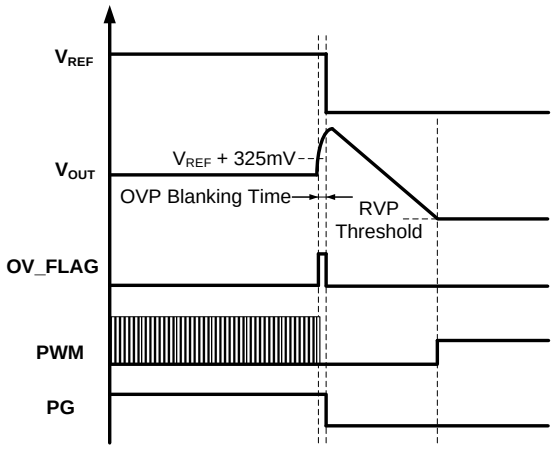


Figure 19: OVP Waveform

Reverse-Voltage Protection (RVP)

A large reverse inductor current may cause negative output voltages that can harm the processor and other output components. The MP2926 provides reverse-voltage protection (RVP) with no additional system cost.

If OVP occurs, all LS-FETs are forced on to discharge the voltage of the output capacitors. The inductor current becomes very negative, which can discharge the voltage of the output capacitors negative enough to destroy the load without RVP.

If the VOSEN voltage falls below 160mV after OVP, the MP2926 triggers RVP by latching all PWM outputs to tri-state. The reverse inductor current can quickly reset to 0A by dissipating the energy in the inductor to the input DC voltage source through the forward-biased body diode of the high-side MOSFETs (HS-FETs). Figure 19 shows the RVP function after OVP.

Over-Temperature Protection (OTP)

Over-temperature protection (OTP) is triggered if the sensed power stage temperature exceeds the maximum temperature threshold. The MP2926 can be configured in latch off mode or hiccup mode if OTP is triggered.

TSENS1, TSENS2, and TSENS3 have two modes for OTP: merge mode or separate mode. These modes are determined by MFR_VR_CONFIG2 (C2h) bit[12].

In merge mode, the MP2926 obtains the junction temperature of the Intelli-Phase™ by connecting VTEMP (TOUT) from the power stage to the controller's TSENS1. Moreover, TSENS3 can achieve OTP for any thermal area of the system by connecting it to the thermistor (PTC or NTC) at the thermal area. Figure 20 shows an example of temperature-sensing via TSENS3.

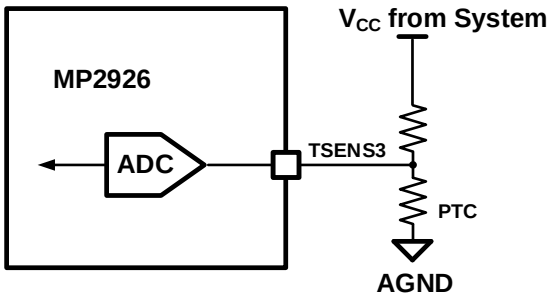


Figure 20: Temperature-Sensing via TSENS3 with PTC

If the temperature sensed via TSENS1 exceeds the threshold set by register MFR_OT_FAULT_LIMIT (4Fh, Page 0), the VR initiates Hi-Z shutdown. The OTP response can be configured to either latch off of auto-retry mode with PMBus command MFR_OT_FAULT_LIMIT (4Fh, page0).

If the temperature sensed via the TSENS3 pin drops below the preset threshold when MFR_TSENS3_SET (36h, Page 1) bit[1] = 1, or exceeds the preset threshold when MFR_TSENS3_SET (36h, Page 1) bit[1] = 0, the VR shuts down.

In separate mode, the TSENS pins monitor the temperature:

- TSENS1 monitors rail 1's temperature reporting

- TSENS2 monitors rail 2's temperature reporting
- TSENS3 monitors rail 3's temperature reporting

Line Float Detection

The MP2926 supports remote sensing line float detection (VOSEN, VORTN) during system initialization, after VDD33 powers on or EN powers on from low-power mode. The MP2926 latches off if a line float is detected, and reports the fault with PMBus command STATUS_VOUT (7Ah), bit[1]. Line float detection can be enabled with MFR_VR_CONFIG4 (C4h, Page 0).

CS Fault and TEMP Fault

The MP2926 supports TEMP faults and CS faults for fast protection if any phase's DrMOS experiences a fault. If the voltage on the TSENS1, TSENS2, or TSENS3 pins exceed 2.2V, the output is disabled for a TEMP fault. If any CS pin is pulled below 160mV, a CS fault takes action to shut off the output.

NVM Faults

The data in the NVM is invalid after the CRC check during the power-on NVM reading process. The VR cannot start until the fault is cleared.

Communication Failure

A data transmission fault occurs if information is not properly transferred between the devices. There are several data transmission faults, listed below:

- Sent too little data
- Read too little data
- Host sent too many bytes
- Read too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The data transmission faults assert ALT_P#. The CLEAR_FAULTS command de-asserts ALT_P#. If the faults remain, ALT_P# asserts again.

Intelli-Phase™ Fault Detection

The MP2926 can detect the type of Intelli-Phase™ fault. There are several types of Intelli-Phase™ faults:

- Current-limit fault
- Over-temperature
- LS-FET shorted fault
- HS-FET shorted fault

This function only works when the Intelli-Phase™ supports fault type indication. Refer to the Intelli-Phase™ datasheet for specific details.

The MP2926 scans the PWM fault after any of the following faults occurs: V_{IN} under-voltage lockout (UVLO), V_{IN} over-voltage protection (OVP), over-temperature protection (OTP), V_{OUT} under-voltage protection (UVP), V_{OUT} OVP, over-current protection (OCP), VTEMP faults, and CS faults if the relevant fault protection and PWM fault detection are both enabled.

When any of the above faults are triggered, the MP2926 follows the steps described below (see Figure 21):

1. Shuts off the associated rail(s).
2. Starts the Intelli-Phase™ fault type scan for related rail(s) by sensing the impedance on the PWM pins (if this function is enabled via register MFR_VR_CONFIG2(C2h) bits[11:9]).
3. Report faults to the FAULTS_REPORT registers (E0~E5h, Page 1).
4. Faults are recorded to the NVM (registers F0h~F5h, page1) when fault recording to the NVM is enabled via MFR_NVM_CTRL (55h, Page 2) bit[1]). The last fault event is stored. To allow fault storing to the NVM, the EN signal should be kept high for at least 20ms after the fault occurs.
5. To clear the record faults in the NVM register, send a FEh, 0-byte command.

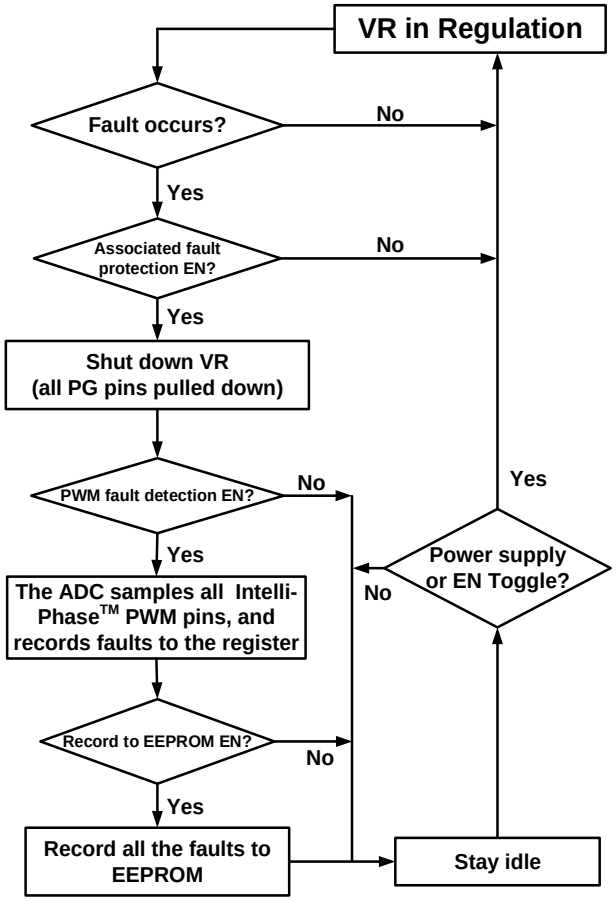


Figure 21: Intelli-Phase™ Fault Detection Flowchart

PMBus Communication

The MP2926 supports real-time monitoring for the VR operation parameters and status with PMBus interface. Table 3 lists the monitored parameters.

Table 3: PMBus-Monitored Parameters

Parameter	PMBus
Output voltage	6.25mV/LSB
Output current	0.25A/LSB or 0.5A/LSB
Temperature	1°C
Input voltage	31.25mV/LSB
OVP	✓
UVP	✓
OCP	✓
OTP	✓
VIN_UVLO	✓
VIN_OV	✓
Line float	✓
CML	✓

PMBus/I²C Interface

To support multiple VR devices being used with the same PMBus/I²C interface, the MFR_ADDR_PMBUS (77h, page0) register or the ADDR pin can be used to configure the PMBus address.

The address is a 7-bit code. The 3MSB bit is set by the register. The 4LSB bit address can either be set by the register or by the ADDR voltage. Address 00h is reserved as an all-call address, which can be set for a single chip.

The ADDR voltage is set by the voltage divider from the VDD18 voltage. Table 4 shows the resistor values for different PMBus addresses when the 3MSB bit is set to 3'b010.

Table 4: Pin Configuration for PMBus Address

PMBus Address	Setting Point (V)	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%
20h	0	-	0
21h	0.047	3.32	0.0887
22h	0.078	3.32	0.15
23h	0.109	3.32	0.215
24h	0.145	3.32	0.287
25h	0.188	3.32	0.383
26h	0.238	3.32	0.51
27h	0.297	3.32	0.649
28h	0.367	3.32	0.845
29h	0.461	3.32	1.15
2Ah	0.578	3.32	1.58
2Bh	0.715	3.32	2.2
2Ch	0.879	3.32	3.16
2Dh	1.078	3.32	4.99
2Eh	1.320	3.32	9.1
2Fh	1.527	3.32	18.7

Figure 22 shows the supported PMBus/I²C transmission structure without packet error checking (PEC).

Figure 23 shows the supported PMBus/I²C transmission structure with PEC.

There are six types of transmission structures:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word
6. Block read

To read or write the MP2926 registers, the PMBus or I²C command correspond with the byte number of the register in the table of PMBus commands for rail 1 and rail 2. PMBus/I²C communication can support speeds up to 1MHz.

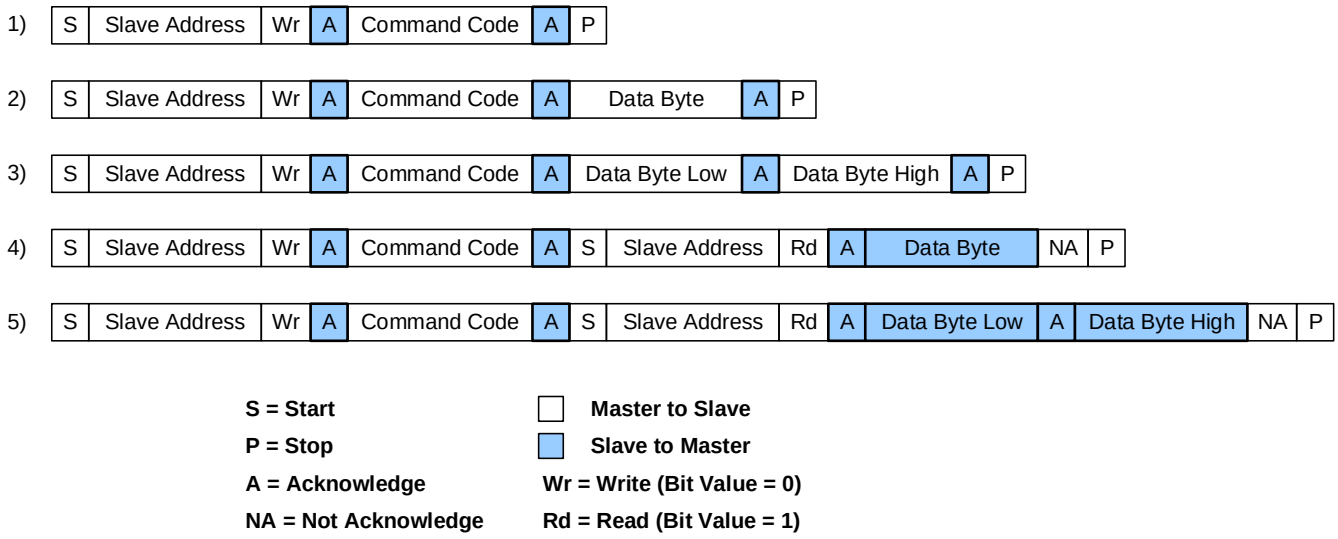


Figure 22: Supported PMBus/I²C Transmission Structure without PEC

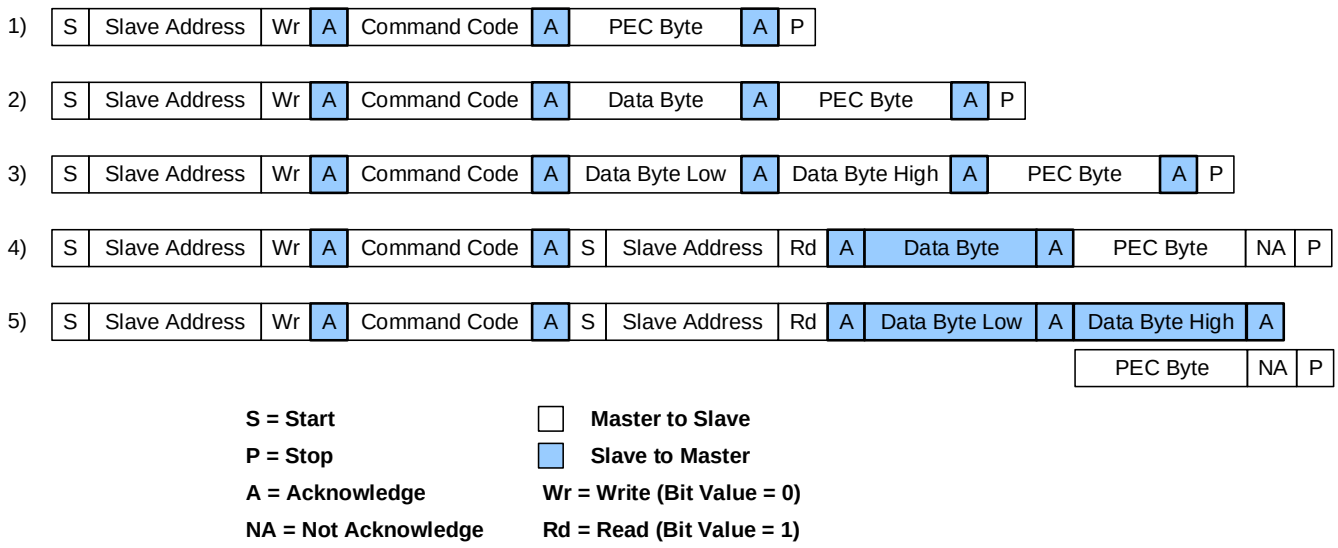


Figure 23: Supported PMBus/I²C Transmission Structure with PEC

PVID Mode

The MP2926 supports 3-bit PVID mode to control V_{OUT} by setting the PVID_ENx bits in register C1h (Page 0) bits[10:8].

The PVID voltage can be set by toggling the PVID pins or by setting register MFR_PVID0 (71h). It determined by VR_CONFIG1 C1h (Page 0) bit[11].

When selecting the pins or toggling the PVID pins, the corresponding PVID_VID value is read from 71h~74h as the new target VID.

There are eight types of PVID voltages with eight different combinations of high/low (H/L) for PVID0, PVID1, and PVID2. Registers 71h~74h are for configuring the PVID voltage with 6.25mV/LSB (see Table 5).

In PVID mode, the power good flag asserts after the V_{BOOT} VID target is reached, and it de-

asserts when EN is pulled low or a protection is triggered to shut down the VR.

Table 5: PVID_VID in Registers 71h through 74h

PVID2	PVID1	PVID0	PVID Voltage	VID_Rail1 (Page 0)	VID_Rail2 (Page 1)	VID_Rail3 (Page 2)
L	L	L	PVID_000	71h bits[7:0]	71h bits [7:0]	71h bits [7:0]
L	L	H	PVID_001	71h bits[15:8]	71h bits [15:8]	71h bits [15:8]
L	H	L	PVID_010	72h bits[7:0]	72h bits [7:0]	72h bits[7:0]
L	H	H	PVID_011	72h bits[15:8]	72h bits [15:8]	72h bits[15:8]
H	L	L	PVID_100	73h bits[7:0]	73h bits [7:0]	73h bits[7:0]
H	L	H	PVID_101	73h bits[15:8]	73h bits [15:8]	73h bits[15:8]
H	H	L	PVID_110	74h bits[7:0]	74h bits [7:0]	74h bits[7:0]
H	H	H	PVID_111	74h bits [15:8]	74h bits [15:8]	74h bits[15:8]

PMBUS COMMANDS

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
00h	PAGE	R/W	1	✓	✓	✓
01h	OPERATION	R/W	1	✓	✓	✓
03h	CLEAR_FAULTS	Send	0	✓	✓	✓
10h	WRITE_PROTECT	R/W	1	✓		
15h	STORE_ALL_CODE	Send	0	✓	✓	✓
16h	RESTORE_ALL_CODE	Send	0	✓	✓	✓
17h	STORE_USER_CODE	Send	0	✓	✓	✓
18h	RESTORE_USER_CODE	Send	0	✓	✓	✓
20h	VOUT_MODE	R/W	2	✓		
21h	VOUT_COMMAND	R/W	2	✓	✓	✓
22h	MFR_VOUT_TRIM	R/W	2	✓	✓	✓
23h	MFR_SD_VID_SET	R/W	2	✓		
	VDIFF1_SNAPSHOT	R	2			✓
24h	VOUT_MAX	R/W	2	✓	✓	✓
25h	MFR_JOUT_LONG_TERM	R/W	2	✓	✓	✓
26h	MFR_JOUT_SHORT_TERM	R/W	2	✓	✓	✓
27h	VOUT_TRANSITION_RATE	R/W	2	✓	✓	✓
28h	VOUT_DROOP	R/W	2	✓	✓	✓
29h	VOUT_SCALE_LOOP	R/W	2	✓	✓	✓
2Ah	MFR_SETTLE_CTRL	R/W	2	✓	✓	✓
2Bh	VOUT_MIN	R/W	2	✓	✓	✓
2Ch	MFR_TRIM_DCM_1P_2P	R/W	2	✓	✓	✓
2Dh	(MFR RESERVED)	R/W	2	✓	✓	
	MFR_PMBUS_VTH	R/W	2			✓
2Eh	(MFR RESERVED)	R/W	2	✓		✓
2Fh	(MFR RESERVED)	R/W	2	✓	✓	✓
30h	(MFR RESERVED)	R/W	2	✓		✓
31h	MFR_BLANK_TIME1	R/W	2	✓	✓	✓
32h	MFR_PRT_CONFIG	R/W	2	✓		
	VIN_SCALE_LOOP	R/W	2		✓	
	MFR_PI_LOOP	R/W	2			✓
33h	FREQUENCY_SWITCH	R/W	2	✓	✓	✓
34h	MFR_OSR_SET	R/W	2	✓	✓	✓
35h	VIN_ON	R/W	2	✓		
	(MFR RESERVED)	R/W	2			✓
36h	VIN_OFF	R/W	2	✓		
	MFR_TSENS3_SET	R/W	2		✓	
	(MFR RESERVED)	R/W	2			✓
37h	MFR_SLOPE_SW_INI	R/W	2	✓	✓	✓
38h	MFR_SLOPE_SR_DCM	R/W	2	✓	✓	✓
39h	MFR_SLOPE_SR_1P	R/W	2	✓	✓	✓

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
3Ah	MFR_SLOPE_SR_2P	R/W	2	✓	✓	✓
3Bh	(MFR RESERVED)	R/W	2	✓	✓	✓
3Ch	(MFR RESERVED)	R/W	2	✓	✓	
	MFR_TRIM_SEL	R/W	2			✓
3Dh	(MFR RESERVED)	R/W	2	✓	✓	
	MFR_TRIM_SEL_R3	R/W	2			✓
3Eh	MFR_VRHOT_SET	R/W	2	✓	✓	✓
3Fh	(MFR RESERVED)	R/W	2	✓	✓	✓
40h	VOUT_OV_FAULT_LIMIT	R/W	2	✓	✓	✓
41h	VOUT_OV_FAULT_RESPONSE	R/W	2	✓	✓	✓
42h	VOUT_MAX_ALERT	R/W	2	✓	✓	✓
43h	VOUT_MIN_ALERT	R/W	2	✓	✓	✓
44h	VOUT_UV_FAULT_LIMIT	R/W	2	✓	✓	✓
45h	VOUT_UV_FAULT_RESPONSE	R/W	2	✓	✓	✓
46h	IOUT_OC_FAULT_LIMIT	R/W	2	✓	✓	✓
47h	IOUT_OC_FAULT_RESPONSE	R/W	2	✓	✓	✓
48h	IOUT_OC_SPIKE_RESPONSE	R/W	2	✓	✓	✓
49h	MFR_OCP_PHASE_LIMIT	R/W	2	✓	✓	✓
4Ah	IOUT_MAX_ALERT	R/W	2	✓	✓	✓
4Bh	MFR_FS_LIMIT_12P	R/W	2	✓	✓	✓
4Ch	(MFR RESERVED)	R/W	2	✓	✓	✓
4Dh	MFR_APS_LEVEL_12P	R/W	2	✓	✓	✓
4Eh	(MFR RESERVED)	R/W	2	✓	✓	✓
4Fh	OT_FAULT_LIMIT	R/W	2	✓	✓	✓
50h	MFR_CORE_OTP_SET	R/W	2	✓		
	MFR_NVM_WP	R/W	2		✓	
	MFR_SMBALERT_MASK	R/W	2			✓
51h	MFR_FS_DETECT	R/W	2	✓	✓	✓
52h	MFR_APS_CTRL	R/W	2	✓	✓	✓
53h	MFR_APS_CTRL2	R/W	2	✓	✓	✓
54h	MFR_APS_CTRL3	R/W	2	✓	✓	✓
55h	VIN_OV_FAULT_LIMIT	R/W	2	✓		
	MFR_CUSTOMER_ID	R/W	2		✓	
	MFR_NVM_CTRL	R/W	2			✓
56h	MFR_FSCB_LOOP_CTRL	R/W	2	✓	✓	✓
57h	MFR_VOUT_LOOP_CTRL	R/W	2	✓	✓	✓
58h	JOUT_SHORT_PK	R/W	2	✓	✓	✓
59h	JOUT_LONG_PK	R/W	2	✓	✓	✓
5Ah	MFR_SLOPE_CNT_1P	R/W	2	✓	✓	✓

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
5Bh	MFR_SLOPE_CNT_23P	R/W	2	✓	✓	✓
5Ch	(MFR RESERVED)	R/W	2	✓	✓	
	VDIFF2_SNAPSHOT	R	2			✓
5Dh	(MFR RESERVED)	R/W	2	✓		
	VDIFF3_SNAPSHOT	R	2			✓
5Eh	MFR_SLOPE_CNT_DCM	R/W	2	✓	✓	✓
5Fh	MFR_PG_DELAY	R/W	2	✓	✓	✓
60h	TON_DELAY	R/W	2	✓	✓	✓
61h	TON_RISE	R/W	2	✓	✓	✓
62h	MFR_PWM_MIN_TIME1	R/W	2	✓	✓	✓
63h	MFR_PWM_MIN_TIME2	R/W	2	✓	✓	✓
64h	TOFF_DELAY	R/W	2	✓	✓	✓
65h	TOFF_FALL	R/W	2	✓	✓	✓
66h	GPIO_SEL_GROUP1	R/W	2	✓		
	(MFR RESERVED)	R/W	2		✓	
	GPIO_SEL_GROUP5	R/W	2			✓
67h	(MFR RESERVED)	R/W	2	✓		
	GPIO_SEL_GROUP4	R/W	2		✓	
	GPIO_SEL_GROUP6	R/W	2			✓
68h	GPIO_MODE	R/W	2	✓		
	GPIO_ACTIVE	R/W	2		✓	
	MFR_EN_SEL	R/W	2			✓
69h	MFR_VR_TEMP_CAL	R/W	2	✓	✓	✓
6Ah	MFR_VOUT_CALC	R/W	2	✓	✓	✓
6Bh	(MFR RESERVED)	R/W	2	✓	✓	✓
6Ch	IOUT_CAL_GAIN_PMBUS	R/W	2	✓	✓	✓
6Dh	IOUT_CAL_OS_PMBUS	R/W	2	✓	✓	✓
6Eh	MFR_IMON_SET	R/W	2	✓	✓	✓
6Fh	IOUT_MIN_ALERT	R/W	2	✓	✓	✓
70h	MFR_PHASE_CFG	R/W	2	✓		
	MFR_CONFIG_ID	R/W	2		✓	
	MFR_PSI_SET	R/W	2			✓
71h	MFR_PVID01	R/W	2	✓	✓	✓
72h	MFR_PVID23	R/W	2	✓	✓	✓
73h	MFR_PVID45	R/W	2	✓	✓	✓
74h	MFR_PVID67	R/W	2	✓	✓	✓
75h	SAMPLE_INTERVAL_12P	R/W	2	✓	✓	✓
76h	CRC_REG_USER	R/W	2			✓
77h	MFR_ADDR_PMBUS	R/W	2	✓		
	CRC_REG_TRIM	R/W	2			✓

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
78h	STATUS_BYTE	R	1	✓	✓	✓
79h	STATUS_WORD	R	2	✓	✓	✓
7Ah	STATUS_VOUT	R	1	✓	✓	✓
7Bh	STATUS_IOUT	R	1	✓	✓	✓
7Ch	STATUS_INPUT	R	1	✓	✓	✓
7Dh	STATUS_TEMPERATURE	R	1	✓	✓	✓
7Eh	STATUS_CML	R	1	✓	✓	✓
81h	READ_ADC_SUM	R	2	✓	✓	✓
82h	READ_VFB_SENSE	R	2	✓	✓	✓
83h	READ_TSENS1_SENSE	R	2	✓		
	READ_TSENS3_SENSE	R	2		✓	
	READ_TSENS2_SENSE	R	2			✓
84h	READ_CS1	R	2	✓		
	READ_CS3	R	2			✓
85h	READ_CS2	R	2	✓		
	READ_CS4	R	2			✓
86h	READ_CS5	R	2			✓
87h	READ_CS6	R	2			✓
88h	READ_VIN	R	2	✓	✓	✓
8Bh	READ_VOUT	R	2	✓	✓	✓
8Ch	READ_IOUT	R	2	✓	✓	✓
8Dh	READ_TEMPERATURE	R	2	✓	✓	✓
8Eh	READ_PH_NVM	R	2	✓		
	READ_ADC_RESULT	R	2		✓	✓
8Fh	READ_VCOMP	R	2	✓	✓	✓
96h	READ_POUT	R	2	✓	✓	✓
98h	PMBUS_REVISION	R	2	✓		
99h	MFR_ID	R	Block	✓		
9Ah	MFR_MODEL	R	Block	✓		
9Bh	MFR_REVISION	R	Block	✓		
9Dh	MFR_DATE	R	Block	✓		
9Fh	MFR_PRODUCT_ID	R/W	2	✓		
C0h	MFR_PRODUCT_REV	R	1	✓		
	(MFR_RESERVED)	R/W	2		✓	
C1h	MFR_VR_CONFIG1	R/W	2	✓		
C2h	MFR_VR_CONFIG2	R/W	2	✓		
C3h	MFR_VR_CONFIG3	R/W	2	✓		
C4h	MFR_VR_CONFIG4	R/W	2	✓		
C5h	MFR_VR_CONFIG5	R/W	2	✓		
C6h	MFR_VR_CONFIG6	R/W	2	✓		
C7h	MFR_VR_CONFIG7	R/W	2	✓		
C8h	MFR_TIMEOUT	R/W	2	✓		

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
D0h	CAPABILITY	R	2	✓	✓	✓
D1h	JOUT_SHORT_TERM	R	2	✓	✓	✓
D2h	JOUT_LONG_TERM	R	2	✓	✓	✓
D3h	IMON_FAST_SENSE	R	2	✓	✓	✓
D4h	VDIFF_FAST_SENSE	R	2	✓	✓	✓
D5h	DIE_TEMP_SENSE	R	2		✓	
E0h	FAULTS_REPORT1	R	2		✓	
E1h	FAULTS_REPORT2	R	2		✓	
E2h	FAULTS_REPORT3	R	2		✓	
E3h	FAULTS_REPORT4	R	2		✓	
E4h	FAULTS_REPORT5	R	2		✓	
E5h	FAULTS_REPORT6	R	2		✓	
F0h	FAULTS_RECORD1	R	2		✓	
F1h	FAULTS_RECORD2	R	2		✓	
F2h	FAULTS_RECORD3	R	2		✓	
F3h	FAULTS_RECORD4	R	2		✓	
F4h	FAULTS_RECORD5	R	2		✓	
F5h	FAULTS_RECORD6	R	2		✓	
FBh	ADC_SUM_RESET	Send	0	✓	✓	✓
FCh	CLEAR CRC FAULT	Send	0	✓	✓	✓
FEh	CLEAR_STORED_FAULTS	Send	0	✓	✓	✓
FFh	CLEAR_NVM_FAULTS	Send	0	✓	✓	✓

PAGE 0 REGISTER MAP

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor all registers (including test mode and the NVM) through only one physical address.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
7:2	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
1:0	PAGE	0x00: Page 0. All PMBus commands address operating registers Page 0 0x01: Page 1. All PMBus commands address operating registers Page 1 0x02: Page 2. All PMBus commands address operating registers Page 2 0x03: Page 3. All PMBus commands address the test mode registers 0x28: Page 28. All PMBus commands address the NVM registers that are mapped to Page 0 operating registers 0x29: Page 29. All PMBus commands address the NVM registers that are mapped to Page 1 operating registers 0x2A: Page 2A. All PMBus commands address the NVM registers that are mapped to Page 2 operating registers

OPERATION_R1 (01h)

The OPERATION_R1 command on Page 0 turns the rail 1 output on or off in conjunction with the input from the EN pin, and sets the output voltage to the upper or lower margin voltages. The controller stays in the OPERATION command setting mode until a subsequent OPERATION command is received, or a change in the EN state changes rail 1 to another mode.

Command	OPERATION_R1							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								

Bits	Bit Name	Description
7:0	OPERATION_R1	Sets the operation mode for rail 1. 8’b 00xx xxxx: Hi-Z off 8’b 01xx xxxx: Soft-off 8’b 1000 xxxx: Normal on 8’b 1001 xxxx: Margin low 8’b 1010 xxxx: Margin high Others: Unused “x” means not applicable.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command clears any fault bit in the following status registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), and STATUS_CML (7Eh).

This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

The WRITE_PROTECT command controls writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate changes to a device's configuration or operation. All support commands can have their parameters read, regardless of the WRITE_PROTECT settings.

Command	WRITE_PROTECT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	WRITE_PROTECT							

Bits	Bit Name	Description
7:0	WRITE_PROTECT	0x80: Disable all writes except to the WRITE_PROTECT command 0x40: Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 0x20: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND commands 0x00: Enable writes to all commands Other commands are invalid

STORE_ALL_CODE (15h)

The STORE_ALL_CODE command instructs the PMBus device to copy all Page 0, Page 1, and Page 2 contents, including internal trim registers of the operating memory, to the matching locations in the NVM. Any items in the operating memory that do not have matching locations in the user store are ignored. This command is controlled by 50h (Page 1) bits[7:0]. When bits[7:0] is set to 0x63, the NVM can be written. The NVM is write-protected for all other values.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents, including internal trim registers from the NVM, and overwrites the matching locations in the operating memory. Any items in the user store that do not have matching locations in the operating memory are ignored.

While the device is outputting power, this command is ignored, and cannot be used. This command is write-only. There is no data byte for this command.

STORE_USER_CODE (17h)

The STORE_USER_CODE command instructs the PMBus to copy the Page 0, Page 1, and Page 2 operating memory contents to the matching locations in the NVM, except the internal trim registers. Items in the operating memory that do not have matching locations in the user store are ignored.

This command is controlled by register 50h (Page 1) bits[7:0]. When bits[7:0] are set to 0x63, the NVM can be written. The NVM is write-protected for all other values.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_USER_CODE (18h)

The RESTORE_USER_CODE command instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the NVM, and overwrites the matching locations in the operating memory. Trim registers are not overwritten by this command.

While the device is outputting power, this command is ignored, and cannot be used. This command is write-only. There is no data byte for this command.

VOUT_MODE (20h)

The VOUT_MODE command on Page 0 returns key VID features that the MP2926 can support.

Command	VOUT_MODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								

Bits	Bit Name	Description
7:5	DEVICE_VOUT_MODE	3’b000: Linear mode 3’b010: Direct mode
4:0	EXPONENT	Linear mode: 5-bit two’s complement exponent for the mantissa is delivered as the data bytes for a command related to the output voltage. Set EXP to 5’b 10111. The resolution is 2mV. Direct mode: Always set to 5’b 00000.

VOUT_COMMAND_R1 (21h)

The VOUT_COMMAND_R1 on Page 0 sets the rail 1 reference voltage VID in PMBus override mode.

Command	VOUT_COMMAND_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_COMMAND_R1	Sets the rail 1 reference voltage (VID_DAC output voltage) in PMBus VID mode. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].

VOUT_TRIM_R1 (22h)

The VOUT_TRIM_R1 command on Page 0 applies a fixed offset voltage to the rail 1 output voltage command value.

Command	VOUT_TRIM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRIM_R1	Sets the V_{OUT} offset. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].

MFR_SD_VID_SET (23h)

MFR_SD_VID command on Page 0 sets the Hi-Z shutdown voltage level. It is only effective while VID slews down to 0V.

Command	MFR_SD_VID_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:8	MFR_VID_OFF	Sets the minimum operating V_{REF} for three rails. If the target VID (in PVID or PMBus mode) drops below MFR_VID_OFF, the associated DVID rail drops to 0V and de-asserts the PG signal. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].
7:0	MFR_SD_VID	Sets the PWM Hi-Z shutdown voltage level. If the VID DAC output drops below the Hi-Z shutdown voltage threshold, the output enters PWM Hi-Z shutdown mode. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].

VOUT_MAX_R1 (24h)

The VOUT_MAX_R1 command on Page 0 sets the maximum reference voltage for rail 1 VID-DAC, so as to set the maximum output voltage. When an external resistor divider is applied, the maximum voltage is clamped to VOUT_MAX / K_R. K_R is the dividing ratio of the external resistor divider. It is effective in PMBus mode and PVID mode.

Command	VOUT_MAX_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MAX_R1	Sets the rail 1 maximum VID + offset voltage. It limits the sum of the VID + VOUT_TRIM offset. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].

MFR_JOUT_LONG_TERM_R1 (25h)

The MFR_JOUT_LONG_TERM_R1 command on Page 0 sets the LONG_TERM value to calculate J_{OUT}.

Command	MFR_JOUT_LONG_TERM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	JOUT_LONG_ TERM	Sets the long-term value for J_{OUT} calculation. LONG_TIME = JOUT_LONG_TERM x SHORT_TIME

MFR_JOUT_SHORT_TERM_R1 (26h)

The MFR_JOUT_SHORT_TERM_R1 command on Page 0 sets the SHORT_TERM value to calculate J_{OUT}.

Command	MFR_JOUT_SHORT_TERM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		X														

Bits	Bit Name	Description
15	JOUT_METHOD_SEL	Selects the J_{OUT} calculation method. 1'b1: Fixed frequency. Samples the current and voltage with a fixed frequency. 1'b0: Adjustable frequency. Samples the current and voltage after a delayed time at the PWM1 falling edge.
14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	JOUT_EN	Enable bit for the J_{OUT} function. 1'b1: Enabled 1'b0: Disabled
12:7	JOUT_SHORT_ TERM_FIX_FREQ	Fixed to 0 in fixed frequency mode.
6:0		Sets JOUT_SHORT_TERM in fixed frequency mode. ADC_TIME/LSB. The time can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_FIX_FREQ x ADC_TIME
12:1	JOUT_SHORT_TERM_ ADAPTIVE_FREQ	50ns/LSB in adaptive frequency mode. The time can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_ADAPTIVE_FREQ x 50ns
0		Fixed to 0 in adaptive frequency mode.

VOUT_TRANSITION_RATE_R1 (27h)

The VOUT_TRANSITION_RATE_R1 command on Page 0 sets the rail 1 dynamic VID transition slew rate in PMBus and PVID mode.

Command	VOUT_TRANSITION_RATE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	VOUT_TRANSITION_ RATE_R1	Sets the rail 1 dynamic VID transition slew rate in PMBus and PVID mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h) bit[15].

VOUT_DROOP_R1 (28h)

The VOUT_DROOP_R1 command on Page 0 sets the rail 1 load line parameters.

Command	VOUT_DROOP_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	IACDROOP_BW _R1	Enable bit to increase the AC droop BW by increasing the bias current. For rail 1 only. 1'b0: Disabled 1'b1: Enabled
14	IACDROOP_BW_R1	Enable bit to increase the AC droop BW by reducing the compensation capacitor. For rail 1 only. 1'b0: Disabled 1'b1: Enabled
13	IACDROOP_GAIN2_R1	Sets the PMBus AC droop's second current mirror ratio (GAIN2) for rail1. It is active when bit [12] = 1. 1'b0: 1 1'b1: 1/2
12	MFR_ACLL_EN_R1	AC or DC load line selection bit. 1'b0: DC load line 1'b1: AC load line

11:9	IDROOP_ GAIN2_R1	Sets the PMBus DC droop's second current mirror ratio (GAIN2) for rail1. It is active when bit[12] = 0. The MP2926 provides eight configurable levels. 3'b000: 0 3'b001: 3/4 3'b010: 4/4 3'b011: 5/4 3'b100: 6/4 3'b101: 7/4 3'b110: 8/4 3'b111: 9/4
8:7	IDROOP_GAIN1_R1	Sets the PMBus I_{DROOP} first current mirror ratio (GAIN1) for rail 1. The initial load line slope can be calculated with the following equation: $R_{LL\_INI} = R_{DROOP} \times K_{CS} \times GAIN1 \times GAIN2$ 2'b00: 1/16 2'b01: 1/8 2'b10: 1/4 2'b11: 1/2
6	SHORT_FIRST_HALF_R1	1'b0: Do not short the first half resistors for rail 1 1'b1: Short the first half resistors for rail 1 Set to 1 if R_{DROOP} is below 800Ω.
5:0	RDROOP_SET_R1	Sets R_{DROOP} for rail 1. 25Ω/LSB. 1.6kΩ maximum.

VOUT_SCALE_LOOP_R1 (29h)

The VOUT_SCALE_LOOP_R1 command on Page 0 sets the rail 1 output voltage to reference voltage dividing ratio when an external output divider is applied.

Command	VOUT_SCALE_LOOP_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	**Bit Name**	**Description**
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VOUT_SCALE_ LOOP_R1	Sets the rail 1 output voltage to reference voltage dividing ratio. V_{REF} ranges from 0V to 1.55V.

MFR_SETTLE_CTRL_R1 (2Ah)

The MFR_SETTLE_CTRL_R1 command on Page 0 sets the DVID parameters.

Command	MFR_SETTLE_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	**Bit Name**	**Description**
15:11	MFR_DROOPFALL_ DELAY_R1	Sets the delay time between V_{REF} reaching the target (VID + DROOP_VID) and V_{REF} falling back to VID. 50ns/LSB.
10:6	MFR_RISE_STEP_R1	Sets the extra VID step count for rail 1 when DVID is up. The extra VID steps compensate for the droop caused by the output capacitor charging during DVID up. 1 step/LSB.

5:0	RESERVED	Fixed to 0.

VOUT_MIN_R1 (2Bh)

The VOUT_MIN_R1 command on Page 0 instructs the device to limit the rail 1 minimum output voltage in PMBus and PVID mode. When the output voltage decoded from the PMBus interface or set by PVID registers below what is set by VOUT_MIN (2Bh), the output voltage is clamped to VOUT_MIN. When an external resistor divider is applied on VOSEN, the minimum output voltage is clamped to VOUT_MIN / K_R. Where K_R is the dividing ratio of the divider.

Command	VOUT_MIN_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MIN_R1	Sets rail 1 minimum's VID in PMBus mode. Any VID below this value is clamped to VOUT_MIN. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].

MFR_TRIM_DCM_1P_2P_R1 (2Ch)

The MFR_TRIM_DCM_1P_2P_R1 command on Page 0 trims the output voltage for 2-phase CCM and 1-phase CCM and the DCM power state of rail 1.

Command	MFR_TRIM_DCM_1P_2P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	MFR_TRIM_2PS_R1	Sets the V_{OUT} trim for 2-phase CCM operation. 2.3mV/LSB.
9:5	MFR_TRIM_1PS_R1	Sets the V_{OUT} trim for 1-phase CCM operation. 2.3mV/LSB.
4:0	MFR_TRIM_DCM_R1	Sets the V_{OUT} trim for 1-phase DCM operation. 2.3mV/LSB.

MFR_RESERVED (2Dh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (2Eh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (2Fh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (30h)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_BLANK_TIME1_R1 (31h)

The MFR_BLANK_TIME1_R1 command on Page 0 programs the slope compensation reset time and the PWM blanking time between two consecutive phases.

Command	MFR_BLANK_TIME1_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:12	RESERVED	Fixed to 0.
11:6	MFR_SLOPE_BLANK_TIME1_R1	Program the slope compensation reset time. The slope compensation reset time should not be longer than PWM blanking time set by PWM_BLANK_TIME (e.g. bit [5:0] in register MFR_BLANK_TIME1 (31h, Page 0). 5ns/LSB.
5:0	MFR_PHASE_BLANK_TIME1_R1	Programs the PWM blanking time between two consecutive phases. 5ns/LSB.

MFR_PRT_CONFIG (32h)

The MFR_PRT_CONFIG command on Page 0 sets certain MP2926 configurations.

Command	MFR_PRT_CONFIG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	OT_WARN_EN	Enables the over-temperature (OT) warning function. If an OT warning occurs, ALT_P# is asserted. 1'b0: OT warning disabled for both rails 1'b1: OT warning enabled for both rails
14	OC_WARN_EN	Enables the over-current (OC) warning function. If an OC warning occurs, ALT_P# is asserted. 1'b0: OC warning disabled for both rails 1'b1: OC warning enabled for both rails
13	UV_WARN_EN	Enables the under-voltage (UV) warning function. If a UV warning occurs, ALT_P# is asserted. 1'b0: UV warning disabled for both rails 1'b1: UV warning enabled for both rails
12	OV_WARN_EN	Enables the over-voltage (OV) warning function. If an OV warning occurs, ALT_P# is asserted. 1'b0: OV warning disabled for both rails 1'b1: OV warning enabled for both rails
11:10	MFR_VIN_UVP_MODE	Sets the V_{IN} under-voltage protection (UVP) response. 2'b00: No action 2'b01: Latch off 2'b1x: Retry
9	MFR_VIN_OVP_MODE	Sets the V_{IN} over-voltage protection (OVP) mode. 1'b0: Retry 1'b1: Latch off
8	MFR_VINUV_WARN_EN	Enables the V_{IN} under-voltage (UV) warning function. If a V_{IN} UV warning occurs, ALT_P# is asserted. 1'b0: Disable V_{IN} UV warning 1'b1: Enable V_{IN} UV warning
7	MFR_VIN_FLT_EN	Enables all V_{IN} fault functions. 1'b0: Disable all V_{IN} protections 1'b1: Enable all V_{IN} faults
6	MFR_CORE_OTP_EN	Enables chip over-temperature protection (OTP). If chip OTP occurs, ALT_P# is asserted. 1'b0: Disable chip OTP 1'b1: Enable chip OTP
5	MFR_OTP_EN_R3	Enables rail 3 over-temperature protection (OTP). 1'b0: Disable DrMOS OTP 1'b1: Enable DrMOS OTP

4	MFR_OTP_EN_R2	Enables rail 2 over-temperature protection (OTP). 1'b0: Disable DrMOS OTP 1'b1: Enable DrMOS OTP
3	MFR_OTP_EN_R1	Enables rail 1 over-temperature protection (OTP) in independent mode. In merge mode, this bit controls all rails. 1'b0: Disable DrMOS OTP 1'b1: Enable DrMOS OTP
2	MFR_CSPIN_FAULT_EN	Enable bit for the CS pin to indicate a DrMOS fault indicator and record the fault to the NVM. The MP2926 monitors the CS pin voltage. If the CS pin voltage drops below 160mV, this means a DrMOS fault has occurred. 1'b0: Disable all CS faults 1'b1: Enable all CS faults
1	MFR_PROTECT_ALL_SHUTDOWN	Enable all rails to shut down if a protection occurs. 1b'0: Disable all rails to shut down if a protection occurs 1b'1: Enable all rails to shut down if a protection occurs
0	MFR_PROTECT_ALL_DIS	1'b0: Enable all protections 1'b1: If bit[0] = 1, bit[2] = 1, bit[3] = 1, and bit[4] = 0, disable all protections

FREQUENCY_SWITCH_R1 (33h)

The FREQUENCY_SWITCH command on Page 0 sets the switching frequency for rail 1. The switching frequency ranges between 200kHz and 5.11MHz, with 10kHz per step.

Command	FREQUENCY_SWITCH_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	FREQUENCY_SWITCH_R1	Sets the switching frequency in direct format. 10kHz/LSB.

MFR_OSR_SET_R1 (34h)

The MFR_OSR_SET command on Page 0 sets the overshoot reduction (OSR) parameters. It is for rail 1 only.

Command	MFR_OSR_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	DBG_WD	Fixed to 1.
14	RESERVED	Fixed to 0.
13	MFR_OSR_EN_R1	Enables the overshoot reduction function. This function can reduce the V_{OUT} overshoot at the load release. 1'b0: Disable the overshoot reduction function 1'b1: Enable the overshoot reduction function
12:7	MFR_OSR_FILTER_R1	Sets the minimum OSR duration time. 5ns/LSB.
6:0	MFR_OSR_ BLANKTIME_R1	Sets the blanking time between two effective OSR events. 10ns/LSB.

VIN_ON (35h)

The VIN_ON command sets the V_{IN} under-voltage lockout (UVLO) rising threshold.

Command	VIN_ON															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VIN_ON	Sets the V_{IN} UVLO rising threshold. 31.25mV/LSB.

VIN_OFF (36h)

The VIN_OFF command sets the V_{IN} under-voltage lockout (UVLO) falling threshold.

Command	VIN_OFF															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VIN_OFF	Set the V_{IN} UVLO falling threshold. 31.25mV/LSB.

MFR_SLOPE_SW_INI_R1 (37h)

The MFR_SLOPE_SW_INI command on Page 0 sets the rail 1 soft start initial ramp.

Command	MFR_SLOPE_SW_INI_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	MFR_VOUT_ FINE_TUNE_R1	Sets the V_{OUT} fine-tune value and the trim value per step. Bit[12] is the sign bit. 0.64mV/LSB when V_{DIFF} gain = 1 0.96mV/LSB when V_{DIFF} gain = 1/2
6:0	MFR_SLOPE_SW_ INI_R1	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_DCM_R1 (38h)

The MFR_SLOPE_SR_DCM_R1 command on Page 0 sets the rail 1 slope compensation slew rate in 1-phase DCM. Slope compensation provides enough noise immunity for PWM generation, and stabilizes the PWM switches on the MP2926. The slope compensation is generated by a PMBus-configurable current source and a PMBus-configurable capacitor. The MP2926 provides a slope voltage command for any phase count operation.

Command	MFR_SLOPE_SR_DCM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_1P_R1 (39h)

The MFR_SLOPE_SR_1P command on Page 0 provides 2 bytes to program the slope compensation for 1-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_1P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_2P_R1 (3Ah)

The MFR_SLOPE_SR_2P command on Page 0 provides 2 bytes to program the slope compensation for 2-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_2P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation. 0.25μA/LSB.

MFR_RESERVED (3Bh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (3Ch)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (3Dh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_VRHOT_SET_R1 (3Eh)

The MFR_VRHOT_SET_R1 command on Page 0 sets the parameters for VR_HOT. It is for rail 1 only.

Command	MFR_VRHOT_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	MFR_VRHOT_MODE	Fixed to 1.
8	MFR_VRHOT_EN_R1	Enable bit for VR_HOT. 1'b0: Disable VR_HOT 1'b1: Enable VR_HOT
7:0	MFR_VRHOT_LIMIT_R1	Sets the VR over-temperature alert threshold. If the temperature sensed via the TSENS1 pin exceeds this threshold, OCP_L from the GPIO pins asserts to alert the system. 1°C/LSB

MFR_RESERVED (3Fh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

VOUT_OV_FAULT_LIMIT_R1 (40h)

The VOUT_OV_FAULT_LIMIT command on Page 0 sets the V_{OUT} OVP threshold.

Command	VOUT_OV_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	OVP_VID_SET_R1	Sets the over-voltage protection (OVP) VID threshold. 3'b001: V_{REF} + 200mV 3'b010: V_{REF} + 325mV 3'b100: V_{REF} + 450mV Other commands are invalid
7:0	OVP_ABS_SET_R1	Sets an absolute over-voltage protection (OVP) threshold. If V_{OUT} exceeds this value, a protection occurs. 10mV/LSB.

VOUT_OV_FAULT_RESPONSE_R1 (41h)

The VOUT_OV_FAULT_RESPONSE command sets the protection mode and delay time if a V_{OUT} over-voltage (OV) fault occurs.

Command	VOUT_OV_FAULT_RESPONSE_R1															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OVP_ABS_EN_R1	1'b0: Disabled 1'b1: Enabled
7:6	MFR_OVP_VID_MODE_R1	Sets the over-voltage (OV) fault response. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	MFR_OVP_VID_DELAYTIME_R1	Sets the OVP_VID blanking time. If an OVP_VID condition occurs for longer than the OVP_VID blanking time, an OVP_VID fault occurs. 100ns/LSB.

VOUT_MAX_ALERT_R1 (42h)

The VOUT_MAX_ALERT_R1 command on Page 0 sets the V_{OUT} over-voltage OV warning threshold, or returns the V_{OUT} peak value for rail 1. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	VOUT_MAX_ALERT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	VOUT_MAX_ALERT_R1	If GPIO_ACTIVE (68h) bit[13] is set to 0, this command sets the V_{OUT} over-voltage (OV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, this command returns the maximum peak value of V_{OUT}; it can be written with a lower value. If a higher V_{OUT} is detected, this register is overwritten. To start a new recording, write 0x0000 to reset this bit. 1.56mV/LSB when V_{DIFF} gain = 1 3.12mV/LSB when V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 0) bit[10].

VOUT_MIN_ALERT_R1 (43h)

The VOUT_MIN_ALERT_R1 command on Page 0 sets the V_{OUT} under-voltage (UV) warn threshold or returns the V_{OUT} minimum value for rail 1. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	VOUT_MIN_ALERT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	VOUT_MIN_ALERT_R1	If GPIO_ACTIVE (68h) bit[13] is set to 0, this command sets the V_{OUT} under-voltage (UV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, this command returns the minimum value of V_{OUT}; it can be written with a higher value. If a lower V_{OUT} is detected, this register is overwritten. To start a new recording, write 0x03FF to reset this bit. 1.56mV/LSB when V_{DIFF} gain = 1 3.12mV/LSB when V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 1) bit[10].

VOUT_UV_FAULT_LIMIT_R1 (44h)

The VOUT_UV_FAULT_LIMIT command sets the V_{OUT} under-voltage (UV) fault threshold.

Command	VOUT_UV_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	UVP_VID_SET_R1	Sets the threshold for under-voltage protection (UVP). 3'b000: V_{REF} - 425mV 3'b001: V_{REF} - 375 mV 3'b010: V_{REF} - 325mV 3'b011: V_{REF} - 275mV 3'b100: V_{REF} - 225mV 3'b101: V_{REF} - 175mV 3'b110: V_{REF} -1 25mV 3'b111: V_{REF} - 75mV
7:0	RESERVED	Fixed to 0.

VOUT_UV_FAULT_RESPONSE_R1 (45h)

The VOUT_UV_FAULT_RESPONSE on Page 0 sets the under-voltage (UV) fault response.

Command	VOUT_UV_FAULT_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_UV_VID_EN_R1	Enable bit for VID under-voltage protection (UVP). 1'b0: Disable VID UVP 1'b1: Enable VID UVP
7:6	MFR_UVP_MODE_R1	Sets the V_{OUT} under-voltage protection (UVP) response. There are four modes available. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	MFR_UVP_ DELAYTIME_R1	Sets the V_{OUT} under-voltage protection (UVP) blanking time. A UVP fault occurs if the sensed V_{DIFF} drops below the UVP threshold for the UVP blanking time. 100ns/LSB.

IOUT_OC_FAULT_LIMIT_R1 (46h)

The IOUT_OC_FAULT_LIMIT command on Page 0 sets the I_{OUT} over-current (OC) fault threshold.

Command	IOUT_OC_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	OCP_SPIKE_SET_R1	Sets the rail 1 OCP_SPIKE_TOTAL current level DAC value. 6.25mV/LSB. OCP_SPIKE_TOTAL = OCP_SPIKE x K_{CS} x G_{IMON} x R_{IMON} / 6.25
7:0	OCP_TDC_SET_R1	Sets the rail 1 OCP_TDC_TOTAL current level. The high 8 MSB of the IMON1 ADC result, IMON1_SENSE [9:0], is compared to this TDC level. 6.25mV/LSB. OCP_TDC_TOTAL = OCP_TDC x K_{CS} x G_{IMON} x R_{IMON} / 6.25

IOUT_OC_FAULT_RESPONSE_R1 (47h)

The IOUT_OC_FAULT_RESPONSE command sets the rail 1 over-current protection (OCP) options and values.

Command	IOUT_OC_FAULT_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	MFR_OCP_MODE_R1	Selects the protection mode for both OCP_TDC and OCP_SPIKE. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
13	MFR_OCP_TDC_EN_R1	Enable bit for over-current protection (OCP_TDC). 1'b0: Disabled 1'b1: Enabled
12:8	MFR_OCPTDC_ ACTION_DELAY_R1	Sets the OCP_TDC fault action time. The time delay is between OCP_L signal assertion and current limiting, hiccup mode entry, or shutdown. 1µs/LSB.
7:0	MFR_OCPTDC_TRIG_ DELAY_R1	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for an OCP_TDC blanking time. 20µs/LSB.

IOUT_OC_SPIKE_RESPONSE_R1 (48h)

The IOUT_OC_SPIKE_RESPONSE command sets the over-current (OC) spike options and values.

Command	IOUT_OC_SPIKE_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	MFR_OCCMP_SEL	Over-current protection (OCP) mode selection. 1'b0: OCP_TDC uses the digital comparator for OCP_TDC 1'b1: OCP_TDC uses the analog comparator for OCP_SPIKE. In this mode, OCP_SPIKE should be disabled
8	MFR_OCP_ SPIKE_EN_R1	Enable bit for over-current protection (OCP_SPIKE). 1'b0: Disabled 1'b1: Enabled
7:4	MFR_OCPSPIKE_ ACTIONDELAY_R1	Sets the OCP_SPIKE fault action delay time. The time is between OCP_L asserts (after exceeding the current threshold relative to $I_{DDSPIKE}$) and current limiting or hiccup mode entry/shutdown. 1µs/LSB.
3:0	MFR_OCPSPIKE_ TRIGDELAY_R1	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for the OCP_SPIKE blanking time. 200ns/LSB.

MFR_OCP_PHASE_LIMIT_R1 (49h)

The MP2926 provides OCP_PHASE protection to limit the per-phase valley current. OCP_PHASE is implemented by monitoring and comparing the cycle-by-cycle sensed current with a current reference. The MFR_OCP_PHASE_LIMIT command on Page 0 sets the rail 1 per-phase valley current limit.

Command	MFR_OCP_PHASE_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	RESERVED	Unused. Fixed to 0.
7:0	OCP_DAC_SET_R1	Sets the per-phase valley current limit DAC value. 5mV/LSB.

IOUT_MAX_ALERT_R1 (4Ah)

The IOUT_MAX_ALERT_R1 command on Page 0 sets the I_{OUT} over-current (OC) warning threshold, or returns the peak value of I_{OUT}. If it for rail 1 only. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	IOUT_MAX_ALERT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	IOUT_MAX_ALERT_R1	If GPIO_ACTIVE (68h) bit[13] is set to 0, this command sets the DAC value of the I_{OUT} over-current (OC) warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, this command returns the peak value of I_{OUT}. In this mode, it can be written with a lower value. If a higher I_{OUT} is detected, this register is overwritten. To start the new recording, write 0x0000 to reset. Convert the read value to the actual output current (in A) with the following equation: $$I_{OUT}(A) = \frac{4Ah[9:0]}{6Ch[9:0]\times 1024} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$$ Where GAIN_SEL is 6Ch bits[11:10].

MFR_FS_LIMIT_12P_R1 (4Bh)

The MFR_FS_LIMIT_12P_R1 command on Page 0 sets the rail 1 FS_LIMIT threshold to 1-phase and 2-phase operation to detect fast load insertion and exit phase-shedding.

Command	MFR_FS_LIMIT_12P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_FS_LIMIT_2P_R1	Sets the exit phase-shedding PWM interval time for 2-phase operation. If the time interval between two phases is shorter than FS_LIMIT_2P, the count adds 1, so that when the count reaches the value set by Page 0, 51h bits[2:0], APS is exited immediately. 5ns/LSB.
7:0	MFR_FS_LIMIT_1P_R1	Sets the PWM1 off-time threshold to exit phase-shedding. If the PWM1 off time (after excluding MIN_OFF_TIME) is shorter than FS_LIMIT_1P, the count adds 1, so that when the count reaches the value set by Page 0, 51h bits[9:7], APS is exited immediately. It is effective for both DCM and CCM. 10ns/LSB.

MFR_RESERVED (4Ch)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_APS_LEVEL_12P_R1 (4Dh)

The MFR_APS_LEVEL_12P command on Page 0 sets the rail 1 automatic phase-shedding (APS) current threshold to 1-phase CCM and 1-phase DCM operation.

Command	MFR_APS_LEVEL_12P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_APS_IIL_1P_CCM_R1	Sets the rail 1 APS current threshold for 1-phase CCM. 1A/LSB.
7:0	MFR_APS_IIL_1P_DCM_R1	Sets the rail 1 APS current threshold for 1-phase DCM. 1A/LSB.

MFR_RESERVED (4Eh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

OT_FAULT_LIMIT_R1 (4Fh)

The OT_FAULT_LIMIT command on Page 0 sets the over-temperature protection (OTP) fault related operation and values.

Command	OT_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	MFR_OTP_MODE	Sets the over-temperature protection (OTP) mode. 1'b0: Latch off 1'b1: Retry
13:8	MFR_OTP_HYS	Sets the temperature hysteresis for the over-temperature protection (OTP) threshold. If the junction temperature on the TSENS pin drops below OTP_LIMIT - OTP_HYS, the PWM initiates a soft start as it would during normal operation. 1°C/LSB.
7:0	MFR_OTP_LIMIT_R1	VR over-temperature protection (OTP) fault limit setting. If the junction temperature on the TSENS1 pin exceeds OTP_LIMIT, the VR shuts off the disabled output. 1°C/LSB.

MFR_CORE_OTP_SET (50h)

The MFR_CORE_OTP_SET command on Page 0 sets the chip over-temperature protection (OTP) fault operations and values.

Command	MFR_CORE_OTP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	MFR_CORE_OTP_RES	Fixed to 0.
14	MFR_CORE_OTP_ MODE	Sets the core over-temperature protection (OTP) mode. 1'b0: Latch off 1'b1: Retry
13:8	MFR_CORE_OTP_HYS	Sets the temperature hysteresis for the over-temperature protection (OTP) threshold. If the junction temperature on the TSENS pin drops below OTP_LIMIT - OTP_HYS, the PWM initiates a soft start as it would during normal operation. 1°C/LSB.
7:0	MFR_CORE_OTP_ LIMIT	Controller over-temperature protection (OTP) fault limit setting. When the junction temperature monitored on the TSENS pin exceeds OTP_LIMIT, the VR shuts off the disabled output. 1°C/LSB.

MFR_FS_DETECT_R1 (51h)

The MFR_FS_DETECT_R1 command sets rail 1 APS timing and behaviors.

Command	MFR_FS_DETECT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables exit phase-shedding according to the PWM1 off time. The PWM minimum off time is excluded from the PWM off time (see Figure 24). 1'b0: Disable PWM1 off time detection to exit APS 1'b1: Enable PWM1 off time detection to exit APS
10	FS_EXIT_APS_EN_NP	Enable exit phase-shedding according to the multi-phase PWM interval time between consecutive phases. The time threshold is set by registers 4Bh on Page 0. The PWM blanking time is excluded from the PWM interval time (see Figure 25). 1'b0: Disable multi-phase PWM interval time detection to exit APS 1'b1: Enable multi-phase PWM interval time detection to exit APS
9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count for the PWM1 off time condition to exit phase-shedding. If the PWM off time conditions reach the counting threshold, the controller exits APS immediately.
6:3	RETURN_APS_DELAY	Sets the minimum full-phase runtime after exiting APS due to a FS_limit event. 20µs/LSB.
2:0	FS_EXIT_APS_CNT_NP	Sets the continuous count of multi-phase PWM interval time to exit phase-shedding. Once the PWM interval condition meets the counting threshold, the controller exits APS immediately.

Figure 24: FS_LIMIT_1P Condition in Single-Phase Operation

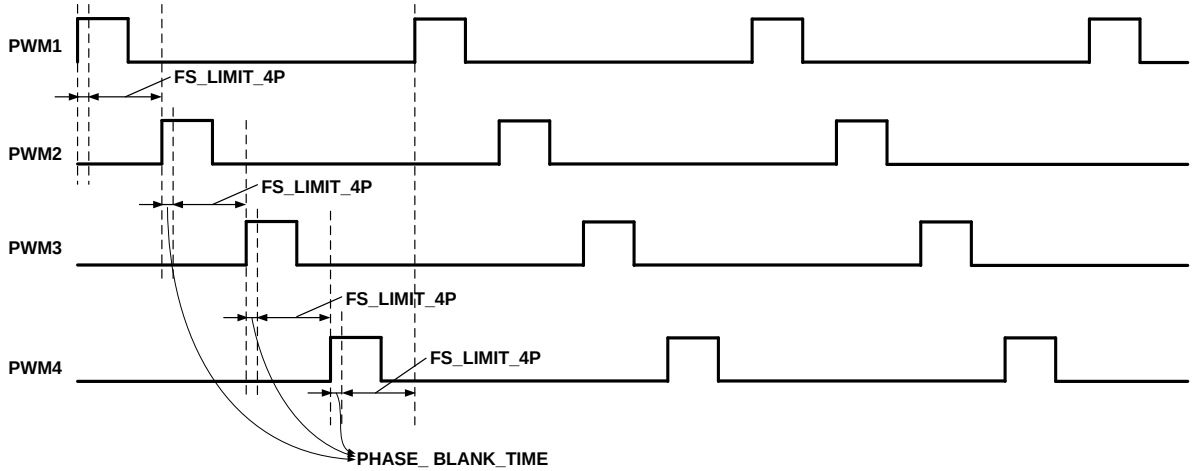


Figure 25: FS_LIMIT_NP Condition in N-Phase Operation (N = 4)

MFR_APS_CTRL_R1 (52h)

The MFR_APS_CTRL_R1 command on Page 0 sets rail 1 APS timing and behaviors.

Command	MFR_APS_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:12	MFR_ADP_OC_NPS _EXIT_CNT_R1	Sets the period delay count from OCP_PHASE being triggered to APS exit. 100ns/LSB.
11	MFR_ADP_OC_NPS _EXIT_EN_R1	Enable OCP_PHASE protection to exit APS at any power state. 1'b0: Disable the OCP_PHASE signal triggering any phase to full-phase operation 1'b1: Enable the OCP_PHASE signal triggering any phase to full-phase operation
10	MFR_ADP_PFM _EXIT_EN_R1	Enable the rail 1 frequency increasing conditions to exit APS. 1'b0: Disable 1'b1: Enable
9	MFR_ADP_OC_ 1PS_EXIT_EN_R1	Enable OCP_PHASE protection exiting APS in 1-phase DCM/CCM. 1'b0: Disable the OCP per-phase signal trigger 1-PH DCM/CCM to full-phase operation 1'b1: Enable the OCP per-phase signal trigger 1-PH DCM/CCM to full-phase operation
8	MFR_ADP_UV _EXIT_EN_R1	Sets rail 1 to enter full-phase operation if V_{FB} < VID - 25mV. 1'b0: Disable 1'b1: Enable
7:2	MFR_PS_ ENTER_TIME_R1	Sets the phase-shedding delay time. When the reported load current is consecutively below the APS threshold for APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE, the controller enters APS mode and automatically sheds the phase count according to the load current.
1	MFR_PHASHED_ EXIT_MOD_R1	Sets the phase-dropping mode during phase-shedding. Phase-shedding may be due to APS. 1'b0: Drop phase count to target immediately 1'b1: Shed phases one by one with a configured delay time. The delay time is set with 54h bits[10:7].
0	MFR_AUTO_PS_EN_R1	Enables rail 1 APS mode. 1'b0: Disable rail 1 APS mode 1'b1: Enable rail 1 APS mode

MFR_APS_CTRL2_R1 (53h)

The MFR_APS_CTRL2_R1 command on Page 0 sets the rail 1 APS timing and behaviors.

Command	MFR_APS_CTRL2_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

13:9	APS_COMP_CNT	The MP2926 provides positive compensation on VREF during phase-shedding to reduce undershoot. Phase-shedding may be due to APS. The V_{REF} compensation is implanted by adding a PMBus-programmable positive voltage on COMP of the DC loop. After phase-shedding begins, the voltage returns to 0 step by step with a time interval. APS_COMP_CNT sets this time interval between each step. 50ns/LSB.
8	DECAY_COMP_EN	Enable V_{REF} compensation when exiting decay mode. The MP2926 provides V_{REF} compensation when exiting decay mode. The compensation voltage level and slew rate is the same value with APS compensation. 1'b0: Disable V_{REF} compensation when exiting decay mode 1'b1: Enable V_{REF} compensation when exiting decay mode
7:4	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce undershoot. The compensation is added to V_{REF} when phase-shedding begins. 1.37mV/LSB.
3:0	MFR_APS_HYS	Sets the current hysteresis between phase-shedding and adding. It prevents back-and-forth phase-shedding when APS is enabled. 1A/LSB.

MFR_APS_CTRL3_R1 (54h)

The MFR_APS_CTRL3_R1 command on Page 0 sets the rail 1 APS timing and behaviors.

Command	MFR_APS_CTRL3_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	**Bit Name**	**Description**
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:7	MFR_PS_INTERVAL_R1	Sets the phase-by-phase dropping time intervals. It is only effective when bit[1] of 52h is set to 1. 2.5μs/LSB.
6:010:7	MFR_PRD_EXIT_APS_ TIME_R1	Sets the period condition for DC loop and current balance loop holding. If the absolute error between the setting switching period and the real switching period $\|t_S - t_{SET}\|$ exceeds MFR_PRD_EXIT_APS_TIME x 80ns, the device holds the DC loop and current balance loop for a given time. 80ns/LSB.Sets the phase-by-phase dropping time intervals. It is only effective when bit[1] of 52h is set to 1. 2.5μs/LSB.

VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command on Page 0 sets the V_{IN} over-voltage protection (OVP) threshold. This register is in linear format. If the sensed input voltage exceeds the VIN_OV fault limit, the VR shuts down immediately.

Command	VIN_OV_FAULT_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	**Bit Name**	**Description**
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VIN_OV_FAULT_LIMIT	Sets the V_{IN} over-voltage protection (OVP) threshold. 31.25mV/LSB.

MFR_FSCB_LOOP_CTRL_R1 (56h)

The MFR_FSCB_LOOP_CTRL command on Page 0 sets the rail 1 switching frequency and current balance loop.

Command	MFR_FSCB_LOOP_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	FS_LOOP_EN_R1	Switching frequency loop enable bit. The frequency loop keeps the switching frequency flat and equals the set value at different input voltages and load currents. This bit is active for both rails. 1'b0: Disable the frequency loop 1'b1: Enable the frequency loop
14	TRANS_HOLD_FS_EN_R1	Holds frequency loop regulation if a load transient event is detected (e.g. V_{FB} exceeds the V_{FB}+ window or V_{FB}- window). 1'b0: Disable holding the frequency loop if a load transient event is detected 1'b1: Enable holding the frequency loop if a load transient event is detected
13	PS_HOLD_FS_EN_R1	Holds frequency loop regulation when the phase count changes. 1'b0: Disable holding the frequency loop if the phase count changes 1'b1: Enable holding frequency loop regulation if the phase count changes
12	DVID_HOLD_FS_EN_R1	Holds frequency loop regulation when DVID occurs. 1'b0: Disable holding the frequency loop if DVID occurs 1'b1: Enable holding the frequency loop regulation if DVID occurs
11:8	MFR_FS_LOOP_CNT_R1	Sets the minimum hold time for the frequency loop if any load transient event, PWM switching period change, phase count change, or DVID event is detected. Once this occurs, the corresponding enable bit is set. 100μs/LSB.
7	MFR_CB_EN_R1	Enables the current balance loop. 1'b1: Enable the current balance loop 1'b0: Disable the current balance loop
6	PRD_HOLD_CB_EN_R1	Holds the current balance loop if the PWM period meets the PWM switching period condition set by PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disable holding the current balance loop if the PWM switching period condition is met 1'b1: Hold the current balance loop if the PWM switching period condition is met
5	PS_HOLD_CB_EN_R1	Holds the current balance loop if the phase number changes. 1'b0: Disable holding the current balance loop if the phase count changes 1'b1: Enable holding the current balance loop if the phase count changes
4	DVID_HOLD_CB_EN_R1	Holds the current balance loop if DVID occurs. 1'b0: Disable holding the current balance loop if DVID occurs 1'b1: Enable holding the current balance loop if DVID occurs
3:0	MFR_DYM_FLT_CNT_R1	Sets the current balance loop hold time. If any load transient event, PWM switching period change, phase count change, or DVID event is detected, then the corresponding enable bit is set and the current balance loop stops regulating for a time set by the CB_LOOP_THOLD command. 100μs/LSB.

MFR_VOUT_LOOP_CTRL_R1 (57h)

The MFR_VOUT_LOOP_CTRL command on Page 0 sets the rail 1 V_{OUT} loop parameters.

Command	MFR_VOUT_LOOP_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	MFR_VDIFF_GAIN_SEL_R1	Selects the V_{DIFF} gain. When the output voltage exceeds 1.55V, which is the maximum sampling range of the internal ADC, select x1/2 gain. It can enlarge V_{OUT} to 3V. 1'b0: 1x 1'b1: 1/2x
9	MFR_DC_REF_SEL_R1	Sets the output voltage DC loop sensing point. 1'b 0: V_{FB} 1'b 1: V_{DIFF}
8	MFR_VCAL_PS2_EN_R1	Enables DC loop calibration during DCM operation. 1'b0: Disabled 1'b1: Enabled
7	MFR_VCAL_EN_R1	Enables DC loop calibration both during DCM and CCM operation. 1'b0: Disabled 1'b1: Enabled
6	PRD_HOLD_DC_EN_R1	Holds the DC loop when the PWM time interval meets the PWM switching period condition set by PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disable holding the DC loop if the PWM switching period condition is met 1'b1: Enable holding the DC loop if the PWM switching period condition is met
5	PS_HOLD_DC_EN_R1	Holds the DC loop if the phase count changes. 1'b0: Disable 1'b1: Enable
4	TRANS_HOLD_DC_EN_R1	Holds DC loop regulation if a load transient event is detected (e.g. V_{FB} exceeds V_{FB}+ window or V_{FB}- window). 1'b0: Disable holding the DC loop if it meets the V_{FB}+/- window condition 1'b1: Enable holding the DC loop if it meets the V_{FB}+/- window condition
3:0	MFR_DC_LOOP_CNT_R1	Sets the DC loop minimum hold time in direct format. 200μs/LSB with a + 100μs offset.

JOUT_SHORT_PK_R1 (58h)

The JOUT_SHORT_PK command returns the peak value of J_{OUT} for every short-term period.

Command	JOUT_SHORT_PK_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	JOUT_SHORT_PK_R1	Always returns the peak value of J_{OUT} in every short-term period when J_{OUT} is enabled and GPIO_ACTIVE (68h) bit[13] is set to 1. If J_{OUT} is disabled or GPIO_ACTIVE (68h) bit[13] is set to 0, it returns the preset value.

JOUT_LONG_PK_R1 (59h)

The JOUT_LONG_PK command returns the peak value of J_{OUT} for every long-term period.

Command	JOUT_LONG_PK_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	JOUT_LONG_PK_R1	Always returns the peak value of J_{OUT} in every long-term period when J_{OUT} is enabled and GPIO_ACTIVE (68h) bit[13] is set to 1. If J_{OUT} is disabled or GPIO_ACTIVE (68h) bit[13] is set to 0, it returns the preset value.

MFR_SLOPE_CNT_1P_R1 (5Ah)

The MFR_SLOPE_CNT_1P_R1 command on Page 0 sets the rail 1 slope voltage clamp time for 1-phase operation.

Command	MFR_SLOPE_CNT_1P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	MFR_SLOPE_CNT_1P_R1	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_2P_R1 (5Bh)

The MFR_SLOPE_CNT_2P_R1 command on Page 0 sets the rail 1 slope voltage clamp time for 2-phase operation.

Command	MFR_SLOPE_CNT_2P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	RESERVED	Fixed to 0.
7:0	MFR_SLOPE_CNT_2P_R1	Sets the slope voltage clamp time. 5ns/LSB.

MFR_RESERVED (5Ch)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (5Dh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_SLOPE_CNT_DCM_PLUS_R1 (5Eh)

The MFR_SLOPE_CNT_DCM_PLUS command on Page 0 sets the rail 1 slope voltage clamp time for DCM operation.

Command	MFR_SLOPE_CNT_DCM_PLUS_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Fixed to 0.
11:10	MFR_SLOPE_CNT_2P_PLUS_R1	The MSB of the 2-phase slope count.
9:0	MFR_SLOPE_CNT_DCM_R1	Sets the slope voltage clamp time. 5ns/LSB.

MFR_PG_DELAY_R1 (5Fh)

The MFR_PG_DELAY_R1 command sets the delay time for power good on and off.

Command	MFR_PG_DELAY_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:10	MFR_PGOFF_DELAY_R1	Sets the power good off delay time. 5µs/LSB.
9:0	MFR_PGON_DELAY_R1	Sets the power good on delay time. 5µs/LSB.

TON_DELAY_R1 (60h)

The TON_DELAY_R1 command on Page 0 sets the delay time from when system initialization ends to when rail 1 V_{REF} starts to boot up.

Command	TON_DELAY_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	TON_DELAY_R1	Sets the delay time from system initialization ending to V_{REF} booting up. 100µs/LSB.

TON_RISE_R1 (61h)

The TON_RISE_R1 command on Page 0 sets the rail 1 reference voltage boot-up slew rate.

Command	TON_RISE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TON_RISE_R1	Sets the rail 1 boot-up slew rate in PMBus and PVID mode. 0.01mV/µs/LSB or 1mV/µs/LSB. Resolution is determined by MFR_VR_CONFIG3 (C3h) bit[15].

MFR_PWM_MIN_TIME1_R1 (62h)

The MFR_PWM_MIN_TIME1 command on Page 0 sets the minimum pulse width when PWM is high, low, or in tri-state. It is for rail 1 only.

Command	MFR_PWM_MIN_TIME1_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	MFR_MIN_LOW_TIME_R1	Sets the minimum PWM low time. 10ns/LSB with a -5ns offset. The minimum PWM low time can be calculated with the following equation: (PWM_MIN_LOW_TIME x 10 - 5) ns
8:6	MFR_MINON_TIME_R1	Sets the minimum PWM high time. 10ns/LSB with a -5ns offset. The minimum PWM high time can be calculated with the following equation: (PWM_MIN_HIGH_TIME x 10 - 5) ns
5:0	MFR_MIN_HIZ_TIME_R1	Sets the minimum PWM tri-state time. 10ns/LSB with a -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: (PWM_MIN_TRI_TIME x 10 - 5) ns

MFR_PWM_MIN_TIME2_R1 (63h)

The MFR_PWM_MIN_TIME2_R1 command on Page 0 sets the PWM minimum off time and PWM on pulse width when under-current protection (UCP) is triggered. It is for rail 1 only.

Command	MFR_PWM_MIN_TIME2_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	TON_LIMIT_TO_VCAL	On the MP2926, the DC loop can be held if the PWM period meets the condition set in MFR_FS (33h, Page 0). If the calculated PWM on time is shorter than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	MFR_ZCD_EN_R1	Enable bit for rail 1 zero-current detection (ZCD). 1'b0: Disable ZCD 1'b1: Enable ZCD
8:5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4:0	MFR_MINOFF_TIME_R1	Sets the PWM minimum off time. 20ns/LSB with a 15ns offset. The PWM minimum off time can be calculated with the following equation: (PWM_MIN_OFF_TIME x 20 + 15) ns

TOFF_DELAY_R1 (64h)

The TOFF_DELAY_R1 command on Page 0 sets the rail 1 delay time from when EN goes low to V_{REF} starting the shutdown on rail 1.

Command	TOFF_DELAY_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	TOFF_DELAY_R1	Sets the delay time from EN going low to V_{REF} shutdown. 100µs/LSB.

TOFF_FALL_R1 (65h)

The TOFF_FALL_R1 command on Page 0 sets the reference voltage transition down slew rate after receiving an OPERATION command for a soft-off on rail 1.

Command	TOFF_FALL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TOFF_FALL_R1	Sets the rail 1 OPERATION command soft-off slew rate in PMBus and PVID mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h) bit[15].

GPIO_SEL_GROUP1 (66h)

The GPIO_SEL_GROUP1 command on Page 0 selects different signals from the multiplexor (mux) inputs of the PGOOD pin.

Command	GPIO_SEL_GROUP1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	RESERVED	Fixed to 0.
14:12	GPIO_PGOOD_SEL	3’b000: PGOOD pin is selected to be AND operation of PG1, PG2, and PG3 3’b001: PGOOD pin is selected to be AND operation of PG2 and PG3 3’b010: PGOOD pin is selected to be AND operation of PG1 and PG3 3’b011: PGOOD pin is selected to be PG3 3’b100: PGOOD pin is selected to be AND operation of PG1 and PG2 3’b101: PGOOD pin is selected to be PG2 3’b110: PGOOD pin is selected to be PG1 3’b111: PGOOD pin is selected to be open-drain high
11:9	RESERVED	Fixed to 0.
8:3	RESERVED	Fixed to 0.
2	GPIO4_HIGH_LOW	Selects a high or low output for GPIO4. 1’b0: Low 1’b1: High Select high when using GPIO4 as an input, and set the mode to open drain (Page 0, 68h[10] = 1).
1	GPIO3_HIGH_LOW	Selects a high or low output for GPIO3. 1’b0: Low 1’b1: High Select high when using GPIO4 as an input, and set the mode to open drain (Page 0, 68h[10] = 1).

0	GPIO2_HIGH_LOW	Selects a high or low output for GPIO2. 1’b0: Low 1’b1: High Select high when using GPIO4 as an input, and set the mode to open drain (Page 0, 68h[10] = 1).

MFR_RESERVED (67h)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

GPIO_MODE (68h)

The GPIO_MODE command on Page 0 sets the GPIO pin output mode.

Command	GPIO_MODE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	GPIO_STB	1’b0: Digital logic output = 0 1’b1: Digital logic output = 1
13	STB_TRI_STATE	1’b0: Tri-state 1’b1: Not tri-state
12	GPIO2_MODE	Selects the GPIO2 mode. Select open drain when using GPIO2 as the input. 1’b0: Push-pull 1’b1: Open drain
11	GPIO3_MODE	Selects the GPIO3 mode. Select open drain when using GPIO3 as the input. 1’b0: Push-pull 1’b1: Open drain
10	GPIO4_MODE	Selects the GPIO4 mode. Select open drain when using GPIO4 as the input. 1’b0: Push-pull 1’b1: Open drain
9	PWM5_TRI_STATE	Selects the PWM5 pin output mode. 1’b0: Push-pull 1’b1: Open drain
8:0	RESERVED	Fixed to 0.

MFR_TEMP_CAL_R1 (69h)

The MFR_TEMP_CAL command on Page 0 sets the TSENS1 pin temperature-sense gain and offset.

Command	MFR_TEMP_CAL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_TEMP_GAIN_R1	Sets the temperature-sense gain to transfer the voltage on the TSENS1 pin to the direct temperature in degrees.
7:0	MFR_TEMP_OFFSET_R1	Sets the temperature-sense offset to convert the voltage on the TSENS1 pin to the direct temperature in degrees. 1°C/LSB. Bit[7] is the sign bit.

MFR_VOUT_CALC_R1 (6Ah)

The MFR_VOUT_CALC command on Page 0 sets the gain and offset for V_{OUT} calculations.

Command	MFR_VOUT_CALC_R1															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:8	MFR_VOUT_CALC_OFFSET_R1	Adds an offset to V_{OUT} reporting in READ_VOUT (8Bh). This bit is for rail 1 output voltage reporting only. This bit is in two's complement format. Bit[13] is the sign bit. VID_STEP/LSB. When the VID_STEP is 6.25mV, the voltage list below shows the direct value and the real-world value. 6'b00 0000: 0mV 6'b00 0001: +6.25mV 6'b01 1111: +193.75mV 6'b10 0000: -200mV 6'b10 0001: -193.75mV 6'b11 1111: -6.25mV
7:0	MFR_VOUT_CALC_GAIN_R1	Sets the gain from the ADC-sensed VOSEN-VORTN voltage to the PMBus V_{OUT} report in READ_VOUT (8Bh). This bit is for rail 1 output voltage reporting only.

MFR_RESERVED (6Bh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

IOUT_CAL_GAIN_PMBUS_R1 (6Ch)

The IOUT_CAL_GAIN_PMBUS_R1 command on Page 0 sets the gain for PMBus output current reporting. The MP2926 senses the output current by sensing the IMON voltage. The reported output current is returned with PMBus command READ_IOUT (8Ch, Page 0).

Command	IOUT_CAL_GAIN_PMBUS_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:10	GAIN_SEL	Sets the exponent value for the IOUT_CAL_GAIN calculation equation in this command.
9:0	IOUT_CALC_GAIN_R1	Set the current sensing gain for the PMBus report. The sense gain can be calculated with the following equation: $$IOUT\_CAL\_GAIN=\frac{1023}{1.6}\times K_{CS}\times G_{IMON}\times R_{IMON}\times 2^{(6-GAIN\_SEL)}$$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bit[11:10] in this command.

IOUT_CAL_OS_PMBUS_R1 (6Dh)

The IOUT_CAL_OS_PMBUS_R1 command on Page 0 sets the offset for the rail 1 output current PMBus report. The offset is for I_{OUT} over-reporting or under-reporting. The reported output current is returned with PMBus command READ_IOUT (8Ch, Page 0).

Command	IOUT_CAL_OS_PMBUS_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:6	IOUT_CAL_PH_OFS_R1	Adds offset according the phase number. A larger N results in a larger offset. Bit[12] is sign bit.
5:0	IOUT_CALC_OFFSET_R1	Adds a current report offset to READ_IOUT (8Ch).

MFR_IMON_SET_R1 (6Eh)

The MFR_IMON_SET command on Page 0 sets configurations for the internal IMON sense in PMBus mode. It is for rail 1 only.

Command	MFR_IMON_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:13	MFR_IMON_RES_SET_R1	Sets the IMON resistor for rail 1. 3'b 000: 2.5kΩ 3'b 001:5kΩ 3'b 010:10kΩ 3'b 011: 40kΩ 3'b1xx: Not connected
12	MFR_IMON_GAIN_SET_R1	1'b0: The IMON1 current mirror gain is 1/8 1'b1: The IMON1 current mirror gain is 1/16
11	RESERVED	Fixed to 0.
10:0	MFR_TRIM_IMON_DIGI_GAIN_R1	Sets the digital calculation gain for I_{OUT} reporting. The gain is multiplied by the IMON ADC-sensed value, and forms the final IMON digital-sense value. The IMON digital-sense value is used for PMBus output current reporting. The final IMON-sensed value can be calculated with the following equation: $IOUT\_PMBUS\_REPORT=1023\times\frac{I_{OUT}\times K_{CS}\times G_{IMON}\times R_{IMON}}{1.6}\times\frac{TRIM\_DIGI\_GAIN}{1024}\times\frac{2^{(6\text{-}GAIN\_SEL)}}{GAIN}$ Where I_{OUT} is the output current (in A), K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the IMON resistor (in Ω), and TRIM_DIGI_GAIN is a decimal value.

IOUT_MIN_ALERT_R1 (6Fh)

The IOUT_MIN_ALERT_R1 command on Page 0 returns the minimum value of I_{OUT} or the preset value. It is for rail 1 only. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	IOUT_MIN_ALERT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IOUT_MIN_ALERT_R1	If GPIO_ACTIVE (68h) bit[13] set to 0, 6Fh sets the DAC value of the I_{OUT} over-current (OC) warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, 6Fh returns the minimum I_{OUT} value. In this mode, it also can be written with a higher value. If a higher I_{OUT} is detected, this register is overwritten. To start a new recording, write 0x03FF to reset this bit. Convert the read value to the actual output current (in A) with the following equation: $I_{OUT}(A)=\frac{6Fh[9:0]}{6Ch[9:0]\times 1024}\times 6Eh[10:0]\times 2^{(6\text{-}GAIN\_SEL)}$ Where GAIN_SEL is 6Ch bits[11:10].

MFR_PHASE_CFG (70h)

The MFR_PHASE_CFG command on Page 0 sets the phase configuration.

Command	MFR_PHASE_CFG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:7	PHASE_NUM_CFG_R3	Sets the phase number for rail 3 .
6:4	PHASE_NUM_CFG_R2	Sets the phase number for rail 2.
3:0	PHASE_NUM_CFG_R1	Sets the phase number for rail 1.

MFR_PVID01_R1 (71h)

The MFR_PVID01_R1 command on Page 0 programs the rail 1 PVID voltage in PVID override mode.

Command	MFR_PVID01_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID1_R1	Sets the rail 1 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3’b001. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID0_R1	Sets the rail 1 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3’b000. It is in VID format. VID_STEP/LSB.

MFR_PVID23_R1 (72h)

The MFR_PVID23_R1 command on Page 0 programs the rail 1 PVID voltage in PVID override mode.

Command	MFR_PVID23_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID3_R1	Sets the rail 1 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3’b011. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID2_R1	Sets the rail 1 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3’b010. It is in VID format. VID_STEP/LSB.

MFR_PVID45_R1 (73h)

The MFR_PVID45_R1 command on Page 0 programs the rail 1 PVID voltage in PVID override mode.

Command	MFR_PVID45_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID5_R1	Set the rail1 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3’b101. It is in VID format. VID_STEP/LSB.

7:0	MFR_PVID4_R1	Set the rail1 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b100. It is in VID format. VID_STEP/LSB.

MFR_PVID67_R1 (74h)

The MFR_PVID67_R1 command on Page 0 programs the rail 1 PVID voltage in PVID override mode.

Command	MFR_PVID67_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID7_R1	Sets the rail 1 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b111. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID6_R1	Sets the rail 1 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b110. It is in VID format. VID_STEP/LSB.

SAMPLE_INTERVAL_12PH_R1 (75h)

The SAMPLE_INTERVAL_12P_R1 command sets the sample interval for 1-phase and 2-phase operation.

Command	SAMPLE_INTERVAL_12PH_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13:7	SAMPLE_INTERVAL_ 2PH_R1	Sets the 2-phase sample interval. 50ns/LSB.
6:0	SAMPLE_INTERVAL_ 1PH_R1	Sets the 1-phase sample interval. 50ns/LSB.

MFR_RESERVED (76h)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_ADDR_PMBUS (77h)

The MFR_ADDR_PMBUS command on Page 0 sets the PMBus address.

Command	MFR_ADDR_PMBUS															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7	ADDR_CONFIG_MODE	Sets the PMBus address 4LSB setting mode. 1'b0: Set the PMBus 4LSB via the ADDR pin voltage 1'b1: Set the PMBus 4LSB via the register
6:4	ADDR_MSB	Sets the 3MSB of the PMBus address. It ranges from 0 to 7.
3:0	ADDR_LSB	Sets or returns the 4LSB of the PMBus address. When bit[7] = 1'b0, the PMBus address 4LSB is set by the ADDR pin voltage. Bits[3:0] return the PMBus 4LSB address. When bit[7] = 1'b1, the 4LSB of the PMBus is set with bits[3:0].

STATUS_BYTE (78h)

The STATUS_BYTE command returns 1 byte of information with a summary of the most critical status and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								X

Bits	Bit Name	Behavior	Description
7	NVM_BUSY	Live	Reports the live status of the NVM. 1'b0: The NVM is idle. The NVM can write and read with a PMBus command 1'b1: The NVM is busy. The NVM cannot write and read with a PMBus command
6	OFF	Live	Rail 1 output is off. This bit is in live mode. It is asserted if the rail 1 output is off. V_{OUT} turning off can be caused by protections, EN going low, or VID = 0. 1'b0: VOUT1 is on 1'b1: VOUT1 is off
5	VOUT_OV_FAULT	Latch	Rail 1 output voltage over-voltage (OV) fault indicator. This bit is set and latched if rail 1 OVP occurs. The CLEAR_FAULTS (03h) command can reset this bit. (Absolute or VID.) 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	Rail 1 output current over-current (OC) fault indicator. This bit is set and latched if rail 1 OCP occurs. The CLEAR_FAULTS (03h) command can reset this bit. (OCP_TDC and OCP_SPIKE.) 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
3	VIN_UV_FAULT	Latch	Input voltage under-voltage (UV) fault indicator. This bit is set and latched if an input voltage UV fault happens. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred

2	TEMPERATURE	Latch	Over-temperature (OT) fault and warning indicator. This bit is set and latched if TSENS1 senses OTP, or a warning occurs. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Latch	PMBus communication fault indicator. If a PMBus communication fault occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	TSENS3_DIGI_FAULT	Latch	TSENS3 digital sense fault indicator. If TSENS3 senses voltage above or below the configurable level set by MFR_TSENS3_SET (36h, Page 1) bits[13:8], a TSENS3 fault occurs, and this bit is set and latched. The TSENS3 sense fault direction is determined by MFR_TSEN3_SET (36h, Page 1), bit[1]. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No TSENS3 digital-sense fault has occurred 1'b1: TSENS3 digital-sense fault has occurred

STATUS_WORD (79h)

The STATUS_WORD (79h) command on Page 0 returns 2 bytes of information with a summary of the device fault or warning condition. The higher byte gives more detailed information of the fault conditions. The lower byte shares the information with the STATUS_BYTE (78h) register.

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function						X	X		STATUS_BYTE(78H)							

Bits	Bit Name	Behavior	Description
15	VOUT	Live	Rail 1 V_{OUT} fault and warning indicator. If an output over-voltage (OV) or under-voltage (UV) protection or warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} fault or warning has occurred 1'b1: A V_{OUT} fault/warning has occurred
14	IOUT	Live	Rail 1 I_{OUT} fault and warning indicator. If an output current fault or warning occurs, or an output power warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No I_{OUT} fault and warning has occurred 1'b1: An I_{OUT} fault or warning has occurred
13	INPUT	Latch	Input voltage and current fault/warning indicator. If any protection or warning of the input voltage or input current occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No input fault and warning has occurred 1'b1: An input fault or warning has occurred

12	TSENS1	Latch	TSENS1 fault indicator. If the TSENS1 sense voltage exceeds 2.2V, a TSENS1 fault occurs, and this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No TSENS1 fault has occurred 1'b1: A TSENS1 fault has occurred
11	PG_NOT_ACTIVE	Live	1'b0: PG is active 1'b1: PG is not active
10:9	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
8	WATCH_DOG_OVF	Latch	Watchdog for the monitor block timer overflow indicator. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset. Meanwhile, this bit is set. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: Watchdog timer has not overflowed 1'b1: Watchdog timer has overflowed

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 0 returns 1 byte of information with the detailed V_{OUT} fault and warning status on rail 1.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function						X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Rail 1 V_{OUT} over-voltage (OV) fault indicator. If output OVP occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
6	VOUT_OV_WARNING	Live	Rail 1 V_{OUT} over-voltage (OV) warning indicator. If output OVP occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: no V_{OUT} OV warning has occurred 1'b1: A V_{OUT} OV warning has occurred
5	VOUT_UV_WARNING	Live	Rail 1 output voltage under-voltage (UV) warning indicator. If rail 1 UVP occurs, this bit is set. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} UV warning has occurred 1'b1: A V_{OUT} UV warning has occurred
4	VOUT_UV_FAULT	Latch	Rail 1 output voltage under-voltage (UV) fault indicator. If rail 1 UVP occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred

3	VOUT_MAX_MIN_ WARNING	Latch	Rail 1 V_{OUT} reaches VOUT_MAX or VOUT_MIN indicator. If the VID value exceeds the value set in VOUT_MAX (24h, Page 0) or VOUT_MIN (2Bh, Page 0), this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID has exceeded VOUT_MAX or is below VOUT_MIN
2	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
1	LINE_FLOAT	Latch	Rail 1 line float protection indicator. Once a line float fault is detected, the device shuts down the associated rail and sets the LINE_FLOAT bit. It is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No line float fault has occurred 1'b1: A line float fault has occurred
0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 0 returns 1 byte of information with the detailed I_{OUT} fault and warning status for rail 1.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function				X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Rail 1 output over-current (OC) fault indicator. If output OCP occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. (OCP_TDC and OCP_SPIKE.) 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6	TDC_OCP_UV_FAULT	Latch	Rail 1 output over-current (OC) and under-voltage (UV) dual fault indicator. If output OC occurs and the UV comparator sets simultaneously, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No output OC and UV fault has occurred 1'b1: Output OC has occurred and the UV comparator is set
5:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_INPUT (7Ch)

The STATUS_INPUT command returns 1 byte of information with detailed input fault and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	VIN_OVP	Latch	Input voltage over-voltage (OV) fault indicator. If the sensed input voltage exceeds the V_{IN} OV fault limit, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command on Page 0 returns 1 byte of information with temperature-related fault and warning conditions.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Over-temperature (OT) fault indicator. If the sensed temperature via the TSENS1 pin exceeds the OT fault limit set by OT_FAULT_LIMIT (4F, Page 0), this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
6	VRHOT	Live	VRHOT indicator. If the sensed temperature via the TSENS1 pin exceeds the over-temperature (OT) warning limit set by MFR_VRHOT_SET (3Eh, Page 0), this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No VRHOT fault has occurred 1'b1: A VRHOT fault has occurred
5:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_CML (7Eh)

The STATUS_CML command on Page 0 returns 1 byte of information with PMBus communication faults.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function					X			

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	Invalid PMBus command indicator. This bit is set and latched if the MP2926 receives an unsupported command code. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received

6	INVALID_DATA	Latch	Invalid PMBus data indicator. This bit is set and latched if the MP2926 receives unsupported data. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received
5	PEC_ERROR	Latch	PMBus PEC fault indicator. The PMBus interface supports the use of the packet error checking (PEC) byte defined in the SMBus standard. The PEC byte is transmitted by the MP2926 during a read transaction, or sent to the MP2926 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed, and a PEC_FAULT is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4	NVM_CRC_ERROR	Latch	CRC fault indicator. In the process of storing operating memory data to the NVM, the MP2926 calculates a CRC code for each bit, and saves the final CRC code to the NVM. In the process of restoring the NVM data to the operating memory, the MP2926 recalculates the CRC code with each bit. The MP2926 checks the CRC results when the restoration process is complete. If the CRC result does not match with what is stored during the store process, the VR shuts down and sets the CRC_FAULT bit. This bit is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No NVM CRC fault 1'b1: An NVM CRC fault has been detected
3	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
2	CML_FLT_TRG	Latch	This bit is set when an NVM operation is blocked because the controller is recording a fault to the NVM. This bit is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: NVM operation is not blocked 1'b1: NVM operation is blocked because the controller is recording a fault to the NVM
1	CML_OTHER_FAULTS	Latch	This bit is set if any of the following PMBus communication faults occur: • Sending too few bits • Reading too few bits • Host sends or reads too few bytes • Reading too many bytes This bit is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit.
0	NVM_SIG_FAULTS	Latch	While restoring data from the NVM to the memory, the device first checks the signature register in address 00h of the NVM. If the signature register is 0x1234, the restoration process is halted immediately, and the NVM_SIG_FAULTS bit is set. This bit is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

READ_ADC_SUM (81h)

The READ_ADC_SUM command on Page 0 returns the sum of 16 consecutive ADC sense results.

Command	READ_ADC_SUM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X		ADC_SUM													

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	ADC_SUM_READY	Indicates when the sum of 16 consecutive ADC sense results is ready. 1'b0: 16 ADC-sense result sum is not ready 1'b1: 16 ADC-sense result sum is ready
13:0	ADC_SUM	Stores the sum of 16 consecutive ADC sense results. Send FBh (0 byte) to start counting the ADC sum.

READ_VFB1_SENSE (82h)

The READ_VFB1_SENSE command on Page 0 returns the ADC-sensed V_{FB}.

Command	READ_VFB1_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_VFB_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_VFB1_SENSE	Returns the ADC-sensed V_{FB1} voltage in direct format. 1.56mV/LSB.

READ_TSENS1_SENSE (83h)

The READ_TSENS1_SENSE command reads the temperature-sense pin voltage.

Command	READ_TSENS1_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_TSENS1	Returns the ADC-sensed voltage on rail 1's TSENS1 pin in direct format. 1.56mV/LSB.

READ_CS1 (84h)

The READ_CS1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS1 pin in direct format. Add an internal low-pass filter before ADC sensing.

Command	READ_CS1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS1	Return the ADC sensed voltage on rail 1's CS1 pin in direct format. 3.125mV/LSB.

READ_CS2 (85h)

The READ_CS2 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS2 pin in direct format. Add an internal low-pass filter before ADC sensing.

Command	READ_CS2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS2	Returns the ADC-sensed voltage on rail 1's CS2 pin in direct format. 3.125mV/LSB.

READ_VIN (88h)

The READ_VIN command on Page 0 provides 2 bytes to return the sensed input voltage based on the VINSEN1 pin in Linear11 format. In VID mode, the returned value must ignore the bits[15:11] exponent value.

Command	READ_VIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	1	1	0	1	1	X	READ_VIN									

Bits	Bit Name	Description
15:11	EXP	Unused. Fixed to 11011.
10	RESERVED	Fixed to 0.
9:0	READ_VIN	Returns the sensed input voltage in Linear11 format. 31.25mV/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 0 returns the sensed rail 1 VOSEN-VORTN voltage. K_R is the dividing ratio of the divider.

Command	READ_VOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	READ_VOUT											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT	Returns the V_{OUT} value. Linear mode: 2mV/LSB. V_{OUT} = READ_VOUT x 2 x K_R Direct mode: VID_STEP/LSB. V_{OUT} = READ_VOUT x VID_STEP x K_R VID_STEP is decided by C1h bits[15:14]. K_R is the dividing ratio of the divider.

READ_IOUT (8Ch)

The READ_IOUT command on Page 0 returns the sensed output current of rail 1 in direct format.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP					READ_IOUT										

Bits	Bit Name	Description
15:11	EXP	This bit is determined by bit[3] of VR_CONFIG1 (C1h). C1h[3]=1: 5'b11110 C1h[3]=0: 5'b11111
10:0	READ_IOUT	Return the sensed output current. It determined by bit[3] of VR_CONFIG1 (C1h). C1h[3] = 1: Represents 0.25A/LSB C1h[3] = 0: Represents 0.5A/LSB

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 0 returns the sensed temperature on the TSENS1 pin in direct format.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	X	X	X	READ_TEMP							

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_TEMP	Returns the sensed temperature on the TSENS1 pin. 1°C/LSB.

READ_PH_NVM (8Eh)

The READ_PH_NVM command on Page 0 returns the active phase number and the GPIO2/3/4 input state.

Command	READ_PH_NVM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	READ_GPIO4	Returns the GPIO4 input state.
8	READ_GPIO3	Returns the GPIO3 input state.
7	READ_GPIO2	Returns the GPIO2 input state.
6	RESERVED	Always return 0.
5:4	PH_NVM_R3	Returns the phase number for rail 3.
3:2	PH_NVM_R2	Returns the phase number for rail 2.
1:0	PH_NVM_R1	Returns the phase number for rail 1.

READ_VCOMP (8Fh)

The READ_VCOMP command on Page 0 returns the COMP value.

Command	READ_VCOMP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_VCOMP							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_VCOMP	Returns the COMP value.

READ_POUT (96h)

The READ_POUT command on Page 0 returns the P_{OUT} value for rail 1.

Command	READ_POUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:0	READ_POUT	Returns the output power, and the ADC value is the same with D1h. Convert the read value to actual power (in W) with the following equation: $$P_{OUT}(W) = \frac{\frac{READ\_POUT \times 8}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}}{t_{SHORT\_TERM}}$$ Where GAIN_SEL is 6Ch bits[11:10], G_{VIDFF} is the V_{DIFF} gain setting from 4Dh bit[10]: 4Dh[10] = 0: G_{VDIFF} = 1 4Dh[10] = 1: G_{VDIFF} = 0.5 And t_{SHORT_TERM} is the short-term time (in µs): 26h[15] = 0: t_{SHORT_TERM} = 26h[12:1] x 0.05µs 26h[15] = 1: t_{SHORT_TERM} = (26h[6:0] + 1) x (Page 2) 55h[13:8] x 0.05µs

PMBUS_REVISION (98h)

The PMBUS_REVISION command on Page 0 returns the PMBus revision to which the device is compliant.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Byte	Byte Name	Byte
7:0	PMBUS_REVISION	Always returns 0x33. It means the MP2926 supports PMBus revisions up to version 1.3.

MFR_ID (99h)

The MFR_ID command allows users to read the unique VR vendor identity. It is block read only.

Byte	Byte Name	Description
3	Character 3	Always read as 0x4D. This represents “M.”
2	Character 2	Always read as 0x50. This represents “P.”
1	Character 1	Always read as 0x53. This represents “S.”

MFR_MODEL (9Ah)

The MFR_MODEL command allows users to reads the unique product identity. It is block read only.

Byte	Byte Name	Description
6	Character 6	Always read as 0x4D. This represents “M.”
5	Character 5	Always read as 0x50. This represents “P.”
4	Character 4	Always read as 0x32. This represents “2.”
3	Character 3	Always read as 0x39. This represents “9.”
2:1	Character 2,1	XX is defined by the register 9Fh value.

MFR_REVISION (9Bh)

The MFR_REVISION command allows users to read the silicon revision track number. It is block read only.

Byte	Byte Name	Description
1	Character 1	Returns the MP2926 product silicon revision tracking number.

MFR_DATE (9Dh)

The MFR_DATE command returns the part's manufacture date in ASCII "DDMMYY" format. For example, if the manufacture date is 2018-06-15, the MFR_DATE value should be: 0x31 35 30 36 31 38. It is block read only.

Byte	Byte Name	Description
6	Character 6	DD identifies the day that the part was manufactured.
5	Character 5	
4	Character 4	MM identifies the month that the part was manufactured.
3	Character 3	
2	Character 2	YY identifies the year that the part was manufactured.
1	Character 1	

MFR_PRODUCT_ID (9Fh)

The MFR_PRODUCT_ID command on Page 0 sets the product ID.

Command	MFR_PRODUCT_ID															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PRODUCT_ID2								PRODUCT_ID1							

Byte	Byte Name	Description
2	PRODUCT_ID2	Always returns 0x32. This represents "2".
1	PRODUCT_ID1	Sets with 0x36. This represents "6".

MFR_PRODUCT_REV (C0h)

The MFR_PRODUCT_REV command on Page 0 tracks the product analog revision. It is read-only.

Command	MFR_PRODUCT_REV							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	PRODUCT_REV							

Bits	Bit Name	Description
7:0	PRODUCT_REV	Returns the MP2926 silicon revision. 0x00: Revision 0 0x01: Revision 2

MFR_VR_CONFIG1 (C1h)

The MFR_VR_CONFIG1 command on Page 0 sets the basic functions of the MP2926.

Command	MFR_VR_CONFIG1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	VID_STEP	Sets the VID resolution. The VID_STEP can be set to 6.25mV, 5mV, and 2mV in PMBus mode and PVID mode. 2'b00: 6.25mV 2'b01: 5mV 2'b1x: 2mV
13	VBOOT_SEL	Selects the boot-up voltage (V_{BOOT}). 1'b0: In PMBus mode, V_{BOOT} is determined by VOUT_COMMAND (21h) 1'b1: In PMBus mode, V_{BOOT} is determined by MFR_PVID (71h)
12	PG_FOR_VID=0V	Selects the PG state when DVID is 0V. 1'b0: High 1'b1: Low
11	PVID_PIN_EN	Selects V_{OUT} for PVID mode. 1'b0: In PVID mode, V_{OUT} is determined by MFR_PVID0 (71h), ignoring the PVID0, PVID1, and PVID2 pins 1'b1: In PVID mode, V_{OUT} is determined by the PVID0, PVID1, and PVID2 pins
10	PVID_EN_R3	Sets the V_{OUT} VID mode to be PVID mode or PMBus mode. This bit is for rail 3 only. 1'b0: PMBus mode 1'b1: PVID mode
9	PVID_EN_R2	Sets the V_{OUT} VID mode to be PVID mode or PMBus mode. This bit is for rail 2 only. 1'b0: PMBus mode 1'b1: PVID mode
8	PVID_EN_R1	Sets the V_{OUT} VID mode to be PVID mode or PMBUS mode. This bit is for for rail 1 only. 1'b0: PMBus mode 1'b1: PVID mode
7	DBG_CRC	Fixed to 1.
6	DEBUG_MODE_EN	Fixed to 0.
5	IOUT_REPORT_SEL_R3	Sets the PMBus report resolution for rail 3. 1'b0: 0.5A/LSB 1'b1: 0.25A/LSB
4	IOUT_REPORT_SEL_R2	Sets the PMBus report resolution for rail 2. 1'b0: 0.5A/LSB 1'b1: 0.25A/LSB

3	IOUT_REPORT_SEL_R1	Sets the PMBus report resolution for rail 1. 1'b0: 0.5A/LSB 1'b1: 0.25A/LSB
2	VIN_TON_CAL_MODE	Selects the V_{IN} value to get the mode when calculating t_{ON}. 1'b0: Update t_{ON} with READ_VIN (88h) 1'b1: Update t_{ON} when READ_VN (88h) exceeds 0.75V. If V_{IN} drops below 0.75V, t_{ON} does not update
1	EN_OFF_MODE_SEL	Sets the EN power-off mode. It is only effective in regular power mode. In low-power mode, EN always powers off the converter with Hi-Z. 1'b 0: Hi-Z off 1'b 1: Soft off
0	RESERVED	Fixed to 1.

MFR_VR_CONFIG2 (C2h)

The MFR_VR_CONFIG2 command sets the basic functions of the MP2926.

Command	MFR_VR_CONFIG2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	DRMOS_TYPE	Selects the DrMOS type. 1'b0: Voltage-sense DrMOS 1'b1: Current-sense DrMOS
14:13	HICCUP_TIME	Sets the hiccup time in retry mode when a protection occurs. 2'b00: 12.5ms 2'b01: 6ms 2'b10: 2ms 2'b11: 0.5ms
12	VR_TEMPER_MERGE_EN	Selects the TSENS pin function. 1'b0: Use the TSENS1 pin to monitor rail 1's temperature reporting. Use the TSENS2 pin to monitor rail 2's temperature reporting. Use the TSENS3 pin to monitor rail 3's temperature reporting 1'b1: Use the TSENS1 pin to monitor the temperature reporting for all rails. All three DrMOS TEMP pins should be shorted together with the TSENS1 pin. The TSENS3 pin can be used as a flexible system-level protection pin.
11	DRMOS_FLT_DETECT_EN_R3	Enable bit for the PWM pin as the DrMOS fault type indicator and fault type recorded to the NVM. This is for rail 3 only. For some Intelli-Phase™ products, PWM can report the DrMOS fault type. When this function is enabled, the MP2926 monitors the voltage on the PWM pin to detect the fault type after the VR shuts down. 1'b0: Disabled 1'b1: Enabled

10	DRMOS_FLT_DETECT_EN_R2	Enable bit for the PWM pin as the DrMOS fault type indicator and fault type recorded to the NVM. This is for rail 2 only. For some Intelli-Phase™ products, PWM can report the DrMOS fault type. When this function is enabled, the MP2926 monitors the voltage on the PWM pin to detect the fault type after the VR shuts down. 1'b0: Disabled 1'b1: Enabled
9	DRMOS_FLT_DETECT_EN_R1	Enable bit for the PWM pin as the DrMOS fault type indicator and fault type recorded to the NVM. This is for rail 1 only. For some Intelli-Phase™ products, PWM can report the DrMOS fault type. When this function is enabled, the MP2926 monitors the voltage on the PWM pin to detect the fault type after the VR shuts down. 1'b0: Disabled 1'b1: Enabled
8	OVP_DVID_BLOCK_EN	Enables blocking V_{OUT} over-voltage protection (OVP) during DVID. 1'b0: Disabled 1'b1: Enabled
7	OVP_DISCHARGE_MODE	Sets the PWM behavior after over-voltage protection (OVP) occurs. 1'b0: If OVP occurs, all PWMs are pulled low until V_{OUT} drops below the reverse-voltage protection (RVP) threshold. All PWMs remain in tri-state, regardless of whether V_{OUT} exceeds the RVP threshold 1'b1: If OVP occurs, all PWMs are pulled low when V_{OUT} exceeds the RVP threshold
6	RESERVED	Fixed to 0.
5	MFR_VRMON_LPF	Set filter parameter for the output voltage report. 1'b0: No V_{OUT} report filter 1'b1: Two points moving average filter
4	MFR_IOUT_LPF	Sets the filter parameter for the output current report. 1'b0: No V_{OUT} report filter 1'b1: Two points moving average filter
3	OCP_PHASE_SS_BLOCK_EN	Enable block over-current protection (OCP) phase limit protection when soft start begins. 1'b0: Disabled 1'b1: Enabled
2	LOW_PWR_MODE_EN	Low-power mode enable bit. In low-power mode, the analog and digital blocks are off and the controller consumes very little quiescent current when EN is off. In regular power mode, when EN goes low it only disables the output power, and the analog block and NVM are still active. It is effective after the power is cycled on VDD33. 1'b0: Disabled 1'b1: Enabled
1	CS_RESISTOR	Selects the IC's internal current-sense (CS) resistor. 1'b0: 1kΩ 1'b1: 2kΩ
0	SDM_FRAC	Enables the decimal fraction for sigma-delta (Σ-Δ) modulation. 1'b0: Disabled 1'b1: Enabled

MFR_VR_CONFIG3 (C3h)

The MFR_VR_CONFIG3 command sets the basic functions of the MP2926.

Command	MFR_VR_CONFIG3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	VOUT_SLEWRATE_RES	V_{OUT} DVID, boot-up, and soft-off slew rate resolution selection. 1'b0: 1mV/µs/LSB 1'b1: 0.01mV/µs/LSB
14	VRMON_SEL_R3	Selects the ADC during V_{OUT} reporting. This is for rail 3 only. 1'b0: Slow ADC 1'b1: Fast ADC
13	VRMON_SEL_R2	Selects the ADC speed during V_{OUT} reporting. This is for rail 2 only. 1'b0: Slow ADC 1'b1: Fast ADC
12	VRMON_SEL_R1	Selects the ADC speed during V_{OUT} reporting. This is for rail 1 only. 1'b0: Slow ADC 1'b1: Fast ADC
11	RESERVED	Fixed to 0.
10	RESERVED	Fixed to 1.
9	RESERVED	Fixed to 0.
8	HIZ_HIGH_BLOCK_EN	Enable the minimum tri-state time constraint when PWM goes from tri-state to high state. The minimum tri-state time is set by PWM_MIN_TIME1 (62h, Page 0 and Page 1), bits[5:0]. 1'b0: Disable minimum tri-state time constraint when PWM goes from Hi-Z to high 1'b1: Enable minimum tri-state time constraint when PWM goes from tri-state to high state
7	RESERVED	Fixed to 0.
6	HIGHFREQ_DEBUG	Enables the PWM signal to be 5ns earlier in high-frequency conditions (>1MHz). Effective in debugging mode. 1'b0: Disabled 1'b1: Enabled
5	WATCH_DOG_EN	Enables the watchdog. 1'b0: Disabled 1'b1: Enabled
4	DELAY_LINE_EN	Enables the delay line loop to sharply reduce PWM jitter when the frequency loop is applied. 1'b0: Disabled 1'b1: Enabled
3	VIN2TON_EN	Enables V_{IN} influence toward t_{ON}. 1'b0: V_{IN} sensing does not influence the PWM on time 1'b1: V_{IN} sensing influences the PWM on time

2:1	BG_CHOP_MODE	Selects the bandgap chop frequency. 2'b00: Disable bandgap chop 2'b01: 125kHz 2'b10: 250kHz 2'b11: 500kHz
0	PWM_TRI_MODE	Sets the tri-state voltage level. 1'b0: Hi-Z 1'b1: Middle voltage

MFR_VR_CONFIG4 (C4h)

The MFR_VR_CONFIG4 command sets basic functions for the MP2926.

Command	MFR_VR_CONFIG4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	COMP_HYS_EN	Fixed to 0.
14	REFIN_EN	Enable bit to provide a 1.23V reference voltage on the GPIO pins with sourcing capabilities. A 1µF external capacitor is required. The GPIO pin can be selected with register GPIO_SEL1 (66h), bits[3:0]. 1'b0: Disabled 1'b1: Enabled
13	COMP_DAC_ENLARGE_EN	Enable bit to enlarge the COMP DAC value in the DC loop. 1'b0: Disabled 1'b1: Enabled
12	TSENS2_FLT_EN	Enables the TSENS2 fault pin to act as a DrMOS fault type indicator and record the fault type to the NVM. The MP2926 monitors the voltage level on TSENS2. If the TSENS2 voltage exceeds 2.2V, it indicates that a DrMOS fault has occurred. 1'b0: Disable TSENS2 fault protection 1'b1: Enable TSENS2 fault protection
11	TSENS1_FLT_EN	Enables the TSENS1 fault pin to act as a DrMOS fault type indicator and record the fault type to the NVM. The MP2926 monitors the voltage level on TSENS1. If the TSENS1 voltage exceeds 2.2V, it indicates that a DrMOS fault has occurred. 1'b0: Disable TSENS1 fault protection 1'b1: Enable TSENS1 fault protection
10	VORTN_LINE_FLOAT_EN	Enable bit to detect whether the VORTN pin is floating for all rails. 1'b0: Disabled 1'b1: Enabled
9	VOSEN_LINE_FLOAT_EN	Enable bit to detect whether the VOSEN pin is floating for all rails. 1'b0: Disabled 1'b1: Enabled
8:7	PVID3V3_1V8	Sets the PVID power logic. 2'b10: 3.3V logic 2'b01:1.8V logic Others are valid.

6	TON_REDUCTION_ DCM_EN_R3	Enables 1/4 t_{ON} reduction during DCM operation for rail 3. If t_{ON} reduction is enabled, the on time is reduced by 1/4 during 1-phase DCM to reduce the output voltage ripple. 1'b0: Disabled 1'b1: Enabled
5	TON_REDUCTION_ DCM_EN_R2	Enables 1/4 t_{ON} reduction during DCM operation for rail 2. If t_{ON} reduction is enabled, the on time is reduced by 1/4 during 1-phase DCM to reduce the output voltage ripple. 1'b0: Disabled 1'b1: Enabled
4	TON_REDUCTION_ DCM_EN_R1	Enables 1/4 t_{ON} reduction during DCM operation for rail 1. If t_{ON} reduction is enabled, the on time is reduced by 1/4 during 1-phase DCM to reduce the output voltage ripple. 1'b0: Disabled 1'b1: Enabled
3	DAC_CMP_EN_R3	Enable bit for smooth transition when DVID going down is preempted by DVID going up. This is for rail 3 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: Disable the rail 3 V_{REF} filter function in continuous down-and-up DVID 1'b1: Enable the rail 3 V_{REF} filter function in continuous down-and-up DVID
2	DAC_CMP_EN_R2	Enable bit for smooth transition when DVID going down is preempted by DVID going up. This is for rail 2 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: Disable the rail 2 V_{REF} filter function in continuous down-and-up DVID 1'b1: Enable the rail 2 V_{REF} filter function in continuous down-and-up DVID
1	DAC_CMP_EN_R1	Enable bit for smooth transition when DVID going down is preempted by DVID going up. This is for rail 1 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: Disable the rail 1 V_{REF} filter function in continuous down-and-up DVID 1'b1: Enable the rail 1 V_{REF} filter function in continuous down-and-up DVID
0	SLOPE_LEAKAGE	Enable bit to turn off the low-leakage switch after the current source during DCM. This avoids leakage from the slope compensation current source via the high-leakage switch. 1'b0: Disabled 1'b1: Enabled

MFR_VR_CONFIG5 (C5h)

The MFR_VR_CONFIG5 command sets basic functions for the MP2926.

Command	MFR_VR_CONFIG5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	OV_UV_1/2_EN_R3	Enables the 1/2 divider for the rail 3 VOUT VID_OVP and VID_UVP thresholds. 1'b0: Disabled 1'b1: Enabled
14	OV_UV_1/2_EN_R2	Enables the 1/2 divider for the rail 2 VOUT VID_OVP and VID_UVP thresholds. 1'b0: Disabled 1'b2: Enabled

13	OV_UV_1/2_EN_R1	Enables the 1/2 divider for the rail 1 VOUT VID_OVP and VID_UVP thresholds. 1'b0: Disabled 1'b3: Enabled
12	RVP_1/2_SET_EN_R3	Enables the rail 3 reverse-voltage protection (RVP) threshold 1/2 divider. 1'b0: Disabled 1'b1: Enabled
11	RVP_1/2_SET_EN_R2	Enables the rail 2 reverse-voltage protection (RVP) threshold 1/2 divider. 1'b0: Disabled 1'b1: Enabled
10	RVP_1/2_SET_EN_R1	Enable the rail 1 reverse-voltage protection (RVP) threshold 1/2 divider. 1'b0: Disabled 1'b1: Enabled
9	MFR_DBG_FIX32	Always fixed to 1.
8:6	ZCD_SET_R3	Fine-tunes the rail 3 zero-current detection (ZCD) threshold. 3'b000: -10mV 3'b001: -5mV 3'b010: 0mV 3'b011: +5mV 3'b100: +10mV 3'b101: +15mV 3'b110: +20mV 3'b111: +25mV
5:3	ZCD_SET_R2	Fine-tunes the rail 2 zero-current detection (ZCD) threshold. 3'b000: -10mV 3'b001: -5mV 3'b010: 0mV 3'b011: +5mV 3'b100: +10mV 3'b101: +15mV 3'b110: +20mV 3'b111: +25mV
2:0	ZCD_SET_R1	Fine-tunes the rail 1 zero-current detection (ZCD) threshold. 3'b000: -10mV 3'b001: -5mV 3'b010: 0mV 3'b011: +5mV 3'b100: +10mV 3'b101: +15mV 3'b110: +20mV 3'b111: +25mV

MFR_VR_CONFIG6 (C6h)

The MFR_VR_CONFIG6 command sets basic functions for the MP2926.

Command	MFR_VR_CONFIG6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	VID_DAC_FILTER_R3	Selects the filter for the rail 3 VID-DAC when VID ramps down. 2'b00: 2.35µs filter 2'b01: 4.7µs filter 2'b10: 7.05µs filter 2'b11: 9.4µs filter
13	VID_DAC_FILTER_R3_EN	Enables the VID-DAC filter for rail 3 when DVID ramps down. This avoids output voltage undershoot. 1'b0: Disabled 1'b1: Enabled
12:11	VID_DAC_FILTER_R2	Selects the VID-DAC filter for rail 2 when VID ramps down. 2'b00: 2.35µs filter 2'b01: 4.7µs filter 2'b10: 7.05µs filter 2'b11: 9.4µs filter
10	VID_DAC_FILTER_R2_EN	Enables the VID-DAC filter for rail 2 when DVID ramps down. This avoids output voltage undershoot. 1'b0: Disabled 1'b1: Enabled
9:8	VID_DAC_FILTER_R1	Selects the VID-DAC filter for rail 1 when VID ramps down. 2'b00: 2.35µs filter 2'b01: 4.7µs filter 2'b10: 7.05µs filter 2'b11: 9.4µs filter
7	VID_DAC_FILTER_R1_EN	Enables the VID-DAC filter for rail 1 when DVID ramps down. This avoids output voltage undershoot. 1'b0: Disabled 1'b1: Enabled
6	VOUT_SR_PLUS_EN	Fixed to 0.
5:4	FILTER_IMON3_JOUT	Sets the filter time constant for the IMON3 J_{OUT} buffer. 2'b00: 810ns 2'b01: 2µs 2'b10: 3.5µs 2'b11: 12.2µs
3:2	FILTER_IMON2_JOUT	Sets the filter time constant for the IMON2 J_{OUT} buffer. 2'b00: 810ns 2'b01: 2µs 2'b10: 3.5µs 2'b11: 12.2µs
1:0	FILTER_IMON1_JOUT	Sets the filter time constant for the IMON1 J_{OUT} buffer. 2'b00: 810ns 2'b01: 2µs 2'b10: 3.5µs 2'b11: 12.2µs

MFR_VR_CONFIG7 (C7h)

The MFR_VR_CONFIG7 command sets basic functions for the MP2926.

Command	MFR_VR_CONFIG7															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	MFR_PAGE_EN	Enable bit to follow the WRITE_PROTECT (10h) register setting. 1'b0: Disabled 1'b1: Enabled
14	MFR_BYTEWR_DEBUG	Fixed to 0.
13	MFR_BYTEWR_ DEBUG2	Fixed to 0.
12:9	MFR_SW_BLOCK_SET	Sets the slope low-leakage switch turn-on time during DCM. The PWM set signal is blocked when turning on the low-leakage switch. 10ns/LSB.
8:6	VID_DATA_UPDATE_ R3	Fixed to 10.
5:3	VID_DATA_UPDATE_ R2	Fixed to 2.
2:0	VID_DATA_UPDATE_ R1	Fixed to 2.

MFR_TIMEOUT (C8h)

The MFR_TIMEOUT command sets the timeout time in PMBus mode.

Command	MFR_TIMEOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:9	MFR_ADC_HOLD_TIME	Sets the ADC hold time. 50ns/LSB.
8	PMBUS_FILTER_EN	1'b0: The PMBus digital degiltch filter is disabled 1'b1: The PMBus digital degiltch filter is enabled
7:4	PMBUS_TIMEOUT	Sets the PMBus timeout time, calculated with the following equation: PMBUS_TIMEOUT x 1.6ms + 1.5ms
3	PMBUS_SDA_DELAY_ EN	1'b0: SCL and SDA have the same delay 1'b1: SDA is delayed 50ns longer than SCL
2:0	RESERVED	Unused. Fixed to 0.

CAPABILITY (D0h)

The CAPABILITY command is read-only.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7:0	CAPABILITY	Fixed to 0xC0.

JOUT1_SHORT_TERM (D1h)

The JOUT1_SHORT_TERM command on Page 0 returns the real-time J_{OUT} value in every short-term period.

Command	JOUT1_SHORT_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT1_SHORT_TERM															

Bits	Bit Name	Description
15:0	JOUT1_SHORT_TERM	Returns the real-time J_{OUT} value in every short-term period. Convert the read value to the actual output (in μJ) with the following equation: $J_{OUT\_SHORT\_TERM}(\mu J) = \frac{D1h \times 8}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch bits[11:10], and G_{VIDFF} is the V_{DIFF} gain setting from 4Dh bit[10]: 4Dh[10] = 0: G_{VIDFF} = 1 4Dh[10] = 1: G_{VIDFF} = 0.5

JOUT1_LONG_TERM (D2h)

The JOUT1_LONG_TERM command on Page 0 returns the J_{OUT} value in every long-term period.

Command	JOUT1_LONG_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT1_LONG_TERM															

Bits	Bit Name	Description
15:0	JOUT1_LONG_TERM	Returns the real-time J_{OUT} value in every long-term period. Convert the read value to the actual output (in mJ) with the following equation: $J_{OUT\_LONG\_TERM}(mJ) = \frac{D2h \times 16.384}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch bits[11:10], and G_{VIDFF} is the V_{DIFF} gain setting from 4Dh bit[10]: 4Dh[10] = 0: G_{VIDFF} = 1 4Dh[10] = 1: G_{VIDFF} = 0.5

IMON1_FAST_SENSE (D3h)

The IMON1_FAST_SENSE command on Page 0 returns a J_{OUT} ADC value.

Command	IMON1_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	IMON1_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IMON1_FAST_SENSE	Returns the I_{OUT} ADC value in J_{OUT} calculations. Convert the read value to the actual output current (in A) with the following equation: $$I_{OUT}(A) = \frac{D3h[9:0]}{6Ch[9:0]\times 1024} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$$ Where GAIN_SEL is 6Ch bits[11:10].

VDIFF1_FAST_SENSE (D4h)

The VDIFF1_FAST_SENSE command on Page 0 returns the J_{OUT} ADC value.

Command	VDIFF1_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	VDIFF1_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VDIFF1_FAST_SENSE	Returns the V_{OUT} ADC value in J_{OUT} calculations. 1.56mV/LSB @ V_{DIFF} gain = 1 3.12mV/LSB @ V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 0) bit[10].

ADC_SUM_RESET (FBh)

The ADC_SUM_RESET command resets the ADC_SUM count.

This command is write-only. There is no data byte for this command.

CLEAR_CRC_FAULT (FCh)

The CLEAR_CRC_FAULT command clears the CRC fault information that is stored in NVM.

This command is write-only. There is no data byte for this command.

CLEAR_STORED_FAULTS (FEh)

The CLEAR_STORED_FAULTS command clears the last fault information that is stored in NVM.

This command is write-only. There is no data byte for this command.

CLEAR_NVM_FAULTS (FFh)

The CLEAR_NVM_FAULTS command clears the NVM faults.

This command is write-only. There is no data byte for this command.

PAGE 1 REGISTER MAP

OPERATION_R2 (01h)

The OPERATION_R2 command on Page 1 turns the rail 2 output on or off in conjunction with the input from the EN pin, and sets the output voltage to the upper or lower margin voltages. The controller stays in the set OPERATION command mode until a subsequent OPERATION command is received, or a change in the EN state changes rail 2 to another mode.

Command	OPERATION_R2							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								

Bits	Bit Name	Description
7:0	OPERATION_R2	Sets the operation mode for rail 2. 8’b 00xx xxxx: Hi-Z off 8’b 01xx xxxx: Soft off 8’b 1000 xxxx: Normal on 8’b 1001 xxxx: Margin low 8’b 1010 xxxx: Margin high Others: Invalid commands “x” means not applicable.

STORE_ALL_CODE (15h)

The STORE_ALL_CODE command instructs the PMBus device to copy all Page 0, Page 1, and Page 2 contents, including the internal trim registers, from the operating memory to the matching locations in the NVM. Any items in the operating memory that do not have matching locations in the user store are ignored.

This command is controlled by 50h (Page 1) bits[7:0]. When bits[7:0] equal 0x63, the NVM can accept writes. For all other values, the NVM is write-protected.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents, including the internal trim registers, from the NVM and overwrites the matching locations in the operating memory. Any items in the user store that do not have matching locations in the operating memory are ignored.

While the device is outputting power, this command is ignored and cannot be used. This command is write-only. There is no data byte for this command.

STORE_USER_CODE (17h)

The STORE_USER_CODE command instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the operating memory to the matching locations in the NVM, except for the internal trim registers. Any items in the operating memory that do not have matching locations in the user store are ignored.

This command is controlled by 50h (Page 1) bits[7:0]. When bits[7:0] equal 0x63, the NVM can accept writes. For all other values, the NVM is write-protected.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_USER_CODE (18h)

The RESTORE_USER_CODE command instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the NVM and overwrites the matching locations in the operating memory. Trim registers are not overwritten by this command.

While the device is outputting power, this command is ignored and cannot be used. This command is write-only. There is no data byte for this command.

VOUT_COMMAND_R2 (21h)

Command	VOUT_COMMAND_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_COMMAND_R2	Sets the rail 2 V_{REF} (VID-DAC output voltage) in PMBus VID mode. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14]. VID_STEP/LSB.

VOUT_TRIM_R2 (22h)

The VOUT_TRIM_R2 command on Page 1 applies a fixed offset voltage to the rail 2 output voltage command value.

Command	VOUT_TRIM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRIM_R2	Sets the V_{OUT} offset value. VID_STEP/LSB.

VOUT_MAX_R2 (24h)

The VOUT_MAX_R2 command on Page 1 sets the maximum reference voltage for rail 2 VID-DAC, so as to set the maximum output voltage. When an external resistor divider is applied, the maximum voltage is clamped to VOUT_MAX / K_R. K_R is the dividing ratio of the external resistor divider. It is effective in PMBus VID mode and PVID mode.

Command	VOUT_MAX_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

10:0	VOUT_MAX_R2	Sets the rail 2 maximum VID + offset voltage. It limits the sum of the VID + VOUT_TRIM offset. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14]. VID_STEP/LSB.

MFR_JOUT_LONG_TERM_R2 (25h)

The MFR_JOUT_LONG_TERM_R2 command on Page 1 sets the long-term value to calculate J_{OUT}.

Command	MFR_JOUT_LONG_TERM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	JOUT_LONG_TERM	Sets the long-term value for J_{OUT} calculations, estimated with the following equation: LONG_TIME = JOUT_LONG_TERM x SHORT_TIME

MFR_JOUT_SHORT_TERM_R2 (26h)

The MFR_JOUT_SHORT_TERM_R2 command on Page 1 sets the short-term value to calculate J_{OUT}.

Command	MFR_JOUT_SHORT_TERM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	JOUT_EN	Enable bit for the J_{OUT} function. 1'b1: Enabled 1'b0: Disabled
12:7	JOUT_SHORT_TERM_FIX_FREQ	Fixed to 0 in fixed-frequency mode.
6:0		Sets JOUT_SHORT_TERM in fixed-frequency mode. ADC_TIME/LSB. The time can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_FIX_FREQ x ADC_TIME
12:1	JOUT_SHORT_TERM_ADAPTIVE_FREQ	50ns/LSB in adaptive frequency mode. The time can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_ADAPTIVE_FREQ x 50ns
0		Fixed to 0 in adaptive frequency mode.

VOUT_TRANSITION_RATE_R2 (27h)

The VOUT_TRANSITION_RATE_R2 command on Page 1 sets the rail 2 dynamic VID transition slew rate in PMBus and PVID mode.

Command	VOUT_TRANSITION_RATE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	VOUT_TRANSITION_RATE_R2	Sets the rail 2 dynamic VID transition slew rate in PMBus and PVID mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h) bit[15].

VOUT_DROOP_R2 (28h)

The VOUT_DROOP_R2 on Page 1 sets the load-line configuration for rail 2.

Command	VOUT_DROOP_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	IACDROOP_BW_SET_R2	Enable bit to increase the AC droop BW by increasing bias current. This is for rail 2 only. 1'b0: Disabled 1'b1: Enabled
14	IACDROOP_BW_SET_R2	Enable bit to increase the AC droop BW by reducing the compensation capacitor. This is for rail 2 only. 1'b0: Disabled 1'b1: Enabled
13	IACDROOP_GAIN2_SET_R2	Sets the PMBus AC droop's second current mirror ratio (GAIN2) for rail2. It is active when bit [12] = 1. 1'b0: 1 1'b1: 1/2
12	MFR_ACLL_EN_R2	AC or DC load line selection bit. 1'b0: DC load line 1'b1: AC load line
11:9	IDROOP_GAIN2_R2	Sets the PMBus DC droop's second current mirror ratio (GAIN2) for rail2. It is active when bit [12] = 0. The MP2926 provides eight configurable levels. 3'b000: 0 3'b001: 3/4 3'b010: 4/4 3'b011: 5/4 3'b100: 6/4 3'b101: 7/4 3'b110: 8/4 3'b111: 9/4
8:7	IDROOP_GAIN1_R2	Sets the PMBus I_{DROOP} first current mirror ratio (GAIN1) for rail 2. The initial load line slope can be calculated with the following equation: $$R_{LL\_INI} = R_{DROOP} \times K_{CS} \times GAIN1 \times GAIN2$$ 2'b00: 1/16 2'b01: 1/8 2'b10: 1/4 2'b11: 1/2
6	SHORT_FIRST_HALF_R2	1'b0: Do not short the first half of the resistors for rail 2 1'b1: Short the first half of the resistors for rail 2 Set to 1 if R_{DROOP} is below 3.2kΩ.
5:0	RDROOP_SET_R2	Sets R_{DROOP} for rail 2. 100Ω/LSB. 6.4kΩ maximum.

VOUT_SCALE_LOOP_R2 (29h)

The VOUT_SCALE_LOOP_R2 command on Page 1 sets the rail 2 output voltage to reference voltage dividing ratio when an external output divider is applied.

Command	VOUT_SCALE_LOOP_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VOUT_SCALE_LOOP_R2	Sets the rail 2 output voltage to reference voltage dividing ratio. V_{REF} ranges from 0V to 1.55V.

MFR_SETTLE_CTRL_R2 (2Ah)

The MFR_SETTLE_CTRL_R2 command on page 1 sets the DVID parameters.

Command	MFR_SETTLE_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:11	MFR_DROOPFALL_DELAY_R2	Sets the delay time between V_{REF} reaching the target (VID + DROOP_VID) and V_{REF} falling back to VID. 50ns/LSB.
0:6	MFR_RISE_STEP_R2	Sets the extra VID steps count for rail 1 when DVID is up. The extra VID steps compensate for the droop caused by the output capacitor charging during DVID up. 1 step/LSB.
5:0	RESERVED	Fixed to 0.

VOUT_MIN_R2 (2Bh)

The VOUT_MIN_R2 command on Page 1 instructs the device to limit the rail 2 minimum output voltage during PMBus and PVID mode. If the output voltage decoded from the PMBus interface or set by the PVID registers drops below what is set by VOUT_MIN (2Bh), the output voltage is clamped to VOUT_MIN. If an external resistor divider is applied on VOSEN, the minimum output voltage is clamped to VOUT_MIN / K_R. K_R is the dividing ratio of the divider.

Command	VOUT_MIN_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MIN_R2	Sets the minimum VID value in PMBus mode for rail 2. Any VID below this value is clamped to VOUT_MIN. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].

MFR_TRIM_DCM_1P_2P_R2 (2Ch)

The MFR_TRIM_DCM_1P_2P command on Page 1 trims the output voltage during 2-phase CCM and 1-phase CCM or the DCM power state for rail 2.

Command	MFR_TRIM_DCM_1P_2P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	MFR_TRIM_2PS_R2	Sets the V_{OUT} trim for 2-phase CCM operation. 2.3mV/LSB.
9:5	MFR_TRIM_1PS_R2	Sets the V_{OUT} trim for 1-phase CCM operation. 2.3mV/LSB.
4:0	MFR_TRIM_DCM_R2	Sets the V_{OUT} trim for 1-phase DCM operation. 2.3mV/LSB.

MFR_RESERVED (2Dh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (2Fh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_BLANK_TIME1_R2 (31h)

The MFR_BLANK_TIME1_R2 command on Page 1 programs the slope compensation reset time and PWM blanking time between two consecutive phases. It is for rail 2 only.

Command	MFR_BLANK_TIME1_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	MFR_SLOPE_BLANK_TIME1_R2	Programs the slope compensation reset time. The slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME (e.g. bits[5:0] in register MFR_BLANK_TIME1 (31h, Page 1)). 5ns/LSB.
5:0	MFR_PHASE_BLANK_TIME1_R2	Programs the PWM blanking time between two consecutive phases. 5ns/LSB.

MFR_VIN_SCALE_LOOP (32h)

The VIN_SCALE_LOOP command on Page 1 sets the resistor divider ratio for input voltage sensing.

Command	MFR_VIN_SCALE_LOOP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:0	MFR_VIN_SCALE_LOOP	Sets the input voltage sensing scale, calculated with the following equation: $VIN\_SCALE\_LOOP = \frac{1280 \times V_{INSEN}}{V_{IN}} = \frac{1280 \times R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}}$ Where R_{TOP} and R_{BOTTOM} are the resistor divider on the VINSEN pin.

FREQUENCY_SWITCH_R2 (33h)

The FREQUENCY_SWITCH_R2 command on Page 1 sets the switching frequency for rail 2. The switching frequency is between 200kHz and 5.11MHz, with 10kHz per step.

Command	FREQUENCY_SWITCH_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	FREQUENCY_SWITCH_R2	Sets the switching frequency in direct format. 10kHz/LSB.

MFR_OSR_SET_R2 (34h)

The MFR_OSR_SET_R2 command on Page 1 sets the overshoot reduction (OSR) parameters. It is for rail 2 only.

Command	MFR_OSR_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	MFR_OSR_EN_R2	Enables overshoot reduction (OSR). OSR can reduce the V_{OUT} overshoot at the load release. 1'b0: Disabled 1'b1: Enabled
12:7	MFR_OSR_FILTER_R2	Sets the minimum overshoot reduction (OSR) time. 5ns/LSB.
6:0	MFR_OSR_BLANKTIME_R2	Sets the blanking time between two effective overshoot reduction (OSR) events. 10ns/LSB.

MFR_TSENS3_SET (36h)

The MFR_TSEN3_SET command on Page 1 sets some configurations for TSEN3 faults.

Command	MFR_TSNS3_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	RESERVED	Fixed to 0.
14	TSENS3_DGTL_FLT_EN	Enables the TSENS3 digital-sense fault to shut down all rails. The MP2926 senses the voltage on the TSENS3 pin with internal ADC. If sensed voltage exceeds or drops below the threshold set by MFR_TSENS3_SET (36h, Page 1) bit[13:8], then a TSENS3 fault occurs and the device shuts down all rails immediately. The TSENS3 sense fault response is determined by MFR_TSENS3_SET (36h, Page 1), bit[1]. 1'b0: Disable TSENS3 digital-sense fault protection 1'b1: Enable TSENS3 digital-sense fault protection
13:8	TSENS3_DAC_SET	Sets the TSENS3 digital fault threshold. 4 ADC step/LSB.
7	MFR_TSENS3_FLT_EN	Enables the TSENS3 fault pin to act as a DrMOS fault type indicator and record the fault type to the NVM. The MP2926 monitors the voltage level on the TSENS3 pin. If sensed voltage exceeds 2.2V, it indicates that a DrMOS fault has occurred. 1'b0: Disable TSENS3 fault protection 1'b1: Enable TSENS3 fault protection
6:2	MFR_TSENS3_DELAY_TIME	Sets the delay time for TSENS3_DGTL_FAULT. 100ns/LSB.
1	MFR_TSENS3_FLT_DIR	Selects the TSENS3 digital fault response. 1'b0: A TSENS3 digital fault is triggered when the TSENS3 voltage exceeds the threshold set by bits[13:8] in this command 1'b1: A TSENS3 digital fault is triggered when the TSENS3 voltage drops below the threshold set by bits[13:8] in this command
0	MFR_TSNS3_FLT_MODE	Selects the TSENS3 digital fault action mode. 1'b0: Auto-retry mode 1'b1: Latch-off mode

MFR_SLOPE_SW_INI_R2 (37h)

The MFR_SLOPE_SW_INI command on 1 sets the rail 2 soft start initial ramp.

Command	MFR_SLOPE_SW_INI_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	MFR_VOUT_FINE_TUNE_R2	Sets the V_{OUT} fine-tune trim value per step. Bit[12] is the sign bit. 0.64mV/LSB when the V_{DIFF} gain = 1 0.96mV/LSB when the V_{DIFF} gain = 1/2
6:0	MFR_SLOPE_SW_INI_R2	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_DCM_R2 (38h)

The MFR_SLOPE_SR_DCM command on Page 1 sets the rail 2 slope compensation slew rate in single-phase DCM.

Command	MFR_SLOPE_SR_DCM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_1P_R2 (39h)

The MFR_SLOPE_SR_1P_R2 command on Page 1 provides 2 bytes to program the slope compensation for single-phase operation. It is for rail 2 only.

Command	MFR_SLOPE_SR_1P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_2P_R2 (3Ah)

The MFR_SLOPE_SR_2P_R2 command on Page 1 provides 2 bytes to program the slope compensation for single-phase operation. It is for rail 2 only.

Command	MFR_SLOPE_SR_2P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_RESERVED (3Bh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (3Ch)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (3Dh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_VRHOT_SET_R2 (3Eh)

The MFR_VRHOT_SET_R2 command on Page 1 sets the VR_HOT parameters. It is for rail 2 only.

Command	MFR_VRHOT_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_VRHOT_EN_R2	Enables VR_HOT. 1'b0: Disable VR_HOT 1'b1: Enable VR_HOT
7:0	MFR_VRHOT_LIMIT_R2	Sets the VR over-temperature alert threshold. If the sensed temperature via TSENS2 pin exceeds this threshold, OCP_L from the GPIO pins asserts to alert the system. 1°C/LSB.

MFR_RESERVED(3Fh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

VOUT_OV_FAULT_LIMIT_R2 (40h)

Command	VOUT_OV_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	OVP_VID_SET_R2	3'b001: V_{REF} + 200mV 3'b010: V_{REF} + 325mV 3'b100: V_{REF} + 450mV Others: Invalid commands
7:0	OVP_ABS_SET_R2	Sets the absolute over-voltage protection (OVP) threshold. If V_{OUT} exceeds this value, OVP is triggered. 10mV/LSB.

VOUT_OV_FAULT_RESPONSE_R2 (41h)

The VOUT_OV_FAULT_RESPONSE_R2 command sets protection modes and delay times when a V_{OUT} over-voltage fault happens.

Command	VOUT_OV_FAULT_RESPONSE_R2															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OVP_ABS_EN_R2	Enable bit for absolute over-voltage protection (OVP). 1'b0: Disabled 1'b1: Enabled
7:6	MFR_OVP_VID_MODE_R2	Sets the over-voltage (OV) fault mode. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	MFR_OVP_VID_ DELAYTIME_R2	Sets the OVP_VID blanking time. When an OVP_VID condition remains for longer than the OVP_VID blanking time, an OVP_VID fault is triggered. 100ns/LSB.

VOUT_MAX_ALERT_R2 (42h)

The VOUT_MAX_ALERT_R2 command on Page 1 sets the V_{OUT} over-voltage (OV) warning threshold, or returns the V_{OUT} peak value for rail 2. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	VOUT_MAX_ALERT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	VOUT_MAX_ALERT_R2	If GPIO_ACTIVE (68h) bit [13] is set to 0, 42h sets the V_{OUT} over-voltage (OV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit [13] is set to 1, 42h returns the maximum peak value of V_{OUT}. It can also be written with a lower value. If a higher V_{OUT} is detected, this register is overwritten. To start a new recording, reset this bit by writing 0x0000. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 1) bit[10].

VOUT_MIN_ALERT_R2 (43h)

The VOUT_MIN_ALERT_R2 command on Page 1 sets the V_{OUT} under-voltage (UV) warning threshold, or returns the V_{OUT} peak value for rail 2. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	VOUT_MIN_ALERT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	VOUT_MIN_ALERT_R2	If GPIO_ACTIVE (68h) bit[13] is set to 0, 43h sets the V_{OUT} under-voltage (UV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, 43h returns the minimum V_{OUT} value. It can also be written with a higher value. If a lower V_{OUT} is detected, this register is overwritten. To start a new recording, reset this bit by writing 0x03FF. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 1) bit[10].

VOUT_UV_FAULT_LIMIT_R2 (44h)

The VOUT_UV_FAULT_LIMIT_R2 command sets the V_{OUT} under-voltage (UV) fault threshold.

Command	VOUT_UV_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	UVP_VID_SET_R2	Sets the under-voltage protection (UVP) threshold. 3'b000: V_{REF} - 425mV 3'b001: V_{REF} - 375 mV 3'b010: V_{REF} - 325mV 3'b011: V_{REF} - 275mV 3'b100: V_{REF} - 225mV 3'b101: V_{REF} - 175mV 3'b110: V_{REF} - 125mV 3'b111: V_{REF} - 75mV
7:0	RESERVED	Fixed to 0.

VOUT_UV_FAULT_RESPONSE_R2 (45h)

The VOUT_UV_FAULT_RESPONSE_R2 on Page 1 sets the under-voltage (UV) fault response.

Command	VOUT_UV_FAULT_RESPONSE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_UV_VID_EN_R2	Enable bit for VID under-voltage protection (UVP). 1'b0: Disabled 1'b1: Enabled
7:6	MFR_UVP_MODE_R2	Sets the V_{OUT} under-voltage protection (UVP) mode. There are four modes available. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	MFR_UVP_ DELAYTIME_R2	Sets the V_{OUT} under-voltage protection (UVP) blanking time. A UVP fault occurs if the sensed V_{DIFF} drops below the UVP threshold for the UVP blanking time. 100ns/LSB.

IOUT_OC_FAULT_LIMIT_R2 (46h)

The IOUT_OC_FAULT_LIMIT_R2 command on Page 1 sets the I_{OUT} over-current (OC) fault threshold.

Command	IOUT_OC_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	OCP_SPIKE_SET_R2	Sets the rail 2 OCP_SPIKE_TOTAL current level DAC value. 6.25mV/LSB. This value can be calculated with the following equation: $OCP\_SPIKE\_TOTAL = OCP\_SPIKE \times KCS \times G_{IMON} \times R_{IMON} / 6.25$
7:0	OCP_TDC_SET_R2	Sets the rail 1 OCP_TDC_TOTAL current level. The high 8 MSB of IMON1 ADC result IMON1_SENSE bits[9:0] is compared to this TDC level. The level can be calculated with the following equation: $OCP\_TDC\_TOTAL = OCP\_TDC \times KCS \times G_{IMON} \times R_{IMON} / 6.25$

IOUT_OC_FAULT_RESPONSE_R2 (47h)

The IOUT_OC_FUALT_RESPONSE command sets the rail 1 over-current protection (OCP) options and values.

Command	IOUT_OC_FAULT_RESPONSE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	MFR_OCP_MODE_R2	Selects the protection mode for both over-current protection (OCP_TDC and OCP_SPIKE) faults. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times

13	MFR_OCP_TDC_EN_R2	Enable bit for over-current protection (OCP_TDC). 1'b0: Disabled 1'b1: Enabled
12:8	MFR_OCPTDC_ ACTION_DELAY_R2	Sets the over-current protection (OCP_TDC) fault action time. The time delay is between when the OCP_L signal asserts and current limiting, hiccup mode entry, or shutdown. 1µs/LSB.
7:0	MFR_OCPTDC_TRIG_ DELAY_R2	Sets the over-current protection (OCP_TDC) fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for the OCP_TDC blanking time. 20µs/LSB.

IOUT_OC_SPIKE_RESPONSE_R2 (48h)

The IOUT_OC_SPIKE_RESPONSE_R2 command sets the over-current (OC) spike options and values.

Command	IOUT_OC_SPIKE_RESPONSE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OCP_SPIKE_EN_R2	Enable bit for over-current protection (OCP_SPIKE). 1’b0: Disabled 1’b1: Enabled
7:4	MFR_OCPSPIKE_ ACTIONDELAY_R1	Sets the over-current protection (OCP_SPIKE) fault action delay time. The time is between when OCP_L asserts (after exceeding the current threshold relative to $I_{DDSPIKE}$) and current limiting, hiccup mode entry, or shutdown. 1µs/LSB.
3:0	MFR_OCPSPIKE_ TRIG_DELAY_R1	Sets the over-current protection (OCP_SPIKE) fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for the OCP_SPIKE blanking time. 200ns/LSB.

MFR_OCP_PHASE_LIMIT_R2 (49h)

The MP2926 provides OCP_PHASE protection to limit the per-phase valley current. OCP_PHASE is implemented by monitoring and comparing the cycle-by-cycle sensed current with a current reference. The MFR_OCP_PHASE_LIMIT_R2 command on Page 1 sets the rail 2 per-phase valley current limit.

Command	MFR_OCP_PHASE_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	RESERVED	Unused. Fixed to 0.
7:0	OCP_DAC_SET_R2	Sets the per-phase valley current limit DAC value. 5mV/LSB.

IOUT_MAX_ALERT_R2 (4Ah)

The IOUT_MAX_ALERT_R2 command on Page 1 sets the I_{OUT} over-current (OC) warning threshold or returns the peak value of I_{OUT}. This command is for rail 2 only, and is determined by GPIO_ACTIVE (68h) bit[13].

Command	IOUT_MAX_ALERT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	IOUT_MAX_ALERT_R2	If GPIO_ACTIVE (68h) bit[13] is set to 0, 4Ah sets the DAC value for the I_{OUT} over-current (OC) warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, 4Ah returns the peak I_{OUT} value. In this mode, it can be written with a lower value. If a higher I_{OUT} is detected, this register is overwritten. To start a new recording, reset this bit by writing 0x0000. Convert the read value to the actual output current (in A) with the following equation: $$I_{OUT}(A) = \frac{4A[9:0]}{6Ch[9:0]\times 1024} \times 6Eh[10:0] \times 2\,\wedge\,(6 - GAIN\_SEL)$$ Where GAIN_SEL is 6Ch bits[11:10].

MFR_FS_LIMIT_12P_R2 (4Bh)

The MFR_FS_LIMIT_12P_R2 command on Page 1 sets the rail 2 FS_LIMIT threshold for 1-phase and 2-phase operation to detect fast load insertion and exit phase-shedding.

Command	MFR_FS_LIMIT_12P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_FS_LIMIT_2P_R2	Sets the exit phase-shedding PWM interval time during 2-phase operation. If the time interval between two phases is shorter than FS_LIMIT_2P, the count adds 1. When the count reaches the value set by Page 1, 51h bits[2:0], APS is exited immediately. 5ns/LSB.
7:0	MFR_FS_LIMIT_1P_R2	Sets the PWM1 off-time threshold to exit phase-shedding. If the PWM1 off time after excluding MIN_OFF_TIME is shorter than FS_LIMIT_1P, count add 1.When the count reaches the value set by Page 1, 51h bits[9:7], APS is exited immediately. It is effective both for DCM and CCM operation. 10ns/LSB.

MFR_RESERVED (4Ch)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_APS_LEVEL_12P_R2 (4Dh)

The MFR_APS_LEVEL_12P_R2 command on Page 1 sets the rail 2 automatic phase-shedding (APS) current threshold for single-phase CCM and DCM operation.

Command	MFR_APS_LEVEL_12P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_APS_IIL_1P_CCM_R2	Sets the rail 2 APS current threshold for single-phase CCM. 1A/LSB.
7:0	MFR_APS_IIL_1P_DCM_R2	Sets the rail 2 APS current threshold for single-phase DCM. 1A/LSB.

MFR_RESERVED (4Eh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

OT_FAULT_LIMIT_R2 (4Fh)

The OT_FAULT_LIMIT_R2 command on Page 1 sets the over-temperature protection (OTP) operation and values.

Command	OT_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	MFR_OTP_LIMIT_R2	Over-temperature protection fault limit setting. If the junction temperature monitored on the TSENS3 pin exceeds OTP_LIMIT, the VR shuts off the disabled output. 1°C/LSB.

MFR_NVM_WP (50h)

The MFR_NVM_WP command on Page 1 enables NVM write protection.

Command	MFR_NVM_WP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	RESERVED	Fixed to 0x85.
7:0	MFR_NVM_WP	Enables NVM write protection. These bits are effective after cycling the power. 0x63: Enable NVM writing Others: Disable NVM writing

MFR_FS_DETECT_R2 (51h)

The MFR_FS_DETECT_R2 command on Page 1 sets rail 2 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_FS_DETECT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables the device to exit phase-shedding according to the PWM4 off time. The PWM minimum off time is excluded from the PWM off time (see Figure 1(a)). 1'b0: Disable PWM4 off-time detection to exit APS 1'b1: Enable PWM4 off-time detection to exit APS
10	FS_EXIT_APS_EN_NP	Enables the device to exit phase-shedding according to the multi-phase PWM interval time between consecutive phases. The time threshold is set by register 4Bh. The PWM blanking time is excluded from the PWM interval time. 1'b0: Disable multi-phase PWM interval time detection to exit APS 1'b1: Enable multi-phase PWM interval time detection to exit APS
9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count for the PWM4 off time condition to exit phase-shedding. If the PWM off time condition meets the counting threshold, the controller exits APS immediately.
6:3	RETURN_APS_DELAY	Sets the minimum full-phase runtime after exiting APS due to an FS limit event. 20μs/LSB.
2:0	FS_EXIT_APS_CNT_NP	Sets the continuous count of the multi-phase PWM interval time to exit phase-shedding. If the PWM interval condition meets the counting threshold, the controller exits APS immediately.

MFR_APS_CTRL_R2 (52h)

The MFR_APS_CTRL_R2 command on Page 1 sets rail 2 automatic phase-shedding (APS) timing and behaviors.

Command	MFR_APS_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:12	MFR_ADP_OC_NPS_EXIT_CNT_R2	Sets the period delay count from when OCP_PHASE is triggered to when the device exits APS. 100ns/LSB.

11	MFR_ADP_OC_NPS_EXIT_EN_R2	Enables OCP_PHASE protection to exit APS at any power state. 1'b0: Disable OCP_PHASE from triggering any phase to full-phase operation 1'b1: Enable the OCP_PHASE to trigger any phase to full-phase operation
10	MFR_ADP_PFM_EXIT_EN_R2	Enables the rail 2 frequency increasing condition to exit APS. 1'b0: Disable 1'b1: Enable
9	MFR_ADP_OC_1PS_ EXIT_EN_R2	Enables OCP_PHASE protection APS exiting for 1-phase DCM/CCM. 1'b0: Disable the OCP per-phase signal trigger for 1-phase DCM/CCM to enter full-phase operation 1'b1: Enable the OCP per-phase signal trigger 1-phase DCM/CCM to enter full-phase operation
8	MFR_ADP_UV_EXIT_ EN_R2	Sets a rail 2 condition (V_{FB} < VID - 25mV) to enter full-phase operation. 1'b0: Disable the rail 2 condition (V_{FB} < VID - 25mV) to enter full-phase operation 1'b1: Enable the rail 2 condition (V_{FB} < VID - 25mV) to enter full-phase operation
7:2	MFR_PS_ENTER_TIME_R2	Sets the phase-shedding delay time. When the reported load current is consecutively below the APS threshold for an APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE period, the controller enters APS mode and automatically sheds the phase count according to the load current.
1	MFR_PHASHED_EXIT_MOD_R2	Sets the phase-dropping mode during phase-shedding. The phase-shedding may be due to APS. 1'b0: Drop the phase count to the target count immediately 1'b1: Shed phases one by one with a configured delay time. The delay time is set with 54h bits[10:7].
0	MFR_AUTO_PS_EN_R2	Enables rail 2 APS mode. 1'b0: Disable rail 2 APS mode 1'b1: Enable rail 2 APS mode

MFR_APS_CTRL2_R2 (53h)

The MFR_APS_CTRL2_R2 command on Page 1 sets rail 2 APS timing and behaviors.

Command	MFR_APS_CTRL2_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:9	APS_COMP_CNT	The MP2926 provides positive compensation on VREF during phase-shedding to reduce the undershoot. Phase-shedding may be due to APS. The V_{REF} compensation is implemented by adding a PMBus-configurable positive voltage on COMP of the DC loop. After phase-shedding starts, the voltage returns 0V step by step with a time interval. APS_COMP_CNT sets the time interval between each step. 50ns/LSB.

8	DECAY_COMP_EN	Enables V_{REF} compensation while exiting decay mode. The MP2926 provides V_{REF} compensation while exiting decay mode. The compensation voltage level and resumed slew rate is the same with APS compensation. 1'b0: Disable V_{REF} compensation while exiting decay mode 1'b1: Enable V_{REF} compensation while exiting decay mode

7:4	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce undershoot. The compensation is added to V_{REF} when phase-shedding begins. 1.37mV/LSB.
3:0	MFR_APS_IHYS_R2	Sets the current hysteresis between phase-shedding and adding. It prevents back-and-forth phase-shedding when APS is enabled. 1A/LSB.

MFR_APS_CTRL3_R2 (54h)

The MFR_APS_CTRL3_R2 command on Page 1 sets rail 2 APS timing and behaviors.

Command	MFR_APS_CTRL3_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9									
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W									
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:7	MFR_PS_INTERVAL_R2	Sets the phase-by-phase dropping time intervals. It is only effective when bit[1] of 52h is set to 1. 2.5µs/LSB.
6:0	MFR_PRD_EXIT_APS_TIME_R2	Sets the period condition for holding the DC loop and current balance loop. If the absolute error between the set switching period and real switching period, $\|t_S - t_{SET}\|$ exceeds MFR_PRD_EXIT_APS_TIME x 80ns, the device holds the DC loop and current balance time for a given time. 80ns/LSB.

MFR_CUSTOMER_ID (55h)

The MFE_CUSTOMER_ID command on Page 1 sets the customer's code revision.

Command	MFR_CUSTOMER_ID															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	MFR_CUSTOMER_ID	Sets the customer's code revision.

MFR_FSCB_LOOP_CTRL_R2 (56h)

The MFR_FSCB_LOOP_CTRL_R2 command on Page 1 sets the rail 2 switching frequency and current balance loop.

Command	MFR_FSCB_LOOP_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	MFR_FS_LOOP_EN_R2	Switching frequency loop enable bit. The frequency loop keeps a constant switching frequency, and equals the setting value at different input voltages and load current values. This bit is active for both rails. 1'b0: Disable the frequency loop 1'b1: Enable the frequency loop
14	TRANS_HOLD_FS_EN_R2	Holds frequency loop regulation if a load transient event is detected (e.g. V_{FB} exceeds the V_{FB}+ window or V_{FB}- window). 1'b0: Disable holding frequency loop regulation if a load transient event is detected 1'b1: Enable holding frequency loop regulation if a load transient event is detected
13	PS_HOLD_FS_EN_R2	Holds the frequency loop regulation if the phase count changes. 1'b0: Disable holding frequency loop regulation if the phase count changes 1'b1: Enable holding frequency loop regulation if the phase count changes
12	DVID_HOLD_FS_EN_R2	Holds frequency loop regulation if DVID occurs. 1'b0: Disable holding frequency loop regulation if DVID occurs 1'b1: Enable holding frequency loop regulation if DVID occurs
11:8	MFR_FS_LOOP_CNT_R2	Sets the minimal holding time for the frequency loop if any load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set. 100μs/LSB.
7	MFR_CB_EN_R2	Enables the current balance loop. 1'b1: Enable the current balance loop 1'b0: Disable the current balance loop
6	PRD_HOLD_CB_EN_R2	This bit holds the current balance loop if the PWM period meets the PWM switching period condition set by PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disable holding the current balance loop if the PWM switching period condition is met 1'b1: Enable holding the current balance loop if the PWM switching period condition is met
5	PS_HOLD_CB_EN_R2	Holds the current balance loop if the phase number changes. 1'b0: Disable holding the current balance loop if the phase count changes 1'b1: Enable holding the current balance loop if the phase count changes
4	DVID_HOLD_CB_EN_R2	Holds the current balance loop if DVID occurs. 1'b0: Disable holding the current balance loop if DVID occurs 1'b1: Enable holding the current balance loop if DVID occurs
3:0	CB_LOOP_HOLD_TIME	Sets the current balance loop hold time. If any load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set, the current balance loop stops regulating for a time set with command CB_LOOP_THOLD. 100μs/LSB.

MFR_VOUT_LOOP_CTRL_R2 (57h)

The MFR_VOUT_LOOP_CTRL_R2 command on Page 1 sets the rail 2 V_{OUT} loop parameters.

Command	MFR_VOUT_LOOP_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	MFR_VDIFF_GAIN_SEL_R2	Selects the V_{DIFF} gain. If the output voltage exceeds 1.55V (the maximum sampling range of the internal ADC), select a half-gain. V_{OUT} has a 3V maximum. 1'b0: 1x 1'b1: 1/2x
9	MFR_DC_REF_SEL_R2	Sets the output voltage DC loop sensing point. 1'b 0: V_{FB} 1'b 1: V_{DIFF}
8	MFR_VCAL_PS2_EN_R2	Enables DC loop calibration during DCM operation. 1'b0: Disable 1'b1: Enable
7	MFR_VCAL_EN_R2	Enables DC loop calibration during both DCM and CCM operation. 1'b0: Disable 1'b1: Enable
6	PRD_HOLD_DC_EN_R2	Holds the DC loop if the PWM time interval meets the PWM switching period condition set by PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disable holding the DC loop if the PWM switching period condition is met 1'b1: Enable holding the DC loop if the PWM switching period condition is met
5	PS_HOLD_DC_EN_R2	Holds the DC loop if the phase count changes. 1'b0: Disable 1'b1: Enable
4	TRANS_HOLD_DC_EN_R2	Holds DC loop regulation if a load transient event is detected (e.g. V_{FB} exceeds the V_{FB}+ window or V_{FB}- window). 1'b0: Disable holding the DC loop if the V_{FB}± window condition is met 1'b1: Enable holding the DC loop if the V_{FB}± window condition is met
3:0	MFR_DC_LOOP_CNT_R2	Sets the DC loop minimum hold time in direct format. 200μs/LSB with a +100μs offset.

JOUT_SHORT_PK_R2 (58h)

The JOUT_SHORT_PK_R2 command returns the rail 2 peak J_{OUT} value in every short-term period.

Command	JOUT_SHORT_PK_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	JOUT_SHORT_PK_R2	Always returns the peak J_{OUT} value in every short-term period if J_{OUT} is enabled and GPIO_ACTIVE (68h) bit[13] is set to 1. If J_{OUT} is disabled or GPIO_ACTIVE (68h) bit[13] is set to 0, it returns the preset value.

JOUT_LONG_PK_R2 (59h)

The JOUT_LONG_PK_R2 command returns the rail 2 peak J_{OUT} value in every long-term period.

Command	JOUT_LONG_PK_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	JOUT_LONG_PK_R2	Always returns the peak J_{OUT} value in every long-term period if J_{OUT} is enabled and GPIO_ACTIVE (68h) bit[13] is set to 1. If J_{OUT} is disabled or GPIO_ACTIVE (68h) bit[13] is set to 0, it returns the preset value.

MFR_SLOPE_CNT_1P_R2 (5Ah)

The MFR_SLOPE_CNT_1P_R2 command on Page 1 sets the rail 2 slope voltage clamp time during single-phase operation.

Command	MFR_SLOPE_CNT_1P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	MFR_SLOPE_CNT_1P_R2	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_2P_R2 (5Bh)

The MFR_SLOPE_CNT_2P_R2 command on Page 1 sets the rail 2 slope voltage clamp time during 2-phase operation.

Command	MFR_SLOPE_CNT_2P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	RESERVED	Fixed to 0.
7:0	MFR_SLOPE_CNT_2P_R2	Sets the slope voltage clamp time. 5ns/LSB.

MFR_RESERVED (5Ch)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description

15:0	RESERVED	Fixed to 0.

MFR_SLOPE_CNT_DCM_PLUS_R2 (5Eh)

The MFR_SLOPE_CNT_DCM_PLUS_R2 command on Page 1 sets the slope voltage clamp time during DCM operation. It is for rail 2 only.

Command	MFR_SLOPE_CNT_DCM_PLUS_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:10	MFR_SLOPE_CNT_2P_PLUS_R2	The MSB of 2-phase count.
9:0	MFR_SLOPE_CNT_ DCM_R2	Sets the slope voltage clamp time. 5ns/LSB.

MFR_PG_DELAY_R2 (5Fh)

The MFR_PG_DELAY_R2 command on Page 1 sets the delay time for power good on and off.

Command	MFR_PG_DELAY_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:10	MFR_PGOFF_DELAY_ R2	Sets the power good off delay time. 5µs/LSB.
9:0	MFR_PGON_DELAY_R2	Sets the power good on delay time. 5µs/LSB.

TON_DELAY_R2 (60h)

The TON_DELAY_R2 command on Page 1 sets the delay time from when system initialization ends to when rail 2 VREF starts to boot up.

Command	TON_DELAY_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	TON_DELAY_R2	Sets the delay time from when system initialization ends to when VREF boots up. 100µs/LSB.

TON_RISE_R2 (61h)

The TON_RISE_R2 command on Page 1 sets the rail 2 reference voltage boot-up slew rate.

Command	TON_RISE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TON_RISE_R2	Sets the rail 2 boot-up slew rate during PMBus and PVID mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h) bit[15].

MFR_PWM_MIN_LIMIT1_R2 (62h)

The MFR_PWM_MIN_TIME1_R2 command on Page 1 sets the minimum pulse width when PWM is high, low, or in tri-state. It is for rail 2 only.

Command	MFR_PWM_MIN_LIMIT1_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	MFR_MIN_LOW_TIME_R2	Sets the minimum PWM low time. 10ns/LSB with a -5ns offset. The minimum PWM low time can be calculated with the following equation: (PWM_MIN_LOW_TIME x 10 - 5) ns
8:6	MFR_MINON_TIME_R2	Sets the minimum PWM high time. 10ns/LSB with a -5ns offset. The minimum PWM high time can be calculated with the following equation: (PWM_MIN_HIGH_TIME x 10 - 5) ns
5:0	MFR_MIN_HIZ_TIME_R2	Sets the minimum PWM tri-state time. 10ns/LSB with a -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: (PWM_MIN_TRI_TIME x 10 - 5) ns

MFR_PWM_MIN_TIME2_R2 (63h)

The MFR_PWM_MIN_TIME2_R2 command on Page 1 sets the PWM minimum off time. It is for rail 2 only.

Command	MFR_PWM_LIMIT2_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	TON_LIMIT_TO_VCAL	On the MP2926, the DC loop can be held if the PWM period meets the condition set by MFR_FS (33h, Page 0). If the calculated PWM on time is shorter than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	MFR_ZCD_EN_R2	Enable bit for rail 2 zero-current detection (ZCD). 1'b0: Disable zero-current detection (ZCD) 1'b1: Enable ZCD
8:5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4:0	MFR_MINOFF_TIME_R2	Sets the PWM minimum off time. 20ns/LSB with a 15ns offset. The PWM minimum off time can be calculated with the following equation: (PWM_MIN_OFF_TIME x 20 + 15) ns

TOFF_DELAY_R2 (64h)

The TOFF_DELAY_R2 command on Page 1 sets the rail 2 delay time from when EN goes low to a V_{REF} shutdown on rail 2.

Command	TOFF_DELAY_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	TOFF_DELAY_R2	Sets the delay time from when EN goes low to a V_{REF} shutdown. 100µs/LSB.

TOFF_FALL_R2 (65h)

The TOFF_FALL_R2 command on Page 1 sets the reference voltage transition down slew rate if rail 2 receives an OPERATION command for soft-off.

Command	TOFF_FALL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TOFF_FALL_R2	Set the rail 2 OPERATION command soft-off slew rate in PMBus and PVID mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h) bit[15].

MFR_RESEVED (66h)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

GPIO_SEL_GROUP4 (67h)

The GPIO_SEL_GROUP4 command on Page 1 sets the GPIO parameters.

Command	GPIO_SEL_GROUP4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:6	IO_SET_8LSB	Sets the VIMON3 buffer on the IMON3 pin. 2'b00: Disable buffer for VIMON3 2'b01: Enable buffer for VIMON3 Others: Invalid
5:4	IO_SET_8LSB	Sets the VIMON2 buffer on the IMON2 pin. 2'b00: Disable buffer for VIMON2 2'b01: Enable buffer for VIMON2 Others: Invalid
3:2	IO_SET_8LSB	Sets the VIMON1 buffer on the IMON1 pin. 2'b00: Disable buffer for VIMON1 2'b01: Enable buffer for VIMON1 Others: Invalid
1	IO_SET_8LSB	1'b0: Disable the VCS_REF buffer on the GPIO1 pin 1'b1: Enable the VCS_REF buffer on the GPIO1 pin
0	RESERVED	Fixed to 0.

GPIO_ACTIVE (68h)

The GPIO_ACTIVE command on Page 1 selects the active high/low output for GPIO.

Command	GPIO_ACTIVE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	GPIO_ALT_SEL	Sets the GPIO alert rail selection. 2'b00: Select the rail 1 signals for OCP_L, OCP_SPIKE, OCP_TDC, VRHOT#, J_{OUT} short-term alert, J_{OUT} long-term alert, I_{OUT} max alert, I_{OUT} min alert, V_{OUT} max alert, and V_{OUT} min alert on the GPIO pin if the related signals are muxed to GPIO 2'b01: Select the rail 2 signals for OCP_L, OCP_SPIKE, OCP_TDC, VRHOT#, J_{OUT} short-term alert, J_{OUT} long-term alert, I_{OUT} max alert, I_{OUT} min alert, V_{OUT} max alert, and V_{OUT} min alert on the GPIO pin if the related signals are muxed to GPIO 2'b10: Select the rail 3 signals for OCP_L, OCP_SPIKE, OCP_TDC, VRHOT#, J_{OUT} short-term alert, J_{OUT} long-term alert, I_{OUT} max alert, I_{OUT} min alert, V_{OUT} max alert. and V_{OUT} min alert on the GPIO pin if the related signals are muxed to GPIO 2'b11: Select the rail 3 signals for J_{OUT} short-term alert, J_{OUT} long-term alert, I_{OUT} max alert, I_{OUT} min alert, V_{OUT} max alert, and V_{OUT} min alert on the GPIO pin if related signals are muxed to GPIO. Select (OCP_L_R1, OCP_L_R2, and OCP_L_R3), (VRHOT#_R1, VRHOT#_R2, and VRHOT#_R3), (OCP_SPIKE_R1 || OCP_SPIKE_R2 || OCP_SPIKE_R3), and (OCP_TDC_R1 || OCP_TDC_R2 || OCP_TDC_R3) on the GPIO pin if the related signals are muxed to GPIO
13	PK_LATCH_EN	1'b0: The related registers in the Page 1 and Page 2 memory for J_{OUT} short-term, J_{OUT} long-term, I_{OUT} max, I_{OUT} min, V_{OUT} max, and V_{OUT} min can report the preset NVM values 1'b1: The related registers in the Page 1 and Page 2 memory for J_{OUT} short-term, J_{OUT} long-term, I_{OUT} max, I_{OUT} min, V_{OUT} max, and V_{OUT} min can report the latched peak values
12	POUT_ALERT_NO_ DELAY_EN	P_{OUT} alert no delay enable bit. 1'b0: One term delay for J_{OUT} alerts 1'b1: No delay for J_{OUT} alerts
11:10	RESERVED	Fixed to 0.
9	OTWARN_SEL	Fixed to 0
8	VRHOT3_SEL	Selects the OT_FAULT_R3 or VRHOT_R3 muxed to GPIO in VRHOT# functionality. 1'b0: OT_FAULT_R3 1'b1: VRHOT_R3
7	VRHOT2_SEL	Selects the OT_FAULT_R2 or VRHOT_R2 muxed to GPIO in VRHOT# functionality. 1'b0: OT_FAULT_R2 1'b1: VRHOT_R2
6	VRHOT1_SEL	Selects the OT_FAULT_R1 or VRHOT_R1 muxed to GPIO in VRHOT# functionality. 1'b0: OT_FAULT_R1 1'b1: VRHOT_R1
5:3	RESERVED	Fixed to 0.
2	IMON_SEL_R3	Selects the IMON current or buffered V_{IMON}. It is for rail 3 only. 1'b0: IMON current 1'b1: V_{IMON}
1	IMON_SEL_R2	Selects the IMON current or buffered V_{IMON}. It is for rail 2 only. 1'b0: IMON current 1'b1: V_{IMON}
0	IMON_SEL_R1	Selects the IMON current or buffered V_{IMON}. It is for rail 1 only. 1'b0: IMON current 1'b1: V_{IMON}

MFR_TEMP_CAL_R2 (69h)

The MFR_TEMP_CAL_R2 command on Page 1 sets the DrMOS temperature-sense gain and offset.

Command	MFR_TEMP_CAL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_TEMP_GAIN_R2	Sets the temperature-sense gain to transfer the voltage on the TSENS3 pin to a direct temperature in degrees Celsius.
7:0	MFR_TEMP_OFFSET_R2	Sets the temperature-sense offset to convert the voltage on the TSENS3 pin to a direct temperature in degrees Celsius. 1°C /LSB. Bit[7] is sign bit.

MFR_VOUT_CALC_R2 (6Ah)

The MFR_VOUT_CALC_R2 command on Page 1 sets the gain and offset of V_{OUT} calculations.

Command	MFR_VOUT_CALC_R2															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:8	MFR_VOUT_CALC_ OFFSET_R2	Adds an offset to V_{OUT} reporting in register READ_VOUT (8Bh). This bit is for the rail 2 output voltage report only. This bit is in two's complement format. Bit[13] is the sign bit. VID_STEP/LSB. When VID_STEP is 6.25mV, the voltage list below shows the direct value and the real-world value. 6'b00 0000: 0mV 6'b00 0001: +6.25mV 6'b01 1111: +193.75mV 6'b10 0000: -200mV 6'b10 0001: -193.75mV 6'b11 1111: -6.25mV
7:0	MFR_VOUT_CALC_ GAIN_R2	Sets the gain from the ADC-sensed VOSEN-VORTN voltage to the V_{OUT} report in register READ_VOUT (8Bh). This bit is for the rail 2 output voltage report only.

MFR_RESERVED (6Bh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

IOUT_CAL_GAIN_PMBUS_R2 (6Ch)

The IOUT_CAL_GAIN_PMBUS_R2 command on Page 1 sets the gain for PMBus output current reporting. The MP2926 senses the output current by sensing the voltage on the IMON pin. The reported output current is returned with PMBus command READ_IOUT (8Ch, Page 1).

Command	IOUT_CAL_GAIN_PMBUS_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:10	GAIN_SEL	Sets the exponent value for IOUT_CAL_GAIN calculations in this command.
9:0	MFR_IOUT_CALC_ GAIN_R2	Sets the current-sense (CS) gain for the PMBus report. The CS gain can be calculated with the following equation: $IOUT\_CAL\_GAIN=\frac{1023}{1.6}\times K_{CS}\times G_{IMON}\times R_{IMON}\times 2^{(6-GAIN\_SEL)}$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bits[11:10] in this command.

IOUT_CAL_OS_PMBUS_R2 (6Dh)

The IOUT_CAL_OS_PMBUS_R2 command on Page 1 sets the offset for the rail 2 PMBus output current report. The offset is for I_{OUT} over-reporting or under-reporting. The reported output current is returned with PMBus command READ_IOUT (8Ch, Page 1).

Command	IOUT_CAL_OS_PMBUS_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:6	IOUT_CAL_PH_OFS_R2	Adds an offset according the phase number. A larger phase number results in a larger offset. Bit[12] is the sign bit.
5:0	MFR_IOUT_CALC_ OFFSET_R2	Adds the current report offset to READ_IOUT (8Ch).

MFR_IMON_SET_R2 (6Eh)

The MFR_IMON_SET_R2 command on Page 1 sets some configurations for the internal IMON sense in PMBus mode. It is for rail 2 only.

Command	MFR_IMON_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:13	MFR_IMON_RES_SET_R2	Sets the IMON resistor for rail 2. 3'b 000: 2.5kΩ 3'b 001: 5kΩ 3'b 010: 10kΩ 3'b 011: 40kΩ 3'b1xx: Unconnected
12	MFR_IMON_GAIN_SET_R2	1'b0: The IMON1 current mirror gain is 1/8 1'b1: The IMON1 current mirror gain is 1/16
11	RESERVED	Fixed to 0.
10:0	MFR_TRIM_IMON_DIGI_GAIN_R2	Sets the digital calculating gain for I_{OUT} reporting. The gain is multiplied by the IMON ADC-sensed valued to form the final IMON digital-sense value. The IMON digital-sense value is used for PMBus output current reporting. The final IMON-sensed value can be calculated with the following equation: $IOUT\_PMBUS\_REPORT=1023\times\frac{I_{OUT}\times K_{CS}\times G_{IMON}\times R_{IMON}}{1.6}\times\frac{TRIM\_DIGI\_GAIN}{1024}\times\frac{2^{(6-GAIN\_SEL)}}{GAIN}$ Where I_{OUT} is the output current (in A), K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the IMON resistor (in Ω), and TRIM_DIGI_GAIN is a decimal value.

IOUT_MIN_ALERT_R2 (6Fh)

The IOUT_MIN_ALERT_R2 command on Page 1 returns the minimum value of I_{OUT} or its preset value. It is for rail 2 only. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	IOUT_MIN_ALERT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

9:0	IOUT_MIN_ALERT_R2	If GPIO_ACTIVE (68h) bit[13] is set to 0, 6Fh sets the DAC value of the I_{OUT} over-current (OC) warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, 6Fh returns the minimum I_{OUT} value. It can be written with a higher value. If a higher I_{OUT} is detected, this register is overwritten. To start a new recording, reset this bit by writing 0x03FF. Convert the read value to the actual output current (in A) with the following equation: $$I_{OUT}(A) = \frac{6Fh[9:0]}{6Ch[9:0] \times 1024} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$$ Where GAIN_SEL is 6Ch bits[11:10].

MFR_CONFIG_ID (70h)

The MFR_CONFIG_ID command on Page 1 programs the 4-digit part number suffix of the MP2926.

Command	MFR_CONFIG_ID															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	MFR_CONFIG_ID	Sets the 4-digit part number suffix setting.

MFR_PVID01_R2 (71h)

The MFR_PVID01_R2 command on Page 1 programs the rail 2 PVID voltage during PVID override mode.

Command	MFR_PVID01_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID1_R2	Sets the rail 2 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b001. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID0_R2	Sets the rail 2 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b000. It is in VID format. VID_STEP/LSB.

MFR_PVID23_R2 (72h)

The MFR_PVID23_R2 command on Page 1 programs the rail 2 PVID voltage during PVID override mode.

Command	MFR_PVID23_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID3_R2	Sets the rail 2 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b011. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID2_R2	Sets the rail 2 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b010. It is in VID format. VID_STEP/LSB.

MFR_PVID45_R2 (73h)

The MFR_PVID45_R2 command on Page 1 programs the rail 2 PVID voltage during PVID override mode.

Command	MFR_PVID45_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID5_R2	Sets the rail 2 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b101. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID4_R2	Sets the rail 2 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b100. It is in VID format. VID_STEP/LSB.

MFR_PVID67_R2 (74h)

The MFR_PVID67_R2 command on Page 1 programs the rail 2 PVID voltage during PVID override mode.

Command	MFR_PVID67_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID7_R2	Sets the rail 2 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b111. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID6_R2	Sets the rail 2 PVID voltage when the PVID2, PVID1, and PVID0 pins = 3'b110. It is in VID format. VID_STEP/LSB.

SAMPLE_INTERVAL_12PH_R2 (75h)

The SAMPLE_INTERVAL_12PH_R2 command sets the sample interval of 1-phase and 2-phase operation.

Command	SAMPLE_INTERVAL_12PH_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	SAMPLE_INTERVAL_2PH_R2	Sets the 2-phase sample interval. 50ns/LSB.
7:0	SAMPLE_INTERVAL_1PH_R2	Sets the 1-phase sample interval. 50ns/LSB.

MFR_RESERVED (76h)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (77h)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

STATUS_BYTE (78h)

The STATUS_BYTE command returns 1 byte of information with a summary of the most critical statuses and faults. This byte is shared with the STATUS_WORD (79h) register.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								X

Bits	Bit Name	Behavior	Description
7	NVM_BUSY	Live	Reports the live status of the NVM. 1’b0: The NVM is idle. The NVM can write and read with PMBus commands 1’b1: The NVM is busy. The NVM cannot write and read with PMBus commands
6	OFF	Live	The rail 2 output is off. This bit is in live mode. It is asserted if the rail 2 output is off. V_{OUT} turns off due to protections, EN going low, or VID = 0. 1’b0: VOUT2 is on 1’b1: VOUT2 is off

5	VOUT_OV_FAULT	Latch	Rail 2 V_{OUT} over-voltage (OV) fault indicator. This bit is set and latched if rail 2 OVP occurs. The CLEAR_FAULTS (03h) command can reset this bit. (Absolute or VID.) 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	Rail 2 I_{OUT} over-current (OC) fault indicator. This bit is set and latched if rail 2 OCP occurs. The CLEAR_FAULTS (03h) command can reset this bit. (OCP_TDC and OCP_SPIKE.) 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
3	VIN_UV_FAULT	Latch	V_{IN} under-voltage (UV) fault indicator. This bit is set and latched if V_{IN} UV fault occurs. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	TEMPERATURE	Latch	Over-temperature (OT) fault and warning indicator. This bit is set and latched if TSENS2 senses an OT condition, and OTP or an OT warning occurs. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Latch	PMBus communication fault indicator. If a PMBus communication fault occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	TSENS3_DIGI_FAULT	Latch	TSENS3 digital-sense fault indicator. If TSENS3 senses a voltage that exceeds or drops below the configurable level set by MFR_TSENS3_SET (36h, Page 1) bits[13:8], then a TSENS3 fault occurs and this bit is set and latched. The TSENS3 sense fault direction is determined by MFR_TSEN3_SET (36h, Page 1), bit[1]. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No TSENS3 digital-sense fault has occurred 1'b1: A TSENS3 digital-sense fault has occurred

STATUS_WORD (79h)

The STATUS_WORD (79h) command on Page 1 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher byte gives more detailed information of the fault conditions. The lower byte shares information with the STATUS_BYTE (78h) register.

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function						X	X		STATUS_BYTE(78H)							

Bits	Bit Name	Behavior	Description
15	VOUT	Live	Rail 2 V_{OUT} fault and warning indicator. If output over-voltage or under-voltage protection or warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} fault/warning has occurred 1'b1: A V_{OUT} fault/warning has occurred

14	IOUT	Live	Rail 2 I_{OUT} fault and warning indicator. If an output current fault/warning or output power warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No I_{OUT} fault/warning or output power warning has occurred 1'b1: An I_{OUT} fault/warning or output power warning has occurred
13	INPUT	Latch	Input voltage, current and power fault/warning indicator. Once any protection or warning of the input voltage, input current, or input power occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No input fault or warning has occurred 1'b1: An input fault or warning has occurred
12	TSENS2	Latch	TSENS2 digital-sense fault indicator. If the TSENS2 voltage exceeds 2.2V, the TSENS2 fault occurs, and this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No TSENS2 fault 1'b1: A TSENS2 fault has occurred
11	PG_NOT_ACTIVE	Live	1'b0: PG is active 1'b1: PG is not active
10:9	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
8	WATCH_DOG_OVF	Latch	Watchdog for the monitor block timer overflow indicator. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset. Meanwhile, this bit is set. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 1 returns 1 byte of information with the detailed V_{OUT} fault and warning status on rail 2.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X			X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Rail 2 V_{OUT} over-voltage (OV) fault indicator. If output OVP occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
6	VOUT_OV_WARNING	Live	Rail 2 V_{OUT} over-voltage (OV) warning indicator. If output OVP occurs, this bit is set. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} OV warning has occurred 1'b1: A V_{OUT} OV warning has occurred

5	VOUT_UV_WARNING	Live	Rail 2 output voltage under-voltage (UV) warning indicator. This bit is set if rail 1 UVP occurs. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} UV warning has occurred 1'b1: A V_{OUT} UV warning has occurred
4	VOUT_UV_FAULT	Latch	Rail 2 output voltage under-voltage (UV) fault indicator. This bit is set and latched if rail 1 UVP occurs. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN_ WARNING	Latch	Indicator for whether rail 2 V_{OUT} reaches VOUT_MAX or VOUT_MIN. If the VID value exceeds the value set in VOUT_MAX (24h, Page 0) and VOUT_MIN (2Bh, Page 0), this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID has exceeded VOUT_MAX or drops below VOUT_MIN
2	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
1	LINE_FLOAT	Latch	Rail 2 line float protection indicator. If a line float fault is detected, the device shuts down the associated rail and sets the LINE_FLOAT bit. It is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No line float fault 1'b1: Line float fault has happened
0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 1 returns 1 byte of information with the detailed I_{OUT} fault and warning statuses for rail 1.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function				X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Rail 2 output over-current (OC) fault indicator. Once output over-current protection occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. (OCP_TDC and OCP_SPIKE.) 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6	TDC_OCP_UV_FAULT	Latch	Rail 2 output over-current (OC) and under-voltage (UV) dual-fault indicator. If output OC occurs and the UV comparator is set simultaneously, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No output OC and UV fault has occurred 1'b1: Output OC has occurred and the UV comparator is set
5:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_INPUT (7Ch)

The STATUS_INPUT command returns 1 byte of information with detailed input faults and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X				X	X	

Bits	Bit Name	Behavior	Description
7	VIN_OVP	Latch	V_{IN} over-voltage (OV) fault indicator. Once the sensed V_{IN} exceeds the V_{IN} OV fault limit, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command on Page 1 returns 1 byte of information with temperature-related fault and warning conditions.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Over-temperature (OT) fault indicator. If the temperature sensed via TSENS3 exceeds the OT fault limit set by OT_FAULT_LIMIT (4F, Page 1), this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
6	VRHOT	Live	VRHOT indicator. If the temperature sensed via TSENS2 exceeds the over-temperature (OT) warning limit set by MFR_VRHOT_SET (3Eh, Page 1), this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No VRHOT has occurred 1'b1: VRHOT has occurred
5:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_CML (7Eh)

The STATUS_CML command on Page 1 returns 1 byte of information with PMBus communication faults.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function					X			

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	Invalid PMBus command indicator. This bit is set and latched when the MP2926 receives an unsupported command code. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	INVALID_DATA	Latch	Invalid PMBus data indicator. If the MP2926 receives unsupported data, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: An invalid PMBus data has been received
5	PEC_ERROR	Latch	PMBus PEC fault indicator. The PMBus interface supports the use of the packet error checking (PEC) byte defined in the SMBus standard. The PEC byte is transmitted by the MP2926 during a read transaction, or sent to the MP2926 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed and a PEC_FAULT is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4	NVM_CRC_ERROR	Latch	CRC fault indicator. While storing the operating memory data to the NVM, the MP2926 calculates a CRC code for each bit and saves the final CRC code to the NVM. While restoring the NVM data to the operating memory, the MP2926 recalculates the CRC code with each bit. The MP2926 checks the CRC results when the restoration process is complete. If the CRC result does not match what is stored, the VR shuts down and sets the CRC_FAULT bit. This bit is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
3	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
2	CML_FLT_TRG	Latch	If an NVM operation is blocked while the controller records a fault to the NVM, this bit is set. This bit is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No NVM operation is blocked 1'b1: NVM operation has been blocked because the controller is recording a fault to the NVM

1	CML_OTHER_FAULTS	Latch	This bit is set if any of the following PMBus communication faults occur: • Sending too few bits • Reading too few bits • Host sends or reads too few bytes • Reading too many bytes This bit is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit.
0	NVM_SIG_FAULTS	Latch	While restoring the data from the NVM to the memory, the device first checks the signature register in address 00h of the NVM. If the signature register is 0x1234, the restoration process is halted immediately, and this bit is set. This bit is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

READ_ADC_SUM (81h)

The READ_ADC_SUM command on Page 1 returns the sum of 16 consecutive ADC-sense results.

Command	READ_ADC_SUM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X		ADC_SUM													

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	ADC_SUM_READY	Indicates whether the sum of 16 consecutive ADC-sense results is ready. 1'b0: 16 ADC-sense result sum is not ready 1'b1: 16 ADC-sense result sum is ready
13:0	ADC_SUM	Stores the sum of 16 consecutive ADC-sense results. Send FBh (0 byte) to start the ADC sum action.

READ_VFB2_SENSE (82h)

The READ_VFB2_SENSE command on Page 1 returns the ADC-sensed V_{FB}.

Command	READ_VFB2_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_VFB_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_VFB_SENSE	Return the ADC-sensed V_{FB} in direct format. 1.56mV/LSB.

READ_TSENS2_SENSE (83h)

The READ_TSENS2_SENSE command reads the temperature-sense pin voltage.

Command	READ_TSENS2_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_TSENS2	Returns the ADC-sensed voltage on rail 2's TSENS2 pin in direct format. 1.56mV/LSB.

READ_VIN (88h)

The READ_VIN command on Page 1 provides 2 bytes to return the sensed V_{IN} based on the VINSEN pin in Linear11 format. In VID mode, the returned value must ignore bits[15:11] exponent value.

Command	READ_VIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	1	1	0	1	1	X	READ_VIN									

Bits	Bit Name	Description
15:11	EXP	Unused. Fixed to 11011.
10	RESERVED	Fixed to 0.
9:0	READ_VIN	Returns the sensed V_{IN} in Linear11 format. 31.25mV/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 1 returns the sensed rail 2 VOSEN-VORTN voltage. K_R is the dividing ratio of the divider.

Command	READ_VOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	READ_VOUT										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	READ_VOUT	Returns the V_{OUT} value. Linear mode: 2mV/LSB. V_{OUT} = READ_VOUT x 2 x K_R Direct mode: VID_STEP/LSB. V_{OUT} = READ_VOUT x VID_STEP x K_R VID_STEP is determined by C1h bits[15:14]. K_R is the dividing ratio of the divider.

READ_IOUT (8Ch)

The READ_IOUT command on Page 1 returns the sensed output current of rail 2 in direct format.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP					READ_IOUT										

Bits	Bit Name	Description
15:11	EXP	This bit is determined by bit[4] of VR_CONFIG1 (C1h). C1h[4] = 1: 5'b11110 C1h[4] = 0: 5'b11111
10:0	READ_IOUT	Return the sensed output current. This is determined by bit [4] of VR_CONFIG1 (C1h). C1h[4] = 1: Represents 0.25A/LSB C1h[4] = 0: Represents 0.5A/LSB

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 1 returns the sensed temperature on the TSENS2 pin in direct format.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	X	X	X	READ_TEMP							

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_TEMP	Returns the sensed temperature on the TSENS2 pin. 1°C/LSB.

READ_AD_RESULT (8Eh)

The READ_AD_RESULT command on Page 1 returns the ADC value.

Command	READ_AD_RESULT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_ADC									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_ADC	Returns the ADC value.

READ_VCOMP (8Fh)

The READ_VCOMP command on Page 1 returns the COMP value.

Command	READ_VCOMP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_VCOMP							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_VCOMP	Returns the COMP value.

READ_POUT (96h)

The READ_POUT command on Page 1 returns the P_{OUT} value of rail 2.

Command	READ_POUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:0	READ_POUT	Returns the output power. The read ADC value is the same as register D1h. Convert the read value to the actual power (in W) with the following equation: $$P_{OUT}(W) = \frac{\frac{READ\_POUT \times 8}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}}{t_{SHORT\_TERM}}$$ Where GAIN_SEL is 6Ch bits[11:10], G_{VIDFF} is the V_{DIFF} gain setting from 4Dh bit[10]: 4Dh[10] = 0: G_{VIDFF} = 1 4Dh[10] = 1: G_{VIDFF} = 0.5 t_{SHORT_TERM} is the short-term time (in µs): 26h[15] = 0: t_{SHORT_TERM} = 26h bits[12:1] x 0.05µs 26h[15] = 1: t_{SHORT_TERM} = (26h bits[6:0] + 1) x (Page 2) 55h bits[13:8] x 0.05µs

CAPABILITY (D0h)

The CAPABILITY command is read-only.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7:0	CAPABILITY	Fixed to 0xC0.

JOUT2_SHORT_TERM (D1h)

The JOUT2_SHORT_TERM command on Page 1 returns the real-time J_{OUT} value in every short-term period.

Command	JOUT2_SHORT_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT2_SHORT_TERM															

Bits	Bit Name	Description
15:0	JOUT2_SHORT_TERM	Returns the real-time J_{OUT} value in every short-term period. Convert the read value to the actual output (in µJ) with the following equation: $J_{OUT\_SHORT\_TERM}(\mu J) = \frac{D1h \times 8}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch bits[11:10], and G_{VIDFF} is the V_{DIFF} gain setting from 4Dh [10]. 4Dh[10] = 0: G_{VDIFF} = 1 4Dh[10] = 1: G_{VDIFF} = 0.5

JOUT2_LONG_TERM (D2h)

The JOUT2_LONG_TERM command on Page 1 returns the J_{OUT} value in every long-term period.

Command	JOUT2_LONG_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT2_LONG_TERM															

Bits	Bit Name	Description
15:0	JOUT2_LONG_TERM	Returns the real-time J_{OUT} value in every long-term period. Convert the read value to the actual output (in mJ) with the following equation: $J_{OUT\_LONG\_TERM}(mJ) = \frac{D2h \times 16.384}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch bits[11:10], and G_{VIDFF} is the V_{DIFF} gain setting from 4Dh bit[10]: 4Dh[10] = 0: G_{VIDFF} = 1 4Dh[10] = 1: G_{VIDFF} = 0.5

IMON2_FAST_SENSE (D3h)

The IMON2_FAST_SENSE command on Page 1 returns the J_{OUT} ADC value.

Command	IMON2_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	IMON2_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IMON2_FAST_SENSE	Returns the I_{OUT} ADC value in J_{OUT} calculations. Convert the read value to the actual output (in A) with the following equation: $$I_{OUT}(A) = \frac{D3h[9:0]}{6Ch[9:0] \times 1024} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$$ Where GAIN_SEL is 6Ch bits[11:10].

VDIFF2_FAST_SENSE (D4h)

The VDIFF2_FAST_SENSE command on Page 1 returns the J_{OUT} ADC value.

Command	VDIFF2_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	VDIFF2_FAST_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VDIFF2_FAST_SENSE	Returns the V_{OUT} ADC value in J_{OUT} calculations. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 1) bit[10].

DIE_TEMP_SENSE (D5h)

The DIE_TEMP_SENSE command on Page 1 returns the die temperature ADC value.

Command	DIE_TEMP_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	DIE_TEMP_SENSE	Returns the die temperature ADC data. 1.5625mV/LSB. Convert the read value to the actual die temperature (in °C) with the following equation: $$T_{DIE\_TEMP}(°C) = \frac{D5h[9:0] \times 1.5625mV - 275mV}{3}$$

FAULTS_REPORT1 (E0h)

The FAULTS_REPORT1 command on Page 1 returns the protection information of the MP2926. This information is lost after the device powers off.

Command	FAULTS_REPORT1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X			X	X										

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	CS5_FAULT_FLAG	CS5 fault indicator. This bit is set to 1 when CS5 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
12	CS6_FAULT_FLAG	CS6 fault indicator. This bit is set to 1 when CS6 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
11:10	RESERVED	X indicates that writes are ignored and reads are always 0.
9	CS3_FAULT_FLAG	CS3 fault indicator. This bit is set to 1 when CS3 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
8	CS4_FAULT_FLAG	CS4 fault indicator. This bit is set to 1 when CS4 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
7:2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1	CS2_FAULT_FLAG	CS2 fault indicator. This bit is set to 1 when CS2 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred
0	CS1_FAULT_FLAG	CS1 fault indicator. This bit is set to 1 when CS1 is pulled low. 1'b0: No CS fault has occurred 1'b1: A CS fault has occurred

FAULTS_REPORT2 (E1h)

The FAULTS_REPORT2 command on Page 1 returns protection information for the MP2926. This information is lost after the device powers off.

Command	FAULTS_REPORT2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	OTP_R2	Rail 2 V_{OUT} over-temperature protection (OTP) fault indicator. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
12	OCP_TDC_R2	Rail 2 V_{OUT} over-current (OC_TDC) fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred 1'b1: A V_{OUT} OC_TDC fault has occurred
11	OCP_SPIKE_R2	Rail 2 V_{OUT} OC_SPIKE fault indicator. 1'b0: No V_{OUT} OC_SPIKE fault has occurred 1'b1: A V_{OUT} OC_SPIKE fault has occurred

10	UVP_R2	Rail 2 V_{OUT} under-voltage protection (UVP) indicator. 1'b0: No V_{OUT} UVP fault has occurred on rail 2 1'b1: A V_{OUT} UVP fault has occurred on rail 2
9	VID_OVP_R2	Rail 2 V_{OUT} over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} VID OVP absolute fault has occurred on rail 2 1'b1: A V_{OUT} VID OVP absolute fault has occurred on rail 2
8	ABSOLUTE_OVP_R2	Rail 2 V_{OUT} over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} OVP absolute fault has occurred on rail 2 1'b1: A V_{OUT} OVP absolute fault has occurred on rail 2
7:6	RESERVED	Fixed to 0.
5	OTP_R1	Rail 1 V_{OUT} over-temperature protection (OTP) fault indicator. 1'b0: No OTP fault has occurred on rail 1 1'b1: An OTP fault has occurred on rail 1
4	OCP_TDC_R1	Rail 1 V_{OUT} over-current (OC_TDC) fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred on rail 1 1'b1: A V_{OUT} OC_TDC fault has occurred on rail 1
3	OCP_SPIKE_R1	Rail 1 V_{OUT} over-current (OC_SPIKE) fault indicator. 1'b0: No V_{OUT} OC_SPIKE fault has occurred on rail 1 1'b1: A V_{OUT} OC_SPIKE fault has occurred on rail 1
2	UVP_R1	Rail 1 V_{OUT} under-voltage protection (UVP) indicator. 1'b0: No V_{OUT} UVP fault has occurred on rail 1 1'b1: A V_{OUT} UVP fault has occurred on rail 1
1	VID_OVP_R1	Rail 1 V_{OUT} over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} VID OVP absolute fault has occurred on rail 1 1'b1: A V_{OUT} VID OVP absolute fault has occurred on rail 1
0	ABSOLUTE_OVP_R1	Rail 1 V_{OUT} over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} OVP absolute fault has occurred on rail 1 1'b1: A V_{OUT} OVP absolute fault has occurred on rail 1

FAULTS_REPORT3 (E2h)

The FAULTS_REPORT3 command on Page 1 returns the protect information for the MP2926. This information is lost after the device powers off.

Command	FAULTS_REPORT3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM1_FAULTS				PWM2_FAULTS											

Bits	Bit Name	Description
15:12	PWM1_FAULTS	Intelli-Phase™ fault type indication for 1-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

11:8	PWM2_FAULTS	Intelli-Phase™ fault type indication for 2-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:0	RESERVED	Fixed to 0.

FAULTS_REPORT4 (E3h)

The FAULTS_REPORT4 command on Page 1 returns the protection information for the MP2926. This information is lost after the device powers off.

Command	FAULTS_REPORT4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

FAULTS_REPORT5 (E4h)

The FAULTS_REPORT5 command on Page 1 returns the protection information for the MP2926. This information is lost after the device powers off.

Command	FAULTS_REPORT5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:12	PWM3_FAULTS	Intelli-Phase™ fault type indication for 3-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM4_FAULTS	Intelli-Phase™ fault type indication for 4-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM5_FAULTS	Intelli-Phase™ fault type indication for 5-pahse operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

3:0	PWM6_FAULTS	Intelli-Phase™ fault type indication for 6-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULTS_REPORT6 (E5h)

The FAULTS_REPORT5 command on Page 1 returns the protection information for the MP2926. This information is lost after the device powers off.

Command	FAULTS_REPORT2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:13	RESERVED	Fixed to 0.
12	TSENS3_ADC_OTP	TSENS3 ADC over-temperature protection (OTP) indicator. 1'b0: No TSENS3 ADC OTP fault has occurred 1'b1: A TSENS3 ADC OTP fault has occurred
11	CHIP_OTP_FLAG	Chip over-temperature protection (OTP) indicator. 1'b0: No chip OTP fault has occurred 1'b1: A chip OTP fault has occurred
10	VIN_UVP	V_{IN} under-voltage protection (UVP) indicator. 1'b0: No V_{IN} UVP fault has occurred 1'b1: A V_{IN} UVP fault has occurred
9	VIN_OVP	V_{IN} over-voltage protection (OVP) indicator. 1'b0: No V_{IN} OVP fault has occurred 1'b1: A V_{IN} OVP has occurred
8	VIN_UVLO	V_{IN} under-voltage lockout (UVLO) indicator. 1'b0: No V_{IN} UVLO fault has occurred 1'b1: A V_{IN} UVLO fault has occurred
7:6	RESERVED	Fixed to 0.
5	OTP_R3	Rail 3 V_{OUT} over-temperature protection (OTP) fault indicator. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
4	OCP_TDC_R3	Rail 3 V_{OUT} over-current (OC_TDC) fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred 1'b1: A V_{OUT} OC_TDC fault has occurred
3	OCP_SPIKE_R3	Rail 3 V_{OUT} over-current (OC_SPIKE) fault indicator. 1'b0: No V_{OUT} OC_SPIKE fault has occurred 1'b1: A V_{OUT} OC_SPIKE fault has occurred
2	UVP_R3	Rail 3 V_{OUT} under-voltage protection (UVP) indicator. 1'b0: No V_{OUT} UVP fault has occurred on rail 3 1'b1: A V_{OUT} UVP fault has occurred on rail 3

1	VID_OVP_R3	Rail 3 V_{OUT} over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} VID OVP absolute fault has occurred on rail 3 1'b1: A V_{OUT} VID OVP absolute fault has occurred on rail 3
0	ABSOLUTE_OVP_R3	Rail 3 V_{OUT} over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} OVP absolute fault has occurred on rail 3 1'b1: A V_{OUT} OVP absolute fault has occurred on rail 3

FAULTS_RECORD1 (F0h)

The FAULTS_RECORD1 command on Page 1 records the latest fault information for the MP2926.

Command	FAULTS_RECORD1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X			X	X										

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	CS5_FAULT_FLAG	CS5 fault indicator. This bit is set to 1 when CS5 is pulled low. 1'b0: No CS5 fault has occurred 1'b1: A CS5 fault has occurred
12	CS6_FAULT_FLAG	CS6 fault indicator. This bit is set to 1 when CS6 is pulled low. 1'b0: No CS6 fault has occurred 1'b1: A CS6 fault has occurred
11:10	RESERVED	X indicates that writes are ignored and reads are always 0.
9	CS3_FAULT_FLAG	CS3 fault indicator. This bit is set to 1 when CS3 is pulled low. 1'b0: No CS3 fault has occurred 1'b1: A CS3 fault has occurred
8	CS4_FAULT_FLAG	CS4 fault indicator. This bit is set to 1 when CS4 is pulled low. 1'b0: No CS4 fault has occurred 1'b1: A CS4 fault has occurred
7:2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1	CS2_FAULT_FLAG	CS2 fault indicator. This bit is set to 1 when CS2 is pulled low. 1'b0: No CS2 fault has occurred 1'b1: A CS2 fault has occurred
0	CS1_FAULT_FLAG	CS1 fault indicator. This bit is set to 1 when CS1 is pulled low. 1'b0: No CS1 fault has occurred 1'b1: A CS1 fault has occurred

FAULTS_RECORD2 (F1h)

The FAULTS_RECORD2 command on Page 1 records the latest fault information for the MP2926

Command	FAULTS_RECORD2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	OTP_R2	Rail 2 V_{OUT} over-temperature protection (OTP) fault indicator. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
12	OCP_TDC_R2	Rail 2 V_{OUT} over-current (OC_TDC) fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred 1'b1: A V_{OUT} OC_TDC fault has occurred
11	OCP_SPIKE_R2	Rail 2 V_{OUT} over-current (OC_SPIKE) fault indicator. 1'b0: No V_{OUT} OC_SPIKE fault has occurred 1'b1: A V_{OUT} OC_SPIKE fault has occurred
10	UVP_R2	Rail 2 V_{OUT} under-voltage protection (UVP) fault indicator. 1'b0: No V_{OUT} UVP fault has occurred 1'b1: A V_{OUT} UVP fault has occurred
9	VID_OVP_R2	Rail 2 V_{OUT} over-voltage protection (OVP) fault indicator. 1'b0: No V_{OUT} VID OVP absolute fault has occurred 1'b1: A V_{OUT} VID OVP absolute fault has occurred
8	ABSOLUTE_OVP_R2	Rail 2 V_{OUT} over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} OVP absolute fault has occurred 1'b1: A V_{OUT} OVP absolute fault has occurred
7:6	RESERVED	Fixed to 0.
5	OTP_R1	Rail 1 V_{OUT} over-temperature protection (OTP) fault indicator. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
4	OCP_TDC_R1	Rail 1 V_{OUT} over-current (OC_TDC) fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred 1'b1: A V_{OUT} OC_TDC fault has occurred
3	OCP_SPIKE_R1	Rail 1 V_{OUT} over-current (OC_SPIKE) fault indicator. 1'b0: No V_{OUT} OC_SPIKE fault has occurred 1'b1: A V_{OUT} OC_SPIKE fault has occurred
2	UVP_R1	Rail 1 V_{OUT} under-voltage protection (UVP) fault indicator. 1'b0: No V_{OUT} UVP fault has occurred 1'b1: A V_{OUT} UVP fault has occurred
1	VID_OVP_R1	Rail 1 V_{OUT} over-voltage protection (OVP) fault indicator. 1'b0: No V_{OUT} VID OVP absolute fault has occurred 1'b1: A V_{OUT} VID OVP absolute fault has occurred
0	ABSOLUTE_OVP_R1	Rail 1 V_{OUT} over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} OVP absolute fault has occurred 1'b1: A V_{OUT} OVP absolute fault has occurred

FAULTS_RECORD3 (F2h)

The FAULTS_RECORD3 command on Page 1 records the latest fault information for the MP2926.

Command	FAULTS_RECORD3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:12	PWM1_FAULTS	Intelli-Phase™ fault type indication for 1-phase operation. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
11:8	PWM2_FAULTS	Intelli-Phase™ fault type indication for 2-phase operation. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
7:0	RESERVED	Fixed to 0.

FAULTS_RECORD4 (F3h)

The FAULTS_RECORD4 command on Page 1 records the latest fault information for the MP2926.

Command	FAULTS_RECORD4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

FAULTS_RECORD5 (F4h)

The FAULTS_RECORD5 command on Page 1 records the latest fault information for the MP2926.

Command	FAULTS_RECORD5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:12	PWM3_FAULTS	Intelli-Phase™ fault type indication for 3-phase operation. 4’b0000: No fault 4’b0001: VIN-SW short 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection

11:8	PWM4_FAULTS	Intelli-Phase™ fault type indication for 4-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM5_FAULTS	Intelli-Phase™ fault type indication for 5-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM6_FAULTS	Intelli-Phase™ fault type indication for 6-phase operation. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULTS_RECORD6 (F5h)

The FAULTS_RECORD6 command on Page 1 records the latest fault information for the MP2926.

Command	FAULTS_RECORD6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Fixed to 0.
12	TSENS3_ADC_OTP	TSENS3 ADC over-temperature protection (OTP) indicator. 1'b0: No TSENS3 ADC OTP fault has occurred 1'b1: A TSENS3 ADC OTP fault has occurred
11	CHIP_OTP_FLAG	Chip over-temperature protection (OTP) indicator. 1'b0: No chip OTP fault has occurred 1'b1: A chip OTP fault has occurred
10	VIN UVP	Rail 1 V_{IN} under-voltage protection (UVP) indicator. 1'b0: No V_{IN} UVP fault has occurred 1'b1: A V_{IN} UVP fault has occurred
9	VIN OVP	Rail 1 V_{IN} over-voltage protection (OVP) indicator. 1'b0: No V_{IN} OVP fault has occurred 1'b1: A V_{IN} OVP fault has occurred
8	VIN UVLO	V_{IN} under-voltage lockout (UVLO) indicator. 1'b0: No V_{IN} UVLO fault has occurred 1'b1: A V_{IN} UVLO fault has occurred
7:6	RESERVED	Fixed to 0.
5	OTP_R3	Rail 3 V_{OUT} over-temperature protection (OTP) fault indicator. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred

4	OCP_TDC_R3	Rail 3 V_{OUT} over-current (OC_TDC) fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred 1'b1: A V_{OUT} OC_TDC fault has occurred
3	OCP_SPIKE_R3	Rail 3 V_{OUT} over-current (OC_SPIKE) fault indicator. 1'b0: No V_{OUT} OC_SPIKE fault has occurred 1'b1: A V_{OUT} OC_SPIKE fault has occurred
2	UVP_R3	Rail 3 V_{OUT} under-voltage protection (UVP) fault indicator. 1'b0: No V_{OUT} UVP fault has occurred 1'b1: A V_{OUT} UVP fault has occurred
1	VID_OVP_R3	Rail 3 V_{OUT} over-voltage protection (OVP) fault indicator. 1'b0: No V_{OUT} VID OVP absolute fault has occurred 1'b1: A V_{OUT} VID OVP absolute fault has occurred
0	ABSOLUTE_OVP_R3	Rail 3 V_{OUT} over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} OVP absolute fault has occurred 1'b1: A V_{OUT} OVP absolute fault has occurred

ADC_SUM_RESET (FBh)

The ADC_SUM_RESET command resets the ADC_SUM count.

This command is write-only. There is no data byte for this command.

CLEAR_CRC_FAULT (FCh)

The CLEAR_CRC_FAULT command clears the CRC fault information that is stored in NVM.

This command is write-only. There is no data byte for this command.

STORE_ALL_AAH (FDh)

The STORE_ALL_AAH command is used for test mode. This command erases the stored NVM cells' value. This command cannot be sent. It can be ignored if the NVM is write-protected (50h bits[7:0] ≠ 0x63).

CLEAR_STORED_FAULTS (FEh)

The CLEAR_STORED_FAULTS command clears the last fault information that is stored in NVM.

This command is write-only. There is no data byte for this command.

CLEAR_NVM_FAULTS (FFh)

The CLEAR_NVM_FAULTS command clears the NVM faults.

This command is write-only. There is no data byte for this command.

PAGE 2 REGISTER MAP

OPERATION_R3 (01h)

The OPERATION_R3 command on Page 2 turns the rail 3 output on or off in conjunction with the input from the EN pin, and sets the output voltage to the upper or lower margin voltages. The controller stays in the OPERATION command setting mode until a subsequent OPERATION command is received, or a change in the EN state changes rail 3 to another mode.

Command	OPERATION_R3							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								

Bits	Bit Name	Description
7:0	OPERATION_R3	Sets the operation mode for rail 3. 8’b 00xx xxxx: Hi-Z off 8’b 01xx xxxx: Soft off 8’b 1000 xxxx: Normal on 8’b 1001 xxxx: Margin low 8’b 1010 xxxx: Margin high Others: Invalid commands “x” means not applicable.

STORE_ALL_CODE (15h)

The STORE_ALL_CODE command instructs the PMBus device to copy all Page 0, Page 1, and Page 2 contents, including internal trim registers of the operating memory, to the matching locations in the NVM. Any items in the operating memory that do not have matching locations in the user store are ignored.

This command is controlled by 50h (Page 1) bits[7:0]. When bits[7:0] is set to 0x63, the NVM can accept writes. The NVM is write-protected for all other values.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents, including internal trim registers, from the NVM, and overwrites the matching locations in the operating memory. Any items in the user store that do not have matching locations in the operating memory are ignored.

While the device is outputting power, this command is ignored and cannot be used. This command is write-only. There is no data byte for this command.

STORE_USER_CODE (17h)

The STORE_USER_CODE command instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents of the operating memory to the matching locations in the NVM, except the internal trim registers. Any items in the operating memory that do not have matching locations in the user store are ignored.

This command is controlled by 50h (Page 1) bits[7:0]. When bits[7:0] is set to 0x63, the NVM can accept writes. The NVM is write-protected for all other values.

This command can be used while the device is outputting power. This command is write-only. There is no data byte for this command.

RESTORE_USER_CODE (18h)

The RESTORE_USER_CODE command instructs the PMBus device to copy the Page 0, Page 1, and Page 2 contents from the NVM, and overwrites the matching locations in the operating memory. Trim registers are not overwritten by this command.

While the device is outputting power, this command is ignored and cannot be used. This command is write-only. There is no data byte for this command.

VOUT_COMMAND_R3 (21h)

The VOUT_COMMAND_R2 on Page 2 sets the rail 3 VID reference voltage in PMBus override mode.

Command	VOUT_COMMAND_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_COMMAND_R3	Sets the rail 3 reference voltage (the VID_DAC output voltage) in PMBus VID mode. VID_STEP/LSB VID_STEP. It is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].

VOUT_TRIM_R3 (22h)

The VOUT_TRIM_R3 command on Page 2 applies a fixed offset voltage to the output voltage command value. It is for rail 3 only.

Command	VOUT_TRIM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRIM_R3	Sets the V_{OUT} offset value. VID_STEP/LSB.

VDIFF1_SNAPSHOT (23h)

The VDIFF1_SNAPSHOT command on Page 2 returns the snapshot (Page 0) D4h value while reading the (Page 0) D3h value.

Command	VDIFF1_SNAPSHOT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

9:0	VDIFF1_SNAPSHOT	Returns the snapshot V_{OUT} ADC value at the time of read (Page 0) D3h. The value is updated to the (Page 0) D4h value while reading (Page 0) D3h. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 1) bit[10].

VOUT_MAX_R3 (24h)

The VOUT_MAX_R3 command on Page 2 sets the maximum rail 3 VID-DAC reference voltage, so as to set the maximum output voltage. When an external resistor divider is applied, the maximum voltage is clamped to VOUT_MAX / K_R. K_R is the dividing ratio of the external resistor divider. It is effective in PMBus VID mode and all PVID modes.

Command	VOUT_MAX_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MAX_R3	Sets the rail 3 maximum VID + offset voltage. It limits the sum of VID + VOUT_TRIM offset. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].

MFR_JOUT_LONG_TERM_R3 (25h)

The MFR_JOUT_LONG_TERM_R3 command on Page 2 sets the long-term value to calculate the rail 3 J_{OUT} value.

Command	MFR_JOUT_LONG_TERM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	JOUT_LONG_TERM	Sets the long-term value for J_{OUT} calculations. LONG_TIME = JOUT_LONG_TERM x SHORT_TIME

MFR_JOUT_SHORT_TERM_R3 (26h)

The MFR_JOUT_SHORT_TERM_R3 command on Page 2 sets the short-term value to calculate the rail 3 J_{OUT} value.

Command	MFR_JOUT_SHORT_TERM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	JOUT_EN	Enable bit for J_{OUT} functionality. 1'b1: Enabled 1'b0: Disabled
12:7	JOUT_SHORT_TERM_FIX_FREQ	Fixed to 0 in fixed-frequency mode.
6:0		Sets JOUT_SHORT_TERM in fixed-frequency mode. ADC_TIME/LSB. The short-term period can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_FIX_FREQ x ADC_TIME
12:1	JOUT_SHORT_TERM_ADAPTIVE_FREQ	50ns/LSB in adaptive frequency mode. The short-term period can be calculated with the following equation: SHORT_TIME = JOUT_SHORT_TERM_ADAPTIVE_FREQ x 50ns
0		Fixed to 0 in adaptive frequency mode.

VOUT_TRANSITION_RATE_R3 (27h)

The VOUT_TRANSITION_RATE_R3 command on Page 2 sets the rail 3 dynamic VID transition slew rate in PMBus and PVID mode.

Command	VOUT_TRANSITION_RATE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	VOUT_TRANSITION_RATE_R3	Sets the rail 3 dynamic VID transition slew rate in PMBus and PVID mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h) bit[15].

VOUT_DROOP_R3 (28h)

The VOUT_DROOP_R3 on Page 2 sets the load-line configuration for rail 3.

Command	VOUT_DROOP_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	IACDROOP_BW_SET_R3	Enable bit to increase the AC droop BW by increasing the bias current. This is for rail 3 only. 1'b0: Disabled 1'b1: Enabled
14	IACDROOP_BW_SET_R3	Enable bit to increase the AC droop BW by reducing the compensation capacitor. This is for rail 3 only. 1'b0: Disabled 1'b1: Enabled

13	IACDROOP_GAIN2_SET_R3	Sets the PMBus AC droop's second current mirror ratio (GAIN2) for rail 3. It is active when bit [12] = 1. 1'b0: 1 1'b1: 1/2
12	MFR_ACLL_EN_R3	AC or DC load line selection bit. 1'b0: DC load line 1'b1: AC load line
11:9	IDROOP_GAIN2 _R3	Sets the PMBus DC droop's second current mirror ratio (GAIN2) for rail 3. It is active when bit [12] = 0. The MP2926 provides eight configurable levels. 3'b000: 0 3'b001: 3/4 3'b010: 4/4 3'b011: 5/4 3'b100: 6/4 3'b101: 7/4 3'b110: 8/4 3'b111: 9/4
8:7	IDROOP_GAIN1_ R3	Sets the PMBus I_{DROOP} first current mirror ratio (GAIN1) for rail 3. The initial load line slope can be calculated with the following equation: $R_{LL\_INI} = R_{DROOP} \times K_{CS} \times GAIN1 \times GAIN2$ 2'b00: 1/16 2'b01: 1/8 2'b10: 1/4 2'b11: 1/2
6	SHORT_FIRST_HALF_ R3	1'b0: Do not short the first half of resistors for rail 3 1'b1: Short the first half of resistors for rail 3 Set this bit to 1 if R_{DROOP} is below 3.2kΩ.
5:0	RDROOP_SET_R2	Sets R_{DROOP} for rail 3. 100Ω/LSB. 6.4kΩ maximum.

VOUT_SCALE_LOOP_R3 (29h)

The VOUT_SCALE_LOOP_R3 command on Page 2 sets the rail 3 output voltage to reference voltage dividing ratio when an external output divider is applied.

Command	VOUT_SCALE_LOOP_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	**Bit Name**	**Description**
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VOUT_SCALE_LOOP_ R3	Set the rail 3 output voltage to reference voltage dividing ratio. V_{REF} ranges from 0V to 1.55V.

MFR_SETTLE_CTRL_R3 (2Ah)

The MFR_SETTLE_CTRL_R3 command on Page 2 sets the DVID parameters.

Command	MFR_SETTLE_CTRL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Function			

Bits	Bit Name	Description
15:11	MFR_DROOPFALL_ DELAY_R3	Sets the delay time between V_{REF} reaching the target (VID + DROOP_VID) and V_{REF} falling back to VID. 50ns/LSB.
10:6	MFR_RISE_STEP_R3	Sets the extra VID step count for rail 1 when DVID is up. The extra VID steps compensate the droop caused by the output capacitor charging when DVID is up. 1 step/LSB.
5:0	RESERVED	Fixed to 0.

VOUT_MIN_R3 (2Bh)

The VOUT_MIN_R3 command on Page 2 instructs the device to limit the rail 3 minimum output voltage in PMBus and PVID mode. If the output voltage decoded from the PMBus interface or set by the PVID registers is below what is set by VOUT_MIN (2Bh), the output voltage is clamped to VOUT_MIN. When an external resistor divider is applied on VOSEN, the minimum output voltage is clamped to VOUT_MIN / K_R. K_R is the dividing ratio of the divider.

Command	VOUT_MIN_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VOUT_MIN_R3	Sets the minimum VID in PMBus mode for rail 3. Any VID below this value is clamped to VOUT_MIN. VID_STEP/LSB. VID_STEP is determined by MFR_VR_CONFIG1 (C1h) bits[15:14].

MFR_TRIM_DCM_1P_2P_R3 (2Ch)

The MFR_TRIM_DCM_1P_2P_R3 command on Page 2 trims the output voltage during 2-phase CCM, and 1-phase CCM and DCM power state of rail 3.

Command	MFR_TRIM_DCM_1P_2P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	MFR_TRIM_2PS_R3	Sets the V_{OUT} trim for 2-phase CCM operation. 2.3mV/LSB.
9:5	MFR_TRIM_1PS_R3	Sets the V_{OUT} trim for 1-phase CCM operation. 2.3mV/LSB.
4:0	MFR_TRIM_DCM_R3	Sets the V_{OUT} trim for 1-phase DCM operation. 2.3mV/LSB.

MFR_PMBUS_VTH (2Dh)

The MFR_PMBUS_VTH command sets the PMBus logic level.

Command	MFR_PMBUS_VTH															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	MFR_PMB_THH_SET	0V to 2.56V. 40mV/LSB.
5:0	MFR_PMB_THL_SET	0V to 2.56V. 40mV/LSB.

MFR_RESERVED (2Eh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (2Fh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (30h)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_BLANK_TIME1_R3 (31h)

The MFR_BLANK_TIME1_R3 command on Page 2 programs the slope compensation reset time and the PWM blanking time between two consecutive phases. It is for rail 3 only.

Command	MFR_BLANK_TIME1_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	MFR_SLOPE_BLANK_TIME1_R3	Programs the slope compensation reset time. The slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME (MFR_BLANK_TIME1 (31h, Page 2) bits[5:0]). 5ns/LSB.
5:0	MFR_PHASE_BLANK_TIME1_R3	Programs the first set of PWM blanking times between two consecutive phases. 5ns/LSB.

MFR_PI_LOOP (32h)

The MFR_PI_LOOP sets integral parameters for the current balance loop and DC loop.

Command	MFR_PI_LOOP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:11	FREQUENCY_LOOP	Sets the frequency loop parameters. The default is 2.
10:7	CURRENT_LOOP	Sets the current share loop parameters. The default is 2.
6:0	VOUT_DC_LOOP	Sets the V_{OUT} DC loop parameters. The default is 16.

FREQUENCY_SWITCH_R3 (33h)

The FREQUENCY_SWITCH_R3 command on Page 2 sets the switching frequency for rail 3. The switching frequency ranges between 200kHz and 5.11MHz, with 10kHz per step.

Command	FREQUENCY_SWITCH_R3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	FREQUENCY_SWITCH_R3	Sets the switching frequency in direct format. 10kHz/LSB.

MFR_OSR_SET_R3 (34h)

The MFR_OSR_SET command on Page 2 sets the overshoot reduction (OSR) related parameters. It is for rail 3 only.

Command	MFR_OSR_SET_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13	MFR_OSR_EN_R3	Enables the overshoot reduction function (OSR). This function can reduce the V_{OUT} overshoot at the load release. 1'b0: Disable OSR 1'b1: Enable OSR
12:7	MFR_OSR_FILTER_R3	Sets the minimum overshoot reduction (OSR) duration. 5ns/LSB.
6:0	MFR_OSR_ BLANKTIME_R3	Sets the blanking time between two effective overshoot reduction (OSR) events. 10ns/LSB.

MFR_RESERVED (35h)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_RESERVED (36h)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_SLOPE_SW_INI_R3 (37h)

The MFR_SLOPE_SW_INI_R3 command on Page 2 sets the rail 3 soft start initial ramp.

Command	MFR_SLOPE_SW_INI_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	MFR_VOUT_FINE_TUNE_R3	Sets the V_{OUT} fine-tune value. The trim value per step. Bit[12] is the sign bit. 0.64mV/LSB when the V_{DIFF} gain = 1 0.96mV/LSB when the V_{DIFF} gain = 1/2
6:0	MFR_SLOPE_SW_INI_R3	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_DCM_R3 (38h)

The MFR_SLOPE_SR_DCM_R3 command on Page 2 sets the rail 3 slope compensation slew rate in 1-phase DCM.

Command	MFR_SLOPE_SR_DCM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_1P_R3 (39h)

The MFR_SLOPE_SR_1P_R3 command on Page 2 provides 2 bytes to program the slope compensation for 1-phase operation. It is for rail 3 only.

Command	MFR_SLOPE_SR_1P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_SR_2P_R3 (3Ah)

The MFR_SLOPE_SR_2P_R3 command on Page 2 provides 2 bytes to program the slope compensation for 2-phase operation. It is for rail 3 only.

Command	MFR_SLOPE_SR_2P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_RESERVED (3Bh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_TRIM_SEL (3Ch)

The MFR_TRIM_SEL command on Page 2 sets the trim selection.

Command	MFR_TRIM_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:12	MFR_DROP_TRIM_SEL_R2	Selects one of the 16 backup trim registers (C1h~CBh on Page 1 and 0Ah~0Dh on Page 2) as the I_{DROOP} trim register for rail 2.
11:8	MFR_DROP_TRIM_SEL_R1	Selects one of the 16 backup trim registers (C1h~CBh on Page 1 and 0Ah~0Dh on Page 2) as the I_{DROOP} trim register for rail 1.
7:4	MFR_IMON_TRIM_SEL_R2	Selects one of the 16 backup trim registers (C1h~CBh on Page 1 and 0Ah~0Dh on Page 2) as the IMON trim register for rail 2.
3:0	MFR_IMON_TRIM_SEL_R1	Selects one of the 16 backup trim registers (C1h~CBh on Page 1 and 0Ah~0Dh on Page 2) as the IMON trim register for rail 1.

MFR_TRIM_SEL_R3 (3Dh)

The MFR_TRIM_SEL_R3 command on Page 2 sets the trim selection.

Command	MFR_TRIM_SEL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:4	MFR_DROP_TRIM_SEL_R3	Selects one of the 16 backup trim registers (C1h~CBh on Page 1 and 0Ah~0Dh on Page 2) as the I_{DROOP} trim register for rail 3.
3:0	MFR_IMON_TRIM_SEL_R3	Selects one of the 16 backup trim registers (C1h~CBh on Page 1 and 0Ah~0Dh on Page 2) as the IMON trim register for rail 3.

MFR_VRHOT_SET_R3 (3Eh)

The MFR_VRHOT_SET_R3 command on Page 2 sets the parameters for VRHOT. It is for rail 3 only.

Command	MFR_VRHOT_SET_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_VRHOT_EN_R3	Enables VR_HOT. 1'b0: Disable VR_HOT 1'b1: Enable VR_HOT
7:0	MFR_VRHOT_LIMIT_R3	Sets the VR over-temperature alert threshold. If the sensed temperature via the TSENS1 pin exceeds this threshold, OCP_L from GPIO pins asserts to alert the system. 1°C/LSB.

MFR_RESERVED (3Fh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

VOUT_OV_FAULT_LIMIT_R3 (40h)

The VOUT_OV_FAULT_LIMIT_R3 command on Page 2 sets the V_{OUT} over-voltage protection (OVP) threshold.

Command	VOUT_OV_FAULT_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	OVP_VID_SET_R3	3'b001: V_{REF} + 200mV 3'b010: V_{REF} + 325mV 3'b100: V_{REF} + 450mV Others: Invalid command
7:0	OVP_ABS_SET_R3	Sets an absolute over-voltage protection (OVP) threshold. If V_{OUT} exceeds this value, a protection is triggered. 10mV/LSB.

VOUT_OV_FAULT_RESPONSE_R3 (41h)

The VOUT_OV_FAULT_RESPONSE_R3 command on Page 2 sets the protection mode and delay time if a V_{OUT} over-voltage fault occurs.

Command	VOUT_OV_FAULT_RESPONSE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OVP_ABS_EN_R3	Enable bit for absolute over-voltage protection (OVP). 1'b0: Disabled 1'b1: Enabled
7:6	MFR_OVP_VID_MODE_R3	Set the over-voltage (OV) fault mode. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	MFR_OVP_VID_DELAYTIME_R3	Sets the OVP_VID blanking time. If an OVP_VID condition lasts for longer than the OVP_VID blanking time, an OVP_VID fault is triggered. 100ns/LSB.

VOUT_MAX_ALERT_R3 (42h)

The VOUT_MAX_ALERT_R3 command on Page 2 sets the VOUT over-voltage (OV) warning threshold, or returns the V_{OUT} peak value for rail 3. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	VOUT_MAX_ALERT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	VOUT_MAX_ALERT_R3	If GPIO_ACTIVE (68h) bit[13] is set to 0, the 42h register sets the V_{OUT} over-voltage (OV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, the 42h register returns the maximum peak V_{OUT}. It can be written with a lower value. If a higher V_{OUT} is detected, this register is overwritten. To start a new recording, reset this bit by writing 0x0000. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 2) bit[10].

VOUT_MIN_ALERT_R3 (43h)

The VOUT_MIN_ALERT_R3 command on Page 2 sets the V_{OUT} under-voltage (UV) warning threshold, or returns the minimum V_{OUT} value for rail 3. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	VOUT_MIN_ALERT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	VOUT_MIN_ALERT_R3	If GPIO_ACTIVE (68h) bit[13] is set to 0, the 43h register sets the V_{OUT} under-voltage (UV) warning limit. VID_STEP/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, the 43h register returns the minimum V_{OUT}. It can also be written with a higher value. If a lower V_{OUT} is detected, this register is overwritten. To start a new recording, reset this bit by writing 0x03FF. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 1) bit[10].

VOUT_UV_FAULT_LIMIT_R3 (44h)

The VOUT_UV_FAULT_LIMIT_R3 command sets the V_{OUT} under-voltage (UV) fault threshold.

Command	VOUT_UV_FAULT_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:8	UVP_VID_SET_R2	Sets the threshold for under-voltage protection (UVP). 3'b000: V_{REF} - 425mV 3'b001: V_{REF} - 375mV 3'b010: V_{REF} - 325mV 3'b011: V_{REF} - 275mV 3'b100: V_{REF} - 225mV 3'b101: V_{REF} - 175mV 3'b110: V_{REF} - 125mV 3'b111: V_{REF} - 75mV
7:0	RESERVED	Fixed to 0.

VOUT_UV_FAULT_RESPONSE_R3 (45h)

The VOUT_UV_FAULT_RESPONSE on Page 2 sets the under-voltage (UV) fault response.

Command	VOUT_UV_FAULT_RESPONSE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_UV_VID_EN_R3	Enables VID under-voltage protection (UVP). 1'b0: Disable VID UVP 1'b1: Enable VID UVP
7:6	MFR_UVP_MODE_R3	Sets the V_{OUT} under-voltage protection (UVP) mode. There are four modes available. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	MFR_UVP_ DELAYTIME_R3	Sets the V_{OUT} under-voltage protection (UVP) blanking time. A UVP fault occurs if the sensed V_{DIFF} drops below the UVP threshold for the UVP blanking time. 100ns/LSB.

IOUT_OC_FAULT_LIMIT_R3 (46h)

The IOUT_OC_FAULT_LIMIT command on Page 2 sets the I_{OUT} over-current (OC) fault threshold.

Command	IOUT_OC_FAULT_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	OCP_SPIKE_SET_R3	Sets the rail 3 OCP_SPIKE_TOTAL current-level DAC value. 6.25mV/LSB. It can be calculated with the following equation: $OCP\_SPIKE\_TOTAL = OCP\_SPIKE \times K_{CS} \times G_{IMON} \times R_{IMON} / 6.25$
7:0	OCP_TDC_SET_R3	Sets the rail1 OCP_TDC_TOTAL current level. The higher 8 MSB of the IMON1 ADC result (IMON1_SENSE bits[9:0]) are compared to this TDC level. 6.25mV/LSB. The result can be calculated with the following equation: $OCP\_TDC\_TOTAL = OCP\_TDC \times K_{CS} \times G_{IMON} \times R_{IMON} / 6.25$

IOUT_OC_FAULT_RESPONSE_R3 (47h)

The IOUT_OC_FAULT_RESPONSE_R3 command sets over-current protection (OCP) options and values.

Command	IOUT_OC_FAULT_RESPONSE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	MFR_OCP_MODE_R3	Selects the protection mode for both OCP_TDC and OCP_SPIKE. 2'b00: No action 2'b01: Latch off 2'b10: Hiccup 2'b11: Retry 6 times

13	MFR_OCP_TDC_EN_R3	Enable bit for over-current protection (OCP_TDC). 1'b0: Disabled 1'b1: Enabled
12:8	MFR_OCPTDC_ ACTIONDELAY_R3	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for the OCP_TDC blanking time. 1µs/LSB.
7:0	MFR_OCPTDC_ TRIGDELAY_R3	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for the OCP_TDC blanking time. 20µs/LSB.

IOUT_OC_SPIKE_RESPONSE_R3 (48h)

The IOUT_OC_SPIKE_RESPONSE command sets the over-current (OC) spike options and values.

Command	IOUT_OC_SPIKE_RESPONSE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	MFR_OCP_SPIKE_EN_R3	Enable bit for over-current protection (OCP_SPIKE). 1’b0: Disabled 1’b1: Enabled
7:4	MFR_OCPSPIKE_ ACTIONDELAY_R3	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for the OCP_SPIKE blanking time. 1µs/LSB.
3:0	MFR_OCPSPIKE_ TRIGDELAY_R3	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for an OCP_SPIKE blanking time. 200ns/LSB.

MFR_OCP_PHASE_LIMIT_R3 (49h)

The MP2926 provides OCP_PHASE protection to limit the per-phase valley current. OCP_PHASE is implemented by monitoring and comparing the cycle-by-cycle sensed current with a current reference. The MFR_OCP_PHASE_LIMIT command on Page 2 sets the rail 3 per-phase valley current limit.

Command	MFR_OCP_PHASE_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	OCP_DAC_SET_R2	Sets the per-phase valley current limit DAC value. 5mV/LSB.

IOUT_MAX_ALERT_R3 (4Ah)

The IOUT_MAX_ALERT_R3 command on Page 2 sets the I_{OUT} over-current (OC) warning threshold, or returns the peak value of I_{OUT}. It is for rail 3 only. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	IOUT_MAX_ALERT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	IOUT_MAX_ALERT_R3	If GPIO_ACTIVE (68h) bit[13] is set to 0, the 4Ah register sets the DAC value for the I_{OUT} over-current (OC) warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, the 4Ah register returns the peak I_{OUT}. In this mode it can be written with a lower value. If a higher I_{OUT} is detected, this register is overwritten. To start a new recording, reset the bit by writing 0x0000. Convert the read value to the actual output current (in A) with the following equation: $$I_{OUT}(A) = \frac{4Ah[9:0]}{6Ch[9:0]\times 1024}\times 6Eh[10:0]\times 2^{(6\text{-}GAIN\_SEL)}$$ Where GAIN_SEL is 6Ch bits[11:10].

MFR_FS_LIMIT_12P_R3 (4Bh)

The MFR_FS_LIMIT_12P_R3 command on Page 2 sets the rail 3 FS_LIMIT threshold for 1-phase and 2-phase operation to detect fast load insertion and exit phase-shedding.

Command	MFR_FS_LIMIT_12P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_FS_LIMIT_2P_R3	Sets the exit phase-shedding PWM interval time during 2-phase operation. If the time interval between the two phases is shorter than FS_LIMIT_2P, the count adds 1. When the count reaches the value set by Page 2, 51h bits[2:0], APS is exited immediately. 5ns/LSB.
7:0	MFR_FS_LIMIT_1P_R3	Sets the PWM off time threshold to exit phase-shedding for rail 1. If the PWM1 off time after excluding MIN_OFF_TIME is shorter than FS_LIMIT_1P, the count adds 1. When the count reaches the value set by Page 2, 51h bits[9:7], APS is exited immediately. It is effective both for DCM and CCM. 10ns/LSB.

MFR_RESERVED (4Ch)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

MFR_APS_LEVEL_12P_R3 (4Dh)

The MFR_APS_LEVEL_12P_R3 command on Page 2 sets the rail 3 automatic phase-shedding (APS) current threshold for single-phase CCM and DCM operation.

Command	MFR_APS_LEVEL_12P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_APS_IIL_1P_CCM_R3	Sets the rail 3 APS current threshold for single-phase CCM. 1A/LSB.
7:0	MFR_APS_IIL_1P_DCM_R3	Sets the rail 3 APS current threshold for single-phase DCM. 1A/LSB.

MFR_RESERVED (4Eh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

OT_FAULT_LIMIT_R3 (4Fh)

The OT_FAULT_LIMIT_R3 command on Page 2 sets the over-temperature protection (OTP) operation and values.

Command	OT_FAULT_LIMIT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X								

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	MFR_OTP_LIMIT_R3	OTP fault limit setting. If the junction temperature monitored on the TSENS2 pin exceeds OTP_LIMIT, the VR shuts off the disabled output. 1°C/LSB.

SMBALERT_MASK (50h)

The SMBALERT_MASK command on Page 2 masks the faults to prevent ALT_P# assertion.

Command	SMBALERT_MASK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	OTP_MASK	1'b0: If an OTP fault occurs, ALT_P# does not assert 1'b1: If an OTP fault occurs, ALT_P# asserts
14	OVP_MASK	1'b0: If an OVP fault occurs, ALT_P# does not assert 1'b1: If an OVP fault occurs, ALT_P# asserts
13	UVP_MASK	1'b0: If an UVP fault occurs, ALT_P# does not assert 1'b1: If a UVP fault occurs, ALT_P# asserts
12	VMAX_VMIN_MASK	1'b0: If V_{OUT} exceeds V_{MAX} or drops below V_{MIN}, ALT_P# does not assert 1'b1: If V_{OUT} exceeds V_{MAX} or drops below V_{MIN}, ALT_P# asserts
11	OCP_MASK	1'b0: If an OCP fault occurs, ALT_P# does not assert 1'b1: If an OCP fault occurs, ALT_P# asserts
10	OC_UV(SCP)_MASK	1'b0: If an OCP and UVP fault occur, ALT_P# does not assert 1'b1: If an OCP and UVP fault occur, ALT_P# asserts
9	CML_INVALID_CMD_ MASK	1'b0: If an invalid command in a communication fault (see the STATUS_CML section on page 192) is triggered, ALT_P# does not assert 1'b1: If an invalid command in a communication fault is triggered, ALT_P# asserts
8	CML_INVALID_DATA_ MASK	1'b0: If invalid data in a communication fault (see the STATUS_CML section on page 192) is triggered, ALT_P# does not assert 1'b1: If invalid data in a communication fault is triggered, ALT_P# asserts
7	PEC_ERROR_MASK	1'b0: If a PEC error occurs, ALT_P# does not assert 1'b1: If a PEC error occurs, ALT_P# asserts
6	CRC_ERROR_MASK	1'b0: If a CRC error occurs, ALT_P# does not assert 1'b1: If a CRC error occurs, ALT_P# asserts
5	CMD_FLT_BLK_TRG_ MASK	1'b0: If a command fault block triggers, ALT_P# does not assert 1'b1: If a command fault block triggers, ALT_P# asserts
4	CML_OTHER_FAULT_ MASK	1'b0: If a communication fault (see the STATUS_CML section on page 192) is triggered, ALT_P# does not assert 1'b1: If a communication fault (see the STATUS_CML section on page 192) is triggered, ALT_P# asserts
3	NVM_FAULT_MASK	1'b0: If an NVM fault occurs, ALT_P# does not assert 1'b1: If an NVM fault occurs, ALT_P# asserts
2	VIN_OVP_MASK	1'b0: If a V_{IN} OV fault occurs, ALT_P# does not assert 1'b1: If a V_{IN} OV fault occurs, ALT_P# asserts
1	VIN_UV_WARN_MASK	1'b0: If a V_{IN} UV warning occurs, ALT_P# does not assert 1'b1: If a V_{IN} UV warning occurs, ALT_P# asserts
0	VIN_UVP_MASK	1'b0: If a VIN UV fault occurs, ALT_P# does not assert 1'b1: If a V_{IN} UV fault occurs, ALT_P# asserts

MFR_FS_DETECT_R3 (51h)

The MFR_FS_DETECT_R3 command on Page 2 sets the rail 3 APS timing and behaviors.

Command	MFR_FS_DETECT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables exit phase-shedding according to the PWM6 off time. The PWM minimum off time is excluded from the PWM off time. 1'b0: Disable PWM6 off-time detection to exit APS 1'b1: Enable PWM6 off-time detection to exit APS
10	FS_EXIT_APS_EN_NP	Enables exit phase-shedding according to the multi-phase PWM interval time between consecutive phases. The time threshold is set by register 4Bh on Page 2. The PWM blanking time is excluded from the PWM interval time. 1'b0: Disable multi-phase PWM interval time detection to exit APS 1'b1: Enable multi-phase PWM interval time detection to exit APS
9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count of PWM6 off time condition to exit phase-shedding. If the PWM off time condition meets the counting threshold, the controller exits APS immediately.
6:3	RETURN_APS_DELAY	Sets the minimum full-phase runtime after exiting APS by an FS_LIMIT event. 20µs/LSB.
2:0	FS_EXIT_APS_CNT_NP	Sets the continuous count of the multi-phase PWM interval time to exit phase-shedding. If the PWM interval condition meets the counting threshold, the controller exits APS immediately.

MFR_APS_CTRL_R3 (52h)

The MFR_APS_CTRL_R3 command on Page 2 sets the rail 3 APS timing and behaviors.

Command	MFR_APS_CTRL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:12	MFR_ADP_OC_NPS_ EXIT_CNT_R3	Sets the period delay count from OCP_PHASE triggered to APS exit. 100ns/LSB.
11	MFR_ADP_OC_NPS_ EXIT_EN_R3	Enables OCP_PHASE protection exit APS at any power state. 1'b0: Disable the OCP_PHASE signal trigger from any phase to full-phase operation 1'b1: Enable the OCP_PHASE signal trigger from any phase to full-phase operation
10	MFR_ADP_PFM_EXIT_EN_R3	Enables the rail 3 frequency increasing condition to exit APS. 1'b0: Disable 1'b1: Enable
9	MFR_ADP_OC_1PS_ EXIT_EN_R3	Enables OCP_PHASE protection to exit APS during single-phase DCM/CCM only. 1'b0: Disable the OCP per-phase signal to trigger single-phase DCM/CCM to full-phase operation 1'b1: Enable the OCP per-phase signal to trigger single-phase DCM/CCM to full-phase operation
8	MFR_ADP_UV_EXIT_ EN_R3	Sets the rail 3 V_{FB} < VID - 25mV to enter full-phase operation. 1'b0: Disable rail 3 V_{FB} < VID - 25mV to enter full-phase operation 1'b1: Enable rail 3 V_{FB} < VID - 25mV to enter full-phase operation

7:2	MFR_PS_ENTER_TIME_R3	Sets the phase-shedding delay time. If the reported load current is consecutively below the APS threshold for an APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE period, the controller enters APS mode and automatically sheds the phase count according to the load current.
1	MFR_PHASHED_EXIT_MOD_R3	Sets the phase-dropping mode during phase-shedding. Phase-shedding may be due to APS. 1'b0: Drop the phase count to the target immediately 1'b1: Shed the phases one by one with a configured delay time. The delay time is set with 54h bits[10:7].
0	MFR_AUTO_PS_EN_R3	Enables the rail 3 APS mode. 1'b0: Disable rail 3 APS mode 1'b1: Enable rail 3 APS mode

MFR_APS_CTRL2_R3 (53h)

The MFR_APS_CTRL2_R3 command on Page 2 sets the rail 3 APS timing and behaviors.

Command	MFR_APS_CTRL2_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	**Bit Name**	**Description**
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:9	APS_COMP_CNT	The MP2926 provides positive compensation on VREF during phase-shedding to reduce undershoot. Phase-shedding may be due to APS. V_{REF} compensation is implemented by adding a PMBus-programmable positive voltage on COMP of the DC loop. After phase-shedding begins, the voltage returns to 0 step by step with a time interval. APS_COMP_CNT sets this time interval between each step. 50ns/LSB.
8	DECAY_COMP_EN	Enables V_{REF} compensation when exiting decay mode. The MP2926 provides V_{REF} compensation when exiting decay mode. The compensation voltage level and slew rate are the same with APS compensation. 1'b0: Disable V_{REF} compensation when exiting decay mode 1'b1: Enable V_{REF} compensation when exiting decay mode
7:4	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce the undershoot. This compensation is added to V_{REF} if phase-shedding occurs. 1.37mV/LSB.
3:0	MFR_APS_IHYS_R3	Sets the current hysteresis between phase-shedding and phase-adding. It prevents back-and-forth phase-shedding when APS is enabled. 1A/LSB.

MFR_APS_CTRL3_R3 (54h)

The MFR_APS_CTRL3_R3 command on Page 2 sets the rail 3 APS timing and behaviors.

Command	MFR_APS_CTRL3_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:7	MFR_PS_INTERVAL_R3	Sets the phase-by-phase dropping time intervals. It is only effective when bit[1] of 52h register is set to 1. 2.5μs/LSB.
6:0	MFR_PRD_EXIT_APS_TIME_R3	Sets the period condition for the DC loop and current balance loop holding. If the absolute error between the set switching period and real switching period $\|t_S - t_{SET}\|$ is greater than MFR_PRD_EXIT_APS_TIME x 80ns, the DC loop and current balancing time are held for a given time. 80ns/LSB.

MFR_NVM_CTRL (55h)

The MFR_NVM_CTRL sets the parameters for the NVM.

Command	MFR_NVM_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	RESERVED	Fixed to 0.
13:8	JOUT_ADC_TIME	Sets the J_{OUT} ADC time. 50ns/LSB.
7	TESTMODE_WRITE_EN	1’b0: Disabled. Cannot write to Page 3 1’b1: Enabled. Can write to Page 3
6	MEMORY_READ_EN	1’b0: Disabled. The read value is FFFF 1’b1: Enabled. The read value is the real value
5	MFR_BYTE_WORD	Enables NVM single-byte writing or reading via the PMBus. 1’b0: Disable NVM byte writing or reading via the PMBus 1’b1: Enable NVM byte writing or reading via the PMBus
4	OPERATION_ALL_CALL_EN	Enables command on/off control for both rails. 1’b0: Disabled 1’b1: Enabled
3	MFR_NVM_COPY_EN	It is applied to the 16h and 18h registers. Set to 0 for normal operation. 1’b0: Disabled 1’b1: Enabled
2	MFR_STORE_ALL_EN	It is applied to the 15h register. 1’b0: Disabled 1’b1: Enabled
1	FAULT_RECORD_EN	Enables fault saving to NVM. 1’b0: Disabled 1’b1: Enabled
0	MFR_CRC_ERROR_EN	Enables CRC fault protection. 1’b0: Disable CRC fault protection for VR shutdown 1’b1: Enable CRC fault protection for VR shutdown

MFR_FSCB_LOOP_CTRL_R3 (56h)

The MFR_FSCB_LOOP_CTRL_R3 command on Page 2 sets the rail 3 switching frequency and current balance loop.

Command	MFR_FSCB_LOOP_CTRL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	MFR_FS_LOOP_EN_R3	Enables the switching frequency loop. The frequency loop keeps the switching frequency flat, and equals the set value at different input voltages and load currents. This bit active for both rails. 1'b0: Disable the frequency loop 1'b1: Enable the frequency loop
14	TRANS_HOLD_FS_EN_R1	Holds frequency loop regulation if a load transient event is detected (e.g. V_{FB} exceeds the V_{FB}+ window or V_{FB}- window). 1'b0: Disable holding the frequency loop if a load transient event is detected 1'b1: Enable holding the frequency loop if a load transient event is detected
13	PS_HOLD_FS_EN_R3	Holds frequency loop regulation if the phase count changes. 1'b0: Disable holding frequency loop regulation if the phase count changes 1'b1: Enable holding frequency loop regulation if the phase count changes
12	DVID_HOLD_FS_EN_R3	Holds frequency loop regulation if DVID occurs. 1'b0: Disable holding frequency loop regulation if DVID occurs 1'b1: Enable holding frequency loop regulation if DVID occurs
11:8	MFR_FS_LOOP_CNT_R3	Sets the minimum frequency loop hold time if any load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set.100μs/LSB.
7	MFR_CB_EN_R3	Enables the current balance loop. 1'b1: Enable the current balance loop 1'b0: Disable the current balance loop
6	PRD_HOLD_CB_EN_R3	Holds the current balance loop when the PWM period meets the PWM switching period condition set with PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disable holding the current balance loop if the PWM switching period condition is met 1'b1: Enable holding the current balance loop if the PWM switching period condition is met
5	PS_HOLD_CB_EN_R3	Holds the current balance loop if the phase number changes. 1'b0: Disable holding the current balance loop if the phase number changes 1'b1: Enable holding the current balance loop if the phase number changes
4	DVID_HOLD_CB_EN_R3	Holds the current balance loop if DVID occurs. 1'b0: Disable holding the current balance loop if DVID occurs 1'b1: Enable holding the current balance loop if DVID occurs
3:0	CB_LOOP_HOLD_TIME	Sets the current balance loop hold time. If any load transient event, PWM switching period change event, phase count change event, or DVID event is detected and the corresponding enable bit is set, the current balance loop stops regulating for the time set by the CB_LOOP_HOLD command. 100μs/LSB.

MFR_VOUT_LOOP_CTRL_R3 (57h)

The MFR_VOUT_LOOP_CTRL command on Page 2 sets the rail 3 V_{OUT} loop parameters.

Command	MFR_VOUT_LOOP_CTRL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	MFR_VDIFF_GAIN_SEL_R3	Selects the V_{DIFF} gain. If the output voltage exceeds 1.55V (the maximum sampling range of the internal ADC), select 1/2x gain. V_{OUT} has a 3V maximum. 1'b0: 1x 1'b1: 1/2x
9	MFR_DC_REF_SEL_R3	Sets the output voltage DC loop sensing point. 1'b0: V_{FB} 1'b1: V_{DIFF}
8	MFR_VCAL_PS2_EN_R3	Enables DC loop calibration during DCM. 1'b0: Disable 1'b1: Enable
7	MFR_VCAL_EN_R3	Enables DC loop calibration both during DCM and CCM operation. 1'b0: Disable 1'b1: Enable
6	DC_LOOP_TSW_DIS_EN	Holds the DC loop if the PWM time interval meets the PWM switching period condition set by PMBus command MFR_APS_CTRL3 (54h), bits[6:0]. 1'b0: Disable holding the DC loop if the PWM switching period condition is met 1'b1: Enable holding the DC loop if the PWM switching period condition is met
5	DC_LOOP_PH_DIS_EN	Holds the DC loop if the phase count changes. 1'b0: Disable 1'b1: Enable
4	DC_LOOP_TR_DIS_EN	Holds DC loop regulation if a load transient event is detected (e.g. V_{FB} exceeds the V_{FB}+ window or V_{FB}- window). 1'b0: Disable holding the DC loop if the V_{FB}± window condition is met 1'b1: Enable holding the DC loop if the V_{FB}± window condition is met
3:0	MFR_DC_LOOP_CNT_R3	Sets the DC loop minimum hold time in direct format. 200µs/LSB with a +100µs offset.

JOUT_SHORT_PK_R3 (58h)

The JOUT_SHORT_PK_R3 command returns the peak J_{OUT} value in every short-term period.

Command	JOUT_SHORT_PK_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	JOUT_SHORT_PK_R3	Always returns the peak J_{OUT} value in every short-term period if J_{OUT} is enabled and GPIO_ACTIVE (68h) bit[13] is set to 1. If J_{OUT} is disabled or GPIO_ACTIVE (68h) bit[13] is set to 0, it returns the preset value.

JOUT_LONG_PK_R3 (59h)

The JOUT_LONG_PK_R3 command returns the peak J_{OUT} value in every long-term period.

Command	JOUT_LONG_PK_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	JOUT_LONG_PK_R3	Always returns the peak J_{OUT} value in every long-term if J_{OUT} is enabled and GPIO_ACTIVE (68h) bit[13] is set to 1. If J_{OUT} is disabled or GPIO_ACTIVE (68h) bit[13] is set to 0, it returns the preset value.

MFR_SLOPE_CNT_1P_R3 (5Ah)

The MFR_SLOPE_CNT_1P_R3 command on Page 2 sets the rail 3 slope voltage clamp time during 1-phase operation.

Command	MFR_SLOPE_CNT_1P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	MFR_SLOPE_CNT_1P_R3	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_CNT_2P_R3 (5Bh)

The MFR_SLOPE_CNT_2P_R3 command on Page 2 sets the rail 3 slope voltage clamp time during 2-phase operation.

Command	MFR_SLOPE_CNT_2P_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	MFR_SLOPE_CNT_2P_R3	Sets the slope voltage clamp time. 5ns/LSB.

VDIFF2_SNAPSHOT (5Ch)

The VDIFF2_SNAPSHOT command on Page 2 returns the snapshot D4h (Page 1) value while reading the D3h (Page 1) value.

Command	VDIFF2_SNAPSHOT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R									
Function							VDIFF2_SNAPSHOT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VDIFF2_SNAPSHOT	Returns a snapshot V_{OUT} ADC value when reading D3h (Page 1). The value is updated to the D4h (Page 1) value while reading D3h (Page 1). 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 1) bit[10].

VDIFF3_SNAPSHOT (5Dh)

The VDIFF3_SNAPSHOT command on Page 2 returns the snapshot D4h (Page 2) value while reading the D3h (Page 2) value.

Command	VDIFF3_SNAPSHOT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function							VDIFF3_SNAPSHOT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VDIFF3_SNAPSHOT	Returns a snapshot V_{OUT} ADC value when reading D3h (Page 2). The value is updated to the D4h (Page 2) value while reading D3h (Page 2). 1.56mV/LSB when V_{DIFF} gain = 1 3.12mV/LSB when V_{DIFF} gain = 1/2 Where V_{DIFF} gain is set by 4Dh (Page 1) bit[10].

MFR_SLOPE_CNT_DCM_R3 (5Eh)

The MFR_SLOPE_CNT_DCM_R3 command on Page 2 sets the slope voltage clamp time during DCM operation. It is for rail 3 only.

Command	MFR_SLOPE_CNT_DCM_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	MFR_SLOPE_CNT_DCM_R3	Sets the slope voltage clamp time. 5ns/LSB.

MFR_PG_DELAY_R3 (5Fh)

The MFR_PG_DELAY_R3 command on Page 2 sets the power good on/off delay time. It is for rail 3 only.

Command	MFR_PG_DELAY_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:10	MFR_PGOFF_DELAY_R3	Sets the power good off delay time. 5µs/LSB.
9:0	MFR_PGON_DELAY_R3	Sets the power good on delay time. 5µs/LSB.

TON_DELAY_R3 (60h)

The TON_DELAY_R3 commands on Page 2 sets the delay time from when system initialization ends to when rail 3 VREF starts to boot up.

Command	TON_DELAY_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	TON_DELAY_R3	Sets the delay time from when system initialization ends to when VREF boots up. 100µs/LSB.

TON_RISE_R3 (61h)

The TON_RISE_R3 command on Page 2 sets the rail 3 reference voltage boot-up slew rate.

Command	TON_RISE_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TON_RISE_R3	Sets the rail 3 boot-up slew rate in PMBus and PVID mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h) bit[15].

MFR_PWM_MIN_TIME1_R3 (62h)

The MFR_PWM_MIN_TIME1_R3 command on Page 2 sets the minimum pulse width if PWM is high, low, or in tri-state. It is for rail 3 only.

Command	MFR_PWM_MIN_TIME1_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	MFR_MIN_LOW_TIME_R3	Sets the minimum PWM low time. 10ns/LSB with a -5ns offset. The minimum PWM low time can be calculated with the following equation: (PWM_MIN_LOW_TIME x 10 - 5) ns
8:6	MFR_MIN_ON_TIME_R3	Sets the minimum PWM high time. 10ns/LSB with a -5ns offset. The minimum PWM high time can be calculated with the following equation: (PWM_MIN_HIGH_TIME x 10 - 5) ns
5:0	MFR_MIN_HIZ_TIME_R3	Sets the minimum PWM tri-state time. 10ns/LSB with a -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: (PWM_MIN_TRI_TIME x 10 - 5) ns

MFR_PWM_MIN_TIME2_R3 (63h)

The MFR_PWM_MIN_TIME2_R3 command on Page 2 sets the PWM minimum off time, and can enable zero-current detection (ZCD). It is for rail 3 only.

Command	MFR_PWM_MIN_LIMIT2_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	TON_LIMIT_TO_VCAL	The DC loop can be held if the PWM period meets the condition set in MFR_FS (33h, Page 0). If the calculated PWM on time is shorter than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	MFR_ZCD_EN_R3	Enables rail 3 zero-current detection (ZCD). 1'b0: Disable ZCD 1'b1: Enable ZCD
8:5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4:0	MFR_MINOFF_TIME_R3	Sets the PWM minimum off time. 20ns/LSB with a 15ns offset. The PWM minimum off time can be calculated with the following equation: (PWM_MIN_OFF_TIME x 20 + 15) ns

TOFF_DELAY_R3 (64h)

The TOFF_DELAY_R3 command on Page 2 sets the rail 3 delay time from when EN goes low to when VREF starts to shut down on rail 3.

Command	TOFF_DELAY_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	TOFF_DELAY_R3	Sets the delay time from when EN goes low to when VREF shuts down. 100µs/LSB.

TOFF_FALL_R3 (65h)

The TOFF_FALL_R3 command on Page 2 sets the V_{REF} down slew rate after receiving an OPERATION command for soft-off on rail 3.

Command	TOFF_FALL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	TOFF_FALL_R3	Sets the rail 3 OPERATION command soft-off slew rate in PMBus and PVID mode. 0.01mV/µs/LSB or 1mV/µs/LSB. The resolution is determined by MFR_VR_CONFIG3 (C3h) bit[15].

GPIO_SEL_GROUP5 (66h)

The GPIO_SEL_GROUP5 command sets the GPIO parameters.

Command	GPIO_SEL_GROUP5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:8	GPIO4_SEL	4'b0000: GPIO4 is selected to be PG3 4'b0001: GPIO4 is selected to be PG1 4'b0010: GPIO4 is selected to be PG2 4'b0011: GPIO4 is selected to be Hi-Low 4'b0100: GPIO4 is selected to be ALT_P# 4'b0101: GPIO4 is selected to be FAULT# 4'b0110: GPIO4 is selected to be OCP_L 4'b0111: GPIO4 is selected to be OCP_SPIKE 4'b1000: GPIO4 is selected to be OCP_TDC 4'b1001: GPIO4 is selected to be VRHOT# 4'b1010: GPIO4 is selected to be J_{OUT} short-term alert 4'b1011: GPIO4 is selected to be J_{OUT} long-term alert 4'b1100: GPIO4 is selected to be I_{OUT} max alert 4'b1101: GPIO4 is selected to be I_{OUT} min alert 4'b1110: GPIO4 is selected to be V_{OUT} max alert 4'b1111: GPIO4 is selected to be V_{OUT} min alert
7:4	GPIO3_SEL	4'b0000: GPIO3 is selected to be PG2 4'b0001: GPIO3 is selected to be PG1 4'b0010: GPIO3 is selected to be Hi-Low 4'b0011: GPIO3 is selected to be PG3 4'b0100: GPIO3 is selected to be ALT_P# 4'b0101: GPIO3 is selected to be FAULT# 4'b0110: GPIO3 is selected to be OCP_L 4'b0111: GPIO3 is selected to be OCP_SPIKE 4'b1000: GPIO3 is selected to be OCP_TDC 4'b1001: GPIO3 is selected to be VRHOT# 4'b1010: GPIO3 is selected to be J_{OUT} short-term alert 4'b1011: GPIO3 is selected to be J_{OUT} long-term alert 4'b1100: GPIO3 is selected to be I_{OUT} max alert 4'b1101: GPIO3 is selected to be I_{OUT} min alert 4'b1110: GPIO3 is selected to be V_{OUT} max alert 4'b1111: GPIO3 is selected to be V_{OUT} min alert
3:0	GPIO2_SEL	4'b0000: GPIO2 is selected to be PG1 4'b0001: GPIO2 is selected to be Hi-Low 4'b0010: GPIO2 is selected to be PG2 4'b0011: GPIO2 is selected to be PG3 4'b0100: GPIO2 is selected to be ALT_P# 4'b0101: GPIO2 is selected to be FAULT# 4'b0110: GPIO2 is selected to be OCP_L 4'b0111: GPIO2 is selected to be OCP_SPIKE 4'b1000: GPIO2 is selected to be OCP_TDC 4'b1001: GPIO2 is selected to be VRHOT# 4'b1010: GPIO2 is selected to be J_{OUT} short-term alert 4'b1011: GPIO2 is selected to be J_{OUT} long-term alert 4'b1100: GPIO2 is selected to be I_{OUT} max alert 4'b1101: GPIO2 is selected to be I_{OUT} min alert 4'b1110: GPIO2 is selected to be V_{OUT} max alert 4'b1111: GPIO2 is selected to be V_{OUT} min alert

GPIO_SEL_GROUP6 (67h)

The GPIO_SEL_GROUP6 command sets the GPIO parameters.

Command	GPIO_SEL_GROUP6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:8	TSENS3_CSX_SEL	Select CSx for the TSENS3 pin: 4'b0001: TSENS3 is selected to be CS1 4'b0010: TSENS3 is selected to be CS2 4'b1001: TSENS3 is selected to be CS3 4'b1010: TSENS3 is selected to be CS4 4'b1011: TSENS3 is selected to be CS5 4'b1100: TSENS3 is selected to be CS6 Others: Invalid
7:4	TSENS2_CSX_SEL	Selects CSx for the TSENS2 pin: 4'b0001: TSENS2 is selected to be CS1 4'b0010: TSENS2 is selected to be CS2 4'b1001: TSENS2 is selected to be CS3 4'b1010: TSENS2 is selected to be CS4 4'b1011: TSENS2 is selected to be CS5 4'b1100: TSENS2 is selected to be CS6 Others: Invalid
3:0	ADDR_CSX_SEL	Selects CSx for the ADDR pin: 4'b0001: ADDR is selected to be CS1 4'b0010: ADDR is selected to be CS2 4'b1001: ADDR is selected to be CS3 4'b1010: ADDR is selected to be CS4 4'b1011: ADDR is selected to be CS5 4'b1100: ADDR is selected to be CS6 Others: Invalid

MFR_EN_SEL (68h)

The MFR_EN_SEL command sets the EN-related parameters.

Command	MFR_EN_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	MFR_PGOOD2EN_SEL_R3	Selects the internal power good combination for the rail 3 internal EN signal (see bits[8:6]). 2'b00: PGOOD_R1 2'b01: PGOOD_R2 2'b10: PGOOD_R1 & PGOOD_R2 2'b11: PGOOD_R1 & PGOOD_R2
13:12	MFR_PGOOD2EN_SEL_R2	Selects the internal power good combination for the rail 2 internal EN signal (see bits[5:3]). 2'b00: PGOOD_R1 2'b01: PGOOD_R3 2'b10: PGOOD_R1 & PGOOD_R3 2'b11: PGOOD_R1 & PGOOD_R3

11:10	MFR_PGOOD2EN_SEL_R1	Selects the internal power good combination for the rail 1 internal EN signal (see bits[2:0]). 2'b00: PGOOD_R2 2'b01: PGOOD_R3 2'b10: PGOOD_R2 & PGOOD_R3 2'b11: PGOOD_R2 & PGOOD_R3
9	EN_PIN_SEL	1'b0: All three rails share one enable signal from the EN pin 1'b1: All three rails use different EN signals (see bits[8:0])
8:6	MFR_EN3_SEL	Selects the internal ENABLE_R3 from several pins: 3'b000: EN 3'b001: GPIO2 3'b010: GPIO3 3'b011: GPIO4 3'b100: PVID0 3'b101: PVID1 3'b110: PVID2 3'b111: Internal power good combination, see bits[15:14]
5:3	MFR_EN2_SEL	Selects the internal ENABLE_R2 from several pins: 3'b000: EN 3'b001: GPIO2 3'b010: GPIO3 3'b011: GPIO4 3'b100: PVID0 3'b101: PVID1 3'b110: PVID2 3'b111: Internal power good combination, see bits[13:12]
2:0	MFR_EN1_SEL	Selects the internal ENABLE_R1 from several pins: 3'b000: EN 3'b001: GPIO2 3'b010: GPIO3 3'b011: GPIO4 3'b100: PVID0 3'b101: PVID1 3'b110: PVID2 3'b111: Internal power good combination, see bits[11:10]

MFR_TEMP_CAL_R3 (69h)

The MFR_TEMP_CAL_R3 command on Page 2 sets the DrMOS temperature-sense gain and offset.

Command	MFR_TEMP_CAL_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_TEMP_GAIN_R3	Sets the temperature-sense gain to transfer the voltage on the TEMP pin to the direct temperature in degrees Celsius.
7:0	MFR_TEMP_OFFSET_R3	Sets the temperature-sense offset to convert the voltage on the TSENS3 pin to the direct temperature in degrees Celsius. 1°C/LSB. Bit[7] is the sign bit.

MFR_VOUT_CALC_R3 (6Ah)

The MFR_VOUT_CALC_R3 command on Page 2 sets the gain and offset for V_{OUT} calculations.

Command	MFR_VOUT_CALC_R3															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:8	MFR_VOUT_CALC_ OFFSET_R3	Adds an offset to V_{OUT} reporting in the READ_VOUT (8Bh) register. This bit is for the rail 3 output voltage report only. This bit is in two's complement format. Bit[13] is the sign bit. VID_STEP/LSB. When the VID_STEP is 6.25mV, the voltage list below shows the direct values and real-world values. 6'b00 0000: 0mV 6'b00 0001: +6.25mV 6'b01 1111: +193.75mV 6'b10 0000: -200mV 6'b10 0001: -193.75mV 6'b11 1111: -6.25mV
7:0	MFR_VOUT_CALC_ GAIN_R3	Sets the gain from the ADC-sensed VOSEN-VORTN voltage to the V_{OUT} report in READ_VOUT (8Bh). This bit is for the rail 3 output voltage report only.

MFR_RESERVED (6Bh)

Command	MFR_RESERVED															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	RESERVED	Fixed to 0.

IOUT_CAL_GAIN_PMBUS_R3 (6Ch)

The IOUT_CAL_GAIN_PMBUS_R3 command on Page 2 sets the gain for output current PMBus reporting. The MP2926 senses the output current by sensing the IMON voltage. The reported output current is returned with PMBus command READ_IOUT (8Ch, Page 2).

Command	IOUT_CAL_GAIN_PMBUS_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:10	GAIN_SEL	Sets the exponent value for the IOUT_CAL_GAIN equation in this command.

9:0	MFR_IOUT_CALC_GAIN_R3	Sets the current-sense (CS) gain for the PMBus report. The CS gain can be calculated with the following equation: $IOUT\_CAL\_GAIN=\frac{1023}{1.6}\times K_{CS}\times G_{IMON}\times R_{IMON}\times 2^{(6-GAIN\_SEL)}$ Where K_{CS} is the Intelli-Phase™ CS gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bits[11:10] of 6Ch (Page 2).

IOUT_CAL_OS_PMBUS_R3 (6Dh)

The IOUT_CAL_OS_PMBUS_R3 command on Page 2 sets the offset for the rail 3 output current PMBus report. The offset is for I_{OUT} over-reporting or under-reporting. The reported output current is returned with the PMBus READ_IOUT (8Ch, Page 1) command.

Command	IOUT_CAL_OS_PMBUS_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:6	IOUT_CAL_PH_OFS_R3	Adds an offset according the phase number. A larger N results in a larger offset. Bit[12] is sign bit.
5:0	MFR_IOUT_CALC_OFFSET_R3	Adds a current report offset to READ_IOUT (8Ch).

MFR_IMON_SET_R3 (6Eh)

The MFR_IMON_SET_R3 command on Page 2 sets some configurations on the internal IMON sense in PMBus mode. It is for rail 3 only.

Command	MFR_IMON_SET_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:13	MFR_IMON_RES_SET_R3	Sets the IMON resistor for rail 3. 3'b 000: 2.5kΩ 3'b 001: 5kΩ 3'b 010: 10kΩ 3'b 011: 40kΩ 3'b1xx: Not connected
12	MFR_IMON_GAIN_SET_R3	1'b0: The IMON1 current mirror gain is 1/8 1'b1: The IMON1 current mirror gain is 1/16
11	RESERVED	Fixed to 0.

10:0	MFR_TRIM_IMON_DIGI_GAIN_R3	Sets the digital calculating gain for I_{OUT} reporting. The gain is multiplied by the IMON ADC-sensed value, and forms the final IMON digital-sense value. The IMON digital-sense value is used for PMBus output current reporting. The final IMON-sensed value can be calculated with the following equation: $IOUT\_PMBUS\_REPORT=1023\times\frac{I_{OUT}\times K_{CS}\times G_{IMON}\times R_{IMON}}{1.6}\times\frac{TRIM\_DIGI\_GAIN}{1024}\times\frac{2^{(6-GAIN\_SEL)}}{GAIN}$ Where I_{OUT} is the output current (in A), K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the IMON resistor (in Ω), and TRIM_DIGI_GAIN is a decimal value.

IOUT_MIN_ALERT_R3 (6Fh)

The IOUT_MIN_ALERT_R3 command on Page 2 returns the minimum I_{OUT} value or the preset value. It is for rail 3 only. It is determined by GPIO_ACTIVE (68h) bit[13].

Command	IOUT_MIN_ALERT_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IOUT_MIN_ALERT_R3	If GPIO_ACTIVE (68h) bit[13] is set to 0, the 6Fh register sets the DAC value of the I_{OUT} over-current (OC) warning threshold. 6.25mV/LSB. If GPIO_ACTIVE (68h) bit[13] is set to 1, the 6Fh register returns the minimum I_{OUT} value. In this mode, it also can be written with a higher value. If a higher I_{OUT} is detected, this register is overwritten. To start a new recording, reset this bit by writing 0x03FF. Convert the read value to the actual output current (in A) with the following equation: $I_{OUT}(A)=\frac{6Fh[9:0]}{6Ch[9:0]\times 1024}\times 6Eh[10:0]\times 2^{(6-GAIN\_SEL)}$ Where GAIN_SEL is 6Ch bits[11:10].

MFR_PSI_SET (70h)

The MFR_PSI_SET command on Page 2 sets the phase configuration.

Command	MFR_PSI_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FORCE_PHASE_NUM_EN_R3	Enable bit to force the power state following what is set by bits[10:9]. 1'b0: Disable the forced power state 1'b1: Enable the forced power state. The system's active phase number is determined by bits[10:9]

10:9	MFR_PSI_SET_R3	Sets the forced phase number. 2'b:00: DCM 2'b:01: 1-phase CCM 2'b:10: 2-phase CCM Others: Invalid
8	FORCE_PHASE_NUM_EN_R2	Enable bit to force the power state following what is set by bits[7:5]. 1'b0: Disable the forced power state 1'b1: Enable the forced power state. The system's active phase number is determined by bits[7:5]
7:5	MFR_PSI_SET_R2	Sets the forced phase number. 3'b000: DCM 3'b001: 1-phase CCM 3'b010: 2-phase CCM Others: Invalid
4	FORCE_PHASE_NUM_EN_R1	Enable bit to force the power state following what it set by bits[3:0]. 1'b0: Disable the forced power state. 1'b1: Enable the forced power state. The system's active phase number is determined by bits[3:0]
3:0	MFR_PSI_SET_R1	Set the forced phase number. 4'b0000: DCM 4'b0001: 1-phase CCM 4'b0010: 2-phase CCM Others: Invalid

MFR_PVID01_R3 (71h)

The MFR_PVID01_R3 command on Page 2 programs the rail 3 PVID voltage in PVID override mode.

Command	MFR_PVID01_R3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID1_R3	Sets the rail 3 PVID voltage for the PVID2, PVID1, and PVID0 pins = 3'b001. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID0_R3	Sets the rail 3 PVID voltage for the PVID2, PVID1, and PVID0 pins = 3'b000. It is in VID format. VID_STEP/LSB.

MFR_PVID23_R3 (72h)

The MFR_PVID23_R3 command on Page 2 programs the rail 3 PVID voltage in PVID override mode.

Command	MFR_PVID23_R3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID3_R3	Sets the rail 3 PVID voltage if the PVID2, PVID1, and PVID0 pins = 3'b011. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID2_R3	Sets the rail 3 PVID voltage if the PVID2, PVID1, and PVID0 pins = 3'b010. It is in VID format. VID_STEP/LSB.

MFR_PVID45_R3 (73h)

The MFR_PVID45_R3 command on Page 2 programs the rail 3 PVID voltage in PVID override mode.

Command	MFR_PVID45_R3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID5_R3	Sets the rail 3 PVID voltage for the PVID2, PVID1, and PVID0 pins = 3'b011. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID4_R3	Sets the rail 3 PVID voltage for the PVID2, PVID1, and PVID0 pins = 3'b010. It is in VID format. VID_STEP/LSB.

MFR_PVID67_R3 (74h)

The MFR_PVID67_R3 command on Page 2 programs the rail 3 PVID voltage in PVID override mode.

Command	MFR_PVID67_R3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	MFR_PVID7_R3	Sets the rail 3 PVID voltage for the PVID2, PVID1, and PVID0 pins = 3'b011. It is in VID format. VID_STEP/LSB.
7:0	MFR_PVID6_R3	Sets the rail 3 PVID voltage for the PVID2, PVID1, and PVID0 pins = 3'b010. It is in VID format. VID_STEP/LSB.

SAMPLE_INTERVAL_12PH_R3 (75h)

The SAMPLE_INTERVAL_12PH_R3 command sets the sample interval for 1-phase and 2-phase operation.

Command	SAMPLE_INTERVAL_12PH_R3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	SAMPLE_INTERVAL_2PH_R3	Sets the 2-phase sample interval. 50ns/LSB.
7:0	SAMPLE_INTERVAL_1PH_R3	Sets the 1-phase sample interval. 50ns/LSB.

CRC_USER_LAST (76h)

The CRC_USER_LAST command returns the user CRC code from the NVM.

Command	CRC_USER_LAST															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	CRC_USER_LAST	Saves the user CRC code from the NVM.

CRC_TRIM_LAST (77h)

The CRC_TRIM_LAST command returns the trim CRC code from the NVM.

Command	CRC_TRIM_LAST															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	CRC_TRIM_LAST	Saves the trim CRC code from the NVM.

STATUS_BYTE (78h)

The STATUS_BYTE command on Page 2 returns 1 byte of information with a summary of the most critical statuses and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								X

Bits	Bit Name	Behavior	Description
7	NVM_BUSY	Live	Reports the live status of the NVM. 1’b0: The NVM is idle. The NVM can write and read with PMBus commands 1’b1: The NVM is busy. The NVM cannot write and read with PMBus commands
6	OFF	Live	The rail 3 output is off. This bit is in live mode. It is asserted if the rail 3 output is off. V_{OUT} turns off due to protections, EN going low, or VID = 0. 1’b0: VOUT3 is on 1’b1: VOUT3 is off
5	VOUT_OV_FAULT	Latch	Rail 3 V_{OUT} over-voltage (OV) fault indicator. This bit is set and latched if rail 3 OVP occurs. The CLEAR_FAULTS (03h) command can reset this bit. (Absolute or VID.) 1’b0: No V_{OUT} OV fault has occurred 1’b1: A V_{OUT} OV fault has occurred

4	IOUT_OC_FAULT	Latch	Rail 3 output current over-current (OC) fault indicator. This bit is set and latched if rail 3 OCP occurs. The CLEAR_FAULTS (03h) command can reset this bit. (OCP_TDC and OCP_SPIKE.) 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
3	VIN_UV_FAULT	Latch	V_{IN} under-voltage (UV) fault indicator. This bit is set and latched if a V_{IN} UV fault occurs. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	TEMPERATURE	Latch	Over-temperature (OT) fault and warning indicator. This bit is set and latched if TSENS3 senses an OT condition, and OTP or an OT warning occurs. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Latch	PMBus communication fault indicator. If a PMBus communication fault occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	TSENS3_DIGI_FAULT	Latch	TSENS3 digital-sense fault indicator. If the TSENS3 sensed voltage exceeds or drops below a configurable level set by MFR_TSENS3_SET (36h, Page 1) bits[13:8], a TSENS3 fault occurs and this bit is set and latched. The TSENS3 sense fault response is determined by MFR_TSEN3_SET (36h, Page 1) bit[1]. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No TSENS3 digital-sense fault has occurred 1'b1: A TSENS3 digital-sense fault has occurred

STATUS_WORD (79h)

The STATUS_WORD (79h) command on Page 2 returns 2 bytes of information with a summary of the device fault/warning conditions. The higher byte gives more detailed information of the fault conditions. The lower byte shares the information with the STATUS_BYTE (78h) register.

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function						X	X		STATUS_BYTE(78H)							

Bits	Bit Name	Behavior	Description
15	VOUT	Live	Rail 3 V_{OUT} fault and warning indicator. If an output OV or UV protection or warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} fault or warning has occurred 1'b1: A V_{OUT} fault or warning has occurred
14	IOUT	Live	Rail 3 I_{OUT} fault and warning indicator. If an output current fault/warning or output power warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No I_{OUT} fault and warning has occurred 1'b1: An I_{OUT} fault or warning has occurred

13	INPUT	Latch	Input voltage, current, and power fault/warning indicator. If any protection or warning of the input voltage, input current, or input power occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No input fault and warning 1'b1: An input fault or warning has occurred
12	TSENS3	Latch	TSENS3 digital-sense fault indicator. If the TSENS3 voltage exceeds 2.2V, a TSENS3 fault occurs and this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No TSENS3 fault 1'b1: A TSENS3 fault has occurred
11	PG_NOT_ACTIVE	Live	1'b0: PG is active 1'b1: PG is not active
10:9	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
8	WATCH_DOG_OVF	Latch	The watchdog for the monitor block timer overflow indicator. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset. Meanwhile, this bit is set. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 2 returns 1 byte of information with the detailed V_{OUT} fault and warning status on rail 3.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X			X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Rail 3 V_{OUT} over-voltage (OV) fault indicator. If output OVP occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
6	VOUT_OV_WARNING	Live	Rail 3 V_{OUT} over-voltage (OV) warning indicator. If output OVP occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: no V_{OUT} OV warning has occurred 1'b1: A V_{OUT} OV warning has occurred
5	VOUT_UV_WARNING	LIVE	Rail 3 V_{OUT} under-voltage (UV) warning indicator. This bit is set if rail 1 UVP occurs. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} UV warning has occurred 1'b1: A V_{OUT} UV warning has occurred

4	VOUT_UV_FAULT	Latch	Rail 3 output voltage under-voltage (UV) fault indicator. This bit is set and latched if rail 1 UVP occurs. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{OUT} under-voltage (UV) fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN_ WARNING	Latch	Rail 3 V_{OUT} reaches VOUT_MAX or VOUT_MIN indicator. If the VID value exceeds the value set in VOUT_MAX (24h, Page 0) or VOUT_MIN (2Bh, Page 0), this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID has exceeded VOUT_MAX or is below VOUT_MIN
2	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
1	LINE_FLOAT	Latch	Rail 3 line float protection indicator. If a line float fault is detected, the device shuts down the associated rail and this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No line float fault has occurred 1'b1: A line float fault has occurred
0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 2 returns 1 byte of information with the detailed I_{OUT} fault and warning statuses for rail 3.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function				X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Rail 3 output over-current (OC) fault indicator. If output OCP occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. (OCP_TDC and OCP_SPIKE.) 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6	TDC_OCP_UV_FAULT	Latch	Rail 3 output over-current (OC) and under-voltage (UV) dual-fault indicator. If output OC occurs and the UV comparator is set simultaneously, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No output OC and UV faults have occurred 1'b1: Output OC has occurred and the UV comparator is set
5:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_INPUT (7Ch)

The STATUS_INPUT command returns 1 byte of information with detailed input fault and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X				X	X	

Bits	Bit Name	Behavior	Description
7	VIN_OVP	Latch	Input voltage over-voltage (OV) fault indicator. If the sensed input voltage exceeds the V_{IN} OV fault limit, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command on Page 2 returns 1 byte of information with temperature-related fault and warning conditions.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Over-temperature fault indicator. Once the temperature sensed via TSENS3 exceeds the OT fault limit set by MFR_OT_FAULT_LIMIT (4F, page2), this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
6	VRHOT	Live	VRHOT indicator. If the temperature sensed via TSENS2 exceeds the over-temperature (OT) warning limit set by MFR_VRHOT_SET (3Eh, Page 1), this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No VRHOT has occurred 1'b1: VRHOT has occurred
5:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_CML (7Eh)

The STATUS_CML command on Page 2 returns one byte of information with PMBus communication faults.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function					X			

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	Invalid PMBus command indicator. If the MP2926 receives an unsupported command code, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	INVALID_DATA	Latch	Invalid PMBus data indicator. If the MP2926 receives unsupported data, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received
5	PEC_ERROR	Latch	PMBus PEC fault indicator. The PMBus interface supports the use of the packet error checking (PEC) byte that is defined in the SMBus standard. The PEC byte is transmitted by the MP2926 during a read transaction, or sent to the MP2926 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed and PEC_FAULT is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4	NVM_CRC_ERROR	Latch	CRC fault indicator. In the process of storing operating memory data to the NVM, the MP2926 calculates a CRC code for each bit and saves the final CRC code to the NVM. In the process of restoring the NVM data to the operating memory, the MP2926 recalculates the CRC code with each bit. The MP2926 checks the CRC results when the restoration process is complete. If the CRC result does not match what is stored, the VR shuts down. The CRC_FAULT bit is then set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
3	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
2	CML_FLT_TRG	Latch	If an NVM operation is blocked because the controller is recording a fault to the NVM, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No NVM operation is blocked 1'b1: NVM operation is blocked because the controller is recording a fault to the NVM
1	CML_OTHER_FAULTS	Latch	This bit is set if any of the following PMBus communication faults occur: • Sending too few bits • Reading too few bits • Host sends or reads too few bytes • Reading too many bytes This bit is in latch mode. The CLEAR_FAULTS (03h) command can reset this bit.

0	NVM_SIG_FAULTS	Latch	While restoring data from the NVM to the memory, the device first checks the signature register in address 00h of the NVM. If the signature register is 0x1234, the restoration process is halted immediately and the NVM_SIG_FAULTS bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

READ_ADC_SUM (81h)

The READ_ADC_SUM command on Page 2 returns the sum of 16 consecutive ADC-sense results.

Command	READ_ADC_SUM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X		ADC_SUM													

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	ADC_SUM_READY	Indicates if the sum of 16 consecutive ADC-sense results is ready. 1'b0: The 16 ADC-sense result sum is not ready 1'b1: The 16 ADC-sense result sum is ready
13:0	ADC_SUM	Stores the sum of 16 consecutive ADC-sense results. Send FBh (0 byte) to start the ADC sum action.

READ_VFB3_SENSE (82h)

The READ_VFB3_SENSE command on Page 0 returns the ADC-sensed VFB voltage (V_{FB}).

Command	READ_VFB3_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_VFB3_SENSE	Returns the ADC-sensed V_{FB3} voltage in direct format. 1.56mV/LSB.

READ_TSENS2_SENSE (83h)

The READ_TSENS2_SENSE command on Page 2 reads the TSENS2 pin voltage.

Command	TEMP_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_TSENS2	Returns the ADC-sensed voltage on the TSENS2 pin in direct format. 1.56mV/LSB.

READ_CS3 (84h)

The READ_CS3 command on Page 2 returns the ADC-sensed average voltage on rail 2's CS3 pin in direct format. Add an internal low-pass filter before ADC sensing.

Command	READ_CS3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS3	Returns the ADC-sensed voltage on rail 2's CS3 in direct format. 3.125mV/LSB.

READ_CS4 (85h)

The READ_CS4 command on Page 2 returns the ADC-sensed average voltage on rail 2's CS4 pin in direct format. Add an internal low-pass filter before ADC sensing.

Command	READ_CS4															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS4	Returns the ADC-sensed voltage on rail 2's CS4 in direct format. 3.125mV/LSB.

READ_CS5 (86h)

The READ_CS5 command on Page 2 returns the ADC-sensed average voltage on rail 3's CS5 pin in direct format. Add an internal low-pass filter before ADC sensing.

Command	READ_CS5															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS5	Returns the ADC-sensed voltage on rail 3's CS5 in direct format. 3.125mV/LSB.

READ_CS6 (87h)

The READ_CS6 command on Page 2 returns the ADC-sensed average voltage on rail 3's CS6 pin in direct format. Add an internal low-pass filter before ADC sensing.

Command	READ_CS6															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:10	RESERVED	Fixed to 0.
9:0	READ_CS6	Returns the ADC-sensed voltage on rail 3's CS6 in direct format. 3.125mV/LSB.

READ_VIN (88h)

The READ_VIN command on Page 2 provides 2 bytes to return the sensed input voltage based on the VINSEN3 pin in Linear11 format. In VID mode, the returned value must ignore bits[15:11] exponent value.

Command	READ_VIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	1	1	0	1	1	X	READ_VIN									

Bits	Bit Name	Description
15:11	EXP	Unused. Fixed to 11011.
10	RESERVED	Fixed to 0.
9:0	READ_VIN	Returns the sensed input voltage in Linear11 format. 31.25mV/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 2 returns the sensed rail 3 VOSEN-VORTN voltage. K_R is the dividing ratio of the divider.

Command	READ_VOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	READ_VOUT										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	READ_VOUT	Returns the V_{OUT} value. Linear mode: 2mV/LSB. V_{OUT} can be calculated with the following equation: V_{OUT} = READ_VOUT x 2 x K_R Direct mode: VID_STEP/LSB. V_{OUT} can be calculated with the following equation: V_{OUT} = READ_VOUT x VID_STEP x K_R VID_STEP is decided by C1h bits[15:14]. K_R is the dividing ratio of the divider.

READ_IOUT (8Ch)

The READ_IOUT command on Page 2 returns the sensed output current of rail 3 in direct format.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP					READ_IOUT										

Bits	Bit Name	Description
15:11	EXP	It is determined by bit[5] of VR_CONFIG1 (C1h). C1h[5]= 1: 5'b11110 C1h[5]= 0: 5'b11111
10:0	READ_IOUT	Returns the sensed output current. It is determined by bit[5] of VR_CONFIG1 (C1h). C1h[5] = 1: 0.25A/LSB C1h[5] = 0: 0.5A/LSB

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 2 returns the temperature sensed on the TSENS2 pin in direct format.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	X	X	X	READ_TEMP							

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_TEMP	Returns the temperature sensed on the TSENS2 pin. 1°C/LSB.

READ_AD_RESULT (8Eh)

The READ_AD_RESULT command on Page 2 returns the ADC result.

Command	READ_AD_RESULT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_ADC									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_ADC	Returns the ADC value.

READ_VCOMP (8Fh)

The READ_VCOMP command on Page 2 returns the COMP value.

Command	READ_VCOMP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_VCOMP							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_VCOMP	Returns the COMP value.

READ_POUT (96h)

The READ_POUT command on Page 2 returns the P_{OUT} value for rail 3.

Command	READ_POUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:0	READ_POUT	Returns the output power. The read ADC value is the same as D1h. Convert the read value to the actual power (in W) with the following equation: $$P_{OUT}(W) = \frac{\frac{READ\_POUT \times 8}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}}{t_{SHORT\_TERM}}$$ Where GAIN_SEL is 6Ch bits[11:10], G_{VIDFF} is the V_{DIFF} gain setting from 4Dh bit[10]: 4Dh[10] = 0: G_{VIDFF} = 1 4Dh[10] = 1: G_{VIDFF} = 0.5 t_{SHORT_TERM} is the short-term time (in µs): 26h[15] = 0: t_{SHORT_TERM} = 26h[12:1] x 0.05µs 26h[15] = 1: t_{SHORT_TERM} = (26h[6:0] + 1) x (Page 2) 55h bits[13:8] x 0.05µs

CAPABILITY (D0h)

The CAPABILITY command is read-only.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
15:0	READ_POUT	Returns the output power. The read ADC value is the same as D1h. Convert the read value to the actual power (in W) with the following equation: $$P_{OUT}(W) = \frac{\frac{READ\_POUT \times 8}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}}{T_{SHORT\_TERM}}$$ Where GAIN_SEL is 6Ch bits[11:10], G_{VIDFF} is the V_{DIFF} gain setting from 4Dh bit[10]: 4Dh[10] = 0: G_{VIDFF} = 1 4Dh[10] = 1: G_{VIDFF} = 0.5 t_{SHORT_TERM} is the short-term time (in µs): 26h[15] = 0: t_{SHORT_TERM} = 26h[12:1] x 0.05µs 26h[15] = 1: t_{SHORT_TERM} = (26h[6:0] + 1) x (Page 2) 55h bits[13:8] x 0.05µs

CAPABILITY (D0h)

The CAPABILITY command is read-only.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7:0	CAPABILITY	Fixed to 0xC0.

JOUT3_SHORT_TERM (D1h)

The JOUT3_SHORT_TERM command on Page 2 returns the real-time J_{OUT} value in every short-term period.

Command	JOUT3_SHORT_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT3_SHORT_TERM															

Bits	Bit Name	Description
15:0	JOUT3_SHORT_TERM	Returns the real-time J_{OUT} value in every short-term period. Convert the read value to the actual output (in µJ) with the following equation: $J_{OUT\_SHORT\_TERM}(\mu J) = \frac{D1h \times 8}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch bits[11:10], and G_{VIDFF} is the V_{DIFF} gain setting from 4Dh bit[10]: 4Dh[10] = 0: G_{VIDFF} = 1 4Dh[10] = 1: G_{VIDFF} = 0.5

JOUT3_LONG_TERM (D2h)

The JOUT3_LONG_TERM command on Page 2 returns the J_{OUT} value in every long-term period.

Command	JOUT3_LONG_TERM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	JOUT3_LONG_TERM															

Bits	Bit Name	Description
15:0	JOUT3_LONG_TERM	Returns the real-time J_{OUT} value in every long-term period. Convert the read value to the actual output (in mJ) with the following equation: $J_{OUT\_LONG\_TERM}(mJ) = \frac{D2h \times 16.384}{6Ch[9:0] \times 1000} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)} \times \frac{1}{1.6 \times G_{VDIFF}}$ Where GAIN_SEL is 6Ch bits[11:10], and G_{VIDFF} is the V_{DIFF} gain setting from 4Dh bit[10]: 4Dh[10] = 0: G_{VIDFF} = 1 4Dh[10] = 1: G_{VIDFF} = 0.5

IMON3_FAST_SENSE (D3h)

The IMON3_FAST_SENSE command on Page 2 returns a J_{OUT} ADC value.

Command	IMON3_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IMON3_FAST_SENSE	Returns the I_{OUT} ADC value in J_{OUT} calculations. Convert the read value to the actual output current (in A) with the following equation: $$I_{OUT}(A) = \frac{D3h[9:0]}{6Ch[9:0]\times 1024} \times 6Eh[10:0] \times 2^{(6\text{-}GAIN\_SEL)}$$ Where GAIN_SEL is 6Ch bits[11:10].

VDIFF3_FAST_SENSE (D4h)

The VDIFF3_FAST_SENSE command on Page 2 returns the J_{OUT} ADC value.

Command	VDIFF3_FAST_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	VDIFF3_FAST_SENSE	Returns the V_{OUT} ADC value in J_{OUT} calculations. 1.56mV/LSB when the V_{DIFF} gain = 1 3.12mV/LSB when the V_{DIFF} gain = 1/2 Where the V_{DIFF} gain is set by 4Dh (Page 2) bit[10].

ADC_SUM_RESET (FBh)

The ADC_SUM_RESET command resets the ADC_SUM count.

This command is write-only. There is no data byte for this command.

CLEAR_CRC_FAULT (FCh)

The CLEAR_CRC_FAULT command clears the CRC fault information stored in NVM.

This command is write-only. There is no data byte for this command.

CLEAR_STORED_FAULTS (FEh)

The CLEAR_STORED_FAULTS command clears the last fault information stored in NVM.

This command is write-only. There is no data byte for this command.

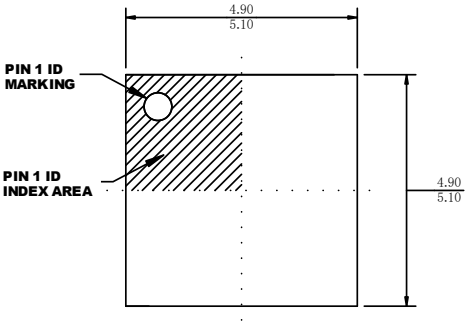
CLEAR_NVM_FAULTS (FFh)

The CLEAR_NVM_FAULTS command clears the NVM faults.

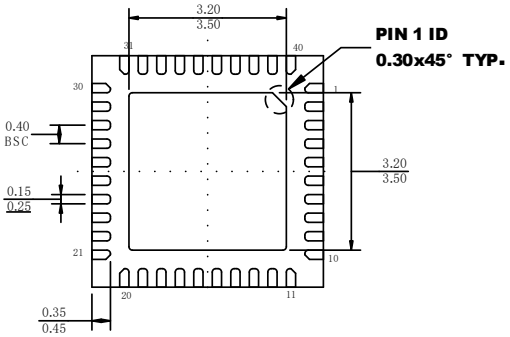
This command is write-only. There is no data byte for this command.

PACKAGE INFORMATION

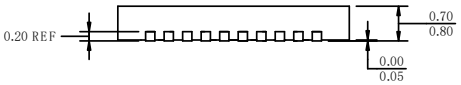
TQFN-40 (5mmx5mm)



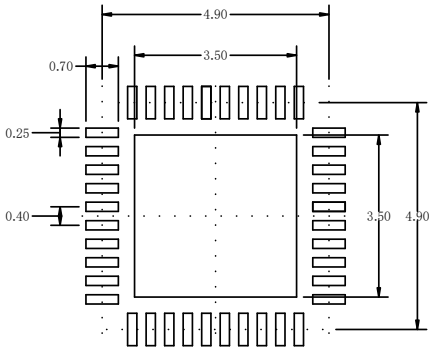
TOP VIEW



BOTTOM VIEW



SIDE VIEW

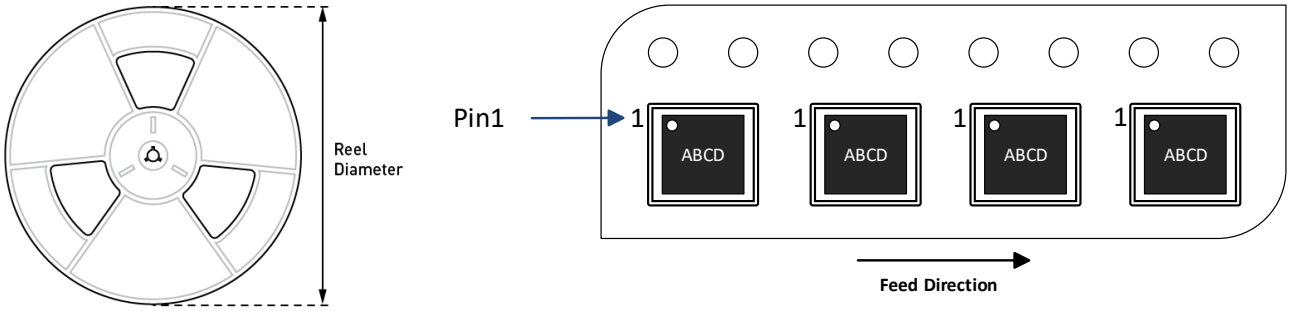


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION WHHE-1
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2926GUT-xxxx–Z	TQFN-40 (5mmx5mm)	5000	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	7/28/2020	Initial Release	-