

### DESCRIPTION

The MP2888A is a digital, multi-phase, pulse-width modulation (PWM) controller with digital PWM-VID interface compatible with the Open VReg specification. The MP2888A can work with MPS's Intelli-Phase products to complete the multi-phase voltage regulator (VR) solution with minimal external components. The MP2888A can be configured with up to 10-phase operation.

The MP2888A provides an on-chip EEPROM to store and restore device configurations. Device configurations and fault parameters can be easily programmed or monitored via the PMBus/I<sup>2</sup>C interface. The MP2888A can monitor and report the output current through the CS output from the Intelli-Phase products.

The MP2888A is based on a unique, digital, multi-phase, non-linear control and provides fast transient response to the load transient with minimal output capacitors. With only one power-loop control method for both steady state and load transient, the power loop compensation is very easy to configure.

The MP2888A is available in a QFN-40 (5mmx5mm) package.

### FEATURES

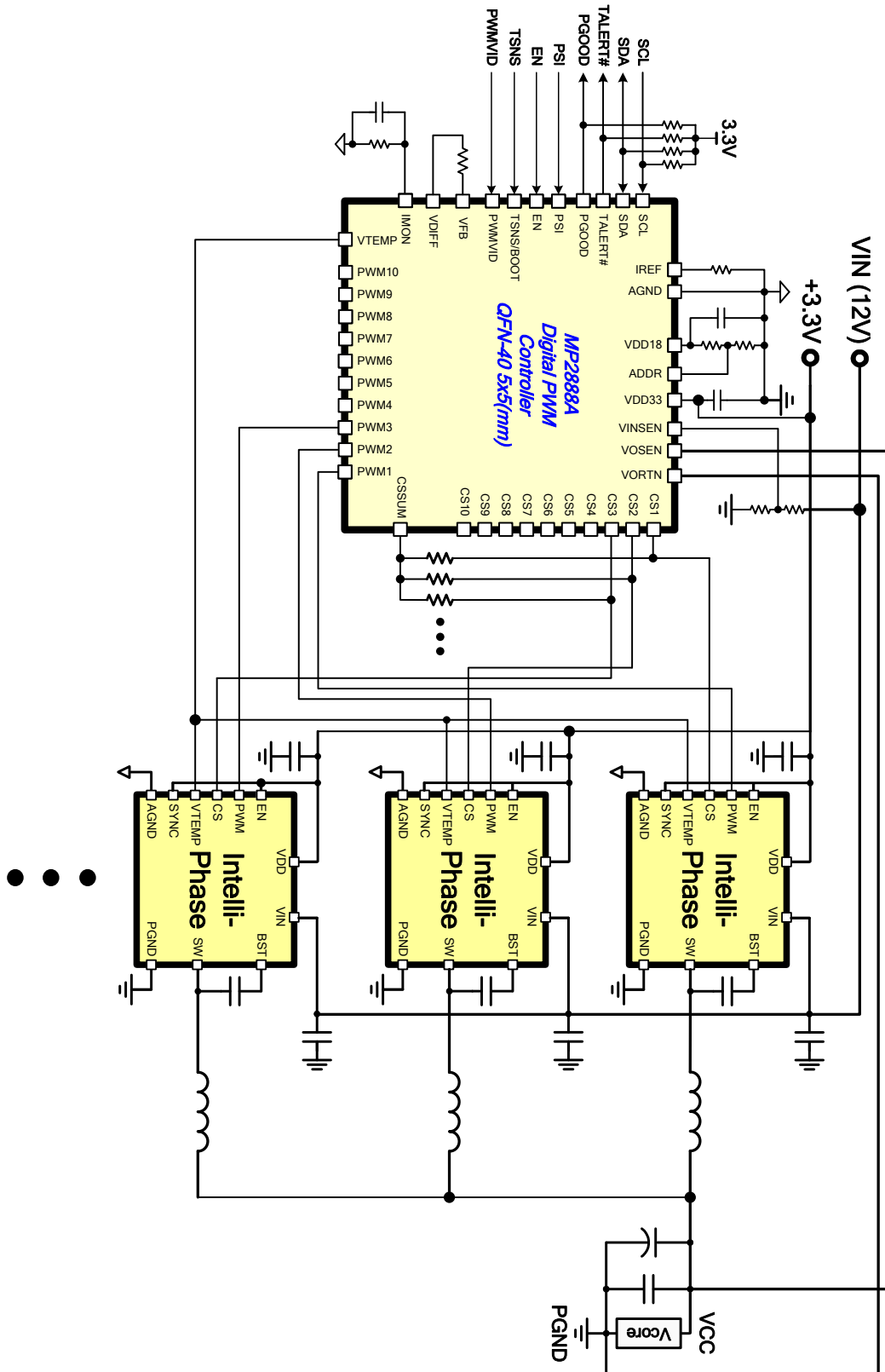
- Programmable Multi-Phase up to 10 Phases
- PWM-VID Interface Compatible with the Open VReg Specification
- PMBus/I<sup>2</sup>C Compliant (1MHz Bus Speed)
- Pin Programmable for PMBus Address
- Built-In EEPROM to Store Custom Configurations
- Switching Frequency Range 200kHz to 5MHz
- Automatic Loop Compensation
- Fewer External Components than Conventional Analog Controller
- Best Transient Performance with Non-Linear Digital Control
- Flexible Phase Assignment
- Auto-Phase Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing with Programmable Offsets for Thermal Balance
- Output Voltage/Current, Input Voltage/Power Monitoring
- Regulator Temperature Monitoring
- VIN UVLO, Output OVP/UVF, OCP, OTP with No Action, Latch, Retry, or Hiccup Mode Options
- Detecting for Intelli-Phase MOSFET Fault Type and Auto-Record to EEPROM
- Register Map Password Lock
- Digital Load-Line Regulation
- Available in an RoHS Compliant QFN-40 (5mmx5mm) Package

### APPLICATIONS

- Graphic Card Core Power
- Server Core Power
- Telecom and Networking Systems
- Base Stations

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# TYPICAL APPLICATION



Multi-Phase Application for PWM-VID

## ORDERING INFORMATION

| Part Number*     | Package          | Top Marking |
|------------------|------------------|-------------|
| MP2888AGU-xxxx** | QFN-40 (5mmx5mm) | See Below   |

\* For Tape & Reel, add suffix -Z (e.g. MP2888AGU-xxxx-Z)

\*\* “xxxx” is the configuration code identifier for the register settings stored in the EEPROM. Each “x” can be a hexadecimal value between 0 and F. Please work with an MPS FAE to create this unique number.

## TOP MARKING

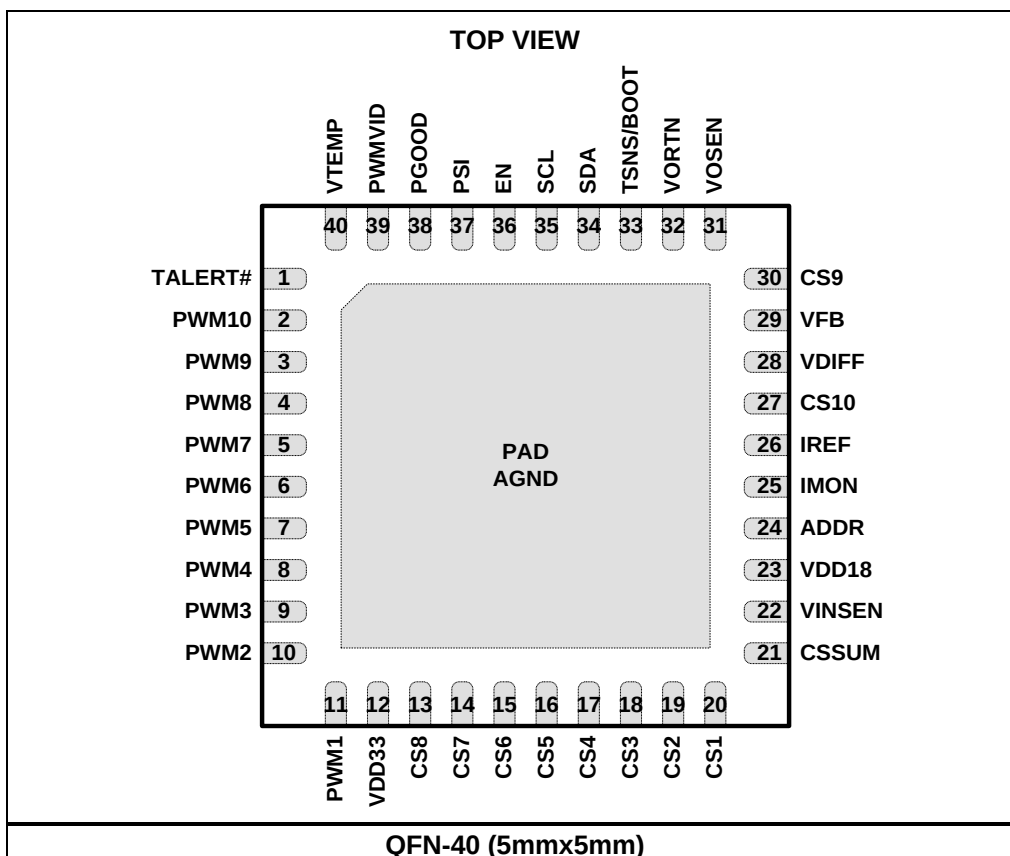
**MPSYYWW**

**MP2888A**

**LLLLLLL**

MPS: MPS prefix  
 YY: Year code  
 WW: Week code  
 MP2888A: Part number  
 LLLLLLL: Lot number

## PACKAGE REFERENCE



## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                                                              |                |
|--------------------------------------------------------------------------------------------------------------|----------------|
| VDD33 .....                                                                                                  | -0.3V to +4.0V |
| VDD18 .....                                                                                                  | -0.3V to +2.0V |
| CS1~10, PWM1~10, VFB, VDIFF, VOSEN, VORTN, PGOOD, PSI, SCL, SDA, TSNS/BOOT, TALERT#, PWMVID, EN, VTEMP ..... | -0.3V to +4.0V |
| CSSUM, IMON, IREF, VINSEN, ADDR .....                                                                        | -0.3V to +2.0V |
| Junction temperature .....                                                                                   | 150°C          |
| Lead temperature .....                                                                                       | 260°C          |
| Continuous power dissipation <sup>(2)</sup> .....                                                            | 3.47W          |

## Recommended Operating Conditions <sup>(3)</sup>

|                                        |                 |
|----------------------------------------|-----------------|
| Supply voltage ( $V_{IN}$ ) .....      | +3.0V to 3.6V   |
| Operating junction temp. ( $T_J$ ) ... | -40°C to +125°C |

| <b>Thermal Resistance <sup>(4)</sup></b> | <b><math>\theta_{JA}</math></b> | <b><math>\theta_{JC}</math></b> |
|------------------------------------------|---------------------------------|---------------------------------|
| QFN-40 (5mmx5mm) .....                   | 36 .....                        | 5 .... °C/W                     |

### NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 6-layer PCB.

## ELECTRICAL CHARACTERISTICS

VDD33 = 3.3V, EN = 1V, current going into the pin is positive. Typical values are at T<sub>A</sub> = 25°C.

| Parameter                                         | Symbol                                | Condition                                                                             | Min  | Typ            | Max | Units |
|---------------------------------------------------|---------------------------------------|---------------------------------------------------------------------------------------|------|----------------|-----|-------|
| <b>Remote Sense Amplifier</b>                     |                                       |                                                                                       |      |                |     |       |
| Bandwidth <sup>(5)</sup>                          | GBW <sub>(RSA)</sub>                  |                                                                                       |      | 20             |     | MHz   |
| VORTN1,2 current                                  | I <sub>RTN1,2</sub>                   | EN = 1V, VOSEN1,2 = 3V,<br>VORTN = 0V                                                 |      | -38            |     | μA    |
| VOSEN1,2 current                                  | I <sub>VOSEN1,2</sub>                 | EN = 1V, VOSEN1,2 = 3V,<br>VORTN = 0V                                                 |      | 38             |     | μA    |
| <b>Oscillator</b>                                 |                                       |                                                                                       |      |                |     |       |
| Frequency                                         | f <sub>OSC</sub>                      | V <sub>IREF</sub> = 1.23V, R <sub>IREF</sub> = 61.9kΩ                                 |      | 1.56           |     | MHz   |
| <b>System Interface Control Inputs</b>            |                                       |                                                                                       |      |                |     |       |
| <b>Enable (EN)</b>                                |                                       |                                                                                       |      |                |     |       |
| Input low voltage                                 | V <sub>IL(EN)</sub>                   |                                                                                       |      |                | 0.4 | V     |
| Input high voltage                                | V <sub>IH(EN)</sub>                   |                                                                                       | 0.8  |                |     | V     |
| Enable high leakage                               | I <sub>IH(EN)</sub>                   | EN = 2V                                                                               |      |                | 2.3 | μA    |
| <b>IMON Output</b>                                |                                       |                                                                                       |      |                |     |       |
| Current gain                                      | I <sub>MON</sub> /I <sub>CS_SUM</sub> | Measured from I <sub>CS_SUM</sub> to I <sub>MON</sub> ,<br>I <sub>CS_SUM</sub> = -2mA |      | 1:16           |     | μA/μA |
| Current gain accuracy                             |                                       |                                                                                       | -1   |                | 1   | %     |
| <b>PWM-VID</b>                                    |                                       |                                                                                       |      |                |     |       |
| Input low voltage                                 | PWM <sub>VIDL</sub>                   |                                                                                       |      |                | 0.4 | V     |
| Input mid-state                                   | PWM <sub>HIZ</sub>                    |                                                                                       |      | 0.9            |     | V     |
| Input high voltage                                | PWM <sub>VIDH</sub>                   |                                                                                       | 1.4  |                |     | V     |
| <b>PSI</b>                                        |                                       |                                                                                       |      |                |     |       |
| Input low voltage                                 | PSI <sub>L</sub>                      |                                                                                       |      |                | 0.4 | V     |
| Input mid-state                                   | PSI <sub>M</sub>                      |                                                                                       |      | 0.9            |     | V     |
| Input high voltage                                | PSI <sub>H</sub>                      |                                                                                       | 1.4  |                |     | V     |
| <b>PWM Outputs</b>                                |                                       |                                                                                       |      |                |     |       |
| Output low voltage                                | V <sub>OL</sub> (PWM)                 | I <sub>PWM(SINK)</sub> = 400μA                                                        |      | 10             | 200 | mV    |
| Output middle voltage                             | V <sub>OM</sub> (PWM)                 | I <sub>PWM(SOURCE)</sub> = -100μA                                                     |      | 1.36           |     | V     |
| Output high voltage                               | V <sub>OH</sub> (PWM)                 | I <sub>PWM(SOURCE)</sub> = -400μA                                                     | 3.15 | VDD33<br>-0.02 |     | V     |
| Rise and fall time <sup>(5)</sup>                 |                                       | C = 10pF                                                                              |      | 10             |     | ns    |
| PWM tri-state leakage                             |                                       | PWM = 1.5V, EN = 0V                                                                   | -1   |                | 1   | μA    |
| PWM fault detection source current <sup>(5)</sup> | I <sub>source(PWM)</sub>              | Enter PWM fault detect mode                                                           |      | 150            |     | μA    |
| <b>TSNS</b>                                       |                                       |                                                                                       |      |                |     |       |
| Current source                                    | I <sub>TSNS</sub>                     |                                                                                       |      | 10             |     | μA    |

# ELECTRICAL CHARACTERISTICS (continued)

VDD33 = 3.3V, EN = 1V, current going into the pin is positive. Typical values are at T<sub>A</sub> = 25°C.

| Parameter                                   | Symbol                | Condition                                                 | Min   | Typ  | Max   | Units |
|---------------------------------------------|-----------------------|-----------------------------------------------------------|-------|------|-------|-------|
| <b>Comparator (Protection)</b>              |                       |                                                           |       |      |       |       |
| Under-voltage threshold                     |                       | Relative to reference DAC voltage (2Ch bit[2:0] = 3b'001) |       | -190 |       | mV    |
|                                             |                       | Relative to reference DAC voltage (2Ch bit[2:0] = 3b'010) |       | -310 |       | mV    |
|                                             |                       | Relative to reference DAC voltage (2Ch bit[2:0] = 3b'100) |       | -430 |       | mV    |
| Over-voltage threshold                      |                       | Relative to reference DAC voltage (2Ch bit[2:0] = 3b'001) |       | 190  |       | mV    |
|                                             |                       | Relative to reference DAC voltage (2Ch bit[2:0] = 3b'010) |       | 310  |       | mV    |
|                                             |                       | Relative to reference DAC voltage (2Ch bit[2:0] = 3b'100) |       | 430  |       | mV    |
| <b>VDD33 Supply</b>                         |                       |                                                           |       |      |       |       |
| Supply voltage range                        | VDD33                 |                                                           | 3.0   | 3.3  | 3.6   | V     |
| Supply current                              | I <sub>VDD33</sub>    | EN = high or programmed as non-low-power mode             |       | 30   |       | mA    |
|                                             |                       | EN = 0 and programmed as low-power mode                   |       | 150  |       | μA    |
| UVLO threshold voltage                      | VDD33 <sub>UVLO</sub> | VDD33 is rising                                           |       | 2.88 | 2.98  | V     |
|                                             | VDD33 <sub>UVLO</sub> | VDD33 is falling                                          | 2.68  | 2.80 |       | V     |
| <b>1.8V Regulator</b>                       |                       |                                                           |       |      |       |       |
| 1.8V regulator output voltage               | VDD18                 | I <sub>VDD18</sub> = 0mA                                  |       | 1.8  |       | V     |
| 1.8v regulator load capability              | I <sub>VDD18</sub>    | VOL = VDD18 - 40mV                                        |       | 30   |       | mA    |
| <b>ADC</b>                                  |                       |                                                           |       |      |       |       |
| ADC Voltage reference                       |                       |                                                           | 1.592 | 1.6  | 1.608 | V     |
| ADC resolution                              |                       |                                                           |       | 10   |       | bits  |
| DNL <sup>(5)</sup>                          |                       |                                                           |       |      | 1     | LSB   |
| Sample rate <sup>(5)</sup>                  |                       |                                                           |       | 700  |       | kHz   |
| <b>DAC (Reference Voltage)</b>              |                       |                                                           |       |      |       |       |
| DAC voltage reference                       | FS <sub>ADC</sub>     |                                                           |       | 1.7  |       | V     |
| Resolution/LSB                              | Δ <sub>ADC</sub>      |                                                           |       | 6.25 |       | mV    |
| Max output voltage slew rate <sup>(5)</sup> |                       |                                                           |       | 50   |       | mV/μs |
| <b>OC_DAC (Protection)</b>                  |                       |                                                           |       |      |       |       |
| Range <sup>(5)</sup>                        | FS <sub>DAC_PRT</sub> | Adjustable via the PMBus                                  | 0.17  |      | 2.72  | V     |
| Resolution/LSB <sup>(5)</sup>               | Δ <sub>DAC_PRT</sub>  |                                                           |       | 10   |       | mV    |
| <b>PMBus DC Characteristics (SDA, SCL)</b>  |                       |                                                           |       |      |       |       |
| Input high voltage                          | V <sub>IH</sub>       |                                                           | 1.35  |      |       | V     |
| Input low voltage                           | V <sub>IL</sub>       |                                                           |       |      | 0.8   | V     |
| Input leakage current                       |                       |                                                           | -10   |      | 10    | μA    |
| Pin capacitance <sup>(5)</sup>              | C <sub>PIN</sub>      |                                                           |       |      | 10    | pF    |

# ELECTRICAL CHARACTERISTICS (continued)

VDD33 = 3.3V, EN = 1V, current going into the pin is positive. Typical values are at T<sub>A</sub> = 25°C.

| Parameter                                                 | Symbol | Condition                        | Min  | Typ | Max  | Units |
|-----------------------------------------------------------|--------|----------------------------------|------|-----|------|-------|
| <b>PMBus Timing Characteristics (1MHz) <sup>(6)</sup></b> |        |                                  |      |     |      |       |
| Operating frequency range                                 |        |                                  | 10   |     | 1000 | kHz   |
| Bus free time                                             |        | Between stop and start condition | 0.5  |     |      | μs    |
| Holding time                                              |        |                                  | 0.26 |     |      | μs    |
| Repeated start condition set-up time                      |        |                                  | 0.26 |     |      | μs    |
| Stop condition set-up time                                |        |                                  | 0.26 |     |      | μs    |
| Data hold time                                            |        |                                  | 0    |     |      | ns    |
| Data set-up time                                          |        |                                  | 50   |     |      | ns    |
| Clock low time-out                                        |        |                                  | 25   |     | 35   | ms    |
| Clock low period                                          |        |                                  | 0.5  |     |      | μs    |
| Clock high period                                         |        |                                  | 0.26 |     | 50   | μs    |
| Clock/data fall time                                      |        |                                  |      |     | 120  | ns    |
| Clock/data rise time                                      |        |                                  |      |     | 120  | ns    |

## NOTE:

- 5) Guaranteed by design or characterization data, not tested in production.
- 6) The device supports 100kHz, 400kHz, and 1MHz bus speeds. The PMBus timing parameters in this table is for operation at 1MHz. If the PMBus operating frequency is 100kHz or 400kHz, refer to the SMBus specification for timing parameters.

## PIN FUNCTIONS

| Package Pin # | Name    | Type <sup>(7)</sup> | Description                                                                                                                                                                                                                                                                              |
|---------------|---------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1             | TALERT# | D [O]               | <b>Open-drain VR thermal indicator.</b> TALERT# is pulled low if the temperature exceeds the programmed threshold from either VTEMP or TSNS.                                                                                                                                             |
| 2             | PWM10   | D [O]               | <b>Tri-state logic-level PWM outputs.</b> Each output is connected to the PWM input of the Intelli-Phase. The low logic level is 0V. The high logic level is 3.3V. The mid-state logic level is 1.5V (or high impedance). Float PWMx if it is not being used.                            |
| 3             | PWM9    | D [O]               |                                                                                                                                                                                                                                                                                          |
| 4             | PWM8    | D [O]               |                                                                                                                                                                                                                                                                                          |
| 5             | PWM7    | D [O]               |                                                                                                                                                                                                                                                                                          |
| 6             | PWM6    | D [O]               |                                                                                                                                                                                                                                                                                          |
| 7             | PWM5    | D [O]               |                                                                                                                                                                                                                                                                                          |
| 8             | PWM4    | D [O]               |                                                                                                                                                                                                                                                                                          |
| 9             | PWM3    | D [O]               |                                                                                                                                                                                                                                                                                          |
| 10            | PWM2    | D [O]               |                                                                                                                                                                                                                                                                                          |
| 11            | PWM1    | D [O]               |                                                                                                                                                                                                                                                                                          |
| 12            | VDD33   | Power               | <b>3.3V power supply input.</b> Connect a 1 $\mu$ F bypass capacitor from VDD33 to AGND.                                                                                                                                                                                                 |
| 13            | CS8     | A [I]               | <b>Phase 1~8 current sense input.</b> Short CSx to AGND or CSSUM if it is not being used.                                                                                                                                                                                                |
| 14            | CS7     | A [I]               |                                                                                                                                                                                                                                                                                          |
| 15            | CS6     | A [I]               |                                                                                                                                                                                                                                                                                          |
| 16            | CS5     | A [I]               |                                                                                                                                                                                                                                                                                          |
| 17            | CS4     | A [I]               |                                                                                                                                                                                                                                                                                          |
| 18            | CS3     | A [I]               |                                                                                                                                                                                                                                                                                          |
| 19            | CS2     | A [I]               |                                                                                                                                                                                                                                                                                          |
| 20            | CS1     | A [I]               |                                                                                                                                                                                                                                                                                          |
| 21            | CSSUM   | A [I]               | <b>Total phase current sensing input.</b> CSSUM is used for load-line and over-current protections. Connect the active phases' CS signals together to CSSUM through the current-sense resistors.                                                                                         |
| 22            | VINSEN  | A [I]               | <b>Input voltage sensing.</b> Place a resistor divider from the power stage (V <sub>IN</sub> ) to VINSEN.                                                                                                                                                                                |
| 23            | VDD18   | Power               | <b>1.8V LDO output.</b> VDD18 provides a power supply for the internal digital circuit. Connect a 1 $\mu$ F bypass capacitor from VDD18 to AGND.                                                                                                                                         |
| 24            | ADDR    | A [I]               | <b>PMBus address setting.</b>                                                                                                                                                                                                                                                            |
| 25            | IMON    | A [I/O]             | <b>Analog total average current sensing signal.</b> IMON sources a current proportional to the sensed total average current from CSSUM. IMON is used for load current reporting.                                                                                                         |
| 26            | IREF    | A [I/O]             | <b>Internal bias current set.</b> Connect a 61.9k $\Omega$ , 1% accuracy resistor from IREF to AGND.                                                                                                                                                                                     |
| 27            | CS10    | A [I]               | <b>Phase 10 current sense input.</b> Short CS10 to AGND or CSSUM if it is not being used.                                                                                                                                                                                                |
| 28            | VDIFF   | A [O]               | <b>Output of the differential remote sense amplifier.</b>                                                                                                                                                                                                                                |
| 29            | VFB     | A [I/O]             | <b>Feedback.</b> VFB sources a current (I <sub>droop</sub> ) proportional to the sensed output current. This current flows through the resistor (R <sub>droop</sub> ) between VFB and VDIFF to create a voltage drop proportional to the load current to achieve the load-line function. |

## PIN FUNCTIONS *(continued)*

| Package Pin # | Name      | Type <sup>(7)</sup> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------------|-----------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30            | CS9       | A [I]               | <b>Phase 9 current sense input.</b> Short CS9 to AGND or CSSUM if it is not being used.                                                                                                                                                                                                                                                                                                                                                                                            |
| 31            | VOSEN     | A [I]               | <b>Remote voltage sensing positive input.</b> VOSEN is connected to the VR output voltage directly at the load. Route VOSEN with VORTN differentially.                                                                                                                                                                                                                                                                                                                             |
| 32            | VORTN     | A [I]               | <b>Remote voltage sensing return input.</b> VORTN is connected to the ground directly at the load. Route VORTN with VOSEN differentially.                                                                                                                                                                                                                                                                                                                                          |
| 33            | TSNS/BOOT | A [I/O]             | <p><b>Thermistor thermal sensing input or boot voltage setting.</b> TSNS/BOOT can be programmed for either thermistor thermal sensing or boot voltage setting.</p> <p>When used as TSNS, the controller compares the voltage of TSNS/BOOT to an internal programmable threshold. Once triggered, TALERT# is asserted, and VR enters a pre-programmed protection mode.</p> <p>When used as BOOT, a voltage divider is required from VDD18 to TSNS/BOOT to set the boot voltage.</p> |
| 34            | SDA       | D [I/O]             | <b>PMBus data.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 35            | SCL       | D [I]               | <b>PMBus clock.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 36            | EN        | D [I]               | <b>Enable control.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 37            | PSI       | A [I]               | <b>Power saving interface.</b> 1.8V logic. When PSI is 1, all phases have forced continuous conduction mode (CCM). When PSI is 0, there is an adjustable low-phase count. When PSI is in Hi-Z, auto-phase-shedding is enabled.                                                                                                                                                                                                                                                     |
| 38            | PGOOD     | D [O]               | <b>Power good indication.</b> PGOOD is an open-drain output. PGOOD asserts when the output voltage is in regulation.                                                                                                                                                                                                                                                                                                                                                               |
| 39            | PWMVID    | A [I]               | <b>PWM-VID signal input.</b> PWMVID is a 1.8V logic. Connect the PWM-VID signal to PWMVID. The VR calculates the target VID based on the duty.                                                                                                                                                                                                                                                                                                                                     |
| 40            | VTEMP     | A [I]               | <b>Analog signal from the VR to the controller.</b> VTEMP indicates the maximum temperature of the power stages. The MP2888A supports temperature sensing from the Intelli-Phase power stages. Tie all temperature reporting pins from the Intelli-Phase together to produce the maximum value on the VTEMP bus.                                                                                                                                                                   |
| PAD           | AGND      | Power               | <b>Analog ground.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

### NOTE:

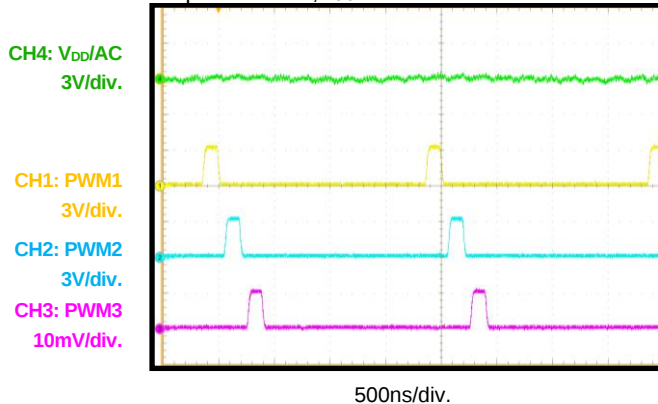
7) A = analog, D = digital, I = input, O = output, I/O = bidirectional.

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $C_{OUT} = 6400\mu F$ ,  $R_{IMON} = 4.42k\Omega$ , PGOOD is pulled up to +3.3V.  $T_A = +25^\circ C$ , unless otherwise noted.

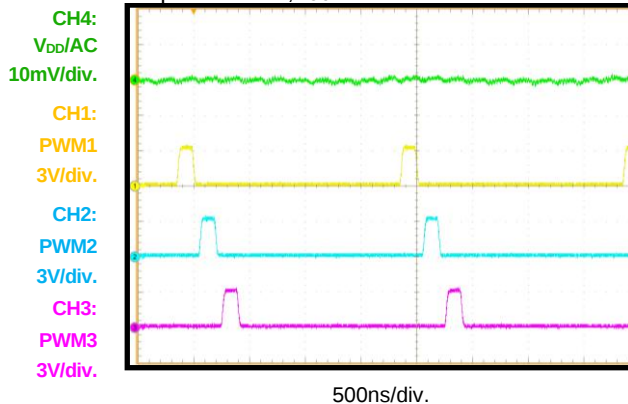
## Steady State

$V_{IN} = 12V$ ,  $V_{DD1} = 0.8V$ ,  $F_{SW} = 500kHz$ ,  
10-phase CCM,  $I_{OUT} = 0A$



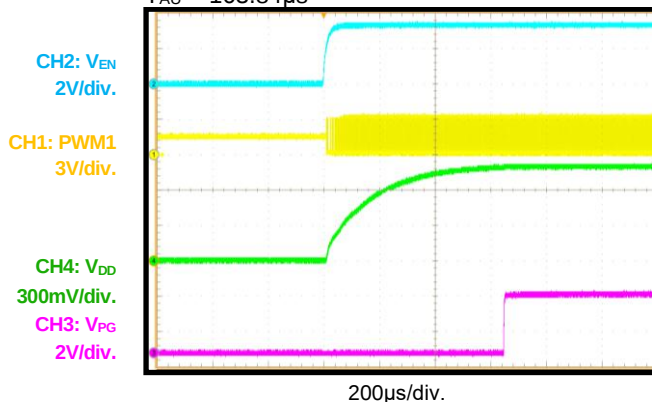
## Steady State

$V_{IN} = 12V$ ,  $V_{DD} = 0.8V$ ,  $F_{SW} = 500kHz$ ,  
10-phase CCM,  $I_{OUT} = 60A$



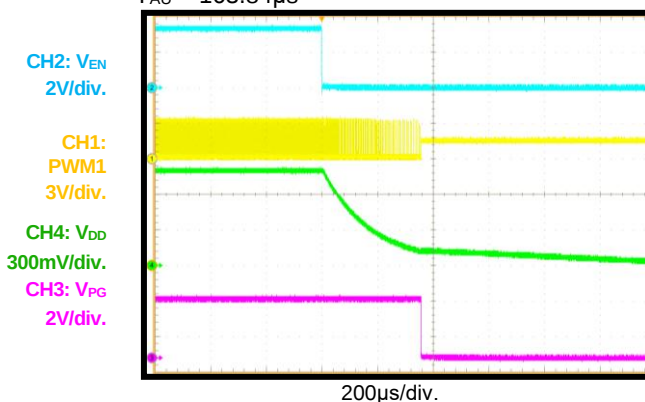
## EN Power On

$V_{IN} = 12V$ ,  $V_{BOOST} = 0.8V$ , RC slew rate,  
 $T_{AU} = 163.84\mu s$



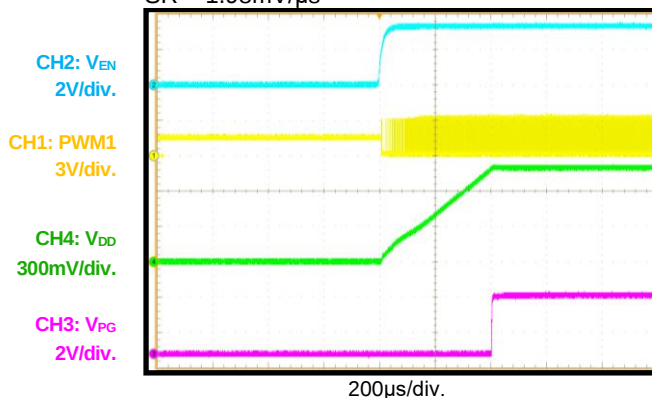
## EN Soft Off

$V_{IN} = 12V$ ,  $V_{BOOST} = 0.8V$ , RC slew rate,  
 $T_{AU} = 163.84\mu s$



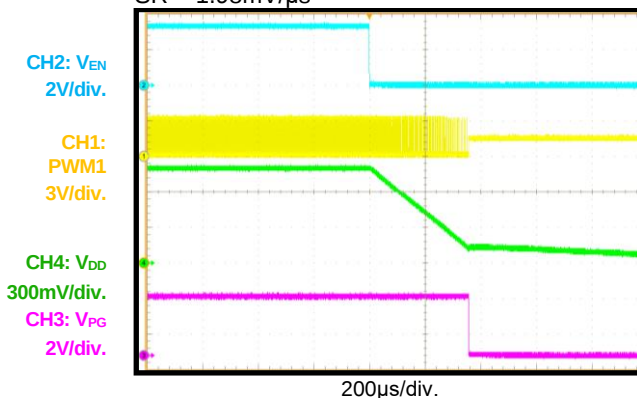
## EN Power On

$V_{IN} = 12V$ ,  $V_{BOOST} = 0.8V$ , linear slew rate,  
 $SR = 1.98mV/\mu s$



## EN Soft Off

$V_{IN} = 12V$ ,  $V_{BOOST} = 0.8V$ , linear slew rate,  
 $SR = 1.98mV/\mu s$

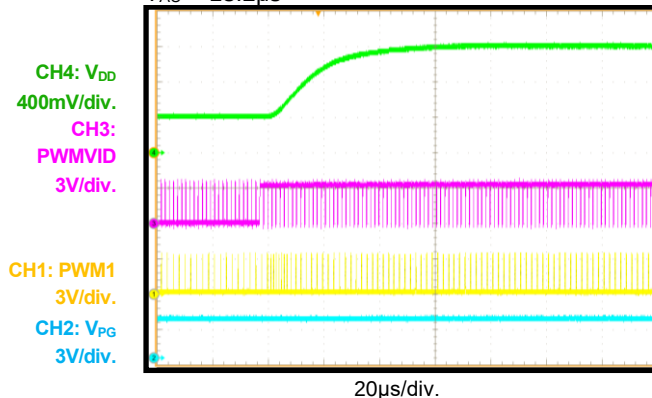


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $C_{OUT} = 6400\mu F$ ,  $R_{IMON} = 4.42k\Omega$ , PGOOD is pulled up to +3.3V.  $T_A = +25^\circ C$ , unless otherwise noted.

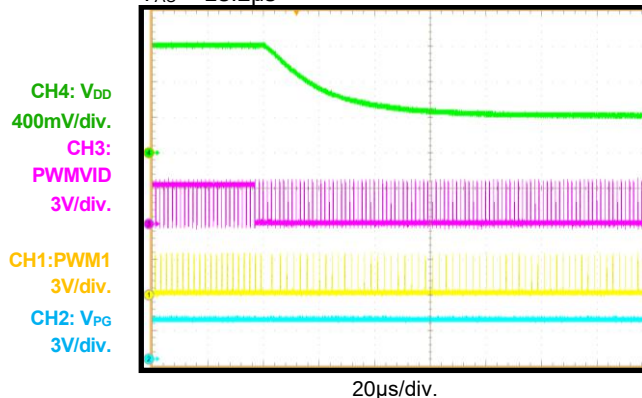
## DVID Up

DVID from 0.4V to 1.2V, RC slew rate,  
 $T_{AU} = 18.2\mu s$



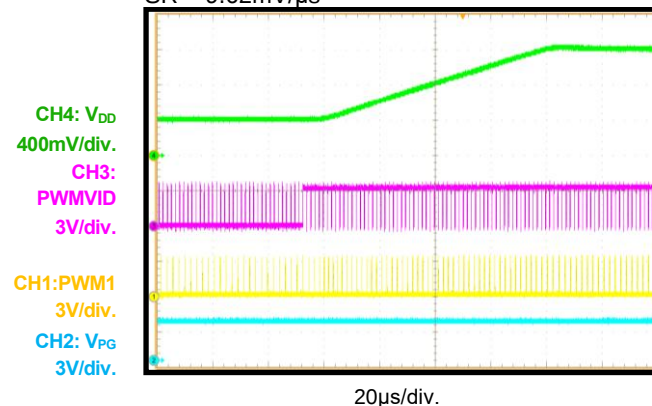
## DVID Down

DVID from 1.2V to 0.4V, RC slew rate,  
 $T_{AU} = 18.2\mu s$



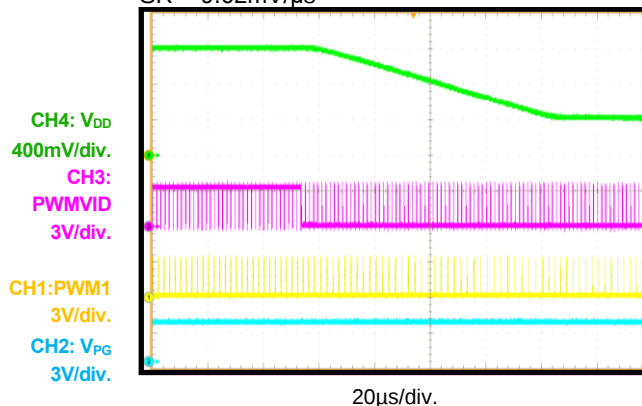
## DVID Up

DVID from 0.4V to 1.2V, linear slew rate,  
 $SR = 9.62mV/\mu s$



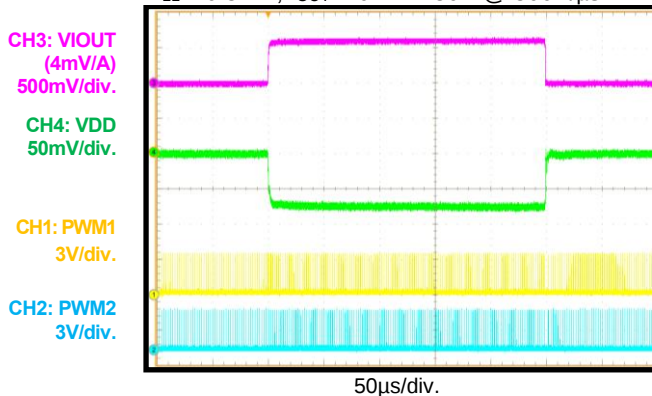
## DVID Down

DVID from 1.2V to 0.4V, linear slew rate,  
 $SR = 9.62mV/\mu s$



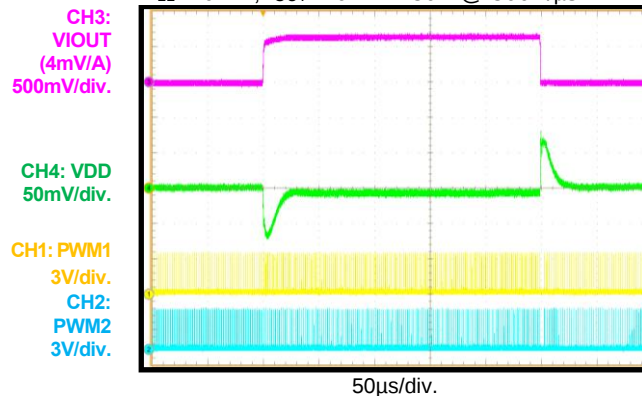
## Load Transient with DC Load Line

$V_{IN} = 12V$ ,  $V_{DD} = 1V$ ,  $F_{SW} = 500kHz$ ,  
 $R_{LL} = 0.5m\Omega$ ,  $I_{OUT} = 0 \leftrightarrow 150A @ 500A/\mu s$



## Load Transient with AC Load Line

$V_{IN} = 12V$ ,  $V_{DD} = 1V$ ,  $F_{SW} = 500kHz$ ,  
 $R_{LL} = 0m\Omega$ ,  $I_{OUT} = 0 \leftrightarrow 150A @ 500A/\mu s$

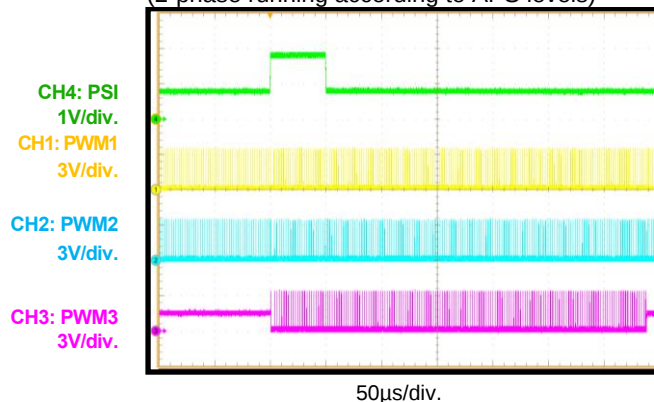


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $C_{OUT} = 6400\mu F$ ,  $R_{IMON} = 4.42k\Omega$ , PGOOD is pulled up to +3.3V.  $T_A = +25^\circ C$ , unless otherwise noted.

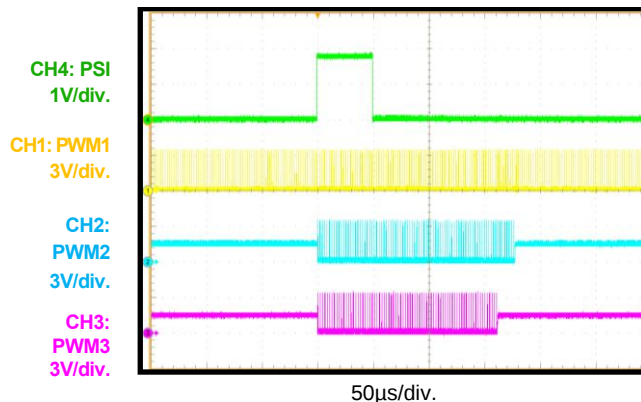
## PSI Changes between High- and Middle-State

Enable APS, low phase count = 1,  $I_{OUT} = 20A$   
(2-phase running according to APS levels)



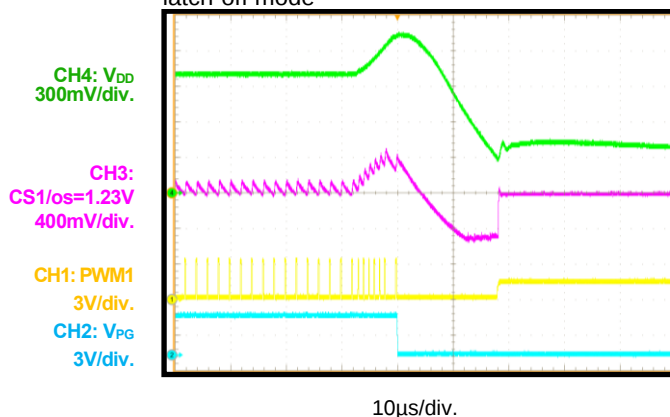
## PSI Changes between High and Low

Enable APS, low phase count = 1,  $I_{OUT} = 20A$   
(2-phase running according to APS levels)



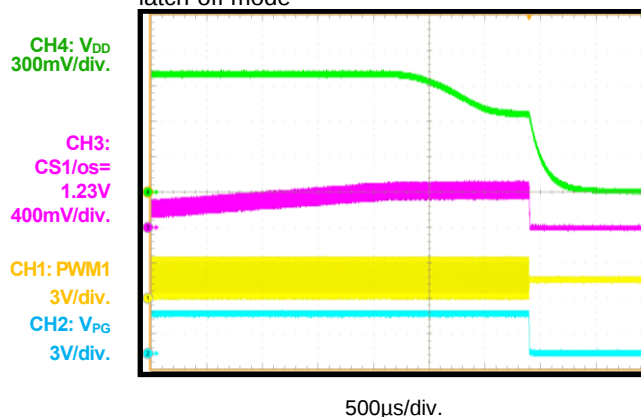
## OVP

$V_{IN} = 12V$ ,  $V_{DD} = 1V$ , OVP delay time = 0.5µs,  
latch-off mode



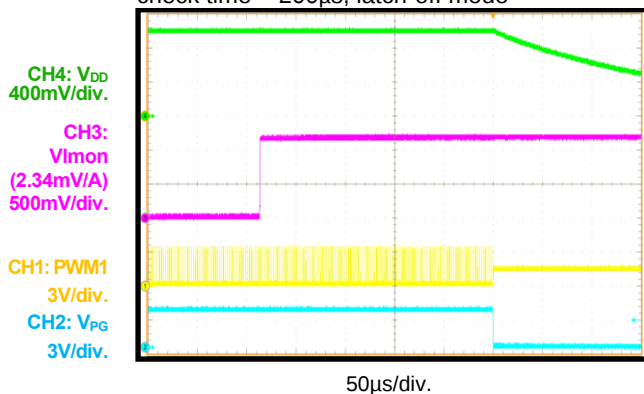
## UVP

$V_{IN} = 12V$ ,  $V_{DD} = 1V$ , UVP delay time = 400µs,  
latch-off mode



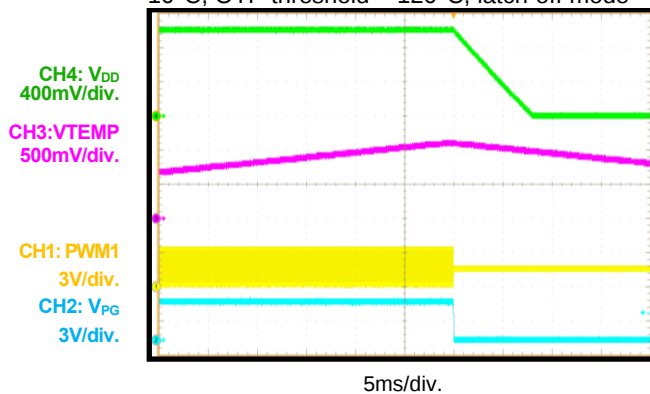
## OCP

$V_{IN} = 12V$ ,  $V_{DD} = 1V$ , OCP threshold = 500A,  
check time = 200µs, latch-off mode



## OTP

$V_{IN} = 12V$ ,  $V_{DD} = 1V$ ,  $T_J = (100^\circ C/V) * V_{TEMP} + 10^\circ C$ , OTP threshold = 120°C, latch-off mode



# BLOCK DIAGRAM

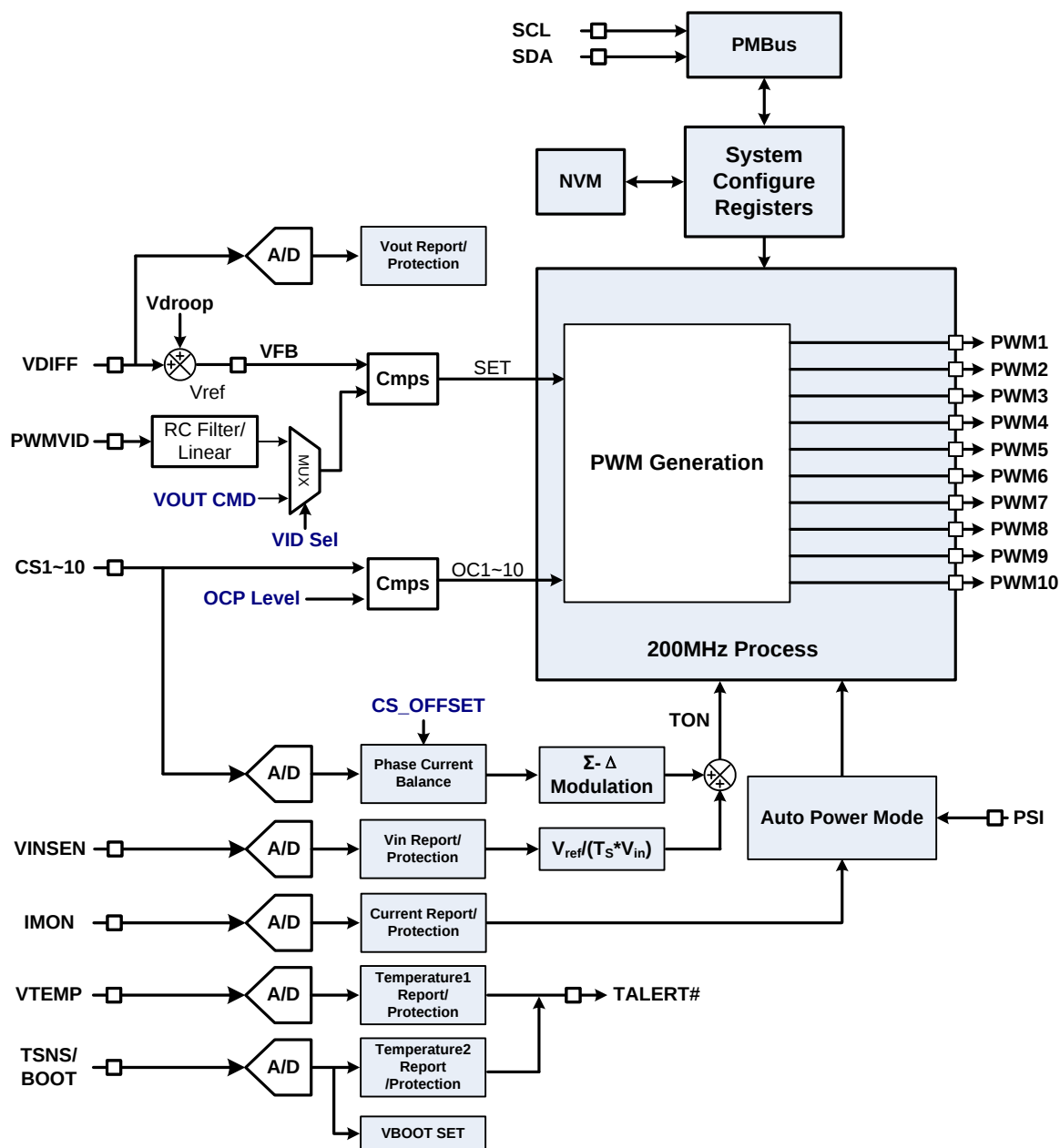


Figure 1: System Functional Block

## OPERATION

The MP2888A is a single-output, digital, multi-phase voltage regulator (VR) controller for high-performance GPU or CPU. It supports PWM-VID's controllable  $V_{OUT}$  reference and is compliant with the Open VReg specification.

The MP2888A uses MPS's unique loop compensation strategy to balance and optimize the steady and transient performance. It also adopts adaptive phase-shedding and phase-adding strategies to optimize the overall VR efficiency according to the load current.

The MP2888A contains precision DAC and ADC, differential remote voltage sense amplifier, fast comparators, current-sense amplifiers, internal slope compensation, digital load-line setting, power good monitor, and temperature monitor.

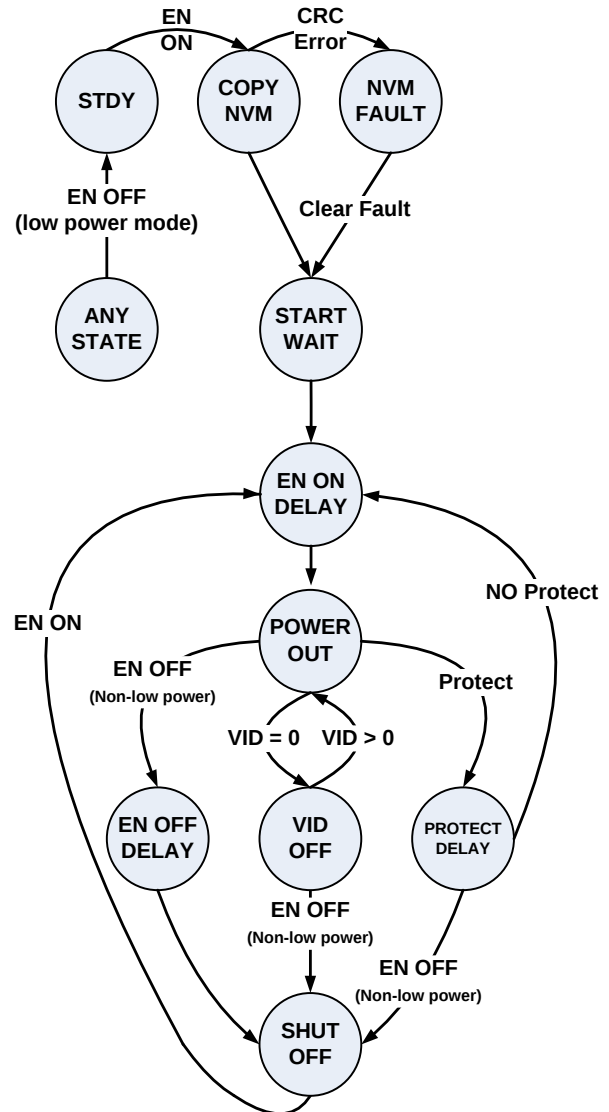
The MP2888A provides rich programmable functions with PMBus 1.3 interface. On-chip EEPROM is flexible for storing custom configurations and auto-records the fault type when a protection occurs.

Fault protection features include  $V_{IN}$  under-voltage lockout (UVLO),  $V_{IN}$  over-voltage protection (OVP),  $V_{OUT}$  over-voltage protection (OVP),  $V_{OUT}$  under-voltage protection (UVP),  $V_{OUT}$  reverse-voltage protection (RVP), output over-current protection (OCP), and over-temperature protection (OTP).

PMBus-programmable functions include phase assignment, switching frequency, reference voltage, loop stability parameters, protection thresholds and behaviors, load-line parameters, and so on.

The MP2888A can also detect the fault type of the Intelli-Phase when a protection occurs. The MP2888A can record all faults into the EEPROM automatically in case the power supply shuts off while the fault is occurring.

The MP2888A system state machine is shown in Figure 2.



**Figure 2: System State Machine**

### PWM Control and Switching Frequency

The MP2888A applies MPS's unique digital pulse-width modulation (PWM) control to provide fast load transient response and easy loop compensation. The switching frequency can be set with the PMBus command MFR\_FS (BDh).

The PWM on-time of each phase updates in real time according to the input voltage, output voltage, and the phase switching frequency adaptively.  $T_{on}$  can be calculated with Equation (1):

$$T_{on} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_s} \quad (1)$$

Where  $V_{OUT}$  is the real time output voltage reference,  $V_{IN}$  is the input voltage, and  $F_S$  is the switching frequency set by the PMBus.

### Voltage Reference

The MP2888A has an 8-bit VID-DAC, which provides the reference voltage ( $V_{REF}$ ) for the individual output.  $V_{REF}$  is in a VID format with 6.25mV per step. The relationship between  $V_{REF}$  and the VID value in decimals is shown in Equation (2):

$$V_{REF}(V) = VID \times 0.00625 \quad (2)$$

When setting the unit gain for the differential voltage sense amplifier and VID is higher than 256,  $V_{REF}$  is limited to 1.6V.

When setting the half gain for the differential voltage sense amplifier,  $V_{REF}$  can range from 0 ~ 3.19375V.

### Output Voltage Setting and Sensing

In PMBus-VID control mode, the desired output voltage can be set by the PMBus command  $VOUT\_COMMAND$  (21h).  $VOUT\_COMMAND$  (21h) is a 9-bit register in a VID format with 6.25mV per step. The output setting range is 0 ~ 3.19375V.

In PWM-VID control mode, the desired output voltage can be set according to Equation (3):

$$VID = (VID_{MAX} - VID_{MIN}) \times D_{PWMVID} + VID_{MIN} \quad (3)$$

Where  $VID_{MAX}$  is the maximum voltage setting,  $VID_{MIN}$  is the minimum voltage setting, and  $D_{PWMVID}$  is the duty of the PWM-VID signal.

The voltage at the load is sensed with the differential voltage sense amplifier. This type of sensing provides better load regulation.

The MP2888A provides high-resolution trimming and digital DC calibration for high output voltage regulation accuracy. With a unit gain of the differential voltage amplifier, the  $V_{OUT}$  regulation accuracy is within  $\pm 1.5625mV$ . With a half-gain of the differential voltage amplifier, the  $V_{OUT}$  regulation accuracy is within  $\pm 3.125mV$ .

### Active Voltage Positioning (AVP)

The MP2888A supports active voltage positioning (AVP) by connecting a droop resistor ( $R_{DROOP}$ ) between  $V_{DIFF}$  and  $V_{FB}$ . With this function, the output voltage drops gradually as the load current increases. This is also known as load-line regulation. The relationship of the output voltage and load current is shown in Equation (4):

$$V_{OUT@I_{OUT}} = V_{OUT@NO\ LOAD} - I_{OUT} \times R_{LL} \quad (4)$$

Where  $R_{LL}$  is the equivalent load line resistor.

The MP2888A provides a PMBus-programmable load-line. The final load-line value is determined by  $R_{DROOP}$  and the value in the register  $IDROOP\_SET$  (1Eh). The load-line calculation is shown in Equation (5):

$$R_{LL} = \left( \frac{IDROOP\_SET + 4}{64} \right) \times K_{CS} \times R_{DROOP} \quad (5)$$

Where  $IDROOP\_SET$  is the value in register  $MFR\_IDROOP\_CTRL$  (1Eh), and  $K_{CS}$  is the current sense gain of the power stage.

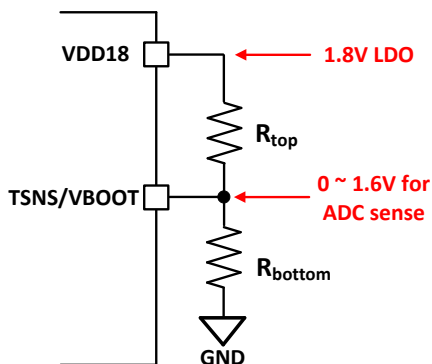
$IDROOP\_SET$  ranges from 1 ~ 15. When setting  $IDROOP\_SET = 0$ , the AVP function is disabled.

When setting a half-gain for the differential voltage sense amplifier, the  $R_{LL}$  value in Equation (5) should be doubled.

For non-AVP VR applications, it is recommended to enable the AC droop function via register  $AC\_DROOP\_EN$  (1Eh) to increase the phase margin of the loop regulation. The AC droop function can inject the AC current of the total inductor current to  $R_{DROOP}$  to introduce the current ripple signal to the loop regulation.

### Boot Voltage Setting

In PMBus-VID control mode, the MP2888A can pre-program the boot voltage ( $V_{BOOT}$ ) either by register  $VOUT\_COMMAND$  (21h) or by  $TSNS/BOOT$ . Figure 3 shows the connection for the pin-programmed  $V_{BOOT}$ .



**Figure 3: Circuit of Pin-Strap Boot Voltage**

Table 1a and Table 1b shows four options for the TSNS/BOOT pin-programmed  $V_{BOOT}$ .

**Table 1a: Pin-Strap Boot Voltage Table 1**

| TSNS/BOOT<br>Voltage Point<br>(V) | Boot Voltage (V)<br>(0.1V/step)<br>45h bit[1:0] = 00 | Boot Voltage (V)<br>(0.2V/step)<br>45h bit[1:0] = 10 |
|-----------------------------------|------------------------------------------------------|------------------------------------------------------|
| 0.05                              | 0                                                    | 0                                                    |
| 0.15                              | 0.1                                                  | 0.2                                                  |
| 0.25                              | 0.2                                                  | 0.4                                                  |
| 0.35                              | 0.3                                                  | 0.6                                                  |
| 0.45                              | 0.4                                                  | 0.8                                                  |
| 0.55                              | 0.5                                                  | 1                                                    |
| 0.65                              | 0.6                                                  | 1.2                                                  |
| 0.75                              | 0.7                                                  | 1.4                                                  |
| 0.85                              | 0.8                                                  | 1.6                                                  |
| 0.95                              | 0.9                                                  | 1.8                                                  |
| 1.05                              | 1                                                    | 2                                                    |
| 1.15                              | 1.1                                                  | 2.2                                                  |
| 1.25                              | 1.2                                                  | 2.4                                                  |
| 1.35                              | 1.3                                                  | 2.6                                                  |
| 1.45                              | 1.4                                                  | 2.8                                                  |
| 1.55                              | 1.5                                                  | 3                                                    |

The boot-up linear slew rate is set via register MFR\_BOOT\_SR (B9h) and ranges from 0.12 - 125mV/ $\mu$ s, as shown in Equation (6):

$$\text{SlewRate} = \frac{6.25\text{mV}}{\text{MFR\_BOOT\_SR} \times 0.05\mu\text{s}} \quad (6)$$

In PWM-VID control mode,  $V_{BOOT}$  can only be set by the register MFR\_VBOOT (BBh). When PWM-VID is in mid-state, the VR output slews to the boot voltage.

There are two boot-up slewing modes for PWM-VID control mode: R-C filter mode and linear mode.

**Table 1b: Pin-Strap Boot Voltage Table 2**

| TSNS/BOOT<br>Voltage Point<br>(V) | Boot Voltage (V)<br>(0.05V/step)<br>45h bit[1:0] = 01 | Boot Voltage (V)<br>(0.1V/step)<br>45h bit[1:0] = 11 |
|-----------------------------------|-------------------------------------------------------|------------------------------------------------------|
| 0.025                             | 0                                                     | 0                                                    |
| 0.075                             | 0.05                                                  | 0.1                                                  |
| 0.125                             | 0.1                                                   | 0.2                                                  |
| 0.175                             | 0.15                                                  | 0.3                                                  |
| 0.225                             | 0.2                                                   | 0.4                                                  |
| 0.275                             | 0.25                                                  | 0.5                                                  |
| 0.325                             | 0.3                                                   | 0.6                                                  |
| 0.375                             | 0.35                                                  | 0.7                                                  |
| 0.425                             | 0.4                                                   | 0.8                                                  |
| 0.475                             | 0.45                                                  | 0.9                                                  |
| 0.525                             | 0.5                                                   | 1                                                    |
| 0.575                             | 0.55                                                  | 1.1                                                  |
| 0.625                             | 0.6                                                   | 1.2                                                  |
| 0.675                             | 0.65                                                  | 1.3                                                  |
| 0.725                             | 0.7                                                   | 1.4                                                  |
| 0.775                             | 0.75                                                  | 1.5                                                  |
| 0.825                             | 0.8                                                   | 1.6                                                  |
| 0.875                             | 0.85                                                  | 1.7                                                  |
| 0.925                             | 0.9                                                   | 1.8                                                  |
| 0.975                             | 0.95                                                  | 1.9                                                  |
| 1.025                             | 1                                                     | 2                                                    |
| 1.075                             | 1.05                                                  | 2.1                                                  |
| 1.125                             | 1.1                                                   | 2.2                                                  |
| 1.175                             | 1.15                                                  | 2.3                                                  |
| 1.225                             | 1.2                                                   | 2.4                                                  |
| 1.275                             | 1.25                                                  | 2.5                                                  |
| 1.325                             | 1.3                                                   | 2.6                                                  |
| 1.375                             | 1.35                                                  | 2.7                                                  |
| 1.425                             | 1.4                                                   | 2.8                                                  |
| 1.475                             | 1.45                                                  | 2.9                                                  |
| 1.525                             | 1.5                                                   | 3                                                    |
| 1.575                             | 1.55                                                  | 3.1                                                  |

The boot-up R-C filter time constant is set with register MFR\_PARM\_RC\_CONST (B5h) and ranges from 10.40 - 655.36 $\mu$ s, as shown in Equation (7):

$$\tau_{RC} (\mu\text{s}) = \frac{0.32\mu\text{s}}{\text{BOOT\_RC}} \times 2^{11} \quad (7)$$

Where BOOT\_RC is the value in register MFR\_PARM\_RC\_CONST (B5h).

The boot-up linear slew rate is set with register MFR\_BOOT\_SR (B9h) and ranges from 0.12 - 125mV/μs (see Equation (6)).

### Dynamic Voltage Identification (DVID)

The MP2888A supports dynamical output voltage transition by changing VID via the PMBus commands or the duty of the PWM-VID signal.

The DVID process is active after V<sub>OUT</sub> is settled and can be either upward or downward.

In PMBus-VID control mode, the DVID linear slew rate is set with register MFR\_DVID\_SR (BAh) and ranges from 0.12 - 125mV/μs, as shown in Equation (8):

$$\text{SlewRate} = \frac{6.25\text{mV}}{\text{MFR\_DVID\_SR} \times 0.05\mu\text{s}} \quad (8)$$

There are two slew rate modes, R-C filter mode and linear mode, in PWM-VID control mode.

The DVID R-C filter slew rate is set with register MFR\_PARM\_RC\_CONST (B5h) and ranges from 10.40 - 655.36μs, as shown in Equation (9):

$$\tau_{RC} (\mu\text{s}) = \frac{0.32\mu\text{s}}{\text{DVID\_RC}} \times 2^{11} \quad (9)$$

Where DVID\_RC is the value in register MFR\_PARM\_RC\_CONST (B5h).

The DVID linear slew rate is set with register MFR\_DVID\_SR (BAh) and ranges from 0.12 - 125mV/μs (see Equation (8)).

### VID Offset

The MP2888A supports two types of VID offset.

The first type is VID step offset, which ranges from -0.69375V to 0.7V with 6.25mV of resolution. When the PMBus writes a new offset to register VOUT\_OFFSET (23h), the VR ramps with the slew rate shown in Equation (8).

The second type is fine-tune offset for the VID set point, which ranges from -31.5mV to 31.5mV with 0.5mV of resolution at a unity gain of the differential voltage sense amplifier and ranges from -50.4mV to 50.4mV with 0.8mV of resolution at a half-gain of differential voltage sense amplifier. Refer to the register map MFR\_RSAMP\_OFFSET (2Dh) section on page 47 for details.

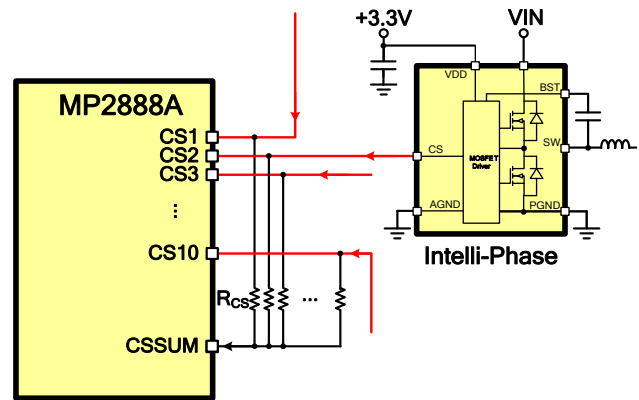
### Inductor Current Sensing

The MP2888A works with Intelli-Phase for inductor current sensing (see Figure 4). The voltage on CSs is sampled, calculated, and stored in the registers. The results are used for multi-phase current balancing and thermal balancing and can be monitored via the PMBus.

The MP2888A provides cycle-by-cycle per-phase current limitation.

The resistor (R<sub>CS</sub>) is connected from CSx to CSSUM. CSSUM is a 1.23V constant voltage and can sink or source current to provide voltage shifts that meet the operating voltage range of CSs.

Short any unused CSx pin to AGND or CSSUM.



**Figure 4: Phase Current Sense**

Different types of Intelli-Phase products have different operating voltage ranges for CS (V<sub>CS\_MIN</sub> and V<sub>CS\_MAX</sub>). Refer to each Intelli-Phase's datasheet to determine the minimum and maximum operating voltage ranges. Calculate a proper R<sub>CS</sub> value with Equation (10):

$$V_{CS\_MIN} < I_{LOAD} \times K_{CS} \times R_{CS} + 1.23\text{V} < V_{CS\_MAX} \quad (10)$$

By working with the Intelli-Phase, the MP2888A does not need temperature compensation and impedance matching compared with traditional DCR sensing to achieve an accurate current sense.

### Total Current Sensing

The total current is summed from CSSUM, and a 1/16 proportional current emerges to IMON. Connect a resistor from IMON to AGND to generate a voltage proportional to the output current. The IMON voltage is sampled,

calculated, and stored in the registers. This result is used for total OCP, auto-phase shedding, and output power calculation, and can be monitored via the PMBus.

If the auto-phase-shedding function is enabled, the total current report is used to determine the real-time phase number.

The MP2888A provides a user-programmable scaling factor and a user-programmable current offset. The programmable parameters allow users to match the IMON scaling to the design's voltage regulator tolerance band (VRTOB) calculation. This provides the most accurate current reporting across the entire load range and maximizes the performance of the processor turbo. The scaling factor can also be reduced or offset to under-report the total current to the system for higher performance. Figure 5 shows the MP2888A IMON sense and report block diagram.

In Figure 5, the MFR\_IMON\_DIGI\_GAIN register (2Fh) is used to fine-tune the ADC sense value with 0.1% resolution. The IOUT\_CAL\_GAIN register (38h) converts the sensed and trimmed IMON voltage to an ampere format with 0.25A/LSB. The detailed calculation of the register value is provided in the MP2888A application note and register map.

The voltage at IMON can be calculated with Equation (11):

$$V_{IMON} = \left( \frac{K_{CS} \times I_{OUT}}{16} \right) \times R_{IMON} \quad (11)$$

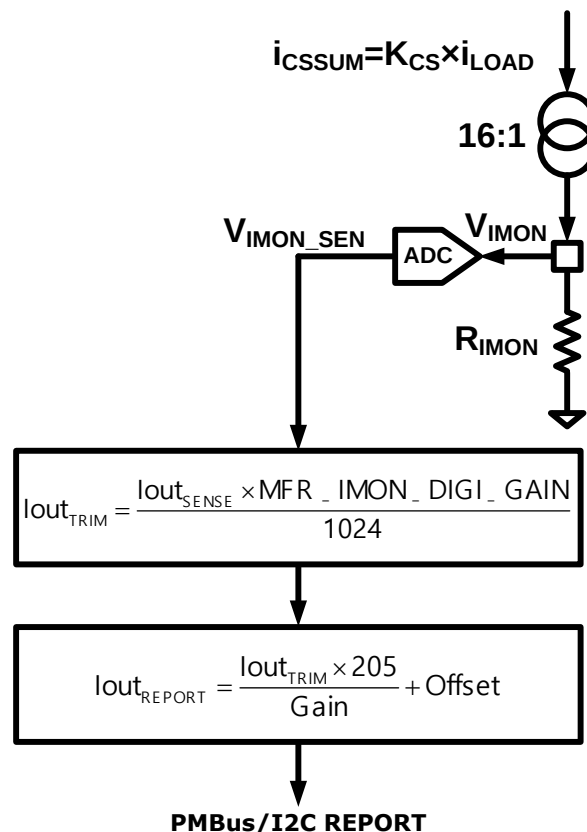
Where  $I_{OUT}$  is the load current,  $K_{CS}$  is the current sense gain of the Intelli-Phase, and  $R_{IMON}$  is the value of the resistor connected from IMON to ground.

## Power Mode

To improve efficiency over the entire load range, the MP2888A supports automatic phase shedding and adjustable high/low phase count with PSI (see Table 2).

**Table 2: Phase Mode Definition**

| PSI Pin | Mode             |
|---------|------------------|
| High    | High-phase count |
| Hi-Z    | Auto-power mode  |
| Low     | Low-phase count  |



**Figure 5: Current Sense and Report**

In high-phase count mode, the VR is forced to operate with a full phase count configured in register MFR\_VR\_CONFIG (E1h).

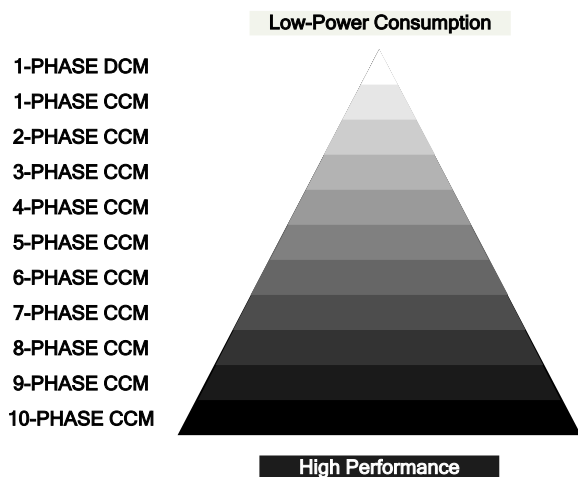
In low-phase count mode, the VR is forced to operate with a low phase count configured in register MFR\_LOW\_PHASE\_CNT (AAh).

In auto-power mode, the VR can be optimized to adjust the phase count according to the real-time sensed load current.

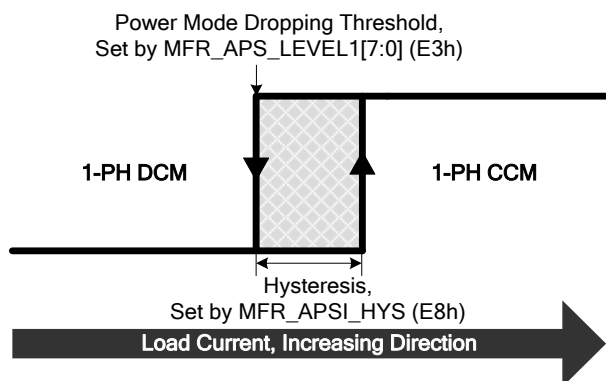
As shown in Figure 6, using 10-phase as an example, the VR works at 10-phase continuous conduction mode (CCM) at heavy loads, and 1-phase CCM at light loads to optimize efficiency. The VR enters 1-phase discontinuous conduction mode (DCM) at extremely light loads reduce the switching loss further.

The APM function is implanted by comparing the sensed load current with each power state current threshold. The MFR\_APS\_LEVEL (E3h~E7h) registers set the power state dropping thresholds. The hysteresis is set with register MFR\_APS\_HYS (E8h) to prevent the

converter from changing the power state back-and-forth at a steady load current. Figure 7 shows the APM current thresholds setting from 1-phase CCM to 1-phase DCM.



**Figure 6: APM Function Diagram at 10-Phase Mode**



**Figure 7: APM Threshold Setting between 1-Phase DCM and 1-Phase CCM**

Table 3 lists the phase shedding and adding entry conditions based on the current report for 10-phase applications.

**Table 3: Phase Shedding/Adding Based on Current Report for 10-Phase Applications**

| Condition                                                     | Phase Number |
|---------------------------------------------------------------|--------------|
| $I_{LOAD} > MFR\_9PH\_LOW + MFR\_APS\_HYS$                    | 10-Ph CCM    |
| $MFR\_8PH\_LOW + MFR\_APS\_HYS < I_{LOAD} \leq MFR\_9PH\_LOW$ | 9-Ph CCM     |
| $MFR\_7PH\_LOW + MFR\_APS\_HYS < I_{LOAD} \leq MFR\_8PH\_LOW$ | 8-Ph CCM     |
| $MFR\_6PH\_LOW + MFR\_APS\_HYS < I_{LOAD} \leq MFR\_7PH\_LOW$ | 7-Ph CCM     |
| $MFR\_5PH\_LOW + MFR\_APS\_HYS < I_{LOAD} \leq MFR\_6PH\_LOW$ | 6-Ph CCM     |
| $MFR\_4PH\_LOW + MFR\_APS\_HYS < I_{LOAD} \leq MFR\_5PH\_LOW$ | 5-Ph CCM     |
| $MFR\_3PH\_LOW + MFR\_APS\_HYS < I_{LOAD} \leq MFR\_4PH\_LOW$ | 4-Ph CCM     |
| $MFR\_2PH\_LOW + MFR\_APS\_HYS < I_{LOAD} \leq MFR\_3PH\_LOW$ | 3-Ph CCM     |
| $MFR\_1PH\_LOW + MFR\_APS\_HYS < I_{LOAD} \leq MFR\_2PH\_LOW$ | 2-Ph CCM     |
| $MFR\_DCM\_LOW + MFR\_APS\_HYS < I_{LOAD} \leq MFR\_1PH\_LOW$ | 1-Ph CCM     |
| $I_{LOAD} \leq MFR\_DCM\_LOW$                                 | 1-Ph DCM     |

In addition to the sensed output current comparison, the MP2888A provides three conditions (listed below) to exit APM immediately and run in full-phase CCM to accelerate the load transient response and reduce the output voltage undershoot.

1. DVID makes the controller runs in full-phase CCM. After the output voltage is settled to the target value, the VR resumes APM.
2. Load step-up causing a VFB window trip triggers full-phase CCM to reduce the output voltage undershoot.
3. Load step-up causing the frequency to change exceeds a programmable threshold and triggers full-phase CCM.

## Current Balance and Thermal Balance

The MP2888A provides a current balance loop to achieve fair current sharing at multi-phase mode, since different circuit impedances lead to difference phase currents.

The phase current is sensed and calculated with the current reference in the current loop. Each phase's PWM on time is adjusted individually to balance the currents accordingly.

The MP2888A applies  $\Sigma$ - $\Delta$  modulation and delay line-loop technology in the current-balance modulation to increase the resolution of the function and reduce PWM jitter greatly. The time resolution of the digital system is 5ns. By applying  $\Sigma$ - $\Delta$  modulation technology, the digital PWM resolution can be increased to 0.08ns.

Each current balance loop can also include a programmable phase current offset to achieve thermal balance among the phases. For example, a phase can have a greater cooling capability due to proximity to the airflow, which allows it to take more phase current by increasing the phase current reference with the offset to keep the phase thermal more balanced. The bandwidth of the current proportional-integral (PI) loop is relatively lower than the output voltage feedback loop, so it barely impacts the output voltage.

## Input Voltage Sensing

The input power supply voltage is sampled at VINSEN with a resistor divider (see Figure 8). The sensed input voltage is used for PWM on-time calculation, VIN\_UVLO, VIN\_OVP fault protection, VIN\_UV warning and input voltage monitoring.

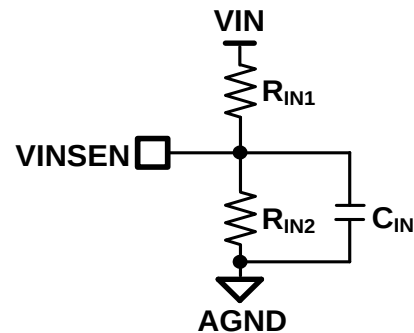
In designs, the divided voltage on VINSEN should not exceed the ADC sampling range (1.6V) at the maximum input voltage. A 1 - 10nF ceramic capacitor from VINSEN to AGND is recommended as an input sense filtering capacitor (C<sub>IN</sub>) (see Figure 8).

Program the input voltage sensing divider ratio with register MFR\_VIN\_SCALE\_LOOP (C0h). The calculation of the ratio (K<sub>IN</sub>) is shown in Equation (12):

$$K_{IN} = \frac{R_{IN2}}{R_{IN1} + R_{IN2}} = \frac{VIN\_SCALE\_LOOP}{2^{10}} \quad (12)$$

Where VIN\_SCALE\_LOOP is the decimal value in the register MFR\_VIN\_SCALE\_LOOP (C0h).

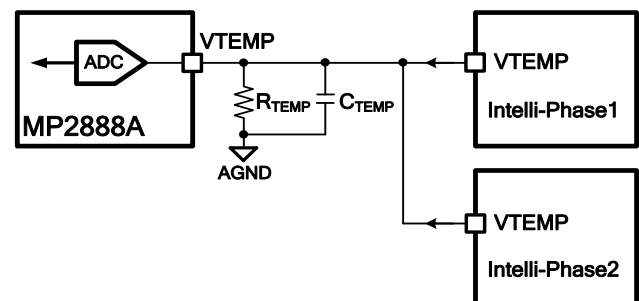
In designs, match the resistor setting (K<sub>IN</sub>) and register setting value for accurate input voltage sensing.



**Figure 8: Input Voltage Sense Connection**

## Temperature Sense of Intelli-Phase

The MP2888A senses the Intelli-Phase's temperature by connecting the Intelli-Phase's VTEMP pin to the MP2888A's VTEMP pin (see Figure 9). The sensed temperature is used for over-temperature fault protection, over-temperature warning (assert TALER#), and power stage temperature monitoring.



**Figure 9: Temperature Sense for MP2888A with Intelli-Phase**

C<sub>TEMP</sub> is a VTEMP pin filtering capacitor (recommend to be a 10nF ceramic capacitor). R<sub>TEMP</sub> is a discharging resistor when the junction temperature is falling (ranging from 10 - 49.9k $\Omega$ ).

The VTEMP pin of the Intelli-Phase reports a voltage proportional to the junction temperature.

Set the calculation gain and offset in register MFR\_TEMP\_GAIN\_OFFSET (C1h).

An example of the Intelli-Phase VTEMP voltage is shown in Equation (13):

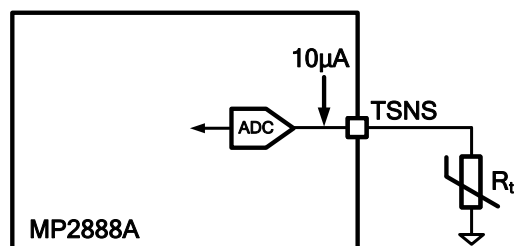
$$T_{\text{JUNCTION}}(^{\circ}\text{C}) = 100 \times V_{\text{TEMP}}(\text{V}) + 10 \quad (13)$$

for  $T_{\text{JUNCTION}} > 10^{\circ}\text{C}$

If VTEMP is 700mV, then the junction temperature of the Intelli-Phase is 80°C. Since VTEMP cannot go below 0V, it reads 0V when the junction temperature is lower than 10°C. Refer to the datasheet of the Intelli-Phase for more information.

### Temperature Sense of the Thermistor

The MP2888A senses the external thermal component's temperature by connecting a thermistor to TSNS (see Figure 10). The sensed temperature is used for over-temperature fault protection and over-temperature warning (assert TALERT#).



**Figure 10: Temperature Sense for MP2888A with Thermistor**

TSNS sources a 10µA current source to the thermistor, and the MP2888A senses the voltage of TSNS. The 10µA current source can be disabled via register TSNS\_CURRENT\_DIS (34h bit[10]), and a voltage signal can be connected to TSNS as a new defined protection function.

Note that if the 10µA current source is enabled, TSNS cannot be floated.

### EEPROM Operation

The MP2888A provides an EEPROM to store custom configurations. A 4-digit part number suffix is assigned for each application. The default configuration for each 4-digit part can be pre-programmed at the MPS factory. The data can be programmed again using the STORE\_USER\_ALL (15h) command via the PMBus and requires 200ms of time for the data

to be stored to the EEPROM. The EEPROM is read automatically during the power-on sequence or by the RESTORE\_USER\_ALL (16h) command via the PMBus and requires at least 300µs of time for data to be restored from the EEPROM.

The operation to the EEPROM can be accomplished easily with the MPS GUI software.

The MP2888A uses register DBh to enable EEPROM write protection.

The EEPROM can be erased or written for more than 100,000 cycles. When the EEPROM is write-protected, the write into EEPROM action is ineffective.

### EEPROM Fault

If the data from the EEPROM is checked as invalid by the cyclic redundancy code (CRC) during the system initialization process, the system enters an EEPROM fault state without outputting power and waits for the error clear command. The configuration from the EEPROM is ignored.

There are three ways to clear the EEPROM fault and start up again with the restored value from the EEPROM:

1. Clear the EEPROM fault via the PMBus command (FFh).
2. Clear the fault status via the PMBus command (03h).
3. Store the configuration into the EEPROM and restart.

### Low-Power Mode

The MP2888A can be programmed to operate in regular-power mode or low-power mode.

In regular-power mode, the PMBus communication is available when EN is low. With low-power mode enabled, when EN is low, the PMBus communication is disabled, and the quiescent current ( $I_Q$ ) can be reduced to 150µA.

Low-power mode is factory-programmable.

### Power On

The MP2888A is supplied by a +3.3V voltage at VDD33. VDD33 provides the bias supply for the analog circuit and internal 1.8V LDO. The 1.8V LDO produces the +1.8V supply for the digital

circuit. The system is reset by the internal power-on reset signal (POR) after the VDD33 supply is ready. If the MP2888A is in regular-power mode, EN must be high. After the system exits POR, the data in the EEPROM is loaded into the operating registers to configure the VR operation.

Figure 11a shows the power on sequence of the MP2888A in regular power mode.

t0~t1: at t0, VDD33 is supplied by a +3.3V voltage and reaches the VDD33 UVLO\_ON threshold at t1. VDD18 reaches +1.8V when VDD33 is higher than 1.8V.

t1~t2: at t1, the data in the EEPROM starts loading into the operating registers. The entire EEPROM copy process takes about 300μs, typically. During this stage, the PMBus address is detected if the voltage on ADDR is selected to set the PMBus address.

t2~t3: at t2, after the EEPROM copy is finished, the MP2888A waits for EN to pull high. The PMBus is available at this stage.

t3~t4: when EN is high, if the PMBus command OPERATION (01h) is pre-set to an off state. The MP2888A halts at this stage and waits for the OPERATION on command. If OPERATION (01h) is pre-programmed to an on state, the turn-on delay time (T<sub>ON</sub> delay) begins counting.

The T<sub>ON</sub> delay is PMBus-programmable from 0 to 3276.75ms with the command TON\_DELAY (60h).

t4~t5: when the T<sub>ON</sub> delay time expires, the VID-DAC starts ramping up V<sub>REF</sub> and a programmed slew rate to the boot-up voltage. During soft start, OCP\_Total, OVP, and UVP are masked until V<sub>REF</sub> reaches the target value.

In PWM-VID mode, before t5, PWM-VID should remain at a Hi-Z state.

Figure 11b shows the power-on sequence of the MP2888A in low-power mode.

t0~t1: at t0, VDD33 is supplied by a +3.3V voltage and reaches the VDD33 UVLO\_ON threshold at t1. VDD18 reaches +1.8V when VDD33 is greater than 1.8V.

t1~t2: after t1, VDD33 rises above the UVLO\_ON threshold, and the MP2888A waits for EN to pull high. The PMBus is unavailable at this stage.

t2~t3: at t2, EN pulls high, the data in the EEPROM starts loading into the operating registers. The entire EEPROM copy process takes about 300μs, typically. During this stage, the PMBus address is detected if the voltage on ADDR is selected to set the PMBus address.

t3~t4: after the EEPROM copy is finished, if the PMBus command OPERATION (01h) is pre-set to an off state. The MP2888A halts at this stage and waits for an OPERATION ON command. If OPERATION (01h) is pre-programmed to an on state, the turn-on delay time (T<sub>ON</sub> delay) begins counting. The T<sub>ON</sub> delay is PMBus-programmable from 0 to 3276.75ms with the command TON\_DELAY (60h).

t4~t5: when the T<sub>ON</sub> delay time expires, the VID-DAC starts ramping up V<sub>REF</sub> with a programmed slew rate to the boot-up voltage. During soft start, OCP\_Total, OVP, and UVP are masked until V<sub>REF</sub> reaches the target value.

In PWM-VID mode, before t5, PWM-VID should remain at Hi-Z.

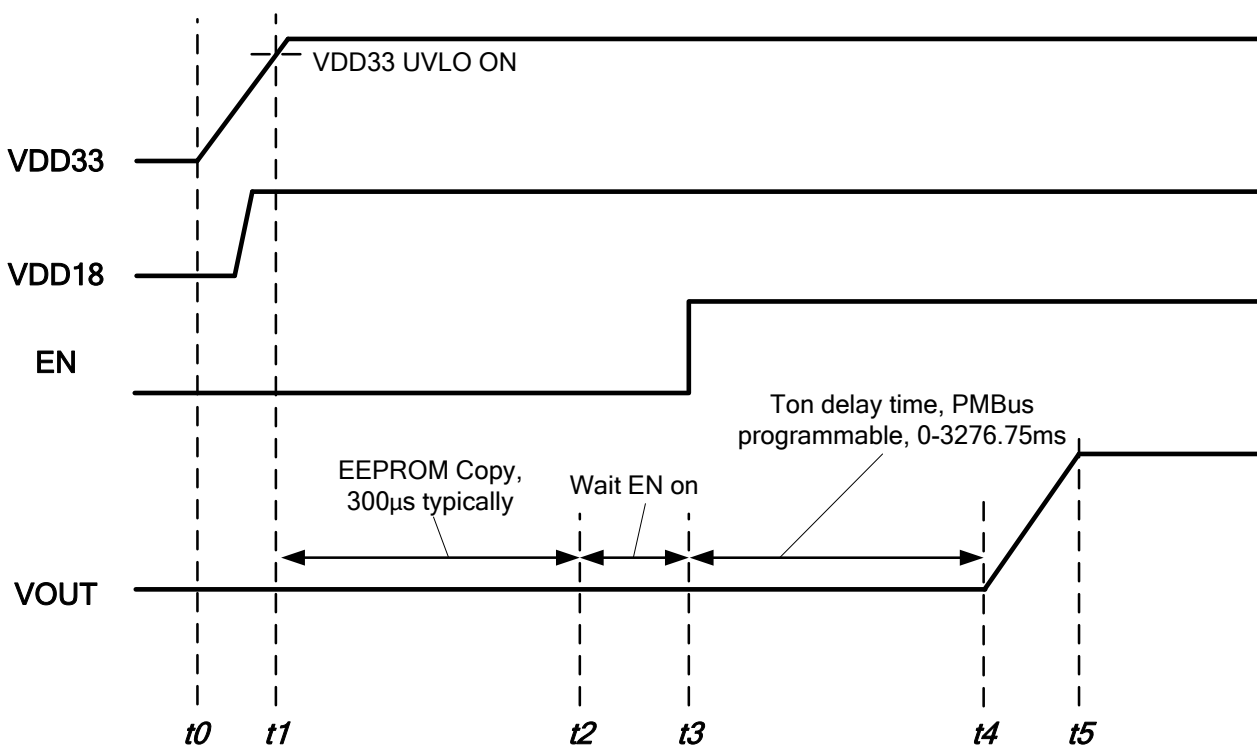


Figure 11a: MP2888A Power-On Sequence at Regular-Power Mode

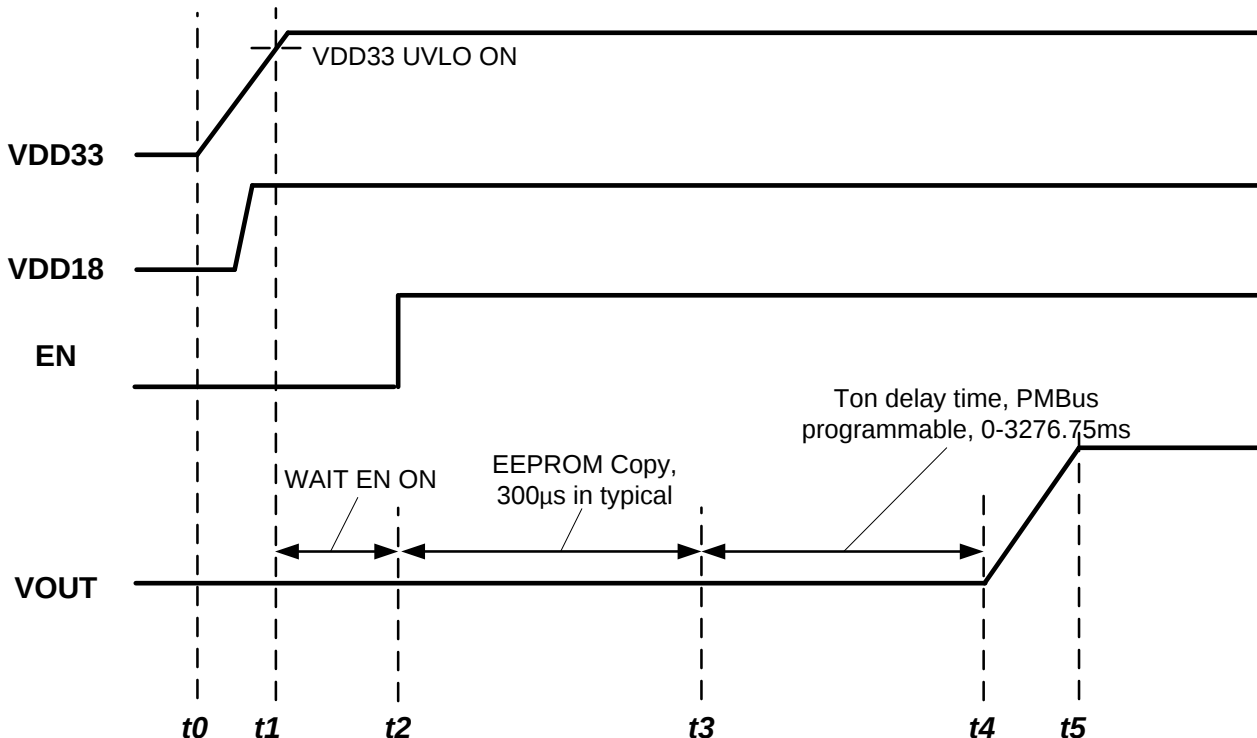


Figure 11b: MP2888A Power-On Sequence at Low-Power Mode

### Power Off

The MP2888A can be powered off by the OPERATION command, EN, or VDD33.

1. **OPERATION command off:** The MP2888A provides Hi-Z off and soft-off with commands. During soft-off,  $V_{OUT}$  drops down with a pre-programmed slew rate in

register MFR\_BOOT\_SR (B9h) until  $V_{REF}$  reaches the level of register MFR\_VID\_SD (BCh) and then enters Hi-Z off. This prevents  $V_{OUT}$  from becoming negative during the shutdown process. A turn-off delay can be set via register TOFF\_DELAY (64h).

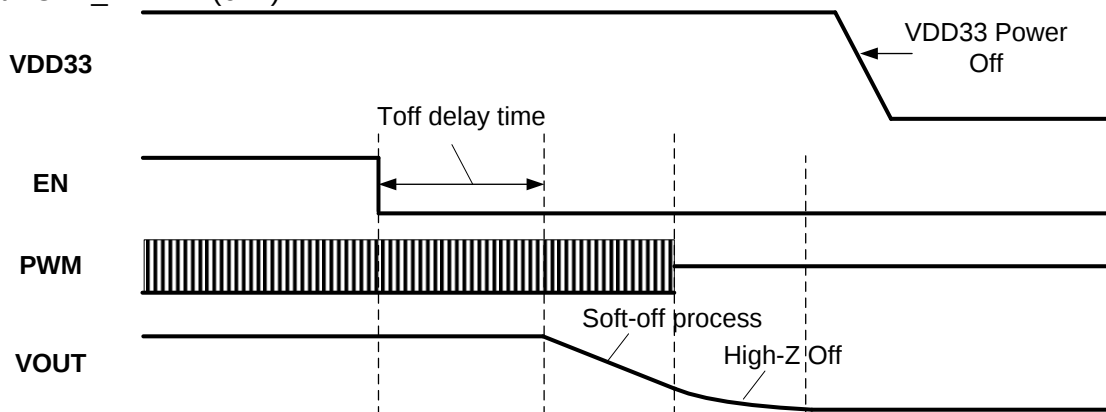
2. **EN off:** The MP2888A provides Hi-Z off and soft-off when EN is pulled low in regular-power mode. During soft-off,  $V_{OUT}$  drops down with a pre-programmed slew rate in register MFR\_BOOT\_SR (B9h) until  $V_{REF}$  reaches the level of register MFR\_VID\_SD (BCh) and then enters Hi-Z off. This prevents  $V_{OUT}$  from becoming negative during the shutdown process. A turn-off delay can be set via TOFF\_DELAY (64h).

In low-power mode when EN is pulled low, the MP2888A can enter Hi-Z off without any turn-off delay immediately, and enters standby mode with the smallest amount of power consumption.

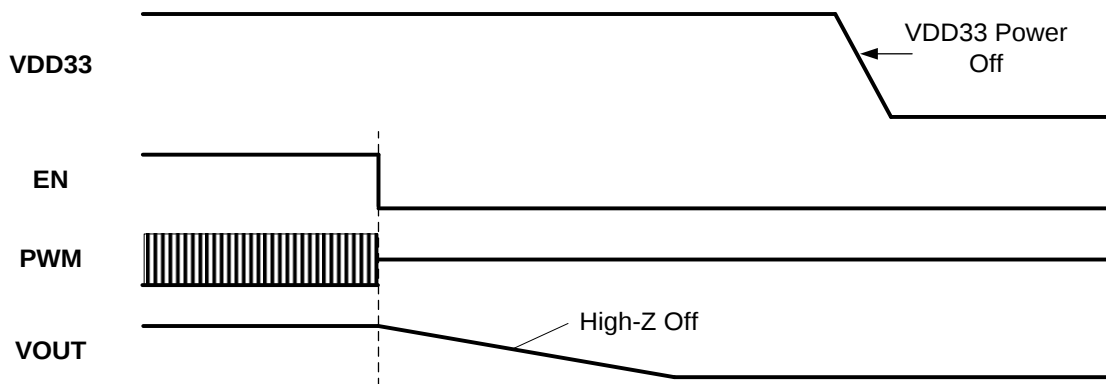
3. **VDD33 power-off:** When the voltage on VDD33 falls below the UVLO threshold, the MP2888A powers off immediately. All PWMs enter Hi-Z.

Figure 12a shows the EN soft-off power sequence in regular-power mode.

Figure 12b shows the EN Hi-Z off power sequence in low-power mode.



**Figure 12a: MP2888A Power-Off Sequence in Regular-Power Mode**



**Figure 12b: MP2888A Power-Off Sequence in Low-Power Mode**

### Power Good Indication (PGOOD)

The MP2888A power good (PGOOD) on/off thresholds are programmable via POWER\_GOOD\_ON (5Eh) and POWER\_GOOD\_OFF (5Fh).

During the soft-start process, when  $V_{REF}$  rises above the POWER\_GOOD\_ON threshold, the MP2888A starts a delay counter before asserting PGOOD. The delay counter time is programmable via register MFR\_DELAY\_SET (5Dh).

During the soft-shutdown process, when  $V_{REF}$  falls below the `POWER_GOOD_OFF` threshold, the MP2888A de-asserts `PGOOD` immediately. The `POWER_GOOD_OFF` threshold must be set below the VID value, which is regulated during the normal operation process.

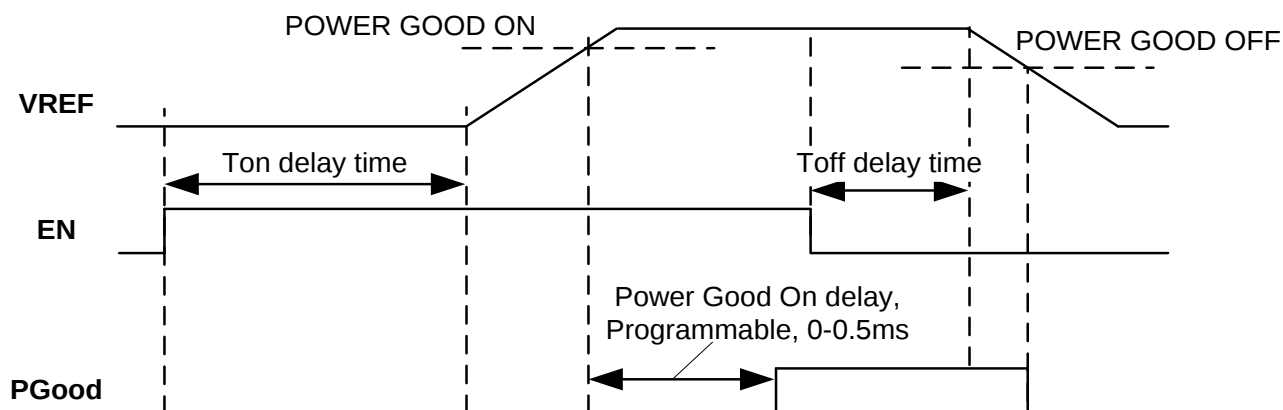
For Hi-Z shutdown caused by protections or `EN` turning off, `PGOOD` is de-asserted immediately. Figure 13 shows the power good indication in regular-power mode.

### V<sub>FB</sub> Window

The MP2888A has a feedback voltage ( $V_{FB}$ ) window ( $V_{REF} \pm 25mV$ ), which provides an advanced non-linear loop control to fasten the transient performance.

When  $V_{FB}$  is higher than  $V_{REF} + 25mV$  ( $V_{FB}$  positive window limit), all PWMs pull low and blank the PWM set signal until  $V_{FB}$  falls below the positive limit. The  $V_{FB}$  positive window is used to reduce the output voltage overshoot at the load release, typically, especially in multi-phase operation.

When  $V_{FB}$  is lower than  $V_{REF} - 25mV$  ( $V_{FB}$  negative window limit), VR exits auto-power mode immediately and enters full-phase running to improve transient response.



**Figure 13: MP2888A Power Good On/Off Sequence in Regular-Power Mode**

### Fault and Protections

The MP2888A supports the following fault monitoring and protections.

#### V<sub>IN</sub> UVLO and OVP

VR can shut down immediately by forcing the PWM signals into tri-state if the sensed input voltage is below the `VIN_OFF` threshold. The VR restarts when the sensed input voltage is above the `VIN_ON` threshold. The  $V_{IN}$  UVLO threshold is programmable with register `VIN_ON` (35h) and `VIN_OFF` (36h) with 0.125V/LSB.

VR latches if the input voltage is above the  $V_{IN}$  OVP threshold, which is set with register `VIN_OV_FAULT_LIMIT` (55h).

### Over-Current Protection (OCP)

OCP applies a dual OCP mechanism with two types of thresholds.

The first OCP type, `OCP_Total`, is a time- and current-based threshold. The PMBus sets the `OCP_Total` threshold using `MFR_OCP_TOTAL` (ECh). `OCP_Total` should trigger when the sensed average output current exceeds the threshold for a period of time referred to as the OCP blanking time. `OCP_Total` can be programmed to No Action, Hiccup, Retry Six Times, and Latch-Off mode via the PMBus.

The controller takes no action at No Action mode and keeps the PWMs switching. The fault indication bit in register `STATUS_IOUT` (7Bh) and `STATUS_WORD` (79h) is not set in No Action mode.

In Hiccup mode, the controller forces the PWM signals into tri-state to disable the output. The controller attempts to restart after 12.5ms of protection delay time.

In Retry Six Times mode, the VR hiccups six times at most. If the fault is removed within the six restarts, the VR resumes normal operation. If the fault remains after the six restarts, the VR shuts down until a new power cycle, an EN toggle, or a PMBus COMMAND ON occurs.

In Latch mode, the VR shuts down until a new power cycle, an EN toggle, or a PMBus COMMAND ON occurs.

These four protection types are also available for  $V_{OUT}$  UVP and  $V_{OUT}$  OVP2.

The second OCP type, OCP\_Phase, is a current-based limitation threshold. The MP2888A monitors the phase current cycle-by-cycle. When the phase current exceeds the OCP\_Phase threshold at the PWM off time, the PWM remains low to discharge the inductor current. If the load current continues rising, the output voltage drops because the inductor current is limited. OCP\_Phase is implemented with  $V_{OUT}$  UVP, generally. The OCP\_Phase threshold is PMBus-programmable with register MFR\_OCP\_PHASE (EDh).

### **Under-Voltage Protection (UVP)**

The MP2888A monitors the VDIFF voltage to provide UVP and uses a dual UVP approach.

The first UVP type, UVP1, is a digital UVP. UVP1 is triggered when the internal ADC senses that the VDIFF voltage is lower than the threshold for a pre-set blanking time. The UVP1 threshold can be set from 0 - 480mV with 32mV of resolution. Refer to the register MFR\_SYS\_CONFIG (44h) section on page 56.

The second UVP type, UVP2, is triggered when the VDIFF voltage is lower than the threshold for a pre-set blanking time. The register OVUV\_LEVEL (2Ch) can program the UVP2 threshold to  $V_{REF} - 430\text{mV}$ ,  $V_{REF} - 310\text{mV}$  or  $V_{REF} - 190\text{mV}$ . Refer to the MFR\_OVUV\_SEL (2Ch) section on page 46. When programming the gain of the differential voltage sense amplifier as half, the UVP2 threshold is doubled. For example, set the register to a -430mV level to achieve the  $V_{REF} - 860\text{mV}$  threshold.

The UVP scheme is the same as the OCP\_Total protection scheme. When the VDIFF voltage is lower than the UVP threshold for a given amount of time (UVP blanking time), the controller forces the PWM signals into tri-state to disable the output. The register MFR\_OVP\_UVP\_SET (EEh) sets the UVP mode and blanking time. Like the OCP\_Total protection scheme, the UVP scheme also provides no action, hiccup, retry six times, and latch-off options.

### **Over-Voltage Protection (OVP)**

The MP2888A monitors the VDIFF voltage to provide OVP and uses a dual OVP approach (described below). When OVP is triggered, the MP2888A pulls all activated PWMs low to turn on the low-side MOSFET to discharge the output capacitors until  $V_{OUT}$  reaches +300mV. Then all PWMs are set to Hi-Z.

The first OVP type, OVP1, is triggered when the VDIFF voltage is higher than the OVP1 threshold without any delay time. The OVP1 fault is in Latch-Off mode.

The OVP1 threshold is  $V_{OUT\_MAX}$  (24h) +400mV, regardless of the gain of the differential voltage sense amplifier.

The second OVP type, OVP2, is triggered when the VDIFF voltage above the OVP2 threshold for a pre-set blanking time. Just like in UVP, the MP2888A provides no Action, hiccup, retry six times, and latch-off modes for the OVP2 fault.

The register MFR\_OVUV\_LEVEL (2Ch) can program the OVP2 level to  $V_{REF} + 430\text{mV}$ ,  $V_{REF} + 310\text{mV}$ , and  $V_{REF} + 190\text{mV}$ . Refer to the MFR\_OVUV\_SEL (2Ch) section on page 46. When programming the gain of the differential voltage sense amplifier as half, the OVP2 threshold is doubled. For example, set the register to a +190mV level to achieve the  $V_{REF} + 380\text{mV}$  threshold.

### **Over-Temperature Protection (OTP)**

The MP2888A uses a dual OTP approach.

The first OTP type is VTEMP protection from the Intelli-Phase (see Figure 9). If the VTEMP report value is higher than the threshold in the register OT\_WARN\_LIMIT (51h), TAlert# is asserted.

If the VTEMP report value is higher than the threshold in the register VTEMP\_OTP\_THRE (EAh), the VR Hi-Z shuts down.

The VTEMP fault can be programmed to either Latch-Off mode or Hiccup mode via register VTEMP\_OTP\_MODE (EAh).

The second OTP type is TSNS protection from the thermistor (see Figure 10). If the TSNS report value is higher than the threshold in register TSNS\_T\_ALT\_THRE (34h), TAlert# is asserted. If the TSNS report value is higher than the threshold in register TSNS\_OTP\_THRE (E9h), the VR Hi-Z shuts down.

The TSNS fault can be programmed to No Action, Latch-Off, or Hiccup mode via register TSNS\_OTP\_MODE (E9h).

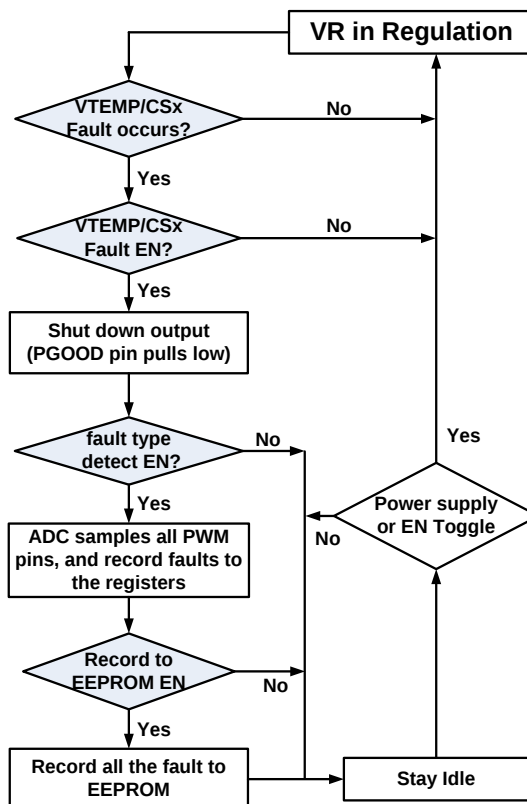
### Intelli-Phase Fault Detection

When VTEMP is pulled up to 3.3V, or any CS pin is pulled down to 0V, the MP2888A latches off immediately. These protections are called VTEMP fault protection and CS fault protection.

When VTEMP or CS fault protection occurs, the MP2888A can detect the fault type of the Intelli-Phase. There are four typical fault types:

- Over-current fault
- Over-temperature fault
- Low-side MOSFET fault
- High-side MOSFET fault

The fault type detection only works when the Intelli-Phase supports fault type indication via PWMx. Refer to the datasheet of the Intelli-Phase for specific details. Figure 14 shows the flow chart of Intelli-Phase fault detection.



**Figure 14: Flow Chart of Intelli-Phase Fault Detection**

The related registers are described below.

1. The enable bit of the VTEMP and CS fault function is bit[9:8] of MFR\_PROTECT\_DIS (3Ah).
2. The enable bit of the ADC sampling the fault type from the Intelli-Phase PWM is bit[10] of MFR\_PROTECT\_DIS (3Ah).
3. The enable bit to record a fault to the EEPROM is bit[1] of MFR\_EEPROM\_CTRL (06h).

### Protection Type Storage in the EEPROM

Once any protection occurs, the fault type is recorded to Page 0's registers F8h ~ FBh. If the EEPROM fault record is enabled, the last fault event is recorded in Page 29's registers FBh ~ FEh. EN must remain high for at least 20ms after the fault occurs to save the fault type into the EEPROM.

To clear the fault record in the EEPROM registers, 0x0000 must be written to these registers (Page 29 FBh ~ FEh). This is a direct access to the EEPROM registers. The time required for each write command is 5ms.

## Phase Number Configuration

The MP2888A can be configured to different phase numbers via the PMBus register or by CSx (see Table 4).

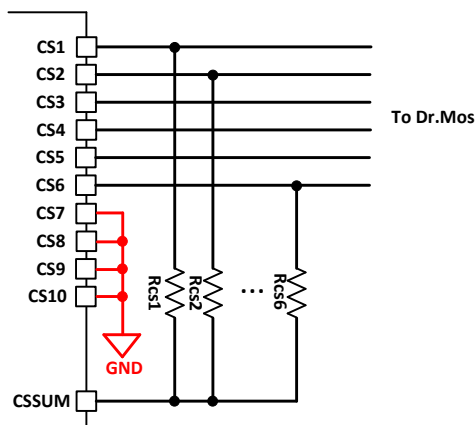
**Table 4: Phase Number Configuration and Activated PWM Pins**

| PHASE_CNT (E1h) | Activated PWM Pins |
|-----------------|--------------------|
| 1               | PWM1               |
| 2               | PWM1~2             |
| 3               | PWM1~3             |
| 4               | PWM1~4             |
| 5               | PWM1~5             |
| 6               | PWM1~6             |
| 7               | PWM1~7             |
| 8               | PWM1~8             |
| 9               | PWM1~9             |
| 10~15           | PWM1~10            |

If PHASE\_CNT is set to 0, the MP2888A operates in 1-phase DCM.

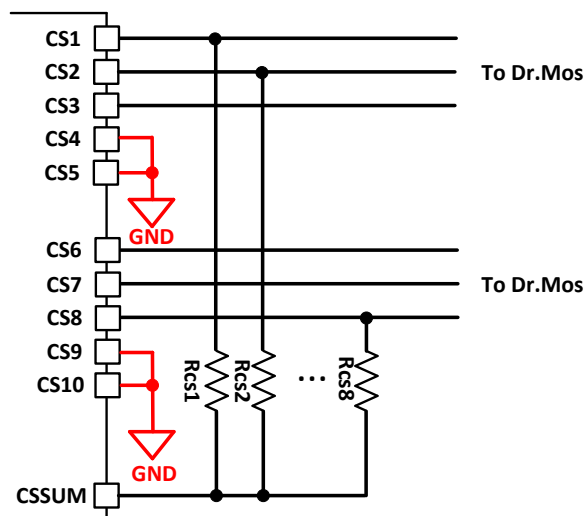
Any unused PWM pin enters tri-state, and the activated phases interleave automatically. Float the unused PWM pins. For example, when the MP2888A is set to 8-phase, PWM9 and PWM10 should be floating. For the Intelli-Phase, if the PWM input is in Hi-Z, the SW node is in Hi-Z as well.

If the CS pins are enabled to program the phase number, the register setting in E1h is ignored. Pull down the unused CS pins to ground. After EN is pulled high, the MP2888A checks the voltage on the CS pins sequentially from CS1 to CS10 until it finds the first low voltage. Figure 15 shows an example of the connection for 6-phase applications. The first low voltage is on CS7.



**Figure 15: CS Pins Program to 6-Phase**

Figure 16 shows the connection for 6-phase applications in couple-inductor mode.



**Figure 16: CS Pins Configure for 6 Phase in Couple-Inductor Mode**

## Couple-Inductor Mode

The MP2888A supports couple-inductor mode to reduce the overshoot during load releasing.

Table 5 shows the relation of coupled phases.

**Table 5: Coupled Phases Group Requirement**

| Couple Group      | Phase Number       |
|-------------------|--------------------|
| Phase 1, Phase 6  | $\geq 2\text{-Ph}$ |
| Phase 2, Phase 7  | $\geq 4\text{-Ph}$ |
| Phase 3, Phase 8  | $\geq 6\text{-Ph}$ |
| Phase 4, Phase 9  | $\geq 8\text{-Ph}$ |
| Phase 5, Phase 10 | $10\text{-Ph}$     |

Figure 17 shows a connection example of 10-phase couple-inductor application. If set to 8-phase, phase 5 and phase 10 are disabled simultaneously.

The MP2888A supports the auto-phase-shedding function for couple-inductor mode to flatten the overall VR efficiency. Each pair of coupled phases shed together.

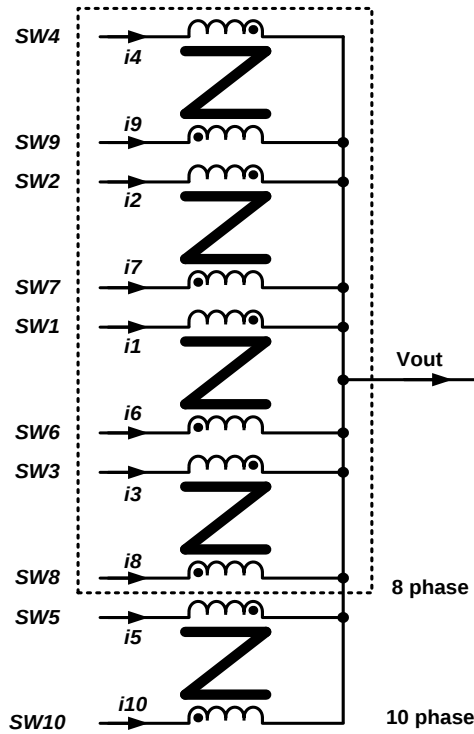


Figure 17: Couple Inductor Connection

When the phase number drops to only one phase at light load, PWM6 is pulled low simultaneously with PWM1 to let the coupled current from the phase one flow through the low-side MOSFET of phase six instead of the bode diode of phase six to improve the efficiency at light load (see Figure 18).

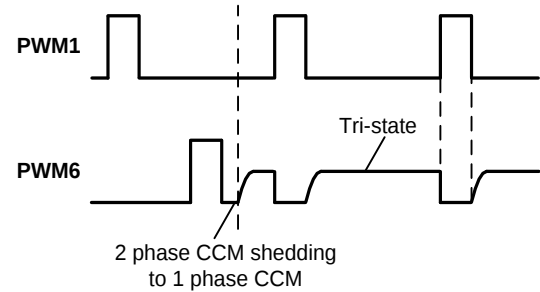


Figure 18: Phase Shedding to 1-Phase CCM

## PMBUS/I<sup>2</sup>C COMMUNICATION

### General Description

The Power Management Bus (PMBus) is an open-standard, power-management protocol that defines a means of communicating with power conversion and other devices. The PMBus is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting the PMBus to the line, a master device generates the SCL signal and device address and arranges the communication sequence. This is based on the principles of I<sup>2</sup>C operation.

The MP2888A supports 100kHz, 400kHz, and 1MHz bus timing requirements. Timing and electrical characteristics of the PMBus can be found in the Electrical Characteristics section on page 6 to page 7 or in the PMBus Power Management Protocol Specification Part 1, revision 1.3 available at <http://PMBus.org>.

### PMBus/I<sup>2</sup>C Address

To support multiple VR devices being used with the same PMBus/I<sup>2</sup>C interface, the MP2888A provides PMBus address programming either by ADDR or a register.

The device address is a 7-bit code and ranges from 0x00 to 0x7F. The 3MSB bits are set by the register. The 4LSB bits can be set either by the register or by the ADDR voltage.

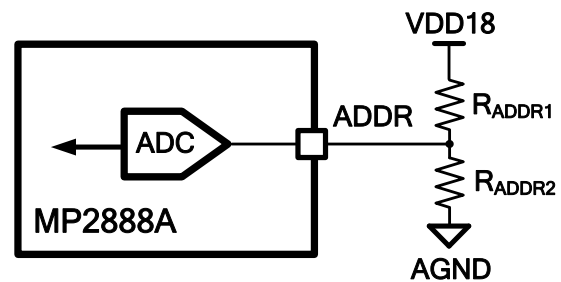
The address of 00h is reserved as the all-call address. Do not use 00h as the MP2888A address.

the Register MFR\_PMBUS\_ADDR (BEh) is used to program or store the device address. Bit[7] sets the mode of the 4LSB address. When bit[7] = 0, the 4LSB bits are determined by the voltage of ADDR, and its value is stored in register BEh bit[3:0] automatically.

The ADDR voltage can be set by a resistor divider (see Figure 19). Using 3MSB = 3'b010 as an example, Table 6 shows the resistor values for different 4LSB addresses.

**Table 6: Pin Configuration for PMBus/I<sup>2</sup>C Address**

| PMBus Address | Setting Point (V) | R <sub>ADDR1</sub> (kΩ) 1% | R <sub>ADDR2</sub> (kΩ) 1% |
|---------------|-------------------|----------------------------|----------------------------|
| 20h           | 0                 | -                          | 0                          |
| 21h           | 0.031             | 3.32                       | 0.059                      |
| 22h           | 0.057             | 3.32                       | 0.11                       |
| 23h           | 0.084             | 3.32                       | 0.162                      |
| 24h           | 0.116             | 3.32                       | 0.226                      |
| 25h           | 0.156             | 3.32                       | 0.316                      |
| 26h           | 0.205             | 3.32                       | 0.43                       |
| 27h           | 0.266             | 3.32                       | 0.576                      |
| 28h           | 0.340             | 3.32                       | 0.768                      |
| 29h           | 0.430             | 3.32                       | 1.05                       |
| 2Ah           | 0.540             | 3.32                       | 1.43                       |
| 2Bh           | 0.675             | 3.32                       | 2                          |
| 2Ch           | 0.844             | 3.32                       | 2.94                       |
| 2Dh           | 1.048             | 3.32                       | 4.64                       |
| 2Eh           | 1.301             | 3.32                       | 8.66                       |
| 2Fh           | 1.500             | 3.32                       | 16.5                       |



**Figure 19: Recommend Circuit Design of ADDR**

### Data and Numerical Format

The MP2888A uses the direct format internally to represent real-world values such as voltage, current, power, temperature, time, etc.

All numbers with no suffix in this document are in a decimal format unless explicitly designated otherwise.

Numbers in a binary format are indicated by a prefix n'b, where n is the binary count. For example, 3'b000 is a 3-bit binary data, and the data is 000. The suffix h indicates a hexadecimal format, which is used for the register address number in this document.

The symbol 0x indicates a hexadecimal format, which is used for the value in the register. For example, 0x88 is a 1-byte number whose decimal value is 136.

## PMBus Communication Failure

A data transmission fault occurs when the data is not transferred properly between the devices. There are several types of data transmission faults listed below.

- Sending too few data
- Reading too few data
- The master sends too many bytes
- The MP2888A reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The CLEAR\_FAULTS (03h) command can be used to clear the fault record.

## PMBus/I<sup>2</sup>C Transmission Structure

The MP2888A supports five kinds of transmission structures with or without PEC.

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

The MP2888A can support the packet error checking (PEC) mechanism, which can improve reliability and communication robustness. The PEC is a CRC-8 error-checking byte calculated on all the message bytes (including addresses and read/write bits). The MP2888A only processes the message if the PEC is correct.

The PEC is calculated in CRC-8 represented by the polynomial in Equation (14):

$$C(x) = x^8 + x^2 + x^1 + 1 \quad (14)$$

Figure 20a shows the supported PMBus/I<sup>2</sup>C transmission structure without PEC. Figure 20b shows the supported PMBus/I<sup>2</sup>C transmission structure with PEC.

To read or write registers of the MP2888A, the PMBus/I<sup>2</sup>C command must be compliant with the byte number of the registers in the table of the register map.

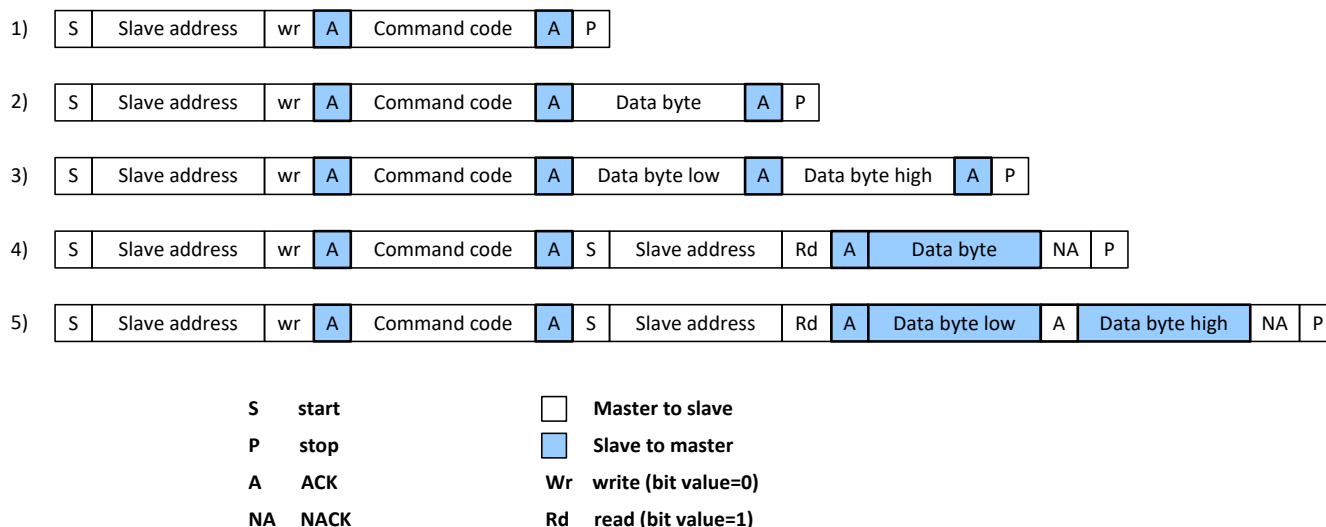
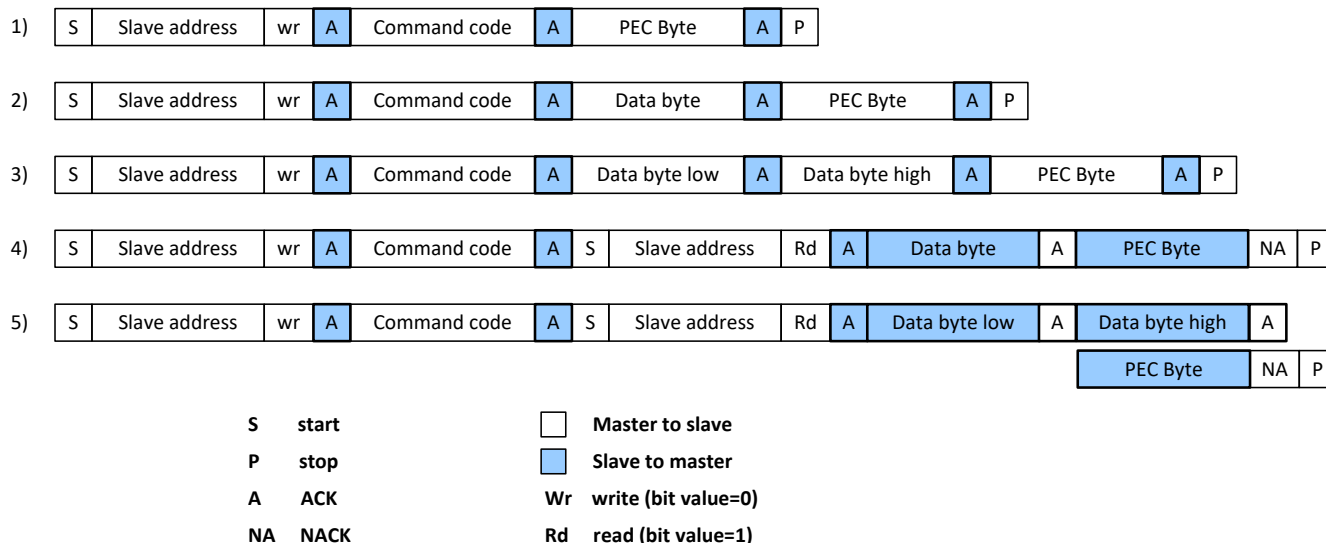


Figure 20a: Supported PMBus/I<sup>2</sup>C Transmission Structure without PEC


**Figure 20b: Supported PMBus/I<sup>2</sup>C Transmission Structure with PEC**

### PMBus Reporting and Status Monitoring

The MP2888A supports real-time monitoring of the VR operation parameters and status using the PMBus interface (see Table 7).

For high-power applications with an output current greater than 1024A, the MP2888A uses register bits to scale the current rate of the platform via register MFR\_SYS\_CONFIG (44h).

When the total current report range is doubled, the setting of the registers in Table 8 should be updated accordingly.

When the phase current report range is doubled, the setting of the registers in Table 9 should be updated accordingly.

**Table 7: PMBus Monitored Parameters**

| Parameter                  | PMBus            | Register |
|----------------------------|------------------|----------|
| Output voltage             | 1mV/LSB          | 8Bh      |
| Output current             | Refer to Table 8 | 8Ch      |
| Output power               |                  | 96h      |
| Input power                |                  | 97h      |
| Temperature                | 0.1°C/LSB        | 8Dh      |
| Input voltage              | 0.03125V/LSB     | 88h      |
| Phase current              | Refer to 73h~77h |          |
| V <sub>OUT</sub> OV fault  | ✓                | 7Ah      |
| V <sub>OUT</sub> UV fault  | ✓                | 7Ah      |
| OC fault                   | ✓                | 7Bh      |
| OT fault                   | ✓                | 7Dh      |
| V <sub>IN</sub> UVLO fault | ✓                | 7Ch      |
| V <sub>IN</sub> OVP fault  | ✓                | 7Ch      |
| PMBus fault                | ✓                | 7Eh      |
| EEPROM fault               | ✓                | 7Eh      |
| V <sub>OUT</sub> UV warn   | ✓                | 7Ah      |
| VID max/min extend warn    | ✓                | 7Ah      |
| OC warn                    | ✓                | 7Bh      |
| OP warn                    | ✓                | 7Bh      |
| OT warn                    | ✓                | 7Dh      |
| V <sub>IN</sub> UV warn    | ✓                | 7Ch      |
| PEC error                  | ✓                | 7Eh      |
| CRC error                  | ✓                | 7Eh      |

**Table 8: Registers Related to Total Current Report Rate**

| Register                    | MFR_SYS_CONFIG<br>(44h) Bit[3] |          |
|-----------------------------|--------------------------------|----------|
|                             | 1'b0                           | 1'b1     |
| Output current (8Ch)        | 0.25A/LSB                      | 0.5A/LSB |
| Output power (96h)          | 0.5W/LSB                       | 1W/LSB   |
| Input power (97h)           |                                |          |
| POUT_OP_WARN_LIMIT<br>(6Ah) | 1W/LSB                         | 2W/LSB   |
| IOUT_OC_WARN_LIMIT<br>(4Ah) | 1A/LSB                         | 2A/LSB   |
| MFR_APS_LEVLE<br>(E3h~E7h)  |                                |          |
| MFR_APS_HYS (E8h)           |                                |          |
| OCP_THRESHOLD (ECh)         |                                |          |
| IOUT_CAL_GAIN (38h)         | Refer to register map          |          |
| IOUT_CAL_OFFSET (39h)       |                                |          |

**Table 9: Registers Related to Phase Current Report Rate**

| Register                | MFR_SYS_CONFIG (44h) Bit[4] |        |
|-------------------------|-----------------------------|--------|
|                         | 1'b0                        | 1'b1   |
| Phase current (73h~77h) | x1                          | x2     |
| MFR_OCP_PHASE (EDh)     | 1A/LSB                      | 2A/LSB |
| MFR_CUR_GAIN (C2h)      | Refer to register map       |        |
| MFR_CS_OFFSET (4Ch~4Eh) |                             |        |

### PMBus Write Protection

The MP2888A supports PMBus write protection (WP) by entering a 16-bit password in register MFR\_USER\_PWD (04h). Store the password to the EEPROM, and after the power-on reset, no register can be written via the PMBus until the correct password is entered.

Note that if a wrong password is entered, the MP2888A disables the PMBus write function until the VDD33 supply toggles.

The correct password can be entered only once. If the password is sent more than once, correct or not, the MP2888A disables the PMBus write function until the VDD33 supply toggles.

Set the register MFR\_USER\_PWD (04h) to 0x0000 if the password function is not needed.

## PMBUS COMMANDS @ PAGE 0

| Command Code | Command Name       | Type | Bytes |
|--------------|--------------------|------|-------|
| 00h          | PAGE               | r/w  | 1     |
| 01h          | OPERATION          | r/w  | 1     |
| 03h          | CLEAR_FAULTS       | Send | 0     |
| 04h          | MFR_USER_PWD       | w    | 2     |
| 05h          | BUF_REG_UPD        | Send | 0     |
| 06h          | MFR_EEPROM_CTRL    | r/w  | 1     |
| 13h          | WRITE_PROTECT      | r/w  | 1     |
| 15h          | STORE_USER_ALL     | Send | 0     |
| 16h          | RESTARE_USER_ALL   | Send | 0     |
| 1Ch          | MFR_DROOP_CMPN1    | r/w  | 2     |
| 1Dh          | MFR_DROOP_CMPN2    | r/w  | 2     |
| 1Eh          | MFR_IDROOP_CTRL    | r/w  | 1     |
| 1Fh          | VOUT_MIN           | r/w  | 2     |
| 21h          | VOUT_COMMAND       | r/w  | 2     |
| 23h          | VOUT_OFFSET        | r/w  | 2     |
| 24h          | VOUT_MAX           | r/w  | 2     |
| 25h          | VOUT_MARGIN_HIGH   | r/w  | 2     |
| 26h          | VOUT_MARGIN_LOW    | r/w  | 2     |
| 27h          | VENDOR_ID_USER     | r/w  | 1     |
| 28h          | PRODUCT_ID_USER    | r/w  | 1     |
| 29h          | PRODUCT_REV_USER   | r/w  | 1     |
| 2Ah          | MFR_DC_DIV_SET     | r/w  | 2     |
| 2Bh          | MFR_IDROOP_OFFSET  | r/w  | 1     |
| 2Ch          | MFR_OVUV_SEL       | r/w  | 2     |
| 2Dh          | MFR_RSAMP_OFFSET   | r/w  | 1     |
| 2Eh          | MFR_VFB_DIGI_GAIN  | r/w  | 2     |
| 2Fh          | MFR_IMON_DIGI_GAIN | r/w  | 2     |
| 30h          | MFR_DC_LOOP_CTRL   | r/w  | 2     |
| 31h          | MFR_CB_LOOP_CTRL   | r/w  | 1     |
| 32h          | MFR_FS_LOOP_CTRL   | r/w  | 2     |
| 34h          | MFR_T_ALERT_CTRL   | r/w  | 2     |
| 35h          | VIN_ON             | r/w  | 2     |
| 36h          | VIN_OFF            | r/w  | 2     |
| 38h          | IOUT_CAL_GAIN      | r/w  | 2     |
| 39h          | IOUT_CAL_OFFSET    | r/w  | 2     |
| 3Ah          | MFR_PROTECT_DIS    | r/w  | 2     |
| 3Bh          | MFR_PS_FORCE       | r/w  | 2     |
| 3Dh          | MFR_SLOPE_ADV      | r/w  | 2     |
| 3Fh          | MFR_PWM_LIMIT      | r/w  | 2     |
| 40h          | MFR_OSR_SET        | r/w  | 2     |
| 43h          | MFR_T_ALERT_CTRL2  | r/w  | 2     |
| 44h          | MFR_SYS_CONFIG     | r/w  | 2     |

# PMBUS COMMANDS @ PAGE 0 (continued)

| Command Code | Command Name       | Type | Bytes |
|--------------|--------------------|------|-------|
| 45h          | MFR_VR_CONFIG3     | r/w  | 2     |
| 46h          | CONFIG_ID          | r/w  | 2     |
| 47h          | CONFIG_REV_MPS     | r/w  | 2     |
| 4Ah          | IOUT_OC_WARN_LIMIT | r/w  | 2     |
| 4Ch          | MFR_CS_OFFSET1     | r/w  | 2     |
| 4Dh          | MFR_CS_OFFSET2     | r/w  | 2     |
| 4Eh          | MFR_CS_OFFSET3     | r/w  | 2     |
| 51h          | OT_WARN_LIMIT      | r/w  | 2     |
| 55h          | VIN_OV_FAULT_LIMIT | r/w  | 2     |
| 58h          | VIN_UV_WARN_LIMIT  | r/w  | 2     |
| 5Dh          | MFR_DELAY_SET      | r/w  | 2     |
| 5Eh          | POWER_GOOD_ON      | r/w  | 2     |
| 5Fh          | POWER_GOOD_OFF     | r/w  | 2     |
| 60h          | TON_DELAY          | r/w  | 2     |
| 64h          | TOFF_DELAY         | r/w  | 2     |
| 6Ah          | POUT_OP_WARN_LIMIT | r/w  | 2     |
| 6Bh          | START_CATCH_AVE    | Send | 0     |
| 73h          | READ_CS1_2         | r    | 2     |
| 74h          | READ_CS3_4         | r    | 2     |
| 75h          | READ_CS5_6         | r    | 2     |
| 76h          | READ_CS7_8         | r    | 2     |
| 77h          | READ_CS9_10        | r    | 2     |
| 78h          | STATUS_BYTE        | r    | 1     |
| 79h          | STATUS_WORD        | r    | 2     |
| 7Ah          | STATUS_VOUT        | r    | 1     |
| 7Bh          | STATUS_IOUT        | r    | 1     |
| 7Ch          | STATUS_INPUT       | r    | 1     |
| 7Dh          | STATUS_TEMPERATURE | r    | 1     |
| 7Eh          | STATUS_CML         | r    | 1     |
| 88h          | READ_VIN           | r    | 2     |
| 8Bh          | READ_VOUT          | r    | 2     |
| 8Ch          | READ_IOUT          | r    | 2     |
| 8Dh          | READ_TEMPERATURE   | r    | 2     |
| 95h          | READ_EFFICIENCY    | r    | 2     |
| 96h          | READ_POUT          | r    | 2     |
| 97h          | READ_PIN           | r    | 2     |
| A3h          | MFR_APS_FS_LIMIT1  | r/w  | 2     |
| A4h          | MFR_APS_FS_LIMIT2  | r/w  | 2     |
| A5h          | MFR_APS_FS_LIMIT3  | r/w  | 2     |
| A6h          | MFR_APS_FS_LIMIT4  | r/w  | 2     |
| A7h          | MFR_APS_FS_CTRL1   | r/w  | 2     |

# PMBUS COMMANDS @ PAGE 0 (continued)

| Command Code | Command Name           | Type | Bytes |
|--------------|------------------------|------|-------|
| A8h          | MFR_APS_FS_CTRL2       | r/w  | 2     |
| A9h          | MFR_PHASE_SHED_CTRL    | r/w  | 2     |
| AAh          | MFR_LOW_PHASE_CNT      | r/w  | 2     |
| ABh          | MFR_APS_CTRL           | r/w  | 2     |
| ADh          | MFR_REPORT_CTRL        | r/w  | 2     |
| AEnh         | MFR_PWMVID_TARGET_CTRL | r/w  | 2     |
| AFh          | MFR_PWMVID_UP_COMP     | r/w  | 2     |
| B0h          | MFR_PWMVID_MAX_DUTY    | r/w  | 2     |
| B1h          | MFR_PWMVID_FLTR_CTRL1  | r/w  | 2     |
| B2h          | MFR_PWMVID_FLTR_CTRL2  | r/w  | 2     |
| B3h          | MFR_DUTY_TO_VID_GAIN   | r/w  | 2     |
| B4h          | MFR_PARM_VOUT_MIN      | r/w  | 2     |
| B5h          | MFR_PARM_RC_CONST      | r/w  | 2     |
| B6h          | MFR_PARM_VBOOT_DUTY    | r/w  | 2     |
| B7h          | MFR_PARM_SLEW_TRAN     | r/w  | 2     |
| B8h          | MFR_PARM_BOOT_TRAN     | r/w  | 2     |
| B9h          | MFR_BOOT_SR            | r/w  | 2     |
| BAh          | MFR_SLEW_SR            | r/w  | 2     |
| BBh          | MFR_VBOOT              | r/w  | 2     |
| BCh          | MFR_VID_SD             | r/w  | 2     |
| BDh          | MFR_FS                 | r/w  | 2     |
| BEh          | MFR_PMBUS_ADDR         | r/w  | 1     |
| BFh          | MFR_VIN_SENSE_OFFSET   | r/w  | 2     |
| C0h          | MFR_VIN_SCALE_LOOP     | r/w  | 1     |
| C1h          | MFR_TEMP_GAIN_OFFSET   | r/w  | 2     |
| C2h          | MFR_CUR_GAIN           | r/w  | 2     |
| C5h          | MFR_BLANK_TIME         | r/w  | 2     |
| C6h          | MFR_SLOPE_SR_DCM       | r/w  | 2     |
| C7h          | MFR_SLOPE_CNT_DCM      | r/w  | 2     |
| C8h          | MFR_SLOPE_SR_10P       | r/w  | 2     |
| C9h          | MFR_SLOPE_CNT_10P      | r/w  | 2     |
| CAh          | MFR_SLOPE_SR_9P        | r/w  | 2     |
| CBh          | MFR_SLOPE_CNT_9P       | r/w  | 2     |
| CCh          | MFR_SLOPE_SR_8P        | r/w  | 2     |
| CDh          | MFR_SLOPE_CNT_8P       | r/w  | 2     |
| CEh          | MFR_SLOPE_SR_7P        | r/w  | 2     |
| CFh          | MFR_SLOPE_CNT_7P       | r/w  | 2     |
| D0h          | MFR_SLOPE_SR_6P        | r/w  | 2     |
| D1h          | MFR_SLOPE_CNT_6P       | r/w  | 2     |
| D2h          | MFR_SLOPE_SR_5P        | r/w  | 2     |
| D3h          | MFR_SLOPE_CNT_5P       | r/w  | 2     |

## PMBUS COMMANDS @ PAGE 0 (continued)

| Command Code | Command Name        | Type | Bytes |
|--------------|---------------------|------|-------|
| D4h          | MFR_SLOPE_SR_4P     | r/w  | 2     |
| D5h          | MFR_SLOPE_CNT_4P    | r/w  | 2     |
| D6h          | MFR_SLOPE_SR_3P     | r/w  | 2     |
| D7h          | MFR_SLOPE_CNT_3P    | r/w  | 2     |
| D8h          | MFR_SLOPE_SR_2P     | r/w  | 2     |
| D9h          | MFR_SLOPE_CNT_2P    | r/w  | 2     |
| DAh          | MFR_SLOPE_SR_1P     | r/w  | 2     |
| DBh          | MFR_SLOPE_CNT_1P    | r/w  | 2     |
| DDh          | MFR_SLOPE_TRIM1     | r/w  | 2     |
| DEh          | MFR_SLOPE_TRIM2     | r/w  | 2     |
| DFh          | MFR_SLOPE_TRIM3     | r/w  | 2     |
| E0h          | MFR_SLOPE_TRIM4     | r/w  | 2     |
| E1h          | MFR_VR_CONFIG1      | r/w  | 2     |
| E2h          | MFR_VR_CONFIG2      | r/w  | 1     |
| E3h          | MFR_APS_LEVEL1      | r/w  | 2     |
| E4h          | MFR_APS_LEVEL2      | r/w  | 2     |
| E5h          | MFR_APS_LEVEL3      | r/w  | 2     |
| E6h          | MFR_APS_LEVEL4      | r/w  | 2     |
| E7h          | MFR_APS_LEVEL5      | r/w  | 2     |
| E8h          | MFR_APS_HYS         | r/w  | 1     |
| E9h          | MFR_TSNS_OT_SET     | r/w  | 2     |
| EAh          | MFR_VTEMP_OT_SET    | r/w  | 2     |
| ECh          | MFR_OCP_TOTAL       | r/w  | 2     |
| EDh          | MFR_OCP_PHASE       | r/w  | 1     |
| EEh          | MFR_OVP_UVP_SET     | r/w  | 2     |
| F8h          | MFR_FAULTS1         | r    | 2     |
| F9h          | MFR_FAULTS2         | r    | 2     |
| FAh          | MFR_FAULTS3         | r    | 2     |
| FBh          | MFR_FAULTS4         | r    | 2     |
| FFh          | CLEAR_EEPROM_FAULTS | Send | 0     |

## PMBUS COMMANDS @ PAGE 29

| Command Code | Command Name     | Type | Bytes |
|--------------|------------------|------|-------|
| FBh          | MFR_LAST_FAULTS1 | r/w  | 2     |
| FCh          | MFR_LAST_FAULTS2 | r/w  | 2     |
| FDh          | MFR_LAST_FAULTS3 | r/w  | 2     |
| FEh          | MFR_LAST_FAULTS4 | r/w  | 2     |

## PAGE 0 REGISTER MAP

### PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor all registers, including test mode and the EEPROM, through only one physical address.

| Command  | PAGE            |     |      |     |     |     |     |     |
|----------|-----------------|-----|------|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |      |     |     |     |     |     |
| Bit      | 7               | 6   | 5    | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w  | r/w | r/w | r/w | r/w | r/w |
| Function | X               | X   | PAGE |     |     |     |     |     |

| Bits | Bit Name | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5:0  | PAGE     | <p>Register page selector.</p> <p>00(hex): Page 0, all PMBus commands address normal function registers<br/> 02(hex): Page 2, all PMBus commands address test mode registers<br/> 28(hex): Page 28, all PMBus commands address EEPROM registers (00h~FFh)<br/> 29(hex): Page 29, all PMBus commands address EEPROM registers (100h~1FFh)</p> <p>EE_WORD_WR_EN = 1: Page 28/Page 29 is accessible<br/> EE_WORD_WR_EN = 0: Page 28/Page 29 is not accessible<br/> EE_WORD_WR_EN is bit2 of MFR_EEPROM_CTRL (06h)</p> |

### OPERATION (01h)

This register is used to turn the output on or off when EN is high. OPERATION is also used to set the output voltage to the upper or lower MARGIN voltages.

| Command  | OPERATION       |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |
| Bit      | 7               | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | OPERATION_MODE  |     |     |     |     |     |     |     |

| Bits | Bit Name       | Description                                                                                                                                                                                   |
|------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | OPERATION_MODE | <p>Operation mode.</p> <p>00xxxxx: Hi-Z off<br/> 01xxxxx: soft off<br/> 1000xxxx: normal on<br/> 1001xxxx: margin low<br/> 1010xxxx: margin high</p> <p>The value of “x” does not matter.</p> |

### CLEAR\_FAULTS (03h)

The CLEAR\_FAULTS command is used to clear any fault bits in all status registers (STATUS\_BYTE, STATUS\_WORD, STATUS\_VOUT, STATUS\_IOUT, STATUS\_INPUT, STATUS\_TEMPERATURE, and STATUS\_CML).

This command is write only. There is no data byte for this command.

### MFR\_USER\_PWD (04h)

This register presets the password for PMBus write protection.

|          |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Command  | MFR_USER_PWD    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Format   | Unsigned binary |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | w               | w  | w  | w  | w  | w  | w | w | w | w | w | w | w | w | w | w |
| Function | MFR_USER_PWD    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bits | Bit Name     | Description                                                                          |
|------|--------------|--------------------------------------------------------------------------------------|
| 16:0 | MFR_USER_PWD | Password for PMBus write protection.<br>Set password to 0x0000 for unprotected mode. |

### BUF\_REG\_UPD (05h)

Registers PHASE\_CNT (E1h) and MFR\_FS (BDh) are double-buffered. The BUF\_REG\_UPD command can update them on-the-fly simultaneously.

This command is write only. There is no data byte for this command.

### MFR\_EEPROM\_CTRL (06h)

This register controls the memory behavior and selects the trim register for the ratio of  $I_{DROOP} / I_{CSSUM}$  to increase overall droop accuracy.

|          |                 |     |     |                 |     |     |     |     |
|----------|-----------------|-----|-----|-----------------|-----|-----|-----|-----|
| Command  | MFR_EEPROM_CTRL |     |     |                 |     |     |     |     |
| Format   | Unsigned binary |     |     |                 |     |     |     |     |
| Bit      | 7               | 6   | 5   | 4               | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w             | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | IDROOP_TRIM_SEL |     |     |     |     |

| Bits | Bit Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                       |               |                       |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------|-----------------------|---------------|-------|-----------------------|-----------|-----------------------|----------|-----------|----------|------------|----------|------------|----------|-----------------------|------------|-----------------------|----------|------------|-----------|------------|-----------|------------|
| 7:5  | RESERVED        | Unused. X indicates that writes are ignored and always reads are 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                       |               |                       |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
| 4:3  | IDROOP_TRIM_SEL | Trim register selector for the ratio of $I_{DROOP} / I_{CSSUM}$ .<br><br>00: select TRIM_IDROOP1 (9Ch)<br>01: select TRIM_IDROOP2 (9Dh)<br>10: select TRIM_IDROOP3 (9Eh)<br>11: select TRIM_IDROOP4 (9Fh)<br><br>There are 16 types of ratios for $I_{DROOP} / I_{CSSUM}$ divided into four groups. Each group has one trim value for corresponding ratios (see table below). The selection of the trim register must match IDROOP_SET in register 1Ch.                                                                                                                                                                                                     |                       |               |                       |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|      |                 | <table><tr><th>IDROOP_SET</th><th>Trim Register</th><th>IDROOP_SET</th><th>Trim Register</th></tr><tr><td>0 (0)</td><td rowspan="4">TRIM_IDROOP1<br/>(9Ch)</td><td>8 (12/64)</td><td rowspan="4">TRIM_IDROOP3<br/>(9Eh)</td></tr><tr><td>1 (5/64)</td><td>9 (13/64)</td></tr><tr><td>2 (6/64)</td><td>10 (14/64)</td></tr><tr><td>3 (7/64)</td><td>11 (15/64)</td></tr><tr><td>4 (8/64)</td><td rowspan="4">TRIM_IDROOP2<br/>(9Dh)</td><td>12 (16/64)</td><td rowspan="4">TRIM_IDROOP4<br/>(9Fh)</td></tr><tr><td>5 (9/64)</td><td>13 (17/64)</td></tr><tr><td>6 (10/64)</td><td>14 (18/64)</td></tr><tr><td>7 (11/64)</td><td>15 (19/64)</td></tr></table> | IDROOP_SET            | Trim Register | IDROOP_SET            | Trim Register | 0 (0) | TRIM_IDROOP1<br>(9Ch) | 8 (12/64) | TRIM_IDROOP3<br>(9Eh) | 1 (5/64) | 9 (13/64) | 2 (6/64) | 10 (14/64) | 3 (7/64) | 11 (15/64) | 4 (8/64) | TRIM_IDROOP2<br>(9Dh) | 12 (16/64) | TRIM_IDROOP4<br>(9Fh) | 5 (9/64) | 13 (17/64) | 6 (10/64) | 14 (18/64) | 7 (11/64) | 15 (19/64) |
|      |                 | IDROOP_SET                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Trim Register         | IDROOP_SET    | Trim Register         |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|      |                 | 0 (0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | TRIM_IDROOP1<br>(9Ch) | 8 (12/64)     | TRIM_IDROOP3<br>(9Eh) |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|      |                 | 1 (5/64)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                       | 9 (13/64)     |                       |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|      |                 | 2 (6/64)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                       | 10 (14/64)    |                       |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|      |                 | 3 (7/64)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                       | 11 (15/64)    |                       |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|      |                 | 4 (8/64)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | TRIM_IDROOP2<br>(9Dh) | 12 (16/64)    | TRIM_IDROOP4<br>(9Fh) |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|      |                 | 5 (9/64)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                       | 13 (17/64)    |                       |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|      |                 | 6 (10/64)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                       | 14 (18/64)    |                       |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |
|      |                 | 7 (11/64)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                       | 15 (19/64)    |                       |               |       |                       |           |                       |          |           |          |            |          |            |          |                       |            |                       |          |            |           |            |           |            |

|   |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2 | EE_WORD_WR_EN  | Enable bit for writing and reading the EEPROM via the PMBus on Page 28/Page 29.<br>0: disable<br>1: enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1 | FAULT_SAVE_EN  | Enable bit for auto-saving a fault status into the EEPROM.<br>0: disable<br>1: enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 0 | CRC_PROTECT_EN | Enable bit for CRC fault protection.<br>0: EEPROM CRC fault does not stop the output power<br>1: EEPROM CRC fault stops the output power. The device enters shutdown mode.<br><br>In the process of storing memory data into the EEPROM, the device calculates the CRC for all saved bits and saves the CRC result in the EEPROM. In the process of restoring the EEPROM data to the memory, the device calculates the CRC for all restored bits. At the end of the restore process, the device checks the CRC results saved in the EEPROM with the calculated CRC. If they do not match, the device reports a CRC fault and sets bit[4] of STATUS_CML (7Eh). |

### WRITE\_PROTECT (13h)

This register is used to enable EEPROM write protection.

| Command  | WRITE_PROTECT           |     |     |     |     |     |     |     |
|----------|-------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary         |     |     |     |     |     |     |     |
| Bit      | 7                       | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                     | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | EEPROM write protection |     |     |     |     |     |     |     |

| Bits | Bit Name  | Description                                                                                             |
|------|-----------|---------------------------------------------------------------------------------------------------------|
| 7:0  | EEPROM_WP | Enable this bit for EEPROM write protection.<br>0x00: disable EEPROM write<br>0x63: enable EEPROM write |

### STORE\_USER\_ALL (15h)

The STORE\_USER\_ALL command instructs the PMBus device to copy the Page 0 contents of the operating memory to the matching locations in the EEPROM. In the process, the device calculates the CRC for all saved bits and saves the CRC result in the EEPROM.

This command is write only. There is no data byte for this command.

### RESTORE\_USER\_ALL (16h)

The RESTORE\_USER\_ALL command instructs the PMBus device to copy the Page 0 contents from the EEPROM and overwrite the matching locations in the operating memory. In this process, the device calculates the CRC for all restored bits. If the calculated CRC does not match the CRC value saved in the EEPROM, the device reports the CRC error via bit[4] of register STATUS\_CML (7Eh). The CRC error protect action is determined by bit[0] of MFR\_EEPROM\_CTRL (06h).

After the POR, the device triggers the memory copy operation from the EEPROM. This process is the same as the operating RESTORE\_USER\_ALL command.

It is NOT permitted to send this command while the device is outputting power; otherwise, the command will be ignored.

This command is write only. There is no data byte for this command.

**MFR\_DROOP\_CMPN1 (1Ch)**

This register is used to compensate for extra droop current for the linear upward DVID with a droop resistor.

| Command  | MFR_DROOP_CMPN1    |     |     |     |     |     |     |     |                  |     |     |     |     |     |     |     |
|----------|--------------------|-----|-----|-----|-----|-----|-----|-----|------------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary    |     |     |     |     |     |     |     |                  |     |     |     |     |     |     |     |
| Bit      | 15                 | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7                | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | CNT_DROOP_CMPN_DEC |     |     |     |     |     |     |     | DROOP_CMPN_LIMIT |     |     |     |     |     |     |     |

| Bits | Bit Name           | Description                                                                                  |
|------|--------------------|----------------------------------------------------------------------------------------------|
| 15   | DROOP_CMPN_EN      | Enable bit of the droop compensation for the upward DVID.<br>0: disable<br>1: enable         |
| 14:9 | CNT_DROOP_CMPN_DEC | Interval time to decrease each step of droop compensation after the upward DVID.<br>50ns/LSB |
| 8:6  | CNT_DROOP_CMPN_INC | VID step counter for increasing each step of droop compensation during the upward DVID.      |
| 5:0  | DROOP_CMPN_LIMIT   | Maximum droop compensation value for upward DVID. 6.25mV/LSB.                                |

**MFR\_DROOP\_CMPN2 (1Dh)**

This register is used to compensate for extra droop current for linear upward DVID with a droop resistor and set the VID-DAC filter parameter.

| Command  | MFR_DROOP_CMPN2     |     |     |     |     |     |     |     |                      |     |     |     |     |     |     |     |
|----------|---------------------|-----|-----|-----|-----|-----|-----|-----|----------------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary     |     |     |     |     |     |     |     |                      |     |     |     |     |     |     |     |
| Bit      | 15                  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7                    | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                 | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w                  | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | CNT_DROOP_CMPN_HOLD |     |     |     |     |     |     |     | DROOP_CMPN_FALL_THRE |     |     |     |     |     |     |     |

| Bits  | Bit Name             | Description                                                                                                                         |
|-------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | VID_DAC_FLT_SEL      | Time constant of the VID-DAC output filter for the downward DVID and steady state.<br>00: 2μs<br>01: 4μs<br>10: 6.5μs<br>11: 8.5μs  |
| 13    | VID_FLT_EN           | Enable bit of the VID-DAC output filter for the downward DVID and steady state.<br>0: disable<br>1: enable                          |
| 12    | DAC_CMPR_EN          | Enable bit of the comparator of the VID-DAC output with its filtered voltage.<br>0: disable<br>1: enable                            |
| 11:6  | CNT_DROOP_CMPN_HOLD  | Holding time before decreasing the droop compensation after the upward DVID.<br>50ns/LSB                                            |
| 5:0   | DROOP_CMPN_FALL_THRE | Droop compensation falling threshold for reactivating the VID-DAC output filter.<br>6.25mV/LSB. Only effective when VID_FLT_EN = 1. |

**MFR\_IDROOP\_CTRL (1Eh)**

This register sets the droop current gain and AC droop.

|          |                 |     |     |     |            |     |     |     |
|----------|-----------------|-----|-----|-----|------------|-----|-----|-----|
| Command  | MFR_IDROOP_CTRL |     |     |     |            |     |     |     |
| Format   | Unsigned binary |     |     |     |            |     |     |     |
| Bit      | 7               | 6   | 5   | 4   | 3          | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w        | r/w | r/w | r/w |
| Function | x               | x   |     |     | IDROOP_SET |     |     |     |

| Bits       | Bit Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                 |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
|------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----------------|------------|-----------------|---|---|---|-------|---|------|---|-------|---|------|----|-------|---|------|----|-------|---|------|----|-------|---|------|----|-------|---|-------|----|-------|---|-------|----|-------|
| 7:6        | RESERVED         | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                 |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 5          | AC_DROOP_EN      | Enable bit of the AC droop loop. This loop eliminates the droop effect in steady state but keeps the droop effective during the load transient or DVID.<br>0: disable<br>1: enable                                                                                                                                                                                                                                                                                                                                                                                                  |                 |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 4          | AC_DROOP_LOOP_BW | Sets the bandwidth of the AC droop loop. Only effective when AC_DROOP_EN = 1.<br>0: BW = 20kHz<br>1: BW = 40kHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                 |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 3:0        | IDROOP_SET       | <table><tr><th>IDROOP_SET</th><th>IdROOP / IcSSUM</th><th>IDROOP_SET</th><th>IdROOP / IcSSUM</th></tr><tr><td>0</td><td>0</td><td>8</td><td>12/64</td></tr><tr><td>1</td><td>5/64</td><td>9</td><td>13/64</td></tr><tr><td>2</td><td>6/64</td><td>10</td><td>14/64</td></tr><tr><td>3</td><td>7/64</td><td>11</td><td>15/64</td></tr><tr><td>4</td><td>8/64</td><td>12</td><td>16/64</td></tr><tr><td>5</td><td>9/64</td><td>13</td><td>17/64</td></tr><tr><td>6</td><td>10/64</td><td>14</td><td>18/64</td></tr><tr><td>7</td><td>11/64</td><td>15</td><td>19/64</td></tr></table> | IDROOP_SET      | IdROOP / IcSSUM | IDROOP_SET | IdROOP / IcSSUM | 0 | 0 | 8 | 12/64 | 1 | 5/64 | 9 | 13/64 | 2 | 6/64 | 10 | 14/64 | 3 | 7/64 | 11 | 15/64 | 4 | 8/64 | 12 | 16/64 | 5 | 9/64 | 13 | 17/64 | 6 | 10/64 | 14 | 18/64 | 7 | 11/64 | 15 | 19/64 |
| IDROOP_SET | IdROOP / IcSSUM  | IDROOP_SET                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | IdROOP / IcSSUM |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 0          | 0                | 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 12/64           |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 1          | 5/64             | 9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 13/64           |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 2          | 6/64             | 10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 14/64           |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 3          | 7/64             | 11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 15/64           |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 4          | 8/64             | 12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 16/64           |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 5          | 9/64             | 13                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 17/64           |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 6          | 10/64            | 14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 18/64           |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |
| 7          | 11/64            | 15                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 19/64           |                 |            |                 |   |   |   |       |   |      |   |       |   |      |    |       |   |      |    |       |   |      |    |       |   |      |    |       |   |       |    |       |   |       |    |       |

**VOUT\_MIN (1Fh)**

This register sets the minimum voltage setting for both PWM-VID mode and PMBus VID override mode.

|          |          |     |     |     |     |     |     |          |     |     |     |     |     |     |     |     |
|----------|----------|-----|-----|-----|-----|-----|-----|----------|-----|-----|-----|-----|-----|-----|-----|-----|
| Command  | VOUT_MIN |     |     |     |     |     |     |          |     |     |     |     |     |     |     |     |
| Format   | VID      |     |     |     |     |     |     |          |     |     |     |     |     |     |     |     |
| Bit      | 15       | 14  | 13  | 12  | 11  | 10  | 9   | 8        | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x        | x   | x   | x   | x   | x   | x   | VOUT_MIN |     |     |     |     |     |     |     |     |

| Bits | Bit Name | Description                                                                                                                                           |
|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                                                                                     |
| 8:0  | VOUT_MIN | Minimum voltage setting. Any setting smaller than this value is clamped. This is the target VID when the pulse duty from PWM-VID is zero. 6.25mV/LSB. |

### VOUT\_COMMAND (21h)

This register is used to set the output voltage on-the-fly for PMBUS VID override mode.

| Command  | VOUT_COMMAND |     |     |     |     |     |     |              |     |     |     |     |     |     |     |     |
|----------|--------------|-----|-----|-----|-----|-----|-----|--------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | VID          |     |     |     |     |     |     |              |     |     |     |     |     |     |     |     |
| Bit      | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8            | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w          | r/w | r/w | r/w | r/w | r/w | r/w | r/w          | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x            | x   | x   | x   | x   | x   | x   | VOUT_COMMAND |     |     |     |     |     |     |     |     |

| Bits | Bit Name     | Description                                                       |
|------|--------------|-------------------------------------------------------------------|
| 15:9 | RESERVED     | Unused. X indicates that writes are ignored and always read as 0. |
| 8:0  | VOUT_COMMAND | Output voltage for PMBus VID override mode. 6.25mV/LSB.           |

### VOUT\_OFFSET (23h)

This register is used to set the output voltage offset from the VID target for PMBus VID override mode.

| Command  | VOUT_OFFSET |     |     |     |     |     |     |     |             |     |     |     |     |     |     |     |
|----------|-------------|-----|-----|-----|-----|-----|-----|-----|-------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | VID         |     |     |     |     |     |     |     |             |     |     |     |     |     |     |     |
| Bit      | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w         | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w         | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x           | x   | x   | x   | x   | x   | x   | x   | VOUT_OFFSET |     |     |     |     |     |     |     |

| Bits | Bit Name    | Description                                                                                                                       |
|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED    | Unused. X indicates that writes are ignored and always read as 0.                                                                 |
| 7:0  | VOUT_OFFSET | Output voltage offset on the VID reference. 6.25mV/LSB. This value is the two's complement binary format. Bit[7] is the sign bit. |

### VOUT\_MAX (24h)

This register sets the maximum voltage setting for both PWM-VID mode and PMBus VID override mode.

| Command  | VOUT_MAX |     |     |     |     |     |     |          |     |     |     |     |     |     |     |     |
|----------|----------|-----|-----|-----|-----|-----|-----|----------|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | VID      |     |     |     |     |     |     |          |     |     |     |     |     |     |     |     |
| Bit      | 15       | 14  | 13  | 12  | 11  | 10  | 9   | 8        | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x        | x   | x   | x   | x   | x   | x   | VOUT_MAX |     |     |     |     |     |     |     |     |

| Bits | Bit Name | Description                                                                                                                                                                                                                          |
|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                    |
| 8:0  | VOUT_MAX | Maximum voltage setting. Any setting higher than this value is clamped. In PWM-VID mode, this is the target VID when the pulse duty PWM-VID pin is 100%. In PMBus VID override mode, the OVP1 level is VOUT_MAX + 400mV. 6.25mV/LSB. |

**VOUT\_MARGIN\_HIGH (25h)**

This register sets the output voltage when the OPERATION (01h) is set to margin high. VID format.

|          |                  |     |     |     |     |     |     |                  |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Command  | VOUT_MARGIN_HIGH |     |     |     |     |     |     |                  |     |     |     |     |     |     |     |     |
| Format   | VID              |     |     |     |     |     |     |                  |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8                | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | x   | VOUT_MARGIN_HIGH |     |     |     |     |     |     |     |     |

| Bits | Bit Name         | Description                                                         |
|------|------------------|---------------------------------------------------------------------|
| 15:9 | RESERVED         | Unused. X indicates that writes are ignored and always read as 0.   |
| 8:0  | VOUT_MARGIN_HIGH | Sets the output voltage for the PMBus margin high mode. 6.25mV/LSB. |

**VOUT\_MARGIN\_LOW (26h)**

This register sets the output voltage when OPERATION (01h) is set to margin low. VID format.

|          |                 |     |     |     |     |     |     |                 |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Command  | VOUT_MARGIN_LOW |     |     |     |     |     |     |                 |     |     |     |     |     |     |     |     |
| Format   | VID             |     |     |     |     |     |     |                 |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8               | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | x   | VOUT_MARGIN_LOW |     |     |     |     |     |     |     |     |

| Bits | Bit Name        | Description                                                       |
|------|-----------------|-------------------------------------------------------------------|
| 15:9 | RESERVED        | Unused. X indicates that writes are ignored and always read as 0. |
| 8:0  | VOUT_MARGIN_LOW | Sets the output voltage for PMBus margin low mode. 6.25mV/LSB.    |

**VENDOR\_ID\_USER (27h)**

This register sets the vendor ID for users.

|          |                 |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Command  | VENDOR_ID_USER  |     |     |     |     |     |     |     |
| Format   | Unsigned binary |     |     |     |     |     |     |     |
| Bit      | 7               | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | VENDOR_ID_USER  |     |     |     |     |     |     |     |

| Bits | Bit Name       | Description                                           |
|------|----------------|-------------------------------------------------------|
| 7:0  | VENDOR_ID_USER | Vendor ID for users. 0x25 represents MPS Corporation. |

**PRODUCT\_ID\_USER (28h)**

This register sets the product ID for users.

|          |                 |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Command  | PRODUCT_ID_USER |     |     |     |     |     |     |     |
| Format   | Unsigned binary |     |     |     |     |     |     |     |
| BIT      | 7               | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | PRODUCT_ID_USER |     |     |     |     |     |     |     |

| Bits | Bit Name        | Description                                        |
|------|-----------------|----------------------------------------------------|
| 7:0  | PRODUCT_ID_USER | Product ID for users. 0x88 represents the MP2888A. |

**PRODUCT\_REV\_USER (29h)**

This register configures the file code revision.

|          |                  |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|
| Command  | PRODUCT_REV_USER |     |     |     |     |     |     |     |
| Format   | Unsigned binary  |     |     |     |     |     |     |     |
| Bit      | 7                | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | PRODUCT_REV_USER |     |     |     |     |     |     |     |

| Bits | Bit Name         | Description                   |
|------|------------------|-------------------------------|
| 7:0  | PRODUCT_REV_USER | Configure file code revision. |

**MFR\_DC\_DIV\_SET (2Ah)**

This register sets the output voltage sensing.

|          |                 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |            |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------------|
| Command  | MFR_DC_DIV_SET  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |            |
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |            |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0          |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w        |
| Function | x               | x   |     |     |     |     |     |     |     |     |     |     |     |     |     | VOUT_SCALE |

| Bits  | Bit Name           | Description                                                                                                                                                                                                                           |
|-------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | RESERVED           | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                     |
| 13    | DC_LOOP_SNS_SEL    | DC loop feedback selector.<br>0: VFB<br>1: VDIFF                                                                                                                                                                                      |
| 12    | DC_LOOP_REF_SEL    | DC loop reference accuracy selector.<br>0: with 2-bit fraction<br>1: without 2-bit fraction                                                                                                                                           |
| 11    | VDIFF_GAIN_SEL     | Gain selector for the remote sense amplifier.<br>0: unity gain. VOUT is limited to 1.6V. The DC loop regulation has 1.5625mV resolution.<br>1: half gain. VOUT can be set to 3.19375V. The DC loop regulation has 3.125mV resolution. |
| 10:9  | DIFF_FB_SENSE_GAIN | ADC sensing gain selector for VDIFF and VFB.<br>00: half gain<br>01: unity gain<br>10: three-quarter gain<br>11: invalid<br><br>When VDIFF_GAIN_SEL = 1, the DIFF_FB_SENSE_GAIN is forced to half the gain of the inner MP2888A.      |
| 8:0   | VOUT_SCALE         | Calculated scale factor consistent with the gain of the external output voltage divider. $VOUT\_SCALE = 32 \times V_{OUT}/V_{OUT\_SENSE}$ .                                                                                           |



This register sets an additional offset on the droop current.

| Bits | Bit Name      | Description                                                                                                        |
|------|---------------|--------------------------------------------------------------------------------------------------------------------|
| 7:6  | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                                                  |
| 5:0  | IDROOP_OFFSET | User offset on droop current. 0.81μA/LSB. This value is in two's complement binary format. Bit[5] is the sign bit. |

This register sets the output voltage OVP2 and UVP2 level.

|          |              |     |     |     |     |     |     |     |     |     |     |     |     |     |     |            |
|----------|--------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------------|
| Command  | MFR_OVUV_SEL |     |     |     |     |     |     |     |     |     |     |     |     |     |     |            |
| Format   | binary       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |            |
| Bit      | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0          |
| Access   | r/w          | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w        |
| Function | x            | x   | x   | x   | x   | x   | x   |     |     |     | 1   |     |     |     | 1   | OVUV_LEVEL |

| Bits | Bit Name         | Description                                                                                                                                                                                                                                                                                                                                                                    |
|------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED         | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                              |
| 8:7  | TRIM_UVP2_OFFSET | Trimming value of UVP2 offset. Factory settings. Do not change.                                                                                                                                                                                                                                                                                                                |
| 6    | RESERVED         | Fixed to 1.                                                                                                                                                                                                                                                                                                                                                                    |
| 5:4  | TRIM_OVP2_OFFSET | Trimming value of OVP2 offset. Factory settings. Do not change.                                                                                                                                                                                                                                                                                                                |
| 3    | RESERVED         | Fixed to 1.                                                                                                                                                                                                                                                                                                                                                                    |
| 2:0  | OVUV_LEVEL       | <p>OVP2 and UVP level.</p> <p>001: 140mV<br/>010: 220mV<br/>100: 300mV<br/>others: invalid</p> <p>If the remote sense amplifier sets the unity gain, then the OVP2 level is VREF + OVUV_LEVEL. The UVP level is VREF - OVUV_LEVEL.<br/>If the remote sense amplifier sets the half gain, then the OVP2 level is VREF + OVUV_LEVEL×2. The UVP level is VREF - OVUV_LEVEL×2.</p> |

### MFR\_RSAMP\_OFFSET (2Dh)

This register is used to apply an offset to the remote sense amplifier. This is used to fine-tune the output voltage offset.

| Command  | MFR_RSAMP_OFFSET |              |     |     |     |     |     |     |
|----------|------------------|--------------|-----|-----|-----|-----|-----|-----|
| Format   | Signed binary    |              |     |     |     |     |     |     |
| Bit      | 7                | 6            | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w          | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | RSAMP_OFFSET |     |     |     |     |     |     |

| Bits | Bit Name     | Description                                                                                                                                                                                                                                                                                     |
|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | RESERVED     | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                               |
| 6:0  | RSAMP_OFFSET | <p>Offset on the remote sense amplifier. This value is in two's complement binary format. Bit[6] is the sign bit.</p> <p>If the remote sense amplifier sets the unity gain, the resolution is 0.5mV/LSB.<br/>If the remote sense amplifier sets the half gain, the resolution is 0.8mV/LSB.</p> |

### MFR\_VFB\_DIGI\_GAIN (2Eh)

This register sets a digital gain to fine-tune the VFB sense value for the DC loop.

| Command  | MFR_VFB_DIGI_GAIN |     |     |     |     |               |     |     |     |     |     |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary   |     |     |     |     |               |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11  | 10            | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w               | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                 | x   | x   | x   | x   | VFB_DIGI_GAIN |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name      | Description                                                                                                                                                                                                                 |
|-------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                           |
| 10:0  | VFB_DIGI_GAIN | <p>Multiplies the VFB ADC sense value by the digital gain. The result is used for the DC loop. Default value is 1024 for the unity gain.</p> <p><math>VFB\_SENSE\_FINAL = VFB\_ADC \times VFB\_DIGI\_GAIN / 1024</math></p> |

**MFR\_IMON\_DIGI\_GAIN (2Fh)**

This register sets a digital gain used to fine-tune the IMON sense value for the output current report.

| Command  | MFR_IMON_DIGI_GAIN |     |     |     |     |                |     |     |     |     |     |     |     |     |     |     |
|----------|--------------------|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary    |     |     |     |     |                |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                 | 14  | 13  | 12  | 11  | 10             | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                  | x   | x   | x   | x   | IMON_DIGI_GAIN |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name       | Description                                                                                                                                                                                                  |
|-------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                            |
| 10:0  | IMON_DIGI_GAIN | Multiplies the IMON ADC sense value by the digital gain. The result is used for output current reporting. Default value is 1024 for the unity gain.<br><br>IMON_SENSE_FINAL = IMON_ADC x IMON_DIGI_GAIN/1024 |

**MFR\_DC\_LOOP\_CTRL (30h)**

This register sets the output voltage DC loop performance and sets the power mode when adding phases during the transient.

| Command  | MFR_DC_LOOP_CTRL |     |                    |     |     |     |     |     |     |     |     |     |                   |     |     |     |
|----------|------------------|-----|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------------------|-----|-----|-----|
| Format   | Unsigned binary  |     |                    |     |     |     |     |     |     |     |     |     |                   |     |     |     |
| Bit      | 15               | 14  | 13                 | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3                 | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w               | r/w | r/w | r/w |
| Function |                  |     | PWM_PRD_ERROR_THRE |     |     |     |     |     |     |     |     |     | DC_LOOP_HOLD_TIME |     |     |     |

| Bits | Bit Name             | Description                                                                                                                                                                                                                                                                                                                                        |
|------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FREQ_ADD_PHASE_MODE  | Mode selector for adding phases due to the PWM frequency increasing. When the controller runs in auto-phase shedding mode, if it detects that the PWM frequency has risen higher than the setting limit due to the load increasing, it enters full-phase CCM.<br><br>0: idle PWMs switch from Hi-Z to low<br>1: idle PWMs switch from Hi-Z to high |
| 14   | UV_ADD_PHASE_MODE    | Mode selector for adding phases due to VFB dropping. When the controller runs in auto-phase-shedding mode, if it detects that VFB has dropped below VO_REF - 25mV due to the load increasing, it enters full-phase CCM.<br><br>0: idle PWMs switch from Hi-Z to low<br>1: idle PWMs switch from Hi-Z to high                                       |
| 13:7 | PWM_PRD_ERROR_THRE   | PWM period error threshold for holding the DC loop and current balance loop. When the actual PWM period has a deviation from the configured period, either the positive or negative deviation exceeds this threshold. The DC loop and current balance loop are held. 80ns/LSB.                                                                     |
| 6    | PRD_HOLD_DC_EN       | Enable bit for holding the DC loop for a certain amount of time when the error of the PWM period exceeds the threshold PWM_PRD_ERROR_THRE.<br><br>0: disable<br>1: enable<br><br>This function needs another condition. See MFR_PWM_LIMIT (3Fh) bit[10:7].                                                                                         |
| 5    | PHASE_CNT_HOLD_DC_EN | Enable bit for holding the DC loop for a certain amount of time when the phase-count changes.<br><br>0: disable<br>1: enable                                                                                                                                                                                                                       |

|     |                   |                                                                                                                                                           |
|-----|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | VFB_HOLD_DC_EN    | Enable bit for holding the DC loop for a certain amount of time when VFB exceeds the VO_REF - 25mV or VO_REF + 20mV threshold.<br>0: disable<br>1: enable |
| 3:0 | DC_LOOP_HOLD_TIME | DC loop holding time. 100µs/LSB.                                                                                                                          |

**MFR\_CB\_LOOP\_CTRL (31h)**

This register sets the current balance (CB) loop performance.

| Command  | MFR_CB_LOOP_CTRL     |     |                                                                                                                                                                       |     |                   |     |     |     |
|----------|----------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------|-----|-----|-----|
| Format   | Unsigned binary      |     |                                                                                                                                                                       |     |                   |     |     |     |
| Bit      | 7                    | 6   | 5                                                                                                                                                                     | 4   | 3                 | 2   | 1   | 0   |
| Access   | r/w                  | r/w | r/w                                                                                                                                                                   | r/w | r/w               | r/w | r/w | r/w |
| Function |                      |     |                                                                                                                                                                       |     | CB_LOOP_HOLD_TIME |     |     |     |
| Bits     | Bit Name             |     | Description                                                                                                                                                           |     |                   |     |     |     |
| 7        | VFB_HOLD_CB_EN       |     | Enable bit for holding the CB loop for a certain amount of time when VFB exceeds the VO_REF - 25mV or VO_REF + 20mV threshold.<br>0: disable<br>1: enable             |     |                   |     |     |     |
| 6        | PRD_HOLD_CB_EN       |     | Enable bit for holding the CB loop for a certain amount of time when the error of the PWM period exceeds the threshold PWM_PRD_ERROR_THRE.<br>0: disable<br>1: enable |     |                   |     |     |     |
| 5        | PHASE_CNT_HOLD_CB_EN |     | Enable bit for holding the CB loop for a certain amount of time when the phase count changes.<br>0: disable<br>1: enable                                              |     |                   |     |     |     |
| 4        | DVID_HOLD_CB_EN      |     | Enable bit for holding the CB loop for a certain amount of time during DVID.<br>0: disable<br>1: enable                                                               |     |                   |     |     |     |
| 3:0      | CB_LOOP_HOLD_TIME    |     | Current balance loop holding time. 100µs/LSB.                                                                                                                         |     |                   |     |     |     |

**MFR\_FS\_LOOP\_CTRL (32h)**

This register is used for PWM frequency loop setting.

| Command  | MFR_FS_LOOP_CTRL |     |     |     |                   |     |     |     |     |            |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-------------------|-----|-----|-----|-----|------------|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |                   |     |     |     |     |            |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11                | 10  | 9   | 8   | 7   | 6          | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w               | r/w | r/w | r/w | r/w | r/w        | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                |     |     |     | FS_LOOP_HOLD_TIME |     |     |     |     | FS_LOOP_KI |     |     |     |     |     |     |

| Bits | Bit Name       | Description                                                                                                                                                      |
|------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                                                                                                |
| 14   | VFB_HOLD_FS_EN | Enable bit for holding the frequency loop for a certain amount of time when VFB exceeds the VO_REF - 25mV or VO_REF + 20mV threshold.<br>0: disable<br>1: enable |

|      |                      |                                                                                                                                 |
|------|----------------------|---------------------------------------------------------------------------------------------------------------------------------|
| 13   | PHASE_CNT_HOLD_FS_EN | Enable bit for holding the frequency loop for a certain amount of time when the phase count changes.<br>0: disable<br>1: enable |
| 12   | DVID_HOLD_FS_EN      | Enable bit for holding the frequency loop for a certain amount of time during DVID.<br>0: disable<br>1: enable                  |
| 11:8 | FS_LOOP_HOLD_TIME    | Frequency loop holding time. 100µs/LSB.                                                                                         |
| 7    | FS_LOOP_EN           | Enable bit for the PWM frequency loop.<br>0: disable<br>1: enable                                                               |
| 6:0  | FS_LOOP_KI           | PWM frequency loop integral parameter.                                                                                          |

**MFR\_T\_ALERT\_CTRL (34h)**

This register sets the thermal alert pin (TALERT#) behavior.

| Command  | MFR_T_ALERT_CTRL |     |             |     |                                                                                                                                                           |     |     |     |                 |     |     |     |     |     |     |     |
|----------|------------------|-----|-------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |             |     |                                                                                                                                                           |     |     |     |                 |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13          | 12  | 11                                                                                                                                                        | 10  | 9   | 8   | 7               | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w         | r/w | r/w                                                                                                                                                       | r/w | r/w | r/w | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | T_ALT_DELAY |     |                                                                                                                                                           |     |     |     | TSNS_T_ALT_THRE |     |     |     |     |     |     |     |
| Bits     | Bit Name         |     |             |     | Description                                                                                                                                               |     |     |     |                 |     |     |     |     |     |     |     |
| 15:14    | RESERVED         |     |             |     | Unused. X indicates that writes are ignored and always read as 0.                                                                                         |     |     |     |                 |     |     |     |     |     |     |     |
| 13:11    | T_ALT_CHECK      |     |             |     | Trigger delay time for pulling TALERT# low. 100µs/LSB.                                                                                                    |     |     |     |                 |     |     |     |     |     |     |     |
| 10       | TSNS_CURRENT_DIS |     |             |     | Enable bit for sourcing a 10µA constant current from TSNS to the thermistor to generate a voltage for the temperature sensing.<br>0: enable<br>1: disable |     |     |     |                 |     |     |     |     |     |     |     |
| 9        | TSNS_T_ALT_EN    |     |             |     | Enable bit for pulling TALERT# low when the controller detects an over-temperature warning from TSNS.<br>0: disable<br>1: enable                          |     |     |     |                 |     |     |     |     |     |     |     |
| 8        | TEMP_T_ALT_EN    |     |             |     | Enable bit for pulling TALERT# low when the controller detects an over-temperature warning from VTEMP.<br>0: disable<br>1: enable                         |     |     |     |                 |     |     |     |     |     |     |     |
| 7:0      | TSNS_T_ALT_THRE  |     |             |     | Digital threshold of the over-temperature warning from TSNS.<br>TSNS_T_ALT_THRE = R <sub>t</sub> x 10µA x 256 / 1.6V                                      |     |     |     |                 |     |     |     |     |     |     |     |

### VIN\_ON (35h)

This register sets the input voltage UVLO rising threshold. When the input voltage rises higher than VIN\_ON, the MP2888A soft starts to the boot voltage with a programmed slew rate.

| Command  | VIN_ON                          |     |     |     |     |     |     |     |          |     |     |     |     |     |     |     |
|----------|---------------------------------|-----|-----|-----|-----|-----|-----|-----|----------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Linear, two's complement binary |     |     |     |     |     |     |     |          |     |     |     |     |     |     |     |
| Bit      | 15                              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7        | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent                        |     |     |     |     | x   |     |     | Mantissa |     |     |     |     |     |     |     |

| Bits  | Bit Name | Description                                                                                                          |
|-------|----------|----------------------------------------------------------------------------------------------------------------------|
| 15:11 | Exponent | This value is two's complement binary format and fixed to 11101.<br>Exponent = -3 (fixed)                            |
| 10:8  | Reserved | Unused. X indicates that writes are ignored and always read as 0.                                                    |
| 7:0   | Mantissa | Input voltage UVLO rising threshold. 0.125V/LSB.<br>$VIN\_ON = Mantissa \times 2^{exponent} = Mantissa \times 0.125$ |

### VIN\_OFF (36h)

This register sets the input voltage UVLO falling threshold. When the input voltage falls below VIN\_OFF, all PWMs enter tri-state mode, and the VR shuts down.

| Command  | VIN_OFF                         |     |     |     |     |     |     |     |          |     |     |     |     |     |     |     |
|----------|---------------------------------|-----|-----|-----|-----|-----|-----|-----|----------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Linear, two's complement binary |     |     |     |     |     |     |     |          |     |     |     |     |     |     |     |
| Bit      | 15                              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7        | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent                        |     |     |     |     | x   |     |     | Mantissa |     |     |     |     |     |     |     |

| Bits  | Bit Name | Description                                                                                                            |
|-------|----------|------------------------------------------------------------------------------------------------------------------------|
| 15:11 | Exponent | This value is two's complement binary format and fixed to 11101.<br>Exponent = -3 (fixed)                              |
| 10:8  | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                                                      |
| 7:0   | Mantissa | Input voltage UVLO falling threshold. 0.125V/LSB.<br>$VIN\_OFF = Mantissa \times 2^{exponent} = Mantissa \times 0.125$ |

### IOUT\_CAL\_GAIN (38h)

This register sets the gain for the total current report in the READ\_IOUT register. This is the ratio of the IMON voltage to the total output current. This is related to the DrMOS current sense gain (Kcs) and IMON current sense resistor (R<sub>IMON</sub>).

| Command  | IOUT_CAL_GAIN                   |     |     |     |     |          |     |     |     |     |     |     |     |     |     |     |
|----------|---------------------------------|-----|-----|-----|-----|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Linear, two's complement binary |     |     |     |     |          |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                              | 14  | 13  | 12  | 11  | 10       | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                             | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent                        |     |     |     |     | Mantissa |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | Exponent | This value is two's complement binary format.<br>10001: exponent = -15<br>10010: exponent = -14<br>10011: exponent = -13<br>others: invalid                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 10:0  | Mantissa | $\text{Mantissa} = \frac{V_{\text{IMON}}}{I_{\text{OUT}}} \times 2^{-\text{exponent}} = \frac{K_{\text{CS}} \times R_{\text{IMON}}}{16000} \times 2^{-\text{exponent}}$ <p>Where <math>V_{\text{IMON}}</math> is the voltage of IMON, <math>I_{\text{OUT}}</math> is the total output current, <math>R_{\text{IMON}}</math> is the resistor connected from IMON to ground (in kΩ), and <math>K_{\text{CS}}</math> is the current sense gain of the DrMOS (in μA/A).</p> <p>When <math>R_{\text{IMON}}</math> is too big for Mantissa &lt; 2<sup>11</sup>, increase the exponent. This usually meets small load-current applications.</p> <p>If TOTAL_CURRENT_RESOLUTION (44h) = 1, then IOUT_CAL_GAIN must be doubled.</p> |

### IOUT\_CAL\_OFFSET (39h)

This register is used to set the offset for the total current report in READ\_IOUT.

| Command  | IOUT_CAL_OFFSET                 |     |     |     |     |     |     |     |     |          |     |     |     |     |     |     |
|----------|---------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|----------|-----|-----|-----|-----|-----|-----|
| Format   | Linear, two's complement binary |     |     |     |     |     |     |     |     |          |     |     |     |     |     |     |
| Bit      | 15                              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6        | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent                        |     |     |     |     |     | x   |     |     | Mantissa |     |     |     |     |     |     |

| Bits  | Bit Name | Description                                                                                                                                                                                                                                                                       |
|-------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | Exponent | This value is in two's complement binary format (fixed at 111100).<br>Exponent = -2 (fixed)                                                                                                                                                                                       |
| 9:7   | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                 |
| 6:0   | Mantissa | $\text{IOUT\_CAL\_OFFSET} = \text{Mantissa} \times 2^{\text{exponent}} = \text{Mantissa} \times 0.25$ <p>0.25A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br/>0.5A/LSB (TOTAL_CURRENT_RESOLUTION = 1)</p> <p>This value is in two's complement binary format. Bit[6] is the sign bit.</p> |

### MFR\_PROTECT\_DIS (3Ah)

This register is used for protection selection.

| Command  | MFR_PROTECT_DIS |     |     |     |     |     |     |     |     |     |     |     |          |     |         |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------|-----|---------|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |          |     |         |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3        | 2   | 1       | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w      | r/w | r/w     | r/w |
| Function | x               | x   | x   | x   | x   |     |     |     |     |     |     |     | OVP1_DIS |     | OTP_DIS |     |

| Bits  | Bit Name             | Description                                                                                                                                                                                 |
|-------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED             | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                           |
| 10    | PWM_CHK_FAULT_EN     | Enable bit for ADC sampling of the Intelli-Phase PWM once a protection occurs.<br>In this process, all PWM outputs stay in Hi-Z status.<br>0: disable<br>1: enable                          |
| 9     | CS_FAULT_EN          | Enable bit for CSx fault protection from CS. Voltage on any CS pin falling below 0.3V can trigger CSx fault protection, and the controller latches.<br>0: disable<br>1: enable              |
| 8     | TEMP_FAULT_EN        | Enable bit for VTEMP fault protection from VTEMP. Voltage on VTEMP exceeding a certain threshold can trigger VTEMP fault protection, and the controller latches.<br>0: disable<br>1: enable |
| 7     | TEMP_FAULT_BLOCK_OTP | Enable bit for blocking OTP when a VTEMP fault protection is triggered.<br>0: enable<br>1: disable                                                                                          |
| 6     | DVID_BLOCK_OVP1      | Enable bit for blocking the output voltage OVP1 during DVID.<br>0: disable<br>1: enable                                                                                                     |
| 5:4   | VIN_PROTECT_DIS      | Enable bits for the input voltage UVLO and OVP.<br>11: disable<br>others: enable                                                                                                            |
| 3:2   | OVP1_DIS             | Enable bits for the output voltage OVP1.<br>01: disable<br>others: enable                                                                                                                   |
| 1:0   | OTP_DIS              | Enable bits for OTP from VTEMP.<br>01: disable<br>others: enable                                                                                                                            |

### MFR\_PS\_FORCE (3Bh)

This register is used to set advanced functions of the controller, such as forced power state, and related parameters.

| Command  | MFR_PS_FORCE    |     |     |     |     |     |     |     |     |     |     |                 |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----------------|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |                 |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4               | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w             | r/w | r/w | r/w | r/w |
| Function |                 |     | x   |     |     | x   | x   |     | x   | x   |     | TRI_STATE_DELAY |     |     |     |     |

| Bits | Bit Name        | Description                                                                                                                                                   |
|------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | PSI_CONTROL     | 0: jump to full-phase during soft start and DVID, even if PSI is low<br>1: follow PSI to reach the target phase-count during soft start and DVID              |
| 14   | PWM_TRI_MODE    | PWM tri-state mode selector.<br>0: Hi-Z<br>1: force 1.5V middle voltage                                                                                       |
| 13   | RESERVED        | Unused. X indicates that writes are ignored and always read as 0.                                                                                             |
| 12   | VIN_MUX_SEL     | V <sub>IN</sub> value mode selector for T <sub>ON</sub> calculation.<br>0: real-time V <sub>IN</sub><br>1: latched V <sub>IN</sub>                            |
| 11   | PROTECT_ALL_DIS | Master enable bit for all protections.<br>0: enable protection<br>1: disable all protection                                                                   |
| 10:9 | RESERVED        | Unused. X indicates that writes are ignored and always read as 2'b11.                                                                                         |
| 8    | VIN2TON_EN      | Enable bit for updating T <sub>ON</sub> when V <sub>IN</sub> varies or moves away from the previous latched V <sub>IN</sub> value.<br>0: disable<br>1: enable |
| 7    | DLL_EN          | Enable bit of DLL. DLL can increase the PWM resolution to 0.625ns/LSB.<br>0: disable<br>1: enable                                                             |
| 6    | RESERVED        | Unused. X indicates that writes are ignored and always read as 2'b01.                                                                                         |
| 5    | IOUT_FILTER_SET | Output current reporting mode selector.<br>0: average I <sub>OUT</sub> report<br>1: real-time I <sub>OUT</sub> report                                         |
| 4:0  | TRI_STATE_DELAY | PWM low-time inserted between PWM high and tri-state when the PWM logic changes from high-state to middle-state. 5ns/LSB.                                     |

### MFR\_SLOPE\_ADV (3Dh)

This register is used for advanced slope compensation setting.

| Command  | MFR_SLOPE_ADV   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name              | Description                                                                                                                                                                                                                                                                                                                                                        |
|-------|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED              | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                  |
| 14    | SS_PHASE_CUR_LIMIT_EN | Enable bit of the per-phase valley current limit during soft start.                                                                                                                                                                                                                                                                                                |
| 13:12 | OC_SKIP_PHASE_TIME    | Trigger delay time for phase skipping when a certain phase triggers the phase current limit. 20ns/LSB with 15ns offset.<br><br>When a certain phase's current is above the phase current limit, its PWM high logic is delayed until the current drops below the limitation. If the delay time is reached, this phase's PWM high logic is passed to the next phase. |

|      |                     |                                                                                                                                                                                                                                                                                                    |
|------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11   | INI_SLOPE_EN        | <p>Enable bit of the initial slope compensation before the first PWM during soft start.</p> <p>0: disable<br/>1: enable</p> <p>If enabled, the initial slope slew rate is set via INI_SLOPE_CURRENT.</p>                                                                                           |
| 10:5 | INI_SLOPE_CURRENT   | <p>Current source value for initial slope compensation before the first PWM during soft start. 0.25µA/LSB.</p> $V_{\text{SLOPE@INI}} = \frac{\text{INI\_SLOPE\_CURRENT}}{16 \times 1.85(\text{pF})} \times T_{\text{charge}}(\text{us})$ <p>The maximum charging time is 0.4µs.</p>                |
| 4    | SLOPE_BLANK_SEL     | <p>Slope compensation blank time selector.</p> <p>0: use the calculated T<sub>ON</sub><br/>1: use register SLOPE_BLANK_TIME</p> <p>The blank time starts when the PWM rises high. During the blank time, the slope compensation capacitor is discharged.</p>                                       |
| 3    | PRE_BIAS_MODE       | <p>Mode selector for idle PWMs to exit tri-state during phase-adding.</p> <p>0: idle PWMs rise high from tri-state when their own high logic comes<br/>1: all idle PWMs drop low from tri-state when the first high logic of any phase comes. This high logic phase's PWM rises high directly.</p> |
| 2    | EXIT_DCM_SLOPE_MODE | <p>Mode selector of the first CCM compensating slope when the controller exits DCM.</p> <p>0: first CCM slope rises on the base of the DCM slope voltage<br/>1: first CCM slope rises after clearing the DCM slope voltage</p>                                                                     |
| 1    | DCM_SLOPE_CLAMP     | <p>Enable bit of the 60mV maximum limit for DCM slope compensation.</p> <p>0: disable<br/>1: enable</p>                                                                                                                                                                                            |
| 0    | SLOPE_SWITCH_OFF_EN | <p>Enable bit for turning off the low leakage switch when the slope compensation current source turns off. The low leakage switch is in series with the capacitor and current source of slope compensation.</p> <p>0: disable<br/>1: enable</p>                                                    |

### MFR\_PWM\_LIMIT (3Fh)

This register sets the PWM minimum on-time and minimum off-time.

| Command  | MFR_PWM_LIMIT   |     |     |     |     |               |     |     |     |             |     |     |              |     |     |     |
|----------|-----------------|-----|-----|-----|-----|---------------|-----|-----|-----|-------------|-----|-----|--------------|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |               |     |     |     |             |     |     |              |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10            | 9   | 8   | 7   | 6           | 5   | 4   | 3            | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w         | r/w | r/w | r/w          | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | ON_TIME_LIMIT |     |     |     | MIN_ON_TIME |     |     | MIN_OFF_TIME |     |     |     |

| Bits  | Bit Name      | Description                                                                                                                                                                                                                                                                                                                    |
|-------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                              |
| 10:7  | ON_TIME_LIMIT | PWM on-time threshold for the DC loop hold function. This is another condition for the function of holding the DC loop via an error of the PWM period. If the calculated T <sub>ON</sub> is less than this threshold, the DC loop cannot be held via the PWM period, even if bit[6] of MFR_DC_LOOP_CTRL (30h) is set. 5ns/LSB. |
| 6:4   | MIN_ON_TIME   | PWM minimum on-time. 5ns/LSB.                                                                                                                                                                                                                                                                                                  |
| 3:0   | MIN_OFF_TIME  | PWM minimum off-time. 20ns/LSB with 15ns offset.                                                                                                                                                                                                                                                                               |

### MFR\_OSR\_SET (40h)

This register sets the minimum PWM off-time and block time of the OSR function.

| Command  | MFR_OSR_SET     |     |                   |     |     |     |     |     |                |     |     |     |     |     |     |     |
|----------|-----------------|-----|-------------------|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |                   |     |     |     |     |     |                |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13                | 12  | 11  | 10  | 9   | 8   | 7              | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w               | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | OSR_DEGLITCH_TIME |     |     |     |     |     | OSR_BLOCK_TIME |     |     |     |     |     |     |     |

| Bits  | Bit Name          | Description                                                       |
|-------|-------------------|-------------------------------------------------------------------|
| 15:14 | RESERVED          | Unused. X indicates that writes are ignored and always read as 0. |
| 13:8  | OSR_DEGLITCH_TIME | Minimum PWM off-time in the OSR process. 5ns/LSB.                 |
| 7:0   | OSR_BLOCK_TIME    | Block time between two OSR events. 5ns/LSB.                       |

### MFR\_T\_ALERT\_CTRL2 (43h)

This register sets thermal alert pin (TALERT#) behavior.

| Command  | MFR_T_ALERT_CTRL2 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w               | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                 | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name            | Description                                                                                                                                         |
|------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED            | Unused. X indicates that writes are ignored and always read as 0.                                                                                   |
| 8    | TSNS_RES_SEL        | Type selection bit of TSNS thermistor.<br>0: PTC<br>1: NTC                                                                                          |
| 7:4  | TSNS_T_ALT_DST_THRE | Digital threshold of the over-temperature warning de-assertion from TSNS.<br>$TSNS\_T\_ALT\_DST\_THRE = R_{t\_dst} \times 10\mu A \times 16 / 1.6V$ |
| 3:0  | OT_WARN_DST_THRE    | Digital threshold of the over-temperature warning deassertion from VTEMP.<br>16°C/LSB.                                                              |

### MFR\_SYS\_CONFIG (44h)

This register sets the system configuration.

| Command  | MFR_SYS_CONFIG  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |                 |     |     |     |     |     |     |     |     |     | x   |     |     |     |     |     |

| Bits  | Bit Name                 | Description                                                                                                                                                                                         |
|-------|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | DGTL_UVP_LEVEL           | Threshold of digital Vo_UVP. 32mV/LSB                                                                                                                                                               |
| 11    | DGTL_UVP_EN              | Enable bit of digital Vo_UVP.<br>0: disable<br>1: enable                                                                                                                                            |
| 10    | OC_BLK_UVP_EN            | Enable bit for blocking analog Vo_UVP when any phase's current reaches the per-phase-valley-current limit (the internal OC signal rises high).<br>1: block<br>0: do not block                       |
| 9     | ANA_UVP_DIS              | Enable bit of analog Vo_UVP.<br>1: disable<br>0: enable                                                                                                                                             |
| 8:7   | OC_DGLTCH_FOR_DGTL_UVP   | Deglintch time of the internal OC signal which is boolean and with a digital UV signal to trigger digital Vo_UVP.<br>00: 800ns<br>01: 1000ns<br>10: 1200ns<br>11: force the internal OC signal high |
| 6     | AC_LL_ACTIVATE_MODE      | AC droop loop activation mode.<br>1: activate AC Droop loop when soft-start begins.<br>0: activate AC Droop loop once the controller finishes POR.                                                  |
| 5     | RESERVED                 | Unused. X indicates that writes are ignored and reads are always 0.                                                                                                                                 |
| 4     | PHASE_CURRENT_RESOLUTION | Resolution selector for per-phase current report and protection.<br>0: original resolution<br>1: half resolution (double range)                                                                     |
| 3     | TOTAL_CURRENT_RESOLUTION | Resolution selector for total current report, protection, warning, and auto-phase shedding (APS) levels.<br>0: original resolution<br>1: half resolution (double range)                             |
| 2:0   | DRMOS_CS_TYPE            | DrMOS current sense gain indicator for GUI.<br>000: CS gain is 8.5μA/A<br>001: CS gain is 9.7μA/A<br>010: CS gain is 10μA/A<br>011: CS gain is 5μA/A<br>others: reserved                            |

### MFR\_VR\_CONFIG3 (45h)

This register selects the main functions of the controller.

| Command  | MFR_VR_CONFIG3  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | 0               | 0   | 0   |     | 1   |     |     |     |     |     |     | 1   |     |     |     | 0   |

| Bits | Bit Name        | Description                                                       |
|------|-----------------|-------------------------------------------------------------------|
| 15   | RESERVED        | Unused. X indicates that writes are ignored and always read as 0. |
| 14   | TEMP_FAULT_MODE | Mode selector of VTEMP_FAULT.<br>0: hiccup<br>1: latch            |

| 13     | APS_ACTIVATE_MODE    | <p>APS activation mode after soft start when PSI is in mid-state.</p> <p>1: activate APS when soft start has finished and PWM-VID signal starts switching (exiting Hi-Z state for the first time)</p> <p>0: activate APS when soft start finishes, regardless of PWM-VID signal</p>                                                                                                                                                                                                                                   |        |     |  |      |          |              |      |                      |                                       |     |          |              |
|--------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|--|------|----------|--------------|------|----------------------|---------------------------------------|-----|----------|--------------|
| 12     | PHASE_CNT_SET_MODE   | <p>Phase-count setting mode.</p> <p>0: phase count set by bit[3:0] of MFR_VR_CONFIG1 (E1h)</p> <p>1: phase count set by external CSx pin. CSx pins of unused phases should be shorted to GND in this mode. The controller only detects CSx pins during the first POR. Short the CS of certain phases to GND to block all higher-number phases.</p>                                                                                                                                                                    |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| 11     | PARAM_VOUT_MIN_MSB   | <p>Highest bit of parameter PARAM_VOUT_MIN.</p> <p>Parameter PARAM_VOUT_MIN_16LSB is described in register MFR_PARAM_VOUT_MIN (B4h).</p>                                                                                                                                                                                                                                                                                                                                                                              |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| 10     | MFR_CB_SS_EN         | <p>Enable bit for not holding the CB loop during soft start.</p> <p>0: disable</p> <p>1: enable</p>                                                                                                                                                                                                                                                                                                                                                                                                                   |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| 9      | CB_LARGE_PI_EN       | <p>Enable bit for variable parameter control of CB loop.</p> <p>0: disable. The PI parameter of the CB loop is always at a constant value.</p> <p>1: enable. When the voltage error between CSx and CS1 is more than 50mV, a large PI parameter is adopted in the CB loop to make the regulation process faster. The large PI parameter is decided by bit[8:6] of MFR_VR_CONFIG3 (45h).</p>                                                                                                                           |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| 8:6    | MFR_CB_LARGE_PI      | <p>Large PI parameter of the CB loop for variable parameter control.</p> <p>Internal PI parameter = MFR_CB_LARGE_PI * 32 + 31</p>                                                                                                                                                                                                                                                                                                                                                                                     |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| 5      | PWMVID_3_LEVEL_EN    | <p>Enable bit for 3-level VID control by the PWMVID pin in PMBus mode.</p> <p>0: disable</p> <p>1: enable</p> <p>Relationship between the PWMVID pin state and VID:</p> <table border="1"> <thead> <tr> <th>PWMVID</th><th colspan="2">VID</th></tr> </thead> <tbody> <tr> <td>High</td><td>VOUT_MAX</td><td>Register 24h</td></tr> <tr> <td>Hi-Z</td><td>VOUT_COMMAND / Vboot</td><td>Register 21h / Determined by BOOT pin</td></tr> <tr> <td>Low</td><td>VOUT_MIN</td><td>Register 1Fh</td></tr> </tbody> </table> | PWMVID | VID |  | High | VOUT_MAX | Register 24h | Hi-Z | VOUT_COMMAND / Vboot | Register 21h / Determined by BOOT pin | Low | VOUT_MIN | Register 1Fh |
| PWMVID | VID                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| High   | VOUT_MAX             | Register 24h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| Hi-Z   | VOUT_COMMAND / Vboot | Register 21h / Determined by BOOT pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| Low    | VOUT_MIN             | Register 1Fh                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| 4      | TON_CLAMP_EN         | <p>Enable bit for clamping the PWM on-time to avoid a negative overflow.</p> <p>0: disable. PWM on-time range must be designed within 90ns to 1120ns. If on-time is less than 90ns, it has risk of negative overflow.</p> <p>1: enable. PWM on-time can be clamped to MIN_ON_TIME(3Fh bit[6:4]). On-time design range is from MIN_ON_TIME to 1120ns.</p>                                                                                                                                                              |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| 3      | VTEMP_OFFSET_SIGNED  | <p>Sign bit of parameter VTEMP_OFFSET.</p> <p>The definition of the parameter VTEMP_OFFSET is described in register MFR_TEMP_GAIN_OFFSET (C1h).</p>                                                                                                                                                                                                                                                                                                                                                                   |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| 2      | PMBUS_VBOOT_SEL      | <p>The V<sub>BOOT</sub> control mode selection in PMBus mode.</p> <p>0: V<sub>BOOT</sub> is determined by the value of VOUT_COMMAND (21h)</p> <p>1: V<sub>BOOT</sub> is determined by the voltage of TSNS/BOOT. After the soft start, the real-time VID can be updated by register VOUT_COMMAND (21h).</p>                                                                                                                                                                                                            |        |     |  |      |          |              |      |                      |                                       |     |          |              |
| 1:0    | PIN_VBOOT_TABLE_SEL  | <p>Pin-strap V<sub>BOOT</sub> table selector.</p> <p>00: V<sub>BOOT</sub> table is 0.1V/step, up to 1.5V</p> <p>01: V<sub>BOOT</sub> table is 0.05V/step, up to 1.55V</p> <p>10: V<sub>BOOT</sub> table is 0.2V/step, up to 3.0V</p> <p>11: V<sub>BOOT</sub> table is 0.1V/step, up to 3.1V</p> <p>Refer to Table 1a and Table 1b for detail.</p>                                                                                                                                                                     |        |     |  |      |          |              |      |                      |                                       |     |          |              |

**CONFIG\_ID (46h)**

This register is the identification code for different applications.

| Command  | CONFIG_ID       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |                 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name  | Description                                                                               |
|------|-----------|-------------------------------------------------------------------------------------------|
| 15:0 | CONFIG_ID | Identification code for different applications. This is part of MPS product part numbers. |

**CONFIG\_REV\_MPS (47h)**

This register saves the revision number to indicate different configurations.

| Command  | CONFIG_REV_MPS  |     |     |     |             |     |     |     |              |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-------------|-----|-----|-----|--------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |             |     |     |     |              |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11          | 10  | 9   | 8   | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w         | r/w | r/w | r/w | r/w          | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | APPLICATION_REV |     |     |     | SILICON_REV |     |     |     | FIRMWARE_REV |     |     |     |     |     |     |     |

| Bits  | Bit Name        | Description                                                                         |
|-------|-----------------|-------------------------------------------------------------------------------------|
| 15:12 | APPLICATION_REV | Application version. "E" is for engineering version, "0" is for production version. |
| 11:8  | SILICON_REV     | Silicon version. "0" indicates R0, "1" indicates R1, and so on.                     |
| 7:0   | FIRMWARE_REV    | Revision number indicates different firmware configurations.                        |

**IOUT\_OC\_WARN\_LIMIT (4Ah)**

This register sets the output current OC warning threshold.

| Command  | IOUT_OC_WARN_LIMIT |     |     |     |     |     |                    |     |     |     |     |     |     |     |     |     |
|----------|--------------------|-----|-----|-----|-----|-----|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary    |     |     |     |     |     |                    |     |     |     |     |     |     |     |     |     |
| Bit      | 15                 | 14  | 13  | 12  | 11  | 10  | 9                  | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                | r/w | r/w | r/w | r/w | r/w | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                  | x   | x   | x   | x   | x   | IOUT_OC_WARN_LIMIT |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name           | Description                                                                                                                                                                                                             |
|-------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED           | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                       |
| 9:0   | IOUT_OC_WARN_LIMIT | Output current OC warning threshold. If the sensed output current is greater than this threshold, bit[5] of STATUS_IOUT (7Bh) is set.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

**MFR\_CS\_OFFSET1 (4Ch)**

This register sets the phase-current offset for the current balance loop.

| Command  | MFR_CS_OFFSET1 |              |     |     |     |     |              |     |     |     |     |              |     |     |     |     |
|----------|----------------|--------------|-----|-----|-----|-----|--------------|-----|-----|-----|-----|--------------|-----|-----|-----|-----|
| Format   | Signed binary  |              |     |     |     |     |              |     |     |     |     |              |     |     |     |     |
| Bit      | 15             | 14           | 13  | 12  | 11  | 10  | 9            | 8   | 7   | 6   | 5   | 4            | 3   | 2   | 1   | 0   |
| Access   | r/w            | r/w          | r/w | r/w | r/w | r/w | r/w          | r/w | r/w | r/w | r/w | r/w          | r/w | r/w | r/w | r/w |
| Function | x              | CS_OS_PHASE4 |     |     |     |     | CS_OS_PHASE3 |     |     |     |     | CS_OS_PHASE2 |     |     |     |     |

| Bits  | Bit Name     | Description                                                                      |
|-------|--------------|----------------------------------------------------------------------------------|
| 15    | RESERVED     | Unused. X indicates that writes are ignored and always read as 0.                |
| 14:10 | CS_OS_PHASE4 | Phase 4 current offset. Two's complement binary format. Bit[14] is the sign bit. |
| 9:5   | CS_OS_PHASE3 | Phase 3 current offset. Two's complement binary format. Bit[9] is the sign bit.  |
| 4:0   | CS_OS_PHASE2 | Phase 2 current offset. Two's complement binary format. Bit[4] is the sign bit.  |

Calculate the phase-current offset with Equation (15)

$$CS\_OS\_PHASEn = 512 \times I_{OFFSET} \times K_{CS} \times R_{CS} / 1600 \quad (15)$$

Where  $R_{CS}$  is the phase current sense resistor (in k $\Omega$ ), and  $K_{CS}$  is the current sense gain of the DrMOS (in  $\mu A/A$ ).

### MFR\_CS\_OFFSET2 (4Dh)

This register sets phase-current offset for the current balance loop.

| Command  | MFR_CS_OFFSET2 |              |     |     |     |     |              |     |     |     |     |              |     |     |     |     |
|----------|----------------|--------------|-----|-----|-----|-----|--------------|-----|-----|-----|-----|--------------|-----|-----|-----|-----|
| Format   | Signed binary  |              |     |     |     |     |              |     |     |     |     |              |     |     |     |     |
| Bit      | 15             | 14           | 13  | 12  | 11  | 10  | 9            | 8   | 7   | 6   | 5   | 4            | 3   | 2   | 1   | 0   |
| Access   | r/w            | r/w          | r/w | r/w | r/w | r/w | r/w          | r/w | r/w | r/w | r/w | r/w          | r/w | r/w | r/w | r/w |
| Function | x              | CS_OS_PHASE7 |     |     |     |     | CS_OS_PHASE6 |     |     |     |     | CS_OS_PHASE5 |     |     |     |     |

| Bits  | Bit Name     | Description                                                                      |
|-------|--------------|----------------------------------------------------------------------------------|
| 15    | RESERVED     | Unused. X indicates that writes are ignored and always read as 0.                |
| 14:10 | CS_OS_PHASE7 | Phase 7 current offset. Two's complement binary format. Bit[14] is the sign bit. |
| 9:5   | CS_OS_PHASE6 | Phase 6 current offset. Two's complement binary format. Bit[9] is the sign bit.  |
| 4:0   | CS_OS_PHASE5 | Phase 5 current offset. Two's complement binary format. Bit[4] is the sign bit.  |

Calculate the phase-current offset with Equation (16):

$$CS\_OS\_PHASEn = 512 \times I_{OFFSET} \times K_{CS} \times R_{CS} / 1600 \quad (16)$$

Where  $R_{CS}$  is the phase current sense resistor (in k $\Omega$ ), and  $K_{CS}$  is the current sense gain of the DrMOS (in  $\mu A/A$ ).

### MFR\_CS\_OFFSET3 (4Eh)

This register sets the phase-current offset for the current balance loop.

| Command  | MFR_CS_OFFSET3 |               |     |     |     |     |              |     |     |     |     |              |     |     |     |     |
|----------|----------------|---------------|-----|-----|-----|-----|--------------|-----|-----|-----|-----|--------------|-----|-----|-----|-----|
| Format   | Signed binary  |               |     |     |     |     |              |     |     |     |     |              |     |     |     |     |
| Bit      | 15             | 14            | 13  | 12  | 11  | 10  | 9            | 8   | 7   | 6   | 5   | 4            | 3   | 2   | 1   | 0   |
| Access   | r/w            | r/w           | r/w | r/w | r/w | r/w | r/w          | r/w | r/w | r/w | r/w | r/w          | r/w | r/w | r/w | r/w |
| Function | x              | CS_OS_PHASE10 |     |     |     |     | CS_OS_PHASE9 |     |     |     |     | CS_OS_PHASE8 |     |     |     |     |

| Bits  | Bit Name      | Description                                                                       |
|-------|---------------|-----------------------------------------------------------------------------------|
| 15    | RESERVED      | Unused. X indicates that write are ignored and always read as 0.                  |
| 14:10 | CS_OS_PHASE10 | Phase 10 current offset. Two's complement binary format. Bit[14] is the sign bit. |
| 9:5   | CS_OS_PHASE9  | Phase 9 current offset. Two's complement binary format. Bit[9] is the sign bit.   |
| 4:0   | CS_OS_PHASE8  | Phase 8 current offset. Two's complement binary format. Bit[4] is the sign bit.   |

Calculate the phase-current offset with Equation (17)

$$CS\_OS\_PHASEn = 512 \times I_{OFFSET} \times K_{CS} \times R_{CS} / 1600 \quad (17)$$

Where  $R_{CS}$  is the phase current sense resistor (in kΩ), and  $K_{CS}$  is the current sense gain of the DrMOS (in μA/A).

### OT\_WARN\_LIMIT (51h)

This register sets the over-temperature warning threshold via VTEMP.

| Command | OT_WARN_LIMIT   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|---------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format  | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit     | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access  | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |

|          |               |   |   |   |                                                                                                                                                        |   |   |   |               |  |
|----------|---------------|---|---|---|--------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---------------|--|
| Function | x             | x | x | x | x                                                                                                                                                      | x | x | x | OT_WARN_LIMIT |  |
| Bits     | Bit Name      |   |   |   | Description                                                                                                                                            |   |   |   |               |  |
| 15:8     | RESERVED      |   |   |   | Unused. X indicates writes are ignored and always reads are 0.                                                                                         |   |   |   |               |  |
| 7:0      | OT_WARN_LIMIT |   |   |   | Over-temperature warning threshold. If the sensed temperature via VTEMP is higher than this value, bit[6] of STATUS_TEMPERATURE (7Dh) is set. 1°C/LSB. |   |   |   |               |  |

### VIN\_OV\_FAULT\_LIMIT (55h)

This register sets the input OVP threshold.

| Command  | VIN_OV_FAULT_LIMIT              |     |     |     |     |                                                                                                                                                                                                                     |     |     |          |     |     |     |     |     |     |     |
|----------|---------------------------------|-----|-----|-----|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|----------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Linear, two's complement binary |     |     |     |     |                                                                                                                                                                                                                     |     |     |          |     |     |     |     |     |     |     |
| Bit      | 15                              | 14  | 13  | 12  | 11  | 10                                                                                                                                                                                                                  | 9   | 8   | 7        | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                             | r/w | r/w | r/w | r/w | r/w                                                                                                                                                                                                                 | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent                        |     |     |     |     | x                                                                                                                                                                                                                   |     |     | Mantissa |     |     |     |     |     |     |     |
| Bits     | Bit Name                        |     |     |     |     | Description                                                                                                                                                                                                         |     |     |          |     |     |     |     |     |     |     |
| 15:11    | Exponent                        |     |     |     |     | This value is in two's complement binary format (fixed at 11101).<br>Exponent = -3                                                                                                                                  |     |     |          |     |     |     |     |     |     |     |
| 10:8     | RESERVED                        |     |     |     |     | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                   |     |     |          |     |     |     |     |     |     |     |
| 7:0      | Mantissa                        |     |     |     |     | $VIN\_OV\_FAULT\_LIMIT = Mantissa \times 2^{\text{exponent}} = Mantissa \times 0.125$<br><br>If the sensed input voltage is greater than this threshold, input OVP is triggered, and the VR shuts down immediately. |     |     |          |     |     |     |     |     |     |     |

### VIN\_UV\_WARN\_LIMIT (58h)

This register sets the input under-voltage warning threshold.

| Command  | VIN_UV_WARN_LIMIT               |     |     |     |     |     |     |     |          |     |     |     |     |     |     |     |
|----------|---------------------------------|-----|-----|-----|-----|-----|-----|-----|----------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Linear, two's complement binary |     |     |     |     |     |     |     |          |     |     |     |     |     |     |     |
| Bit      | 15                              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7        | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent                        |     |     |     |     | x   |     |     | Mantissa |     |     |     |     |     |     |     |

| Bits  | Bit Name | Description                                                                                                                                                                                                |
|-------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | Exponent | This value is in two's complement binary format (fixed at 11101).<br>Exponent = -3                                                                                                                         |
| 10:8  | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                          |
| 7:0   | Mantissa | $VIN\_UV\_WARN\_LIMIT = Mantissa \times 2^{\text{exponent}} = Mantissa \times 0.125$<br>If the sensed input voltage is lower than this threshold, bit[5] of the status register STATUS_INPUT (7Ch) is set. |

### MFR\_DELAY\_SET (5Dh)

The register sets the delay time of the power good signal and internal V<sub>OUT</sub> settle signal.

| Command  | MFR_DELAY_SET   |     |     |              |     |     |     |          |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|--------------|-----|-----|-----|----------|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |              |     |     |     |          |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12           | 11  | 10  | 9   | 8        | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w          | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | SETTLE_DELAY |     |     |     | PG_DELAY |     |     |     |     |     |     |     |     |

| Bits  | Bit Name     | Description                                                                                                                                                                                                                                                                                                                                                                          |
|-------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED     | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                    |
| 12:9  | SETTLE_DELAY | Delay time from when the output voltage reference reaches the target level to when the internal V <sub>OUT</sub> settle signal becomes high. 100µs/LSB.<br>When V <sub>REF</sub> is ramping (soft start or DVID), the settle signal is low. When V <sub>REF</sub> is settled, the settle signal is high. The DC loop or auto-power mode operate only when the settle signal is high. |
| 8:0   | PG_DELAY     | Delay time for asserting the power good signal. 1µs/LSB.                                                                                                                                                                                                                                                                                                                             |

### POWER\_GOOD\_ON (5Eh)

This register sets the output voltage threshold at which the power good signal is asserted.

| Command  | POWER_GOOD_ON |     |     |     |     |     |     |               |     |     |     |     |     |     |     |     |
|----------|---------------|-----|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | VID           |     |     |     |     |     |     |               |     |     |     |     |     |     |     |     |
| Bit      | 15            | 14  | 13  | 12  | 11  | 10  | 9   | 8             | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w           | r/w | r/w | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x             | x   | x   | x   | x   | x   | x   | POWER_GOOD_ON |     |     |     |     |     |     |     |     |

| Bits | Bit Name      | Description                                                                      |
|------|---------------|----------------------------------------------------------------------------------|
| 15:9 | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                |
| 8:0  | POWER_GOOD_ON | Output voltage threshold at which the power good signal is asserted. 6.25mV/LSB. |

### POWER\_GOOD\_OFF (5Fh)

This register sets the output voltage threshold at which the power good signal is deasserted.

| Command  | POWER_GOOD_OFF |     |     |     |     |     |     |                |     |     |     |     |     |     |     |     |
|----------|----------------|-----|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | VID            |     |     |     |     |     |     |                |     |     |     |     |     |     |     |     |
| Bit      | 15             | 14  | 13  | 12  | 11  | 10  | 9   | 8              | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w            | r/w | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x              | x   | x   | x   | x   | x   | x   | POWER_GOOD_OFF |     |     |     |     |     |     |     |     |

| Bits | Bit Name       | Description                                                                          |
|------|----------------|--------------------------------------------------------------------------------------|
| 15:9 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                    |
| 8:0  | POWER_GOOD_OFF | Output voltage threshold at which the power good signal is deasserted.<br>6.25mV/LSB |

### TON\_DELAY (60h)

This register sets the time from when the controller receives the EN on signal to when  $V_{REF}$  starts to boot up.

| Command  | TON_DELAY       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | EN_ON_DELAY     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name    | Description                                                                                                         |
|------|-------------|---------------------------------------------------------------------------------------------------------------------|
| 15:0 | EN_ON_DELAY | Delay time from EN on to $V_{REF}$ boot-up.<br>50 $\mu$ s/LSB (DLY_CLK_SEL = 1)<br>20 $\mu$ s/LSB (DLY_CLK_SEL = 0) |

### TOFF\_DELAY (64h)

This register sets the time from when the controller receives the EN off signal to when  $V_{REF}$  starts to soft-shut down.

| Command  | TOFF_DELAY      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | EN_OFF_DELAY    |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name     | Description                                                                                                                |
|------|--------------|----------------------------------------------------------------------------------------------------------------------------|
| 15:0 | EN_OFF_DELAY | Delay time from EN off to $V_{REF}$ soft-shutdown.<br>50 $\mu$ s/LSB (DLY_CLK_SEL = 1)<br>20 $\mu$ s/LSB (DLY_CLK_SEL = 0) |

### POUT\_OP\_WARN\_LIMIT (6Ah)

This register sets the output over-power warning threshold.

| Command  | POUT_OP_WARN_LIMIT |     |     |     |     |     |                    |     |     |     |     |     |     |     |     |     |
|----------|--------------------|-----|-----|-----|-----|-----|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary    |     |     |     |     |     |                    |     |     |     |     |     |     |     |     |     |
| Bit      | 15                 | 14  | 13  | 12  | 11  | 10  | 9                  | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                | r/w | r/w | r/w | r/w | r/w | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                  | x   | x   | x   | x   | x   | POUT_OP_WARN_LIMIT |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name           | Description                                                                                                                                                                                                          |
|-------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED           | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                    |
| 9:0   | POUT_OP_WARN_LIMIT | Output over-power warning threshold. If the sensed output power is higher than this threshold, bit[0] of STATUS_IOUT (7Bh) is set.<br>1W/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2W/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

### START\_CATCH\_AVE (6Bh)

This command is used for READ\_IOUT, READ\_PIN, READ\_POUT, and READ\_EFFECIENCY when these registers are in latch mode. Send the START\_CATCH\_AVE command to trigger the averaging process within a certain average window. At the end of the average window, the results are latched.

The averaging mode and average window are determined by MFR\_REPORT\_CTRL (ADh).

This command is write only. There is no data byte for this command.

### READ\_CS1\_2 (73h)

This register is phase-current ADC value of phase 1 and phase 2. An internal low pass filter is used before ADC.

|          |                 |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----|---|---|----------|---|---|---|---|---|---|---|
| Command  | READ_CS1_2      |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Format   | Unsigned binary |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r  | r | r | r        | r | r | r | r | r | r | r |
| Function | READ_CS2        |    |    |    |    |    |   |   | READ_CS1 |   |   |   |   |   |   |   |

| Bits | Bit Name | Description                      |
|------|----------|----------------------------------|
| 15:8 | READ_CS2 | Phase 2 current ADC sense value. |
| 7:0  | READ_CS1 | Phase 1 current ADC sense value. |

Calculate the per-phase current sense with Equation (18):

$$CS_n = 256 \times (I_{CS} \times K_{CS} \times R_{CS} / 1000 + 1.23) / 3.2 \quad (18)$$

Where  $R_{CS}$  is the phase current sense resistor (in kΩ), and  $K_{CS}$  is the current sense gain of the DrMOS (in μA/A).

If PHASE\_CURRENT\_RESOLUTION = 1 in register 44h, the CS report should be doubled.

### READ\_CS3\_4 (74h)

This register is the phase-current ADC value of phase 3 and phase 4. An internal low-pass filter is used before ADC.

|          |                 |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----|---|---|----------|---|---|---|---|---|---|---|
| Command  | READ_CS3_4      |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Format   | Unsigned binary |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r  | r | r | r        | r | r | r | r | r | r | r |
| Function | READ_CS4        |    |    |    |    |    |   |   | READ_CS3 |   |   |   |   |   |   |   |

| Bits | Bit Name | Description                      |
|------|----------|----------------------------------|
| 15:8 | READ_CS4 | Phase 4 current ADC sense value. |
| 7:0  | READ_CS3 | Phase 3 current ADC sense value. |

Calculate the per-phase current sense with Equation (19):

$$CS_n = 256 \times (I_{CS} \times K_{CS} \times R_{CS} / 1000 + 1.23) / 3.2 \quad (19)$$

Where  $R_{CS}$  is the phase current sense resistor (in kΩ), and  $K_{CS}$  is the current sense gain of the DrMOS (in μA/A).

If PHASE\_CURRENT\_RESOLUTION = 1 in register 44h, the CS report should be doubled.

**READ\_CS5\_6 (75h)**

This register is the phase-current ADC value of phase 5 and phase 6. An internal low-pass filter is used before ADC.

|          |                 |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----|---|---|----------|---|---|---|---|---|---|---|
| Command  | READ_CS5_6      |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Format   | Unsigned binary |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r  | r | r | r        | r | r | r | r | r | r | r |
| Function | READ_CS6        |    |    |    |    |    |   |   | READ_CS5 |   |   |   |   |   |   |   |

| Bits | Bit Name | Description                      |
|------|----------|----------------------------------|
| 15:8 | READ_CS6 | Phase 6 current ADC sense value. |
| 7:0  | READ_CS5 | Phase 5 current ADC sense value. |

Calculate the per-phase current sense with Equation (20):

$$CS_n = 256 \times (I_{CS} \times K_{CS} \times R_{CS}/1000 + 1.23) / 3.2 \quad (20)$$

Where  $R_{CS}$  is the phase current sense resistor (in kΩ), and  $K_{CS}$  is the current sense gain of the DrMOS (in μA/A).

If PHASE\_CURRENT\_RESOLUTION = 1 in register 44h, the CS report should be doubled.

**READ\_CS7\_8 (76h)**

This register is the phase-current ADC value of phase 7 and phase 8. An internal low-pass filter is used before ADC.

|          |                 |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----|---|---|----------|---|---|---|---|---|---|---|
| Command  | READ_CS7_8      |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Format   | Unsigned binary |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r  | r | r | r        | r | r | r | r | r | r | r |
| Function | READ_CS8        |    |    |    |    |    |   |   | READ_CS7 |   |   |   |   |   |   |   |

| Bits | Bit Name | Description                      |
|------|----------|----------------------------------|
| 15:8 | READ_CS8 | Phase 8 current ADC sense value. |
| 7:0  | READ_CS7 | Phase 7 current ADC sense value. |

Calculate the per-phase current sense with Equation (21):

$$CS_n = 256 \times (I_{CS} \times K_{CS} \times R_{CS}/1000 + 1.23) / 3.2 \quad (21)$$

Where  $R_{CS}$  is the phase current sense resistor (in kΩ), and  $K_{CS}$  is the current sense gain of the DrMOS (in μA/A).

If PHASE\_CURRENT\_RESOLUTION = 1 in register 44h, the CS report should be doubled.

**READ\_CS9\_10 (77h)**

This register is the phase-current ADC value of phase 9 and phase 10. An internal low-pass filter is used before ADC.

|          |                 |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----|---|---|----------|---|---|---|---|---|---|---|
| Command  | READ_CS9_10     |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Format   | Unsigned binary |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r  | r | r | r        | r | r | r | r | r | r | r |
| Function | READ_CS10       |    |    |    |    |    |   |   | READ_CS9 |   |   |   |   |   |   |   |

| Bits | Bit Name  | Description                       |
|------|-----------|-----------------------------------|
| 15:8 | READ_CS10 | Phase 10 current ADC sense value. |
| 7:0  | READ_CS9  | Phase 9 current ADC sense value.  |

Calculate the per-phase current sense with Equation (22):

$$CS_n = 256 \times (I_{CS} \times K_{CS} \times R_{CS}/1000 + 1.23) / 3.2 \quad (22)$$

Where  $R_{CS}$  is the phase current sense resistor (in kΩ), and  $K_{CS}$  is the current sense gain of the DrMOS (in μA/A).

If PHASE\_CURRENT\_RESOLUTION = 1 in register 44h, the CS report should be doubled.

**STATUS\_BYTE (78h)**

This register returns one byte of information for critical faults.

|          |                 |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Command  | STATUS_BYTE     |     |     |     |     |     |     |     |
| Format   | Unsigned binary |     |     |     |     |     |     |     |
| Bit      | 7               | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               |     |     |     |     |     |     | x   |

| Bits | Bit Name      | Description                                                                                                                                    |
|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                                                                              |
| 6    | OFF           | This bit is asserted if the unit is not providing power to the output. This bit is in live mode.                                               |
| 5    | VOUT_OV_FAULT | Once output OVP occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                               |
| 4    | IOUT_OC_FAULT | Once output OCP occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                               |
| 3    | VIN_UV_FAULT  | Once input UVP occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                |
| 2    | TEMPERATURE   | Once OTP or a warning occur, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                          |
| 1    | CML           | Once a communications, memory, or logic fault occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit. |
| 0    | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                                                                              |

## STATUS\_WORD (79h)

This register returns two bytes of information for fault statuses. Based on this information, the host can get more information by reading the appropriate status registers. The low byte of STATUS\_WORD is the same as the STATUS\_BYTE register.

| Command  | STATUS_WORD     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r  | r | r | r | r | r | r | r | r | r | r |
| Function |                 |    |    |    |    | x  | x |   | x |   |   |   |   |   |   | x |

| Bits | Bit Name      | Description                                                                                                                                                                                                                                                                 |
|------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | VOUT          | Once output OVP, UVP, or a warning occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                         |
| 14   | IOUT/POUT     | Once output OCP, over-power protection (OPP), or a warning occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                 |
| 13   | INPUT         | Once any protection or warning of the input voltage, input current, or input power occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                         |
| 12   | READ_DATA_RDY | When READ_PIN, READ_POUT, or READ_EFFECTICIENCY uses average window mode and once the average window calculation is done, the data is ready in the resister, and this bit is set. Sending the command START_CATCH_AVE triggers a new averaging process and resets this bit. |
| 11   | POWER_GOOD    | When V <sub>OUT</sub> rises higher than the POWER_GOOD_ON level during the soft-start process and the delay time is reached, this bit is asserted. This bit is in live mode.                                                                                                |
| 10:9 | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                           |
| 8    | WATCH_DOG_OVF | The monitor value calculation has a watchdog timer. If the timer expires, the monitor value calculation state machine and the timer are reset. Meanwhile, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                          |
| 7    | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                           |
| 6    | OFF           | This bit is asserted if the unit is not providing power to the output. This bit is in live mode.                                                                                                                                                                            |
| 5    | VOUT_OV_FAULT | Once output OVP occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                            |
| 4    | IOUT_OC_FAULT | Once output OCP occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                            |
| 3    | VIN_UV_FAULT  | Once input UVP occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                             |
| 2    | TEMPERATURE   | Once OTP or a warning occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                      |
| 1    | CML           | Once a communications, memory, or logic fault occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                              |
| 0    | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                           |

## STATUS\_VOUT (7Ah)

This register records the fault and warning status of the output voltage.

| Command  | STATUS_VOUT     |   |   |   |   |   |   |   |
|----------|-----------------|---|---|---|---|---|---|---|
| Format   | Unsigned binary |   |   |   |   |   |   |   |
| Bit      | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r | r | r | r | r | r | r |
| Function |                 | x |   |   |   | x |   |   |

| Bits | Bit Name             | Description                                                                                                                                                                                                                                                           |
|------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | VOUT_OV_FAULT        | Once output OVP occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                      |
| 6    | RESERVED             | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                     |
| 5    | VOUT_UV_WARNING      | Once an output over-voltage warning occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                  |
| 4    | VOUT_UV_FAULT        | Once output UVP occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                      |
| 3    | VOUT_MAX_MIN_WARNING | Once the value of the PMBus command VOUT_COMMAND, VOUT_MARGIN_HIGH, or VOUT_MARGIN_LOW exceeds VOUT_MAX or VOUT_MIN, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                         |
| 2    | RESERVED             | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                     |
| 1    | LINE_FLOAT           | During the EEPROM restore process after the chip powers on, the controller can check if the output voltage remote sense pin is floating with this function enabled. Once the controller detects that VOSEN is floating, it enters shutdown mode, and this bit is set. |
| 0    | VDIFF_FAULT          | During the soft-start process, once the MP2888A detects that VOSEN is greater than VDIFF by 0.5V, the VR is shut down immediately, and this bit is set.                                                                                                               |

## STATUS\_IOUT (7Bh)

This register records the fault and warning status of the output current.

| Command  | STATUS_IOUT     |   |   |   |   |   |   |   |
|----------|-----------------|---|---|---|---|---|---|---|
| Format   | Unsigned binary |   |   |   |   |   |   |   |
| Bit      | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r | r | r | r | r | r | r |
| Function |                 |   |   | x | x | x | x |   |

| Bits | Bit Name        | Description                                                                                                                        |
|------|-----------------|------------------------------------------------------------------------------------------------------------------------------------|
| 7    | IOUT_OC_FAULT   | Once output OCP occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                   |
| 6    | OC_UV_FAULT     | If both output OCP and OVP occur, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.         |
| 5    | IOUT_OC_WARNING | Once an output OC warning occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.         |
| 4:1  | RESERVED        | Unused. X indicates that writes are ignored and always read as 0.                                                                  |
| 0    | POUT_OP_WARNING | Once output over-power protection occurs, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit. |

## STATUS\_INPUT (7Ch)

This register records the fault and warning status of the input voltage, input current, and input power.

| Command  | STATUS_INPUT    |   |   |   |   |   |   |   |
|----------|-----------------|---|---|---|---|---|---|---|
| Format   | Unsigned binary |   |   |   |   |   |   |   |
| Bit      | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r | r | r | r | r | r | r |
| Function |                 | x |   |   |   | x | x | x |

| Bits | Bit Name       | Description                                                                                                                                                                  |
|------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | VIN_OV_FAULT   | Once the sensed input voltage is greater than VIN_OV_FAULT_LIMIT (55h), this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.             |
| 6    | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                                                                                                            |
| 5    | VIN_UV_WARNING | Once the sensed input voltage is less than VIN_UV_WARN_LIMIT (58h), this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                 |
| 4    | VIN_UVLO_LATCH | Once the sensed input voltage is less than VIN_OFF, the VR turns off the power, and this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit. |
| 3    | VIN_UVLO_LIVE  | Once the sensed input voltage is less than VIN_OFF, this bit is set. Once the sensed input voltage is greater than VIN_ON, this bit is reset. This bit is in live mode.      |
| 2:0  | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                                                                                                            |

## STATUS\_TEMPERATURE (7Dh)

This register records the fault and warning status of temperature.

| Command  | STATUS_TEMPERATURE |   |   |   |   |   |   |   |
|----------|--------------------|---|---|---|---|---|---|---|
| Format   | Unsigned binary    |   |   |   |   |   |   |   |
| Bit      | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r                  | r | r | r | r | r | r | r |
| Function |                    |   | x | x |   |   | x | x |

| Bits | Bit Name        | Description                                                                                                                                                         |
|------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | TEMP_OT_FAULT   | Once the sensed temperature via VTEMP is greater than VTEMP_OTP_LIMIT, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.     |
| 6    | TEMP_OT_WARNING | Once the sensed temperature via VTEMP is greater than VTEMP_OT_WARN_LIMIT, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit. |
| 5:4  | RESERVED        | Unused. X indicates that writes are ignored and always read as 0.                                                                                                   |
| 3    | TSNS_OT_FAULT   | Once the sensed temperature via TSNS is greater than the TSNS_OTP_LIMIT, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.   |
| 2    | TSNS_OT_WARNING | Once the sensed temperature via TSNS is greater than TSNS_OT_WARN_LIMIT, this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.   |
| 1:0  | RESERVED        | Unused. X indicates that writes are ignored and always read as 0.                                                                                                   |

**STATUS\_CML (7Eh)**

This register records the fault status of PMBus communication and EEPROM operation.

| Command  | STATUS_CML      |   |   |   |   |   |   |   |
|----------|-----------------|---|---|---|---|---|---|---|
| Format   | Unsigned binary |   |   |   |   |   |   |   |
| Bit      | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r | r | r | r | r | r | r |
| Function |                 |   |   |   |   |   |   |   |

| Bits | Bit Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | INVALID_CMD      | This bit is set when it receives an unsupported command code. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                                                                                                                                                                                                                          |
| 6    | INVALID_DATA     | This bit is set when it receives invalid or unsupported data (host sends too many bytes). This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                                                                                                                                                                                              |
| 5    | PEC_FAULT        | The PMBus interface supports the use of a packet error checking (PEC) byte that is defined in the SMBus standard. The PEC byte is transmitted by the MP2888A during a read transaction or sent by the bus host to the MP2888A during a write transaction. If the PEC byte is sent during a write transaction is incorrect, the command is not executed, and this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                           |
| 4    | CRC_FAULT        | During the process of storing memory data to the EEPROM, the MP2888A calculates the CRC for each bit and saves the final CRC code to the EEPROM. During the process of restoring the EEPROM data to the memory, the MP2888A calculates the CRC code with each bit. The MP2888A checks the CRC results when the restore process is done. If the CRC result is incorrect, the VR does not start up, and this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit. |
| 3    | MEMORY_PWD_MATCH | There is write protection for the PMBus registers. If enabled, the PMBus registers can be read only and are not writeable. The register MFR_USER_PWD (04h) stores the password. Once the key is matched with MFR_USER_PWD, this bit is set. Otherwise, this bit is reset. This bit is in live mode.                                                                                                                                                                                            |
| 2    | FUALT_STORE_FLAG | This device automatically records fault statuses to the EEPROM. Once the power shuts down for any protection, the fault status record process is triggered, and this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                                                                                                       |
| 1    | CML_OTHER_FAULTS | If any of the below faults occur during PMBus communication, this bit is set.<br>1) Sending too few bits<br>2) Reading too few bits<br>3) Host sends or reads too few bytes<br>4) Reading too many bytes<br>This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                                                                            |
| 0    | EEPROM_FAULTS    | When restoring data from the EEPROM to the memory, this bit first checks the signature register in address 00h of the EEPROM. If the signature is not matched, this process is ceased immediately, and this bit is set. This bit is in latch mode. The CLEAR_FAULTS command can reset this bit.                                                                                                                                                                                                |

### READ\_VIN (88h)

This register records the sensed input voltage.

| Command  | READ_VIN        |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r  | r        | r | r | r | r | r | r | r | r | r |
| Function | x               | x  | x  | x  | x  | x  | READ_VIN |   |   |   |   |   |   |   |   |   |

| Bits  | Bit Name | Description              |
|-------|----------|--------------------------|
| 15:10 | RESERVED | Unused. Fixed to 111011. |
| 9:0   | READ_VIN | 0.03125V/LSB.            |

### READ\_VOUT (8Bh)

This register records the sensed output voltage.

| Command  | READ_VOUT       |    |    |    |           |    |   |   |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|-----------|----|---|---|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary |    |    |    |           |    |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11        | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r         | r  | r | r | r | r | r | r | r | r | r | r |
| Function | x               | x  | x  | x  | READ_VOUT |    |   |   |   |   |   |   |   |   |   |   |

| Bits  | Bit Name  | Description                                                       |
|-------|-----------|-------------------------------------------------------------------|
| 15:12 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0. |
| 11:0  | READ_VOUT | 1mV/LSB.                                                          |

### READ\_IOUT (8Ch)

This register records the sensed output current.

| Command  | READ_IOUT       |    |    |    |           |    |   |   |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|-----------|----|---|---|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary |    |    |    |           |    |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11        | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r         | r  | r | r | r | r | r | r | r | r | r | r |
| Function | x               | x  | x  | x  | READ_IOUT |    |   |   |   |   |   |   |   |   |   |   |

| Bits  | Bit Name  | Description                                                                         |
|-------|-----------|-------------------------------------------------------------------------------------|
| 15:12 | RESERVED  | Unused. Fixed to 1110.                                                              |
| 11:0  | READ_IOUT | 0.25A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>0.5A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

### READ\_TEMPERATURE (8Dh)

This register records the sensed temperature.

| Command  | READ_TEMPERATURE |    |    |    |    |                  |   |   |   |   |   |   |   |   |   |   |
|----------|------------------|----|----|----|----|------------------|---|---|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary  |    |    |    |    |                  |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15               | 14 | 13 | 12 | 11 | 10               | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r                | r  | r  | r  | r  | r                | r | r | r | r | r | r | r | r | r | r |
| Function | x                | x  | x  | x  | x  | READ_TEMPERATURE |   |   |   |   |   |   |   |   |   |   |

| Bits  | Bit Name         | Description                                                       |
|-------|------------------|-------------------------------------------------------------------|
| 15:11 | RESERVED         | Unused. X indicates that writes are ignored and always read as 0. |
| 10:0  | READ_TEMPERATURE | 0.1°C/LSB.                                                        |

### READ\_EFFECIENCY (95h)

This register records the calculated efficiency of the VR.

| Command  | READ_EFFECIENCY |    |    |    |    |    |   |                 |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----|---|-----------------|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary |    |    |    |    |    |   |                 |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8               | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r  | r | r               | r | r | r | r | r | r | r | r |
| Function | x               | x  | x  | x  | x  | x  | x | READ_EFFECIENCY |   |   |   |   |   |   |   |   |

| Bits | Bit Name        | Description                                                       |
|------|-----------------|-------------------------------------------------------------------|
| 15:9 | RESERVED        | Unused. X indicates that writes are ignored and always read as 0. |
| 8:0  | READ_EFFECIENCY | 0.195%/LSB.                                                       |

### READ\_POUT (96h)

This register records the sensed output power.

| Command  | READ_POUT       |    |    |    |    |           |   |   |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|-----------|---|---|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary |    |    |    |    |           |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10        | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r         | r | r | r | r | r | r | r | r | r | r |
| Function | x               | x  | x  | x  | x  | READ_POUT |   |   |   |   |   |   |   |   |   |   |

| Bits  | Bit Name  | Description                                                                      |
|-------|-----------|----------------------------------------------------------------------------------|
| 15:11 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                |
| 10:0  | READ_POUT | 0.5W/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>1W/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

### READ\_PIN (97h)

This register records the calculated input power.

| Command  | READ_PIN        |    |    |    |    |          |   |   |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary |    |    |    |    |          |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11 | 10       | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r  | r        | r | r | r | r | r | r | r | r | r | r |
| Function | x               | x  | x  | x  | x  | READ_PIN |   |   |   |   |   |   |   |   |   |   |

| Bits  | Bit Name | Description                                                                      |
|-------|----------|----------------------------------------------------------------------------------|
| 15:11 | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                |
| 10:0  | READ_PIN | 0.5W/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>1W/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

**MFR\_APS\_FS\_LIMIT1 (A3h)**

This register sets the interval time threshold between the consecutive phases' PWM rising edges to detect a fast load increase. When APS is enabled and the system sheds phases, once the interval time is lower than this threshold, the VR exits phase shedding and runs with a full phase for a configurable amount of time.

|          |                   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Command  | MFR_APS_FS_LIMIT1 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Format   | Unsigned binary   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w               | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |                   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name    | Description                                                                                                                                                                |
|------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | FS_LIMIT_4P | Threshold of the interval time between consecutive phases' PWM rising edges when the VR has shed to four phases. 5ns/LSB.<br>Add PHASE_BLANK_TIME to the final threshold.  |
| 7:0  | FS_LIMIT_3P | Threshold of the interval time between consecutive phases' PWM rising edges when the VR has shed to three phases. 5ns/LSB.<br>Add PHASE_BLANK_TIME to the final threshold. |

**MFR\_APS\_FS\_LIMIT2 (A4h)**

This register sets the interval time threshold between the consecutive phases' PWM rising edges to detect a fast load increase. When APS is enabled and the system sheds phases, once the interval time is lower than this threshold, the system exits phase shedding and runs with a full phase for a configurable amount of time.

|          |                   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Command  | MFR_APS_FS_LIMIT2 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Format   | Unsigned binary   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w               | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |                   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name    | Description                                                                                                                                                               |
|------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | FS_LIMIT_6P | Threshold of the interval time between consecutive phases' PWM rising edges when the VR has shed to six phases. 5ns/LSB.<br>Add PHASE_BLANK_TIME to the final threshold.  |
| 7:0  | FS_LIMIT_5P | Threshold of the interval time between consecutive phases' PWM rising edges when the VR has shed to five phases. 5ns/LSB.<br>Add PHASE_BLANK_TIME to the final threshold. |

**MFR\_APS\_FS\_LIMIT3 (A5h)**

This register sets the interval time threshold between the consecutive phases' PWM rising edges to detect a fast load increase. When APS is enabled and the system sheds phases, once the interval time is lower than this threshold, system exits phase shedding and runs with a full-phase for a configurable amount of time.

|         |                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Command | MFR_APS_FS_LIMIT3 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Format  | Unsigned binary   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Bit     | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

|          |             |     |     |     |                                                                                                                                                                            |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-------------|-----|-----|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Access   | r/w         | r/w | r/w | r/w | r/w                                                                                                                                                                        | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |             |     |     |     |                                                                                                                                                                            |     |     |     |     |     |     |     |     |     |     |     |     |
| Bits     | Bit Name    |     |     |     | Description                                                                                                                                                                |     |     |     |     |     |     |     |     |     |     |     |     |
| 15:8     | FS_LIMIT_8P |     |     |     | Threshold of the interval time between consecutive phases' PWM rising edges when the VR has shed to eight phases. 5ns/LSB.<br>Add PHASE_BLANK_TIME to the final threshold. |     |     |     |     |     |     |     |     |     |     |     |     |
| 7:0      | FS_LIMIT_7P |     |     |     | Threshold of the interval time between consecutive phases' PWM rising edges when the VR has shed to seven phases. 5ns/LSB.<br>Add PHASE_BLANK_TIME to the final threshold. |     |     |     |     |     |     |     |     |     |     |     |     |

#### MFR\_APS\_FS\_LIMIT4 (A6h)

This register sets the interval time threshold between the consecutive phases' PWM rising edges to detect a fast load increase. When APS is enabled and the system sheds phases, once the interval time is lower than this threshold, the system exits phase shedding and runs with a full-phase for a configurable amount of time.

|          |                   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Command  | MFR_APS_FS_LIMIT4 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Format   | Unsigned binary   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |     |
| Access   | r/w               | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |                   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

|      |              |  |  |  |                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |
|------|--------------|--|--|--|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|
| Bits | Bit Name     |  |  |  | Description                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |
| 15:8 | FS_LIMIT_10P |  |  |  | Threshold of the interval time between consecutive phases' PWM rising edges when the VR has shed to 10 phases. 5ns/LSB.<br>Add PHASE_BLANK_TIME to the final threshold.   |  |  |  |  |  |  |  |  |  |  |  |  |
| 7:0  | FS_LIMIT_9P  |  |  |  | Threshold of the interval time between consecutive phases' PWM rising edges when the VR has shed to nine phases. 5ns/LSB.<br>Add PHASE_BLANK_TIME to the final threshold. |  |  |  |  |  |  |  |  |  |  |  |  |

#### MFR\_APS\_FS\_CTRL1 (A7h)

This register sets the interval time threshold for phase 1's PWM to detect a fast load increase. When APS is enabled and the system sheds phases, once the controller detects that the PWM interval is lower than this threshold, the system exits phase shedding and runs with a full-phase for a configurable amount of time. This register also sets the enable bit for the exit-phase-shedding strategy via PWM frequency detection.

|          |                  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Command  | MFR_APS_FS_CTRL1 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Format   | Unsigned binary  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |     |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name         | Description                                                                                                                                                                                                                       |
|-------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED         | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                 |
| 12    | FS_EXIT_APS_EN1  | Enable bit of exit-phase-shedding according to phase 1's PWM interval time.<br>0: disable<br>1: enable<br>The controller detects phase 1's PWM interval time from the end of MIN_OFF_TIME.                                        |
| 11    | FS_EXIT_APS_EN2  | Enable bit of exit-phase-shedding according to the PWM interval time between consecutive phases.<br>0: disable<br>1: enable<br>The controller detects the consecutive phases' PWM interval time from the end of PHASE_BLANK_TIME. |
| 10:8  | FS_EXIT_APS_CNT1 | Continuous counting threshold for exit-phase-shedding according to phase 1's PWM interval time.                                                                                                                                   |
| 7:0   | FS_LIMIT_1P      | Threshold of phase 1's PWM interval time. 5ns/LSB.<br>Add MIN_OFF_TIME to the final threshold.                                                                                                                                    |

### MFR\_APS\_FS\_CTRL2 (A8h)

This register sets the threshold of the interval time between the consecutive phases' PWM rising edges to detect a fast load increase. When APS is enabled and the system sheds phases, once the controller detects that the PWM interval is lower than this threshold, the system exits phase shedding and runs with a full phase for a configurable amount of time. This register also sets the full-phase running time from exiting phase shedding to returning to phase-shedding mode.

| Command  | MFR_APS_FS_CTRL2 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name         | Description                                                                                                                                                              |
|-------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED         | Unused. X indicates that writes are ignored and always read as 0.                                                                                                        |
| 14:11 | RETURN_APS_DELAY | Delay time for returning APS from exiting phase shedding due to the PWM interval time being shorter than the configured threshold. 20µs/LSB.                             |
| 10:8  | FS_EXIT_APS_CNT2 | Continuous counting time threshold for exit-phase-shedding mode according to the PWM interval time between consecutive phases.                                           |
| 7:0   | FS_LIMIT_2P      | Threshold of the interval time between consecutive phases' PWM rising edges when the VR has shed to two phases. 5ns/LSB.<br>Add PHASE_BLANK_TIME to the final threshold. |

### MFR\_PHASE\_SHED\_CTRL (A9h)

This register sets the checking time for phase shedding by detecting the output current and set compensation to reduce voltage undershoot during phase dropping.

| Command  | MFR_PHASE_SHED_CTRL |     |     |     |     |     |     |     |                        |     |     |     |     |     |     |     |
|----------|---------------------|-----|-----|-----|-----|-----|-----|-----|------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary     |     |     |     |     |     |     |     |                        |     |     |     |     |     |     |     |
| Bit      | 15                  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7                      | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                 | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w                    | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | APS_DROP_CHECK_CNT  |     |     |     |     |     |     |     | EXIT_VO_CMPN_STEP_TIME |     |     |     |     |     |     |     |

| Bits | Bit Name               | Description                                                                                                                                                                                                                                                                                                                                                                   |
|------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | APS_DROP_CHECK_CNT     | Continuous counting-times threshold for phase shedding when the APS function is enabled. Once the output current enters the drop-phase window, an internal timer starts counting until it reaches this counting-times threshold. Then the VR drops phases. The timer resets if the output current exits the drop-phase window before it reaches the counting-times threshold. |
| 8:4  | EXIT_VO_CMPN_STEP_TIME | Interval time for reducing each 1.37mV step for $V_{OUT}$ compensation when the phase-dropping process ends. 50ns/LSB.                                                                                                                                                                                                                                                        |
| 3:0  | DROP_PHASE_VO_CMPN     | $V_{OUT}$ undershoot compensation value for phase dropping. 1.37mV/LSB.                                                                                                                                                                                                                                                                                                       |

### MFR\_LOW\_PHASE\_CNT (AAh)

This register sets the phase number when PSI is low (low-phase mode).

| Command  | MFR_LOW_PHASE_CNT |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w               | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                 | x   | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |

| Bits | Bit Name           | Description                                                                                                                                     |
|------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED           | Unused. X indicates that writes are ignored and always read as 0.                                                                               |
| 7:4  | LOW_PHASE_CNT_WARM | Phase number in low-phase mode (PSI is low) for warm boot. First time power-on after POR is considered to be a cool boot.                       |
| 3:0  | LOW_PHASE_CNT_COLD | Phase number in low-phase mode (PSI is low) for cold boot. Boot-up process beside the first power-on after POR is considered to be a warm boot. |

### MFR\_APS\_CTRL (ABh)

This register configures the detailed performance related to APS.

| Command  | MFR_APS_CTRL     |     |     |     |                                                                                                                                                                                                 |     |     |     |     |                     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|---------------------|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |                                                                                                                                                                                                 |     |     |     |     |                     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11                                                                                                                                                                                              | 10  | 9   | 8   | 7   | 6                   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w                                                                                                                                                                                             | r/w | r/w | r/w | r/w | r/w                 | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | RETURN_APS_DELAY |     |     |     |                                                                                                                                                                                                 |     |     |     |     | DROP_PHASE_INTERVAL |     |     |     |     |     |     |
| Bits     | Bit Name         |     |     |     | Description                                                                                                                                                                                     |     |     |     |     |                     |     |     |     |     |     |     |
| 15:10    | RETURN_APS_DELAY |     |     |     | Delay time for returning APS from exiting phase shedding due to phase 1 triggering the valley current limit when the system runs at 1-phase or $V_{FB}$ drops below $V_{REF}$ - 25mV. 20μs/LSB. |     |     |     |     |                     |     |     |     |     |     |     |
| 9        | N25MV_EXIT_EN    |     |     |     | Enable bit for exiting phase shedding (jumping to full-phase running) due to $V_{FB}$ dropping below $V_{REF}$ - 25mV when APS mode is enabled.<br>0: disable<br>1: enable                      |     |     |     |     |                     |     |     |     |     |     |     |
| 8        | PRD_EXIT_EN      |     |     |     | Enable bit for exiting phase-shedding (jumping to full-phase running) due to the PWM interval being shorter than the configured threshold.<br>0: disable<br>1: enable                           |     |     |     |     |                     |     |     |     |     |     |     |

|     |                     |                                                                                                                                                                                      |
|-----|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | OC_EXIT_EN          | Enable bit for exiting phase-shedding (jumping to full-phase running) due to phase 1 triggering the valley current limit when the system runs at 1-phase.<br>0: disable<br>1: enable |
| 6:1 | DROP_PHASE_INTERVAL | Interval time between dropping two adjacent phases when drop-phase mode is dropping sequentially (bit[0] = 1). 1μs/LSB.                                                              |
| 0   | DROP_PHASE_MODE     | Drop-phase mode selector.<br>0: drop phases together<br>1: drop phases one-by-one with interval time determined by bit[6:1]                                                          |

### MFR\_REPORT\_CTRL (ADh)

This register controls the reporting mode for READ\_VIN, READ\_VOUT, READ\_IOUT, READ\_PIN, READ\_POUT, READ\_EFFECIENCY, READ\_TON, and READ\_SWITCH\_PRD.

| Command  | MFR_REPORT_CTRL |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits             | Bit Name     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |            |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
|------------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------|----------------|------------|----------|---|---|---|-----------|---|---|---|-----------|---|---|---|------------------|---|---|---|-----------------|---|---|---|-----------|---|---|---|----------|---|---|---|
| 15:12            | RESERVED     | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
| 11:10            | REPORT_MODE  | <p>Reporting mode selector.</p> <p>00: average mode<br/>01: real-time mode<br/>1x: latch mode. Send the command START_CATCH_AVE to trigger the averaging process within the average window. At the end of the average window, the average results are latched.</p> <p>When reporting mode is set to real time or latch, some registers that do not have real time or latch mode report with average mode.</p> <p>READ_TEMPERATURE is always in real-time mode.</p> <table><tr><th></th><th>Average mode</th><th>Real-time mode</th><th>Latch mode</th></tr><tr><td>READ_VIN</td><td>✓</td><td>✓</td><td>x</td></tr><tr><td>READ_VOUT</td><td>✓</td><td>✓</td><td>x</td></tr><tr><td>READ_IOUT</td><td>✓</td><td>✓</td><td>✓</td></tr><tr><td>READ_TEMPERATURE</td><td>x</td><td>✓</td><td>x</td></tr><tr><td>READ_EFFICIENCY</td><td>✓</td><td>x</td><td>✓</td></tr><tr><td>READ_POUT</td><td>✓</td><td>x</td><td>✓</td></tr><tr><td>READ_PIN</td><td>✓</td><td>x</td><td>✓</td></tr></table> |            | Average mode | Real-time mode | Latch mode | READ_VIN | ✓ | ✓ | x | READ_VOUT | ✓ | ✓ | x | READ_IOUT | ✓ | ✓ | ✓ | READ_TEMPERATURE | x | ✓ | x | READ_EFFICIENCY | ✓ | x | ✓ | READ_POUT | ✓ | x | ✓ | READ_PIN | ✓ | x | ✓ |
|                  | Average mode | Real-time mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Latch mode |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
| READ_VIN         | ✓            | ✓                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | x          |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
| READ_VOUT        | ✓            | ✓                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | x          |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
| READ_IOUT        | ✓            | ✓                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | ✓          |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
| READ_TEMPERATURE | x            | ✓                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | x          |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
| READ_EFFICIENCY  | ✓            | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | ✓          |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
| READ_POUT        | ✓            | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | ✓          |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
| READ_PIN         | ✓            | x                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | ✓          |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |
| 9:0              | AVE_WINDOW   | Averaging window for reporting. 100μs/LSB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |            |              |                |            |          |   |   |   |           |   |   |   |           |   |   |   |                  |   |   |   |                 |   |   |   |           |   |   |   |          |   |   |   |

**MFR\_PWMVID\_TARGET\_CTRL (AEh)**

This register sets the relationship between the PWM-VID duty and target output voltage.

| Command  | MFR_PWMVID_TARGET_CTRL |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary        |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                     | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                    | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                      | x   | x   | x   | x   |     |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED                 | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 10:9  | TON_PRD_FIL_SEL          | Time constant of the digital low-pass filter for sensing the PWM frequency and on-time used for efficiency calculation.<br><br>00: (500kHz / Fs) x 6ms<br>01: (500kHz / Fs) x 12ms<br>10: (500kHz / Fs) x 24ms<br>11: (500kHz / Fs) x 48ms<br><br>Fs is the configured PWM frequency.                                                                                                                                                                                                                                                                                                                                                                                  |
| 8:6   | DVID_FLAG_DELAY          | Delay time from when DVID completes to when the internal DVID flag resets. 20μs/LSB.<br><br>If the output voltage is in PMBus-controlling mode (VID_CONTROL_MODE = 1), this register is ignored (delay time is zero).                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5     | DUTY_TO_VID_GAIN_MODE    | Gain mode selector for target VID calculation. The target output voltage is calculated by the defined register VOUT_MIN (1Fh), real-time PWM-VID on-time, and a GAIN factor as shown below:<br><br>$\text{VID\_TARGET} = \text{PWMVID\_ON\_TIME} \times \text{GAIN} + \text{VOUT\_MIN}$<br>0: always use the register value from DUTY_TO_VID_GAIN (B3h)<br>1: update the current GAIN by the real-time calculated value when the error between the latest calculated GAIN and the current GAIN exceeds DUTY_TO_VID_GAIN_HYS (but is still within ±10% deviation from the current GAIN). In this case, the register DUTY_TO_VID_GAIN (B3h) is used as the initial GAIN. |
| 4:3   | DUTY_TO_VID_GAIN_FIL_SEL | Averaging window of digital filter for VID_TARGET calculation.<br><br>00: average of four points<br>01: average of eight points<br>10: average of 16 points<br>11: average of 32 points                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 2:0   | DUTY_TO_VID_GAIN_HYS     | Gain hysteresis used to update the current GAIN for the target VID calculation if DUTY_TO_VID_GAIN_SEL = 1. When the error between the latest calculated GAIN and current GAIN exceeds this hysteresis (but is still within the 10% deviation from the current GAIN), the current GAIN is updated by the most-recently calculated one. In this case, the register DUTY_TO_VID_GAIN (B3h) is used as the initial GAIN.                                                                                                                                                                                                                                                  |

**MFR\_PWMVID\_UP\_COMP (AFh)**

This register sets VID compensation for upward DVID.

|          |                    |     |     |     |     |     |     |     |     |     |     |                  |     |     |     |     |
|----------|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------------------|-----|-----|-----|-----|
| Command  | MFR_PWMVID_UP_COMP |     |     |     |     |     |     |     |     |     |     |                  |     |     |     |     |
| Format   | Unsigned binary    |     |     |     |     |     |     |     |     |     |     |                  |     |     |     |     |
| Bit      | 15                 | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4                | 3   | 2   | 1   | 0   |
| Access   | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w              | r/w | r/w | r/w | r/w |
| Function | DVID_UP_CMPN       |     |     |     |     |     |     |     |     |     |     | DVID_UP_END_THRE |     |     |     |     |

| Bits | Bit Name         | Description                                                                                                                                                                                                                                                                                                                                                   |
|------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | DVID_UP_CMPN     | <p>PWM-VID duty compensation value based on the desired compensation step. This bit is added in the detected PWM-VID duty during upward DVID.</p> $DVID\_UP\_CMPN = \frac{VID\_CMPN\_STEP + 2}{VOUT\_MAX - VOUT\_MIN} \times 2^{12}$ <p>VOUT_MAX (24h) and VOUT_MIN (1Fh) are in VID format.</p>                                                              |
| 4    | DVID_UP_CMPN_EN  | <p>Enable bit of the extra VID step for upward DVID.</p> <p>0: disable<br/>1: enable</p>                                                                                                                                                                                                                                                                      |
| 3:0  | DVID_UP_END_THRE | <p>Threshold for the upward DVID ending indicator. During upward DVID, the controller uses the output of the first-stage filter as VO_REF. When the current VO_REF is greater than the calculated VID_TARGET - DVID_UP_END_THRE, this bit switches to the output of second stage filter.</p> <p>DVID_UP_START_THRE must be greater than DVID_UP_END_THRE.</p> |

**MFR\_PWMVID\_MAX\_DUTY (B0h)**

This register sets the PWM-VID on-time threshold used to indicate 100% PWM-VID duty.

|          |                     |     |     |     |     |     |                 |     |     |     |     |     |     |     |     |     |
|----------|---------------------|-----|-----|-----|-----|-----|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Command  | MFR_PWMVID_MAX_DUTY |     |     |     |     |     |                 |     |     |     |     |     |     |     |     |     |
| Format   | Unsigned binary     |     |     |     |     |     |                 |     |     |     |     |     |     |     |     |     |
| Bit      | 15                  | 14  | 13  | 12  | 11  | 10  | 9               | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                 | r/w | r/w | r/w | r/w | r/w | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                   | x   | x   | x   | x   | x   | PWMVID_MAX_DUTY |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name              | Description                                                                                                                                                                                        |
|-------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED              | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                  |
| 9:1   | PWMVID_MAX_DUTY       | PWM-VID on-time threshold to indicate 100% PWM-VID duty. When the detected PWM-VID on time is greater than this threshold, the controller considers the current PWM-VID duty to be 100%. 10ns/LSB. |
| 0     | PWMVID_HIGHLOW_DET_EN | <p>Enable bit for PWM-VID constant high/low detection.</p> <p>0: disable<br/>1: enable</p>                                                                                                         |

**MFR\_PWMVID\_FLTR\_CTRL1 (B1h)**

This register sets the performance of the digital PWM-VID filters.

|          |                       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Command  | MFR_PWMVID_FLTR_CTRL1 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Format   | Unsigned binary       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                    | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                   | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |                       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name             | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | DVID_DOWN_START_THRE | Threshold for the downward DVID starting indicator (DVID_TRIG_MODE = 0). When V <sub>OUT</sub> is settled, the controller uses the output of the second-stage filter as VO_REF. When the calculated VID_TARGET is less than the current VO_REF - DVID_DOWN_START_THRE, the controller enters the downward DVID, and VO_REF switches to the first-stage filter output.<br><br>DVID_DOWN_START_THRE must be greater than DVID_DOWN_END_THRE. |
| 12:10 | DVID_UP_START_THRE   | Threshold for the upward DVID starting indicator (DVID_TRIG_MODE = 0). When V <sub>OUT</sub> is settled, the controller uses the output of the second-stage filter as VO_REF. When the calculated VID_TARGET is greater than the current VO_REF + DVID_UP_START_THRE, the controller enters the upward DVID, and VO_REF switches to the output of the first-stage filter.<br><br>DVID_UP_START_THRE must be greater than DVID_UP_END_THRE. |
| 9:7   | DVID_DOWN_END_THRE   | Threshold for the downward DVID ending indicator. During the downward DVID, the controller uses the output of the first-stage filter as VO_REF. When the current VO_REF is less than the calculated VID_TARGET + DVID_DOWN_END_THRE, this bit switches to the output of the second-stage filter.<br><br>DVID_DOWN_START_THRE must be greater than DVID_DOWN_END_THRE.                                                                      |
| 6:2   | FILT2_CHECK_TIME     | Check time of the synchronizing function of the second-stage PWM-VID filter to improve output voltage accuracy after DVID. 100µs/LSB.<br><br>The second-stage PWM-VID filter uses an internal hysteresis module to avoid jitter on its output. When the output remains unchanged for this checking time, the hysteresis module synchronizes its output with the input to eliminate small DC errors.                                        |
| 1:0   | SECOND_FIL_AVE       | Averaging window of the second-stage PWM-VID filter.<br><br>00: average of 512 points<br>01: average of 1024 points<br>10: average of 2048 points<br>11: average of 4056 points                                                                                                                                                                                                                                                            |

**MFR\_PWMVID\_FLTR\_CTRL2 (B2h)**

This register sets the performance of the digital PWM-VID filters.

| Command  | MFR_PWMVID_FLTR_CTRL2 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                    | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                   | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |                       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | DVID_TRIG_MODE    | DVID trigger mode selector.<br>0: according to the relationship between the calculated VID_TARGET and current VO_REF<br>1: according to whether the real-time counted PWM-VID on-time changes more than the threshold set in bit[5:3] or bit[2:0]                                                                                                                                                                    |
| 14    | FILT2_SYNC_EN     | Enable bit for the synchronizing function of the second stage PWM-VID filter to improve output voltage accuracy after DVID.<br>0: disable<br>1: enable<br><br>The second stage PWM-VID filter uses an internal hysteresis module to avoid jitter on its output. When the output remains unchanged for this checking time, the hysteresis module synchronizes its output with the input to eliminate small DC errors. |
| 13:10 | DVID_DOWN_THRE    | DVID direction identification threshold for downward DVID. When the current VO_REF is greater than VID_TARGET + DVID_DOWN_THRE, the controller considers the DVID to be downward.                                                                                                                                                                                                                                    |
| 9:6   | DVID_UP_THRE      | DVID direction identification threshold for upward DVID. When the current VO_REF is less than VID_TARGET - DVID_UP_THRE, the controller considers the DVID to be upward.                                                                                                                                                                                                                                             |
| 5:3   | TON_CHANGE_THRE_N | Threshold for the downward DVID starting indicator (DVID_TRIG_MODE = 1). When V <sub>OUT</sub> is settled, the controller uses the output of the second stage filter as VO_REF. When the detected on-time negative variation of PWM-VID is greater than TON_CHANGE_THRE_N, the controller enters downward DVID, and VO_REF switches to the first- stage filter output. 5ns/LSB.                                      |
| 2:0   | TON_CHANGE_THRE_P | Threshold for the upward DVID starting indicator (DVID_TRIG_MODE = 1). When V <sub>OUT</sub> is settled, the controller uses the output of the second-stage filter as VO_REF. When the detected on-time positive variation of PWM-VID is greater than TON_CHANGE_THRE_P, the controller enters upward DVID, and VO_REF switches to the first-stage filter output. 5ns/LSB.                                           |

**MFR\_DUTY\_TO\_VID\_GAIN (B3h)**

This register is the initial parameter for the target voltage calculation.

| Command  | MFR_DUTY_TO_VID_GAIN |     |     |     |     |                  |     |     |     |     |     |     |     |     |     |     |
|----------|----------------------|-----|-----|-----|-----|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary      |     |     |     |     |                  |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                   | 14  | 13  | 12  | 11  | 10               | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                  | r/w | r/w | r/w | r/w | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                    | x   | x   | x   | x   | DUTY_TO_VID_GAIN |     |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED         | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 10:0  | DUTY_TO_VID_GAIN | <p>Initial parameter for the VID_TARGET calculation. It is calculated according to the period of PWM-VID, VOUT_MAX, and VOUT_MIN:</p> $\text{DUTY\_TO\_VID\_GAIN} = \frac{\text{VOUT\_MAX} - \text{VOUT\_MIN}}{\text{PWM\_VID\_PERIOD}(\text{ns})/5(\text{ns})} \times 2^9$ <p>VOUT_MAX (24h) and VOUT_MIN (1Fh) are in VID format.</p> <p>VID_TARGET is calculated by defined the register VOUT_MIN (1Fh), real-time PWM-VID on-time, and DUTY_ADC sense of VDIFF, and VFB TO_VID_GAIN:</p> $\text{VID\_TARGET} = \text{PWM\_VID\_ON\_TIME} \times \text{DUTY\_TO\_VID\_GAIN} + \text{VOUT\_MIN}$ |

**MFR\_PARM\_VOUT\_MIN (B4h)**

This register is a parameter corresponding to VOUT\_MIN.

| Command  | MFR_PARM_VOUT_MIN |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w               | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | PARAM_VOUT_MIN    |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name       | Description                                                                                                                                                                                                      |
|------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | PARAM_VOUT_MIN | <p>The parameter corresponds to VOUT_MIN:</p> $\text{PARAM\_VOUT\_MIN} = \frac{\text{VOUT\_MIN}}{\text{VOUT\_MAX} - \text{VOUT\_MIN}} \times 2^{11}$ <p>VOUT_MAX (24h) and VOUT_MIN (1Fh) are in VID format.</p> |

**MFR\_PARM\_RC\_CONST (B5h)**

This register is the parameter corresponding to the desired output voltage slew rate during boot-up and DVID.

| Command  | MFR_PARM_RC_CONST |     |     |     |         |     |     |     |     |     |         |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|---------|-----|-----|-----|-----|-----|---------|-----|-----|-----|-----|-----|
| Format   | Unsigned binary   |     |     |     |         |     |     |     |     |     |         |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11      | 10  | 9   | 8   | 7   | 6   | 5       | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w               | r/w | r/w | r/w | r/w     | r/w | r/w | r/w | r/w | r/w | r/w     | r/w | r/w | r/w | r/w | r/w |
| Function | x                 | x   | x   | x   | BOOT_RC |     |     |     |     |     | DVID_RC |     |     |     |     |     |

| Bits  | Bit Name | Description                                                                                                                                                                                                                                                                                               |
|-------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                         |
| 11:6  | BOOT_RC  | <p>The parameter corresponds to the desired time constant of the PWM-VID low-pass filter in the boot-up process:</p> $BOOT\_RC = \frac{320(ns)}{\tau_{BOOT}(ns)} \times 2^{11}$ <p>Where <math>\tau_{BOOT}</math> is the desired time constant of the PWM-VID low-pass filter in the boot-up process.</p> |
| 5:0   | DVID_RC  | <p>The parameter corresponds to the desired time constant of the PWM-VID low-pass filter in the DVID process:</p> $DVID\_RC = \frac{320(ns)}{\tau_{DVID}(ns)} \times 2^{11}$ <p>Where <math>\tau_{DVID}</math> is the desired time constant of the PWM-VID low-pass filter in the DVID process.</p>       |

### MFR\_PARM\_VBOOT\_DUTY (B6h)

This register is the parameter corresponding to desired  $V_{BOOT}$  for PWM-VID mode.

| Command  | MFR_PARM_VBOOT_DUTY |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                 | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | VBOOT_DUTY          |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name   | Description                                                                                                                                                                                                                                                                |
|------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | VBOOT_DUTY | <p>The parameter corresponds to the desired <math>V_{BOOT}</math>:</p> $VBOOT\_DUTY = \frac{VBOOT-VOUT\_MIN}{VOUT\_MAX-VOUT\_MIN} \times 2^{16}$ <p><math>V_{BOOT}</math> (BBh), <math>VOUT\_MAX</math> (24h), and <math>VOUT\_MIN</math> (1Fh) are all in VID format.</p> |

### MFR\_PARM\_SLEW\_TRAN (B7h)

This register is the parameter corresponding to DVID\_RC in MFR\_PARM\_RC\_CONST (B5h).

| Command  | MFR_PARM_SLEW_TRAN |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary    |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                 | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | DVID_RC_PARM       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name     | Description                                                                                                                                                                                                                                          |
|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | DVID_RC_PARM | <p>The parameter corresponds to DVID_RC in MFR_PARM_RC_CONST (B5h):</p> $DVID\_RC\_PARM = \frac{1}{DVID\_RC \times (VOUT\_MAX-VOUT\_MIN)} \times 2^{24}$ <p><math>VOUT\_MAX</math> (24h) and <math>VOUT\_MIN</math> (1Fh) are all in VID format.</p> |

**MFR\_PARM\_BOOT\_TRAN (B8h)**

This register is the parameter corresponding to BOOT\_RC in MFR\_PARM\_RC\_CONST (B5h).

| Command  | MFR_PARM_BOOT_TRAN |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary    |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                 | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | BOOT_RC_PARM       |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name     | Description                                                                                                                                                                                                                                            |
|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | BOOT_RC_PARM | <p>The parameter corresponds to BOOT_RC in MFR_PARM_RC_CONST (B5h):</p> $\text{BOOT\_RC\_PARM} = \frac{1}{\text{BOOT\_RC} \times (\text{VOUT\_MAX} - \text{VOUT\_MIN})} \times 2^{24}$ <p>VOUT_MAX (24h) and VOUT_MIN (1Fh) are all in VID format.</p> |

**MFR\_BOOT\_SR (B9h)**

This register sets the output voltage slew rate for linear boot-up.

| Command  | MFR_BOOT_SR     |     |     |     |     |     |                    |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |                    |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9                  | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | LINEAR_BOOT_SR_CNT |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name           | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:0  | LINEAR_BOOT_SR_CNT | <p>Sets the linear boot-up slew rate.</p> $\text{LINEAR\_BOOT\_SR\_CNT} = \frac{6.25\text{mV}}{\text{SR}_{\text{BOOT}} \times 50\text{ns}}$ <p>Bit[0] of MFR_VR_CONFIG2 (E2h) sets the boot-up and DVID mode.<br/>           VO_SR_MODE_SEL= 0: linear mode<br/>           VO_SR_MODE_SEL= 1: R-C filter mode</p> <p>Set LINEAR_BOOT_SR_CNT to 0002h when VO_SR_MODE_SEL= 1 (R-C filter mode).</p> |

**MFR\_SLEW\_SR (BAh)**

This register sets the output voltage slew rate for linear DVID.

| Command  | MFR_SLEW_SR     |     |     |     |     |     |                    |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |                    |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9                  | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | LINEAR_DVID_SR_CNT |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name           | Description                                                                                                                                                                                                                                                                                                                                                                  |
|------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:0  | LINEAR_DVID_SR_CNT | <p>Sets the linear DVID slew rate.</p> $\text{LINEAR\_DVID\_SR\_CNT} = \frac{6.25\text{mV}}{\text{SR}_{\text{DVID}} \times 50\text{ns}}$ <p>Bit[0] of MFR_VR_CONFIG2 (E2h) sets the boot-up and DVID mode.</p> <p>VO_SR_MODE_SEL= 0: linear mode<br/>VO_SR_MODE_SEL= 1: R-C filter mode</p> <p>Set LINEAR_DVID_SR_CNT to 0002h when VO_SR_MODE_SEL= 1 (R-C filter mode).</p> |

### MFR\_VBOOT (BBh)

This register is used to set boot voltage for PWM-VID mode. It is in VID format.

| Command  | MFR_VBOOT |     |     |     |     |     |     |       |     |     |     |     |     |     |     |     |
|----------|-----------|-----|-----|-----|-----|-----|-----|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | VID       |     |     |     |     |     |     |       |     |     |     |     |     |     |     |     |
| Bit      | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8     | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w       | r/w | r/w | r/w | r/w | r/w | r/w | r/w   | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x         | x   | x   | x   | x   | x   | x   | VBOOT |     |     |     |     |     |     |     |     |

| Bits | Bit Name | Description                                                       |
|------|----------|-------------------------------------------------------------------|
| 15:9 | RESERVED | Unused. X indicates that writes are ignored and always read as 0. |
| 8:0  | VBOOT    | Boot voltage for PWM-VID mode. 6.25mV/LSB.                        |

### MFR\_VID\_SD (BCh)

This register sets the VID threshold to set all PWMs to tri-state during soft shutdown or the DVID-to-zero process.

| Command  | MFR_VID_SD |     |     |     |     |     |     |               |     |     |     |     |     |     |     |     |
|----------|------------|-----|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | VID        |     |     |     |     |     |     |               |     |     |     |     |     |     |     |     |
| Bit      | 15         | 14  | 13  | 12  | 11  | 10  | 9   | 8             | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w        | r/w | r/w | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x          | x   | x   | x   | x   | x   | x   | VID_SHUT_DOWN |     |     |     |     |     |     |     |     |

| Bits | Bit Name      | Description                                                                                              |
|------|---------------|----------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED      | Unused. X indicates that writes are ignored and always read as 0.                                        |
| 8:0  | VID_SHUT_DOWN | VID threshold to set all PWMs to tri-state during soft shutdown or the DVID-to-zero process. 6.25mV/LSB. |

### MFR\_FS (BDh)

This register sets the PWM frequency.

| Command  | MFR_FS |     |     |     |     |     |     |        |     |     |     |     |     |     |     |     |
|----------|--------|-----|-----|-----|-----|-----|-----|--------|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | VID    |     |     |     |     |     |     |        |     |     |     |     |     |     |     |     |
| Bit      | 15     | 14  | 13  | 12  | 11  | 10  | 9   | 8      | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w    | r/w | r/w | r/w | r/w | r/w | r/w | r/w    | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x      | x   | x   | x   | x   | x   | x   | MFR_FS |     |     |     |     |     |     |     |     |

| Bits | Bit Name | Description                                                       |
|------|----------|-------------------------------------------------------------------|
| 15:9 | RESERVED | Unused. X indicates that writes are ignored and always read as 0. |
| 8:0  | MFR_FS   | 10kHz/LSB.                                                        |

### MFR\_PMBUS\_ADDR (BEh)

This register sets the PMBus address for the controller.

| Command  | MFR_PMBUS_ADDR  |          |     |     |          |     |     |     |
|----------|-----------------|----------|-----|-----|----------|-----|-----|-----|
| Format   | Unsigned binary |          |     |     |          |     |     |     |
| Bit      | 7               | 6        | 5   | 4   | 3        | 2   | 1   | 0   |
| Access   | r/w             | r/w      | r/w | r/w | r/w      | r/w | r/w | r/w |
| Function | MODE            | ADDR_MSB |     |     | ADDR_LSB |     |     |     |

| Bits | Bit Name      | Description                                                     |
|------|---------------|-----------------------------------------------------------------|
| 7    | ADDR_LSB_MODE | ADDR_LSB mode selector.<br>0: set by ADDR<br>1: set by register |
| 6:4  | ADDR_MSB      | MSB of address.                                                 |
| 3:0  | ADDR_LSB      | LSB of address.                                                 |

### MFR\_VIN\_SENSE\_OFFSET (BFh)

This register sets input voltage sensing offset and input power loss calibrating parameter.

| Command  | MFR_VIN_SENSE_OFFSET |     |     |     |     |     |     |     |                  |     |     |     |     |     |     |     |
|----------|----------------------|-----|-----|-----|-----|-----|-----|-----|------------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary      |     |     |     |     |     |     |     |                  |     |     |     |     |     |     |     |
| Bit      | 15                   | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7                | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                  | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | PWR_LOSS_OFFSET      |     |     |     |     |     |     |     | VIN_SENSE_OFFSET |     |     |     |     |     |     |     |

| Bits | Bit Name         | Description                                                                                                                                                                                                                                                                                                                       |
|------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | PWR_LOSS_OFFSET  | Power loss offset for the input power report and efficiency calculation.<br>0.5W/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>1W/LSB (TOTAL_CURRENT_RESOLUTION = 1)                                                                                                                                                                      |
| 7:0  | VIN_SENSE_OFFSET | Input voltage sensing offset:<br>$ V_{in\_offset}  = \frac{1.6 \times VIN\_SENSE\_OFFSET \times (R_{TOP} + R_{BOTTOM})}{1024 \times R_{BOTTOM}}$ Where $V_{in\_offset}$ is the target offset on the input voltage sensing, $R_{TOP}$ and $R_{BOTTOM}$ are the resistor divider for input voltage sensing, bit[7] is the sign bit. |

### MFR\_VIN\_SCALE\_LOOP (C0h)

This register sets the ratio of the resistor divider for the input voltage sensing.

| Command  | MFR_VIN_SCALE_LOOP |     |     |     |     |     |     |     |
|----------|--------------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary    |     |     |     |     |     |     |     |
| Bit      | 7                  | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | VIN_SENSE_SCALE    |     |     |     |     |     |     |     |

| Bits | Bit Name        | Description                                                                                                                                                                                                          |
|------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | VIN_SENSE_SCALE | Parameter used to set the input voltage sensing scale.<br>$\text{VIN\_SENSE\_SCALE} = \frac{1024 \times V_{\text{INSEN}}}{V_{\text{IN}}} = \frac{1024 \times R_{\text{BOTTOM}}}{R_{\text{TOP}} + R_{\text{BOTTOM}}}$ |

### MFR\_TEMP\_GAIN\_OFFSET (C1h)

This register sets the gain and offset for temperature sensing via VTEMP.

| Command  | MFR_TEMP_GAIN_OFFSET |              |     |     |     |     |     |     |            |     |     |     |     |     |     |     |
|----------|----------------------|--------------|-----|-----|-----|-----|-----|-----|------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary      |              |     |     |     |     |     |     |            |     |     |     |     |     |     |     |
| Bit      | 15                   | 14           | 13  | 12  | 11  | 10  | 9   | 8   | 7          | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w                  | r/w          | r/w | r/w | r/w | r/w | r/w | r/w | r/w        | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                    | VTEMP_OFFSET |     |     |     |     |     |     | VTEMP_GAIN |     |     |     |     |     |     |     |

| Bits | Bit Name     | Description                                                                                                                                                                                                                                                                                                                    |
|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED     | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                              |
| 14:8 | VTEMP_OFFSET | Offset used to report the temperature from VTEMP:<br>$\text{VTEMP\_OFFSET} = \frac{\text{DrMOS\_TEMP\_OFFSET}}{\text{DrMOS\_TEMP\_GAIN}}$<br>Assuming that:<br>$\text{VTEMP} = \text{DrMOS\_TEMP\_GAIN} \times \text{Temperature} - \text{DrMOS\_TEMP\_OFFSET}$                                                                |
| 7:0  | VTEMP_GAIN   | Gain used to report the temperature from VTEMP. VTEMP has an internal 1/2 divider before ADC:<br>$\text{VTEMP\_GAIN} = \frac{2 \times 1.6 \times 2^9 \times 1000}{\text{DrMOS\_TEMP\_GAIN} \times 1024}$<br>Assuming that:<br>$\text{VTEMP} = \text{DrMOS\_TEMP\_GAIN} \times \text{Temperature} - \text{DrMOS\_TEMP\_OFFSET}$ |

### MFR\_CUR\_GAIN (C2h)

This register sets the gain for phase-current sensing.

| Command  | MFR_CUR_GAIN    |     |     |     |     |     |                |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |                |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9              | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | PHASE_CUR_GAIN |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                         |
| 9:0   | PHASE_CUR_GAIN | Gain for phase-current sensing.<br>$\text{PHASE\_CUR\_GAIN} = K_{\text{CS}} \times R_{\text{CS}} \times 2^{13} \quad (\text{PHASE\_CURRENT\_RESOLUTION} = 0)$<br>$\text{PHASE\_CUR\_GAIN} = K_{\text{CS}} \times R_{\text{CS}} \times 2^{14} \quad (\text{PHASE\_CURRENT\_RESOLUTION} = 1)$<br>Where $R_{\text{CS}}$ is the phase-current sensing resistor, and $K_{\text{CS}}$ is the current sensing gain of the DrMOS. |

### MFR\_BLANK\_TIME (C5h)

This register sets the minimum interval time between consecutive phases' PWM rising edges and the discharging time of slope compensation capacitors.

| Command  | MFR_BLANK_TIME  |     |     |     |                  |     |     |     |     |     |                  |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|------------------|-----|-----|-----|-----|-----|------------------|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |                  |     |     |     |     |     |                  |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11               | 10  | 9   | 8   | 7   | 6   | 5                | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w              | r/w | r/w | r/w | r/w | r/w | r/w              | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | SLOPE_BLANK_TIME |     |     |     |     |     | PHASE_BLANK_TIME |     |     |     |     |     |

| Bits  | Bit Name         | Description                                                                                                                                    |
|-------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED         | Unused. X indicates that writes are ignored and always read as 0.                                                                              |
| 11:6  | SLOPE_BLANK_TIME | Discharging time of slope compensation capacitors. 5ns/LSB.<br>SLOPE_BLANK_TIME <i>must</i> be less than or equal to PHASE_BLANK_TIME.         |
| 5:0   | PHASE_BLANK_TIME | Minimum interval time between consecutive phases' PWM rising edges. 5ns/LSB.<br>PHASE_BLANK_TIME <i>must</i> be greater than SLOPE_BLANK_TIME. |

### MFR\_SLOPE\_SR\_DCM (C6h)

This register sets the slew rate of slope compensation for 1-phase DCM.

| Command  | MFR_SLOPE_SR_DCM |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5              | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | x   | x   | x   | x   | CURRENT_SOURCE |     |     |     |     |     |

| Bits | Bit Name       | Description                                                       |
|------|----------------|-------------------------------------------------------------------|
| 15:6 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 5:0  | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (23):

$$V_{\text{SLOPE@DCM}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{16 \times 1.85(\text{pF})} \times (T_{\text{SW}} - T_{\text{BLANK}}) \quad (23)$$

Where  $V_{\text{SLOPE@DCM}}$  is the desired voltage of slope compensation for 1-phase DCM,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

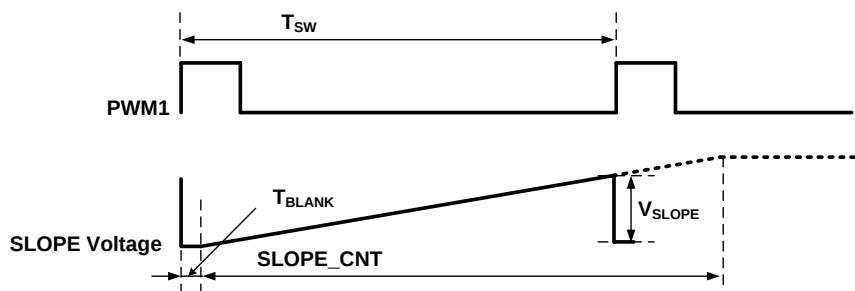
If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

**MFR\_SLOPE\_CNT\_DCM (C7h)**

This register sets the maximum ramping time of slope compensation for 1-phase DCM. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_DCM |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|-----|-----|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary   |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11  | 10  | 9         | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w               | r/w | r/w | r/w | r/w | r/w | r/w       | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                 | x   | x   | x   | x   | x   | SLOPE_CNT |     |     |     |     |     |     |     |     |     |

| Bits  | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                |
|-------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                          |
| 9:0   | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 1-phase DCM. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times (T_{\text{SW}} - T_{\text{BLANK}})(\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register MFR_FS (BDh), and <math>T_{\text{BLANK}}</math> is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h).</p> |



**Figure 22: Slope Compensation for 1-Phase DCM**

**MFR\_SLOPE\_SR\_10P (C8h)**

This register sets the slew rate of slope compensation for 10-phase status.

| Command  | MFR_SLOPE_SR_10P |     |     |     |     |     |     |     |     |     |     |                |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |     |     |     |     |     |                |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4              | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | x   | CAP |     |     |     | CURRENT_SOURCE |     |     |     |     |

| Bits | Bit Name       | Description                                                       |
|------|----------------|-------------------------------------------------------------------|
| 15:9 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 8:6  | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.               |
| 5:0  | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (24):

$$V_{\text{SLOPE@10P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(8 - \text{CAP}) \times 1.85(\text{pF})} \times \left( \frac{T_{\text{SW}}}{10} - T_{\text{BLANK}} \right) \quad (24)$$

Where  $V_{\text{SLOPE@10P}}$  is the desired voltage of slope compensation for 10-phase,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### MFR\_SLOPE\_CNT\_10P (C9h)

This register sets the maximum ramping time of slope compensation for 10-phase status. Once the timer ends, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_10P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w               | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                 | x   | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                                             |
|------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                       |
| 7:0  | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 10-phase status. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times \left( \frac{T_{\text{SW}}}{10} - T_{\text{BLANK}} \right) (\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register MFR_FS (BDh), and <math>T_{\text{BLANK}}</math> is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h).</p> |

### MFR\_SLOPE\_SR\_9P (CAh)

This register sets the slew rate of slope compensation for 9-phase status.

| Command  | MFR_SLOPE_SR_9P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name       | Description                                                       |
|------|----------------|-------------------------------------------------------------------|
| 15:9 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 8:6  | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.               |
| 5:0  | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (25):

$$V_{\text{SLOPE@9P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(8 - \text{CAP}) \times 1.85(\text{pF})} \times \left( \frac{T_{\text{SW}}}{9} - T_{\text{BLANK}} \right) \quad (25)$$

Where  $V_{\text{SLOPE@9P}}$  is the desired voltage of slope compensation for 9-phase status,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### MFR\_SLOPE\_CNT\_9P (CBh)

This register sets the maximum ramping time of slope compensation for 9-phase status. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_9P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                     |
| 7:0  | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 9-phase status. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times \left( \frac{T_{\text{SW}}}{9} - T_{\text{BLANK}} \right) (\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register MFR_FS (BDh), and <math>T_{\text{BLANK}}</math> is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h).</p> |

### MFR\_SLOPE\_SR\_8P (CCh)

This register sets the slew rate of slope compensation for 8-phase status.

| Command  | MFR_SLOPE_SR_8P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name       | Description                                                       |
|------|----------------|-------------------------------------------------------------------|
| 15:9 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 8:6  | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.               |
| 5:0  | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (26):

$$V_{\text{SLOPE@8P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(8 - \text{CAP}) \times 1.85(\text{pF})} \times \left( \frac{T_{\text{SW}}}{8} - T_{\text{BLANK}} \right) \quad (26)$$

Where  $V_{\text{SLOPE@8P}}$  is the desired voltage of slope compensation for 8-phase status,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### MFR\_SLOPE\_CNT\_8P (CDh)

This register sets the maximum ramping time of slope compensation for 8-phase status. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_8P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |

SLOPE\_CNT

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                     |
| 7:0  | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 8-phase status. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times \left( \frac{T_{\text{SW}}}{8} - T_{\text{BLANK}} \right) (\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register MFR_FS (BDh), and <math>T_{\text{BLANK}}</math> is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h).</p> |

### MFR\_SLOPE\_SR\_7P (CEh)

This register sets the slew rate of slope compensation for 7-phase status.

| Command  | MFR_SLOPE_SR_7P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |     |

CAP

CURRENT\_SOURCE

| Bits | Bit Name       | Description                                                       |
|------|----------------|-------------------------------------------------------------------|
| 15:9 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 8:6  | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.               |
| 5:0  | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (27):

$$V_{\text{SLOPE@7P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(8 - \text{CAP}) \times 1.85(\text{pF})} \times \left( \frac{T_{\text{SW}}}{7} - T_{\text{BLANK}} \right) \quad (27)$$

Where  $V_{\text{SLOPE@7P}}$  is the desired voltage of slope compensation for 7-phase status,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### MFR\_SLOPE\_CNT\_7P (CFh)

This register sets the maximum ramping time of slope compensation for 7-phase status. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_7P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |

SLOPE\_CNT

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                     |
| 7:0  | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 7-phase status. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times \left( \frac{T_{\text{SW}}}{7} - T_{\text{BLANK}} \right) (\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register MFR_FS (BDh), and <math>T_{\text{BLANK}}</math> is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h).</p> |

### MFR\_SLOPE\_SR\_6P (D0h)

This register sets the slew rate of slope compensation for 6-phase status.

| Command  | MFR_SLOPE_SR_6P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |     |

CAP

CURRENT\_SOURCE

| Bits | Bit Name       | Description                                                       |
|------|----------------|-------------------------------------------------------------------|
| 15:9 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 8:6  | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.               |
| 5:0  | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (28):

$$V_{\text{SLOPE@6P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(8 - \text{CAP}) \times 1.85(\text{pF})} \times \left( \frac{T_{\text{SW}}}{6} - T_{\text{BLANK}} \right) \quad (28)$$

Where  $V_{\text{SLOPE@6P}}$  is the desired slope compensation voltage for 6-phase status,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### MFR\_SLOPE\_CNT\_6P (D1h)

This register sets the maximum slope compensation ramping time for 6-phase status. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_6P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |

SLOPE\_CNT

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                                       |
|------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                 |
| 7:0  | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 6-phase status. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times \left( \frac{T_{\text{SW}}}{6} - T_{\text{BLANK}} \right) (\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register MFR_FS (BDh), <math>T_{\text{BLANK}}</math> is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h).</p> |

### MFR\_SLOPE\_SR\_5P (D2h)

This register sets the slope compensation slew rate for 5-phase status.

| Command  | MFR_SLOPE_SR_5P |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | x   |     |     |     |     |     |     |     |     |     |

CAP

CURRENT\_SOURCE

| Bits | Bit Name       | Description                                                    |
|------|----------------|----------------------------------------------------------------|
| 15:9 | RESERVED       | Unused. X indicates writes are ignored and always reads are 0. |
| 8:6  | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.            |
| 5:0  | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.       |

Calculate the slope compensation slew rate with Equation (29):

$$V_{\text{SLOPE@5P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(8 - \text{CAP}) \times 1.85(\text{pF})} \times \left( \frac{T_{\text{SW}}}{5} - T_{\text{BLANK}} \right) \quad (29)$$

Where  $V_{\text{SLOPE@5P}}$  is the desired slope compensation voltage for 5-phase status,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### MFR\_SLOPE\_CNT\_5P (D3h)

This register sets the maximum slope compensation ramping time for 5-phase status. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_5P |     |     |     |     |     |     |           |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----------|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |     |           |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8         | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w       | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | x   | SLOPE_CNT |     |     |     |     |     |     |     |     |

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                     |
| 7:0  | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 5-phase status. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times \left( \frac{T_{\text{SW}}}{5} - T_{\text{BLANK}} \right) (\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register MFR_FS (BDh), and <math>T_{\text{BLANK}}</math> is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h).</p> |

### MFR\_SLOPE\_SR\_4P (D4h)

This register sets the slope compensation slew rate for 4-phase status.

| Command  | MFR_SLOPE_SR_4P |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5              | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | x   | CAP |     |     | CURRENT_SOURCE |     |     |     |     |     |

| Bits | Bit Name       | Description                                                       |
|------|----------------|-------------------------------------------------------------------|
| 15:9 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 8:6  | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.               |
| 5:0  | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (30):

$$V_{\text{SLOPE@4P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(8 - \text{CAP}) \times 1.85(\text{pF})} \times \left( \frac{T_{\text{SW}}}{4} - T_{\text{BLANK}} \right) \quad (30)$$

Where  $V_{\text{SLOPE@4P}}$  is the desired slope compensation voltage for 4-phase status,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### MFR\_SLOPE\_CNT\_4P (D5h)

This register sets the maximum slope compensation ramping time for 4-phase status. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_4P |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9         | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w       | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | SLOPE_CNT |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                     |
| 7:0  | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 4-phase status. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times \left( \frac{T_{\text{SW}}}{4} - T_{\text{BLANK}} \right) (\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register MFR_FS (BDh), and <math>T_{\text{BLANK}}</math> is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h).</p> |

### MFR\_SLOPE\_SR\_3P (D6h)

This register sets the slope compensation slew rate for 3-phase status.

| Command  | MFR_SLOPE_SR_3P |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5              | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | CAP |     |     |     | CURRENT_SOURCE |     |     |     |     |     |

| Bits  | Bit Name       | Description                                                       |
|-------|----------------|-------------------------------------------------------------------|
| 15:10 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 9:6   | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.               |
| 5:0   | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (31):

$$V_{\text{SLOPE@3P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(16 - \text{CAP}) \times 1.85(\text{pF})} \times \left( \frac{T_{\text{SW}}}{3} - T_{\text{BLANK}} \right) \quad (31)$$

Where  $V_{\text{SLOPE@3P}}$  is the desired slope compensation voltage for 3-phase status,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### MFR\_SLOPE\_CNT\_3P (D7h)

This register sets the maximum slope compensation ramping time for 3-phase status. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_3P |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9         | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w       | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | SLOPE_CNT |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                     |
| 7:0  | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 3-phase status. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times \left( \frac{T_{\text{SW}}}{3} - T_{\text{BLANK}} \right) (\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register MFR_FS (BDh), and <math>T_{\text{BLANK}}</math> is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h).</p> |

### MFR\_SLOPE\_SR\_2P (D8h)

This register sets the slope compensation slew rate for 2-phase status.

| Command  | MFR_SLOPE_SR_2P |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5              | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | CAP |     |     |     | CURRENT_SOURCE |     |     |     |     |     |

| Bits  | Bit Name       | Description                                                       |
|-------|----------------|-------------------------------------------------------------------|
| 15:10 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 9:6   | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.               |
| 5:0   | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (32):

$$V_{\text{SLOPE@2P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(16 - \text{CAP}) \times 1.85(\text{pF})} \times \left( \frac{T_{\text{SW}}}{2} - T_{\text{BLANK}} \right) \quad (32)$$

Where  $V_{\text{SLOPE@2P}}$  is the desired slope compensation voltage for 2-phase status,  $T_{\text{SW}}$  is the PWM period determined by register **MFR\_FS** (BDh),  $T_{\text{BLANK}}$  is **SLOPE\_BLANK\_TIME** set in register **MFR\_BLANK\_TIME** (C5h).

If setting **VDIFF\_GAIN\_SEL** (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### **MFR\_SLOPE\_CNT\_2P (D9h)**

This register sets the maximum slope compensation ramping time for 2-phase status. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_2P |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9         | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w       | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | SLOPE_CNT |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                          |
| 7:0  | SLOPE_CNT | <p>Maximum ramping time of slope compensation for 2-phase status. 5ns/LSB.</p> $\text{SLOPE\_CNT} = \frac{1.3 \times \left( \frac{T_{\text{SW}}}{2} - T_{\text{BLANK}} \right) (\text{ns})}{5(\text{ns})}$ <p>Where <math>T_{\text{SW}}</math> is the PWM period determined by register <b>MFR_FS</b> (BDh), and <math>T_{\text{BLANK}}</math> is <b>SLOPE_BLANK_TIME</b> set in register <b>MFR_BLANK_TIME</b> (C5h).</p> |

### **MFR\_SLOPE\_SR\_1P (DAh)**

This register sets the slope compensation slew rate for 1-phase CCM status.

| Command  | MFR_SLOPE_SR_1P |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |                |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5              | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | x   | x   | x   |     | CURRENT_SOURCE |     |     |     |     |     |

| Bits | Bit Name       | Description                                                       |
|------|----------------|-------------------------------------------------------------------|
| 15:7 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0. |
| 6    | CAP            | Capacitor value for slope compensation. 1.85pF/LSB.               |
| 5:0  | CURRENT_SOURCE | Current source value for slope compensation. 0.25μA/LSB.          |

Calculate the slope compensation slew rate with Equation (33):

$$V_{\text{SLOPE@1P}} = \frac{0.25(\mu\text{A}) \times \text{CURRENT\_SOURCE}}{(16 - \text{CAP}) \times 1.85(\text{pF})} \times (T_{\text{SW}} - T_{\text{BLANK}}) \quad (33)$$

Where  $V_{\text{SLOPE@1P}}$  is desired slope compensation voltage for 1-phase CCM status,  $T_{\text{SW}}$  is the PWM period determined by register MFR\_FS (BDh), and  $T_{\text{BLANK}}$  is SLOPE\_BLANK\_TIME set in register MFR\_BLANK\_TIME (C5h).

If setting VDIFF\_GAIN\_SEL (2Ah) = 1 to get a half gain for the remote sense amplifier,  $V_{\text{SLOPE}}$  should be doubled.

### MFR\_SLOPE\_CNT\_1P (DBh)

This register sets the maximum slope compensation ramping time for 1-phase CCM status. Once the timer is over, the current source turns off, and the slope compensation voltage is held.

| Command  | MFR_SLOPE_CNT_1P |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |           |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9         | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w       | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   | x   | x   | x   | SLOPE_CNT |     |     |     |     |     |     |     |     |     |

| Bits | Bit Name  | Description                                                                                                                                                                                                                                                                                                                                      |
|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                |
| 7:0  | SLOPE_CNT | Maximum ramping time of slope compensation for 1-phase CCM status. 5ns/LSB.<br>$\text{SLOPE\_CNT} = \frac{1.3 \times (T_{\text{SW}} - T_{\text{BLANK}})(\text{ns})}{5(\text{ns})}$ Where $T_{\text{SW}}$ is the PWM period determined by register MFR_FS (BDh), and $T_{\text{BLANK}}$ is SLOPE_BLANK_TIME set in register MFR_BLANK_TIME (C5h). |

### MFR\_SLOPE\_TRIM1 (DDh)

This register is used to calibrate the  $V_{\text{OUT}}$  offset caused by slope compensation and  $V_{\text{OUT}}$  ripple.

| Command  | MFR_SLOPE_TRIM1 |          |     |     |     |     |          |     |     |     |     |           |     |     |     |     |
|----------|-----------------|----------|-----|-----|-----|-----|----------|-----|-----|-----|-----|-----------|-----|-----|-----|-----|
| Format   | Unsigned binary |          |     |     |     |     |          |     |     |     |     |           |     |     |     |     |
| Bit      | 15              | 14       | 13  | 12  | 11  | 10  | 9        | 8   | 7   | 6   | 5   | 4         | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w      | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w       | r/w | r/w | r/w | r/w |
| Function | x               | VTRIM_2P |     |     |     |     | VTRIM_1P |     |     |     |     | VTRIM_DCM |     |     |     |     |

| Bits  | Bit Name  | Description                                                                                                                                       |
|-------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                                 |
| 14:10 | VTRIM_2P  | Output voltage calibration value for 2-phase status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1     |
| 9:5   | VTRIM_1P  | Output voltage calibration value for 1-phase CCM status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1 |
| 4:0   | VTRIM_DCM | Output voltage calibration value for 1-phase DCM status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1 |

**MFR\_SLOPE\_TRIM2 (DEh)**

This register is used to calibrate the  $V_{OUT}$  offset caused by slope compensation and  $V_{OUT}$  ripple.

| Command  | MFR_SLOPE_TRIM2 |          |     |     |     |     |          |     |     |     |     |          |     |     |     |     |
|----------|-----------------|----------|-----|-----|-----|-----|----------|-----|-----|-----|-----|----------|-----|-----|-----|-----|
| Format   | Unsigned binary |          |     |     |     |     |          |     |     |     |     |          |     |     |     |     |
| Bit      | 15              | 14       | 13  | 12  | 11  | 10  | 9        | 8   | 7   | 6   | 5   | 4        | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w      | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w |
| Function | x               | VTRIM_5P |     |     |     |     | VTRIM_4P |     |     |     |     | VTRIM_3P |     |     |     |     |

| Bits  | Bit Name | Description                                                                                                                                   |
|-------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                                                                             |
| 14:10 | VTRIM_5P | Output voltage calibration value for 5-phase status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1 |
| 9:5   | VTRIM_4P | Output voltage calibration value for 4-phase status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1 |
| 4:0   | VTRIM_3P | Output voltage calibration value for 3-phase status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1 |

**MFR\_SLOPE\_TRIM3 (DFh)**

This register is used to calibrate  $V_{OUT}$  offset caused by slope compensation and  $V_{OUT}$  ripple.

| Command  | MFR_SLOPE_TRIM3 |          |     |     |     |     |          |     |     |     |     |          |     |     |     |     |
|----------|-----------------|----------|-----|-----|-----|-----|----------|-----|-----|-----|-----|----------|-----|-----|-----|-----|
| Format   | Unsigned binary |          |     |     |     |     |          |     |     |     |     |          |     |     |     |     |
| Bit      | 15              | 14       | 13  | 12  | 11  | 10  | 9        | 8   | 7   | 6   | 5   | 4        | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w      | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w |
| Function | x               | VTRIM_8P |     |     |     |     | VTRIM_7P |     |     |     |     | VTRIM_6P |     |     |     |     |

| Bits  | Bit Name | Description                                                                                                                                   |
|-------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED | Unused. X indicates that writes are ignored and always read as 0.                                                                             |
| 14:10 | VTRIM_8P | Output voltage calibration value for 8-phase status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1 |
| 9:5   | VTRIM_7P | Output voltage calibration value for 7-phase status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1 |
| 4:0   | VTRIM_6P | Output voltage calibration value for 6-phase status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1 |

**MFR\_SLOPE\_TRIM4 (E0h)**

This register is used to calibrate the  $V_{OUT}$  offset caused by slope compensation and  $V_{OUT}$  ripple.

| Command  | MFR_SLOPE_TRIM4 |     |     |     |     |     |           |     |     |     |     |          |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----------|-----|-----|-----|-----|----------|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |           |     |     |     |     |          |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9         | 8   | 7   | 6   | 5   | 4        | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w       | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w |
| Function | x               | x   | x   | x   | x   | x   | VTRIM_10P |     |     |     |     | VTRIM_9P |     |     |     |     |

| Bits  | Bit Name  | Description                                                                                                                                    |
|-------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED  | Unused. X indicates that writes are ignored and always read as 0.                                                                              |
| 9:5   | VTRIM_10P | Output voltage calibration value for 10-phase status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1 |
| 4:0   | VTRIM_9P  | Output voltage calibration value for 9-phase status.<br>2.35mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 0<br>4.7mV/LSB, when VDIFF_GAIN_SEL (2Ah) = 1  |

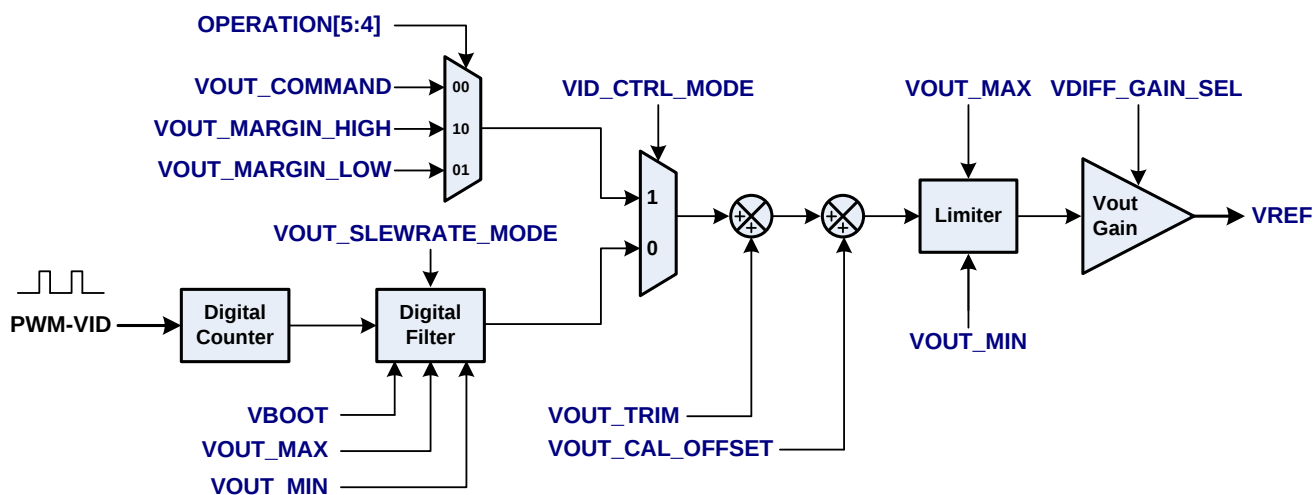
**MFR\_VR\_CONFIG1 (E1h)**

This register sets the main functions of the controller.

| Command  | MFR_VR_CONFIG1  |     |     |     |     |     |     |     |     |     |     |     |           |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----------|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |     |     |     |     |           |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3         | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w       | r/w | r/w | r/w |
| Function |                 |     |     |     |     |     |     |     |     |     |     |     | PHASE_CNT |     |     |     |

| Bits  | Bit Name          | Description                                                                                                            |
|-------|-------------------|------------------------------------------------------------------------------------------------------------------------|
| 15    | DC_LOOP_EN_PS2    | Enable bit of the DC loop for DCM.<br>0: disable<br>1: enable                                                          |
| 14    | DC_LOOP_EN        | Enable bit of the DC loop for CCM.<br>0: disable<br>1: enable                                                          |
| 13    | PSI_SEL           | PSI controlling mode selector.<br>0: controlled by PSI<br>1: controlled by PMBus command (bit[12:11] of this register) |
| 12:11 | PSI_PMBUS         | PSI command via PMBus.<br>00: full-phase CCM<br>01: 1-phase CCM<br>1x: 1-phase DCM                                     |
| 10    | RESERVED          | Unused. X indicates that writes are ignored and always read as 0.                                                      |
| 9     | PS2_TON_REDUCE_EN | Enable bit for reducing PWM on-time to 3/4 of its normal value at PS2.<br>0: disable<br>1: enable                      |

|           |                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |           |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
|-----------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|------|-----------|------|------|-------------|------|----------|------|-------------|------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|-----------|------|----------|--------|-----------|
| 8         | PMBUS_PSI_BYPASS_EN | Enable bit for bypassing the PSI command. When APS is enabled, set this bit to ignore the PSI command from PSI or the PMBus.<br>0: disable<br>1: enable                                                                                                                                                                                                                                                                                                                                                                                                                  |           |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 7         | CB_EN               | Enable bit for current balance loop.<br>0: disable<br>1: enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |           |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 6         | OSR_EN              | Enable bit for overshoot reduction.<br>0: disable<br>1: enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |           |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 5         | APS_EN              | Enable bit for auto-phase shedding.<br>0: disable<br>1: enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |           |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 4         | VID_CTRL_MODE       | Output voltage controlling mode.<br>0: output voltage is controlled via PWM-VID<br>1: output voltage is controlled via the PMBus                                                                                                                                                                                                                                                                                                                                                                                                                                         |           |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 3:0       | PHASE_CNT           | Phase number setting for full-phase mode. <table><tr><td>PHASE_CNT</td><td>Mode</td><td>PHASE_CNT</td><td>Mode</td></tr><tr><td>0000</td><td>1-phase DCM</td><td>0110</td><td>6 phases</td></tr><tr><td>0001</td><td>1-phase CCM</td><td>0111</td><td>7 phases</td></tr><tr><td>0010</td><td>2 phases</td><td>1000</td><td>8 phases</td></tr><tr><td>0011</td><td>3 phases</td><td>1001</td><td>9 phases</td></tr><tr><td>0100</td><td>4 phases</td><td>1010</td><td>10 phases</td></tr><tr><td>0101</td><td>5 phases</td><td>others</td><td>10 phases</td></tr></table> | PHASE_CNT | Mode | PHASE_CNT | Mode | 0000 | 1-phase DCM | 0110 | 6 phases | 0001 | 1-phase CCM | 0111 | 7 phases | 0010 | 2 phases | 1000 | 8 phases | 0011 | 3 phases | 1001 | 9 phases | 0100 | 4 phases | 1010 | 10 phases | 0101 | 5 phases | others | 10 phases |
| PHASE_CNT | Mode                | PHASE_CNT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Mode      |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 0000      | 1-phase DCM         | 0110                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 6 phases  |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 0001      | 1-phase CCM         | 0111                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 7 phases  |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 0010      | 2 phases            | 1000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 8 phases  |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 0011      | 3 phases            | 1001                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 9 phases  |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 0100      | 4 phases            | 1010                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 10 phases |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |
| 0101      | 5 phases            | others                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 10 phases |      |           |      |      |             |      |          |      |             |      |          |      |          |      |          |      |          |      |          |      |          |      |           |      |          |        |           |



**Figure 23: Conceptual View of How Output Voltage Related Commands are Applied**

**MFR\_VR\_CONFIG2 (E2h)**

This register sets the main functions of the controller.

| Command  | MFR_VR_CONFIG2  |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |
| Bit      | 7               | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | x   |     |     |     |     |     |     |

| Bits | Bit Name             | Description                                                                                                                                                                                                                                                                                                                                              |
|------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | RESERVED             | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                        |
| 5    | COUPLE_INDUCTOR_PWM6 | PWM6 performance selector to fit coupled inductor operating mode.<br>0: PWM6 remains in tri-state when the controller is running in 1-phase CCM or DCM. This is used for normal inductor operating mode.<br>1: PWM6 pulls low while PWM1 is high when the controller is running in 1-phase CCM or DCM. This is used for coupled inductor operating mode. |
| 4    | COUPLE_INDUCTOR_EN   | Enable bit for coupled inductor operating mode.<br>0: disable<br>1: enable                                                                                                                                                                                                                                                                               |
| 3    | LOW_PWR_EN           | Enable bit for low-power mode. Low-power mode is when EN is low, and the controller disables some internal circuits to save power. PMBus communication is also disabled in low-power mode.<br>0: disable<br>1: enable                                                                                                                                    |
| 2    | EN_SD_MODE           | Shutdown mode via EN.<br>0: immediate shutdown (all PWMs are set to tri-state)<br>1: soft shutdown (output voltage falls to zero with a boot-up slew rate)<br>If LOW_PWR_EN = 1, only immediate shutdown is available.                                                                                                                                   |
| 1    | DLY_CLK_SEL          | Delay time clock selector for TON_DELAY and TOFF_DELAY.<br>0: 20µs/LSB<br>1: 50µs/LSB                                                                                                                                                                                                                                                                    |
| 0    | VOUT_SLEWRATE_MODE   | Output voltage (boot-up, shutdown, and DVID) slewing mode selector for PWM-VID mode.<br>0: linear mode<br>1: R-C filter mode<br>In PMBus override mode, the slew rate is always linear.                                                                                                                                                                  |

**MFR\_APS\_LEVEL1 (E3h)**

This register sets the output current threshold for phase dropping when APS is enabled.

| Command  | MFR_APS_LEVEL1  |     |     |     |     |     |     |     |                |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|----------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |                |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7              | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w            | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | DROP_LEVEL_1P   |     |     |     |     |     |     |     | DROP_LEVEL_DCM |     |     |     |     |     |     |     |

| Bits | Bit Name       | Description                                                                                                                                        |
|------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | DROP_LEVEL_1P  | Output current threshold for dropping to 1-phase CCM status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1)     |
| 7:0  | DROP_LEVEL_DCM | Output current threshold for dropping to the 1-phase DCM status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

### MFR\_APS\_LEVEL2 (E4h)

This register sets the output current threshold for phase dropping when APS is enabled.

| Command  | MFR_APS_LEVEL2  |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | DROP_LEVEL_3P   |     |     |     |     |     |     |     | DROP_LEVEL_2P |     |     |     |     |     |     |     |

| Bits | Bit Name      | Description                                                                                                                                |
|------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | DROP_LEVEL_3P | Output current threshold for dropping to 3-phase status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |
| 7:0  | DROP_LEVEL_2P | Output current threshold for dropping to 2-phase status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

### MFR\_APS\_LEVEL3 (E5h)

This register sets the output current threshold for phase dropping when APS is enabled.

| Command  | MFR_APS_LEVEL3  |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | DROP_LEVEL_5P   |     |     |     |     |     |     |     | DROP_LEVEL_4P |     |     |     |     |     |     |     |

| Bits | Bit Name      | Description                                                                                                                                |
|------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | DROP_LEVEL_5P | Output current threshold for dropping to 5-phase status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |
| 7:0  | DROP_LEVEL_4P | Output current threshold for dropping to 4-phase status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

**MFR\_APS\_LEVEL4 (E6h)**

This register sets the output current threshold for phase dropping when APS is enabled.

|          |                 |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|
| Command  | MFR_APS_LEVEL4  |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
| Format   | Unsigned binary |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | DROP_LEVEL_7P   |     |     |     |     |     |     |     | DROP_LEVEL_6P |     |     |     |     |     |     |     |

| Bits | Bit Name      | Description                                                                                                                                |
|------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | DROP_LEVEL_7P | Output current threshold for dropping to 7-phase status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |
| 7:0  | DROP_LEVEL_6P | Output current threshold for dropping to 6-phase status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

**MFR\_APS\_LEVEL5 (E7h)**

This register sets the output current threshold for phase dropping when APS is enabled.

|          |                 |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|
| Command  | MFR_APS_LEVEL6  |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
| Format   | Unsigned binary |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | DROP_LEVEL_9P   |     |     |     |     |     |     |     | DROP_LEVEL_8P |     |     |     |     |     |     |     |

| Bits | Bit Name      | Description                                                                                                                                |
|------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | DROP_LEVEL_9P | Output current threshold for dropping to 9-phase status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |
| 7:0  | DROP_LEVEL_8P | Output current threshold for dropping to 8-phase status.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

**MFR\_APS\_HYS (E8h)**

This register sets the output current hysteresis threshold for APS.

|          |                 |     |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Command  | MFR_APS_HYS     |     |     |     |     |     |     |     |
| Format   | Unsigned binary |     |     |     |     |     |     |     |
| Bit      | 7               | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | HYS_APS         |     |     |     |     |     |     |     |

| Bits | Bit Name | Description                                                                                                                                |
|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | HYS_APS  | Hysteresis of output current threshold for APS function.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1) |

**MFR\_TSNS\_OT\_SET (E9h)**

This register sets the OTP function via TSNS.

| Command  | MFR_TSNS_OT_SET |     |              |     |     |     |     |     |               |     |     |     |     |     |     |     |
|----------|-----------------|-----|--------------|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |              |     |     |     |     |     |               |     |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13           | 12  | 11  | 10  | 9   | 8   | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w          | r/w | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |                 |     | TSNS_OTP_HYS |     |     |     |     |     | TSNS_OTP_THRE |     |     |     |     |     |     |     |

| Bits | Bit Name      | Description                                                                                                                                                                             |
|------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | TSNS_OTP_EN   | Enable bit for OTP via TSNS.<br>0: disable<br>1: enable                                                                                                                                 |
| 14   | TSNS_OTP_MODE | Mode selector for OTP via TSNS.<br>0: hiccup mode<br>1: latch mode                                                                                                                      |
| 13:8 | TSNS_OTP_HYS  | Hysteresis for exiting OTP via TSNS in hiccup mode.<br>$TSNS\_OTP\_HYS = \frac{256 \times V_{TSNS\_HYS}}{1.6}$<br>Where $V_{TSNS\_HYS}$ is the voltage hysteresis of TSNS for TSNS OTP. |
| 7:0  | TSNS_OTP_THRE | Threshold for triggering OTP via TSNS.<br>$TSNS\_OTP\_THRE = \frac{256 \times V_{TSNS\_THRE}}{1.6}$<br>Where $V_{TSNS\_THRE}$ is the voltage threshold of TSNS for OTP.                 |

**MFR\_VTEMP\_OT\_SET (EAh)**

This register sets the OTP function via VTEMP.

| Command  | MFR_VTEMP_OT_SET |     |     |     |     |     |     |     |     |               |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |     |     |     |     |     |               |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6             | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w           | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | VTEMP_OTP_THRE   |     |     |     |     |     |     |     |     | VTEMP_OTP_HYS |     |     |     |     |     |     |

| Bits | Bit Name       | Description                                                         |
|------|----------------|---------------------------------------------------------------------|
| 15:8 | VTEMP_OTP_THRE | Threshold for OTP via VTEMP. 1°C/LSB.                               |
| 7    | VTEMP_OTP_MODE | Mode selector for OTP via VTEMP.<br>0: hiccup mode<br>1: latch mode |
| 6:0  | VTEMP_OTP_HYS  | Hysteresis for exiting OTP via VTEMP in hiccup mode. 1°C/LSB.       |

### MFR\_OCP\_TOTAL (ECh)

This register sets the total output over current protection. Total OCP is not active during soft start.

| Command  | MFR_OCP_TOTAL   |     |     |                   |     |     |     |     |     |          |     |     |     |     |     |     |
|----------|-----------------|-----|-----|-------------------|-----|-----|-----|-----|-----|----------|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |                   |     |     |     |     |     |          |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12                | 11  | 10  | 9   | 8   | 7   | 6        | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w               | r/w | r/w | r/w | r/w | r/w | r/w      | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               |     |     | OCP_DEGLITCH_TIME |     |     |     |     |     | OCP_THRE |     |     |     |     |     |     |

| Bits  | Bit Name          | Description                                                                                                            |
|-------|-------------------|------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED          | Unused. X indicates that writes are ignored and always read as 0.                                                      |
| 14:13 | OCP_MODE          | Total OCP action mode selector.<br>00: no action<br>01: latch off<br>10: hiccup<br>11: retry six times                 |
| 12:7  | OCP_DEGLITCH_TIME | Deglitch time for total OCP. When the protection condition lasts for this deglitch time, the VR shuts down. 100µs/LSB. |
| 6:0   | OCP_THRE          | Threshold of total OCP.<br>1A/LSB (TOTAL_CURRENT_RESOLUTION = 0)<br>2A/LSB (TOTAL_CURRENT_RESOLUTION = 1)              |

### MFR\_OCP\_PHASE (EDh)

This register sets the phase valley current limit. When a certain phase's inductor current is greater than this threshold, this PWM is cannot turn high.

| Command  | MFR_OCP_PHASE   |                 |     |     |     |     |     |     |
|----------|-----------------|-----------------|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |                 |     |     |     |     |     |     |
| Bit      | 7               | 6               | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w             | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x               | PHASE_CUR_LIMIT |     |     |     |     |     |     |

| Bits | Bit Name        | Description                                                                                                       |
|------|-----------------|-------------------------------------------------------------------------------------------------------------------|
| 7    | RESERVED        | Unused. X indicates that writes are ignored and always read as 0.                                                 |
| 6:0  | PHASE_CUR_LIMIT | Per-phase valley current limit.<br>1A/LSB (PHASE_CURRENT_RESOLUTION = 0)<br>2A/LSB (PHASE_CURRENT_RESOLUTION = 1) |

### MFR\_OVP\_UVP\_SET (EEh)

This register sets  $V_{OUT}$  OVP and UVP. The OVP2 and UVP2 level is selected by bit[2:0] of register MFR\_OVUV\_SEL (2Ch). OVP2 and UVP are not active during the soft-start process.

| Command  | MFR_OVP_UVP_SET |     |     |                    |     |     |     |     |     |                   |     |     |     |     |     |     |
|----------|-----------------|-----|-----|--------------------|-----|-----|-----|-----|-----|-------------------|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |     |     |                    |     |     |     |     |     |                   |     |     |     |     |     |     |
| Bit      | 15              | 14  | 13  | 12                 | 11  | 10  | 9   | 8   | 7   | 6                 | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w             | r/w | r/w | r/w                | r/w | r/w | r/w | r/w | r/w | r/w               | r/w | r/w | r/w | r/w | r/w | r/w |
| Function |                 |     |     | OVP2_DEGLITCH_TIME |     |     |     |     |     | UVP_DEGLITCH_TIME |     |     |     |     |     |     |

| Bits  | Bit Name           | Description                                                                                                             |
|-------|--------------------|-------------------------------------------------------------------------------------------------------------------------|
| 15:13 | OVP2_MODE          | OVP mode selector.<br>000: no action<br>010: latch off<br>100: hiccup<br>110: retry six times<br>111: retry three times |
| 12:8  | OVP2_DEGLITCH_TIME | Deglitch time for OVP. When the protection condition lasts for this deglitch time, the VR shuts down. 100ns/LSB.        |
| 7:6   | UVP_MODE           | UVP mode selector.<br>00: no action<br>01: latch off<br>10: hiccup<br>11: retry six times                               |
| 5:0   | UVP_DEGLITCH_TIME  | Deglitch time for UVP. When the protection condition lasts for this deglitch time, the VR shuts down. 20µs/LSB.         |

### MFR\_FAULTS1 (F8h)

This register returns the faults of the present protection. These bits are in latch mode. The CLEAR\_FAULTS command can reset these bits.

| Command  | MFR_FAULTS1     |    |    |    |              |    |   |   |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|--------------|----|---|---|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary |    |    |    |              |    |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11           | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r            | r  | r | r | r | r | r | r | r | r | r | r |
| Function | x               | x  | x  |    | CS_FAULT_TRG |    |   |   | x |   |   |   |   |   |   |   |

| Bits  | Bit Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 12    | TEMP_FAULT_TRG | Flag of TEMP_FAULT protection.<br>0: protection not triggered by TEMP_FAULT of the Intelli-Phase<br>1: protection triggered by TEMP_FAULT of the Intelli-Phase                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11:8  | CS_FAULT_TRG   | Flag for CS_FAULT triggering VR protection.<br>0000: protection not triggered by CS_FAULT of the Intelli-Phase<br>0001: protection triggered by CS1_FAULT of the Intelli-Phase<br>0010: protection triggered by CS2_FAULT of the Intelli-Phase<br>0011: protection triggered by CS3_FAULT of the Intelli-Phase<br>0100: protection triggered by CS4_FAULT of the Intelli-Phase<br>0101: protection triggered by CS5_FAULT of the Intelli-Phase<br>0110: protection triggered by CS6_FAULT of the Intelli-Phase<br>0111: protection triggered by CS7_FAULT of the Intelli-Phase<br>1000: protection triggered by CS8_FAULT of the Intelli-Phase<br>1001: protection triggered by CS9_FAULT of the Intelli-Phase<br>1010: protection triggered by CS10_FAULT of the Intelli-Phase |
| 7     | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 6     | VIN_OV_FLAG    | Flag of input OVP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 5     | VIN_UVLO_FLAG  | Flag of input UVP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 4     | VTEMP_OTP_FLAG | Flag of OTP from VTEMP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3     | TSNS_OTP_FLAG  | Flag of OTP from TSNS.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

|   |          |                     |
|---|----------|---------------------|
| 2 | OVP_FLAG | Flag of output OVP. |
| 1 | UVP_FLAG | Flag of output UVP. |
| 0 | OCP_FLAG | Flag of output OCP. |

### MFR\_FAULTS2 (F9h)

This register returns the faults of the present protection. These bits are in latch mode. The CLEAR\_FAULTS command can reset these bits.

|          |                 |    |    |    |             |    |   |   |             |   |   |   |             |   |   |   |
|----------|-----------------|----|----|----|-------------|----|---|---|-------------|---|---|---|-------------|---|---|---|
| Command  | MFR_FAULTS2     |    |    |    |             |    |   |   |             |   |   |   |             |   |   |   |
| Format   | Unsigned binary |    |    |    |             |    |   |   |             |   |   |   |             |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11          | 10 | 9 | 8 | 7           | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r           | r  | r | r | r           | r | r | r | r           | r | r | r |
| Function | PWM1_FAULTS     |    |    |    | PWM2_FAULTS |    |   |   | PWM3_FAULTS |   |   |   | PWM4_FAULTS |   |   |   |

| Bits  | Bit Name    | Description                                                                                                                                                                                      |
|-------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | PWM1_FAULTS | Intelli-Phase fault type indication of phase 1.<br>0000: no fault<br>0001: VIN-SW short<br>0010: current limit protection<br>0100: over-temperature protection<br>1000: SW-PGND short protection |
| 11:8  | PWM2_FAULTS | Intelli-Phase fault type indication of phase 2. Same types as bit[15:12].                                                                                                                        |
| 7:4   | PWM3_FAULTS | Intelli-Phase fault type indication of phase 3. Same types as bit[15:12].                                                                                                                        |
| 3:0   | PWM4_FAULTS | Intelli-Phase fault type indication of phase 4. Same types as bit[15:12].                                                                                                                        |

### MFR\_FAULTS3 (FAh)

This register returns the faults of the present protection. These bits are in latch mode. The CLEAR\_FAULTS command can reset these bits.

|          |                 |    |    |    |             |    |   |   |             |   |   |   |             |   |   |   |
|----------|-----------------|----|----|----|-------------|----|---|---|-------------|---|---|---|-------------|---|---|---|
| Command  | MFR_FAULTS3     |    |    |    |             |    |   |   |             |   |   |   |             |   |   |   |
| Format   | Unsigned binary |    |    |    |             |    |   |   |             |   |   |   |             |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11          | 10 | 9 | 8 | 7           | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r           | r  | r | r | r           | r | r | r | r           | r | r | r |
| Function | PWM5_FAULTS     |    |    |    | PWM6_FAULTS |    |   |   | PWM7_FAULTS |   |   |   | PWM8_FAULTS |   |   |   |

| Bits  | Bit Name    | Description                                                                                                                                                                                      |
|-------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | PWM5_FAULTS | Intelli-Phase fault type indication of phase 5.<br>0000: no fault<br>0001: VIN-SW short<br>0010: current limit protection<br>0100: over-temperature protection<br>1000: SW-PGND short protection |
| 11:8  | PWM6_FAULTS | Intelli-Phase fault type indication of phase 6. Same types as bit[15:12].                                                                                                                        |
| 7:4   | PWM7_FAULTS | Intelli-Phase fault type indication of phase 7. Same types as bit[15:12].                                                                                                                        |
| 3:0   | PWM8_FAULTS | Intelli-Phase fault type indication of phase 8. Same types as bit[15:12].                                                                                                                        |

### MFR\_FAULTS4 (FBh)

This register returns the faults of the present protection. These bits are in latch mode. The CLEAR\_FAULTS command can reset these bits.

| Command  | MFR_FAULTS4     |    |    |    |              |    |   |   |   |   |   |   |   |   |   |   |
|----------|-----------------|----|----|----|--------------|----|---|---|---|---|---|---|---|---|---|---|
| Format   | Unsigned binary |    |    |    |              |    |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15              | 14 | 13 | 12 | 11           | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r               | r  | r  | r  | r            | r  | r | r | r | r | r | r | r | r | r | r |
| Function | PWM9_FAULTS     |    |    |    | PWM10_FAULTS |    |   |   | x | x | x | x | x | x | x | x |

| Bits  | Bit Name     | Description                                                                                                                                                                                      |
|-------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | PWM9_FAULTS  | Intelli-Phase fault type indication of phase 9.<br>0000: no fault<br>0001: VIN-SW short<br>0010: current limit protection<br>0100: over-temperature protection<br>1000: SW-PGND short protection |
| 11:8  | PWM10_FAULTS | Intelli-Phase fault type indication of phase 10. Same types as bit[15:12].                                                                                                                       |
| 7:0   | RESERVED     | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                |

### CLEAR\_EEPROM\_FAULTS (FFh)

This command is used to clear the EEPROM fault. This command is write only. There is no data byte for this command.

## PAGE 29 REGISTER MAP

### MFR\_LAST\_FAULTS1 (FBh)

This register returns the faults of the last protection. To clear the fault bits, 0x0000 can be written to this register. Then wait for 5ms.

| Command  | MFR_LAST_FAULTS1 |     |     |     |              |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|--------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |              |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11           | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w          | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | x                | x   | x   |     | CS_FAULT_TRG |     |     |     | x   |     |     |     |     |     |     |     |

| Bits  | Bit Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 12    | TEMP_FAULT_TRG | Flag of TEMP_FAULT protection.<br>0: protection not triggered by TEMP_FAULT of the Intelli-Phase<br>1: protection triggered by TEMP_FAULT of the Intelli-Phase                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 11:8  | CS_FAULT_TRG   | Flag for CS_FAULT triggering VR protection.<br><br>0000: protection is not triggered by CS_FAULT of the Intelli-Phase<br>0001: protection is triggered by CS1_FAULT of the Intelli-Phase<br>0010: protection is triggered by CS2_FAULT of the Intelli-Phase<br>0011: protection is triggered by CS3_FAULT of the Intelli-Phase<br>0100: protection is triggered by CS4_FAULT of the Intelli-Phase<br>0101: protection is triggered by CS5_FAULT of the Intelli-Phase<br>0110: protection is triggered by CS6_FAULT of the Intelli-Phase<br>0111: protection is triggered by CS7_FAULT of the Intelli-Phase<br>1000: protection is triggered by CS8_FAULT of the Intelli-Phase<br>1001: protection is triggered by CS9_FAULT of the Intelli-Phase<br>1010: protection is triggered by CS10_FAULT of the Intelli-Phase |
| 7     | RESERVED       | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 6     | VIN_OV_FLAG    | Flag of input OVP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 5     | VIN_UVLO_FLAG  | Flag of input UVP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 4     | VTEMP_OTP_FLAG | Flag of OTP from VTEMP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 3     | TSNS_OTP_FLAG  | Flag of OTP from TSNS.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 2     | OVP_FLAG       | Flag of output OVP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 1     | UVP_FLAG       | Flag of output UVP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 0     | OCP_FLAG       | Flag of output OCP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

### MFR\_LAST\_FAULTS2 (FCh)

This register returns the faults of the last protection. To clear the fault bits, 0x0000 can be written to this register. Then wait for 5ms.

| Command  | MFR_LAST_FAULTS2 |     |     |     |             |     |     |     |             |     |     |     |             |     |     |     |
|----------|------------------|-----|-----|-----|-------------|-----|-----|-----|-------------|-----|-----|-----|-------------|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |             |     |     |     |             |     |     |     |             |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11          | 10  | 9   | 8   | 7           | 6   | 5   | 4   | 3           | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w         | r/w | r/w | r/w | r/w         | r/w | r/w | r/w | r/w         | r/w | r/w | r/w |
| Function | PWM1_FAULTS      |     |     |     | PWM2_FAULTS |     |     |     | PWM3_FAULTS |     |     |     | PWM4_FAULTS |     |     |     |

| Bits  | Bit Name    | Description                                                                                                                                                                                      |
|-------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | PWM1_FAULTS | Intelli-Phase fault type indication of phase 1.<br>0000: no fault<br>0001: VIN-SW short<br>0010: current-limit protection<br>0100: over-temperature protection<br>1000: SW-PGND short protection |
| 11:8  | PWM2_FAULTS | Intelli-Phase fault type indication of phase 2. Same types as bit[15:12].                                                                                                                        |
| 7:4   | PWM3_FAULTS | Intelli-Phase fault type indication of phase 3. Same types as bit[15:12].                                                                                                                        |
| 3:0   | PWM4_FAULTS | Intelli-Phase fault type indication of phase 4. Same types as bit[15:12].                                                                                                                        |

### MFR\_LAST\_FAULTS3 (FDh)

This register returns the faults of the last protection. To clear the fault bits, 0x0000 can be written to this register. Then wait for 5ms.

| Command  | MFR_LAST_FAULTS3 |     |     |     |             |     |     |     |             |     |     |     |             |     |     |     |
|----------|------------------|-----|-----|-----|-------------|-----|-----|-----|-------------|-----|-----|-----|-------------|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |             |     |     |     |             |     |     |     |             |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11          | 10  | 9   | 8   | 7           | 6   | 5   | 4   | 3           | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w         | r/w | r/w | r/w | r/w         | r/w | r/w | r/w | r/w         | r/w | r/w | r/w |
| Function | PWM5_FAULTS      |     |     |     | PWM6_FAULTS |     |     |     | PWM7_FAULTS |     |     |     | PWM8_FAULTS |     |     |     |

| Bits  | Bit Name    | Description                                                                                                                                                                                      |
|-------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | PWM5_FAULTS | Intelli-Phase fault type indication of phase 5.<br>0000: no fault<br>0001: VIN-SW short<br>0010: current-limit protection<br>0100: over-temperature protection<br>1000: SW-PGND short protection |
| 11:8  | PWM6_FAULTS | Intelli-Phase fault type indication of phase 6. Same types as bit[15:12].                                                                                                                        |
| 7:4   | PWM7_FAULTS | Intelli-Phase fault type indication of phase 7. Same types as bit[15:12].                                                                                                                        |
| 3:0   | PWM8_FAULTS | Intelli-Phase fault type indication of phase 8. Same types as bit[15:12].                                                                                                                        |

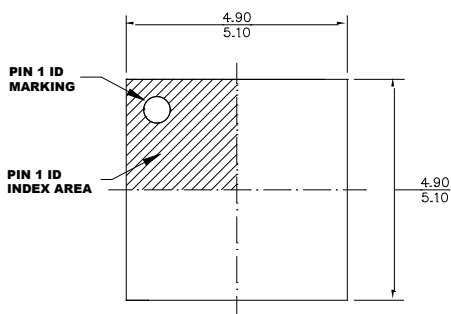
### MFR\_LAST\_FAULTS4 (FEh)

This register returns the faults of the last protection. To clear the fault bits, 0x0000 can be written to this register. Then wait for 5ms.

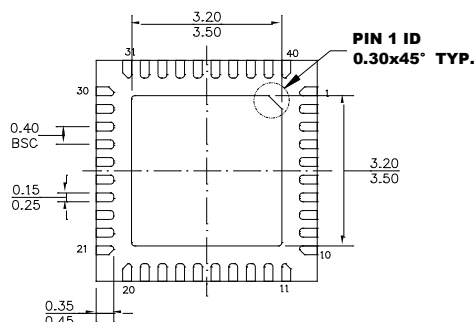
| Command  | MFR_LAST_FAULTS4 |     |     |     |                                                                                                                                                                                                      |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------|-----|-----|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Unsigned binary  |     |     |     |                                                                                                                                                                                                      |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14  | 13  | 12  | 11                                                                                                                                                                                                   | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r/w              | r/w | r/w | r/w | r/w                                                                                                                                                                                                  | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | PWM9_FAULTS      |     |     |     | PWM10_FAULTS                                                                                                                                                                                         |     |     |     | x   | x   | x   | x   | x   | x   | x   | x   |
| Bits     | Bit Name         |     |     |     | Description                                                                                                                                                                                          |     |     |     |     |     |     |     |     |     |     |     |
| 15:12    | PWM9_FAULTS      |     |     |     | Intelli-Phase fault type indication of phase 9.<br><br>0000: no fault<br>0001: VIN-SW short<br>0010: current-limit protection<br>0100: over-temperature protection<br>1000: SW-PGND short protection |     |     |     |     |     |     |     |     |     |     |     |
| 11:8     | PWM10_FAULTS     |     |     |     | Intelli-Phase fault type indication of phase 10. Same types as bit[15:12].                                                                                                                           |     |     |     |     |     |     |     |     |     |     |     |
| 7:0      | RESERVED         |     |     |     | Unused. X indicates that writes are ignored and always read as 0.                                                                                                                                    |     |     |     |     |     |     |     |     |     |     |     |

# PACKAGE INFORMATION

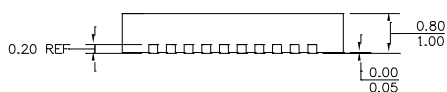
## QFN-40 (5mmx5mm)



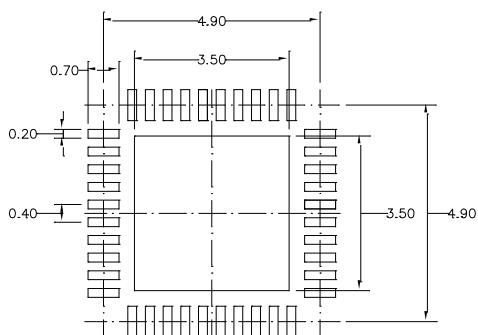
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**



**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHE-1
- 5) DRAWING IS NOT TO SCALE.

| Revision # | Revision Date | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Pages Updated |
|------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 1.0        | 01/03/2018    | Initial Release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | -             |
| 1.1        | 12/21/2018    | Updated Enable high leakage from 2.1uA to 2.3uA in Electrical Characteristics section.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 5             |
|            |               | Updated Electrical Characteristics section:<br><ul style="list-style-type: none"> <li>Updated Under-voltage threshold typ values to -190mV, -310mV, and -430mV.</li> <li>Updated Under-voltage threshold description and related registers.</li> <li>Updated Over-voltage threshold typ values to 190mV, 310mV, and 430mV.</li> <li>Updated Over-voltage threshold description and related registers.</li> <li>Updated ADC Voltage reference min/typ/max to 1.592/1.6/1.608.</li> <li>Updated DAC voltage reference typ value to 1.7 and removed min/max values.</li> </ul> | 6             |
| 1.11       | 11/14/2025    | <ul style="list-style-type: none"> <li>Updated Description section to remove confidential customer name.</li> <li>Updated Features section to remove confidential customer name.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                 | 1             |
|            |               | Updated Operation section to remove confidential customer name.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 14            |
|            |               | Formatting updates to Revision History section.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 114           |

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