MP2882

Dual-Loop, Digital, 16-Phase Controller with PMBus Interface for SVI2/AVSBus

DESCRIPTION

The MP2882 is a dual-loop, digital, multi-phase controller that provides power for the memory and system-on-chip (SoC). The MP2882 can work with MPS's Intelli-Phase™ products to complete the multi-phase voltage regulator (VR) solution with a minimal number of external components. The MP2882 can be configured for up to 16-phase operation on rail 1 and up to 8-phase operation on rail 2.

The MP2882 provides an on-chip non-volatile memory (NVM) to store and restore device configurations. Device configurations and fault parameters can be easily configured or monitored via the PMBus/I²C interface. The device can monitor and report the output current through the CS output from Intelli-Phase™ devices.

The MP2882 is based on unique, digital, multi-phase control to provide fast transient response to the load transient with minimal output capacitors. With only one power loop control method for both steady state and load transient, the power loop compensation is simple to configure.

The MP2882 is available in a TQFN-56 (7mmx7mm) package.

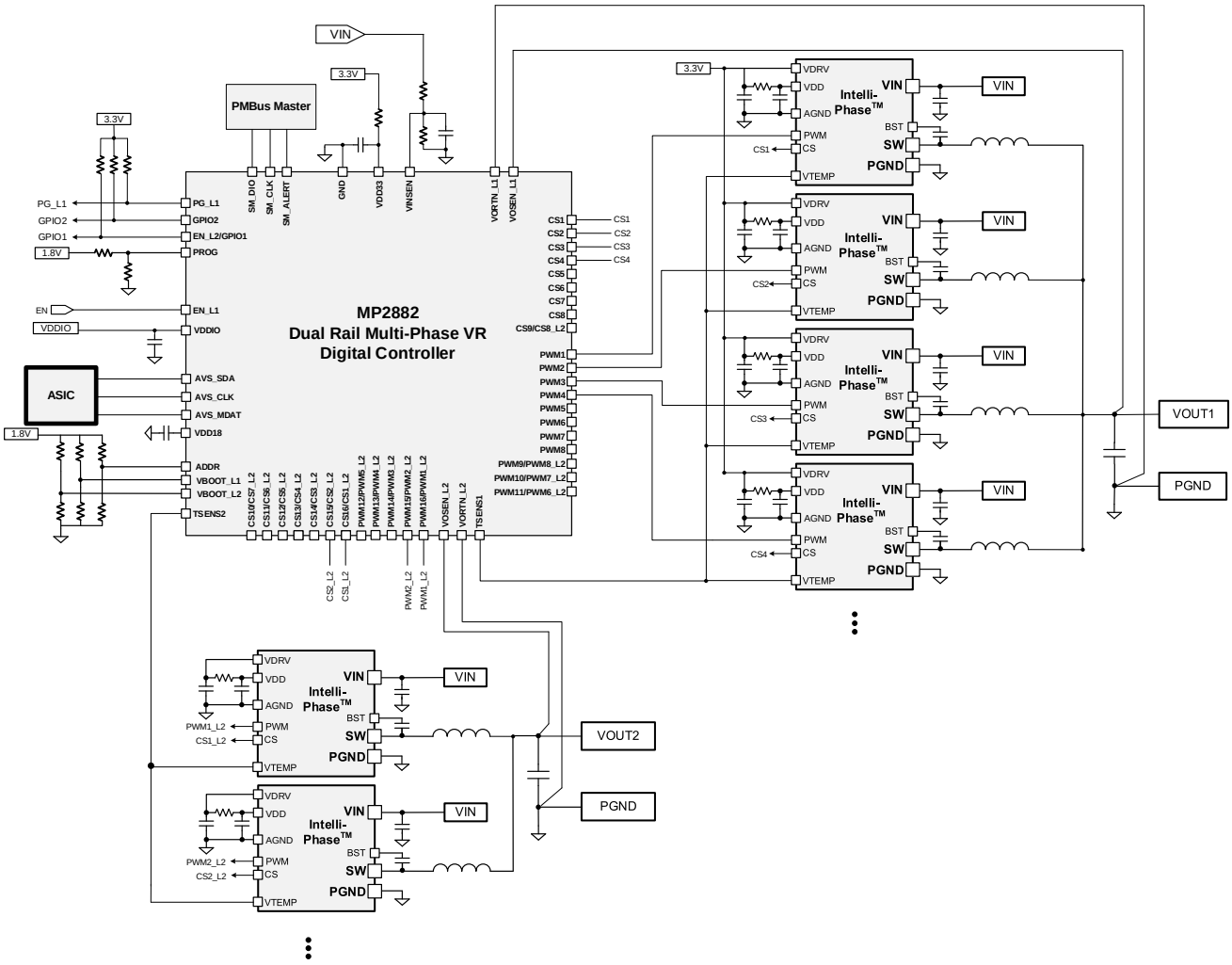
FEATURES

- Multi-Phase, Dual-Output Digital Controller
- PMBus/I²C Compatible (1MHz Bus Speed)
- AMD SVI2 Compatible
- AVSBus Compatible
- N + 2 Phase Redundancy Function
- Pin-Configurable PMBus Address
- Built-In NVM to Store Custom Configurations
- Can Support 16 Rails with Register Setting
- 200kHz to 3MHz Switching Frequency Range
- Automatic Loop Compensation
- Fewer External Components than a Conventional Analog Controller
- Best Transient Performance with Nonlinear Digital Control
- Flexible Phase Assignment for Dual Rails
- Automatic Phase-Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing with Configurable Offsets for Thermal Balance
- Input Voltage and Output Voltage, Current, and Power Monitoring
- Regulator Temperature Monitoring
- V_{IN} UVLO, Output OVP/UVP, OCP, OTP with No Action, Latch, or Hiccup Mode
- Intelli-Phase™ Fault Diagnostics
- Black-Box Record in NVM
- Digital Load-Line Regulation
- Available in a TQFN-56 (7mmx7mm) Package

APPLICATIONS

- SoC/CPU/GPU Power
- AI Power
- Telecom and Networking Systems
- Base Stations

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2882GQNT-xxxx**	TQFN-56 (7mmx7mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MP2882GQNT-xxxx-Z).

**: “xxxx” is the configuration code identifier for the register settings stored in the non-volatile memory (NVM). Each “x” could be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number.

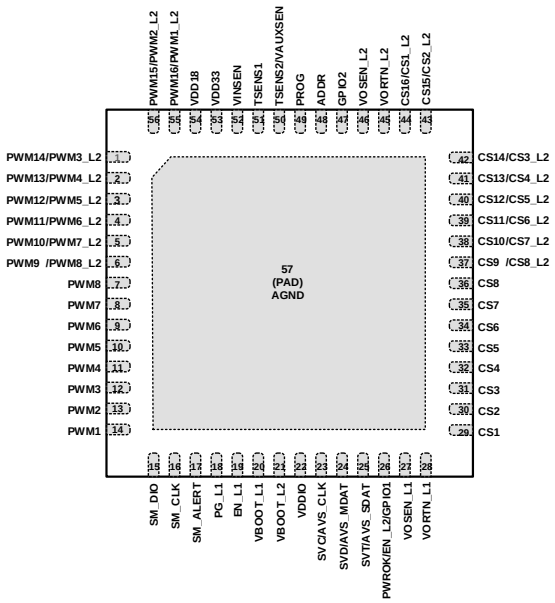
TOP MARKING

MPSYYWW
MP2882
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2882: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



TQFN-56 (7mmx7mm)

PIN FUNCTIONS

Pin #	Name	Type	Description
1	PWM14/ PWM3_L2	D [O]	**PWM for phase 14 on rail 1 (or phase 3 on rail 2).** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
2	PWM13/ PWM4_L2	D [O]	**PWM for phase 13 on rail 1 (or phase 4 on rail 2).** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
3	PWM12/ PWM5_L2	D [O]	**PWM for phase 12 on rail 1 (or phase 5 on rail 2).** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
4	PWM11/ PWM6_L2	D [O]	**PWM for phase 11 on rail 1 (or phase 6 on rail 2).** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
5	PWM10/ PWM7_L2	D [O]	**PWM for phase 10 on rail 1 (or phase 7 on rail 2).** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
6	PWM9/ PWM8_L2	D [O]	**PWM for phase 9 on rail 1 (or phase 8 on rail 2).** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
7	PWM8	D [O]	**PWM for phase 8 on rail 1.** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
8	PWM7	D [O]	**PWM for phase 7 on rail 1.** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
9	PWM6	D [O]	**PWM for phase 6 on rail 1.** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
10	PWM5	D [O]	**PWM for phase 5 on rail 1.** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
11	PWM4	D [O]	**PWM for phase 4 on rail 1.** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
12	PWM3	D [O]	**PWM for phase 3 on rail 1.** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
13	PWM2	D [O]	**PWM for phase 2 on rail 1.** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
14	PWM1	D [O]	**PWM for phase 1 on rail 1.** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
15	SM_DIO	D [I/O]	**PMBus data pin.**
16	SM_CLK	D [I]	**PMBus clock pin.**
17	SM_ALERT	D [O]	**PMBus alert# function.**
18	PG_L1	D [O]	**Power good output for rail 1, rail 2, or both rails.** PG_L1 is an open-drain output.
19	EN_L1	A [I]	**Enable controller for rail 1 or both rails.**
20	VBOOT_L1	A [I]	**Rail 1 boot voltage setting.**
21	VBOOT_L2	A [I]	**Rail 2 boot voltage setting.**
22	VDDIO	A [I]	**I/O bus voltage for AVSBus communication.**
23	AVS_CLK	D [I/O]	**Clock from SoC/CPU (AVSBus communication).**
	SVC	D [I]	**Serial VID clock from the CPU.** The SVC frequency ranges between 3.3MHz and 20MHz.
24	AVS_MDAT	D [I/O]	**Data line from SoC/CPU (AVSBus communication).**
	SVD	D [I/O]	**Serial VID data signal between the CPU and VR controller.**

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
25	AVS_SDAT	D [O]	**Data line from MP2882 to SoC/CPU (AVSBus communication).**
	SVT	D [O]	**Push-pull output.** SVT is the SVI2 telemetry signal from the VR controller to the CPU.
26	EN_L2	A [I]	**Rail 2 enable control for the controller.**
	GPIO1	A [I/O]	**General-purpose input/output.**
	PWROK	D [I]	**System-wide power good signal.** PWROK indicates that all voltage planes and free-running clocks are within specification if PWROK is high.
27	VOSEN_L1	A [I]	**Positive remote voltage-sense input.** VOSEN_L1 is connected to the VR output voltage directly at the load, and should be routed differentially with VORTN_L1.
28	VORTN_L1	A [I]	**Remote voltage-sense return input.** VORTN_L1 is connected to ground directly at the load, and should be routed differentially with VOSEN_L1.
29	CS1	A [I]	**Current-sense input for phase 1 on rail 1.** Float CS the pin of any unused phases.
30	CS2	A [I]	**Current-sense input for phase 2 on rail 1.** Float the CS pin of any unused phases.
31	CS3	A [I]	**Current-sense input for phase 3 on rail 1.** Float the CS pin of any unused phases.
32	CS4	A [I]	**Current-sense input for phase 4 on rail 1.** Float the CS pin of any unused phases.
33	CS5	A [I]	**Current-sense input for phase 5 on rail 1.** Float the CS pin of any unused phases.
34	CS6	A [I]	**Current-sense input for phase 6 on rail 1.** Float the CS pin of any unused phases.
35	CS7	A [I]	**Current-sense input for phase 7 on rail 1.** Float the CS pin of any unused phases.
36	CS8	A [I]	**Current-sense input for phase 8 on rail 1.** Float the CS pin of any unused phases.
37	CS9/CS8_L2	A [I]	**Current-sense input for phase 9 on rail 1 (or phase 8 on rail 2).** Float the CS pin of any unused phases.
38	CS10/CS7_L2	A [I]	**Current-sense input for phase 10 on rail 1 (or phase 7 on rail 2).** Float the CS pin of any unused phases.
39	CS11/CS6_L2	A [I]	**Current-sense input for phase 11 on rail 1 (or phase 6 on rail 2).** Float the CS pin of any unused phases.
40	CS12/CS5_L2	A [I]	**Current-sense input for phase 12 on rail 1 (or phase 5 on rail 2).** Float the CS pin of any unused phases.
41	CS13/CS4_L2	A [I]	**Current-sense input for phase 13 on rail 1 (or phase 4 on rail 2).** Float the CS pin of any unused phases.
42	CS14/CS3_L2	A [I]	**Current-sense input for phase 14 on rail 1 (or phase 3 on rail 2).** Float the CS pin of any unused phases.
43	CS15/CS2_L2	A [I]	**Current-sense input for phase 15 on rail 1 (or phase 2 on rail 2).** Float the CS pin of any unused phases.
44	CS16/CS1_L2	A [I]	**Current-sense input for phase 16 on rail 1 (or phase 1 on rail 2).** Float the CS pin of any unused phases.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
45	VORTN2	A [I]	**Remote voltage-sense return input.** VORTN2 is connected to ground directly at the load, and should be routed differentially with VOSEN2.
46	VOSEN2	A [I]	**Positive remote voltage-sense input.** VOSEN2 is connected to the VR output voltage directly at the load, and should be routed differentially with VORTN2.
47	GPIO2	A [I]	**General-purpose output.**
48	ADDR	A [I]	**PMBus address setting.**
49	PROG	A [I]	**User configuration file selection.** In the non-volatile memory (NVM), there are 16 configuration files. Before loading data from the NVM, the voltage on the PROG pin is sampled by the analog-to-digital converter (ADC). The ADC result determines which file to load from the 16 total files.
50	TSENS2	A [I]	**Rail 2 temperature-sense input.** TSENS2 can be configured to protect rail 2.
	VAUXSEN	A [I]	**General-purpose analog auxiliary voltage sense.** This pin has optional fault detection functions.
51	TSENS1	A [I]	**Rail 1/2 or rail 1 temperature-sense input.** TSENS1 can be configured to protect rail 1 or both rails.
52	VINSEN	A [I]	**Input voltage sense.**
53	VDD33	Power	**3.3V power supply input.** Connect a 1µF bypass capacitor from VDD33 to AGND.
54	VDD18	Power	**1.8V LDO output.** VDD18 provides a power supply for the internal digital circuit. Connect a 1µF bypass capacitor from VDD18 to AGND.
55	PWM16/ PWM1_L2	D [O]	**PWM for phase 16 on rail 1 (or phase 1 on rail 2).** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
56	PWM15/ PWM2_L2	D [O]	**PWM for phase 15 on rail 1 (or phase 2 on rail 2).** Tri-state logic level PWM outputs. Each output is connected to the PWM input of the Intelli-Phase™.
PAD	AGND	A [I/O]	**Analog ground.**

Note:

1) A = analog, D = digital, I = input, O = output, I/O = bidirectional.

ABSOLUTE MAXIMUM RATINGS (1)

VDD33 .....-0.3V to +4.0V
VDD18 .....-0.3V to +2.2V
VORTN1/2…..... -0.3V to +0.3V
CS1~16, PWM1~16, VOSEN_L1, VOSEN_L2, SM_DIO, SM_CLK, SM_ALERT, EN_L1, PWROK/EN_L2/GPIO1, TSENS1/2, PG_L1, GPIO2.....-0.3V to +4.0V
VINSEN, AVS_SDAT/SVT, AVS_MDAT/SVD, AVS_CLK/SVC, PROG, VDDIO, ADDR, VBOOT1/2 .....-0.3V to +2.2V
Junction temperature .....150°C
Lead temperature .....260°C
Storage Temperature..... -65°C to +150°C
Continuous power dissipation (2) 5.02W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM)..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (VDD33) .....3.15V to 3.45V
Operating junction temp (T_J)..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TQFN-56 (7mmx7mm) .....19.9 ..... 6.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (6)

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Remote-Sense Amplifier (Rail 1/2)						
Bandwidth (5)	$GBW_{(RSA)}$			20		MHz
VORTN1/2 current	$I_{RTN1/2}$	EN = 3.3V, VOSEN1/2 = 3V, VORTN1/2 = 0V	-80	-40		µA
VOSEN1/2 current	$I_{VOSEN1/2}$	EN = 3.3V, VOSEN1/2 = 3V, VORTN1/2 = 0V		40	80	µA
Oscillator						
Frequency	f_{OSC}			1.56		MHz
System Interface Control Inputs						
EN (EN_L1)						
Input low voltage	$V_{IL(EN)}$				0.8	V
Input high voltage	$V_{IH(EN)}$		2			V
Enable high leakage current	$I_{IH(EN)}$	EN = 3.3V		3.3		µA
PG_L1						
Output low voltage		Sink 4mA	0		0.2	V
Open-drain leakage current	I_{PGLKG}	V_{PG} = 3.3V			3	µA
Die Temperature Sense (5) (Read at D8h, Page 1)						
Die temperature-sense gain				3		mV/°C
Die temperature-sense offset		T_J = 25°C		0.350		V
Under-Voltage Protection, Over-Voltage Protection Comparator (Rail 1/2, UVP, OVP)						
Relative under-voltage (UV) threshold (V_{VID_UV})	Range	Relative to the DAC reference voltage	75		425	mV
	Resolution/ LSB	3-bit DAC		50		mV
Relative over-voltage (OV) threshold (V_{VID_OV})	Range	Relative to the DAC reference voltage	200		450	mV
	Resolution/ LSB	2-bit DAC		125		mV
TSENS1 Fault Comparator (Protection)						
TSENS1 fault threshold	V_{TH} (V_{TEMP_FLT})			2.2	2.4	V
TSENS2 Threshold Digital-to-Analog Converter (DAC)						
Maximum threshold				2.52		V
Resolution/LSB	ΔDAC_{TSENS2}	6-bit DAC		40		mV

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM Outputs (PWM1~PWM16)						
Output low voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400µA		10	200	mV
Output high voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = -400µA	3.0	VDD33 - 0.02		V
Rising and falling time (6)		C = 10pF		10		ns
PWM tri-state leakage		PWM = 1.5V, EN = 0V	-1		+1	µA
PWM middle state voltage				1.50		V
PWM fault detection source current	$I_{SOURCE(PWM)}$	Need to enter PWM fault detection mode		150		µA
VDD33 Supply						
Supply current	I_{VDD33}	EN = 0 or 1, configured to regular power mode		55	65	mA
		EN = 0, configured to low-power mode		150		µA
Under-voltage lockout threshold (UVLO) threshold voltage		VDD33 is rising		2.89	3.05	V
UVLO threshold voltage		VDD33 is falling	2.6	2.78		V
UVLO hysteresis		VDD33 is falling		110		mV
1.8V Regulator						
1.8V regulator output voltage	VDD18	I_{VDD18} = 0mA, T_J = 25°C	1.79	1.8	1.81	V
1.8V regulator load capability	I_{VDD18}	I_{LOAD} = 30mA		1.77		V
Analog-to-Digital Converter (ADC)						
ADC reference voltage				1.600		V
Resolution/LSB		10-bit ADC		1.5625		mV
DNL (6)		T_J = 25°C		1		LSB
Sample rate (6)				780		kHz
VID DAC (Reference Voltage for Rail 1/2)						
DAC reference voltage		T_J = 25°C	1.592	1.600	1.608	V
Maximum voltage (6)				1.6		V
Resolution/LSB	ΔDAC	10-bit ADC		1.5625		mV
Maximum output voltage slew rate (6)				50		mV/µs
V_{OUT} DC Loop DAC (V_{OUT} Calibration for Rail 1/2)						
Range				240		mV
Resolution/LSB (6)	ΔDAC			0.9375		mV
OCP_SPIKE DAC (Rail 1/2, OCP_SPIKE Protection)						
Range		Adjustable via the PMBus	0.3		1.55	V
Resolution/LSB	ΔDAC_{OC}	8-bit DAC		6.25		mV

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
OCP_PHASE DAC (Rail 1/2, OCP_PHASE Protection)						
Range		Adjustable via the PMBus	1.27		2.48	V
Resolution/LSB		8-bit DAC		5		mV
OVP ABS DAC (Rail 1/2, Absolute OVP)						
Range	FS_{DAC_OVP}	Adjustable via the PMBus	0.5		2.48	V
Resolution/LSB	ΔDAC_{OVP}	8-bit DAC		10		mV
IMON Rail 1/2						
IMON1 ADC reading accuracy		Gain = 1/16, 5kΩ, T_J = 25°C	-1		+1	%
IMON2 ADC reading accuracy		Gain = 1/8, 10kΩ, T_J = 25°C	-1		+1	%
PMBus DC Characteristics (SM_DIO, SM_CLK)						
Input high voltage	V_{IH}	SM_CLK, SM_DIO, for VBUS = 3.3V	2.08			V
		SM_CLK, SM_DIO, for VBUS = 1.8V	1.24			
		SM_CLK, SM_DIO, for VBUS = 1.2V	0.84			
Input low voltage	V_{IL}	SM_CLK, SM_DIO, for VBUS = 3.3V			0.8	V
		SM_CLK, SM_DIO, for VBUS = 1.8V			0.44	
		SM_CLK, SM_DIO, for VBUS = 1.2V			0.32	
Input leakage current		SM_CLK, SM_DIO, SM_ALERT	-10		+10	µA
Output low voltage	V_{OL}	SM_ALERT sinks 2mA			200	mV
Pin capacitance (6)	C_{PIN}				10	pF
PMBus Timing Characteristics (1MHz) (6) (7)						
Operating frequency range			10		1000	kHz
Bus free time		Between a stop and start condition	0.5			µs
Hold time			0.26			µs
Repeated start condition set-up time			0.26			µs
Stop condition set-up time			0.26			µs
Data hold time			0			ns

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, current going into the pin is positive, typical values are T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Data set-up time			50			ns
Clock low timeout			25		35	ms
Clock low period			0.5			µs
Clock high period			0.26		50	µs
Clock/data fall time					120	ns
Clock/data rise time					120	ns
SVI2/AVSBus Interface						
Interface voltage	VDDIO			1.8		V
Interface voltage (SVC, SVD, PWROK) (AVS_CLK, AVS_MDAT)	V_{IH_DC}	Logic high	0.7 x (VDDIO)		VDDIO	V
	V_{IH_AC} (5)				VDDIO + 0.5	
	V_{IL_DC}	Logic low	0		0.4	V
	V_{IL_AC} (5)		-0.5			
	V_{HYST}	Hysteresis	50			mV
Output high voltage (SVT)	V_{OH_DC}	I_{OH} = 4mA	VDDIO - 0.2		VDDIO	V
Output low voltage (SVT)	V_{OL_DC}	I_{OL} = 4mA	0		0.2	V
Leakage current (SVC, SVD, PWROK) (AVS_CLK, AVS_MDAT, AVS_SDAT)	I_L	0V to 1.8V	-10		+10	µA
Pin capacitance (SVC, SVD, SVT) (AVS_CLK, AVS_MDAT, AVS_SDAT)	C_{PIN}				5	pF
Buffer on resistance (AVS_SDAT)	R_{ON}			14		Ω
Slew rate (5) (AVS_CLK, AVS_MDAT, AVS_SDAT)		2nH, 10pF load	0.5		2	V/ns
VR clock to data delay (6)			4		8.3	ns
Set-up time (6)				7		ns
Hold time (6)				14		ns

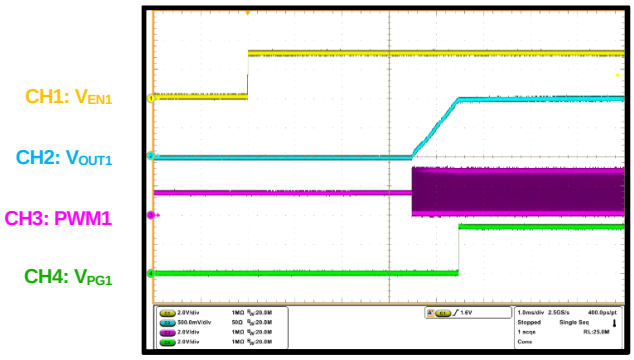
Notes:

5) Guaranteed by design or characterization data. Not tested in production.
6) The device supports 100kHz, 400kHz, and 1MHz bus speeds. The PMBus timing parameters in this table are for operation at 1MHz. If the PMBus operating frequency is between 100kHz and 400kHz, refer to the SMBus specification for timing parameters.

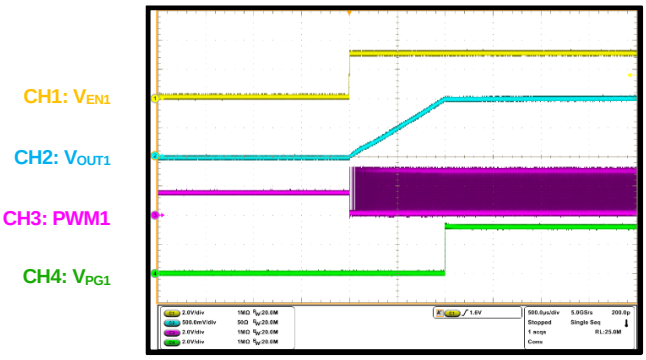
TYPICAL PERFORMANCE CHARACTERISTICS

Rail 1: 13-phase, V_{IN} = 12V, V_{OUT1} = 1V, f_{SW1} = 500kHz, L1 = 150nH, C_{OUT1} = 28 x 470µF + 140 x 22µF.
Rail 2: 3-phase, V_{IN} = 12V, V_{OUT2} = 1V, f_{SW2} = 500kHz, L2 = 150nH, C_{OUT2} = 16 x 470µF+88 x 22µF, unless otherwise noted.

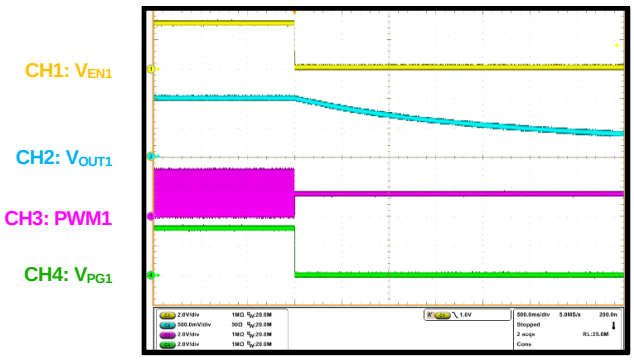
Rail 1 Enable On
Low-power mode, t_{ON} delay = 0s



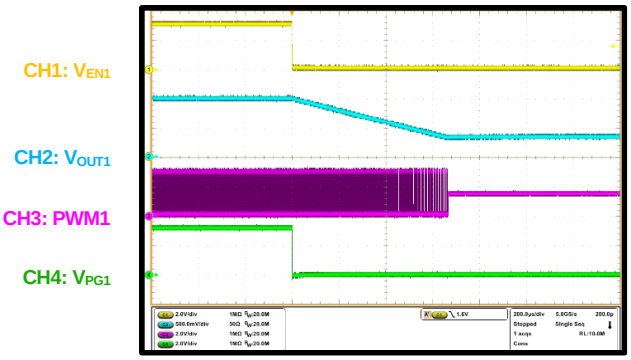
Rail 1 Enable On
Regular power mode, t_{ON} delay = 0s



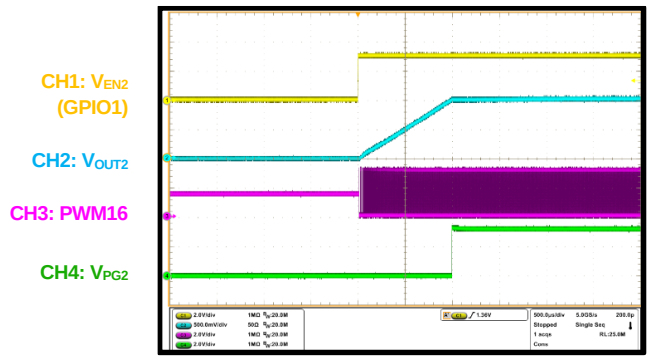
Rail 1 Enable Off
Hi-Z off



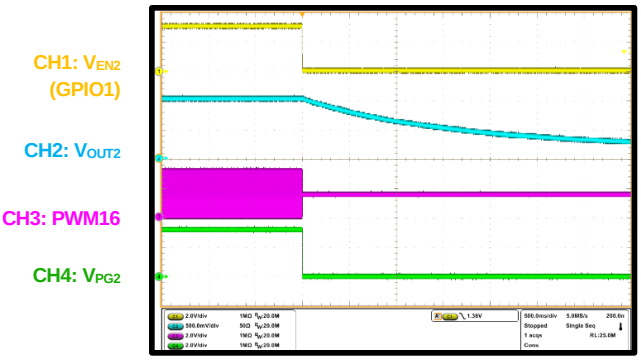
Rail 1 Enable Off
Soft-off with 1mV/µs



Rail 2 Enable On
Regular power mode, t_{ON} delay = 0s



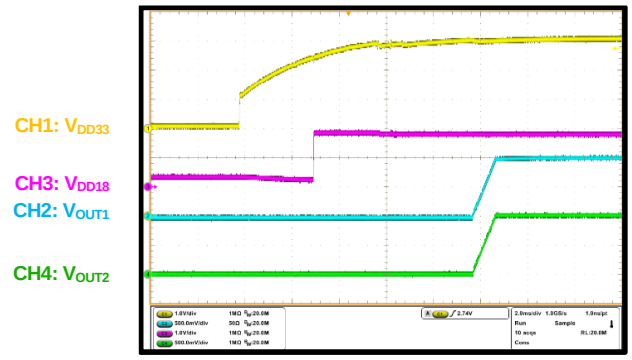
Rail 2 Enable Off
Hi-Z off



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

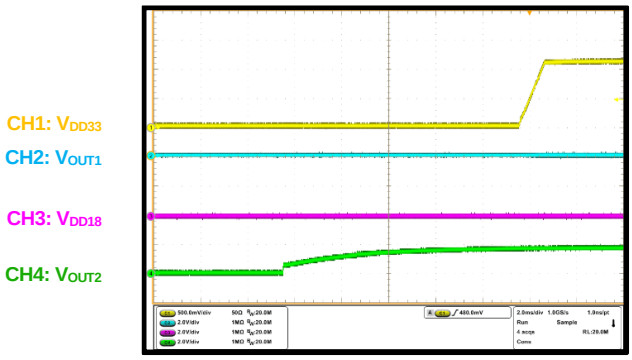
Rail 1: 13-phase, V_{IN} = 12V, V_{OUT1} = 1V, f_{SW1} = 500kHz, L1 = 150nH, C_{OUT1} = 28 x 470µF + 140 x 22µF. Rail 2: 3-phase, V_{IN} = 12V, V_{OUT2} = 1V, f_{SW2} = 500kHz, L2 = 150nH, C_{OUT2} = 16 x 470µF+88 x 22µF, unless otherwise noted.

VDD33 On



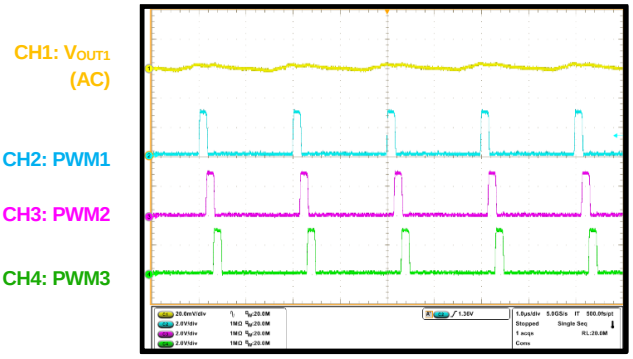
Boot-Up Sequence in SVI2 Mode

V_{BOOT} = 1.1V, boot slew rate = 1mV/µs



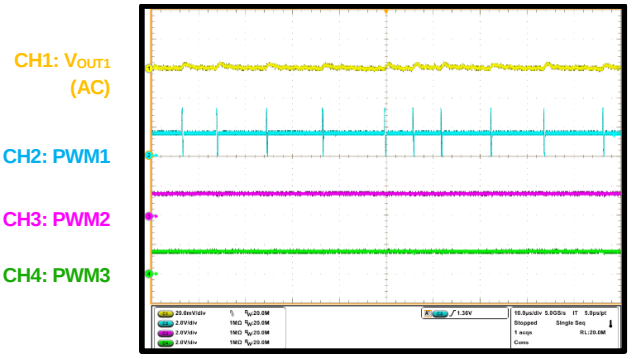
Steady State

13-phase CCM, I_{OUT1} = 0A



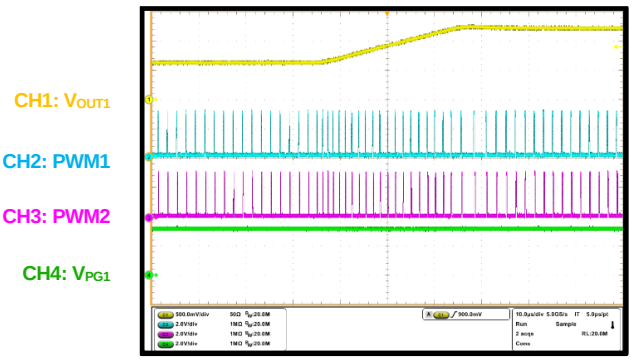
Steady State

1-phase DCM, I_{OUT1} = 1A



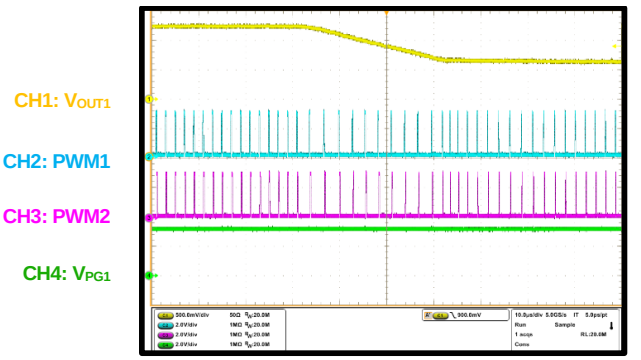
DVID Up

DVID from 0.6V to 1.2V, SR = 20mV/µs



DVID Down

DVID from 1.2V to 0.6V, SR = 20mV/µs

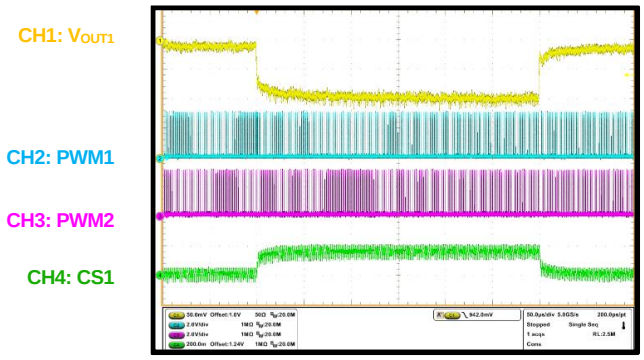


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Rail 1: 13-phase, V_{IN} = 12V, V_{OUT1} = 1V, f_{SW1} = 500kHz, L1 = 150nH, C_{OUT1} = 28 x 470µF + 140 x 22µF.
Rail 2: 3-phase, V_{IN} = 12V, V_{OUT2} = 1V, f_{SW2} = 500kHz, L2 = 150nH, C_{OUT2} = 16 x 470µF+88 x 22µF, unless otherwise noted.

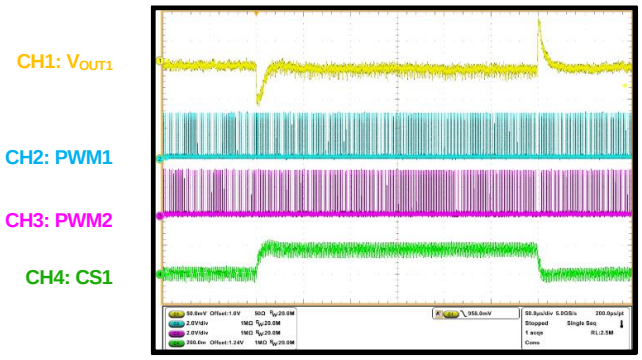
Load Transient with DC Load Line

R_{LL} = 0.47mΩ, 0A to 200A at 200A/µs



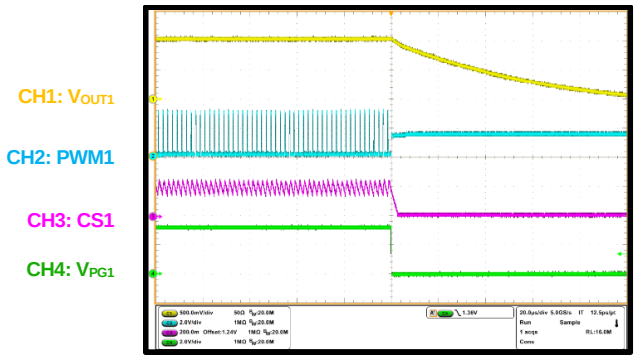
Load Transient with AC Load Line

R_{LL} = 0mΩ, 0A to 200A at 200A/µs



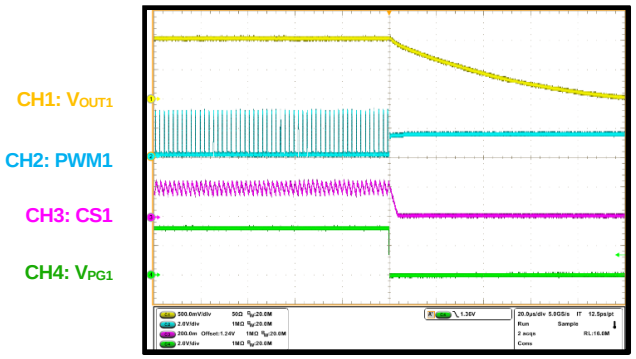
OCP_TDC

OCP_TDC = 200A,
OCP_TDC action delay = 18µs, latch-off mode



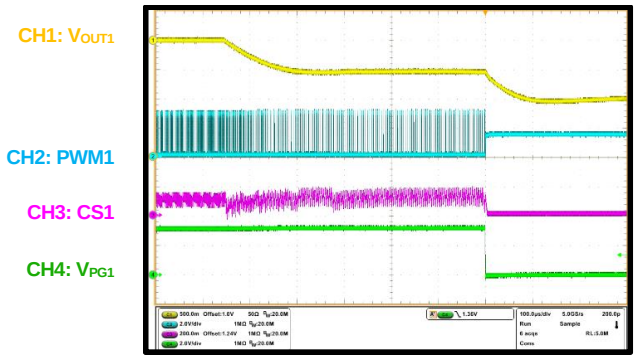
OCP_SPIKE

OCP_SPIKE = 240A,
OCP_SPIKE action delay = 9µs, latch-off mode



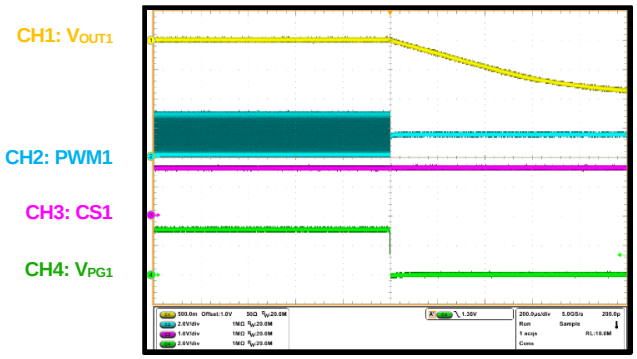
UVP

UVP delay = 500µs, latch-off mode



OTP

OTP threshold = 120°C, latch-off mode



FUNCTIONAL BLOCK DIAGRAM

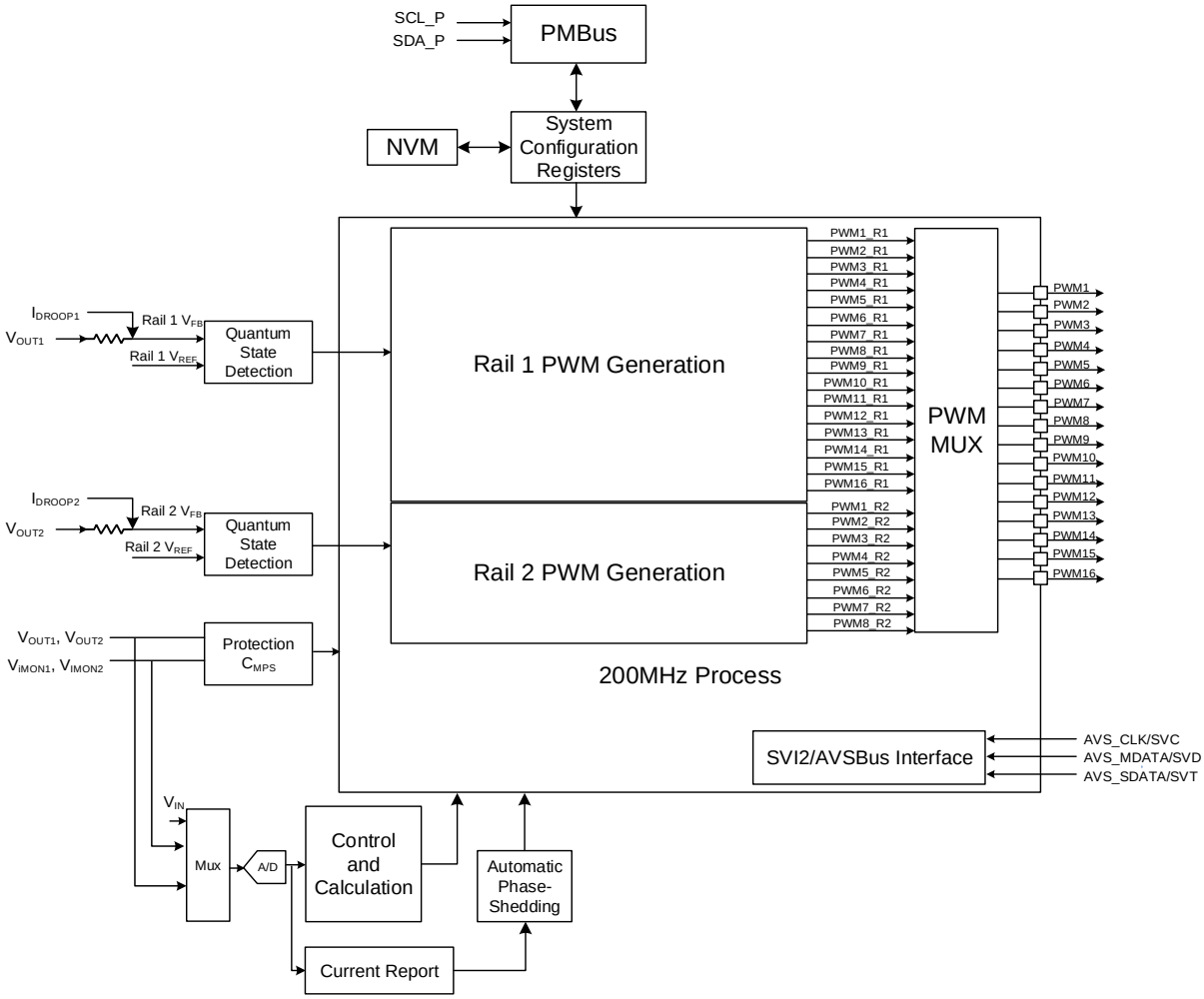


Figure 1: System Functional Block Diagram

OPERATION

The MP2882 is a dual-output, digital, multi-phase VR controller for general-purpose multi-phase voltage regulators. The device can implement adaptive phase-shedding and phase-adding according to the load current to improve overall VR efficiency. The MP2882 contains a precision digital-to-analog converter (DAC) and analog-to-digital converter (ADC), a differential remote voltage-sense amplifier, fast comparators, current sense, internal slope compensation, digital load-line setting, PGOOD monitoring, temperature monitoring, a PMBus/I^{2}C interface, and a non-volatile memory (NVM) for custom configurations.

Fault protection features include V_{IN} under-voltage lockout (UVLO), over-current protection based on the TDC (OCP_TDC), OCP based on ICCSPIKE/EDC/ICCMAX (OCP_SPIKE), cycle-by-cycle phase current OCP (OCP_PHASE), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP). The MP2882 can also detect the fault type of the Intelli-Phase™ if a protection occurs. The MP2882 can record all faults to the NVM automatically in the event that the power supply shuts off while a fault is occurring.

Pulse-Width Modulation (PWM) Control and Switching Frequency

The MP2882 applies MPS's unique digital pulse-width modulation (PWM) control to provide fast load transient response and simple loop compensation. The switching frequency can (f_{SW}) be set with PMBus command FREQUENCY_SWITCH (33h).

The PWM on time (t_{ON}) of each phase updates in real time according to the input voltage (V_{IN}), output voltage (V_{OUT}), and adaptive phase f_{SW}. t_{ON} can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

Where V_{OUT} is the real-time output voltage, V_{IN} is the input voltage, and f_{SW} is the switching frequency set by FREQUENCY_SWITCH (33h).

System Configuration

The MP2882 provides a V_{IN} sense and differential V_{OUT} sense. It can work with Intelli-Phase™ (MPS's DrMOS) devices to sense the phase current, total load current, and the maximum temperature among the Intelli-Phase™ devices with a minimal number of external components. To achieve pre-biased functions, the MP2882's PWM outputs Hi-Z middle-state signals before outputting power to the load.

The PMBus slave address can be set up by ADDR pin or by the register via the PMBus.

The MP2882 provides a maximum of 16 PWMs that can be configured for different phase count applications on rail 1 and rail 2.

Table 1 shows phase-setting examples. Applications include, but are not limited to, these examples.

Table 1: Phase Count Configuration and Active PWM Pins

Phase Count Registers		Active PWM Pins	
B4h on Page 0, Bits[4:0]	B4h on Page 1, Bits[3:0]	Rail 1	Rail 2
5'b10000	4'b0000	1~16	N/A
5'b01111	4'b0001	1~15	16
5'b01110	4'b0010	1~14	16~15
5'b00101	4'b0011	1~13	16~14
5'b00100	4'b0100	1~12	16~13
5'b00011	4'b0101	1~11	16~12
5'b00010	4'b0110	1~0	16~11
5'b00010	4'b0111	1~9	16~10
5'b00010	4'b1000	1~8	16~9

Rail 2 can be set to a maximum of 8 phases. If rail 1 is configured to 0 phases, rail 1 operates in 1-phase DCM. If rail 2 is configured to 0 phases, rail 2 is disabled.

Any unused PWM enters tri-state. The active phase is interleaved automatically. Float the unused PWM and CS pins.

If rail 2 is not used, connect the related rail 2 pins using the steps below:

1. Tie VBOOT2 to GND.
2. Pull EN_L2/GPIO1 up to 3.3V with a 4.7kΩ resistor to use the GPIO1 function.

3. Connect VOSEN2 and VORTN2 to AGND.

If the CS pins are enabled to configure the phase number, register B4h, bits[4:0] on Page 0, and register B4h, bits[3:0] on Page 1 are ignored. Pull the unused CS pins down to ground. This function can be enabled with B4h, bit[13] on Page 1.

After EN is pulled high, the MP2882 checks the voltage on the CS pins sequentially (from CS1 to CS16) until it finds the first low voltage. Figure 2 shows an example of the connection for a 13-phase application. The first low voltage is on CS14, which means that phases 14, 15, and 16 are disabled. Any CSx (1 ≤ x ≤ 16) pin connected to GND means that the all phases from phase x to phase 16 all disabled.

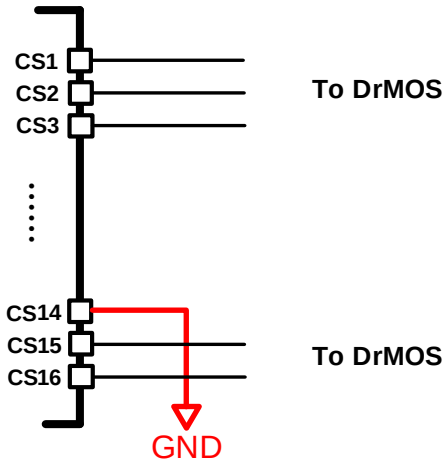


Figure 2: CS Pin Configurations

Non-Volatile Memory (NVM) Operation

The MP2882 uses the non-volatile memory (NVM) for storing the application configuration parameters. The default values are pre-configured at the factory.

The configurations are restored from the NVM during the start-up sequence, or by receiving the RESTORE_USER_ALL (16h) command from the PMBus. Figure 2 shows the MP2882's state machine diagram.

NVM operation can be easily accomplished with MPS's GUI software, which can be downloaded from the MPS website. The NVM can be subjected to more than 1000 erase/write cycles.

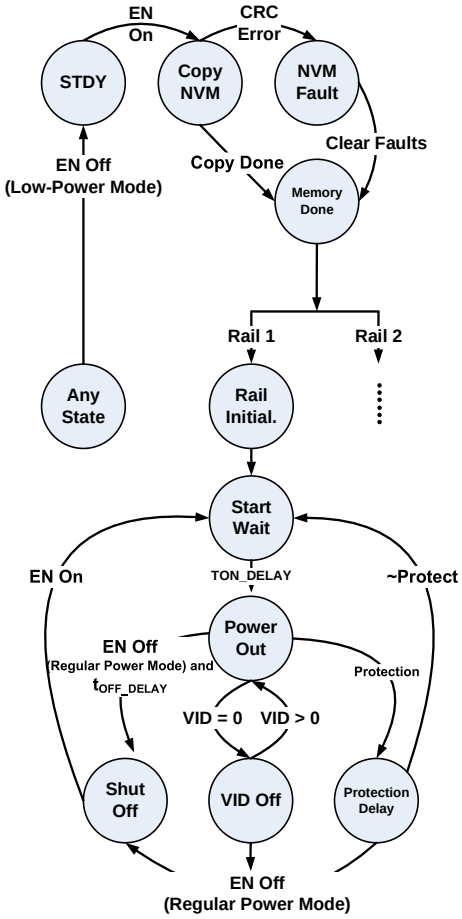


Figure 3: System State Machine

Automatic Slope Function

The MP2882 provides an automatic slope function. After the MTP is copied, the system automatically calculates the slope value once. This function is enabled by setting AUTO_SLOPE_EN (C1h on Page 0), bit[15] to 1 and set the MFR_SLOPE_PEAK_SET, (BFh), bits[8:5] to 15 to select the automatic slope parameters. The automatic slope parameter calculation depends on the frequency value, which is set by MFR_FREQUENCY_SWITCH (33h on Page 0 and Page 1), as well as the blanking time set by registers BBh, BCh, and BDh. The peak ramp value is set by register BFh, bits[4:0], which is 1.875mV/LSB.

To select the manual mode slope, disable the automatic slope function by setting AUTO_SLOPE_EN to 0. Then set MFR_SLOPE_PEAK_SET (BFh), bits[8:5] to 0, 1, 2, or 3 to select a slope value using C3h~CDh on Page 0.

NVM Fault

If the data in the NVM is determined to be invalid by the cyclic redundancy check (CRC) during the system initialization process, the system enters an NVM fault state without PWM switching. The MP2882 waits for the clear faults command, and the NVM configurations are ignored.

There are two ways to clear an NVM fault and reinitiate start-up with the default values in the register:

1. Clear the NVM fault via the PMBus.
2. Store the configurations to the NVM and restart the device.

Low-Power Mode

The MP2882 can be configured for low-power mode or regular power mode via register MFR_VR_CONFIG1 (B7h on Page 0), bit[15].

In low-power mode, PMBus communication is disabled and the quiescent current (I_Q) drops to 150µA when EN goes low.

In regular power mode, PMBus communication is available when EN is low.

Wait State

After system initialization, the MP2882 begins the t_{ON} delay period and the soft start (SS) process. If any of the following conditions occur, the MP2882 enters the corresponding wait state:

1. A protection is triggered (such as if the sensed V_{IN} falls below the VIN_UVLO_OFF threshold), or the sensed temperature exceeds the OTP threshold. The MP2882 enters the set protection mode (hiccup or retry mode) and waits for the fault to clear. Then the device enters the protection delay state for about 12.5ms before the next start-up/restart cycle.
2. The OPERATION off command is received via the PMBus. The MP2882 shuts down until it receives the on command from the PMBus master.
3. VID is commanded off. The MP2882 enters the VID off state, and there is no PWM output until the VID command exceeds the off level. The SS process begins immediately after exiting the VID off state.
4. EN turning off shuts down the MP2882.

Start-Up Sequence

The MP2882 is supplied by a 3.3V voltage at VDD33. VDD33 provides the bias supply for the analog circuit and the internal 1.8V LDO, which powers the digital circuit. The system is reset by the internal power-on reset signal (POR) after the VDD33 supply is ready. After the system exits POR, the data in the NVM is loaded into the operating registers to configure the VR operation. Figure 4 on page 19 shows the start-up sequence in regular power mode, described below:

t0 to t1: At t0, VDD33 is supplied by a 3.3V voltage. VDD33 reaches the under-voltage lockout (UVLO) threshold at t1. VDD18 reaches 1.8V when the VDD33 pin exceeds 1.8V.

t1 to t2: At t1, the data in the NVM starts loading into the operating registers. The entire NVM copying process takes about 1.5ms. During this process, if the voltage on the ADDR pin was selected to set the PMBus address, the PMBus address is detected.

t2 to t3: At t2, the MP2882 waits for the EN pin to be pulled high once NVM copying is finished. The PMBus is available at this stage.

t3 to t4: After the EN pin pulls high, rail 1 stops and waits for an on command if the PMBus OPERATION (01h on Page 0) command is preset to the off state. If OPERATION is set to the on state, the turn-on delay time (t_{ON} delay) starts counting. The delay time can be configured to be between 0ms and 3.1ms with PMBus command TON_DELAY (9Fh), bits [15:11].

t4 to t5: When the t_{ON} delay expires, the rail VID DAC starts ramping up the reference voltage (V_{REF}) to the boot-up voltage with the configured slew rate. During SS, OCP_TDC, OVP and UVP are masked until V_{REF} reaches the target value. The rail start-up sequence is complete at t5. Then the rail is ready to output power, and the start-up sequence of all rails is complete.

Figure 5 on page 19 shows the start-up sequence in low-power mode.

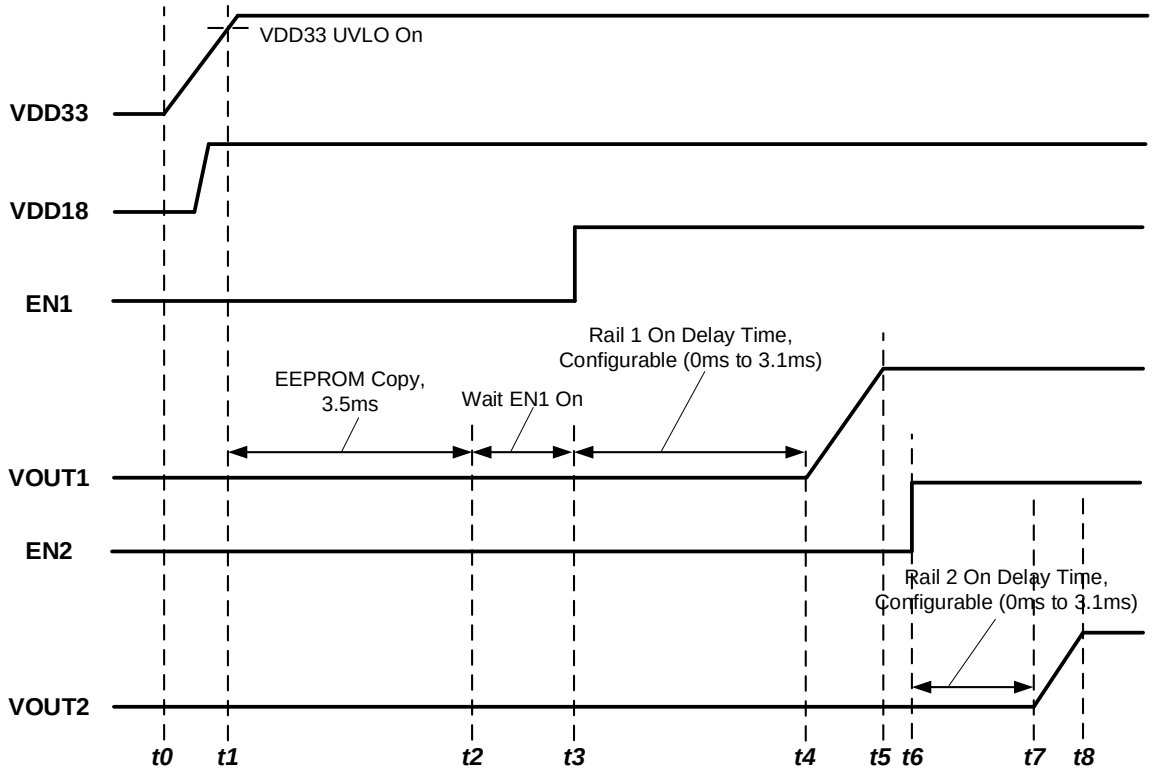


Figure 4: Start-Up Sequence in Regular Power Mode

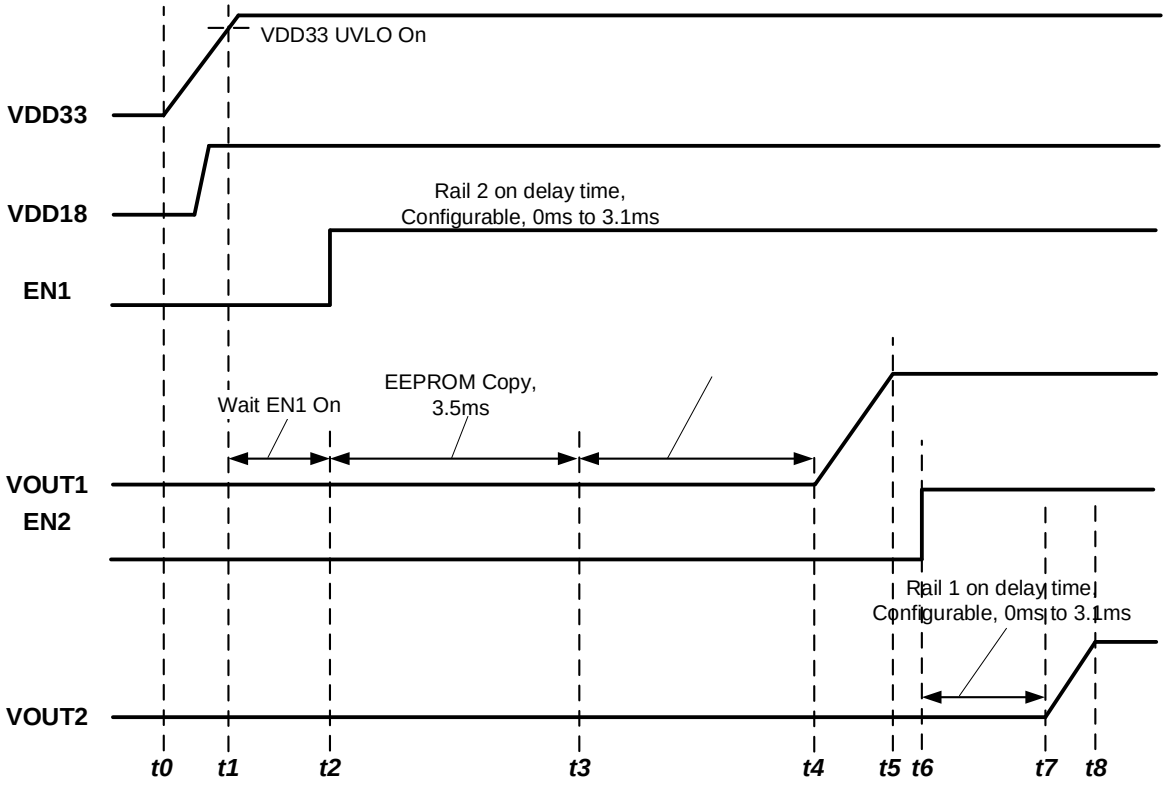


Figure 5: Start-Up Sequence in Low-Power Mode

Shutdown

The MP2882 can be shut down by the OPERATION command, the EN pin, VDD33 under-voltage lockout (UVLO), or a protection. These shutdown methods are described below:

1. VDD33 shutdown: If the power supply on the VDD33 pin falls below the VDD33 UVLO falling threshold, the MP2882 shuts down immediately.
2. EN pin off: The MP2882 provides Hi-Z and soft shutdown with a selectable slew rate when the EN pin goes low in regular power mode. During soft shutdown, V_{OUT} ramps down with the selected slew rate until V_{REF} falls to the VID shutdown level set by register MFR_SD_VID_SET (C5h on Page 1), bits[7:0]. Then all PWMs enter tri-state.

   If the EN pin goes low in low-power mode, the MP2882 initiates Hi-Z off immediately without a turn-off delay. The device enters standby mode with the smallest possible power consumption. The PMBus is unavailable until either EN pin is pulled high.
3. OPERATION command off: The MP2882 provides Hi-Z off and soft shutdown after receiving an OPERATION off command. When the OPERATION command is set to Hi-Z, all PWMs enter tri-state after an off command is received. Then V_{OUT} is discharged by the load current. When OPERATION commands a soft shutdown, V_{OUT} initiates the shutdown with the slow slew rate until V_{REF} reaches the VID shutdown level. Then all PWMs enter tri-state.
4. Protection shutdown: If V_{IN} over-voltage protection (OVP), V_{IN} UVLO, V_{OUT} under-voltage protection (UVP), over-current protection (OCP_SPIKE or OCP_TDC), over-temperature protection (OTP), a CS fault, or a VTEMP fault from the Intelli-Phase™ is triggered, the VR enters Hi-Z off immediately. Once the V_{OUT} OVP threshold is triggered, the VR turns on all the active low-side MOSFETs (LS-FETs) to discharge C_{OUT}, then immediately shuts down until V_{OUT} falls below the reverse voltage protection (RVP) threshold (about 160mV).

Figure 6 shows the EN pin soft shutdown power sequence in regular power mode.

Figure 7 shows the EN pin Hi-Z off power sequence in low-power mode. When the EN pins are pulled low, the VR shuts down immediately.

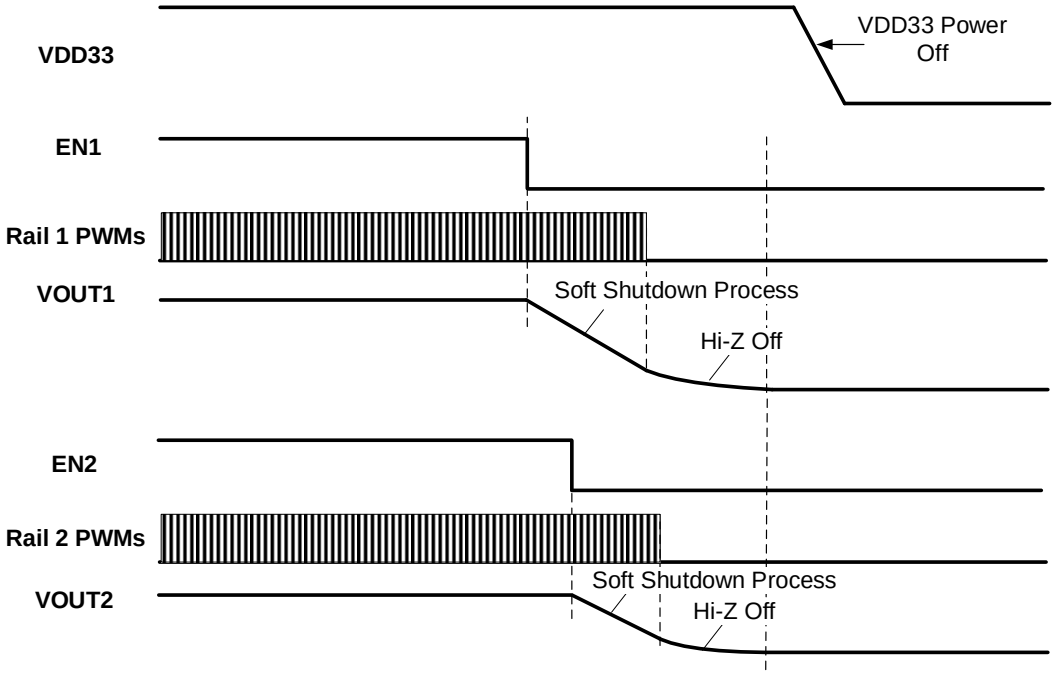


Figure 6: Shutdown Sequence in Regular Power Mode with Soft Shutdown

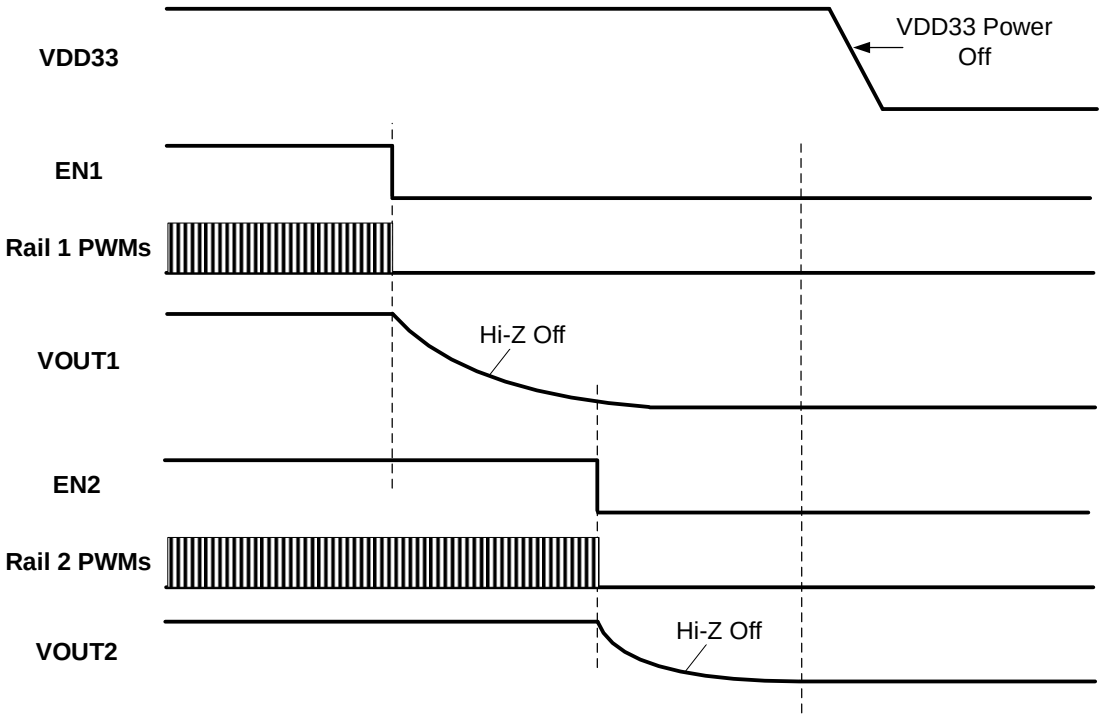


Figure 7: Shutdown Sequence in Low Power Mode with Hi-Z Off

Power Good (PG) Indication

The MP2882 indicates the power good (PG) status with the PG_L1 pin. The PG_L1 pin can be configured to PG1 or PG1 and PG2. It can be configured via the MFR_GPIO_SEL (B5h on Page 0).

During soft start, when V_{REF} reaches the VID value, the MP2882 starts the delay time counter and asserts PG after the delay time ends. The delay time is configurable via MFR_PG_DELAY (B6h), bits[9:0].

If the MP2882 is in a Hi-Z off or soft shutdown state for a fault protection, a PMBus OPERATION off command, or if EN is pulled low, then thee PG pin is de-asserted after a configurable delay time. This time can also be configured by MFR_PG_DELAY (B6h), bits[15:10].

Figure 8 shows power good indication in regular power mode.

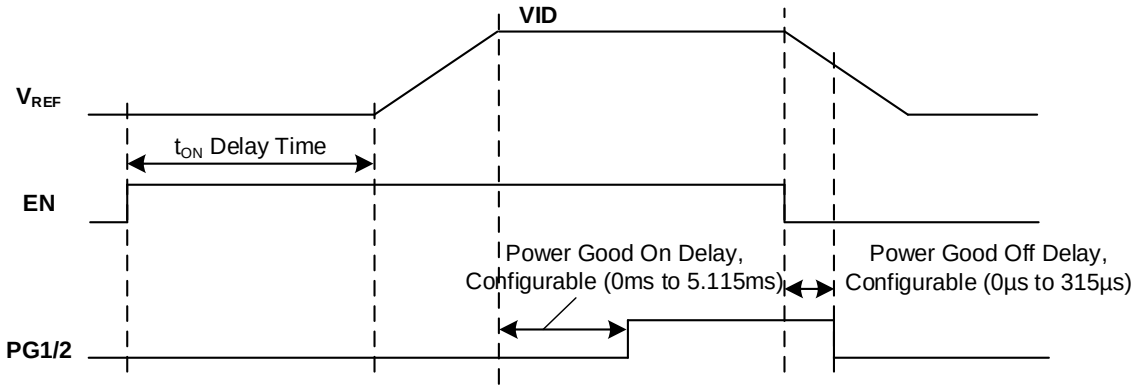


Figure 8: Power Good On/Off Sequence in Regular Power Mode with EN Soft Shutdown

Voltage Reference

The MP2882 has two 10-bit VID DACs that provide V_{REF} for the individual output. V_{REF} is in VID format with 6.25mV, 5mV, 2mV, 1.953125mV, or 3.90625mV per step, and ranges from 0V to 1.6V.

The MP2882 provides three different VID control modes: PMBus mode, SVI2 mode, and AVSBus mode. The VID control starts with VID mode selection.

Figure 9 shows the VID control related commands.

There are two VID mode selection bits and related registers:

- SVI2_EN: MFR_VR_CONFIG3 (A2h), bit[9]
- AVSBus_EN: OPERATION (01h)

After VID mode selection, the commanded voltage is added to the offset voltage. Then this value is compared to the V_{OUT} limits set by the VOUT_MAX (24h) and VOUT_MIN (2Bh). If the calculated voltage creates a V_{OUT} that exceeds VOUT_MAX or is below VOUT_MIN, the PMBus device limits V_{OUT} to VOUT_MAX and VOUT_MIN. The PMBus ALERT# pin can be asserted as a warning to the master.

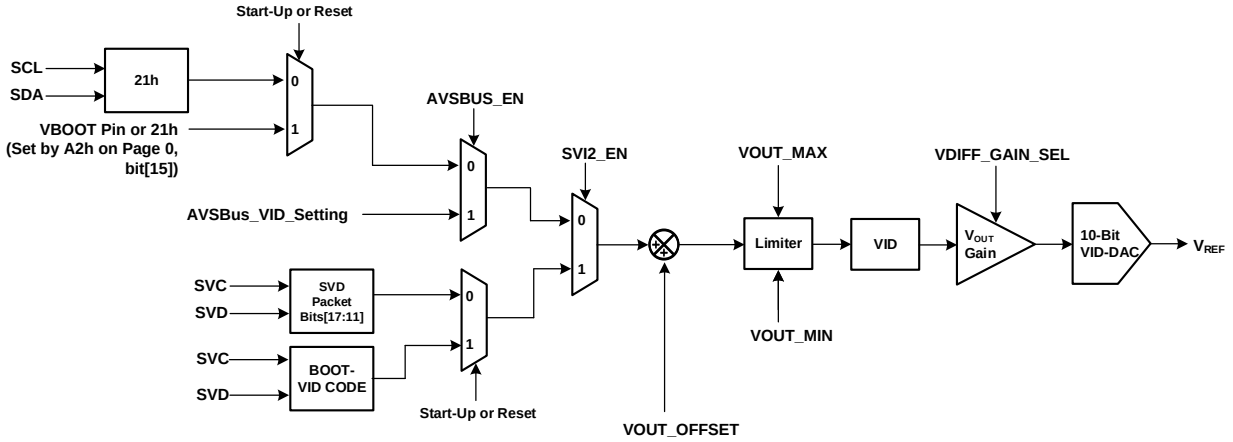


Figure 9: VID Control Related Commands

Output Voltage Setting

Figure 10 shows that the voltage at the load is sensed with the differential voltage-sense amplifier. This type of sensing improves load regulation. The remote-sense amplifier gain can be configured to be 1, 0.5, 0.8, or 0.4 by PMBus command MFR_VOUT_LOOP_CTRL (B2h).

The VOUT_TRIM (22h) commands on Page 0 and Page 1 (for rail 1 and rail 2, respectively) can add a voltage offset. This fine-tunes V_{OUT} (at 1 VID step/LSB) by adding or subtracting an offset from the remote sensed V_{OUT}. Fine-tuning can adjust V_{OUT} and improve V_{OUT} accuracy for the end user's system.

This register cannot be stored in the NVM, and must be changed on the fly.

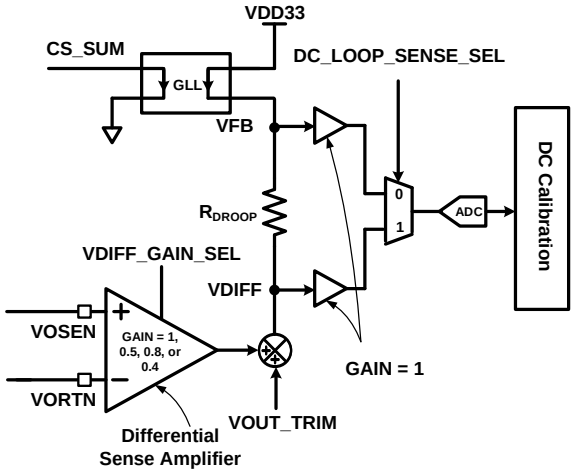


Figure 10: DC Loop Gain Selection

After trimming the voltage, the MP2882 senses on V_{DIFF} or V_{FB} with ADC for DC voltage calibration. This provides accurate voltage regulation. Table 2 shows the voltage supporting range for different VID steps and voltage-sense gains.

Table 2: Voltage Support Range

VID Step (B2h, Bits[15:14])	V_{DIFF} Gain (B2h, Bits[11:10])	V_{OUT} Range
5mV	1	0V to 1.55V
6.25mV		
5mV	0.5	0V to 3V
6.25mV		
5mV	0.8	0V to 2V
1.953125mV		
5mV	0.4	0V to 3.3V
3.90625mV		

VBOOT Setting

The VBOOT pin voltage (V_{BOOT}) setting has two forms of selection: one method provides 31 V_{BOOT} values (31 type), and the second provides 230 V_{BOOT} values (230 type). The V_{BOOT} selection type can be configured by MFR_PRE_CFG (0Fh on Page 1) bits[2:1]. Set MFR_PRE_CFG to 10 for 31 type, or set it to 11 for 230 type.

If 31 type is selected, the voltage divider on VDD18 can set V_{BOOT}.

In this scenario, if the VBOOT pin is connected to GND, V_{BOOT} is set by VOUT_COMMAND (21h). Otherwise, V_{BOOT} is determined by the VBOOT pin's voltage. If the V_{DIFF} gain = 0.8 and the VID step = 1.953125mV, V_{BOOT} is between 0.5V and 2V, with 50mV per step.

Table 3 shows the recommended values for V_{BOOT} when using the 31 type method.

The 230 type is set by the voltage divider from VDD18, as well as the internal 20µA current source. If the V_{DIFF} gain = 0.8, the VID step = 1.953125mV, and V_{BOOT} ranges between 0.203125V and 2V, with 7.8125mV per step.

Table 4 on page 24 shows the recommended values for V_{BOOT} when using the 230 type method.

Table 3: 31 Type V_{BOOT} Setting

V_{BOOT} (V)	Pin Setting Voltage (V)	R_{TOP} 1% (kΩ)	R_{BOTTOM} 1% (kΩ)
Set by 21h, bits[9:0]	0	-	0
0.5	0.102	3.32	0.2
0.55	0.126	3.32	0.249
0.6	0.150	3.32	0.301
0.65	0.175	3.32	0.357
0.7	0.199	3.32	0.412
0.75	0.221	3.32	0.464
0.8	0.245	3.32	0.523
0.85	0.272	3.32	0.59
0.9	0.300	3.32	0.665
0.95	0.332	3.32	0.75
1	0.358	3.32	0.825
1.05	0.394	3.32	0.931
1.1	0.423	3.32	1.02
1.15	0.457	3.32	1.13
1.2	0.498	3.32	1.27
1.25	0.542	3.32	1.43
1.3	0.590	3.32	1.62
1.35	0.637	3.32	1.82
1.4	0.687	3.32	2.05
1.45	0.740	3.32	2.32
1.5	0.802	3.32	2.67
1.55	0.868	3.32	3.09
1.6	0.933	3.32	3.57
1.65	1.007	3.32	4.22
1.7	1.081	3.32	4.99
1.75	1.152	3.32	5.9
1.8	1.229	3.32	7.15
1.85	1.301	3.32	8.66
1.9	1.383	3.32	11
1.95	1.468	3.32	14.7
2	1.559	3.32	21.5

Table 4: 230 Type V_{BOOT} Setting

Set Point	V_{BOOT} (V)	R_{TOP} 1% (kΩ)	R_{BOTTOM} 1% (kΩ)	Set Point	V_{BOOT} (V)	R_{TOP} 1% (kΩ)	R_{BOTTOM} 1% (kΩ)
1	0.203125	NA	0	51	0.6015625	330	17.8
2	0.2109375	32.4	1.27	52	0.609375	402	21.5
3	0.2265625	53.6	2.1	53	0.6171875	487	26.1
4	0.234375	76.8	3	54	0.625	576	30.9
5	0.2421875	105	4.12	55	0.6328125	698	37.4
6	0.25	137	5.36	56	0.640625	820	44.2
7	0.2578125	174	6.81	57	0.6484375	976	52.3
8	0.265625	220	8.66	58	0.65625	1150	62
9	0.2734375	270	10.5	59	0.6640625	1370	73.2
10	0.28125	330	13	60	0.671875	1.5	0.0953
11	0.2890625	402	15.8	61	0.6796875	15	0.953
12	0.296875	487	19.1	62	0.6875	32.4	2.05
13	0.3046875	576	22.6	63	0.6953125	53.6	3.4
14	0.3125	698	27.4	64	0.703125	76.8	4.87
15	0.3203125	820	32.4	65	0.7109375	105	6.65
16	0.328125	976	38.3	66	0.71875	137	8.66
17	0.3359375	1150	45.3	67	0.7265625	174	11
18	0.34375	1370	53.6	68	0.734375	220	14
19	0.3515625	1600	62	69	0.7421875	270	17.4
20	0.359375	1870	73.2	70	0.75	330	21
21	0.3671875	1.5	0.0698	71	0.7578125	402	25.5
22	0.375	15	0.698	72	0.765625	487	30.9
23	0.3828125	32.4	1.5	73	0.7734375	576	36.5
24	0.390625	53.6	2.47	74	0.78125	698	44.2
25	0.3984375	76.8	3.57	75	0.7890625	820	52.3
26	0.40625	105	4.87	76	0.796875	976	62
27	0.4140625	137	6.34	77	0.8046875	1150	73.2
28	0.421875	174	8.06	78	0.8125	1.5	0.113
29	0.4296875	220	10.2	79	0.8203125	15	1.13
30	0.4375	270	12.4	80	0.828125	32.4	2.43
31	0.4453125	330	15	81	0.8359375	53.6	4.02
32	0.453125	402	18.7	82	0.84375	76.8	5.76
33	0.4609375	487	22.6	83	0.8515625	105	7.87
34	0.46875	576	26.7	84	0.859375	137	10.2
35	0.4765625	698	32.4	85	0.8671875	174	13
36	0.484375	820	37.4	86	0.875	220	16.5
37	0.4921875	976	45.3	87	0.8828125	270	20.5
38	0.5	1150	52.3	88	0.890625	330	24.7
39	0.5078125	1370	63.4	89	0.8984375	402	30.1
40	0.515625	1600	73.2	90	0.90625	487	36.5
41	0.5234375	1.5	0.0806	91	0.9140625	576	43.2
42	0.53125	15	0.806	92	0.921875	698	52.3
43	0.5390625	32.4	1.74	93	0.9296875	820	61.9
44	0.546875	53.6	2.87	94	0.9375	976	73.2
45	0.5546875	76.8	4.12	95	0.9453125	1.5	0.133
46	0.5625	105	5.62	96	0.953125	15	1.33
47	0.5703125	137	7.32	97	0.9609375	32.4	2.87
48	0.578125	174	9.31	98	0.96875	53.6	4.75
49	0.5859375	220	11.8	99	0.9765625	76.8	6.81
50	0.59375	270	14.7	100	0.984375	105	9.31

Set Point	V_{BOOT} (V)	R_{TOP} 1% (kΩ)	R_{BOTTOM} 1% (kΩ)	Set Point	V_{BOOT} (V)	R_{TOP} 1% (kΩ)	R_{BOTTOM} 1% (kΩ)
101	0.9921875	137	12.1	151	1.3828125	402	60.4
102	1	174	15.4	152	1.390625	487	73.2
103	1.0078125	220	19.6	153	1.3984375	1.5	0.267
104	1.015625	270	24	154	1.40625	15	2.67
105	1.0234375	330	29.4	155	1.4140625	32.4	5.76
106	1.03125	402	35.7	156	1.421875	53.6	9.53
107	1.0390625	487	43.2	157	1.4296875	76.8	13.7
108	1.046875	576	51.1	158	1.4375	105	18.7
109	1.0546875	698	61.9	159	1.4453125	137	24.3
110	1.0625	820	73.2	160	1.453125	174	30.9
111	1.0703125	1.5	0.158	161	1.4609375	220	39.2
112	1.078125	15	1.58	162	1.46875	270	47.5
113	1.0859375	32.4	3.4	163	1.4765625	330	59
114	1.09375	53.6	5.62	164	1.484375	402	71.5
115	1.1015625	76.8	8.06	165	1.4921875	1.5	0.324
116	1.109375	105	11	166	1.5	15	3.24
117	1.1171875	137	14.3	167	1.5078125	32.4	6.98
118	1.125	174	18.2	168	1.515625	53.6	11.5
119	1.1328125	220	23.2	169	1.5234375	76.8	16.5
120	1.140625	270	28.7	170	1.53125	105	22.6
121	1.1484375	330	34.8	171	1.5390625	137	29.4
122	1.15625	402	42.2	172	1.546875	174	37.4
123	1.1640625	487	51.1	173	1.5546875	220	47
124	1.171875	576	60.4	174	1.5625	270	57.6
125	1.1796875	698	73.2	175	1.5703125	330	71.5
126	1.1875	1.5	0.187	176	1.578125	1.5	0.383
127	1.1953125	15	1.87	177	1.5859375	15	3.83
128	1.203125	32.4	4.02	178	1.59375	32.4	8.45
129	1.2109375	53.6	6.65	179	1.6015625	53.6	14
130	1.21875	76.8	9.53	180	1.609375	76.8	20
131	1.2265625	105	13	181	1.6171875	105	27.4
132	1.234375	137	16.9	182	1.625	137	35.7
133	1.2421875	174	21.5	183	1.6328125	174	45.3
134	1.25	220	27.4	184	1.640625	220	57.6
135	1.2578125	270	34	185	1.6484375	270	69.8
136	1.265625	330	41.2	186	1.65625	1.5	0.475
137	1.2734375	402	49.9	187	1.6640625	15	4.75
138	1.28125	487	60.4	188	1.671875	32.4	10.2
139	1.2890625	576	71.5	189	1.6796875	53.6	16.9
140	1.296875	1.5	0.221	190	1.6875	76.8	24.3
141	1.3046875	15	2.21	191	1.6953125	105	33.2
142	1.3125	32.4	4.87	192	1.703125	137	43.2
143	1.3203125	53.6	8.06	193	1.7109375	174	54.9
144	1.328125	76.8	11.5	194	1.71875	220	69.8
145	1.3359375	105	15.8	195	1.7265625	1.5	0.59
146	1.34375	137	20.5	196	1.734375	15	5.9
147	1.3515625	174	26.1	197	1.7421875	32.4	12.7
148	1.359375	220	32.4	198	1.75	53.6	21
149	1.3671875	270	40.2	199	1.7578125	76.8	30
150	1.375	330	48.7	200	1.765625	105	41.2

Set Point	V_{BOOT} (V)	R_{TOP} 1% (kΩ)	R_{BOTTOM} 1% (kΩ)
201	1.7734375	137	53.6
202	1.78125	174	68
203	1.7890625	1.5	0.732
204	1.796875	15	7.32
205	1.8046875	32.4	15.8
206	1.8125	53.6	26.1
207	1.8203125	76.8	37.4
208	1.828125	105	51
209	1.8359375	137	66.5
210	1.84375	1.5	0.931
211	1.8515625	15	9.31
212	1.859375	32.4	20
213	1.8671875	53.6	33
214	1.875	76.8	47.5
215	1.8828125	105	64.9
216	1.890625	1.5	1.2
217	1.8984375	15	12
218	1.90625	32.4	26.1
219	1.9140625	53.6	43
220	1.921875	76.8	61.9
221	1.9296875	1.5	1.62
222	1.9375	15	16.2
223	1.9453125	32.4	34.8
224	1.953125	53.6	57.6
225	1.9609375	1.5	2.32
226	1.96875	15	23.2
227	1.9765625	32.4	49.9
228	1.984375	1.5	3.6
229	1.9921875	15	36
230	2	1.5	7.15

Input Voltage Sense

The input power supply voltage is sampled at VINSEN and used for V_{OUT} regulation for feed-forward control, V_{IN} UVLO, V_{IN} OVP fault protection, and V_{IN} monitoring via the PMBus.

A resistor divider network outside the chip is connected to VINSEN (see Figure 11). It is recommended to place a minimum 10nF filtering capacitor at VINSEN.

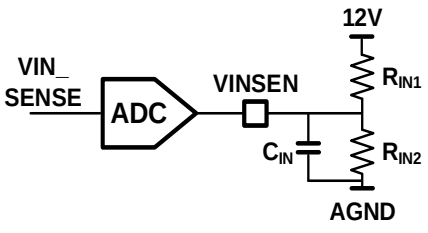


Figure 11: VIN Sense Network

VIN_OV_FAULT_LIMIT (55h on Page 0), bits[15:8] sets the divider ratio of the input voltage divider network. This can be used to calculate V_{IN} for monitoring and protection.

Inductor Current Sense

The MP2882 works with MPS's Intelli-Phase™ to sense the phase inductor current and the total current. The cycle-by-cycle current information is used for phase-current balancing, thermal balancing, over-current protection (OCP), and adaptive voltage positioning (output voltage droop).

To enable current sensing, connect the MP2882's CSx pin directly to the Intelli-Phase™ CS pin. The MP2882's CSx pin can take either current or voltage information from the Intelli-Phase™ CS, which indicates the phase inductor current. VCS_REF (typically 1.24V) can be connected to the Intelli-Phase™ to act as a CS reference voltage if required.

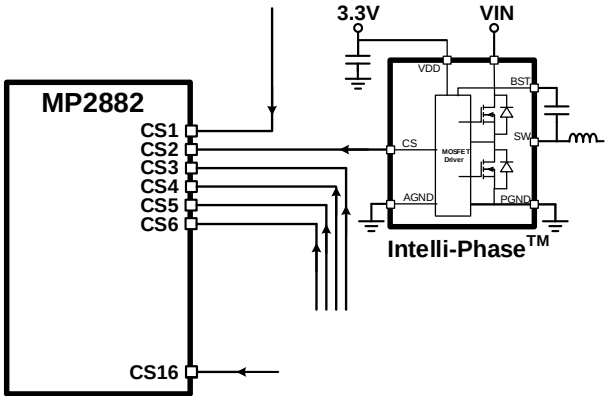


Figure 12: Phase Current Sense

Total Current Sense

The total current is summed from each CS pin and converted into an IMON voltage via the internal resistors.

The IMON resistors of both rails are internal. The resistance and IMON current mirror gain are configurable (see Figure 13 on page 27). These combinations cover the I_{BASE} range, which is between 56A and 1792A (assuming the current-sense gain = 5μA/A).

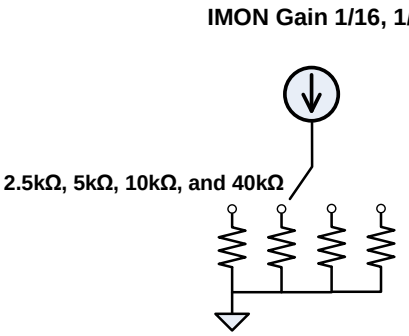


Figure 13: IMON Setting

All sensed currents from the CS pins are summed to generate a configurable, proportional current. This current can be applied to an internal, configurable resistor to obtain the IMON voltage (V_{IMON}). Configure the current gain and resistor value using register ABh on Page 0 and Page 1.

V_{IMON} is sampled, calculated, and stored in the I_{OUT} reporting register. The value in the I_{OUT} register is reported to the processor to avoid exceeding the thermal design point and maximum current capability of the system.

If automatic phase-shedding (APS) is enabled, the I_{OUT} report determines the real-time phase count to flatten the overall efficiency across the whole operating current range.

The MP2882 provides a user-configurable scaling factor and a user-configurable current offset. The configurable parameters allow users to match the IMON scaling to the design's voltage regulator tolerance band (VRTOB) calculation. This provides the most accurate current reporting across the entire load range, and maximizes the processor's turbo performance.

Figure 14 shows the MP2882 IMON sense and report block diagram.

GAIN_PMBUS, GAIN_SEL and OFFSET_PMBUS convert the ADC-sensed V_{IMON} value to direct format with 1A/LSB. This value is then reported via PMBus command READ_IOUT (8Ch). See the ABh registers on page 68 and page 122, and the and ACh registers on page 69 and page 123 for more details.

GAIN_AVS and OFFSET_AVS convert the IMON-sensed value to the AVSBus current reported format.

The AVSBus current report share the same gain and offset registers. See the ADh registers on page 69 and page 123 for more details.

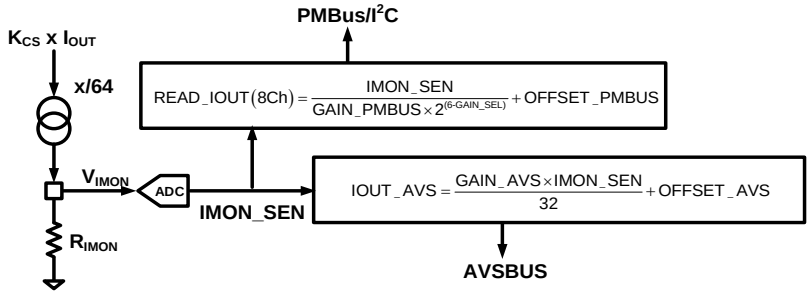


Figure 14: Total Current Sense and Report

Intelli-Phase™ Temperature Sense

The MP2882 measures the temperature of the power stage by connecting all Intelli-Phase™ VTEMP pins to the TSENS1 or TSENS2 pins (see Figure 15). The voltage on the MP2882's TSENS1 or TSENS2 pins indicate the highest junction temperature of all Intelli-Phase™ devices in the VR power system. The sensed temperature is used for over-temperature protection (OTP), OT warning, and power stage temperature monitoring.

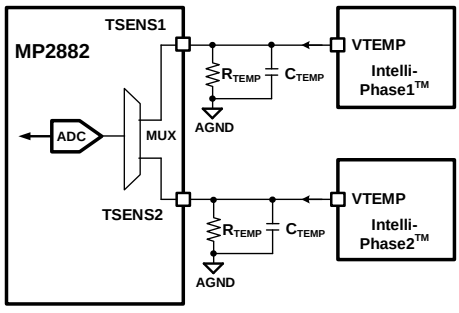


Figure 15: External Temperature Sense

C_{TEMP} is filtering capacitor on the VTEMP pin. It is recommended to use a ceramic 10nF to 47nF capacitor for C_{TEMP}. R_{TEMP} is a discharging resistor that ranges between 10kΩ and 49.9kΩ.

The Intelli-Phases's™ V_{TEMP} is a voltage output proportional to the junction temperature.

The MP2882 has an internal 1/2 divider on the TSENS1 and TSENS2 pins. The junction temperature can be calculated with Equation (6):

$$T_{JUNCTION}(℃) = 2 \times a \times V_{TEMP} + b \quad (6)$$

Where *a* is the temperature gain (in °C/V), and *b* is the temperature offset (in °C).

For example, if *a* = 125°C/V, *b* = -75°C, and V_{TEMP} = 0.62V, the junction temperature of the Intelli-Phase™ is 80°C. Refer to the Intelli-Phase™ datasheet for details on the *a* and *b* values.

Die Temperature Sense

The MP2882 senses the die temperature. A thermal sensor converts the die temperature into a voltage (see Figure 16). This voltage is saved to DIE_TEMP_SENSE (D8h on Page 1). This register value can be read via the PMBus.

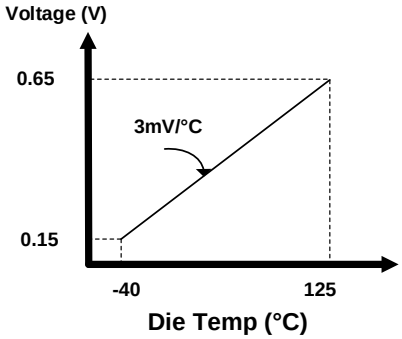


Figure 16: Die Temperature Sense

Dynamic Voltage Identification (DVID)

The MP2882 supports dynamic V_{OUT} transitions by changing the VID code via the PMBus interface and AVSBus interface.

In PMBus override control mode, the DVID slew rate is set by VOUT_TRANSITION_RATE (27h) with 1mV/μs/LSB or 0.01mV/μs/LSB, which is determined by MFR_VR_CONFIG2 (A1h), bit[0]. The maximum slew rate is 50mV/μs.

The MP2882 applies an advanced digital control method to improve V_{OUT} performance while VID ramps up and down.

Ramping Upward

When V_{OUT} is ramping upward, the inductor current (I_L) rises to charge the output capacitors. This current introduces a large, positive droop voltage, and lowers V_{OUT}.

When V_{REF} stops ramping, V_{OUT} may be below the minimum regulation tolerance budget (TOB). The MP2882 can automatically ramp up more VID steps than the target VID, then fall back to allow V_{OUT} to rise to the regulation TOB.

Ramping Downward

When V_{OUT} ramps downward, I_L decreases to discharge the output capacitors. The output capacitors continue to discharge when ramping ends, which may lead to output voltage undershoot.

The MP2882 applies a low-pass filter for VID DAC to smooth out V_{REF} when V_{OUT} is ramping downward. Figure 17 shows V_{OUT} when VID ramps upward after the previous VID finishes ramping downward.

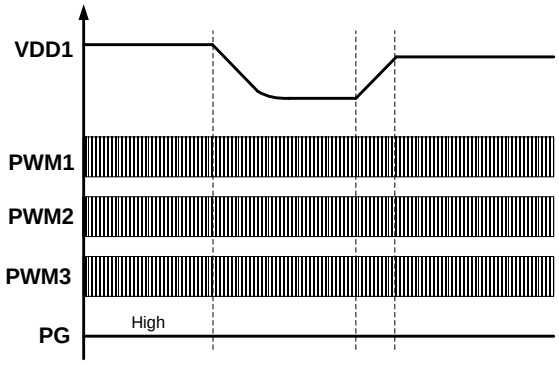


Figure 17: VID Ramping Downward to VID Ramping Upward

Automatic Phase-Shedding (APS)

To improve efficiency across the entire load range, the MP2882 supports automatic phase-shedding (APS) according to the load current report. In APS mode, the VR can be optimized to automatically adjust the phase count to balance the performance between transient and power consumption.

Figure 18 on page 29 shows how the VR works in 7-phase CCM under heavy loads and 1-phase CCM under light loads. This optimizes the efficiency, and the device enters 1-phase DCM under extremely light loads to reduce switching loss.

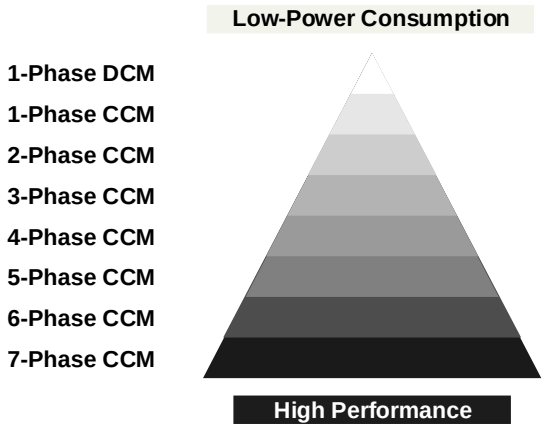


Figure 18: APS Function Diagram during 7-Phase CCM

APS is implemented by comparing the sensed load current with each power state's current threshold. The MP2882 provides two types of registers to configure APS functionality. MFR_APS_ITH_SET (AEh on Page 0 and Page 1), bits[9:0] sets the phase-shedding level. Bits[15:10] of the same command configure the hysteresis value to prevent the converter from changing power states under a steady load current.

Figure 19 shows the APS current thresholds from 2-phase CCM to 1-phase CCM. See the MFR_APS_CTRL_SET (AFh) registers on page 70 and page 124 and the MFR_APS_CTRL23_SET (B0h) section on page 71 and page 125 more information.

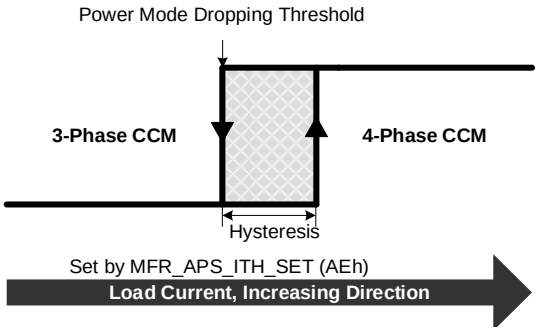


Figure 19: APS Threshold Setting

In addition to sensed I_{OUT} comparison, the MP2882 provides three conditions that force the device to exit APS immediately and run with full-phase CCM, which accelerates the load transient response and reduces output voltage undershoot:

1. The DVID process makes the controller runs with full-phase CCM. After V_{OUT} settles to the target value, the new power state is determined by the load current.
2. Load step-up causes VFB- window tripping, which triggers full-phase CCM to reduce output voltage undershoot.
3. Once the phase current exceeds the per-phase over-current limit, the MP2882 runs with the full phase number.

Current Balancing/Thermal Balancing

The MP2882 provides a current balance loop to achieve fair current sharing in multi-phase mode while different circuit impedances lead to phase current differences.

The phase current is sensed and calculated with the current reference in the current loop. Each zone's PWM on time is adjusted individually to balance the currents.

The MP2882 applies sigma-delta (Σ-Δ) modulation and delay line-loop (DLL) technology in the current balance modulation to increase the resolution of the current balance modulation and greatly reduce PWM jittering. The time resolution of the digital system is 5ns. By applying Σ-Δ modulation and DLL technology, the digital PWM resolution can be increased to 0.08ns.

The MP2882 assigns the 16 phases to 8 zones. Each zone has a configurable phase current offset to achieve thermal balance between the phases. MFR_CS_OS_ZONE (B8h on Page 0) configures the phase number assigned to each zone. The bandwidth of the current loop is relatively low compared to the output voltage regulation loop, so it does not impact V_{OUT}.

VFB Window

The VFB window (V_{REF} - 25mV to V_{REF} + 25mV) provides advanced, nonlinear loop control to fasten the transient performance.

When the feedback voltage (V_{FB}) exceeds V_{REF} + 25mV (VFB+ window), all PWMs pull low and blank the PWM set signal until V_{FB} falls below the VFB+ window. The VFB+ window reduces the overshoot when loads are released, especially during multi-phase operation.

When V_{FB} is below V_{REF} - 25mV (VFB- window), the VR exits automatic power state mode immediately, then runs at full phase to improve transient response.

Digital Load Line

The droop current mirror has two gains for two rails. The first current mirror ratio (GAIN1) can be set to 1/16, 1/8, 1/4, and 1/2. The DC/AC droop's second current mirror ratio (GAIN2) can be set to eight levels: 0, 3/4, 4/4, 5/4, 6/4, 7/4, 8/4, and 9/4.

GAIN1 and GAIN2 are both effective in PMBus mode and SVI2 mode. In PMBus mode, MFR_AVS_SET (C8h on Page 1), bit[15] and bit[14] are set to 1, and the gains always follow their set values. In the SVI2 mode, MFR_AVS_SET (C8h on Page 1), bit[15] and bit[14] are set to 0, and the default set of GAIN2 should be 5/4 (100%). A set of percentage current mirror gains (60%, 80%, 100%, 120%, 140%, 160%, and 180%) is required for SVI2 mode.

The load-line slope with the GAIN1 and GAIN2 current-sense gain can be calculated with Equation (7):

$$R_{LL} = R_{DROOP} \times K_{CS} \times GAIN1 \times GAIN2 \quad (7)$$

Where R_{LL} is the initial load-line slope (in Ω), K_{CS} is the current-sense gain of the Intelli-Phase™ (in A/A), and R_{DROOP} is the internal droop resistor (in Ω).

There are 64 internal droop resistors in series on rail 1 and rail 2, and each is set to 20Ω. They can be configured from 20Ω to 1.28kΩ (see Figure 20).

PWM Assign

The MP2882 supports configurable PWM signals. They can be configured in the following registers:

- MFR_PWM_MUX1 (B7h on Page 1)
- MFR_PWM_MUX2 (B8h on Page 1)
- MFR_PWM_MUX3 (B9h on Page 1)
- MFR_PWM_MUX4 (BAh on Page 1)
- MFR_PWM_1MSB (BBh on Page 1)

The rail 1 PWM signal can be set from PWM_0 through PWM_15, while the rail 2 PWM signal can be set from PWM_19 (PWM1_L2) through PWM_12 (PWM8_L2).

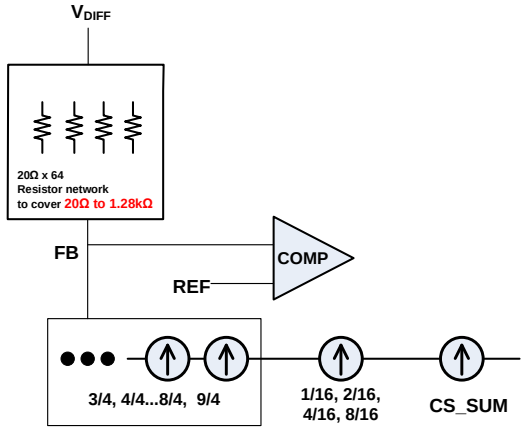


Figure 20: Digital Load Line for Rail One

Multi-Configuration

The MP2882 supports multi-configuration. Use the PROG pin to select 16 different configurations. Table 5 shows the corresponding resistor divider settings.

Table 5: Pin Configuration for PROG

Multi-Configure	Setting Point (V)	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%
0	0	-	0
1	0.137	3.32	0.274
2	0.186	3.32	0.383
3	0.235	3.32	0.499
4	0.285	3.32	0.619
5	0.345	3.32	0.787
6	0.409	3.32	0.976
7	0.481	3.32	1.21
8	0.56	3.32	1.5
9	0.657	3.32	1.91
10	0.782	3.32	2.55
11	0.9	3.32	3.32
12	1.039	3.32	4.53
13	1.191	3.32	6.49
14	1.343	3.32	9.76
15	1.512	3.32	17.4

Fault Monitoring and Protections

The MP2882 supports various fault monitoring and protections, described below.

V_{IN} Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)

The VR shuts off immediately by forcing the PWM signals to tri-state if the sensed V_{IN} drops below the VIN_OFF threshold. It restarts again when the sensed V_{IN} exceeds the VIN_ON threshold. The V_{IN} under-voltage lockout (UVLO) threshold can be configured via register MFR_VIN_UVLO (55h on Page 1), with 62.5mV/LSB.

The VR shuts off if V_{IN} exceeds the V_{IN} over-voltage protection (OVP) threshold that is set via register VIN_OV_FAULT_LIMIT (55h on Page 0). V_{IN} OVP can be selected to either latch-off or auto-retry mode.

Over-Current Protection (OCP)

The over-current protection (OCP) function applies to two OCP mechanisms, with two types of thresholds.

The first type is a time-based and current-based threshold (OCP_TDC). OCP_TDC limit is programmable via PMBus command IOUT_OC_FAULT_LIMIT (46h). OCP_TDC is triggered if the sensed average I_{OUT} exceeds the OCP_TDC threshold for preset time (OCP_TDC blanking time).

The second type is a current-only based threshold (OCP_SPIKE). The OCP_SPIKE threshold can be configured via the PMBus command IOUT_OC_FAULT_LIMIT (46h). OCP_SPIKE is triggered if the cycle-by-cycle total sensed average I_{OUT} exceeds the OCP_SPIKE threshold. This is an optional protection.

If either mechanism is triggered on either rail, the MP2882 asserts OCP_L and delays any further action. This delay is called an action delay. If the current has not dropped below the threshold after the action delay has expired, the MP2882 shuts down the VR to protect the power MOSFETs.

OCP_TDC and OCP_SPIKE can be configured to no action, hiccup, retry 6 times, or latch-off mode via the PMBus.

The controller takes no action in no action mode, and continues switching until other protections are tripped. The fault indication bits in registers STATUS_IOUT (7Bh) and STATUS_WORD (79h) are not set if no action mode is selected.

In hiccup mode, the controller forces the PWM signals to tri-state to disable the output, and attempts to restart after a 12.5ms protection delay time. This time can be configured via MFR_PRT_CONFIG (A9h on Page 1), bits[2:1].

In retry 6 times mode, the VR restarts six times at most. If the fault is removed within these six restarts, the VR resumes normal operation. If the fault remains, the VR shuts down until a PMBus OPERATION on command is received, the power is cycled on VDD33, or EN is toggled.

In latch-off mode, the VR shuts down until PMBus OPERATION off, then on commands are received, the power is cycled on VDD33, or EN is toggled.

The above four protection modes are available for OCP_TDC, OCP_SPIKE and V_{OUT} under-voltage protection (UVP).

In addition to the dual OCP mechanism described above, the MP2882 utilizes an extra current-based limitation protection called OCP_PHASE. The MP2882 monitors the phase current cycle by cycle. If the phase current exceeds the OCP_PHASE threshold during the PWM off time, the PWM remains low to discharge the inductor current below the set threshold.

If the present phase PWM on signal is blocked for more than 80ns, the PWM on signal is skipped for this cycle, then the next phase turns on directly to regulate V_{OUT}. Per-phase OCP typically works with UVP to protect the regulator system. The OCP_PHASE threshold is PMBus-configurable via the MFR_FAST_OCP_SET (A7h) register.

Under-Voltage Protection (UVP)

The MP2882 provides under-voltage (UV) and over-voltage protection (OVP) by monitoring the V_{DIFF}.

If V_{DIFF} drops below the UVP threshold for a set time (known as the UVP blanking time), the

controller forces the PWMs to tri-state to disable the output power.

The VOUT_OV_UV_FAULT_RESPONSE (A6h) register determines the UVP mode. Similar to the OCP_TDC protection scheme, the UVP scheme also provides also provides no action, hiccup, retry 6 times, and latch-off options.

The UVP threshold can be configured with PMBus command MFR_OV_UV_LIMIT (A5h) (see page 65 and page 118 for more details).

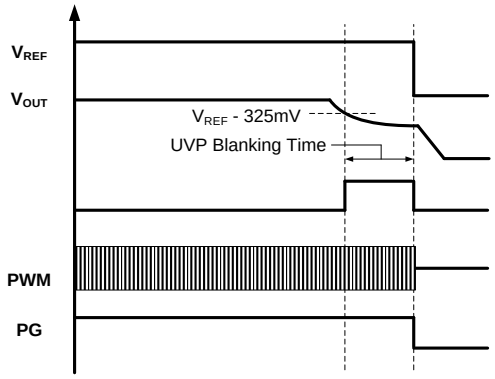


Figure 21: Under-Voltage Protection (UVP)

Generally, UVP can be triggered when the per-phase OCP current limit is reached, and the PWM signals are blocked by the per-phase OC signals (see Figure 22).

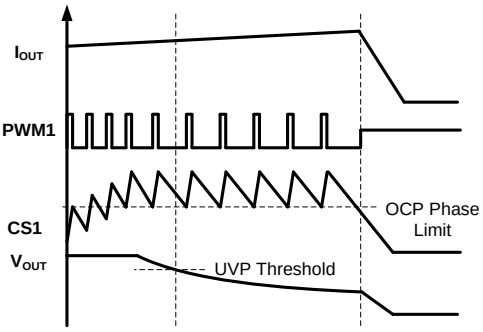


Figure 22: UVP Triggered when the Per-Phase Current is Limited by OCP_PHASE

Over-Voltage Protection (OVP)

The MP2882 provides two types of over-voltage protection (OVP): ABS_OVP (OVP1) and VID_OVP (OVP2). When any OVP is triggered, the MP2882 turns on all LS-FETs to discharge C_{OUT} until V_{OUT} falls below 160mV. Then the devices initiates Hi-Z off.

VID_OVP is the OVP type that refers to V_{REF}. It is tripped if V_{DIFF} exceeds the VID_OVP threshold for a set blanking time. The VID_OVP threshold can be configured via PMBus command MFR_OV_FAULT_LIMIT (44h), bits[10:8].

Figure 23 shows the OVP waveform.

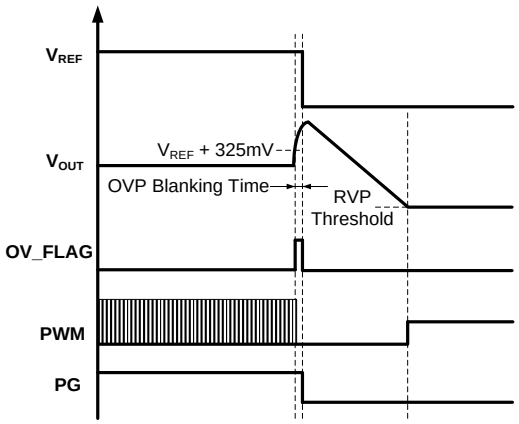


Figure 23: OVP Waveform

The MP2882 provides no action, retry 3 times, and latch-off mode for VID_OVP.

The second type is called ABS_OVP. ABS_OVP is triggered if V_{DIFF} exceeds the ABS_OVP threshold without a trigger delay time. The ABS_OVP threshold is determined by VOUT_MAX (24h) and MFR_OV_UV_LIMIT (A5h), bits[7:0]. The ABS_OVP fault always initiates latch-off mode.

Reverse-Voltage Protection (RVP)

A large reverse inductor current may cause negative output voltages that can harm the processor and other output components. The MP2882 provides reverse-voltage protection (RVP) with no additional system cost.

If OVP occurs, all LS-FETs are forced on to quickly discharge the voltage of the output capacitors. The inductor current becomes very negative, which can discharge the voltage of the output capacitors until they are negative enough to destroy the load without RVP.

If the VOSEN voltage falls below 160mV after OVP and RVP is enabled, the MP2882 triggers RVP by latching all PWM outputs to tri-state. The reverse inductor current can quickly be reset to 0A by dissipating the energy in the inductor to the input DC voltage source through the forward-biased body diode of the HS-FETs. Figure 23 on page 32 shows the RVP function after OVP.

Over-Temperature Protection (OTP)

Over-temperature protection (OTP) is triggered if the sensed power stage temperature exceeds the maximum temperature threshold. The MP2882 can be configured to latch-off mode or hiccup mode when OTP is triggered.

The MP2882 monitors the junction temperature of the Intelli-Phase™ by connecting power stage's VTEMP (T_{OUT}) to the controller's TSENS1 and TSENS2 pins.

TSENS2 Digital Fault

The MP2882 senses the voltage on the TSENS2 pin with the internal ADC. If the TSENS2 voltage exceeds or falls below a configurable level set by MFR_TSENS2_SET (A8h on Page1), bits[13:8], a TSENS2 digital fault occurs. The MP2882 shuts down all rails immediately. The TSENS2 digital fault direction is determined by MFR_TSENS2_SET (A8h on Page 1), bit[1].

The TSENS2 digital fault action modes include latch-off mode and hiccup mode, determined by MFR_TSENS2_SET (A8h on Page1), bit[0]. In latch-off mode, V_{OUT} is shut down. Latch-off mode remains regardless of the state of the TSENS2 pin. In hiccup mode, the system attempts to restart after a configurable protection delay time.

Line-Float Detection

The MP2882 supports remote sensing line (VOSEN, VORTN) float detection during system initialization, after VDD33 powers on, or after EN powers on from low-power mode. The MP2882 latches off if a line float is detected, and reports the fault via PMBus command STATUS_VOUT (7Ah), bit[1]. Line-float detection can be enabled via MFR_VR_CONFIG1 (B7h on Page 0).

Phase Redundancy

The MP2882 can detect the abnormal DrMOS and remove in. Meanwhile, the remaining phases interleave automatically. The maximum number of faulty phases is two. If there are more than two faulty phases, the MP2882 shuts down the associated rail. During this time, FAULT_REPORT1 (Dah on Page 1), bit[14] (for rail 2) and bit[6] (for rail 1) is asserted.

There are two detection modes; each is described below.

The first detection mode detects the value of the CS voltage (V_{CS}) ripple (see Figure 24).

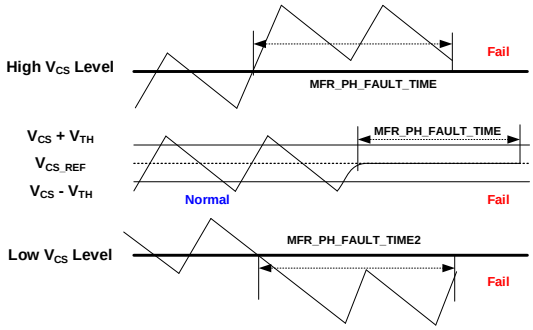


Figure 24: CS Voltage Detection

There are three ways to judge the fault phase.

1. If V_{CS} is below the CS ripple's high threshold (V_{CS_REF} + V_{TH}), which is set by MFR_PH_FAULT_H_SET (4Ah on Page 0), bits[13:11], and exceeds the CS ripple's low threshold (V_{CS_REF} - V_{TH}), which is set by MFR_PH_FAULT_L_SET (4Ah on Page 1), bits[13:11], this phase's V_{CS} value is considered to be V_{CS_REF}. If the MP2882 detects that V_{CS} remains at V_{CS_REF} for the time set by MFR_PH_FAULT_TIME (4Ah), bits[15:14], this is considered an abnormal phase.
2. If V_{CS} exceeds the high V_{CS} level for the time set by MFR_PH_FAULT_TIME (4Ah on Page 0 and Page 1), bits[15:14], this is considered an abnormal phase.
3. If V_{CS} drops below the low V_{CS} level for the time set by MFR_PH_FAULT_TIME2 (C4h on Page 1), bits[15:14], this is considered an abnormal phase.

The high V_{CS} level is same as the threshold for OCP_PHASE, which is set by MFR_FAST_OCP_SET (A7h), bits [15:8]. The low V_{CS} level threshold is fixed internally. For a 5μA/A DrMOS gain and a 2kΩ R_{CS}, the low threshold is -45A.

CS ripple detection is enabled by MFR_PRT_CONFIG (A9h on Page 1), bit[13] for rail 2, and bit[12] for rail 1.

After enabling CS ripple detection, once the fault occurs, STATUS_WORD (79h on Page 0 and Page 1), bit[8] is asserted. If the action EN function is enabled via OT_WARN_LIMIT_R1 (51h on Page 0), bit[15], the MP2882 removes the fault phase.

The second mode detects t_{ON} variation. If the deviation between the current t_{ON} and the average t_{ON} exceeds the set threshold, this phase is considered abnormal. The threshold is set by a 10-bit value, where the 7LSB is set by FREQUENCY_SWITCH (33h), bits[15:9], and the 3MSB is set by bits[15:13] of IOUT_CAL_OFFSET_PMBUS (ACh).

TEMP Fault

The MP2882 supports a TEMP fault for a fast protection if any phase's DrMOS experiences a fault. If the voltage on the TSENS1 pin exceeds 2.2V, the output is disabled and a TEMP fault is triggered.

Figure 25 shows a TEMP fault application example when the MP2882 works with the MP86956 Intelli-Phase™. If a fault occurs on any MP86956, its TOUT/FLT signal is asserted, and TSENS1 pulls high to 3.3V.

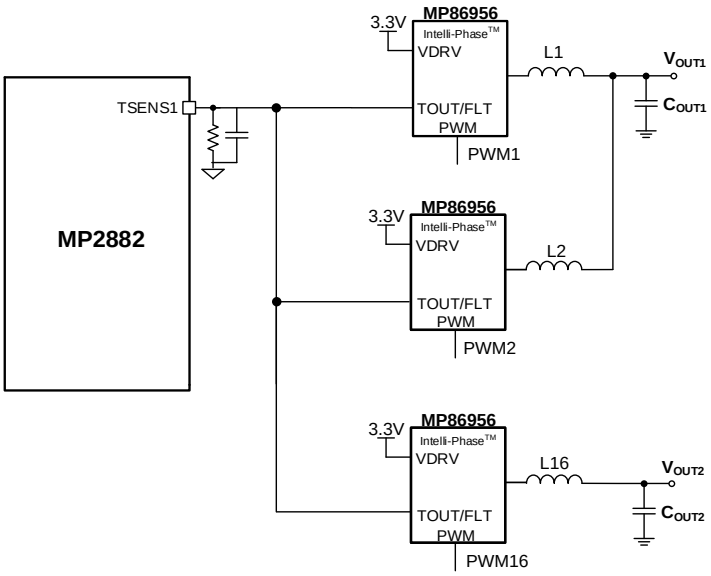


Figure 25: TEMP Fault Application for the MP2882 and MP86956

NVM Fault

If the data in the non-volatile memory (NVM) is invalid after the CRC check during the start-up NVM process, the VR does not start until the fault is cleared.

Communication Failure

A data transmission fault occurs when information is not properly transferred between the devices. Several data transmission faults can occur:

- Sending too little data
- Reading too little data
- Host sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The data transmission faults assert ALT_P#. The CLEAR_FAULTS command de-asserts ALT_P#.

If the faults still remains after this process, ALT_P# asserts again.

Intelli-Phase™ Fault Detection

The MP2882 supports Intelli-Phase™ fault type detection. Several types of Intelli-Phase faults can occur:

- Current-limit fault
- Over-temperature fault
- LS-FET shorted fault
- High-side MOSFET (HS-FET) shorted fault

This fault detection function only works when the Intelli-Phase™ supports fault type indication. Refer to the Intelli-Phase™ datasheet for more details.

The MP2882 scans the PWM fault if any of the following faults occur: V_{IN} UVLO, V_{IN} OVP, OTP, V_{OUT} UVP, V_{OUT} OVP, OCP, or a VTEMP fault.

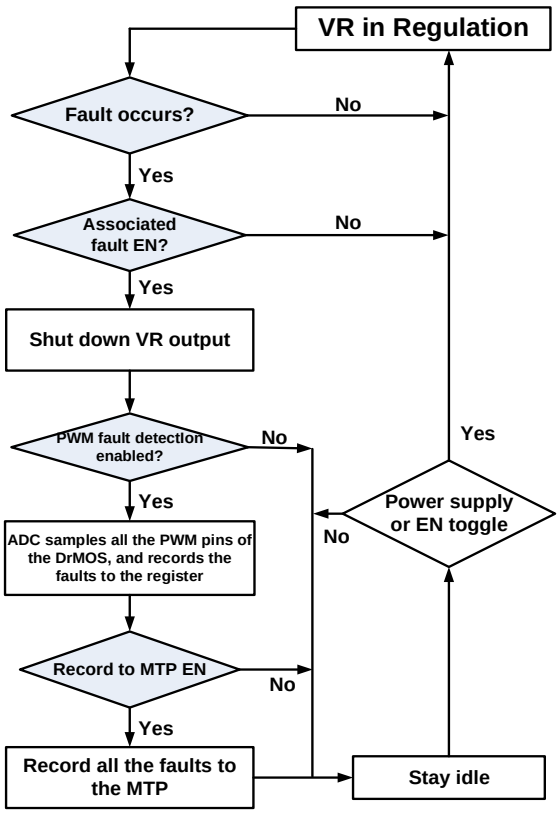


Figure 26: Intelli-Phase™ Fault Detection Flowchart

Figure 26 shows that when any of the above faults are triggered, the MP2882 executes the following steps:

1. Shuts off the associated rail(s).
2. Starts the Intelli-Phase™ fault type scan for related rail(s) by sensing the impedance on the PWM pins if this function is enabled via MFR_PRT_CONFIG (A9h on Page1), bits[5:4].
3. Faults are reported to the Page 1 FAULTS_REPORT (D9~DFh) registers.
4. Faults are recorded to the NVM (registers E9h~EFh) when fault recording to the NVM is enabled via MFR_NVM_CTRL (4Eh on Page 1), bit[1]. The last fault event is stored. To store faults to the NVM, the EN signal should be kept high for at least 20ms after a fault occurs.

To clear the recorded fault in the NVM registers, send a FEh command.

PMBUS/I²C COMMUNICATION

General Description

The Power Management Bus (PMBus) is an open standard power-management protocol that defines a means of communicating with power conversion and other devices. The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle.

Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. It is based on the principles of operation of I²C.

The MP2882 supports 100kHz, 400kHz and 1MHz bus timing requirements. The timing and electrical characteristics of the PMBus can be found in the Electrical Characteristics section on page 8, or in the PMBus Power Management Protocol Specification, part 1, revision 1.3, available at http://PMBus.org.

PMBus Communication

The MP2882 supports real-time monitoring for the VR operation parameters and statuses with the PMBus interface. Table 6 lists the monitored parameters.

Table 6: PMBus-Monitored Parameters

Parameter	PMBus
Output voltage	VID_STEP/LSB
Output current	0.25A/LSB or 0.5A/LSB
Temperature	1°C
Input voltage	31.25mV/LSB
OVP	✓
UVP	✓
OCP	✓
OTP	✓
VIN_UVLO	✓
VIN_OV	✓
Line Float	✓
CML	✓

PMBus/I²C Address

To support multiple VR devices using the same PMBus/I²C interface, the MFR_ADDR_PMBUS

register or the ADDR pin can be used to configure the PMBus address.

The address is a 7-bit code. The 3MSB bit are set by the register. The 4LSB bit address can either be set by the register or by the voltage on the ADDR pin. 00h is reserved as an all-call address, which can be set for single-chip operation.

The ADDR voltage is set by the voltage divider connected from ADDR to VDD18. Table 7 shows the resistor values for different PMBus addresses when the 3MSB are set to 3'b010.

Table 7: Pin Configuration for PMBus Address

PMBus Address	Setting Point (V)	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%
20h	0	-	0
21h	0.137	3.32	0.274
22h	0.186	3.32	0.383
23h	0.235	3.32	0.499
24h	0.285	3.32	0.619
25h	0.345	3.32	0.787
26h	0.409	3.32	0.976
27h	0.481	3.32	1.21
28h	0.56	3.32	1.5
29h	0.657	3.32	1.91
2Ah	0.782	3.32	2.55
2Bh	0.9	3.32	3.32
2Ch	1.039	3.32	4.53
2Dh	1.191	3.32	6.49
2Eh	1.343	3.32	9.76
2Fh	1.512	3.32	17.4

Figure 27 shows the supported PMBus/I²C transmission structure without packet error checking (PEC).

Figure 28 on page 37 shows the supported PMBus/I²C transmission structure with PEC.

There are six kinds of transmission structures:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word
6. Block read

To read or write the registers of the MP2882, the PMBus or I²C command must be compliant with the byte number of the register in the PMBus command table for rail 1 and rail 2.

AVSBus Mode

The MP2882 supports the following AVSBus protocol specified commands:

- Voltage read/write
- V_{OUT} transition rate read/write
- Current read
- Temperature read
- Voltage reset
- Power mode read/write
- AVSBus status read/write
- AVSBus version read

The MP2882 also supports slave interrupt functionality.

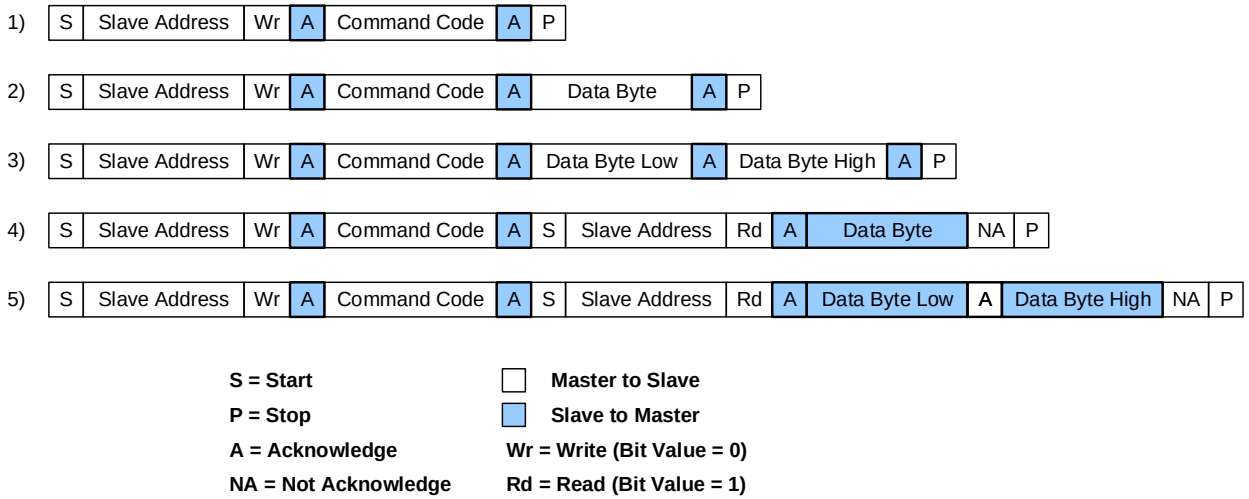


Figure 27: Supported PMBus/I²C Transmission Structure without PEC

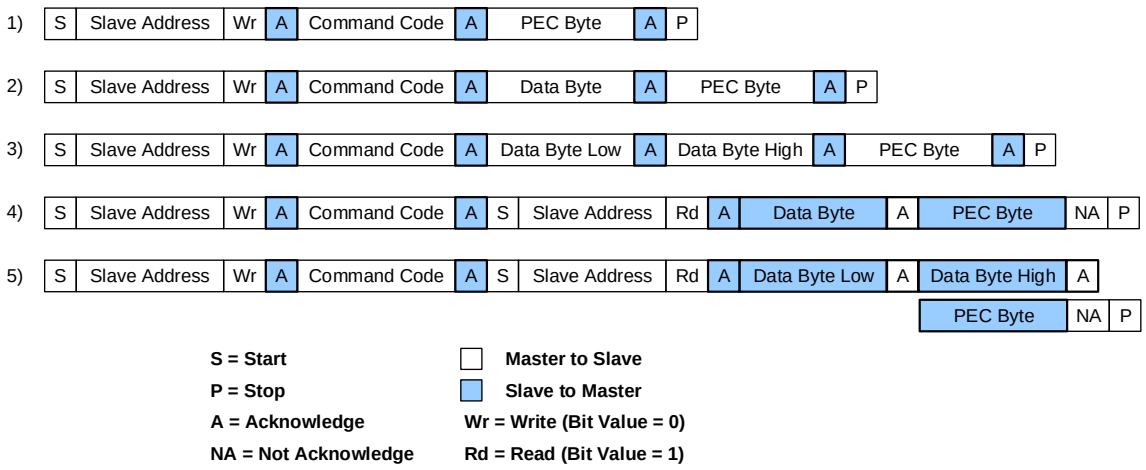


Figure 28: Supported PMBus/I²C Transmission Structure with PEC

SVI2 2.0 Interface

The MP2882 supports all SVI2 2.0 commands. Figure 29 shows the AMD SVD packet structure.

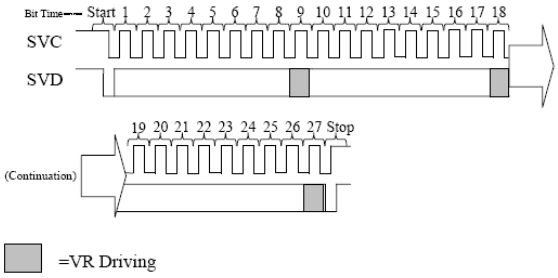


Figure 29: SVD Packet Structure

Table 8 shows the SVI2 2.0 commands.

Table 8: SVD Packet from the CPU to the VR

Bits	Description
1:5	Always 11000b
6	VDD domain selector bit
7	VDDNB domain selector bit
8	Always 0b
9	Acknowledge bit
10	PSI0_L
11:17	VID code, bits[7:1]
18	Acknowledge bit
19	VID code, bit[0]
20	PSI1_L
21	TFN
22:24	Load line slope trim, bits[2:0]
25:26	Offset trim, bits[1:0]
27	Acknowledge bit

Table 9 shows the definition of the PSI0_L and PSI1_L bits.

Table 9: PSI0_L and PSI1_L Definition

Function	Description
PSI0_L	Power state indicates level 0. When this signal is asserted (active low), the processor is in a low enough power state for the MP2882 to boost efficiency by dropping the phases to 1-phase CCM.
PSI1_L	Power state indicates level 1. When this signal is asserted (active low) and PSI0_L is asserted, the processor is in a low enough power state for the MP2882 to boost efficiency by forcing the only working phase into diode emulation mode.

The TFN bit and the core and Northbridge domain selector bits are used by the processor to change the telemetry functionality (see Table 10).

Table 10: TFN = 1 Truth Table

VDD1	VDD2	Description
0	1	Telemetry is in voltage and current mode. Therefore, the voltage and current for the VDD1 and VDD2 domains are sent by the controller.
0	0	Telemetry is in voltage mode only. Only the voltage for the VDD1 and VDD2 domains are sent by the controller.
1	0	Telemetry is disabled.
1	1	Reserved.

PMBUS COMMANDS

Command Code	Command Name	Type	Bytes	Page 0	Page 1
00h	PAGE	R/W	1	✓	-
01h	OPERATION	R/W	2	✓	✓
03h	CLEAR_FAULTS	Send	0	✓	✓
10h	MFR_NVM_WP	R/W	2	✓	-
	MFR_VIN_UV_LIMIT	R/W	2	-	✓
13h	MFR_TEMP_CAL	R/W	2	-	✓
16h	RESTORE_ALL_CODE	Send	0	✓	✓
21h	VOUT_COMMAND	R/W	2	✓	✓
22h	MFR_VOUT_TRIM	R/W	2	✓	✓
24h	VOUT_MAX	R/W	2	✓	✓
25h	VOUT_MARGIN_HIGH	R/W	2	✓	✓
26h	VOUT_MARGIN_LOW	R/W	2	✓	✓
27h	VOUT_TRANSITION_RATE	R/W	2	✓	✓
28h	VOUT_DROOP	R/W	2	✓	✓
2Bh	VOUT_MIN	R/W	2	✓	✓
33h	MFR_FREQUENCY_SWITCH	R/W	2	✓	✓
46h	IOUT_OC_FAULT_LIMIT	R/W	2	✓	✓
47h	IOUT_OC_FAULT_RESPONSE	R/W	2	✓	✓
4Ah	MFR_PH_FAULT_SET	R/W	2	✓	✓
4Fh	OT_FAULT_LIMIT	R/W	2	✓	✓
51h	OT_WARN_LIMIT	R/W	2	✓	✓
55h	VIN_OV_FAULT_LIMIT	R/W	2	✓	-
	MFR_VIN_UVLO	R/W	2	-	✓
61h	TON_RISE	R/W	2	✓	✓
78h	STATUS_BYTE	R	1	✓	✓
79h	STATUS_WORD	R	2	✓	✓
7Ah	STATUS_VOUT	R	1	✓	✓
7Bh	STATUS_IOUT	R	1	✓	✓
7Ch	STATUS_INPUT	R	1	✓	✓
7Dh	STATUS_TEMPERATURE	R	1	✓	✓
7Eh	STATUS_CML	R	1	✓	✓
83h	READ_TSENS1_SENSE	R	2	✓	✓
84h	READ_IMON	R	2	✓	✓
85h	READ_VDIFF_SENSE	R	2	✓	✓
86h	READ_VFB_SENSE	R	2	✓	✓
88h	READ_VIN	R	2	✓	✓
8Bh	READ_VOUT	R	2	✓	✓
8Ch	READ_IOUT	R	2	✓	✓
8Dh	READ_TEMPERATURE	R	2	✓	✓
91h	READ_VBOOT	R	2	✓	✓
96h	READ_POUT	R	2	✓	✓
98h	PMBUS_REVISION	R	1	✓	-
99h	MFR_ID	R	BLOCK	✓	-
9Ah	MFR_MODEL	R	BLOCK	✓	-

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1
9Bh	MFR_REVISION	R	1	✓	-
9Dh	MFR_DATE	R	BLOCK	✓	-
9Fh	MFR_APS_OPTI	R/W	2	✓	✓
A0h	MFR_TIMEOUT	R/W	2	-	✓
A1h	MFR_VR_CONFIG2	R/W	2	✓	-
	MFR_VR_CONFIG4	R/W	2	-	✓
A2h	MFR_VR_CONFIG3	R/W	2	✓	-
	MFR_VR_CONFIG5	R/W	2	-	✓
A3h	MFR_PWM_LIMIT1	R/W	2	✓	✓
A4h	MFR_CORE_OTP_SET	R/W	2	✓	
	MFR_NVM_CTRL	R/W	2	✓	✓
A5h	MFR_OV_UV_LIMIT	R/W	2	✓	✓
A6h	MFR_OV_UV_RESPONSE	R/W	2	✓	✓
A7h	MFR_FAST_OCP_SET	R/W	2	✓	✓
A8h	MFR_SMBALERT_MASK	R/W	2	✓	-
	MFR_TSNS2_SET	R/W	2	-	✓
A9h	MFR_ADDR_PMBUS	R/W	2	✓	✓
	MFR_PRT_CONFIG	R/W	2	✓	✓
AAh	MFR_VOUT_CALC	R/W	2	✓	✓
ABh	MFR_IOUT_GAIN_PMBUS	R/W	2	✓	✓
ACh	MFR_IOUT_OS_PMBUS	R/W	2	✓	✓
ADh	MFR_IOUT_CAL_AVSBUS	R/W	2	✓	✓
AEh	MFR_APS_ITH_SET	R/W	2	✓	✓
AFh	MFR_APS_CTRL_SET	R/W	2	✓	✓
B0h	MFR_APS_CTRL23_SET	R/W	2	✓	✓
B1h	MFR_FSCB_LOOP_CTRL	R/W	2	✓	✓
B2h	MFR_VOUT_LOOP_CTRL	R/W	2	✓	✓
B3h	MFR_SETTLE_CTRL	R/W	2	✓	✓
B4h	MFR_PHASE_SET	R/W	2	✓	✓
B5h	MFR_GPIO_SEL	R/W	2	✓	-
	MFR_GPIO2_SEL	R/W	2	-	✓
B6h	MFR_PG_DELAY	R/W	2	✓	✓
B7h	MFR_VR_CONFIG1	R/W	2	✓	-
	MFR_PWM_MUX1	R/W	2	-	✓
B8h	MFR_CS_OS_ZONE	R/W	2	✓	-
	MFR_PWM_MUX2	R/W	2	-	✓
B9h	MFR_CS_OS_PART1	R/W	2	✓	-
	MFR_PWM_MUX3	R/W	2	-	✓
BAh	MFR_CS_OS_PART2	R/W	2	✓	✓
	MFR_PWM_MUX4	R/W	2	✓	✓
BBh	MFR_BLANK_TIME1	R/W	2	✓	✓
	MFR_PWM_MUX_1MSB	R/W	2	✓	✓
BCh	MFR_BLANK_TIME2	R/W	2	✓	✓
BDh	MFR_BLANK_TIME3	R/W	2	✓	✓

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1
BEh	MFR_SLOPE_CNT_SET	R/W	2	✓	✓
BFh	MFR_SLOPE_PEAK_SET	R/W	2	✓	✓
C0h	MFR_TRIM_14P	R/W	2	✓	-
C1h	MFR_SLOPE_DCM_SET	R/W	2	-	✓
C2h	MFR_PWM_MIN_TIME2	R/W	2	✓	-
	MFR_TRIM_SEL	R/W	2	-	✓
C3h	MFR_SLOPE_SR_2MSB_1	R/W	2	✓	-
	MFR_PWM_MUX5	R/W	2	-	✓
C4h	MFR_SLOPE_SR_2MSB_2	R/W	2	✓	-
	MFR_CP_SET	R/W	2	-	✓
C5h	MFR_SD_VID_SET	R/W	2	-	✓
C6h	MFR_SLOPE_SR_1P_2P_R1	R/W	2	✓	-
	MFR_SR_MAX	R/W	2	-	✓
C7h	MFR_SLOPE_SR_3P_4P_R1	R/W	2	✓	-
	MFR_AVS_SET2	R/W	2	-	✓
C8h	MFR_SLOPE_SR_5P_6P_R1	R/W	2	✓	-
	MFR_AVS_SET	R/W	2	-	✓
C9h	MFR_SLOPE_SR_7P_8P_R1	R/W	2	✓	
	MFR_AVS_WARN_MASK	R/W	2	-	✓
CAh	MFR_SLOPE_SR_9P_10P_R1 /78P_R2	R/W	2	✓	-
	MFR_PMB_SET	R/W	2	-	✓
CBh	MFR_SLOPE_SR_11P_12P_R1 /5P_6P_R2	R/W	2	✓	-
	MFR_OSR_SET_R1	R/W	2	-	✓
CCh	MFR_SLOPE_SR_13P_14P_R1 /3P_4P_R2	R/W	2	✓	✓
	MFR_OSR_SET_R2	R/W	2	✓	✓
CDh	MFR_SLOPE_SR_15P_16P_R1 /1P_2P_R2	R/W	2	✓	-
D0h	READ_CS1_R1	R	2	✓	-
	READ_CS1_R2	R	2	-	✓
D1h	READ_CS2_R1	R	2	✓	-
	READ_CS2_R2	R	2	-	✓
D2h	READ_CS3_R1	R	2	✓	-
	READ_CS3_R2	R	2	-	✓
D3h	READ_CS4_R1	R	2	✓	-
	READ_CS4_R2	R	2	-	✓
D4h	READ_CS5_R1	R	2	✓	-
	READ_CS5_R2	R	2	-	✓
D5h	READ_CS6_R1	R	2	✓	-
	READ_CS6_R2	R	2	-	✓
D6h	READ_CS7_R1	R	2	✓	-
	READ_CS7_R2	R	2	-	✓

PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1
D7h	READ_CS8_R1	R	2	✓	-
	READ_CS8_R2	R	2		✓
D8h	READ_CS9_R1	R	2	✓	
	READ_DIE_TEMP	R	2	-	✓
D9h	READ_CS10_R1	R	2	✓	-
	FAULT_REPORT0	R	2	-	✓
DAh	READ_CS11_R1	R	2	✓	-
	FAULT_REPORT1	R	2	-	✓
DBh	READ_CS12_R1	R	2	✓	-
	FAULT_REPORT2	R	2	-	✓
DCh	READ_CS13_R1	R	2	✓	-
	FAULT_REPORT3	R	2	-	✓
DDh	READ_CS14_R1	R	2	✓	-
	FAULT_REPORT4	R	2	-	✓
DEh	READ_CS15_R1	R	2	✓	-
	FAULT_REPORT5	R	2	-	✓
DFh	READ_CS16_R1	R	2	✓	-
	FAULT_REPORT6	R	2	-	✓
E0h	FAULT_TIME0	R	2	-	✓
E1h	FAULT_TIME1	R	2	-	✓
E2h	FAULT_TIME2	R	2	-	✓
E3h	FAULT_IMON1_SENSE	R	2	-	✓
E4h	READ_ADDR	R	2	✓	-
	FAULT_IMON2_SENSE	R	2	-	✓
E5h	READ_CONFIG_NUM	R	2	✓	-
	FAULT_VDIFF1_SENSE	R	2	-	✓
E6h	FAULT_VDIFF2_SENSE	R	2	-	✓
E7h	PH_REDUNDANCY_NUM1	R	2	✓	-
	FAULT_VIN_SENSE	R	2	-	✓
E8h	PH_REDUNDANCY_NUM2	R	2	✓	-
	FAULT_FIRST_RECORD	R	2	-	✓
E9h	MFR_PROTEC_PH_R1	R	2	✓	-
	FAULT_RECORD0	R	2	-	✓
EAh	MFR_PROTEC_PH_R2	R	2	✓	-
	FAULT_RECORD1	R	2	-	✓
EBh	FAULT_RECORD2	R	2	-	✓
ECh	FAULT_RECORD3	R	2	-	✓
EDh	FAULT_RECORD4	R	2	-	✓
EEh	FAULT_RECORD5	R	2	-	✓
EFh	FAULT_RECORD6	R	2	-	✓

PAGE 0 REGISTER MAP

PAGE (00h)

The PAGE command on Page 0 provides the ability to configure, control, and monitor all registers, including test mode and NVM, through only one physical address.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
7:2	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
1:0	PAGE	0x00: Page 0. All PMBus commands address the operating registers on Page 0 0x01: Page 1. All PMBus commands address the operating registers on Page 1 0x02: Page 2. All PMBus commands address the test mode registers 0x28: Page 28. All PMBus commands address the NVM registers that are mapped to the operating registers on Page 0 0x29: Page 29. All PMBus commands address the NVM registers that are mapped to the operating registers on Page 1

MFR_OPERATION_R1 (01h)

The MFR_OPERATION_R1 command on Page 0 turns the rail 1 output on and off in conjunction with the input from EN pin, and sets V_{OUT} to the upper or lower margin voltages. The controller stays in the OPERATION command setting mode until a subsequent OPERATION command is received, or a change to EN sets rail 1 to another mode.

Command	MFR_OPERATION_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CONFIG_ID								OPERATION_R1							

Bits	Bit Name	Description
15:8	CONFIG_ID	Sets the 4-digit part number suffix (e.g. MP2882GQNT-xxxx). The 8 highest bytes are fixed to 00. CONFIG_ID sets the 2 lowest bytes' values. Each byte can be between 0 and F in hexadecimal format. Contact an MPS FAE to get the 4-digital part number.
7:0	OPERATION_R1	Sets the operation mode for rail 1. 8'b 00xx xxxx: Hi-Z off 8'b 01xx xxxx: Soft shutdown 8'b 1000 xxxx: Normal on 8'b 1001 xxxx: Margin low 8'b 1010 xxxx: Margin high 8'b 1011 xxxx: AVSBus mode Others: Invalid commands "x" means not applicable.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page 0 clears any fault bits in the following registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), and STATUS_CML (7Eh).

This command is write-only. There is no data byte for this command.

MFR_NVM_WP (10h)

The MFR_NVM_WP command on Page 0 controls writing to the PMBus device. This command provides protection against accidental changes. This command is not intended to provide protection against deliberate changes to the device's configuration or operation.

All support commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Command	MFR_NVM_WP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_STORE_TEST_WP								WRITE_PROTECT				MFR_STORE_NVM_WP			

Bits	Bit Name	Description
15:8	MFR_STORE_TEST_WP	0x85: A command can be issued to automatically store the NVM auto-test pattern (FDh on Page 0 and Page 1) can be issued. Other: No command can be issued to automatically store the NVM auto-test pattern (FDh on Page 0 and Page 1)
7:4	WRITE_PROTECT	Enables the PMBus WRITE_PROTECT command. 0x8: Disable all writes except to the WRITE_PROTECT command 0x4: Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 0x2: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands 0x0: Enable writes to all commands Others: Invalid commands
3:0	MFR_STORE_NVM_WP	0x9: A command can be issued to store data to the NVM Others: No command can be issued to store data to the NVM

RESTORE_ALL_CODE (16h)

The RESTORE_ALL_CODE command on Page 0 instructs the PMBus device to copy the Page 0 and Page 1 contents, including the internal trim registers, from the NVM, and overwrite the matching locations in the operating memory. Any items in user store that do not have matching locations in the operating memory are ignored.

This command cannot be used while the device is outputting power, and is ignored if attempted.

This command is write-only. There is no data byte for this command.

VOUT_COMMAND_R1 (21h)

The VOUT_COMMAND_R1 command on Page 0 sets the rail 1 V_{REF} VID in PMBus override mode.

Command	VOUT_COMMAND_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	0	MFR_FB_PI_R1				X	VOUT_COMMAND_R1									

Bits	Bit Name	Description
15	MFR_VCAL_I_R1_BIT6	Fixed to 0.
14:11	MFR_FB_PI_R1	Fixed to 2.
10	RESERVED	Reserved.
9:0	VOUT_COMMAND_R1	Sets the rail 1 V_{REF} (VID_DAC V_{OUT}) in PMBus VID mode. 1 VID_STEP/LSB. VID_STEP is determined by MFR_VOUT_LOOP_CTRL (B2h), bits[15:14].

VOUT_TRIM_R1 (22h)

The VOUT_TRIM_R1 command applies a fixed offset voltage to the commanded rail 1 V_{OUT}. This value cannot be stored to the NVM, and can only be changed on the fly.

Command	VOUT_TRIM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	VOUT_TRIM_R1						

Bits	Bit Name	Description
15:7	RESERVED	Reserved.
6:0	VOUT_TRIM_R1	Sets the V_{OUT} offset voltage on rail 1. This register does not have a NVM cell, which means it can only be changed on the fly. The NVM cannot modify this command. The default value is 0V. 1 VID_STEP/LSB. VID_STEP is determined via MFR_VOUT_LOOP_CTRL (B2h), bits[15:14].

VOUT_MAX_R1 (24h)

The VOUT_MAX_R1 command on Page 0 sets the maximum V_{REF} limitation on rail 1. VID + offset is limited to VOUT_MAX if the configured VID + offset exceeds VOUT_MAX. This command is effective in PMBus, AVSBus, and SVI2 modes.

Command	VOUT_MAX_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	0	MFR_CB_PI_R1				X	VOUT_MAX_R1									

Bits	Bit Name	Description
15	MFR_VCAL_I_R1_BIT5	Fixed to 0.
14:11	MFR_CB_PI_R1	Fixed to 2. MFR_CB_PI_R1 can be masked by MFR_HIGHBITS_MASK (A4h on Page 1), bit[6]. If MFR_HIGHBITS_MASK = 1, then this register is masked. If MFR_HIGHBITS_MASK = 0, then this command is available.

10	RESERVED	Reserved.
9:0	VOUT_MAX_R1	Set the rail 1 maximum voltage in PMBus, AVSBus, and SVI2 modes. Any VID + offset that exceeds this value is clamped to VOUT_MAX. VID_STEP/LSB. VID_STEP is set by MFR_VOUT_LOOP_CTRL (B2h on Page 0), bits[15:14].

VOUT_MARGIN_HIGH_R1 (25h)

The VOUT_MARGIN_HIGH_R1 command on Page 0 cannot be stored to the NVM, and can only be changed on the fly. This command cannot be modified by the NVM. The default value is 0xB8B0, where 1 VID step is equal to 1.953125mV.

Command	VOUT_MARGIN_HIGH_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	1	0	1	1	1	X	VOUT_MARGIN_HIGH_R1									

Bits	Bit Name	Description
15:11	EXP	Fixed to 10111.
10	RESERVED	Reserved.
9:0	VOUT_MARGIN_HIGH_R1	Sets the rail 1 margin high voltage. 1 VID_STEP/LSB. VID_STEP is determined by MFR_VOUT_LOOP_CTRL (B2h), bits[15:14].

VOUT_MARGIN_LOW_R1 (26h)

The VOUT_MARGIN_LOW_R1 command on Page 0 cannot be stored to the NVM, and can only be changed on the fly. This command cannot be modified by the NVM. The default value is 0xB890, where 1 VID step is equal 1.953125mV.

Command	VOUT_MARGIN_LOW_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	1	0	1	1	1	X	VOUT_MARGIN_LOW_R1									

Bits	Bit Name	Description
15:11	EXP	Fixed to 10111.
10	RESERVED	Reserved.
9:0	VOUT_MARGIN_LOW_R1	Sets the rail 1 margin low voltage. 1 VID_STEP/LSB. VID_STEP is determined by MFR_VOUT_LOOP_CTRL (B2h), bits [15:14].

MFR_VOUT_TRANSITION_RATE_R1 (27h)

The VOUT_TRANSITION_RATE_R1 command on Page 0 sets the rail 1 dynamic VID transition slew rate and EN soft-off slew rate in PMBus mode.

Command	MFR_VOUT_TRANSITION_RATE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X		VOUT_TRANSITION_RATE_R1												

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

13	MFR_OFF_SR_SEL_R1	Selects the source of TOFF_FALL_R1, which is only effective during soft shutdown. During EN soft shutdown, the slew rate is always same as the t_{ON} rising slew rate. 1'b0: TOFF_FALL_R1 = TON_RISE_R1 1'b1: TOFF_FALL_R1 = VOUT_TRANSITION_RATE_R1
12:0	VOUT_TRANSITION_ RATE_R1	Sets the rail 1 V_{OUT} slew rate during DVID. Use MFR_SR_RES (A1h on Page 0), bit[0] to set the resolution.

VOUT_DROOP_R1 (28h)

The VOUT_DROOP_R1 command on Page 0 sets the rail 1 load line parameters.

Command	VOUT_DROOP_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function											RDROOP_SET_R1					

Bits	Bit Name	Description
15	MFR_DROOP_BW_ SET_R1	Enables increasing the BW of the AC droop by increasing the bias current. It is for rail 1 only. 1'b0: Disabled 1'b1: Enabled
14		Enables increasing the BW of the AC droop by reducing the compensation capacitor. It is for rail 1 only. 1'b0: Disabled 1'b1: Enabled
13	IACDROOP_GAIN2_ SET_R1	Sets the PMBus load-line slope for Cdroop's second current mirror ratio. 1'b0: 1 1'b1: 1/2
12	MFR_ACLL_EN_R1	Selects the AC or DC load line. 1'b0: DC load line 1'b1: AC load line
11:9	IDROOP_GAIN2_R1	Set the PMBus load-line slope for DC or AC droop's second current mirror ratio (GAIN2) for rail 1. 3'b000: 0 3'b001: 3/4 3'b010: 4/4 3'b011: 5/4 3'b100: 6/4 3'b101: 7/4 3'b110: 8/4 3'b111: 9/4
8:7	IDROOP_GAIN1_R1	Sets the I_{DROOP} first current mirror ratio (GAIN1) on rail 1. The initial load-line slope can be calculated with the following equation: $R_{LL\_INI} = R_{DROOP} \times GAIN1 \times GAIN2$ 2'b00: 1/16 2'b01: 1/8 2'b10: 1/4 2'b11: 1/2

6	SHORT_FIRST_HALF_R1	1'b0: Do not short first half resistors on rail 1 1'b1: Short the first half resistors on rail 1 Set this bit to 1 if R_{DROOP} is below 640Ω.
5:0	RDROOP_SET_R1	Sets the rail 1 R_{DROOP}. 20Ω/LSB. 1.28kΩ maximum.

VOUT_MIN_R1 (2Bh)

The VOUT_MIN_R1 command on Page 0 instructs the device to limit the rail 1 minimum V_{OUT} in PMBus, AVSBus, and SVI2 modes. If the V_{OUT} value decoded from the PMBus interface is below the value set by VOUT_MIN (2Bh), then V_{OUT} is clamped to VOUT_MIN.

Command	VOUT_MIN_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_VCAL_I_R1_5LSB					X	VOUT_MIN_R1									

Bits	Bit Name	Description
15:11	MFR_VCAL_I_R1_5LSB	Fixed to 10.
10	RESERVED	Reserved.
9:0	VOUT_MIN_R1	Sets the minimum VID in PMBus, AVSBus, and SVI2 modes on rail 1. Any VID below this value is clamped to VOUT_MIN. 1 VID_STEP/LSB. VID_STEP is determined by MFR_VOUT_LOOP_CTRL (B2h), bits[15:14].

MFR_FREQUENCY_SWITCH_R1 (33h)

The MFR_FREQUENCY_SWITCH command on Page 0 sets the rail 1 f_{SW}. f_{SW} ranges between 200kHz and 5.11MHz, with 10kHz per step.

Command	MFR_FREQUENCY_SWITCH_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_CS_LOOP_TH_7LSB_R1							FREQUENCY_SWITCH_R1								

Bits	Bit Name	Description
15:9	MFR_CS_LOOP_TH_7LSB_R1	The 7LSB of MFR_CS_LOOP_TH_R1, which sets the threshold of the current imbalance function.
8:0	FREQUENCY_SWITCH_R1	Sets f_{SW} in direct format. 10kHz/LSB.

IOUT_OC_FAULT_LIMIT_R1 (46h)

The IOUT_OC_FAULT_LIMIT command on Page 0 sets the rail 1 I_{OUT} over-current (OC) fault threshold.

Command	IOUT_OC_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OCP_SPIKE_R1								OCP_TDC_R1							

Bits	Bit Name	Description
15:8	OCP_SPIKE_R1	Sets the rail 1 OCP_SPIKE_TOTAL current level DAC value. 6.25mV/LSB. The threshold can be calculated with the following equation: OCP_SPIKE_TOTAL = OCP_SPIKE x K_{CS} x G_{IMON} x R_{IMON} / 6.25
7:0	OCP_TDC_R1	Sets the rail 1 OCP_TDC_TOTAL current level DAC value. 6.25mV/LSB. The threshold can be calculated with the following equation: OCP_TDC_TOTAL = OCP_TDC x K_{CS} x G_{IMON} x R_{IMON} / 6.25

IOUT_OC_FAULT_RESPONSE_R1 (47h)

The IOUT_OC_FUALT_RESPONSE command on Page 0 sets the rail 1 over-current protection (OCP) related options and values.

Command	IOUT_OC_FAULT_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									MFR_OCPTDC_TRIGDELAY_R1							

Bits	Bit Name	Description
15:14	MFR_OCP_MODE_R1	Selects the protection mode for both OCP_TDC and OCP_SPIKE. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 6 times (not recommend OCP_SPIKE)
13	MFR_OCP_TDC_EN_R1	Enables over-current protection (OCP_TDC). 1'b0: Disabled 1'b1: Enabled
12:8	MFR_OCPTDC_ ACTIONDELAY_R1	Sets the OCP_TDC fault action time, which is the delay between when the OCP_L signal asserts and an action is taken (e.g. hiccup mode or shutdown). 1µs/LSB.
7:0	MFR_OCPTDC_ TRIGDELAY_R1	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts whether the sensed inductor current exceeds the OCP_TDC threshold for the blanking time. 20µs/LSB.

MFR_PH_FAULT_SET_R1 (4Ah)

The MFR_PH_FAULT_SET command on Page 0 sets the current ripple detection related parameters.

Command	MFR_PH_FAULT_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						IOUT_OC_WARN_LIMIT_R1										

Bits	Bit Name	Description
15:14	MFR_PH_FAULT_TIME_2MSB	The 2MSB of MFR_PH_FAULT_TIME. MFR_PH_FAULT_TIME are used for phase current sense (V_{CS}) detection. If V_{CS} exceeds OCP_PHASE or stays almost equal to V_{CS_REF} (no CS ripple) for the time set by MFR_PH_FAULT_TIME, the phase is considered abnormal. If MFR_CR_DETECT_TIME_SEL, bit[0] = 1, then this register is 2µs/LSB. If MFR_CR_DETECT_TIME_SEL, bit[0] = 0, then this register is 20µs/LSB.

13:11	MFR_PH_FAULT_H_ SET	Sets the high threshold for detecting the phase current ripple fault comparator. 3'b000: V_{CS_REF} + 10mV 3'b001: V_{CS_REF} + 20mV 3'b010: V_{CS_REF} + 30mV 3'b011: V_{CS_REF} + 40mV 3'b100: V_{CS_REF} + 50mV 3'b101: V_{CS_REF} + 60mV 3'b110: V_{CS_REF} + 70mV 3'b111: V_{CS_REF} + 80mV
10:0	IOUT_OC_WARN_LIMIT_R1	Sets the rail 1 OC_WARN threshold. If the READ_IOUT (8Ch) value exceeds the set threshold, an over-current (OC) warning occurs, and the OC_WARN flag is asserted. This flag can be read from the PMBus status register or pulled out to GPIO. B7h on Page 0, bit[6] = 1: 0.25A/LSB B7h on Page 0, bit[6] = 0: 0.5A/LSB

OT_FAULT_LIMIT_R1 (4Fh)

The OT_FAULT_LIMIT command on Page 0 sets the over-temperature protection (OTP) fault related operation and values.

Command	OT_FAULT_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		MFR_OTP_HYS_R1							MFR_OTP_LIMIT_R1							

Bits	Bit Name	Description
15	MFR_OTP_MODE_R1	Sets the over-temperature protection (OTP) mode. 1'b0: Latch-off mode 1'b1: Auto-retry mode
14:9	MFR_OTP_HYS_R1	Sets the temperature hysteresis for the OTP threshold. If the junction temperature monitored on the TSENS1 pin is below OTP_LIMIT-OTP_HYS, the PWM initiates a soft start as it would during a normal start-up sequence. 1°C/LSB.
8	MFR_OTP_EN_R1	Enables over-temperature protection (OTP). 1'b0: Disabled 1'b1: Enabled
7:0	MFR_OTP_LIMIT_R1	VR over-temperature protection (OTP) fault limit setting. If the junction temperature monitored on the TSENS1 pin exceeds OTP_LIMIT, the VR shuts off the disabled output. 1°C/LSB.

OT_WARN_LIMIT_R1 (51h)

The OT_WARN_LIMIT command on Page 0 sets the VR_HOT temperature threshold, hysteresis, and TSENS1 mode.

Command	OT_WARN_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		VRHOT_HYS_R1							VRHOT_LIMIT_R1							

Bits	Bit Name	Description
15	CS_RIPPLE_ACTION_EN_R1	Enables removing the fault phase if the CS ripple detects phase redundancy. It is for rail 1 only. 1'b0: Disabled 1'b1: Enabled
14:9	VRHOT_HYS_R1	Sets the hysteresis for VR_HOT. If the temperature sensed on the TSENS1 pin is below (MFR_VRHOT_LIMIT_R1 - MFR_VRHOT_HYS_R1), then the VRHOT flag is de-asserted.
8	VRHOT_EN_R1	Enables VRHOT. 1'b0: Disabled 1'b1: Enabled
7:0	VRHOT_LIMIT_R1	Sets the over-temperature (OT) warning threshold. If the temperature sensed via TSENS1 pin exceeds this threshold, then the VRHOT flag is asserted. 1°C/LSB.

MFR_VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command on Page 0 sets the V_{IN} over-voltage protection (OVP) threshold. This register is in linear format. If the sensed V_{IN} exceeds the VIN_OV fault limit, the VR shuts down immediately.

Command	MFR_VIN_OV_FAULT_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_VIN_SCALE_LOOP								VIN_OV_FAULT_LIMIT							

Bits	Bit Name	Description
15:8	MFR_VIN_SCALE_LOOP	Sets the V_{IN} sensing scale, calculated with the following equation: $VIN\_SCALE\_LOOP = \frac{1280 \times V_{INSEN}}{V_{IN}} = \frac{1280 \times R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}}$ Where R_{TOP} and R_{BOTTOM} are the resistor dividers on the VINSEN pin.
7:0	VIN_OV_FAULT_LIMIT	0.125V/LSB.

TON_RISE_R1 (61h)

The TON_RISE_R1 command on Page 0 sets the rail 1 V_{REF} start-up slew rate.

Command	TON_RISE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					TON_RISE_R1											

Bits	Bit Name	Description
15:13	MFR_TRIMLOOP_TH	Fixed to 0.
12	MFR_SLOWLOOP_TH_HYS	Fixed to 0.
11:0	TON_RISE_R1	Sets the rail 1 V_{OUT} slew rate during start-up. Set the resolution via MFR_SR_RES (A1h on Page 0), bit[0].

STATUS_BYTE (78h)

The STATUS_BYTE command on Page 0 returns 1 byte of information with a summary of the most critical statuses and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		OFF					CML	

Bits	Bit Name	Behavior	Description
7	NVM_BUSY	Live	Reports the live status of the non-volatile memory (NVM). Can't be reset by send CLEAR_FAULTS(03h). 1'b0: The NVM is idle. The NVM write and read with PMBus command is available 1'b1: The NVM is busy. The NVM write and read with PMBus command is unavailable
6	OFF	Live	Indicates whether the rail 1 output is off. This bit is in live mode. It is asserted if the rail 1 output is off. VOUT1 turning off can be caused by protections, EN going low, or if VID = 0. 1'b0: VOUT1 is on 1'b1: VOUT1 is off
5	VOUT_OV_FAULT	Latch	Rail 1 V_{OUT} over-voltage (OV) fault indicator. If rail 1 OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit (absolute or VID). 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	Rail 1 output current over-current (OC) fault indicator. If rail 1 OCP happens, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit (OCP_TDC and OCP_SPIKE). 1'b0: No output OC fault has occurred 1'b1: Output OC fault has occurred
3	VIN_UV_FAULT	Latch	V_{IN} under-voltage (UV) fault indicator. If a V_{IN} UV fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	TEMPERATURE	Latch	Over-temperature (OT) fault and warning indicator. If TSENS1/2 OTP or an OT warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Latch	PMBus communication fault indicator. If a PMBus communications related fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred

0	TSENS2_DIGI_FAULT	Latch	TSENS2 digital sense fault indicator. This function is enabled by MFR_TBD_FLT_EN (A8h on Page 1), bit[14] if the device is in temp merge mode, which set if B7h (on Page 0), bit[5] = 1. If the voltage on TSENS2 exceeds or drops below the value set by MFR_TSENS2_SET (A8h on Page 1), bits[13:8], then a TSENS2 fault occurs and this bit is set and latched. The TSENS2 fault direction is determined by MFR_TSENS2_SET (A8h on Page 1), bit[1]. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No TSENS2 digital sense fault has occurred 1'b1: A TSENS2 digital sense fault has occurred

STATUS_WORD (79h)

The STATUS_WORD (79h) command on Page 0 returns 2 bytes of information with a summary of the device fault/warning conditions. The higher byte gives more detailed information of the fault conditions. The lower byte shares this information with register STATUS_BYTE (78h).

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function						X	X		STATUS_BYTE (78h)							

Bits	Bit Name	Behavior	Description
15	VOUT	Latch	Rail 1 V_{OUT} fault and warning indicator. If a V_{OUT} over-voltage (OV) or under-voltage (UV) protection or warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} fault/warning has occurred 1'b1: A V_{OUT} fault/warning has occurred
14	IOUT	Latch	Rail 1 I_{OUT} fault and warning indicator. Once I_{OUT} fault or warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} fault and warning has occurred 1'b1: An I_{OUT} fault or warning has occurred
13	INPUT	Latch	Input voltage and current fault/warning indicator. If any protection or warning related to V_{IN} or I_{IN} occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No input fault and warning has occurred 1'b1: An input fault or warning has occurred
12	TSENS1	Latch	TSENS1 fault indicator. Once the TSENS1 fault function has been enabled, set MFR_TSNS1_FLT_EN(A8h on Page 1), bit[15] = 1. If the TSENS1 voltage exceeds 2.2V, a TSENS1 fault occurs and this bit is set and latched. Reset this bit by cycling the power on VDD33. 1'b0: No TSENS1 fault has occurred 1'b1: A TSENS1 fault has occurred
11	PG_NOT_ACTIVE	Live	1'b0: PG is active 1'b1: PG is not active
10:9	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

8	WATCH_DOG_OVF or PHASE_REDUNDENCY	Latch	Monitor block timer overflow watchdog indicator. The monitor value calculation has a watchdog timer. If the timer overflows, the calculated monitor value and the timer are reset. Meanwhile, this bit is set. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed This bit also indicates phase redundancy. If either of this scenarios occur, this bit is set. Phase redundancy indication cannot be reset by issuing a CLEAR_FAULTS (03h) command. 1'b0: No phase redundancy fault has occurred 1'b1: A phase redundancy fault has occurred

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 0 returns 1 byte of information with the detailed V_{OUT} fault and warning statuses for rail 1.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X			X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Rail 1 V_{OUT} over-voltage (OV) fault indicator. If output OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
6:5	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
4	VOUT_UV_FAULT	Latch	Rail 1 V_{OUT} under-voltage (UV) fault indicator. If rail 1 UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN_ WARNING	Latch	Rail 1 V_{OUT} has reached VOUT_MAX or VOUT_MIN indicator. If the VID value exceeds VOUT_MAX (24h on Page 0) or is below VOUT_MIN (2Bh Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID exceeds VOUT_MAX or is below VOUT_MIN
2	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
1	LINE_FLOAT	Latch	Rail 1 line-float protection indicator. If a line float fault is detected, the device shuts down the associated rail, and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No line float fault has occurred 1'b1: A line float fault has occurred
0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 0 returns 1 byte of information with the detailed I_{OUT} fault and warning statuses for rail 1.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function				X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Rail 1 output over-current (OC) fault indicator (OCP_TDC and OCP_SPIKE). If output OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6	OCP_UV_FAULT	Latch	Rail 1 output over-current (OC) and under-voltage (UV) dual faults indicator. If output OCP occurs and the UV comparator is set simultaneously, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OC and UV fault has occurred 1'b1: An output OC fault has occurred, and the UV comparator is set
5	IOUT_OC_WARN	Latch	Rail 1 output over-current (OC) warning indicator. If an output OC warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OC warning has occurred 1'b1: An output OC warning has occurred
4:0	RESERVED	N/A	Unused. X indicates that reads are always 0.

STATUS_INPUT (7Ch)

The STATUS_INPUT command on Page 0 returns 1 byte of information with detailed input fault and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X		VIN_UVP		X	X	X

Bits	Bit Name	Behavior	Description
7	VIN_OVP	Latch	V_{IN} over-voltage (OV) fault indicator. If V_{IN} exceeds the VIN_OV fault limit, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6	RESERVED	N/A	Unused. X indicates that reads are always 0.

5	VIN_UV_WARNING	Live	V_{IN} under-voltage (UV) warning indicator. If the sensed V_{IN} drops below the threshold set by VIN_UV_LIMIT (10h on Page 1), bits[13:7], this bit is set. This bit resets once V_{IN} exceeds VIN_UV_LIMIT. 1'b0: No V_{IN} UV warning has occurred 1'b1: A V_{IN} UV warning has occurred
4	VIN_UVP	Latch	V_{IN} under-voltage (UV) fault indicator. If the sensed V_{IN} drops below the value set by VIN_UV_LIMIT (10h on Page 1), bits[6:0], then this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
3	VIN_UVLO_LIVE	Live	V_{IN} under-voltage lockout (UVLO) indicator. If V_{IN} drops below VIN_OFF, this bit is set. This bit resets once V_{IN} exceeds VIN_ON. 1'b0: V_{IN} has exceeded VIN_ON (55h on Page 1), bits[15:8] 1'b1: V_{IN} is below VIN_OFF (55h on Page 1), bits[7:0]
2:0	RESERVED	N/A	Unused. X indicates that reads are always 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command on Page 0 returns 1 byte of information with the temperature related fault and warning conditions.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		VRHOT	X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Over-temperature (OT) fault indicator. If the sensed TSENS1 temperature exceeds the OT fault limit set by OT_FAULT_LIMIT (4Fh on Page 0), bits[7:0], this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
6	VRHOT	Live	VRHOT indicator. Once the sensed TSENS1 temperature exceeds the VRHOT limit set by MFR_VRHOT_SET (51h on Page 0), bits[7:0], this bit is set. This bit is reset once the TSENS1 temperature falls below this limit. 1'b0: No VRHOT fault has occurred 1'b1: A VRHOT fault has occurred
5:0	RESERVED	N/A	Unused. X indicates that reads are always 0.

STATUS_CML (7Eh)

The STATUS_CML command on Page 0 returns 1 byte of information with PMBus communication related faults.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function					X			

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	Invalid PMBus command indicator. If the MP2882 receives an unsupported command code, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	INVALID_DATA	Latch	Invalid PMBus data indicator. If the MP2882 receives unsupported data, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received
5	PEC_ERROR	Latch	PMBus PEC fault indicator. The PMBus interface supports the use of the packet error checking (PEC) byte that is defined in the SMBus standard. The PEC byte is transmitted by the MP2882 during a read transaction, or sent to the MP2882 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed and this bit is set and latched. Send a CLEAR_FAULTS (03h) to reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4	NVM_CRC_ERROR	Latch	CRC fault indicator. When storing the operating memory data to the NVM, the MP2882 calculates a CRC code for each bit, then saves the final CRC code to the NVM. When restoring the NVM data to the operating memory, the MP2882 re-calculates the CRC code with each bit. The MP2882 checks the CRC results when the restoration process is complete. If the CRC result does not match what was stored during the store process, the VR shuts down and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
3	RESERVED	N/A	Unused. X indicates that reads are always 0.
2	CML_FLT_TRG	Latch	If an NVM operation is blocked because the controller is recording a fault to the NVM, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: NVM operation is not blocked 1'b1: NVM operation has been blocked because the controller is recording a fault to the NVM
1	CML_OTHER_FAULTS	Latch	If any of the communication faults listed below occur, this bit is set and latched: 1) Sending too few bits 2) Reading too few bits 3) Host sends or reads too few bytes 4) Reading too many bytes Send a CLEAR_FAULTS (03h) command to reset this bit.
0	NVM_SIG_FAULTS	Latch	When restoring data from the NVM to the memory, the device first checks the signature register in address 00h of the NVM. If the signature register is 0x1234, the restoration process stops immediately, and this bit is set and latched. Send a CLEAR_FAULTS (03h) to reset this bit. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

READ_TSENS1_SENSE (83h)

The READ_TSENS1_SENSE command on Page 0 returns the TSENS1 pin's voltage.

Command	READ_TSENS1_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_TSENS1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_TSENS1	Returns the ADC-sensed voltage on rail 1's TSENS1 pin in direct format. 1.5625mV/LSB.

READ_IMON1 (84h)

The READ_IMON1 command on Page 0 returns the VIMON1 pin's voltage.

Command	READ_IMON1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_IMON1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_IMON1	Returns the ADC-sensed voltage on rail 1's VIMON1 pin in direct format. 1.5625mV/LSB.

READ_VDIFF1_SENSE (85h)

The READ_VDIFF1_SENSE command on Page 0 returns the ADC-sensed VDIFF1 voltage.

Command	READ_VDIFF1_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_VDIFF1_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_VDIFF1_SENSE	Returns the ADC-sensed VDIFF1 voltage in direct format. 1 VID_STEP/LSB. VID_STEP is determined by B2h (on Page 0), bits[15:14].

VFB1_SENSE (86h)

The READ_VFB1_SENSE command on Page 0 returns the ADC-sensed VFB1 voltage.

Command	READ_VFB1_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_VFB1_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_VFB1_SENSE	Returns the ADC-sensed VFB1 voltage in direct format when B2h (on Page 0), bit[9] = 0. 1 VID_STEP/LSB. VID_STEP is determined by B2h (on Page 0), bits[15:14].

READ_VIN (88h)

The READ_VIN command on Page 0 provides 2 bytes to return the sensed V_{IN} based on theVINSEN1 pin in Linear11 format. In VID mode, the returned value ignores bits[15:11] (the exponent value).

Command	READ_VIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	1	1	0	1	1	0	READ_VIN									

Bits	Bit Name	Description
15:11	EXP	Fixed to 11011.
10	RESERVED	Fixed to 0.
9:0	READ_VIN	Returns the sensed V_{IN} in Linear11 format. 31.25mV/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 0 returns the sensed VOSEN - VORTN voltage for rail 1.

Command	READ_VOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	READ_VOUT											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that reads are always 0.
11:0	READ_VOUT	Returns the rail 1 V_{OUT}, calculated with the following equation: V_{OUT} = READ_VOUT(8Bh) x VID_STEP Where VID_STEP is determined by B2h (on Page 0), bits[15:14].

READ_IOUT (8Ch)

The READ_IOUT command on Page 0 returns the sensed I_{OUT} for rail 1 in direct format.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP					READ_IOUT										

Bits	Bit Name	Description
15:11	EXP	This bit is determined by MFR_VR_CONFIG1 (B7h on Page 0), bit[6]. B7h, bit[6] = 0: 5'b11111 B7h, bit[6] = 1: 5'b11110

10:0	READ_IOUT	Returns the sensed I_{OUT}. The resolution is determined by MFR_VR_CONFIG1 (B7h on Page 0), bit[6]. B7h, bit[6] = 0: 0.5A/LSB B7h, bit[6] = 1: 0.25A/LSB

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 0 returns the temperature sensed on the TSENS1 pin in direct format.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	X	X	X	READ_TEMP							

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:8	RESERVED	Unused. X indicates that reads are always 0.
7:0	READ_TEMP	Returns the temperature sensed on the TSENS1 pin. 1°C/LSB.

READ_VBOOT1 (91h)

The READ_VBOOT1 command on Page 0 returns selected the VBOOT1 value.

Command	READ_VBOOT1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function				VBOOT1												

Bits	Bit Name	Description
15:13	RESERVED	Always returns 0.
12:8	VBOOT1	Always return the selected VBOOT1 number, which is between 0 and 31.
7:0	RESERVED	Reserved.

READ_POUT (96h)

The READ_POUT command on Page 0 returns the rail 1 P_{OUT} value.

Command	READ_POUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_POUT															

Bits	Bit Name	Description
15:0	READ_POUT	Returns P_{OUT}. Convert the read value to the actual power (in Watts) using MFR_VR_CONFIG, bit[6], and the equations below: B7h, bit[6] = 1: $P_{OUT}(W) = \frac{READ\_POUT}{8}$ B7h, bit[6] = 0: $P_{OUT}(W) = \frac{READ\_POUT}{4}$

PMBUS_REVISION (98h)

The PMBUS_REVISION command on Page 0 on returns the revision of the PMBus to which the device is compliant.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	PMBUS_REVISION							

Byte	Byte Name	Description
7:0	PMBUS_REVISION	Always returns 0x33. This means the MP2882 supports PMBus revision to 1.3.

MFR_ID (99h)

The MFR_ID command on Page 0 returns the unique identity for the VR vendor. It is block read only.

Byte	Byte Name	Description
3	Character 3	Always reads as 0x4D. This represents “M.”
2	Character 2	Always reads as 0x50. This represents “P.”
1	Character 1	Always reads as 0x53. This represents “S.”

MFR_MODEL (9Ah)

MFR_MODEL command on Page 0 returns the unique identity for the product. It is block read only.

Byte	Byte Name	Description
6	Character 6	Always reads as 0x4D. This represents “M.”
5	Character 5	Always reads as 0x50. This represents “P.”
4	Character 4	Always reads as 0x32. This represents “2.”
3	Character 3	Always reads as 0x38. This represents “8.”
2	Character 2	Always reads as 0x38. This represents “8.”
1	Character 1	Always reads as 0x32. This represents “2.”

MFR_REVISION (9Bh)

MFR_REVISION command on Page 0 returns the silicon revision tracking number.

Bits	Bit Name	Description
7:0	REVISION	Returns the MP2882 product silicon revision tracking number. 0x00: Silicon Rev 0 0x01: Silicon Rev 1

MFR_DATE (9Dh)

MFR_DATE command on Page 0 returns the part’s date of manufacture with the format ASCII “DDMMYY”. For example, if the manufacture date is 06/15/2019, the MFR_DATE value is: 0x31 35 30 36 31 39. It is block read only.

Byte	Byte Name	Description
6	Character 6	DD. Identifies the day that the part was manufactured.
5	Character 5	
4	Character 4	MM. Identifies the month that the part was manufactured.
3	Character 3	
2	Character 2	YY. Identifies the year that the part was manufactured.
1	Character 1	

MFR_APS_OPTI_R1 (9Fh)

The MFR_APS_OPTI_R1 command on Page 0 sets the rail 1 APS related timing and behaviors.

Command	MFR_APS_OPTI_R1															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TON_DELAY_R1							APS_COMP_CNT					APS_COMP_LEVEL			

Bits	Bit Name	Description
15:11	TON_DELAY_R1	100µs/LSB.
10	MFR_AVS_IOUT_RES1	Sets the AVSBus I_{OUT} report resolution. 1'b0: 10mA/LSB 1'b1: 20mA/LSB
9	MFR_APS_OPTI_R1	Enables V_{REF} compensation when exiting decay mode. The compensation voltage level and slew rate are the same as with automatic phase-shedding (APS) compensation. 1'b0: Disabled 1'b1: Enabled
8:4	APS_COMP_CNT	The MP2882 provides positive compensation on V_{REF} during phase-shedding to reduce undershoot. V_{REF} compensation is implemented by adding a PMBus-configurable positive voltage on the DC loop COMP. After phase-shedding starts, the voltage returns to 0V step by step with a time interval. APS_COMP_CNT sets the time interval between each step. 50ns/LSB.
3:0	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce undershoot. The compensation is added to V_{REF} when phase-shedding occurs. 1.37mV/LSB.

MFR_VR_CONFIG2 (A1h)

The MFR_VR_CONFIG2 command on Page 0 sets some basic functions for the MP2882.

Command	MFR_VR_CONFIG2															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	MFR_DEBUG_MODE_EN	Fixed to 0.
14	MFR_AVSBUS_REFIX_MODE	Selects when the MP2882 issues a status response frame to the CPU during dynamic VID transitions. It is only effective in AVSBus override mode. 1'b0: The MP2882 issues a status response frame when either rail settles 1'b1: The MP2882 issues a status response frame when both rails settle
13	MFR_DIS_PREFIX_MODE	Selects the behavior mode of the status response frame in AVSBus mode when VID is controlled by the PMBus interface. 1'b0: A status response frame is issued from the VR to the CPU when any of the AVSBus status bits (OCW, UVW, OTW, or OPW) flags are changed 1'b1: A status response frame is not issued from the VR to the CPU when any of the AVSBus status bits (OCW, UVW, OTW, or OPW) flags are changed

12	MFR_SETTLE_PREFIX_MODE	Selects the behavior of issuing status response frame during AVSBus DVID. 1'b0: Slave-only phases issue a status response frame when getting the status of the corresponding rail 1'b1: In addition to the GET_STATUS command, the slave also issues a status response frame if the VDONE flag is 1
11	WATCH_DOG_EN	Enables the watchdog. 1'b0: Disabled 1'b1: Enabled
10	MFR_SDM_FRAC_EN	Enables the decimal fraction of sigma-delta (Σ-Δ) and the delay line. 1'b0: Disabled 1'b1: Enabled
9	MFR_VRMON_LPF	Sets the V_{OUT} report filter parameters. 1'b0: No V_{OUT} report filter 1'b1: 2-point moving average filter
8	MFR_IOUT_LPF	Sets the I_{OUT} report filter parameters. 1'b0: No I_{OUT} report filter 1'b1: 2-point moving average filter
7:6	MFR_OVUV_DVID_MODE	2'b00: Ignore VID-OV/UV during DVID, start-up, and shutdown 2'b01: Ignore VID-OV/UV during start-up and shutdown 2'b10: Ignore VID-OV/UV during DVID 2'b11: VID-OV/UV is always available once power is enabled
5	MFR_OVP_DISCH_MODE	Sets the PWM behavior after over-voltage protection (OVP) occurs. 1'b0: If OVP occurs, all PWMs are pulled low until V_{OUT} drops below the RVP threshold. Then all PWMs remain in tri-state, regardless of whether V_{OUT} exceeds the RVP threshold 1'b1: If OVP occurs, all PWMs are pulled low for as long as V_{OUT} exceeds the RVP threshold. All PWMs remain low if V_{OUT} reaches the RVP threshold again
4	MFR_OCP_SS_BLK	Enables block over-current protection (OCP) phase limit protection during soft start. 1'b0: Disabled 1'b1: Enabled
3	MFR_OCCMP_SEL	Over-current protection (OCP_TDC) mode selection. 1'b0: OCP_TDC uses the digital comparator of OCP_TDC 1'b1: OCP_TDC uses the analog comparator of OCP-SPIKE. In this mode, OCP_SPIKE should be disabled
2	VIN_TON_CAL_MODE	Selects the V_{IN} value when calculating t_{ON}. 1'b0: Updates t_{ON} with READ_VIN (88h) 1'b1: Updates t_{ON} with READ_VN (88h) when V_{IN} exceeds 0.75V. If V_{IN} drops below 0.75V, t_{ON} does not update
1	MFR_VIN2TON_EN	Enables V_{IN} to influence the PWM on time. 1'b0: Disabled. V_{IN} does not influence the PWM on time 1'b1: Enabled. V_{IN} influences the PWM on time
0	MFR_SR_RES	Sets the start-up and DVID slew rate resolution. 1'b0: 1mV/µs 1'b1: 0.01mV/µs

MFR_VR_CONFIG3 (A2h)

The MFR_VR_CONFIG3 command on Page 0 sets some basic functions for the MP2882.

Command	MFR_VR_CONFIG3															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		MFR_SW_BLOCK_SET							0	0	0					1

Bits	Bit Name	Description
15	VBOOT_MODE	1'b0: Start-up to VOUT_COMMAND (21h on Page 0 and Page 1) 1'b1: Start-up to the VBOOT1/2 voltage as determined by the VBOOT1/2 pin.
14:11	MFR_SW_BLOCK_SET	Sets the slope low leakage switch turn on time in DCM. The PWM set signal is blocked when turning on the low-leakage switch. 10ns/LSB.
10	MFR_SLOPE_LEAKAGE	Enables turning off the low-leakage switch after the current source in DCM to avoid leakage (via the high-leakage switch) from the current source of slope compensation. 1'b0: Disabled 1'b1: Enabled
9	AMD_MODE	Selects the AVSBus or SVI2 interface. 1'b0: Pin 23, pin 24, and pin 25 comprise the AVSBus interface 1'b1: Pin 23, pin 24, and pin 25 comprise the SVI2 interface
8	REFIN_EN	Fixed to 0.
7	COMPDAC_HI_SET	Fixed to 0.
6	MFR_DBG_FIX_SR	Fixed to 0.
5	MFR_HIZ_HIGH_BLOCK_EN	Enables the minimum tri-state time constraint when PWM goes from tri-state to high. The minimum tri-state time is set by PWM_MIN_TIME1 (A3h on Page 0 and Page 1), bits[5:0]. 1'b0: Disables the minimum tri-state time constraint when PWM goes from Hi-Z to high 1'b1: Enables the minimum tri-state time constraint when PWM goes from tri-state to high
4:3	MFR_BG_CHOP_MODE	Selects the bandgap chop frequency. 2'b00: Disables the bandgap chop 2'b01: 125kHz 2'b10: 250kHz 2'b11: 500kHz
2	DAC_CMP_EN_R2	Enables smooth transition when DVID going down is preempted by DVID going up. It is for rail 2 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: Disable the rail 2 V_{REF} filter function in continuous DVID down and up 1'b1: Enable the rail 2 V_{REF} filter function in continuous DVID down and up
1	DAC_CMP_EN_R1	Enables smooth transition when DVID going down is preempted by DVID going up. It is for rail 1 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: Disable the rail 1 V_{REF} filter function in continuous DVID down and up 1'b1: Enable the rail 1 V_{REF} filter function in continuous DVID down and up
0	MFR_DBG_FIX32	Fixed to 1.

MFR_PWM_LIMIT1 (A3h)

The MFR_PWM_LIMIT1 command on Page 0 sets the minimum pulse width when PWM is high, low, or in tri-state. It is effective for both rails.

Command	MFR_PWM_LIMIT1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	MFR_MIN_LOW_TIME									MFR_MIN_HIZ_TIME					

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	MFR_MIN_LOW_TIME	Sets the minimum PWM low time. 10ns/LSB with a -5ns offset. The minimum PWM low time can be calculated with the following equation: (PWM_MIN_LOW_TIME x 10 - 5) ns
8:6	MFR_MINON_TIME	Sets the minimum PWM high time. 10ns/LSB with a -5ns offset. The minimum PWM high time can be calculated with the following equation: (PWM_MIN_HIGH_TIME x 10 - 5) ns
5:0	MFR_MIN_HIZ_TIME	Sets the minimum PWM tri-state time. 10ns/LSB with a -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: (PWM_MIN_TRI_TIME x 10 - 5) ns

MFR_CORE_OTP_SET (A4h)

The MFR_CORE_OTP_SET command on Page 0 sets the chip's over-temperature protection (OTP) related parameters.

Command	MFR_CORE_OTP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			MFR_CORE_OTP_HYS						MFR_CORE_OTP_LIMIT							

Bits	Bit Name	Description
15	MFR_CORE_OTP_EN	Enables chip over-temperature protection (OTP). The MP2882 monitors the chip temperature voltage level. If the chip's sensed voltage exceeds the configurable threshold set by A4h, bits[7:0], an OT fault occurs and both shut down rails immediately. 1'b0: Disabled 1'b1: Enabled
14	MFR_CORE_OTP_ MODE	Selects the chip over-temperature (OT) fault action mode. 1'b0: Latch-off mode 1'b1: Auto-retry mode
13:8	MFR_CORE_OTP_HYS	Sets the temperature hysteresis of the core OTP threshold. If the junction temperature monitored by register D8h falls below OTP_LIMIT_OTP_HYS, the PWM initiates soft start as it would during a normal start-up. 1°C/LSB.
7:0	MFR_CORE_OTP_ LIMIT	Sets the over-temperature (OT) threshold for chip OTP. Calculate the OTP threshold (T_{OTP_DIE}) with the following equation: $A4h[7:0] = \frac{3 \times T_{OTP\_DIE} + 275}{3.125}$

MFR_OV_UV_LIMIT_R1 (A5h)

The MFR_OV_UV_LIMIT command on Page 0 sets the rail 1 V_{OUT} under-voltage protection (UVP) and over-voltage protection (OVP) thresholds.

Command	MFR_OV_UV_LIMIT_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			UVP_VID_R1			OVP_VID_R1			OVP_ABS_R1							

Bits	Bit Name	Description
15	RESERVED	Reserved to 0.
14	OVUV_DIV2_R1	Fixed to 0.
13:11	UVP_VID_R1	3'b000: V_{REF} - 425mV 3'b001: V_{REF} - 375mV 3'b010: V_{REF} - 325mV 3'b011: V_{REF} - 275mV 3'b100: V_{REF} - 225mV 3'b101: V_{REF} - 175mV 3'b110: V_{REF} - 125mV 3'b111: V_{REF} - 75mV
10:8	OVP_VID_R1	3'b001: V_{REF} + 200mV 3'b010: V_{REF} + 325mV 3'b100: V_{REF} + 450mV Others: Invalid commands
7:0	OVP_ABS_R1	Sets an absolute over-voltage protection (OVP) threshold. OVP occurs if V_{OUT} exceeds this value. 10mV/LSB. Set OVP_ABS_R1 to 0 to disable this function.

MFR_OV_UV_RESPONSE_R1 (A6h)

The MFR_OV_UV_RESPONSE command on Page 0 sets the rail 1 V_{OUT} under-voltage protection (UVP) and over-voltage protection (OVP) fault modes.

Command	MFR_OV_UV_RESPONSE_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			MFR_UVP_DELAYTIME_R1								MFR_OVP_VID_DELAYTIME_R1					

Bits	Bit Name	Description
15:14	MFR_UVP_MODE_R1	Sets the under-voltage (UV) fault mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 3 times
13:8	MFR_UVP_DELAYTIME_R1	Sets the V_{OUT} under-voltage protection (UVP) blanking time. UVP occurs if the sensed V_{DIFF} drops below the UVP threshold for the UVP blanking time. 20µs/LSB.
7:6	MFR_OVP_VID_MODE_R1	Sets the over-voltage (OV) fault mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Invalid mode 2'b11: Retry 3 times

5:0	MFR_OVP_VID_ DELAYTIME_R1	Sets the OVP_VID blanking time. If the OVP_VID condition lasts for longer than the OVP_VID blanking time, a OVP_VID fault occurs. 100ns/LSB.

MFR_FAST_OCP_SET_R1 (A7h)

The MFR_FAST_OCP_SET command on Page 0 sets the rail 1 per-phase over-current protection (OCP) threshold.

Command	MFR_FAST_OCP_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OCP_PHASE_SET_R1															

Bits	Bit Name	Description
15:8	OCP_PHASE_SET_R1	Sets the per-phase valley current limit DAC value. 5mV/LSB.
7:4	OCPSPIKE_ ACTIONDELAY_R1	Sets the OCP_SPIKE fault action time. The time delay is between when the OCP_L signal asserts and the action occurs (current limiting, hiccup mode, entry, or shutdown). 1µs/LSB.
3:0	OCPSPIKE_TRIGDELAY _R1	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for the set OCP_SPIKE blanking time. 200ns/LSB.

MFR_SMBALERT_MASK (A8h)

The MFR_SMBALERT_MASK command on Page 0 masks the faults, which means ALT_P# does not assert if a fault occurs.

Command	MFR_SMBALERT_MASK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	OTP	1’b0: If over-temperature protection (OTP) occurs or VRHOT occurs, ALT_P# does not assert 1’b1: No mask
14	OVP	1’b0: If over-voltage protection (OVP) occurs, ALT_P# does not assert 1’b1: No mask
13	UVP	1’b0: If under-voltage protection (UVP) occurs, ALT_P# does not assert 1’b1: No mask
12	VOUT_MAXMIN	1’b0: If VOUT_MAX or VOUT_MIN exceed the warning threshold, ALT_P# does not assert 1’b1: No mask
11	OCP	1’b0: If over-current protection (OCP) occurs, ALT_P# does not assert 1’b1: No mask
10	SCP	1’b0: If OCP and UVP occur, ALT_P# does not assert 1’b1: No mask
9	CML_INVALID_CMD	1’b0: If an invalid command in the communication fault (see the STATUS_CML section on page 55) occurs, ALT_P# does not assert 1’b1: No mask

8	CML_INVALID_DATA	1’b0: If an invalid data in a communication fault (see the STATUS_CML section on page 55) occurs, ALT_P# does not assert 1’b1: No mask
7	PEC_ERROR	1’b0: If a packet error checking (PEC) error occurs, ALT_P# does not assert 1’b1: No mask
6	CRC_ERROR	1’b0: If a cyclic redundancy check (CRC) error occurs, ALT_P# does not assert 1’b1: No mask
5	CMD_FLT_BLK_TRG	1’b0: If a command fault block trig occurs, ALT_P# does not assert 1’b1: No mask
4	CML_OTHER_FAULT	1’b0: If another communication fault (see the STATUS_CML section on page 55) occurs, ALT_P# does not assert 1’b1: No mask
3	NVM_FAULT	1’b0: If a non-volatile memory (NVM) fault occurs, ALT_P# does not assert 1’b1: No mask
2	VIN_OVP	1’b0: If a V_{IN} over-voltage (OV) fault occurs, ALT_P# does not assert 1’b1: No mask
1	VIN_UV_WARN	1’b0: If V_{IN} under-voltage (UV) warning occurs, ALT_P# does not assert 1’b1: No mask
0	PHASE_REDUNDANCY	1’b0: If a phase redundancy fault occurs, ALT_P# does not assert 1’b1: No mask

MFR_ADDR_PMBUS (A9h)

The MFR_ADDR_PMBUS command on Page 0 sets the PMBus address and DrMOS temperature gain and offset parameters.

Command	MFR_ADDR_PMBUS															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function										PMBUS_ADDR_VALUE						

Bits	Bit Name	Description
15:14	MFR_AVS_TH_SEL	2b’00: 3.3V 2b’01: 1.8V 2b’10: Configurable (see register C7h on Page 1, bits[11:10]) 2b’11: 1.2V
13:12	MFR_PMB_TH_SEL	2b’00: 3.3V 2b’01: 1.8V 2b’10: Configurable (see register C7h on Page 1, bits[11:10]) 2b’11: 1.2V
11:10	MFR_TEMP_GAIN_R2	Selects the DrMOS temp gain and offset. 2b’00: MFR_TEMP_CALC_R2 uses the value of 13h on Page 1, bits[15:0] 2b’01: MFR_TEMP_CALC_R2 uses 0x500A 2b’10: MFR_TEMP_CALC_R2 uses the value of 13h on Page 1, bits[15:0] 2b’11: MFR_TEMP_CALC_R2 uses 0x64B5
9:8	MFR_TEMP_GAIN_R1	Selects the DrMOS temp gain and offset. 2b’00: MFR_TEMP_CALC_R1 uses the value of 13h on Page 1, bits[15:0] 2b’01: MFR_TEMP_CALC_R1 uses 0x500A 2b’10: MFR_TEMP_CALC_R1 uses the value of 13h on Page 1, bits[15:0] 2b’11: MFR_TEMP_CALC_R1 uses 0x64B5

7	PMBUS_ADDR_MODE	Sets the PMBus address 4LSB mode. 1'b0: Set the PMBus address 4LSB from the ADDR pin voltage 1'b1: Set the PMBus address 4LSB from the register
6:0	PMBUS_ADDR_VALUE	Sets the PMBus address setting or reading. Bit[7] = 1'b1, the 7-bit PMBus address is sets via the register Bit[7] = 1'b0, the 3MSB is configured by the register. The 4LSB of the PMBus address is determined by the ADDR pin voltage, and bits[3:0] are read-only. Any values written to bits[3:0] are ignored

MFR_VOUT_CALC_R1 (AAh)

The MFR_VOUT_CALC command on Page 0 sets the gain and offset of the V_{OUT} calculations.

Command	MFR_VOUT_CALC_R1															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	OFFSET						GAIN							

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:8	OFFSET	Adds an offset to the V_{OUT} report in register READ_VOUT (8Bh). This bit is for the rail 1 V_{OUT} report only. This bit is in two's complement format. Bit[13] is the signed bit. 1 VID_STEP/LSB. If the VID_STEP is 6.25mV, the voltage list below shows the direct and real-world values: 6'b00 0000: 0mV 6'b00 0001: +6.25mV 6'b01 1111: +193.75mV 6'b10 0000: -200mV 6'b10 0001: -193.75mV 6'b11 1111: -6.25mV
7:0	GAIN	Sets the gain from the ADC-sensed VOSEN - VORTN voltage to the V_{OUT} report in register READ_VOUT (8Bh). It is for rail 1 only. READ_VOUT can be calculated with the following equation: $READ\_VOUT = \frac{1024 \times V_{OUT} \times VDIFF\_GAIN}{1.6} \times \frac{GAIN}{2^7} + OFFSET$ Where VDIFF_GAIN is determined by B2h (on Page 0), bits[11:10].

MFR_IOUT_GAIN_PMBUS_R1 (ABh)

The MFR_IOUT_GAIN_PMBUS command on Page 0 sets the I_{OUT} gain PMBus report. The MP2882 senses I_{OUT} by sensing the voltage on IMON. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch on Page 0).

Command	MFR_IOUT_GAIN_PMBUS_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function							IOUT_CAL_GAIN									

Bits	Bit Name	Description
15:13	MFR_IMON_RES_SET_R1	Sets the rail 1 IMON resistor. 3'b 000: 2.5kΩ 3'b 001: 5kΩ 3'b 010: 10kΩ 3'b 011: 40kΩ 3'b 1xx: Disconnected
12	MFR_IMON_GAIN_SET_R1	1'b0: The IMON1 current mirror gain is 1/8 1'b1: The IMON1 current mirror gain is 1/16
11:10	GAIN_SEL	Sets the exponent value for the IOUT_CAL_GAIN calculation equation of this command.
9:0	IOUT_CAL_GAIN	Sets the current-sense gain for the PMBus report. The gain can be calculated with the following equation: $IOUT\_CAL\_GAIN=\frac{1024}{1.6}\times K_{CS}\times G_{IMON}\times R_{IMON}\times 2^{(6-GAIN\_SEL)}$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bits[11:10] of this command.

MFR_IOUT_OS_PMBUS_R1 (ACh)

The MFR_IOUT_OS_PMBUS_R1 command on Page 0 sets the rail 1 I_{OUT} PMBus report offset. The offset is for I_{OUT} over-reporting or under-reporting. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch on Page 0).

Command	MFR_IOUT_OS_PMBUS_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				MFR_IOUT_CALC_PH_OFS_R1							MFR_IOUT_CALC_OFFSET_R1					

Bits	Bit Name	Description
15:13	MFR_CS_LOOP_TH_3MSB_R1	The 3MSB of MFR_CS_LOOP_TH_R1. MFR_CS_LOOP_TH_R1 is used to set the current imbalance threshold for rail 1. If the current balance loop tune value exceeds this threshold, the related phase is considered abnormal.
12:6	MFR_IOUT_CALC_PH_OFS_R1	Adds an offset according the phase number. A larger N results in a larger offset. Bit[12] is the signed bit.
5:0	MFR_IOUT_CALC_OFFSET_R1	Adds current report offset to READ_IOUT (8Ch).

MFR_IOUT_CAL_AVSBUS_R1 (ADh)

The MFR_IOUT_CAL_AVSBUS_R1 command on Page 0 sets the rail 1 I_{OUT} AVSBus report offset and gain.

Command	MFR_IOUT_CAL_AVSBUS_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_IOUT_AVS_OS_R1					MFR_IOUT_AVS_GAIN_R1										

Bits	Bit Name	Description
15:11	MFR_IOUT_AVS_OS_R1	Sets the rail 1 AVSBus mode I_{OUT} report resolution, which is determined by 9Fh (on Page 0), bit[10]. 9Fh, bit[10] = 0: 160mA/LSB 9Fh, bit[10] = 1: 320mA/LSB Bit[15] is the signed bit.
10:0	MFR_IOUT_AVS_GAIN_R1	Sets the rail 1 I_{OUT} telemetry report in AVSBus mode. 10mA/LSB. 9Fh, bit[10] = 0: $AVS\_GAIN = \frac{1.6 \times 32 \times 10\text{^}5}{1024 \times K_{CS} \times G_{IMON} \times R_{IMON}}$ 9Fh, bit[10] = 1: $AVS\_GAIN = \frac{1.6 \times 16 \times 10\text{^}5}{1024 \times K_{CS} \times G_{IMON} \times R_{IMON}}$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the IMON resistor (in Ω).

MFR_APS_ITH_SET_R1 (AEh)

The MFR_APS_ITH_SET command on Page 0 sets the rail 1 automatic phase-shedding (APS) level and hysteresis level.

Command	MFR_APS_ITH_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function							MFR_APS_IIL_INC_R1									

Bits	Bit Name	Description
15:14	MFR_APS_HYS_INC_R1	MFR_APS_HYS_R1 = PHASE_NUM_ACTIVE x MFR_APS_HYS_INC_R1 + MFR_APS_HYS_BASE_R1. 1A/LSB
13:10	MFR_APS_HYS_BASE_R1	Sets the basic automatic phase-shedding (APS) hysteresis level. 1A/LSB
9:4	MFR_APS_IIL_INC_R1	MFR_APS_IIL_R1 = PHASE_NUM_ACTIVE x MFR_APS_IIL_INC_R1 + MFR_APS_IIL_BASE_R1. 1A/LSB
3:0	MFR_APS_IIL_BASE_R1	Sets the basic APS basic phase shedding level. 1A/LSB

MFR_APS_CTRL_SET_R1 (AFh)

The MFR_APS_CTRL_SET command on Page 0 sets rail 1 automatic phase-shedding (APS) related timing and behaviors.

Command	MFR_APS_CTRL_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function												MFR_PS_ENTER_TIME_R1				

Bits	Bit Name	Description
15:12	MFR_ADP_OC_NPS_EXIT_CNT_R1	Sets the period delay count from when OCP_PHASE is triggered to when the device exits automatic phase-shedding (APS). 100ns/LSB.
11	MFR_ADP_OC_NPS_EXIT_EN_R1	Enables OCP_PHASE protection to exit APS at any power state. 1'b0: Disable the OCP_PHASE signal to trigger any phase to full-phase operation 1'b1: Enable the OCP_PHASE signal to trigger any phase to full-phase operation

10	MFR_ADP_OC_1PS_EXIT_EN_R1	Enables OCP_PHASE protection to exit APS during 1-phase DCM/CCM only. 1'b0: Disabled 1'b1: Enabled
9	MFR_ADP_UV_EXIT_EN_R1	Sets rail 1 V_{FB} < VID - 25mV to enter full-phase operation. 1'b0: Disabled 1'b1: Enabled
8	MFR_ADP_PFM_EXIT_EN_R1	Enables the rail 1 frequency to increase to exit APS. 1'b0: Disabled 1'b1: Enabled
7:5	MFR_APS_FS_COEF_R1	3'b000: The f_{SW} limit threshold is 40%*(Ts/N-Tblank) 3'b001: The f_{SW} limit threshold is 60%*(Ts/N-Tblank) 3'b010: The f_{SW} limit threshold is 80%*(Ts/N-Tblank) 3'b011: The f_{SW} limit threshold is 100%*(Ts/N-Tblank) 3'b100: The f_{SW} limit threshold is 120%*(Ts/N-Tblank) 3'b101: The f_{SW} limit threshold is 140%*(Ts/N-Tblank) 3'b110: The f_{SW} limit threshold is 160%*(Ts/N-Tblank) 3'b111: The f_{SW} limit threshold is 180%*(Ts/N-Tblank) N: phase number, Ts: period time, Tblank: blank time
4:0	MFR_PS_ENTER_TIME_R1	Sets the phase-shedding delay time. If the reported load current remains below the APS threshold for the time set by APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE, the controller enters APS and automatically sheds the phase count according to the load current.

MFR_APS_CTRL23_SET_R1 (B0h)

The MFR_APS_CTRL23_SET command on Page 0 sets rail 1 automatic phase-shedding (APS) related timing and behaviors.

Command	MFR_APS_CTRL23_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						RETURN_APS_DELAY							MFR_PS_INTERVAL_R1			

Bits	Bit Name	Description
15	MFR_FS_DETECT_R1	Enables the device to exit phase-shedding according to the PWM1 off time. The PWM minimum off time is excluded from the PWM off time. 1'b0: Disable PWM1 off time detection to exit automatic phase-shedding (APS) 1'b1: Enable PWM1 off time detection to exit APS
14	FS_EXIT_APS_EN_NP	Enables the device to exit phase-shedding according to the multi-phase PWM interval time between consecutive phases. The time threshold is set by register 4Bh on Page 0. The PWM blanking time is excluded from the PWM interval time. 1'b0: Disable multi-phase PWM interval time detection to exit APS 1'b1: Enable multi-phase PWM interval time detection to exit APS
13:11	FS_EXIT_APS_CNT_1P	Set the continuous count of the PWM1 off time condition to exit phase-shedding. If the PWM off time conditions meet the counting threshold, the controller exits APS immediately.
10:7	RETURN_APS_DELAY	Sets the minimum full-phase runtime after exiting APS due to a f_{SW} event. 20µs/LSB.
6:4	FS_EXIT_APS_CNT_NP	Sets the continuous count of the multi-phase PWM interval time to exit phase-shedding. If the PWM interval condition meets the counting threshold, the controller exits APS immediately.

3:0	MFR_PS_INTERVAL_R1	Set the phase by phase dropping time intervals. It is only effective when p0/B4h bit [14] is set to 0. 2.5µs/LSB

MFR_FSCB_LOOP_CTRL_R1 (B1h)

The MFR_FSCB_LOOP_CTRL_R1 command on Page 0 sets the rail 1 f_{SW} and current balance loop.

Command	MFR_FSCB_LOOP_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function													CB_LOOP_HOLD_TIME			

Bits	Bit Name	Description
15	MFR_FS_LOOP_EN_R1	Enables the f_{SW} loop. The frequency loop keeps f_{SW} constant, and equal to the set value at different input voltages and load currents. This bit is active for both rails. 1'b0: Disabled 1'b1: Enabled
14	MFR_FS_LOOP_CTRL_R1	Holds frequency loop regulation if a load transient event is detected (e.g. V_{FB} exceeds the VFB+ window or VFB- window). 1'b0: Disables holding the frequency loop if a load transient event is detected 1'b1: Enable holding the frequency loop if a load transient event is detected
13	PS_HOLD_FS_EN_R1	Holds frequency loop regulation if the phase count changes. 1'b0: Disables holding the frequency loop if the phase count changes 1'b1: Enable holding the frequency loop if the phase count changes
12	DVID_HOLD_FS_EN_R1	Holds frequency loop regulation if DVID occurs. 1'b0: Disables holding the frequency loop if DVID occurs 1'b1: Enable holding the frequency loop if DVID occurs
11:8	MFR_FS_LOOP_CNT_R1	Sets the minimum frequency loop hold time if any load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set. 100µs/LSB.
7	MFR_CB_LOOP_EN_R1	Enables the current balance loop. 1'b1: Enabled 1'b0: Disabled
6	PRD_HOLD_CB_EN_R2	Holds the current balance loop if the PWM period meets the PWM switching period condition set via PMBus command MFR_APS_CTRL23 (B7h), bits[1:0]. 1'b0: Disables holding the current balance loop if the PWM switching period condition is met 1'b1: Enable holding the current balance loop if the PWM switching period condition is met
5	PS_HOLD_CB_EN_R2	Holds the current balance loop if the phase count changes. 1'b0: Disables holding the current balance loop if the phase count changes 1'b1: Enable holding the current balance loop if the phase count changes
4	DVID_HOLD_CB_EN_R2	Holds the current balance loop if DVID occurs. 1'b0: Disable holding the current balance loop if DVID occurs 1'b1: Enable holding the current balance loop if DVID occurs
3:0	CB_LOOP_HOLD_TIME	Sets the current balance loop hold time. If any load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set, then the current balance loop stops regulating for a time set with the CB_LOOP_THOLD command. 100µs/LSB.

MFR_VOUT_LOOP_CTRL_R1 (B2h)

The MFR_VOUT_LOOP_CTRL_R1 command on Page 0 sets the rail 1 V_{OUT} loop parameters.

Command	MFR_VOUT_LOOP_CTRL_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	MFR_VID_RES_R1	Sets the VID step. VID step with VDIFF gain = 1, V_{OUT} = 0V to 1.55V: 2'b00: 6.25mV 2'b01: 5mV 2'b1x: Invalid command VID step with VDIFF gain = 0.5, V_{OUT} = 0V to 3V: 2'b00: 6.25mV 2'b01: 5mV 2'b1x: Invalid command VID step with VDIFF gain = 0.8, V_{OUT} = 0V to 2V: 2'b00: 1.953125mV 2'b01: 5mV 2'b1x: Invalid command VID step with VDIFF gain = 0.4, V_{OUT} = 0V to 3.3V: 2'b00: 3.906250mV 2'b01: 5mV 2'b1x: Invalid command
13	VIN_BLOCK_EN	Enables the V_{IN} sense block current-sense (CS) ripple detection. 1'b0: Disabled 1'b1: Enabled
12	MFR_VDIFF_LOOP_EN_R1	Fixed to 0.
11:10	MFR_VDIFF_GAIN_SEL_R1	Sets the rail 1 remote-sense amplifier gain: 2'b00: 1 2'b01: 0.5 2'b10: 0.8 2'b11: 0.4
9	MFR_DC_REF_SEL_R1	1'b0: The COMP error amplifier (EA) uses V_{FB} and V_{REF} 1'b1: The COMP EA uses V_{DIFF} and V_{REF}
8	DC_LOOP_EN_DCM	Enables DC loop calibration in discontinuous conduction mode (DCM). 1'b0: Disabled 1'b1: Enabled
7	DC_LOOP_EN	Enables DC loop calibration in DCM and continuous conduction mode (CCM). 1'b0: Disabled 1'b1: Enabled
6	PRD_HOLD_DC_EN_R1	Holds the DC loop if the PWM time interval meets the PWM switching period condition set by PMBus command MFR_VR_CONFIG1 (B7h), bits[1:0]. 1'b0: Disable holding DC loop when the PWM switching period condition is met 1'b1: Enable holding the DC loop when the PWM switching period condition is met

5	PS_HOLD_DC_EN_R1	Holds the DC loop when the phase count is changes. 1'b0: Disable holding the DC loop when the phase count changes 1'b1: Enable holding the DC loop when the phase count changes
4	TRANS_HOLD_DC_EN_R1	Holds the DC loop regulation if a load transient event is detected (e.g. V_{FB} exceeds VFB+ window or VFB- window.) 1'b0: Disable holding the DC loop when the VFB+/- window condition is met 1'b1: Enable holding the DC loop when the VFB+/- window condition is met
3:0	MFR_DC_LOOP_CNT_R1	Sets the DC loop minimum hold time in direct format. 200μs/LSB with a +100μs offset.

MFR_SETTLE_CTRL_R1 (B3h)

The MFR_SETTLE_CTRL command on Page 0 sets the DVID parameters.

Command	MFR_SETTLE_CTRL_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						MFR_RISE_STEP_R1					MFR_SETTLE_DELAY_R1					

Bits	Bit Name	Description
15:11	MFR_DROOPFALL_DELAY_R1	Sets the delay time between V_{REF} reaching the target (VID + DROOP_VID) and V_{REF} falling back to VID. 50ns/LSB.
10:6	MFR_RISE_STEP_R1	Sets the extra VID step count for rail 1 when DVID is up. The extra VID steps compensate for the droop caused by the output capacitor charging during DVID up. 1 step/LSB.
5:0	MFR_SETTLE_DELAY_R1	Fixed to 5.

MFR_PHASE_SET_R1 (B4h)

The MFR_PHASE_SET command on Page 0 sets the rail 1 phase configuration.

Command	MFR_PHASE_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				PSI_SET_R1							0	MFR_PHASE_NUM_CFG_R1				

Bits	Bit Name	Description
15	MFR_AUTO_PS_EN_R1	Enables rail 1 automatic phase-shedding (APS) mode. 1'b0: Disabled 1'b1: Enabled
14	MFR_PHASHED_EXIT_MOD_R1	Sets the phase-dropping mode during phase-shedding. The phase-shedding may be due to APS. 1'b0: Shed phases one by one with a configured delay time. The delay time is set with the DROP_PHASE_WAIT_TIME command 1'b1: Drop the phase count to the target immediately
13	PSI_SET_ENR1	Forces the rail 1 power state to follow what is set by bits[12:8] of this command. 1'b0: Disable the forced power state 1'b1: Enable the forced power state. The system's active phase number is determined by bits[12:8] of this command

12:8	PSI_SET_R1	Sets the forced phase number for rail 1. 5'b00000: DCM 5'b00001: 1-phase CCM 5'b00010: 2-phase CCM 5'b00011: 3-phase CCM 5'b00100: 4-phase CCM 5'b00101: 5-phase CCM 5'b00110: 6-phase CCM 5'b00111: 7-phase CCM 5'b01000: 8-phase CCM 5'b01001: 9-phase CCM 5'b01010: 10-phase CCM 5'b01011: 11-phase CCM 5'b01100: 12-phase CCM 5'b01101: 13-phase CCM 5'b01110: 14-phase CCM 5'b01111: 15-phase CCM 5'b10000: 16-phase CCM
7:6	MFR_REDUNDANT_PH_R1	Fixed to 0.
5	RESERVED	Fixed to 0.
4:0	MFR_PHASE_NUM_CFG_R1	Sets the rail 1 phase number.

MFR_GPIO_SEL (B5h)

The MFR_GPIO_SEL command on Page 0 sets the GPIO-related parameters.

Command	MFR_GPIO_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function												0		GPIO1_SEL		

Bits	Bit Name	Description
15	GPIO_ALT_MERGE	1'b0: The alert signal in GPIO1/2 indicates a single rail, and refers to GPIO_ALT_SEL (B5h on Page 1), bit[15] 1b'1: The alert signal in GPIO1/2 indicates both rails. GPIO_ALT_SEL (B5h on Page 1), bit[15] has no effect. The alert signal includes the following: OCP_SPIKE#, OCP_TDC#, VRHOT#, OC_WARN#, OCP_L, and DRMOS_FAULT#.
14	GPIO1_STATE	1'b0: GPIO1 is an open-drain output 1'b1: GPIO1 is a push-pull output
13	PWROK_SEL	1'b0: PWROK is from GPIO1 1'b1: PWROK is from TSENS2
12	EN_PIN_SEL	1'b0: Only the EN pin is available 1'b1: Both the EN and EN_L2 pins are available
11	GPIO1_DIN_EN	1'b0: Set GPIO1 to an IO output 1'b1: Set GPIO1 to a digital IO input
10	GPIO1_EN_SEL	1'b0: Set GPIO1 to the monitoring function 1'b1: Set GPIO1 to the EN function. GPIO1_DIN_EN must be set to 1

9:8	MFR_EN1_SEL	2'b00: The internal rail 1 enable signal is from the EN pin 2'b01: The internal rail 1 enable signal is from the GPIO1 pin 2'b10: The internal rail 1 enable signal is from the GPIO2 pin 2'b11: The internal rail 1 enable signal is from the internal rail 2 power good (PG) signal
7:6	VIMON_SEL	Sets the VIMONx buffer on the GPIO pin. 2'b00: Disable buffer 2'b01: Enable buffer to VIMON1_FIL 2'b10: Enable buffer to VIMON2_FIL 2'b11: Disable buffer
5	VCS_REF_SEL	Enables the VCS_REF buffer on the GPIO pin. 1'b0: Disabled 1'b1: Enabled
4	REFIN_SEL	Fixed to 0.
3	PG_MERGE	1'b0: The PG_L1 pin is for single-rail PG (see MFR_PG_SEL (B5h on Page 1), bit[3]) 1'b1: The PG_L1 pin is for both rails' PG. MFR_PG_SEL (B5h on Page 1), bit[3] is ineffective
2:0	GPIO1_SEL	3'b000: GPIO1_DOUT = 1 or 0, determined by MFR_GPIO_FORCE (B5h on Page 1), bit[12] 3'b001: GPIO1_DOUT = FAULT# 3'b010: GPIO1_DOUT = rail 1 or rail 2 PG, determined by MFR_PH_SEL (B5h on Page 1), bit[13] 3'b011: GPIO1_DOUT = OCP_L 3'b100: GPIO1_DOUT = DRMOS_FAULT# 3'b101: GPIO1_DOUT = OC_WARN# 3'b110: GPIO1_DOUT = VHOT# 3'b111: GPIO1_DOUT = OCP_TDC# or OCP_SPIKE#, determined by MFR_GPIO_FORCE (B5h on Page 1), bit[12]

MFR_PG_DELAY_R1 (B6h)

The MFR_PG_DELAY_R1 command on Page 0 sets the power good (PG) on and off delay times.

Command	MFR_PG_DELAY_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PGOFF_DELAY_R1						MFR_PGON_DELAY_R1									

Bits	Bit Name	Description
15:10	MFR_PGOFF_DELAY_R1	Sets the power good (PG) off delay time. 5µs/LSB.
9:0	MFR_PGON_DELAY_R1	Sets the PG on delay time. 5µs/LSB.

MFR_VR_CONFIG1 (B7h)

The MFR_VR_CONFIG1 command on Page 0 sets some basic functions for the MP2882.

Command	MFR_VR_CONFIG1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function												1				

Bits	Bit Name	Description
15	MFR_LOW_PWR	Enables low-power mode. In low-power mode, the analog and digital block is off and the controller consumes very little quiescent current when EN is off. In regular power mode, EN going low only disables the output power. Meanwhile, the analog and NVM are still active. It is effective after power is reset on VDD33. 1'b0: Disabled 1'b1: Enabled
14	MFR_EN_SOFT_OFF_EN	Enables EN soft shutdown. 1'b0: Hi-Z off 1'b1: Soft shutdown
13	MFR_TON_PS2_R2	Enables t_{ON} 1/4 reduction in DCM for rail 2. When t_{ON} reduction is enabled, t_{ON} is reduced by 1/4 in 1-phase DCM to reduce the output voltage ripple. 1'b0: Disabled 1'b1: Enabled
12	MFR_TON_PS2_R1	Enables t_{ON} 1/4 reduction in DCM for rail 1. When t_{ON} reduction is enabled, t_{ON} is reduced by 1/4 in 1-phase DCM to reduce the output voltage ripple. 1'b0: Disabled 1'b1: Enabled
11	PG_FOR_VID=0V	Selects the PG state when DVID goes to 0V. 1'b0: High 1'b1: Low
10	VORTN_LINE_FLOAT_EN	Enables detecting whether the VORTN pin is floating or not for both rails. 1'b0: Disabled 1'b1: Enabled
9	VOSEN_LINE_FLOAT_EN	Enables detecting whether the VOSEN pin is floating or not for both rails. 1'b0: Disabled 1'b1: Enabled
8	RCS_2K_SEL	Selects the internal current-sense resistor. 1'b0: 1kΩ 1'b1: 2kΩ
7	IOUT_REPORT_SEL_R2	Sets the rail 2 PMBus READ_IOUT report resolution. 1'b0: 0.5A/LSB 1'b1: 0.25A/LSB
6	IOUT_REPORT_SEL_R1	Sets the rail 1 PMBus READ_IOUT report resolution. 1'b0: 0.5A/LSB 1'b1: 0.25A/LSB
5	MFR_TEMP_MERGE	Selects the TSENS1 pin function. 1'b0: Individual mode. Use the TSENS1 pin to monitor rail 1's temperature report. Use the TSENS2 pin to monitor rail 2's temperature reporting 1'b1: Merge mode. Use the TSENS1 pin to monitor both rails' temperature reports. Both rails' DrMOS TEMP pins should be shorted together with the TSENS1 pin
4	MFR_DRMOS_TYPE	Fixed to 1.

3:2	MFR_PRD_CHG_TH_SEL_R2	Sets the rail 2 change period threshold to stop the DC loop, CB loop, or FS loop. 2'b00: (t_{SW} / n - t_{BLANK_TIME}) x 3/8 2'b01(t_{SW} / n - t_{BLANK_TIME}) x 4/8 2'b10: (t_{SW} / n - t_{BLANK_TIME}) x 5/8 2'b11(t_{SW} / n - t_{BLANK_TIME}) x 6/8 Where t_{SW} is the setting period, *n* is the phase number, and t_{BLANK_TIME} is set by registers BCh and BDh on Page 1.
1:0	MFR_PRD_CHG_TH_SEL_R1	Sets the rail 1 change period threshold to stop the DC loop, CB loop, or FS loop. 2'b00: (t_{SW} / n - t_{BLANK_TIME}) x 3/8 2'b01(t_{SW} / n - t_{BLANK_TIME}) x 4/8 2'b10: (t_{SW} / n - t_{BLANK_TIME}) x 5/8 2'b11(t_{SW} / n - t_{BLANK_TIME}) x 6/8 Where t_{SW} is the setting period, *n* is the phase number, and t_{BLANK_TIME} is set by registers BBh, BCh, and BDh on Page 0.

MFR_CS_OS_ZONE (B8h)

The MFR_CS_OS_ZONE command on Page 0 sets the 16 phases to 9 fences. Each fence shares one current-sense offset (thermal balance offset).

For example, FENCE0 is MFR_CS_OS0, FENCE1 is MFR_CS_OS1, and FENCE8 is MFR_CS_OS8.

If MFR_CS_OS0 is set to 0, the others values use B9h and Bah on Page 0. Each zone is set to ZONE1, ZONE2, and so on. Each zone can be set between 0 and 3.

The fence is determined by each zone, which is described below:

- FENCE1 = ZONE1 + 1
- FENCE2 = ZONE2 + 1 + FENCE1
- FENCE3 = ZONE3 + 1 + FENCE2
- FENCE4 = ZONE4 + 1 + FENCE3
- FENCE5 = ZONE5 + 1 + FENCE4
- FENCE6 = ZONE6 + 1 + FENCE5
- FENCE7 = ZONE7 + 1 + FENCE6
- FENCE8 = ZONE8 + 1 + FENCE7

Command	MFR_CS_OS_ZONE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	MFR_CS_OS_ZONE8	Sets the phase number for ZONE8 (between 0 and 3). FENCE8 can be calculated with the following equation: FENCE8 = ZONE8 + 1 + FENCE7 The FENCE7 + 1 to FENCE8 phases are determined by MFR_CS_OS8 (BAh on Page 0, bits[15:12]).
13:12	MFR_CS_OS_ZONE7	Sets the phase number for ZONE7 (between 0 and 3). FENCE7 can be calculated with the following equation: FENCE7 = ZONE7 + 1 + FENCE6 The FENCE6 + 1 to FENCE7 phases are determined by MFR_CS_OS7 (BAh on Page 0, bits[11:8]).

11:10	MFR_CS_OS_ZONE6	Sets the phase number for ZONE6 (between 0 and 3). FENCE6 can be calculated with the following equation: FENCE6 = ZONE6 + 1 + FENCE5 The FENCE5 + 1 to FENCE6 phases are determined by MFR_CS_OS6 (BAh on Page 0, bits[7:4]).
9:8	MFR_CS_OS_ZONE5	Sets the phase number for ZONE5 (between 0 and 3). FENCE5 can be calculated with the following equation: FENCE5 = ZONE5 + 1 + FENCE4 The FENCE4 + 1 to FENCE5 phases are determined by MFR_CS_OS5 (BAh on Page 0, bits[3:0]).
7:6	MFR_CS_OS_ZONE4	Sets the phase number for ZONE4 (between 0 and 3). FENCE4 can be calculated with the following equation: FENCE4 = ZONE4 + 1 + FENCE3 The FENCE3 + 1 to FENCE4 phases are determined by MFR_CS_OS4 (B9h on Page 0, bits[15:12]).
5:4	MFR_CS_OS_ZONE3	Sets the phase number for ZONE3 (between 0 and 3). FENCE3 can be calculated with the following equation: FENCE3 = ZONE3 + 1 + FENCE2 The FENCE2 + 1 to FENCE3 phases are determined by MFR_CS_OS3 (B9h on Page 0, bits[11:8]).
3:2	MFR_CS_OS_ZONE2	Sets the phase number for ZONE2 (between 0 and 3). FENCE2 can be calculated with the following equation: FENCE2 = ZONE2 + 1 + FENCE1 The FENCE1 + 1 to FENCE2 phases are determined by MFR_CS_OS2 (B9h on Page 0, bits[7:4]).
1:0	MFR_CS_OS_ZONE1	Sets the phase number for ZONE1 (between 0 and 3). FENCE1 can be calculated with the following equation: FENCE1 = ZONE1 + 1 The 1 to FENCE1 phases are determined by MFR_CS_OS1 (B9h on Page 0, bits[3:0]).

MFR_CS_OS_PART1 (B9h)

The MFR_CS_OS_PART1 command on Page 0 sets each fence's current-sense offset (thermal balance offset).

Command	MFR_CS_OS_PART1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_CS_OS4				MFR_CS_OS3				MFR_CS_OS2				MFR_CS_OS1			

Bits	Bit Name	Description
15:12	MFR_CS_OS4	Sets OFFSET4 for the ADC-sensed value. It is in two's complement format. Bit[15] is the signed bit. 0.625A/LSB (2kΩ R_{CS}, 5μA/A DrMOS CS gain).
11:8	MFR_CS_OS3	Sets OFFSET3 for the ADC-sensed value. It is in two's complement format. Bit[11] is the signed bit. 0.625A/LSB (2kΩ R_{CS}, 5μA/A DrMOS CS gain).
7:4	MFR_CS_OS2	Sets OFFSET2 for the ADC-sensed value. It is in two's complement format. Bit[7] is the signed bit. 0.625A/LSB (2kΩ R_{CS}, 5μA/A DrMOS CS gain).

3:0	MFR_CS_OS1	Sets OFFSET1 for the ADC-sensed value. It is in two's complement format. Bit[3] is the signed bit. 0.625A/LSB (2kΩ R_{CS}, 5μA/A DrMOS CS gain).

MFR_CS_OS_PART2 (BAh)

The MFR_CS_OS_PART1 command on Page 0 sets each fence's current-sense offset (thermal balance offset).

Command	MFR_CS_OS_PART2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_CS_OS8				MFR_CS_OS7				MFR_CS_OS6				MFR_CS_OS5			

Bits	Bit Name	Description
15:12	MFR_CS_OS8	Sets OFFSET8 for the ADC-sensed value. It is in two's complement format. Bit[15] is the signed bit. 0.625A/LSB (2kΩ R_{CS}, 5μA/A DrMOS CS gain).
11:8	MFR_CS_OS7	Sets OFFSET7 for the ADC-sensed value. It is in two's complement format. Bit[11] is the signed bit. 0.625A/LSB (2kΩ R_{CS}, 5μA/A DrMOS CS gain).
7:4	MFR_CS_OS6	Sets OFFSET6 for the ADC-sensed value. It is in two's complement format. Bit[7] is the signed bit. 0.625A/LSB (2kΩ R_{CS}, 5μA/A DrMOS CS gain).
3:0	MFR_CS_OS5	Sets OFFSET5 for the ADC-sensed value. It is in two's complement format. Bit[3] is the signed bit. 0.625A/LSB (2kΩ R_{CS}, 5μA/A DrMOS CS gain).

MFR_BLANK_TIME1_R1 (BBh)

The MFR_BLANK_TIME command on Page 0 configures the first set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 1 only.

Three sets of SLOPE_RESET_TIME and PWM_BLANK_TIME can be set via registers BBh, BCh, and BDh on Page 0. One of these times is selected as real-time value according to the operation phase number. The relationship is described below:

$$SLOPE\_RESET\_TIME=\begin{cases} SLOPE\_RESET\_TIME1(\text{reg BBh bit[11:6]}), & \text{phase num} \geq PHS\_NUM\_LV1 \\ SLOPE\_RESET\_TIME2(\text{reg BCh bit[11:6]}), & PHS\_NUM\_LVL2 \leq \text{phase num} < PHS\_NUM\_LV1 \\ SLOPE\_RESET\_TIME3(\text{reg BDh bit[11:6]}), & \text{phase num} < PHS\_NUM\_LV2 \end{cases}$$

$$PWM\_BLANK\_TIME=\begin{cases} PWM\_BLANK\_TIME1(\text{reg BBh bit[5:0]}), & \text{phase num} \geq PHS\_NUM\_LV1 \\ PWM\_BLANK\_TIME2(\text{reg BCh bit[5:0]}), & PHS\_NUM\_LV2 \leq \text{phase num} < PHS\_NUM\_LV1 \\ PWM\_BLANK\_TIME3(\text{reg BDh bit[5:0]}), & \text{phase num} < PHS\_NUM\_LV2 \end{cases}$$

Where PHS_NUM_LV1 is the phase number set by register MFR_BLANK_TIME1_R1 (BBh on Page 0), bits[15:12], and PHS_NUM_LV2 is the phase number set by register MFR_BLANK_TIME2_R1 (BCh on Page 0), bits[15:12].

Command	MFR_BLANK_TIME1_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					MFR_SLOPE_RESET_TIME1_R1						MFR_PHASE_BLANK_TIME1_R1					

Bits	Bit Name	Description
15:12	MFR_BLANK_TIME_ LV1_R1	Sets the phase number threshold to the slope compensation reset time and PWM blanking time.

11:6	MFR_SLOPE_RESET_TIME1_R1	Configures the first set of slope compensation reset times. The slope compensation reset time should be not exceed the PWM blanking time set by PWM_BLANK_TIME, bits[5:0] in register MFR_BLANK_TIME1_R1 (BBh on Page 0). 5ns/LSB.
5:0	MFR_PHASE_BLANK_TIME1_R1	Configures the PWM blanking time between two consecutive phases. 5ns/LSB. The actual blanking time value is equal to the internal fixed 20ns + BBh, bits[5:0] x 5ns.

MFR_BLANK_TIME2_R1 (BCh)

The MFR_BLANK_TIME2_R1 command on Page 0 configures the first set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 1 only.

Command	MFR_BLANK_TIME2_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					MFR_SLOPE_RESET_TIME2_R1						MFR_PHASE_BLANK_TIME2_R1					

Bits	Bit Name	Description
15:12	MFR_BLANK_TIME_LV2_R1	Sets the phase number threshold to the slope compensation reset time and PWM blanking time.
11:6	MFR_SLOPE_RESET_TIME2_R1	Configures the first set of slope compensation reset times. The slope compensation reset time should be not exceed the PWM blanking time set by PWM_BLANK_TIME, bits[5:0] in register MFR_BLANK_TIME2_R1 (BCh on Page 0). 5ns/LSB.
5:0	MFR_PHASE_BLANK_TIME2_R1	Configures the PWM blanking time between two consecutive phases. 5ns/LSB. The actual blanking time value is equal to the internal fixed 20ns + BCh, bits[5:0] x 5ns.

MFR_BLANK_TIME3_R1 (BDh)

The MFR_BLANK_TIME3_R1 command on Page 0 configures the second set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 1 only.

Command	MFR_BLANK_TIME3_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	MFR_SLOPE_RESET_TIME3_R1						MFR_PHASE_BLANK_TIME3_R1					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	MFR_SLOPE_RESET_TIME3_R1	Configures the first set of slope compensation reset times. The slope compensation reset time should be not exceed the PWM blanking time set by PWM_BLANK_TIME, bits[5:0] in register MFR_BLANK_TIME3_R1 (BDh on Page 0). 5ns/LSB.
5:0	MFR_PHASE_BLANK_TIME3_R1	Configures the PWM blanking time between two consecutive phases. 5ns/LSB. The actual blanking time value is equal to the internal fixed 20ns + BDh, bits[5:0] x 5ns.

MFR_SLOPE_CNT_SET_R1 (BEh)

The MFR_SLOPE_CNT_SET command on Page 0 sets the slope CNT coefficient.

Command	MFR_SLOPE_CNT_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_TRIM_DCM_R1						MFR_SLOPE_CNT_DCM_R1									

Bits	Bit Name	Description
15:12	MFR_TRIM_DCM_R1	Sets the V_{OUT} trim for 4-phase CCM. 2.3mV/LSB.
11:10	MFR_SLOPE_CNT_ COEF_R1	Sets the CCM slope CNT coefficient. 2b'00: CNT x 1.2 2b'01: CNT x 1.3 2b'10: CNT x 1.4 2b'11: CNT x 1.5 Where CNT is t_{SW} / n - $t_{SLOPE\_RESET\_TIME}$, *n* is the phase number, and $t_{SLOPE\_RESET\_TIME}$ is set by registers BBh, BCh, and BDh on Page 0.
9:0	MFR_SLOPE_CNT_DCM _R1	Sets the slope voltage clamp time. 5ns/LSB.

MFR_SLOPE_PEAK_SET_R1 (BFh)

The MFR_SLOPE_PEAK_SET command on Page 0 sets the slope peak value.

Command	MFR_SLOPE_PEAK_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_SLOPE_SW_INI_R1							MFR_SLOPE_SR_SEL				MFR_SLOPE_PEAK_DATA_R1				

Bits	Bit Name	Description
15:9	MFR_SLOPE_SW_INI_ R1	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
8:5	MFR_SLOPE_SR_SEL	4'b0000: Selects number 0 slope parameters 4'b0001: Selects number 1 slope parameters 4'b0010: Selects number 2 slope parameters 4'b0011: Selects number 3 slope parameters 4'b1110: Auto-slope 4'b1111: Auto-slope Others: Invalid commands
4:0	MFR_SLOPE_PEAK_ DATA_R1	Sets the slope peak value. 1.875mV/LSB.

MFR_TRIM_14P_R1 (C0h)

The MFR_TRIM_14P_R1 command on Page 0 sets the slope trim value for 1-phase to 4-phase CCM.

Command	MFR_TRIM_14P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_TRIM_3P_R1				MFR_TRIM3P_R1				MFR_TRIM_2P_R1				MFR_TRIM_1P_R1			

Bits	Bit Name	Description
15:12	MFR_TRIM_4P_R1	Fixed to 0.
11:8	MFR_TRIM_3P_R1	Fixed to 0.
7:4	MFR_TRIM_2P_R1	Fixed to 0.
3:0	MFR_TRIM_1P_R1	Fixed to 0.

MFR_SLOPE_DCM_SET_R1 (C1h)

The MFR_SLOPE_DCM_SET command on Page 0 trims the rail 1 V_{OUT} in 1-phase DCM.

Command	MFR_SLOPE_DCM_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				DRMOS_KCS1			CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15	AUTO_SLOPE_EN	Enables the auto-slope function. 1’b0: Disabled 1’b1: Enabled
14:13	MFR_TRIM_DCM_BIAS_R1	Fixed to 0.
12:10	DRMOS_KCS1	Sets the rail 1 DrMOS current-sense gain. 3'b000: 5μA/A 3'b001: 8.5μA/A 3'b010: 9μA/A 3'b011: 9.7μA/A 3'b100: 10μA/A Other: Reserved
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets current-source value for slope compensation. 0.25μA/LSB.

MFR_PWM_MIN_TIME2 (C2h)

The MFR_PWM_MIN_TIME2 command on Page 0 sets the PWM minimum off time and minimum on-pulse width.

Command	MFR_PWM_MIN_TIME2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								MFR_MINON_LIM				MFR_MINOFF_TIME				

Bits	Bit Name	Description
15:13	MFR_CR_DETECT_TON_TH	Sets the PWM on time. If this time is below (MFR_CR_DETECT_TON_TH x 4 + 4) x 5ns, the device does not detect the phase current ripple to check if there is an abnormal phase.
12:11	MFR_ZCD_SEL	Selects the zero-current detection (ZCD) threshold. 2’b00: The ZCD threshold is the low phase current ripple detection threshold 2’b01: The ZCD threshold is the initial threshold 2’b10: The ZCD threshold is the high phase current ripple detection threshold 2’b11: The ZCD threshold is the initial threshold

10	MFR_ZCD_EN_R2	Enables rail 2 zero-current detection (ZCD). 1'b0: Disabled 1'b1: Enabled
9	MFR_ZCD_EN_R1	Enables rail 1 zero-current detection (ZCD). 1'b0: Disabled 1'b1: Enabled
8:5	MFR_MINON_LIM	Sets the PWM minimum on time. 5ns/LSB with a 5ns offset. The PWM minimum on time can be calculated with the following equation: (PWM_MIN_ON_TIME x 5 + 5) ns
4:0	MFR_MINOFF_TIME	Sets the PWM minimum off time. 20ns/LSB with a 15ns offset. The PWM minimum off time can be calculated with the following equation: (PWM_MIN_OFF_TIME x 20 + 15) ns

MFR_SLOPE_SR_2MSB_1 (C3h)

The MFR_SLOPE_SR_2MSB_1 command on Page 0 provides the high 2MSB setting for the capacitor quantity for the slope voltage in 1-phase to 8-phase CCM.

Command	MFR_SLOPE_SR_2MSB_1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	MFR_SLOPE_SR_8P_2MSB	Sets the 2MSB of the 8-phase capacitor quantity for slope voltage generation.
13:12	MFR_SLOPE_SR_7P_2MSB	Sets the 2MSB of the 7-phase capacitor quantity for slope voltage generation.
11:10	MFR_SLOPE_SR_6P_2MSB	Sets the 2MSB of the 6-phase capacitor quantity for slope voltage generation.
9:8	MFR_SLOPE_SR_5P_2MSB	Sets the 2MSB of the 5-phase capacitor quantity for slope voltage generation.
7:6	MFR_SLOPE_SR_4P_2MSB	Sets the 2MSB of the 4-phase capacitor quantity for slope voltage generation.
5:4	MFR_SLOPE_SR_3P_2MSB	Sets the 2MSB of the 3-phase capacitor quantity for slope voltage generation.
3:2	MFR_SLOPE_SR_2P_2MSB	Sets the 2MSB of the 2-phase capacitor quantity for slope voltage generation.
1:0	MFR_SLOPE_SR_1P_2MSB	Sets the 2MSB of the 1-phase capacitor quantity for slope voltage generation.

MFR_SLOPE_SR_2MSB_2 (C4h)

The MFR_SLOPE_SR_2MSB_2 command on Page 0 provides the high 2MSB setting for the capacitor quantity for the slope voltage in 9-phase to 16-phase CCM.

Command	MFR_SLOPE_SR_2MSB_2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	MFR_SLOPE_SR_16P_2MSB	Sets the 2MSB of the 16-phase capacitor quantity for slope voltage generation.
13:12	MFR_SLOPE_SR_15P_2MSB	Sets the 2MSB of the 15-phase capacitor quantity for slope voltage generation.
11:10	MFR_SLOPE_SR_14P_2MSB	Sets the 2MSB of the 14-phase capacitor quantity for slope voltage generation.
9:8	MFR_SLOPE_SR_13P_2MSB	Sets the 2MSB of the 12-phase capacitor quantity for slope voltage generation.
7:6	MFR_SLOPE_SR_12P_2MSB	Sets the 2MSB of the 12-phase capacitor quantity for slope voltage generation.
5:4	MFR_SLOPE_SR_11P_2MSB	Sets the 2MSB of the 11-phase capacitor quantity for slope voltage generation.
3:2	MFR_SLOPE_SR_10P_2MSB	Sets the 2MSB of the 10-phase capacitor quantity for slope voltage generation.
1:0	MFR_SLOPE_SR_9P_2 MSB	Sets the 2MSB of the 9-phase capacitor quantity for slope voltage generation.

MFR_SLOPE_SR_1P_2P_R1 (C6h)

The MFR_SLOPE_SR_1P_2P_R1 command Page 0 configures the slope compensation for 1-phase and 2-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_1P_2P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CAP_2P		CURRENT_2P						CAP_1P		CURRENT_1P					

Bits	Bit Name	Description
15:14	CAP_2P	Works with C3h, bits[3:2] to set the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_2P. 1.85pF/LSB.
13:8	CURRENT_2P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
7:6	CAP_1P	Works with C3h, bits[1:0] to set the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_1P. 1.85pF/LSB.
5:0	CURRENT_1P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_3P_4P_R1 (C7h)

The MFR_SLOPE_SR_3P_4P_R1 command Page 0 configures the slope compensation for 3-phase and 4-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_3P_4P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CAP_4P		CURRENT_4P						CAP_3P		CURRENT_3P					

Bits	Bit Name	Description
15:14	CAP_4P	Works with C3h, bits[7:6] to set the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_4P. 1.85pF/LSB.
13:8	CURRENT_4P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
7:6	CAP_3P	Works with C3h, bits[5:4] to set the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_3P. 1.85pF/LSB.

5:0	CURRENT_3P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_5P_6P_R1 (C8h)

The MFR_SLOPE_SR_5P_6P_R1 command on Page 0 configures the slope compensation for 5-phase to 6-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_5P_6P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CAP_6P		CURRENT_6P						CAP_5P		CURRENT_5P					

Bits	Bit Name	Description
15:14	CAP_6P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_6P. 1.85pF/LSB.
13:8	CURRENT_6P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
7:6	CAP_5P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_5P. 1.85pF/LSB.
5:0	CURRENT_5P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_7P_8P_R1 (C9h)

The MFR_SLOPE_SR_5P_6P_R1 command on Page 0 configures the slope compensation for 7-phase and 8-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_7P_8P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CAP_8P		CURRENT_8P						CAP_7P		CURRENT_7P					

Bits	Bit Name	Description
15:14	CAP_8P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_8P. 1.85pF/LSB.
13:8	CURRENT_8P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
7:6	CAP_7P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_7P. 1.85pF/LSB.
5:0	CURRENT_7P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_9P_10P_R1 (CAh)

The MFR_SLOPE_SR_9P_10P_R1 command on Page 0 configures the slope compensation for 9-phase and 10-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_9P_10P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CAP_10P		CURRENT_10P						CAP_9P		CURRENT_9P					

Bits	Bit Name	Description
15:14	CAP_10P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_10P. 1.85pF/LSB.
13:8	CURRENT_10P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
7:6	CAP_9P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_9P. 1.85pF/LSB.
5:0	CURRENT_9P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_11P_12P_R1 (CBh)

The MFR_SLOPE_SR_11P_12P_R1 command on Page 0 configures the slope compensation for 11-phase and 12-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_11P_12P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CAP_12P		CURRENT_12P						CAP_11P		CURRENT_11P					

Bits	Bit Name	Description
15:14	CAP_12P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_12P. 1.85pF/LSB.
13:8	CURRENT_12P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
7:6	CAP_11P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_11P. 1.85pF/LSB.
5:0	CURRENT_11P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_13P_14P_R1 (CCh)

The MFR_SLOPE_SR_13P_14P_R1 command on Page 0 configures the slope compensation for 13-phase and 14-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_13P_14P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CAP_14P		CURRENT_14P						CAP_13P		CURRENT_13P					

Bits	Bit Name	Description
15:14	CAP_14P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_14P. 1.85pF/LSB.
13:8	CURRENT_14P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
7:6	CAP_13P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_13P. 1.85pF/LSB.
5:0	CURRENT_13P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_15P_16P_R1 (CDh)

The MFR_SLOPE_SR_15P_16P_R1 command on Page 0 configures the slope compensation for 15-phase and 16-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_15P_16P_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CAP_16P		CURRENT_16P						CAP_15P		CURRENT_15P					

Bits	Bit Name	Description
15:14	CAP_16P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_16P. 1.85pF/LSB.
13:8	CURRENT_16P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
7:6	CAP_15P	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is 16 - CAP_15P. 1.85pF/LSB.
5:0	CURRENT_15P	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.

READ_CS1_R1 (D0h)

The READ_CS1_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS1 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS1_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS1_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS1_R1	Returns the ADC-sensed voltage on rail 1's CS1 pin. 3.125mV/LSB.

READ_CS2_R1 (D1h)

The READ_CS2_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS2 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS2_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS2_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS2_R1	Returns the ADC-sensed voltage on rail 1's CS2 pin. 3.125mV/LSB.

READ_CS3_R1 (D2h)

The READ_CS3_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS3 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS3_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS3_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS3_R1	Returns the ADC-sensed voltage on rail 1's CS3 pin. 3.125mV/LSB.

READ_CS4_R1 (D3h)

The READ_CS4_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS4 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS4_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS4_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS4_R1	Returns the ADC-sensed voltage on rail 1's CS4 pin. 3.125mV/LSB.

READ_CS5_R1 (D4h)

The READ_CS5_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS5 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS5_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS5_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS5_R1	Returns the ADC-sensed voltage on rail 1's CS5 pin. 3.125mV/LSB.

READ_CS6_R1 (D5h)

The READ_CS6_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS6 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS6_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS6_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS6_R1	Returns the ADC-sensed voltage on rail 1's CS6 pin. 3.125mV/LSB.

READ_CS7_R1 (D6h)

The READ_CS7_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS7 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS7_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS7_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS7_R1	Returns the ADC-sensed voltage on rail 1's CS7 pin. 3.125mV/LSB.

READ_CS8_R1 (D7h)

The READ_CS8_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS8 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS8_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS8_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS8_R1	Returns the ADC-sensed voltage on rail 1's CS8 pin. 3.125mV/LSB.

READ_CS9_R1 (D8h)

The READ_CS9_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS9 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS9_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS9_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS9_R1	Returns the ADC-sensed voltage on rail 1's CS9 pin. 3.125mV/LSB.

READ_CS10_R1 (D9h)

The READ_CS10_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS10 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS10_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS10_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS10_R1	Returns the ADC-sensed voltage on rail 1's CS10 pin. 3.125mV/LSB.

READ_CS11_R1 (DAh)

The READ_CS11_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS11 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS11_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS11_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS11_R1	Returns the ADC-sensed voltage on rail 1's CS11 pin. 3.125mV/LSB.

READ_CS12_R1 (DBh)

The READ_CS12_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS12 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS12_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS12_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS12_R1	Returns the ADC-sensed voltage on rail 1's CS12 pin. 3.125mV/LSB.

READ_CS13_R1 (DCh)

The READ_CS13_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS13 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS13_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS13_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS13_R1	Returns the ADC-sensed voltage on rail 1's CS13 pin. 3.125mV/LSB.

READ_CS14_R1 (DDh)

The READ_CS14_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS14 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS14_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS14_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS14_R1	Returns the ADC-sensed voltage on rail 1's CS14 pin. 3.125mV/LSB.

READ_CS15_R1 (DEh)

The READ_CS15_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS15 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS15_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS15_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS15_R1	Returns the ADC-sensed voltage on rail 1's CS15 pin. 3.125mV/LSB.

READ_CS16_R1 (DFh)

The READ_CS16_R1 command on Page 0 returns the ADC-sensed average voltage on rail 1's CS16 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS16_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS16_R1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS16_R1	Returns the ADC-sensed voltage on rail 1's CS16 pin. 3.125mV/LSB.

READ_ADDR (E4h)

The READ_ADDR command on Page 0 returns the actual PMBus address.

Command	READ_ADDR															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_ADDR							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that reads are always 0.
7:0	READ_ADDR	Returns the PMBus address.

READ_CONFIG_NUM (E5h)

The READ_CONFIG_NUM command on Page 0 returns the current working configuration number.

Command	READ_ADDR															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	X	X	X	X	READ_CONFIG_NUM			

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates that reads are always 0.
3:0	READ_CONFIG_NUM	Returns the current working configuration number (between 0 and 15).

PHASE_REDUNDANCY_NUM1 (E7h)

The PHASE_REDUNDANCY_NUM1 command on Page 0 reads the phase number if a phase redundancy fault occurs.

Command	PHASE_REDUNDANCY_NUM1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	PH16_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 16
14	PH15_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 15
13	PH14_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 14
12	PH13_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 13
11	PH12_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 12
10	PH11_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 11
9	PH10_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 10

8	PH9_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 9
7	PH8_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 8
6	PH7_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 7
5	PH6_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 6
4	PH5_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 5
3	PH4_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 4
2	PH3_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 3
1	PH2_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 2
0	PH1_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 1

PHASE_REDUNDANCY_NUM2 (E8h)

The PHASE_REDUNDANCY_NUM1 command on Page 0 reads the phase number if a phase redundancy fault occurs.

Command	PHASE_REDUNDANCY_NUM2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	X				

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3	PH20_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 20
2	PH19_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 19
1	PH18_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 18
0	PH17_FAULT	1’b0: No phase redundancy fault has occurred 1’b1: A phase redundancy fault has occurred on phase 17

MFR_PROTECTED_PH_R1 (E9h)

The MFR_PROTECTED_PH_R1 command on Page 0 forces the rail 1 active phase to stop working. The remaining phases interleave automatically.

Command	MFR_PROTECTED_PH_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	FORCE_PH16_SKIP_R1	Enables phase 16 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
14	FORCE_PH15_SKIP_R1	Enables phase 15 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
13	FORCE_PH14_SKIP_R1	Enables phase 14 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
12	FORCE_PH13_SKIP_R1	Enables phase 13 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
11	FORCE_PH12_SKIP_R1	Enables phase 12 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
10	FORCE_PH11_SKIP_R1	Enables phase 11 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
9	FORCE_PH10_SKIP_R1	Enables phase 10 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
8	FORCE_PH9_SKIP_R1	Enables phase 9 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
7	FORCE_PH8_SKIP_R1	Enables phase 8 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
6	FORCE_PH7_SKIP_R1	Enables phase 7 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
5	FORCE_PH6_SKIP_R1	Enables phase 6 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
4	FORCE_PH5_SKIP_R1	Enables phase 5 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled

3	FORCE_PH4_SKIP_R1	Enables phase 4 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
2	FORCE_PH3_SKIP_R1	Enables phase 3 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
1	FORCE_PH2_SKIP_R1	Enables phase 2 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
0	FORCE_PH1_SKIP_R1	Enables phase 1 to stop work, PWM signal become Hi-Z. The remaining rail 1 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled

MFR_PROTECTED_PH_R2 (EAh)

The MFR_PROTECTED_PH_R2 command on Page 0 forces the rail 2 active phase to protect. The remaining phases interleave automatically.

Command	MFR_PROTECTED_PH_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FORCE_PH8_SKIP_R2	Enables phase 8 to stop work, PWM signal become Hi-Z. The remaining rail 2 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
10	FORCE_PH7_SKIP_R2	Enables phase 7 to stop work, PWM signal become Hi-Z. The remaining rail 2 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
9	FORCE_PH6_SKIP_R2	Enables phase 6 to stop work, PWM signal become Hi-Z. The remaining rail 2 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
8	FORCE_PH5_SKIP_R2	Enables phase 5 to stop work, PWM signal become Hi-Z. The remaining rail 2 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
7	FORCE_PH4_SKIP_R2	Enables phase 4 to stop work, PWM signal become Hi-Z. The remaining rail 2 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
6	FORCE_PH3_SKIP_R2	Enables phase 3 to stop work, PWM signal become Hi-Z. The remaining rail 2

		phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
5	FORCE_PH2_SKIP_R2	Enables phase 2 to stop work, PWM signal become Hi-Z. The remaining rail 2 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
4	FORCE_PH1_SKIP_R2	Enables phase 1 to stop work, PWM signal become Hi-Z. The remaining rail 2 phases interleave automatically. This is for debugging mode. 1'b0: Disabled 1'b1: Enabled
3:0	RESERVED	Fixed to 0.

PAGE 1 REGISTER MAP

MFR_OPERATION_R2 (01h)

The MFR_OPERATION_R2 command on Page 1 turns the rail 2 output on and off in conjunction with the input from the EN pin, and sets V_{OUT} to the upper or lower margin voltages. The controller stays in the OPERATION command setting mode until a subsequent OPERATION command is received, or a change to EN sets rail 2 to another mode.

Command	MFR_OPERATION_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CUSTOMER_CODE_REV								OPERATION_R2							

Bits	Bit Name	Description
15:8	CUSTOMER_CODE_ REV	Set the customer code revision.
7:0	OPERATION_R2	Sets the operation mode for rail 2. 8’b 00xx xxxx: Hi-Z off 8’b 01xx xxxx: Soft-off 8’b 1000 xxxx: Normal on 8’b 1001 xxxx: Margin low 8’b 1010 xxxx: Margin high 8’b 1011 xxxx: AVSBus mode Others: Invalid commands “x” means not applicable.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page 1 clears any fault bits in the following registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), and STATUS_CML (7Eh).

This command is write-only. There is no data byte for this command.

MFR_VIN_UV_LIMIT (10h)

The MFR_VIN_UV_LIMIT command on Page 1 sets the V_{IN} UVP threshold and protection mode.

Command	MFR_TEMP_CALC															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VIN_UVP_MODE			VIN_UV_WARN						VIN_UVP						

Bits	Bit Name	Description
15:14	VIN_UVP_MODE	Sets the V_{IN} under-voltage protection (UVP) mode. 2’b00: No action 2’b01: Latch-off mode 2’b1x: Auto-retry mode
13:7	VIN_UV_WARN	Sets the V_{IN} under-voltage (UV) warning threshold. If V_{IN} drops below the set value, ALERT_P# is asserted with no mask. Write 0 to VIN_UV_WARN to disable this function. 125mV/LSB.

6:0	VIN_UVP	Sets the V_{IN} under-voltage protection (UVP) threshold. If V_{IN} drops below the set value, the system enters latch-off mode. 125mV/LSB.

MFR_TEMP_CALC (13h)

The MFR_TEMP_CAL command on Page 1 sets the temperature-sense gain and offset to convert the voltage on the TSENS1 pin to a direct temperature (in °C).

Command	MFR_TEMP_CALC															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_TEMP_GAIN								MFR_TEMP_OFFSET							

Bits	Bit Name	Description
15:8	MFR_TEMP_GAIN	Sets the temperature-sense gain to convert the voltage on the TSENS1 pin to direct temperature (in °C). The gain unit is °C/V, and can be calculated with the following equation: TEMP_GAIN = 1.6 x a Where *a* is the temperature-sense gain from Intelli-Phase™ applied on the TSENS1 pin (in °C/V). For example, for 8mV/°C on the TSENS1 pin, the TEMP_GAIN = 200 (0xC8).
7:0	MFR_TEMP_OFFSET	Sets the temperature-sense offset to convert the voltage on the TSENS1 pin to direct temperature (in °C). Bit[7] is the signed bit, and is in binary format. 1°C/LSB. For a +10°C offset, TEMP_OFFSET = 0x0A; for a -75°C offset, TEMP_OFFSET = 0xB5.

VOUT_COMMAND_R2 (21h)

The VOUT_COMMAND_R2 on Page 0 set the rail 2 V_{REF} VID in PMBus override mode.

Command	VOUT_COMMAND_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	0					X	VOUT_COMMAND_R2									

Bits	Bit Name	Description
15	MFR_VCAL_I_R2_BIT6	Fixed to 0.
14:11	MFR_FB_PI_R2	Fixed to 2.
10	RESERVED	Reserved.
9:0	VOUT_COMMAND_R2	Sets the rail 2 V_{REF} (VID_DAC V_{OUT}) in PMBus VID mode. 1 VID_STEP/LSB. VID_STEP is determined by MFR_VOUT_LOOP_CTRL (B2h), bits[15:14].

VOUT_TRIM_R2 (22h)

The VOUT_TRIM_R2 command on Page 1 applies a fixed offset voltage to the commanded rail 2 V_{OUT}. This value cannot be stored to the NVM, and can only be changed on the fly.

Command	VOUT_TRIM_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	VOUT_TRIM_R2						

Bits	Bit Name	Description
15:7	RESERVED	Reserved.
6:0	VOUT_TRIM_R2	Sets the V_{OUT} offset voltage on rail 2. This register does not have an NVM cell, which means it can only be changed on the fly. The NVM cannot modify this command. The default value is 0V. 1 VID_STEP/LSB. VID_STEP is determined via MFR_VOUT_LOOP_CTRL (B2h), bits[15:14].

VOUT_MAX_R2 (24h)

The VOUT_MAX_R2 command on Page 1 sets the maximum V_{REF} limitation on rail 2. VID + offset is limited to VOUT_MAX if the configured VID + offset exceeds VOUT_MAX. This command is effective in PMBus, AVSBus, and SVI2 modes.

Command	MFR_VOUT_MAX_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	0					X	VOUT_MAX_R2									

Bits	Bit Name	Description
15	MFR_VCAL_I_R2_BIT5	Fixed to 0.
14:11	MFR_CB_PI_R2	Fixed to 2.
10	RESERVED	Reserved.
9:0	VOUT_MAX_R2	Set the rail 2 maximum voltage in PMBus, AVSBus, and SVI2 mode. Any VID + offset exceeding this value is clamped to VOUT_MAX. 1 VID_STEP/LSB. VID_STEP is set by MFR_VOUT_LOOP_CTRL (B2h on Page 0), bits[15:14].

VOUT_MARGIN_HIGH_R2 (25h)

The VOUT_MARGIN_HIGH_R2 command on Page 1 cannot be stored to the NVM, and can only be changed on the fly. This command cannot be modified by the NVM. The default value is 0xB8B0, where 1 VID step is equal to 1.953125mV.

Command	VOUT_MARGIN_HIGH_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	1	0	1	1	1	X	VOUT_MARGIN_HIGH_R2									

Bits	Bit Name	Description
15:11	EXP	Fixed to 10111.
10	RESERVED	Reserved.
9:0	VOUT_MARGIN_HIGH_R2	This register cannot be saved to the NVM. It can only be changed on the fly. These bits reset to 0 after shutdown.

VOUT_MARGIN_LOW_R2 (26h)

The VOUT_MARGIN_LOW_R2 command on Page 1 cannot be stored to the NVM, and can only be changed on the fly. This command cannot be modified by the NVM. The default value is 0xB890, where 1 VID step is equal to 1.953125mV.

Command	VOUT_MARGIN_LOW_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	1	0	1	1	1	X	VOUT_MARGIN_LOW_R2									

Bits	Bit Name	Description
15:11	EXP	Fixed to 10111.
10	RESERVED	Reserved.
9:0	VOUT_MARGIN_LOW_R2	This register cannot be saved to the NVM. It can only be changed on the fly. These bits reset to 0 after shutdown.

MFR_VOUT_TRANSITION_RATE_R2 (27h)

The VOUT_TRANSITION_RATE_R2 command on Page 1 sets the rail 2 dynamic VID transition slew rate and EN soft shutdown slew rate in PMBus mode.

Command	MFR_VOUT_TRANSITION_RATE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X		VOUT_TRANSITION_RATE_R2												

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	MFR_OFF_SR_SEL_R2	Selects the source of TOFF_FALL_R2. This register does not have an NVM cell. 1: TOFF_FALL_R2 = VOUT_TRANSITION_RATE_R2 0: TOFF_FALL_R2 = TON_RISE_R2
12:0	VOUT_TRANSITION_ RATE_R2	Sets the rail 2 V_{OUT} slew rate during DVID. Use MFR_SR_RES (A1h on Page 0), bit[0] to set the resolution.

VOUT_DROOP_R2 (28h)

The VOUT_DROOP_R2 command on Page 1 sets the parameters for the rail 2 load line.

Command	VOUT_DROOP_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function											DROOP_SET_R2					

Bits	Bit Name	Description
15	MFR_DROOP_BW_SET_R2	Enables increasing the AC droop BW by increasing the bias current. It is for rail 2 only. 1'b0: Disabled 1'b1: Enabled
14		Enables increasing the AC droop BW by reducing the compensation capacitor. It is for rail 2 only. 1'b0: Disabled 1'b1: Enabled
13	IACDROOP_GAIN2_SET_R2	Sets the PMBus load-line slope for the Cdroop's second current mirror ratio. 1'b0: 1 1'b1: 1/2
12	MFR_ACLL_EN_R2	Selects the load line to be AC or DC. 1'b0: DC load line 1'b1: AC load line
11:9	IDROOP_GAIN2_R2	Set the PMBus load-line slope for the DC or AC droop's second current mirror ratio (GAIN2) for rail 2. 3'b000: 0 3'b001: 3/4 3'b010: 4/4 3'b011: 5/4 3'b100: 6/4 3'b101: 7/4 3'b110: 8/4 3'b111: 9/4
8:7	IDROOP_GAIN1_R2	Sets the I_{DROOP} first current mirror ratio (GAIN1) for rail 2. The initial load-line slope can be calculated with the following equation: $R_{LL\_INI} = R_{DROOP} \times GAIN1 \times GAIN2$ 2'b00: 1/16 2'b01: 1/8 2'b10: 1/4 2'b11: 1/2
6	SHORT_FIRST_HALF_R2	1'b0: Do not short first half resistors on rail 2 1'b1: Short the first half resistors on rail 2 Set this bit to 1 if R_{DROOP} is below 640Ω.
5:0	DROOP_SET_R2	Sets the rail 2 R_{DROOP}. 20Ω/LSB. 1.28kΩ maximum.

VOUT_MIN_R2 (2Bh)

The VOUT_MIN_R2 command on Page 1 instructs the device to limit the rail 2 minimum V_{OUT} in PMBus, AVSBus, and SVI2 modes. If the V_{OUT} value decoded from the PMBus interface drops below what is set by VOUT_MIN (2Bh), V_{OUT} is clamped to VOUT_MIN.

Command	VOUT_MIN_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_VCAL_I_R2_5LSB					X	VOUT_MIN_R2									

Bits	Bit Name	Description
15:11	MFR_VCAL_I_R2_5LSB	Fixed to 10.
10	RESERVED	Reserved.
9:0	VOUT_MIN_R2	Sets the minimum VID under PMBus, AVSBus, and SVI2 modes on rail 1. Any VID below this value is clamped to VOUT_MIN. 1 VID_STEP/LSB. VID_STEP is determined by MFR_VOUT_LOOP_CTRL (B2h), bits[15:14].

FREQUENCY_SWITCH_R2 (33h)

The FREQUENCY_SWITCH command on Page 1 sets the rail 2 f_{SW}. f_{SW} ranges between 200kHz and 5.11MHz, with 10kHz per step.

Command	FREQUENCY_SWITCH_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_CS_LOOP_TH_7LSB_R2							FREQUENCY_SWITCH_R2								

Bits	Bit Name	Description
15:9	MFR_CS_LOOP_TH_ 7LSB_R2	The 7LSB of MFR_CS_LOOP_TH_R2, which sets the threshold for the current imbalance function.
8:0	FREQUENCY_SWITCH_R2	Sets the switching frequency in direct format. 10kHz/LSB.

IOUT_OC_FAULT_LIMIT_R2 (46h)

The IOUT_OC_FAULT_LIMIT command on Page 1 sets the rail 2 I_{OUT} over-current (OC) fault threshold.

Command	IOUT_OC_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OCP_SPIKE_R2								OCP_TDC_R2							

Bits	Bit Name	Description
15:8	OCP_SPIKE_R2	Sets the rail 2 OCP_SPIKE_TOTAL current level DAC value. 6.25mV/LSB. The threshold can be calculated with the following equation: OCP_SPIKE_TOTAL = OCP_SPIKE x K_{CS} x G_{IMON} x R_{IMON} / 6.25
7:0	OCP_TDC_R2	Sets the rail 2 OCP_TDC_TOTAL current DAC value. 6.25mV/LSB. The threshold can be calculated with the following equation: OCP_TDC_TOTAL = OCP_TDC x K_{CS} x G_{IMON} x R_{IMON} / 6.25

IOUT_OC_FAULT_RESPONSE_R2 (47h)

The IOUT_OC_FAULT_RESPONSE command on Page 1 sets the rail 2 over-current protection (OCP) related options and values.

Command	IOUT_OC_FAULT_RESPONSE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				OCPTDC_ACTIONDELAY_R2					OCPTDC_TRIGDELAY_R2							

Bits	Bit Name	Description
15:14	OCP_MODE_R2	Selects the protection mode for both OCP_TDC and OCP_SPIKE. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 6 times(not recommend OCP_SPIKE to choose this Retry 6 times)
13	OCP_TDC_EN_R2	Enables over-current protection (OCP_TDC). 1'b0: Disabled 1'b1: Enabled
12:8	OCPTDC_ ACTIONDELAY_R2	Sets the OCP_TDC fault action time, which is the delay between when the OCP_L signal asserts and an action is taken (e.g. hiccup mode or shutdown). 1µs/LSB.
7:0	OCPTDC_TRIGDELAY_R2	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for the blanking time. 20µs/LSB.

MFR_PH_FAULT_SET_R2 (4Ah)

The MFR_PH_FAULT_SET command on Page 1 sets the current ripple detection related parameters.

Command	MFR_PH_FAULT_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						IOUT_OC_WARN_LIMIT_R2										

Bits	Bit Name	Description
15:14	MFR_PH_FAULT_TIME_2LSB	The 2LSB of MFR_PH_FAULT_TIME. MFR_PH_FAULT_TIME is used for phase current sense (V_{CS}) detection. If V_{CS} always exceeds OCP_PHASE or stays almost equal to V_{CS_REF} (no CS ripple) for the time set by MFR_PH_FAULT_TIME, then the fail is considered abnormal. If MFR_CR_DETECT_TIME_SEL, bit[0] = 1, then this register is 2µs/LSB. If MFR_CR_DETECT_TIME_SEL, bit[0] = 0, then this register is 20µs/LSB.
13:11	MFR_PH_FAULT_L_ SET	Sets the low threshold for detecting the phase current ripple fault comparator. 3'b000: V_{CS_REF} - 10mV 3'b001: V_{CS_REF} - 20mV 3'b010: V_{CS_REF} - 30mV 3'b011: V_{CS_REF} - 40mV 3'b100: V_{CS_REF} - 50mV 3'b101: V_{CS_REF} - 60mV 3'b110: V_{CS_REF} - 70mV 3'b111: V_{CS_REF} - 80mV
10:0	IOUT_OC_WARN_ LIMIT_R2	Sets the rail 2 OC_WARN threshold. If the READ_IOUT (8Ch) value exceeds the set threshold, an over-current (OC) warning occurs and the OC_WARN flag is asserted. This flag can be read from the PMBus status register or pulled to GPIO. B7h on Page 0, bit[7] = 1: 0.25A/LSB B7h on Page 0, bit[7] = 0: 0.5A/LSB

OT_FAULT_LIMIT_R2 (4Fh)

The OT_FAULT_LIMIT command on Page 1 sets the over-temperature protection (OTP) fault related operation and values of TSENS2. It is only effective when set the TEMP mode is set to individual mode.

Command	OT_FAULT_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		MFR_OTP_HYS_R2							MFR_OTP_LIMIT_R2							

Bits	Bit Name	Description
15	MFR_OTP_MODE_R2	Sets the over-temperature protection (OTP) mode. 1'b0: Latch-off mode 1'b1: Auto-retry mode
14:9	MFR_OTP_HYS_R2	Sets the temperature hysteresis for the OTP threshold. If the junction temperature monitored on the TSENS2 pin is below OTP_LIMIT-OTP_HYS, the PWM initiates soft start as it would during a normal start-up sequence. 1°C/LSB.
8	MFR_OTP_EN_R2	Enables over-temperature protection (OTP). 1'b0: Disabled 1'b1: Enabled
7:0	MFR_OTP_LIMIT_R2	VR over-temperature protection (OTP) fault limit setting. If the junction temperature monitored on the TSENS2 pin exceeds OTP_LIMIT, the VR shuts off the disabled output. 1°C/LSB.

OT_WARN_LIMIT_R2 (51h)

The OT_WARN_LIMIT command on Page 1 sets the VR_HOT temperature threshold, hysteresis, and TSENS2 mode. It is only effective when set the TEMP mode is set to individual mode.

Command	OT_WARN_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		VRHOT_HYS_R2							VRHOT_LIMIT_R2							

Bits	Bit Name	Description
15	CS_RIPPLE_ACTION _EN_R2	Enables removing the fault phase if the CS ripple detects phase redundancy. It is for rail 1 only. 1'b0: Disabled 1'b1: Enabled
14:9	VRHOT_HYS_R2	Sets the VR_HOT hysteresis. 1°C/LSB.
8	VRHOT_EN_R2	Enables VRHOT. 1'b0: Disabled 1'b1: Enabled
7:0	VRHOT_LIMIT_R2	Sets the over-temperature (OT) warning threshold. If the temperature sensed via TSENS1 pin exceeds this threshold, the VRHOT flag is asserted. 1°C/LSB.

MFR_VIN_UVLO (55h)

The MFR_VIN_UVLO command on Page 1 sets the V_{IN} under-voltage lockout (UVLO) rising and falling thresholds.

Command	MFR_VIN_UVLO															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VIN_ON								VIN_OFF							

Bits	Bit Name	Description
15:8	VIN_ON	Sets the V_{IN} under-voltage lockout (UVLO) rising threshold. 62.5mV/LSB.
7:0	VIN_OFF	Sets the V_{IN} under-voltage lockout (UVLO) falling threshold. 62.5mV/LSB.

TON_RISE_R2 (61h)

The TON_RISE_R2 command on Page 1 sets the rail 2 V_{REF} start-up slew rate.

Command	MFR_TON_RISE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_SLOWLOOP_TH				TON_RISE_R2											

Bits	Bit Name	Description
15:12	MFR_SLOWLOOP_TH	Fixed to 0.
11:0	TON_RISE_R2	Sets the rail 2 V_{OUT} start-up slew rate. Set the resolution via MFR_SR_RES (A1h on Page 0), bit[0].

STATUS_BYTE (78h)

The STATUS_BYTE command returns 1 byte of information with a summary of the most critical statuses and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								X

Bits	Bit Name	Behavior	Description
7	NVM_BUSY	Live	Reports the live status of the non-volatile memory (NVM). Can't be reset by send CLEAR_FAULTS(03h). 1'b0: the NVM is idle. The NVM write and read with PMBus command is available 1'b1: The NVM is busy. The NVM write and read with PMBus command is unavailable
6	OFF	Live	Indicates whether the rail 2 output is off. This bit is in live mode. It is asserted if the rail 2 output is off. VOUT2 turning off can be caused by protections, EN going low, or if VID = 0. 1'b0: VOUT2 is on 1'b1: VOUT2 is off

5	VOUT_OV_FAULT	Latch	Rail 2 V_{OUT} over-voltage (OV) fault indicator. If rail 2 OVP (absolute or VID) occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	Rail 2 I_{OUT} over-current (OC) fault indicator. If rail 2 OCP occurs (OCP_TDC and OCP_SPIKE), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
3	VIN_UV_FAULT	Latch	V_{IN} under-voltage (UV) fault indicator. If a V_{IN} UV fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	TEMPERATURE	Latch	Over-temperature (OT) fault and warning indicator. If TSENS2 OTP or an OT warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Latch	PMBus communication fault indicator. If a PMBus communications related fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	TSENS2_DIGI_FAULT	Latch	TSENS2 digital sense fault indicator. This function is enabled by MFR_TBD_FLT_EN (A8h on Page 1), bit[14] if the device is in temp merge mode, which set if B7h (on Page 0), bit[5] = 1. If the voltage on TSENS2 exceeds or drops below the value set by MFR_TSENS2_SET (A8h on Page 1), bits[13:8], then a TSENS2 fault occurs and this bit is set and latched. The TSENS2 fault direction is determined by MFR_TSENS2_SET (A8h on Page 1), bit[1]. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No TSENS2 digital sense fault has occurred 1'b1: A TSENS2 digital sense fault has occurred

STATUS_WORD (79h)

The STATUS_WORD (79h) command on Page 1 returns 2 bytes of information with a summary of the device's fault and warning conditions. The higher byte gives more detailed information on the fault conditions. The lower byte shares this information with the STATUS_BYTE (78h) register.

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function						X	X		STATUS_BYTE (78h)							

Bits	Bit Name	Behavior	Description
15	VOUT	Latch	Rail 2 V_{OUT} fault and warning indicator. If a V_{OUT} over-voltage (OV) or under-voltage (UV) protection or warning occurs, this bit is set. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} fault/warning has occurred 1'b1: A V_{OUT} fault/warning has occurred
14	IOUT	Latch	Rail 2 I_{OUT} fault and warning indicator. If an I_{OUT} fault or warning occurs, this bit is set. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} fault and warning has occurred 1'b1: An I_{OUT} fault or warning has occurred
13	INPUT	Latch	Input voltage, current, and power fault/warning indicator. If any protection or warning related to V_{IN}, I_{IN}, or P_{IN} occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No input fault or warning has occurred 1'b1: An input fault or warning has occurred
12	TSENS2	Latch	TSENS2 fault indicator. Once the TSENS1 fault function has been enabled, set MFR_TSNS1_FLT_EN (A8h on Page 1), bit[15] = 1. If the TSENS2 voltage exceeds 2.2V (set by A8h on Page 1, bits[13:8), then a TSENS2 fault occurs and this bit is set and latched. Reset this bit by cycling the power on VDD33. 1'b0: No TSENS2 fault has occurred 1'b1: A TSENS2 fault has occurred
11	PG_NOT_ACTIVE	Live	1'b0: PG is active 1'b1: PG is not active
10:9	RESERVED	N/A	Unused. X indicates that reads are always 0.
8	WATCH_DOG_OVF	Latch	Monitor block timer overflow watchdog indicator. The monitor value calculation has a watchdog timer. If the timer overflows, the calculated monitor value and the timer will be reset. Meanwhile, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed This bit also indicates phase redundancy. If either of this scenarios occur, this bit is set and latched. Phase redundancy indication cannot be reset by issuing a CLEAR_FAULTS (03h) command. 1'b0: No phase redundancy fault has occurred 1'b1: A phase redundancy fault has occurred

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 1 returns 1 byte of information with the detailed V_{OUT} fault and warning statuses for rail 2.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X			X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Rail 2 V_{OUT} over-voltage (OV) fault indicator. If output OVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} OV fault has occurred 1'b1: A V_{OUT} OV fault has occurred
6:5	RESERVED	N/A	Unused. X indicates that reads are always 0.
4	VOUT_UV_FAULT	Latch	Rail 2 V_{OUT} under-voltage (UV) fault indicator. If rail 1 UVP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{OUT} UV fault has occurred 1'b1: A V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN_ WARNING	Latch	Rail 2 V_{OUT} has reached VOUT_MAX or VOUT_MIN indicator. If the VID value exceeds VOUT_MAX (24h on Page 0) or is below VOUT_MIN (2Bh Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID exceeds VOUT_MAX or is below VOUT_MIN
2	RESERVED	N/A	Unused. X indicates that reads are always 0.
1	LINE_FLOAT	Latch	Rail 2 line-float protection indicator. If a line float fault is detected, the device shuts down the associated rail, and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No line float fault has occurred 1'b1: A line float fault has occurred
0	RESERVED	N/A	Unused. X indicates that reads are always 0.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 1 returns 1 byte of information with the detailed I_{OUT} fault and warning statuses for rail 2.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function				X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Rail 2 output over-current (OC) fault indicator (OCP_TDC and OCP_SPIKE). If output OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6	OCP_UV_FAULT	Latch	Rail 2 output over-current (OC) and under-voltage (UV) dual faults indicator. If output OCP occurs and the UV comparator is set simultaneously, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OC and UV fault has occurred 1'b1: An output OC fault has occurred, and the UV comparator is set

5	IOUT_OC_WARN	Latch	Rail 2 output over-current (OC) warning indicator. If an output OC warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OC warning has occurred 1'b1: An output OC warning has occurred
4:0	RESERVED	N/A	Unused. X indicates that reads are always 0.

STATUS_INPUT (7Ch)

The STATUS_INPUT command on Page 1 returns 1 byte of information with detailed input fault and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	VIN_OVP	X		VIN_UVP		X	X	X

Bits	Bit Name	Behavior	Description
7	VIN_OVP	Latch	V_{IN} over-voltage (OV) fault indicator. If V_{IN} exceeds the VIN_OV fault limit, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6	RESERVED	N/A	Unused. X indicates that reads are always 0.
5	VIN_UV_WARNING	Live	V_{IN} under-voltage (UV) warning indicator. If the sensed V_{IN} drops below the threshold set by VIN_UV_LIMIT (10h on Page 1), bits[13:7], this bit is set. This bit is reset once V_{IN} exceeds VIN_UV_LIMIT. 1'b0: No V_{IN} UV warning has occurred 1'b1: A V_{IN} UV warning has occurred
4	VIN_UVP	Latch	V_{IN} under-voltage (UV) fault indicator. If the sensed V_{IN} drops below the value set by VIN_UV_LIMIT (10h on Page 1), bits[6:0], this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
3	VIN_UVLO_LIVE	Live	V_{IN} under-voltage lockout (UVLO) live indicator. If V_{IN} drops below VIN_OFF, this bit is set. This bit rests once V_{IN} exceeds VIN_ON. 1'b0: V_{IN} has exceeded VIN_ON (55h on Page 1), bits[15:8] 1'b1: V_{IN} is below VIN_OFF (55h on Page 1), bits[7:0]
2:0	RESERVED	N/A	Unused. X indicates that reads are always 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command on Page 1 returns 1 byte of information with temperature-related fault and warning conditions.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		VRHOT	X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Over-temperature (OT) fault indicator. If the sensed TSENS1 temperature exceeds the OT fault limit set by OT_FAULT_LIMIT (4Fh on Page 0), bits[7:0], this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
6	VRHOT	Live	VRHOT indicator. If the sensed TSENS1 temperature exceeds the VRHOT limit set by MFR_VRHOT_SET (51h on Page 1), bits[7:0], this bit is set. This bit is reset once the TSENS1 temperature falls below this limit. 1'b0: No VRHOT fault has occurred 1'b1: A VRHOT fault has occurred
5:0	RESERVED	N/A	Unused. X indicates that reads are always 0.

STATUS_CML (7Eh)

The STATUS_CML command on Page 1 returns 1 byte of information with PMBus communication-related faults.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function					X			

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	Invalid PMBus command indicator. If the MP2882 receives and unsupported command code, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	INVALID_DATA	Latch	Invalid PMBus data indicator. If the MP2882 receives unsupported data, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received
5	PEC_ERROR	Latch	PMBus PEC fault indicator. The PMBus interface supports the use of the packet error checking (PEC) byte that is defined in the SMBus standard. The PEC byte is transmitted by the MP2882 during a read transaction, or sent to the MP2882 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed and PEC_FAULT is set and latched. Send a CLEAR_FAULTS (03h) to reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected

4	NVM_CRC_ERROR	Latch	CRC fault indicator. When storing the operating memory data into the NVM, the MP2882 calculates a CRC code for each bit, and saves the final CRC code to the NVM. When restoring the NVM data to the operating memory, the MP2882 recalculates the CRC code with each bit. The MP2882 checks the CRC results when the restoration process is complete. If the CRC result does not match what was stored , the VR shuts down, and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
3	RESERVED	N/A	Unused. X indicates that reads are always 0.
2	CML_FLT_TRG	Latch	If a NVM operation is blocked because the controller is recording a fault to the NVM, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: NVM operation is not blocked 1'b1: NVM operation has been blocked because the controller is recording a fault to the NVM
1	CML_OTHER_FAULTS	Latch	If any of the communication faults listed below occur, this bit is set and latched: 1) Sending too few bits 2) Reading too few bits 3) Host sends or reads too few bytes 4) Reading too many bytes Send a CLEAR_FAULTS (03h) command to reset this bit.
0	NVM_SIG_FAULTS	Latch	When restoring data from the NVM to the operating memory, the device first checks the signature register in address 00h of the NVM. If the signature register is 0x1234, the restoration process is halted immediately, and this bit is set and latched. Send a CLEAR_FAULTS (03h) to reset this bit. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

READ_TSENS1_SENSE (83h)

The READ_TSENS1_SENSE command on page1 returns the ADC-sensed TSENS1 voltage.

Command	READ_TSENS1_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_TSENS1									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_TSENS1	Returns the ADC-sensed voltage on rail 1's TSENS1 pin in direct format. 1.5625mV/LSB.

READ_IMON2 (84h)

The READ_IMON2 command on Page 1 returns the ADC-sensed VIMON2 voltage.

Command	READ_IMON2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_IMON2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_IMON2	Returns the ADC-sensed voltage on rail 1's VIMON2 pin in direct format. 1.5625mV/LSB.

READ_VDIFF2_SENSE (85h)

The READ_VDIFF2_SENSE command on Page 1 returns the ADC-sensed VDIFF2 voltage.

Command	READ_VDIFF2_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_VDIFF2_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_VDIFF2_SENSE	Returns the ADC-sensed VDIFF2 voltage in direct format. 1 VID_STEP/LSB. VID_STEP is determined by B2h (on Page 1), bits[15:14].

READ_VFB2_SENSE (86h)

The READ_VFB2_SENSE command on Page 1 returns the ADC-sensed VFB2 voltage.

Command	READ_VFB2_SENSE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_VFB2_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_VFB2_SENSE	Returns the ADC-sensed VFB2 voltage in direct format when B2h (on Page 1), bit[9] = 0. 1 VID_STEP/LSB. VID_STEP is determined by B2h (on Page 1), bits[15:14].

READ_VIN (88h)

The READ_VIN command on Page 1 provides 2 bytes to return the sensed V_{IN} based on the VINSEN pin in Linear11 format. In VID mode, the returned value ignores bits[15:11] (the exponent value).

Command	READ_VIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	1	1	0	1	1	0	READ_VIN									

Bits	Bit Name	Description
15:11	EXP	Fixed to 11011.
10	RESERVED	Fixed to 0.
9:0	READ_VIN	Returns the sensed V_{IN} in Linear11 format. 31.25mV/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 1 returns the sensed rail 2 VOSEN - VORTN voltage.

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	READ_VOUT										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that reads are always 0.
10:0	READ_VOUT	Returns the rail 2 V_{OUT}, calculated with the following equation: V_{OUT} = READ_VOUT (8Bh) x VID_STEP Where VID_STEP is determined by B2h (on Page 0), bits[15:14].

READ_IOUT (8Ch)

The READ_IOUT command on Page 1 returns the sensed rail 2 I_{OUT} in direct format.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	EXP					READ_IOUT										

Bits	Bit Name	Description
15:11	EXP	This is determined by MFR_VR_CONFIG1 (B7h on Page 0), bit[7]. B7h, bit[7] = 0: 5'b11111 B7h, bit[7] = 1: 5'b11110
10:0	READ_IOUT	Returns the sensed rail 2 I_{OUT}. The resolution is determined by MFR_VR_CONFIG1 (B7h on Page 0), bit[7]. B7h, bit[7] = 0: 0.5A/LSB B7h, bit[7] = 1: 0.25A/LSB

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 1 returns the temperature sensed on the TSENS2 pin in direct format.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	X	X	X	READ_TEMP							

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.

10:8	RESERVED	Unused. X indicates that reads are always 0.
7:0	READ_TEMP	Returns the sensed temperature on the TSENS2 pin. 1°C/LSB.

READ_VBOOT2 (91h)

The READ_VBOOT2 command on Page 1 returns the selected VBOOT2 number.

Command	READ_VBOOT2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function				VBOOT2					X	X	X	X	X	X	X	X

Bits	Bit Name	Description
15:13	RESERVED	Always returns 0.
12:8	VBOOT2	Always return the selected VBOOT2 number, which is between 0 and 31.
7:0	RESERVED	Reserved.

READ_POUT (96h)

The READ_POUT command on Page 1 returns the rail 2 P_{OUT} value.

Command	READ_POUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_POUT															

Bits	Bit Name	Description
15:0	READ_POUT	Returns P_{OUT}. Convert the read value to the actual power (in Watts) using MFR_VR_CONFIG (B7h), bit[6], and the equations below: B7h, bit[6] = 1: $P_{OUT}(W) = \frac{READ\_POUT}{8}$ B7h, bit[6] = 0: $P_{OUT}(W) = \frac{READ\_POUT}{4}$

MFR_APS_OPTI_R2 (9Fh)

The MFR_APS_OPTI_R2 command on Page 1 sets rail 2 automatic phase-shedding (APS) related timing and behaviors.

Command	MFR_APS_OPTI_R2															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TON_DELAY_R2							APS_COMP_CNT					APS_COMP_LEVEL			

Bits	Bit Name	Description
15:11	TON_DELAY_R2	100µs/LSB.
10	MFR_AVS_IOUT_RES2	Sets the AVSBus I_{OUT} report resolution. 1'b0: 10mA/LSB 1'b1: 20mA/LSB

9	MFR_APS_OPTI_R2	Enables V_{REF} compensation when exiting decay mode. The compensation voltage level and slew rate is the same as it is with auto phase-shedding (APS) compensation. 1'b0: Disabled 1'b1: Enabled
8:4	APS_COMP_CNT	The MP2882 provides positive compensation on V_{REF} during phase-shedding to reduce undershoot. V_{REF} compensation is implemented by adding a PMBus-configurable positive voltage on the COMP of the DC loop. After phase-shedding starts, the voltage returns to 0V step by step with a time interval. APS_COMP_CNT sets the time interval between each step. 50ns/LSB.
3:0	APS_COMP_LEVEL	Sets the V_{REF} compensation level during phase-shedding to reduce undershoot. The compensation is added to V_{REF} when phase-shedding occurs. 1.37mV/LSB.

MFR_TIMEOUT (A0h)

MFR_TIMEOUT command on Page 1 set the timeout-related parameters in PMBus mode and AVSBus mode.

Command	MFR_TIMEOUT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				MFR_PMBUS_TIMEOUT2_DATA												

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	MFR_PMBUS_ TIMEOUT2_EN	Enables AVSBus pack-to-pack timeout protection. 1'b0: Disabled 1'b1: Enabled
13	MFR_PMBUS_ TIMEOUT2_SEL	Sets the target data resolution for the AVSBus pack-to-pack timeout protection counter. 1'b0: 100µs x 128 1'b1: 200ns x 128
12:6	MFR_PMBUS_ TIMEOUT2_DATA	Target data for the AVSBus pack-to-pack timeout protection counter.
5	MFR_PMBUS_FILTER_ EN	Enables the PMBus digital degiltch filter. 1'b0: Disabled 1'b1: Enabled
4	MFR_SDA_DELAY_EN	Enables the PMBus SDA delay. 1'b0: SCL and SDA have the same delay inside the IC 1'b1: SDA has a delay that is longer than SCL by 50ns inside the IC
3:0	MFR_PMBUS_TIMEOUT	Sets the PMBus timeout time, calculated with the following equation: PMBUS_TIMEOUT x 1.6ms + 1.5ms

MFR_VR_CONFIG4 (A1h)

The MFR_VR_CONFIG4 command on Page 1 sets some basic functions for the MP2882.

Command	MFR_VR_CONFIG4															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		0	0	ZCD_TRIM_R2			ZCD_TRIM_R1			ADC_HOLD_TIME						

Bits	Bit Name	Description
15	MFR_PWM_TRI_MODE	Set the tri-state voltage level. 1'b0: Hi-Z 1'b1: Middle voltage
14	RVP_SET_R2	Fixed to 0.
13	RVP_SET_R1	Fixed to 0.
12:10	ZCD_TRIM_R2	Fine-tunes the rail 2 zero-current detection (ZCD) threshold. Only PWM16 has ZCD. If phase 1 of rail 2 changes from PWM16 to another PWM, there is no ZCD function. 3'b000: -10mV 3'b001: -5mV 3'b010: 0mV 3'b011: +5mV 3'b100: +10mV 3'b101: +15mV 3'b110: +20mV 3'b111: +25mV
9:7	ZCD_TRIM_R1	Fine-tunes the rail 1 ZCD threshold. Only PWM1 has ZCD. If phase 1 of rail 1 changes from PWM1 to another PWM, there is no ZCD function. 3'b000: -10mV 3'b001: -5mV 3'b010: 0mV 3'b011: +5mV 3'b100: +10mV 3'b101: +15mV 3'b110: +20mV 3'b111: +25mV
6:0	ADC_HOLD_TIME	Sets the ADC hold time. 50ns/LSB.

MFR_VR_CONFIG5 (A2h)

The MFR_VR_CONFIG5 command on Page 1 sets some basic functions for the MP2882.

Command	MFR_VR_CONFIG5															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	MFR_PAGE_EN	Enables the device to follow the WRITE_PROTECT (10h) register. 1'b0: Disabled 1'b1: Enabled

14	MFR_BYTEWR_DEBUG	Fixed to 0
13	MFR_BYTEWR_ DEBUG2	Fixed to 0
12:11	MFR_VID_FIL_SEL_R2	Selects the filter for the VID-DAC on rail 2 while VID is ramping down. 2'b00: 2.35µs filter 2'b01: 4.7µs filter 2'b10: 7.05µs filter 2'b11: 9.4µs filter
10	MFR_VID_FIL_EN_R2	Enables the VID-DAC filter for rail 2 when DVID goes down to avoid V_{OUT} undershoot. 1'b0: Disabled 1'b1: Enabled
9:8	MFR_VID_FIL_SEL_R1	Selects the filter rail 1 VID-DAC filter while VID ramps down. 2'b00: 2.35µs filter 2'b01: 4.7µs filter 2'b10: 7.05µs filter 2'b11: 9.4µs filter
7	MFR_VID_FIL_EN_R1	Enables the rail 1 VID-DAC filter when DVID goes down to avoid V_{OUT} undershoot. 1'b0: Disabled 1'b1: Enabled
6	MFR_UCP_DBG	Fixed to 0.
5:3	MFR_VID_DATA_ UPDATE_R2	Fixed to 0.
2:0	MFR_VID_DATA_ UPDATE_R1	Fixed to 0.

MFR_NVM_CTRL (A4h)

The MFR_NVM_CTRL command on Page 1 sets the NVM-related parameters for the MP2882.

Command	MFR_NVM_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	0		X	X	X	X	1									

Bits	Bit Name	Description
15	PMBUS_ TIMEOUT_MASK	Fixed to 0.
14	TSENS2_ DIGITAL_MASK	1'b0: If a TSENS2 digital fault occurs, ALT_P# does not assert 1'b1: No mask
13:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	FAULT_RECORD_ MODE	Fixed to 1.
8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7	TESTMODE_WRITE_EN	Enables writing EN in test mode. 1'b0: Disabled 1'b1: Enabled. Can write to Page 2
6	MFR_HIGHBITS_MASK	Enables masking registers 21h, 24h, 2Bh on Page 0 and Page 1.

		1’b0: 21h, 24h, and 2Bh bits[15:11] are masked 1’b1: No mask
5	MFR_BYTE_WORD	Fixed to 0.
4	OPERATION_ALL_ CALL_EN	Enables the on/off controls for both rails. 1’b0: Disabled 1’b1: Enabled
3	MFR_EEPROM_COPY_ EN	Fixed to 0.
2	MFR_STORE_ALL_EN	Fixed to 0.
1	MFR_FAULT_SAVE_EN	Enables the fault type to be saved the NVM. 1’b0: Disabled 1’b1: Enabled
0	MFR_CRC_ERROR_EN	Enables CRC fault protection to shut down the VR. 1’b0: Disabled 1’b1: Enabled

MFR_OV_UV_LIMIT_R2 (A5h)

The MFR_OV_UV_LIMIT command on Page 1 sets rail 2 V_{OUT} under-voltage protection (UVP) and over-voltage protection (OVP) thresholds.

Command	MFR_OV_UV_LIMIT_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X		UVP_VID_R2			OVP_VID_R2			OVP_ABS_R2							

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	OVUV_DIV2_EN	Enables the 1/2 divider for the V_{OUT} VID_OVP and VID_UVP thresholds on rail 2. 1’b0: Disabled 1’b1: Enabled
13:11	UVP_VID_R2	Sets the VID under-voltage protection (UVP) threshold. 3’b000: V_{REF} - 425mV 3’b001: V_{REF} - 375 mV 3’b010: V_{REF} - 325mV 3’b011: V_{REF} - 275mV 3’b100: V_{REF} - 225mV 3’b101: V_{REF} - 175mV 3’b110: V_{REF} - 125mV 3’b111: V_{REF} - 75mV

10:8	OVP_VID_R2	Sets the VID over-voltage protection (OVP) threshold. 3'b001: V_{REF} + 200mV 3'b010: V_{REF} + 325mV 3'b100: V_{REF} + 450mV All other values are invalid.
7:0	OVP_ABS_R2	Sets an absolute OVP threshold. OVP occurs if V_{OUT} exceeds this value. 10mV/LSB. Set OVP_ABS_R2 to 0 to disable this function.

MFR_OV_UV_RESPONSE_R2 (A6h)

The MFR_OV_UV_RESPONSE command on Page 1 sets rail 2 V_{OUT} under-voltage protection (UVP) and over-voltage protection (OVP) fault modes.

Command	MFR_OV_UV_RESPONSE_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			MFR_UVP_DELAYTIME_R2								MFR_OVP_VID_DELAYTIME_R2					

Bits	Bit Name	Description
15:14	MFR_UVP_MODE_R2	Sets the under-voltage (UV) fault mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 3 times
13:8	MFR_UVP_DELAYTIME_R2	Sets the V_{OUT} under-voltage protection (UVP) blanking time. UVP occurs if the sensed V_{DIFF} drops below the UVP threshold for the UVP blanking time. 20µs/LSB.
7:6	MFR_OVP_VID_MODE_R2	Sets the over-voltage (OV) fault mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Invalid mode 2'b11: Retry 3 times
5:0	MFR_OVP_VID_DELAYTIME_R2	Sets the OVP_VID blanking time. If the OVP_VID condition lasts for longer than the OVP_VID blanking time, a OVP_VID fault occurs. 100ns/LSB.

MFR_FAST_OCP_SET_R2 (A7h)

The MFR_FAST_OCP_SET command on Page 1 sets rail 2 per-phase over-current protection (OCP) threshold.

Command	MFR_FAST_OCP_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OCP_PHASE_R2															

Bits	Bit Name	Description
15:8	OCP_PHASE_R2	Sets the per-phase valley current limit DAC value. 5mV/LSB.
7:4	OCPSPIKE_ACTIONDELAY_R2	Sets the OCP_SPIKE fault action time. The time delay is between when the OCP_L signal asserts and the action occurs (current limiting, hiccup mode, entry, or shutdown). 1µs/LSB.

3:0	OCPSPIKE_ TRIGDELAY_R2	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for an OCP_SPIKE blanking time. 200ns/LSB.

MFR_TSNS2_SET (A8h)

The MFR_TSNS2_SET command on Page 1 sets some TSENS2 digital fault configurations.

Command	MFR_TSNS2_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			TSNS2_DAC_SET							MFR_TSNS2_DELAY_TIME						

Bits	Bit Name	Description
15	MFR_TSNS1_FLT_EN	Enables the TSENS1 fault pin for DrMOS fault type indication and fault type recording to the EEPROM. The MP2882 monitors the voltage level on the TSENS1 pin. If the TSENS1 voltage exceeds 2.2V, a DrMOS fault has occurred. 1'b0: Disable TSENS1 fault protection 1'b1: Enable TSENS1 fault protection
14	MFR_TBD_FLT_EN	In temperature merge mode (set by B7h on Page 0, bit[5] = 1), the device can enable a TSENS2 digital sense fault to shut down all rails. The MP2882 senses the voltage on the TSENS2 pin with the internal ADC. If the voltage exceeds or falls below the value set by MFR_TSENS2_SET (A8h on Page 1), bits[13:8], a TSENS2 fault occurs, and all rails shut down immediately. The TSENS2 sense fault direction is determined by MFR_TSENS2_SET (A8h on Page 1), bit[1]. 1'b0: Disable TSENS2 digital sense fault protection 1'b1: Enable TSENS2 digital sense fault protection
13:8	TSNS2_DAC_SET	Sets the TSENS2 digital fault threshold. 40mV/LSB.
7	MFR_TSNS2_FLT_EN	In temperature individual mode (set by B7h on Page 0, bit[5] = 0), enables the TSENS2 fault pin for DrMOS fault type indication and fault type recording to the EEPROM. The MP2882 monitors the voltage level on the TSENS2 pin. If the TSENS2 voltage exceeds 2.2V, a DrMOS fault has occurred. 1'b0: Disable TSENS2 fault protection 1'b1: Enable TSENS2 fault protection
6:2	MFR_TSNS2_DELAY_ TIME	Sets the delay time for TSENS2_DGTL_FAULT. 100ns/LSB.
1	MFR_TSNS2_FLT_DIR	Selects the TSENS2 digital fault direction. 1'b0: TSENS2 digital fault is triggered when the TSENS2 voltage exceeds the threshold set by bits[13:8] of this command 1'b1: TSENS2 digital fault is triggered when TSENS2 voltage falls below the threshold set by bits[13:8] of this command
0	MFR_TSNS2_FLT_ MODE	Select the TSENS2 digital fault action mode. 1'b0: Auto-retry mode 1'b1: Latch-off mode

MFR_PRT_CONFIG (A9h)

The MFR_PRT_CONFIG command on Page 1 sets the CR redundancy related parameters.

Command	MFR_PRT_CONFIG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	MFR_CR_DETECT_ TIME_SEL_L	Sets the resolution for the low average level detection. 1'b0: 20µs/LSB 1'b1: 2µs/LSB
14	MFR_CR_DETECT_ TIME_SEL_H	Sets the resolution for the high average level and CS ripple detection. 1'b0: 20µs/LSB 1'b1: 2µs/LSB
13	MFR_CR_DETECT_EN_ R2	Enables rail 2 phase current ripple detection.
12	MFR_CR_DETECT_EN_ R1	Enables rail 1 phase current ripple detection.
11:10	MFR_CR_FAULT_NUM_ R2	Sets the rail 2 redundant phase number. The maximum value is 2. The redundant phase number must be below the rail 2 phase number.
9:8	MFR_CR_FAULT_NUM_ R1	Sets the rail 1 redundant phase number. The maximum value is 2. The redundant phase number must be below the rail 1 phase number.
7:6	MFR_CR_DETECT_ MODE	Sets the CS redundant detection mode. 2'b00: Enable CS ripple detection and high/low average detection 2'b01: Enable CS ripple detection and high average detection 2'b10: Only enable CS ripple detection. High/low average detection is disabled 2'b11: Enable low average detection
5	MFR_DRMOS_PWM_ FLT_EN_R2	Enables both the DrMOS fault type indication function and fault record to the NVM function. It is for rail 2 only. For some Intelli-Phase™ devices, the PWM can report the DrMOS fault type. When this function is enabled, the MP2882 monitors the PWM voltage to detect faults after the VR shuts down. 1'b0: Disabled 1'b1: Enabled
4	MFR_DRMOS_PWM_ FLT_EN_R1	Enables both the DrMOS fault type indication function and fault record to the NVM function. It is for rail 1 only. For some Intelli-Phase™ devices, the PWM can report the DrMOS fault type. When this function is enabled, the MP2882 monitors the voltage on the PWM pin to detect the fault type after the VR shuts down. 1'b0: Disabled 1'b1: Enabled
3	MFR_VIN_OVP_MODE	Set the V_{IN} over-voltage protection (OVP) mode. 1'b0: Auto-retry mode 1'b1: Latch-off mode
2:1	HICCUP_TIME	Sets the hiccup time in auto-retry mode if a protection occurs. 2'b00: 12.5ms 2'b01: 6ms 2'b10: 2ms 2'b11: 0.5ms

0	MFR_PROTECT_BOTH_SHUTDOWN	Enables both rails to shut down if a protection occurs. 1b'0: Disabled 1b'1: Enabled

MFR_VOUT_CALC_R2 (AAh)

The MFR_VOUT_CALC command on Page 1 sets the V_{OUT} calculation gain and offset.

Command	MFR_VOUT_CALC_R2															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	MFR_VOUT_CALC_OS_R2						MFR_VOUT_CALC_GAIN_R2							

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:8	MFR_VOUT_CALC_OS_R2	Adds an offset to the V_{OUT} report in register READ_VOUT (8Bh). This bit is for the rail 1 V_{OUT} report only. This bit is in two's complement format. Bit[13] is the signed bit. 1 VID_STEP/LSB. If the VID_STEP is 6.25mV, the voltage list below shows the direct and real-world values: 6'b00 0000: 0mV 6'b00 0001: +6.25mV 6'b01 1111: +193.75mV 6'b10 0000: -200mV 6'b10 0001: -193.75mV 6'b11 1111: -6.25mV
7:0	MFR_VOUT_CALC_GAIN_R2	Sets the gain from the ADC-sensed VOSEN - VORTN voltage to the V_{OUT} report in register READ_VOUT (8Bh). It is for rail 1 only. READ_VOUT can be calculated with the following equation: $READ\_VOUT = \frac{1023 \times V_{OUT} \times VDIFF\_GAIN}{1.6} \times \frac{GAIN}{2^7} + OFFSET$ Where VDIFF_GAIN is determined by B2h (on Page 1), bits[11:10].

MFR_IOUT_GAIN_PMBUS_R2 (ABh)

The MFR_IOUT_GAIN_PMBUS command on Page 1 sets the PMBus I_{OUT} report gain. The MP2882 senses I_{OUT} by sensing the voltage on IMON. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch on Page 0).

Command	MFR_IOUT_GAIN_PMBUS_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					GAIN_SEL		GAIN									

Bits	Bit Name	Description
15:13	MFR_IMON_RES_SET_R2	Sets the rail 2 IMON resistor. 3'b 000: 2.5kΩ 3'b 001: 5kΩ 3'b 010: 10kΩ 3'b 011: 40kΩ 3'b 1xx: Disconnected
12	MFR_IMON_GAIN_SET_R2	1'b0: The IMON1 current mirror gain is 1/8 1'b1: The IMON2 current mirror gain is 1/16

11:10	GAIN_SEL	Sets the exponent value for the IOUT_CAL_GAIN calculation equation in bits[9:0] of this command.
9:0	GAIN	Sets the PMBus report current-sense gain. The gain can be calculated with the following equation: $IOUT\_CAL\_GAIN=\frac{1024}{1.6}\times K_{CS}\times G_{IMON}\times R_{IMON}\times 2^{(6-GAIN\_SEL)}$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, R_{IMON} is the internal IMON resistor (in Ω), and GAIN_SEL is bits[11:10] of this command.

MFR_IOUT_OS_PMBUS_R2 (ACh)

The MFR_IOUT_OS_PMBUS_R2 command on Page 1 sets the rail 2 I_{OUT} PMBus report offset. The offset is for I_{OUT} over-reporting or under-reporting. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch on Page 0).

Command	MFR_IOUT_OS_PMBUS_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				MFR_IOUT_CALC_PH_OFS_R2							MFR_IOUT_CALC_OFFSET_R2					

Bits	Bit Name	Description
15:13	MFR_CS_LOOP_TH_3MSB_R2	The 3MSB of MFR_CS_LOOP_TH_R2. MFR_CS_LOOP_TH_R2 is used to set the current imbalance threshold for rail 2. If the current balance loop tune value exceeds this threshold, the related phase will be treat as problem phase.
12:6	MFR_IOUT_CALC_PH_OFS_R2	Adds an offset according the phase number. A larger N results in a larger offset. Bit[12] is the signed bit.
5:0	MFR_IOUT_CALC_OFFSET_R2	Adds a current report offset to READ_IOUT (8Ch).

MFR_IOUT_CAL_AVSBUS_R2 (ADh)

The MFR_IOUT_CAL_AVSBUS_R2 command on Page 1 sets the rail 2 I_{OUT} AVSBus report offset and gain.

Command	MFR_IOUT_CAL_AVSBUS_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IOUT_AVS_OFFSET_R2					IOUT_AVS_GAIN_R2										

Bits	Bit Name	Description
15:11	IOUT_AVS_OFFSET_R2	Sets the rail 2 AVSBus mode current report resolution, which is determined by 9Fh (on Page 0), bit[10]. 9Fh, bit[10] = 0: 160mA/LSB 9Fh, bit[10] = 1: 320mA/LSB Bit[15] is the signed bit.

10:0	IOUT_AVS_GAIN_R2	Sets the rail 2 I_{OUT} telemetry report in AVSBus mode. 10mA/LSB. 9Fh, bit[10] = 0: $AVS\_GAIN = \frac{1.6 \times 32 \times 10\text{^}5}{1024 \times K_{CS} \times G_{IMON} \times R_{IMON}}$ 9Fh, bit[10] = 1: $AVS\_GAIN = \frac{1.6 \times 16 \times 10\text{^}5}{1024 \times K_{CS} \times G_{IMON} \times R_{IMON}}$ Where K_{CS} is the Intelli-Phase™ current-sense gain (in A/A), G_{IMON} is the IMON current mirror gain, and R_{IMON} is the IMON resistor (in Ω).

MFR_APS_ITH_SET_R2 (AEh)

The MFR_APS_ITH_SET command on Page 1 sets the rail 2 automatic phase-shedding (APS) level and hysteresis level.

Command	MFR_APS_ITH_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function							MFR_APS_IIL_INC_R2									

Bits	Bit Name	Description
15:14	MFR_APS_HYS_INC_R2	MFR_APS_HYS_R2 = PHASE_NUM_ACTIVE x MFR_APS_HYS_INC_R2 + MFR_APS_HYS_BASE_R2. 1A/LSB
13:10	MFR_APS_HYS_BASE_R2	Sets the basic automatic phase-shedding (APS) hysteresis level. 1A/LSB
9:4	MFR_APS_IIL_INC_R2	MFR_APS_IIL_R2 = PHASE_NUM_ACTIVE x MFR_APS_IIL_INC_R2 + MFR_APS_IIL_BASE_R2. 1A/LSB
3:0	MFR_APS_IIL_BASE_R2	Sets the basic APS basic phase-shedding level. 1A/LSB

MFR_APS_CTRL_SET_R2 (AFh)

The MFR_APS_CTRL_SET command on Page 1 sets rail 2 automatic phase-shedding (APS) related timing and behaviors.

Command	MFR_APS_CTRL_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function												MFR_PS_ENTER_TIME_R2				

Bits	Bit Name	Description
15:12	OC_NPH_EXIT_CNT_R2	Sets the period delay count from OCP_PHASE being triggered to the device exiting APS. 100ns/LSB.
11	OC_NPH_EXIT_EN_R2	Enables OCP_PHASE protection to exit automatic phase-shedding (APS) at any power state. 1'b0: Disable the OCP_PHASE signal to trigger any phase to full-phase operation 1'b1: Enable the OCP_PHASE signal to trigger any phase to full-phase operation
10	OC_1PS_EXIT_EN_R2	Enables OCP_PHASE protection to exit APS during 1-phase DCM/CCM only. 1'b0: Disabled 1'b1: Enabled

9	MFR_ADP_UV_EXIT_EN_R2	Sets rail 2 V_{FB} < VID - 25mV to enter full-phase operation. 1'b0: Disabled 1'b1: Enabled
8	MFR_ADP_PFM_EXIT_EN_R2	Enables the rail 2 frequency to increase to exit APS. 1'b0: Disabled 1'b1: Enabled
7:5	MFR_APS_FS_COEF_R2	3'b000: The f_{SW} limit threshold is 40%*(Ts/N-Tblank) 3'b001: The f_{SW} limit threshold is 60%*(Ts/N-Tblank) 3'b010: The f_{SW} limit threshold is 80%*(Ts/N-Tblank) 3'b011: The f_{SW} limit threshold is 100%*(Ts/N-Tblank) 3'b100: The f_{SW} limit threshold is 120%*(Ts/N-Tblank) 3'b101: The f_{SW} limit threshold is 140%*(Ts/N-Tblank) 3'b110: The f_{SW} limit threshold is 160%*(Ts/N-Tblank) 3'b111: The f_{SW} limit threshold is 180%*(Ts/N-Tblank) N: phase number, Ts: period time, Tblank: blank time
4:0	MFR_PS_ENTER_TIME_R2	Sets the phase-shedding delay time. If the reported load current remains below the APS threshold for the time set by APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE, then the controller enters APS mode and automatically sheds the phase count according to the load current.

MFR_APS_CTRL23_SET_R2 (B0h)

The MFR_APS_CTRL23_SET command on Page 1 sets rail 2 automatic phase-shedding (APS) related timing and behaviors.

Command	MFR_APS_CTRL23_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						RETURN_APS_DELAY										

Bits	Bit Name	Description
15	MFR_FS_DETECT_R2	Enables the device to exit phase-shedding according to the PWM1 off time. The PWM minimum off time is excluded from the PWM off time. 1'b0: Disable PWM1 off time detection to exit automatic phase-shedding (APS) 1'b1: Enable PWM1 off time detection to exit APS
14	FS_EXIT_APS_EN_NP	Enables the device to exit phase-shedding according to the multi-phase PWM interval time between consecutive phases. The time threshold is set by register 4Bh on Page 0. The PWM blanking time is excluded from the PWM interval time. 1'b0: Disable multi-phase PWM interval time detection to exit APS 1'b1: Enable multi-phase PWM interval time detection to exit APS
13:11	FS_EXIT_APS_CNT_1P	Sets the continuous count of the PWM1 off-time condition to exit phase-shedding. If the PWM off-time condition meets the counting threshold, the controller exits APS immediately.
10:7	RETURN_APS_DELAY	Sets the minimum full-phase runtime after exiting APS due to a f_{SW} event. 20µs/LSB.
6:4	FS_EXIT_APS_CNT_NP	Sets the continuous count of the multi-phase PWM interval time to exit phase-shedding. If the PWM interval condition meets the counting threshold, the controller exits APS immediately.
3:0	MFR_PS_INTERVAL_R2	Set the phase by phase dropping time intervals. It is only effective when p1/B4h bit [14] is set to 0. 2.5µs/LSB

MFR_FSCB_LOOP_CTRL_R2 (B1h)

The MFR_FSCB_LOOP_CTRL_R2 command on Page 1 set the rail 2 f_{SW} and current balance loop.

Command	MFR_FSCB_LOOP_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					FS_LOOP_CNT_R2											

Bits	Bit Name	Description
15	FS_LOOP_EN_R2	Enables the f_{SW} loop. The frequency loop keeps f_{SW} constant, and is equal to the set value at different input voltages and load currents. This bit is active for both rails. 1'b0: Disabled 1'b1: Enabled
14	FS_LOOP_CTRL_R2	Holds frequency loop regulation if a load transient event is detected (e.g. V_{FB} exceeds the VFB+ window or VFB- window). 1'b0: Disables holding frequency loop regulation if a load transient event is detected 1'b1: Enables holding frequency loop regulation if a load transient event is detected
13	PS_HOLD_FS_EN	Holds frequency loop regulation if the phase count changes. 1'b0: Disables holding frequency loop regulation if the phase count changes 1'b1: Enables holding frequency loop regulation if the phase count changes
12	DVID_HOLD_FS_EN	Holds frequency loop regulation if DVID occurs. 1'b0: Disables holding frequency loop regulation if DVID occurs 1'b1: Enables holding frequency loop regulation if DVID occurs
11:8	FS_LOOP_CNT_R2	Sets the minimum frequency loop hold time if a load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set. 100µs/LSB.
7	CB_LOOP_EN_R2	Enables the current balance loop. 1'b1: Enabled 1'b0: Disabled
6	PRD_HOLD_CB_EN_R2	Holds the current balance loop if the PWM period meets the PWM switching period condition set via PMBus command MFR_VR_CONFIG1 (B7h), bits[3:2]. 1'b0: Disables holding the current balance loop if the PWM switching period condition is met 1'b1: Enables holding the current balance loop if the PWM switching period condition is met
5	PS_HOLD_CB_EN_R2	Holds the current balance loop if the phase number changes. 1'b0: Disables holding the current balance loop if the phase count changes 1'b1: Enables holding the current balance loop if the phase count changes
4	DVID_HOLD_CB_EN_R2	Holds the current balance loop if DVID occurs. 1'b0: Disable holding the current balance loop if DVID occurs 1'b1: Enables holding the current balance loop if DVID occurs
3:0	CB_LOOP_HOLD_TIME	Sets the current balance loop hold time. If a load transient event, PWM switching period change event, phase count change event, or DVID event is detected, and the corresponding enable bit is set, the current balance loop stops regulating for the time set by the CB_LOOP_THOLD command. 100µs/LSB.

MFR_VOUT_LOOP_CTRL_R2 (B2h)

The MFR_VOUT_LOOP_CTRL_R2 command on Page 1 the rail 2 V_{OUT} loop parameters.

Command	MFR_VOUT_LOOP_CTRL_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			X	0												

Bits	Bit Name	Description
15:14	MFR_VID_RES_R2	Sets the VID step. VID step with VDIFF gain = 1, V_{OUT} = 0V to 1.55V: 2'b00: 6.25mV 2'b01: 5mV 2'b1x: Invalid command VID step with VDIFF gain = 0.5, V_{OUT} = 0V to 3V: 2'b00: 6.25mV 2b01: 5mV 2'b1x: Invalid command VID step with VDIFF gain = 0.8, V_{OUT} = 0V to 2V: 2'b00: 1.953125mV 2'b01: 5mV 2'b1x: Invalid command VID step with VDIFF gain = 0.4, V_{OUT} = 0V to 3.3V: 2'b00: 3.906250mV 2'b01: 5mV 2'b1x: Invalid command
13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	MFR_VDIFF_LOOP_EN_R2	Fixed to 0.
11:10	MFR_VDIFF_GAIN_SEL_R2	Sets the rail 2 remote-sense amplifier gain: 2'b00: 1 2'b01: 0.5 2'b10: 0.8 2'b11: 0.4
9	MFR_DC_REF_SEL_R2	1'b0: The COMP error amplifier (EA) uses V_{FB} and V_{REF} 1'b1: The COMP EA uses V_{DIFF} and V_{REF}
8	MFR_VCAL_PS2_EN_R2	Enables DC loop calibration in DCM. 1'b0: Disabled 1'b1: Enabled
7	MFR_VCAL_EN_R2	Enables DC loop calibration in DCM and CCM. 1'b0: Disabled 1'b1: Enabled
6	PRD_HOLD_DC_EN_R2	Holds the DC loop if the PWM time interval meets the PWM switching period condition set by PMBus command MFR_VR_CONFIG1 (B7h), bits[3:2]. 1'b0: Disables holding the DC loop when the PWM switching period condition is met 1'b1: Enables holding the DC loop when the PWM switching period condition is met

5	PS_HOLD_DC_EN_R2	Holds the DC loop when the phase count changes. 1'b0: Disables holding the DC loop when the phase count changes 1'b1: Enables holding the DC loop when the phase count changes
4	TRANS_HOLD_DC_EN_R2	Holds DC loop regulation if a load transient event is detected (e.g. V_{FB} exceeds VFB+ window or VFB- window.) 1'b0: Disables holding DC loop regulation when the VFB+/- window condition is met 1'b1: Enables holding DC loop regulation when the VFB+/- window condition is met
3:0	MFR_DC_LOOP_CNT_R2	Sets the DC loop minimum hold time in direct format. 200µs/LSB with a +100µs offset.

MFR_SETTLE_CTRL_R2 (B3h)

The MFR_SETTLE_CTRL command on Page 1 sets the DVID parameters.

Command	MFR_SETTLE_CTRL_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						MFR_RISE_STEP_R2					MFR_SETTLE_DELAY_R2					

Bits	Bit Name	Description
15:11	MFR_DROOPFALL_DELAY_R2	Sets the delay time between V_{REF} reaching the target (VID + DROOP_VID) and V_{REF} falling back to VID. 50ns/LSB.
10:6	MFR_RISE_STEP_R2	Sets the extra VID step count for rail 2 when DVID is up. The extra VID steps compensate for the droop caused by the output capacitor charging when DVID is up. 1 step/LSB.
5:0	MFR_SETTLE_DELAY_R2	Fixed to 5.

MFR_PHASE_SET_R2 (B4h)

The MFR_PHASE_SET command on Page 1 sets the rail 2 phase configuration.

Command	MFR_PHASE_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					MFR_PSI_SET_R2											

Bits	Bit Name	Description
15	MFR_AUTO_PS_EN_R2	Enables rail 2 automatic phase-shedding (APS). 1'b0: Disabled 1'b1: Enabled
14	MFR_PHASHED_EXIT_MOD_R2	Sets the phase-dropping mode during phase-shedding. The phase-shedding may be due to APS. 1'b0: Shed phases one by one with a configured delay time. The delay time is set with the DROP_PHASE_WAIT_TIME command 1'b1: Drop the phase count to the target immediately
13	MFR_CS_PIN_SEL_EN	Disable certain phases by shorting the CSx pin to GND. For example, If the NVM configuration is 14 + 2, and CS9 and CS15 are shorted to GND, then phases 8 + 1 operate.

12	MFR_PSI_SET_EN_R2	Enables forcing the rail 2 power state based on bits[11:8]. 1'b0: Disable the forced power state 1'b1: Enable the forced power state. The active phase number is determined by bits[11:8] of this command
11:8	MFR_PSI_SET_R2	Sets the forced phase number for the rail 2 power state. 4'b0000: DCM 4'b0001: 1-phase CCM 4'b0010: 2-phase CCM 4'b0011: 3-phase CCM 4'b0100: 4-phase CCM 4'b0101: 5-phase CCM 4'b0110: 6-phase CCM 4'b0111: 7-phase CCM 4'b1000: 8-phase CCM
7:6	MFR_REDUNDANT_PH_R2	Fixed to 0.
5	PHASE1_REDUNDANCY_RESET	Enables the phase 1 redundancy flag to be reset. 1'b0: Disabled 1'b1: Enabled
4	MFR_RAIL_SWAP	Fixed to 0.
3:0	MFR_PHASE_NUM_CFG_R2	Sets the rail 2 phase number.

MFR_GPIO2_SEL (B5h)

The MFR_GPIO2_SEL command on Page 1 sets the GPIO2-related parameters.

Command	MFR_GPIO2_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			X											GPIO2_SEL		

Bits	Bit Name	Description
15	MFR_GPIO_ALT_SEL	1'b0: The alert signal in GPIO1 indicates rail 1, and the GPIO2 signal indicates rail 2 1'b1: The alert signal in GPIO1 indicates rail 2, and the GPIO2 signal indicates rail 1 The alert signal includes: OCP_SPIKE#, OCP_TDC#, VRHOT#, OC_WARN#, OCP_L, and DRMOS_FAULT#.
14	GPIO2_TRI_STATE	1'b0: GPIO2 is an open-drain output 1'b1: GPIO2 is a push-pull output
13	GPIO2_DIG_EN	Reserved.
12	MFR_GPIO_FORCE	1'b0: Low level 1'b1: High level
10	GPIO2_EN_SEL	1'b0: Set GPIO2 to the monitoring function 1'b1: Set GPIO2 to the EN function. GPIO1_DIN_EN must be set to 1
9:8	MFR_EN2_SEL	2'b00: The internal rail 2 enable signal is from the EN pin 2'b01: The internal rail 2 enable signal is from the GPIO1 pin 2'b10: The internal rail 2 enable signal is from the GPIO2 pin 2'b11: The internal rail 2 enable signal is from the internal rail 2 power good (PG) signal

7:6	VIMON_SEL	Sets the VIMONx buffer on the GPIO2 pin. 2'b00: Disable buffer 2'b01: Enable buffer to VIMON1_FIL 2'b10: Enable buffer to VIMON2_FIL 2'b11: Disable buffer
5	VCS_REF_SEL	Enables the VCS_REF buffer on the GPIO2 pin. 1'b0: Disabled 1'b1: Enabled
4	REFIN_SEL	Enables the REFIN buffer on the GPIO2 pin 1'b0: Disabled 1'b1: Enabled
3	MFR_PG_SEL	1'b0: The PG_L1 pin is used for rail 1 PG indication. GPIOx_DOUT can select rail 2 PG 1'b1: The PG_L1 pin is used for rail 2 PG indication. GPIOx_DOUT can select rail 1 PG
2:0	GPIO2_SEL	3'b000: GPIO2_DOUT = 1 or 0, determined by MFR_GPIO_FORCE (B5h on Page 1), bit[12] 3'b001: GPIO2_DOUT = FAULT# 3'b010: GPIO2_DOUT = rail 1 or rail 2 PG, determined by MFR_PH_SEL (B5h on Page 1), bit[13] 3'b011: GPIO2_DOUT = OCP_L 3'b100: GPIO2_DOUT = DRMOS_FAULT# 3'b101: GPIO2_DOUT = OC_WARN# 3'b110: GPIO2_DOUT = VHOT# 3'b111: GPIO2_DOUT = OCP_TDC# or OCP_SPIKE#, determined by MFR_GPIO_FORCE (B5h on Page 1), bit[12]

MFR_PG_DELAY_R2 (B6h)

The MFR_PG_DELAY_R2 command on Page 1 sets the delay time for power good (PG) on and off.

Command	MFR_PG_DELAY_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PGOFF_DELAY_R2						MFR_PGON_DELAY_R2									

Bits	Bit Name	Description
15:10	MFR_PGOFF_DELAY_R2	Sets the power good (PG) off delay time. 5µs/LSB.
9:0	MFR_PGON_DELAY_R2	Sets the PG on delay time. 5µs/LSB.

MFR_PWM_MUX1 (B7h)

The MFR_PWM_MUX1 command on Page 1 sets the internal PWM signal selection. The internal PWM_x ($1 \le x \le 20$) signal can select the PWM1~PWM16 pins. PWM_1~PWM_16 is used for rail 1, and PWM_13~PWM_20 is used for rail 2.

Command	MFR_PWM_MUX1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PWM_MUX4				MFR_PWM_MUX3				MFR_PWM_MUX2				MFR_PWM_MUX1			

Bits	Bit Name	Description
15:12	MFR_PWM_MUX4	Selects the internal PWMx (1 ≤ x ≤ 20) signal for the PWM4 pin. It is for rail 1 only. 4'b0000: PWM_1 4'b0001: PWM_2 4'b0010: PWM_3 4'b0011: PWM_4 4'b0100: PWM_5 4'b0101: PWM_6 4'b0110: PWM_7 4'b0111: PWM_8 4'b1000: PWM_9 4'b1001: PWM_10 4'b1010: PWM_11 4'b1011: PWM_12 4'b1100: PWM_13 4'b1101: PWM_14 4'b1110: PWM_15 4'b1111: PWM_16
11:8	MFR_PWM_MUX3	Selects the internal PWMx (1 ≤ x ≤ 20) signal for the PWM3 pin. It is for rail 1 only. 4'b0000: PWM_1 4'b0001: PWM_2 4'b0010: PWM_3 4'b0011: PWM_4 4'b0100: PWM_5 4'b0101: PWM_6 4'b0110: PWM_7 4'b0111: PWM_8 4'b1000: PWM_9 4'b1001: PWM_10 4'b1010: PWM_11 4'b1011: PWM_12 4'b1100: PWM_13 4'b1101: PWM_14 4'b1110: PWM_15 4'b1111: PWM_16
7:4	MFR_PWM_MUX2	Selects the internal PWMx (1 ≤ x ≤ 20) signal for the PWM2 pin. It is for rail 1 only. 4'b0000: PWM_1 4'b0001: PWM_2 4'b0010: PWM_3 4'b0011: PWM_4 4'b0100: PWM_5 4'b0101: PWM_6 4'b0110: PWM_7 4'b0111: PWM_8 4'b1000: PWM_9 4'b1001: PWM_10 4'b1010: PWM_11 4'b1011: PWM_12 4'b1100: PWM_13 4'b1101: PWM_14 4'b1110: PWM_15 4'b1111: PWM_16

3:0	MFR_PWM_MUX1	Selects the internal PWMx (1 ≤ x ≤ 20) signal for the PWM1 pin. It is for rail 1 only. 4'b0000: PWM_1 4'b0001: PWM_2 4'b0010: PWM_3 4'b0011: PWM_4 4b0100: PWM_5 4'b0101: PWM_6 4'b0110: PWM_7 4'b0111: PWM_8 4'b1000: PWM_9 4'b1001: PWM_10 4'b1010: PWM_11 4'b1011: PWM_12 4'b1100: PWM_13 4'b1101: PWM_14 4'b1110: PWM_15 4'b1111: PWM_16

MFR_PWM_MUX2 (B8h)

The MFR_PWM_MUX2 command on Page 1 sets the internal PWM signal selection.

Command	MFR_PWM_MUX2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PWM_MUX8				MFR_PWM_MUX7				MFR_PWM_MUX6				MFR_PWM_MUX5			

Bits	Bit Name	Description
15:12	MFR_PWM_MUX8	Selects the internal PWMx (1 ≤ x ≤ 20) signal for the PWM8 pin. It is for rail 1 only. 4'b0000: PWM_1 4'b0001: PWM_2 4'b0010: PWM_3 4'b0011: PWM_4 4'b0100: PWM_5 4'b0101: PWM_6 4'b0110: PWM_7 4'b0111: PWM_8 4'b1000: PWM_9 4'b1001: PWM_10 4'b1010: PWM_11 4'b1011: PWM_12 4'b1100: PWM_13 4'b1101: PWM_14 4'b1110: PWM_15 4'b1111: PWM_16

11:8	MFR_PWM_MUX7	Selects the internal PWMx (1 ≤ x ≤ 20) signal for the PWM7 pin. It is for rail 1 only. 4'b0000: PWM_1 4'b0001: PWM_2 4'b0010: PWM_3 4'b0011: PWM_4 4'b0100: PWM_5 4'b0101: PWM_6 4'b0110: PWM_7 4'b0111: PWM_8 4'b1000: PWM_9 4'b1001: PWM_10 4'b1010: PWM_11 4'b1011: PWM_12 4'b1100: PWM_13 4'b1101: PWM_14 4'b1110: PWM_15 4'b1111: PWM_16
7:4	MFR_PWM_MUX6	Selects the internal PWMx (1 ≤ x ≤ 20) signal for the PWM6 pin. It is for rail 1 only. 4'b0000: PWM_1 4'b0001: PWM_2 4'b0010: PWM_3 4'b0011: PWM_4 4'b0100: PWM_5 4'b0101: PWM_6 4'b0110: PWM_7 4'b0111: PWM_8 4'b1000: PWM_9 4'b1001: PWM_10 4'b1010: PWM_11 4'b1011: PWM_12 4'b1100: PWM_13 4'b1101: PWM_14 4'b1110: PWM_15 4'b1111: PWM_16
3:0	MFR_PWM_MUX5	Selects the internal PWMx (1 ≤ x ≤ 20) signal for the PWM5 pin. It is for rail 1 only. 4'b0000: PWM_1 4'b0001: PWM_2 4'b0010: PWM_3 4'b0011: PWM_4 4'b0100: PWM_5 4'b0101: PWM_6 4'b0110: PWM_7 4'b0111: PWM_8 4'b1000: PWM_9 4'b1001: PWM_10 4'b1010: PWM_11 4'b1011: PWM_12 4'b1100: PWM_13 4'b1101: PWM_14 4'b1110: PWM_15 4'b1111: PWM_16

MFR_PWM_MUX3 (B9h)

The MFR_PWM_MUX3 command on Page 1 sets the internal PWM signal selection.

Command	MFR_PWM_MUX3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PWM_MUX16				MFR_PWM_MUX15				MFR_PWM_MUX14				MFR_PWM_MUX13			

Bits	Bit Name	Description
15:12	MFR_PWM_MUX16	This command works with register BBh (on Page 1), bit[11]. Selects the internal PWMx (1 ≤ x ≤ 16 for rail 1, or 13 ≤ x ≤ 20 for rail 2) signal for the PWM12 pin on rail 1, or the PWM5_L2 pin on rail 2.
11:8	MFR_PWM_MUX15	This command works with register BBh (on Page 1), bit[10]. Selects the internal PWMx (1 ≤ x ≤ 16 for rail 1, or 13 ≤ x ≤ 20 for rail 2) signal for the PWM11 pin on rail 1, or the PWM6_L2 pin on rail 2.
7:4	MFR_PWM_MUX14	This command works with register BBh (on Page 1), bit[9]. Selects the internal PWMx (1 ≤ x ≤ 16 for rail 1, or 13 ≤ x ≤ 20 for rail 2) signal for the PWM10 pin on rail 1, or the PWM7_L2 pin on rail 2.
3:0	MFR_PWM_MUX13	This command works with register BBh (on Page 1), bit[8]. Selects the internal PWMx (1 ≤ x ≤ 16 for rail 1, or 13 ≤ x ≤ 20 for rail 2) signal for the PWM9 pin on rail 1, or the PWM7_L8 pin on rail 2.

MFR_PWM_MUX4 (BAh)

The MFR_PWM_MUX4 command on Page 1 sets the internal PWM signal selection.

Command	MFR_PWM_MUX4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PWM_MUX20				MFR_PWM_MUX19				MFR_PWM_MUX18				MFR_PWM_MUX17			

Bits	Bit Name	Description
15:12	MFR_PWM_MUX20	This command works with register BBh (on Page 1), bit[15]. Selects the internal PWMx (1 ≤ x ≤ 16 for rail 1, or 13 ≤ x ≤ 20 for rail 2) signal for the PWM16 pin on rail 1, or the PWM1_L2 pin on rail 2.
11:8	MFR_PWM_MUX19	This command works with register BBh (on Page 1), bit[14]. Selects the internal PWMx (1 ≤ x ≤ 16 for rail 1, or 13 ≤ x ≤ 20 for rail 2) signal for the PWM15 pin on rail 1, or the PWM2_L2 pin on rail 2.
7:4	MFR_PWM_MUX18	This command works with register BBh (on Page 1), bit[13]. Selects the internal PWMx (1 ≤ x ≤ 16 for rail 1, or 13 ≤ x ≤ 20 for rail 2) signal for the PWM14 pin on rail 1, or the PWM3_L2 pin on rail 2.
3:0	MFR_PWM_MUX17	This command works with register BBh (on Page 1), bit[12]. Selects the internal PWMx (1 ≤ x ≤ 16 for rail 1, or 13 ≤ x ≤ 20 for rail 2) signal for the PWM13 pin on rail 1, or the PWM4_L2 pin on rail 2.

MFR_PWM_MUX_1MSB (BBh)

The MFR_PWM_MUX_1MSB command on Page 1 sets the internal PWM signal selection.

Command	MFR_PWM_MUX_1MSB															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									0	0	0	0	0	0	0	0

Bits	Bit Name	Description
15	MFR_PWM_MUX20_MSB	The 1MSB of the internal PWM_20.
14	MFR_PWM_MUX19_MSB	The 1MSB of the internal PWM_19.
13	MFR_PWM_MUX18_MSB	The 1MSB of the internal PWM_18.
12	MFR_PWM_MUX17_MSB	The 1MSB of the internal PWM_17.
11	MFR_PWM_MUX16_MSB	The 1MSB of the internal PWM_16.
10	MFR_PWM_MUX15_MSB	The 1MSB of the internal PWM_15.
9	MFR_PWM_MUX14_MSB	The 1MSB of the internal PWM_14.
8	MFR_PWM_MUX13_MSB	The 1MSB of the internal PWM_13.
7	MFR_PWM_MUX8_MSB	Fixed to 0.
6	MFR_PWM_MUX7_MSB	Fixed to 0.
5	MFR_PWM_MUX6_MSB	Fixed to 0.
4	MFR_PWM_MUX5_MSB	Fixed to 0.
3	MFR_PWM_MUX4_MSB	Fixed to 0.
2	MFR_PWM_MUX3_MSB	Fixed to 0.
1	MFR_PWM_MUX2_MSB	Fixed to 0.
0	MFR_PWM_MUX1_MSB	Fixed to 0.

MFR_BLANK_TIME2_R2 (BCh)

The MFR_BLANK_TIME2_R2 command configures the second set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 2 only.

Three sets of SLOPE_RESET_TIME and PWM_BLANK_TIME can be set via registers BBh and BDh on Page 1. One of these times is selected as real-time value according to the operation phase number. The relationship is described below:

$$\text{SLOPE\_RESET\_TIME}=\begin{cases}\text{SLOPE\_RESET\_TIME1(reg BCh bit[11:6]),} & \text{phase num} \geq \text{PHS\_NUM\_LV2}\\ \text{SLOPE\_RESET\_TIME3(reg BDh bit[11:6]),} & \text{phase num} < \text{PHS\_NUM\_LV2}\end{cases}$$

$$\text{PWM\_BLANK\_TIME}=\begin{cases}\text{PWM\_BLANK\_TIME1(reg BCh bit[5:0]),} & \text{phase num} \geq \text{PHS\_NUM\_LV2}\\ \text{PWM\_BLANK\_TIME3(reg BDh bit[5:0]),} & \text{phase num} < \text{PHS\_NUM\_LV2}\end{cases}$$

Where PHS_NUM_LV2 is the phase number set by register MFR_BLANK_TIME2_R2 (BCh on Page 1), bits[15:12].

Command	MFR_BLANK_TIME2_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					MFR_SLOPE_BLANK_TIME2_R2						MFR_PHASE_BLANK_TIME2_R2					

Bits	Bit Name	Description
15:12	MFR_BLANK_TIME_LV2_R2	Sets the phase number threshold to the slope compensation reset time and PWM blanking time.
11:6	MFR_SLOPE_BLANK_TIME2_R2	Configures the second set of slope compensation reset times. The slope compensation reset time should be not exceed the PWM blanking time set by MFR_BLANK_TIME2_R2 (BCh on Page 1), bits[5:0]. 5ns/LSB.
5:0	MFR_PHASE_BLANK_TIME2_R2	Configures the PWM blanking time between two consecutive phases. 5ns/LSB. The actual blanking time is equal to the internal fixed 20ns + BCh, bits[5:0] x 5ns.

MFR_BLANK_TIME3_R2 (BDh)

The MFR_BLANK_TIME3_R2 command configures the third set of slope compensation reset times and PWM blanking times between two consecutive phases. It is for rail 2 only.

Command	MFR_BLANK_TIME3_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	MFR_SLOPE_BLANK_TIME3_R2						MFR_PHASE_BLANK_TIME3_R2					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	MFR_SLOPE_BLANK_TIME3_R2	Configures the third set of slope compensation reset times. The slope compensation reset time should be not exceed the PWM blanking time set by MFR_BLANK_TIME3_R2 (BDh on Page 1), bits[5:0]. 5ns/LSB.
5:0	MFR_PHASE_BLANK_TIME3_R2	Configures the PWM blanking time between two consecutive phases. 5ns/LSB. The actual blanking time is equal to the internal fixed 20ns + BDh, bits[5:0] x 5ns.

MFR_SLOPE_CNT_SET_R2 (BEh)

The MFR_SLOPE_CNT_SET command on Page 1 sets the slope CNT coefficient on rail 2.

Command	MFR_SLOPE_CNT_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function							MFR_SLOPE_CNT_DCM_R2									

Bits	Bit Name	Description
15:12	MFR_TRIM_DCM_R2	Sets the V_{OUT} trim for 1-phase DCM operation. 2.3mV/LSB.
11:10	MFR_SLOPE_CNT_COEF_R2	Sets the CCM slope CNT coefficient. 2b'00: CNT x 1.2 2b'01: CNT x 1.3 2b'10: CNT x 1.4 2b'11: CNT x 1.5 Where CNT is t_{SW} / n - $t_{SLOPE\_RESET\_TIME}$, *n* is phase number, and $t_{SLOPE\_RESET\_TIME}$ is set by BCh and BDh on Page 1.

9:0	MFR_SLOPE_CNT_DCM_R2	Sets the slope compensation saturation time for rail 2 in 1-phase DCM. 5ns/LSB.

MFR_SLOPE_PEAK_SET_R2 (BFh)

The MFR_SLOPE_PEAK_SET command on Page 1 sets the slope peak value.

Command	MFR_SLOPE_PEAK_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_SLOPE_SW_INI_R2							MFR_VCAL_I_SLOW				MFR_SLOPE_PEAK_DATA_R2				

Bits	Bit Name	Description
15:9	MFR_SLOPE_SW_INI_R2	Sets the current-source quantity for slope voltage generation. 0.25μA/LSB.
8:5	MFR_VCAL_I_SLOW	Fixed to 1.
4:0	MFR_SLOPE_PEAK_DATA_R2	Sets the slope peak value. 1.875mV/LSB.

MFR_TRIM_14P_R2 (C0h)

The MFR_TRIM_14P_R2 command on Page 1 sets the slope trim value from 1-phase to 4-phase CCM in manual slope mode.

Command	MFR_TRIM_14P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_TRIM_4P_R2				MFR_TRIM_3P_R2				MFR_TRIM_2P_R2				MFR_TRIM_1P_R2			

Bits	Bit Name	Description
15:12	MFR_TRIM_4P_R2	Sets the V_{OUT} trim for 4-phase CCM. 2.3mV/LSB.
11:8	MFR_TRIM_3P_R2	Sets the V_{OUT} trim for 3-phase CCM. 2.3mV/LSB.
7:4	MFR_TRIM_2P_R2	Sets the V_{OUT} trim for 2-phase CCM. 2.3mV/LSB.
3:0	MFR_TRIM_1P_R2	Sets the V_{OUT} trim for 1-phase CCM. 2.3mV/LSB.

MFR_SLOPE_DCM_SET_R2 (C1h)

The MFR_SLOPE_DCM_SET command on Page 1 trims the rail 2 V_{OUT} in 1-phase DCM.

Command	MFR_TRIM_14P_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X			DRMOS_KCS2			CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:13	MFR_TRIM_DCM_BIAS_R2	Fixed to 0.

12:10	DRMOS_KCS2	Sets the rail 2 DrMOS current-sense gain. 3'b000: 5μA/A 3'b001: 8.5μA/A 3'b010: 9μA/A 3'b011: 9.7μA/A 3'b100: 10μA/A Others: Invalid commands
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets current-source value for slope compensation. 0.25μA/LSB.

MFR_TRIM_SEL (C2h)

The MFR_TRIM_SEL command on Page 1 sets the TRIM selection.

Command	MFR_TRIM_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:12	MFR_DROP_TRIM_SEL_R2	Selects one of the 16 backup trim registers (18h~1Fh in both Page 0 and Page 1) as the I_{DROOP} trim register for rail 2. See Table 11 for details.
11:8	MFR_IMON_TRIM_SEL_R2	Selects one of the 16 backup trim registers (18h~1Fh in both Page 0 and Page 1) as the IMON2 trim register for rail 2. See Table 11 for details.
7:4	MFR_DROP_TRIM_SEL_R1	Selects one of the 16 backup trim registers (18h~1Fh in both Page 0 and Page 1) as the I_{DROOP} trim register for rail 1. See Table 11 for details.
3:0	MFR_IMON_TRIM_SEL_R1	Selects one of the 16 backup trim registers (18h~1Fh in both Page 0 and Page 1) as the IMON1 trim register for rail 1. See Table 11 for details.

Table 11 shows the TRIM_SEL# values and conditions. Select the trim register based on R_{IMON} and the G_{IMON} value used for configuration.

Table 11: Trim Register Selection

TRIM_SEL#	Trim Register	IMON1	IMON2	I_{DROOP1}	I_{DROOP2}
0	18h (Page 0)	10kΩ,1/16	-	-	-
1	19h (Page 0)	-	10kΩ,1/16	-	-
2	1Ah (Page 0)	-	-	1.26kΩ, 5/16	-
3	1Bh (Page 0)	-	-	-	1.26kΩ, 5/16
4	1Ch (Page 0)	5kΩ,1/16	-	-	-
5	1Dh (Page 0)	10kΩ,1/8	-	-	-
6	1Eh (Page 0)	40kΩ,1/16	-	-	-
7	1Fh (Page 0)	-	10kΩ,1/8	-	-
8	18h (Page 1)	-	40kΩ,1/16	-	-
9	19h (Page 1)	-	40kΩ,1/8	-	-
10	1Ah (Page 1)	-	5kΩ,1/16	-	-
11	1Bh (Page 1)	2.5kΩ,1/16	-	-	-
12	1Ch (Page 1)	-	-	400Ω,1/16	-
13	1Dh (Page 1)	-	400Ω,1/16	-	-
14	1Eh (Page 1)	-	400Ω,1/4	-	-
15	1Fh (Page 1)	40kΩ,1/8	-	-	-

MFR_PWM_MUX_PART5 (C3h)

The MFR_PWM_MUX_PART5 command is fixed to 0xFFFF.

Command	MFR_PWM_MUX_PART5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_PWM_MUX12				MFR_PWM_MUX11				MFR_PWM_MUX10				MFR_PWM_MUX9			

Bits	Bit Name	Description
15:12	MFR_PWM_MUX12	Fixed to 15.
11:8	MFR_PWM_MUX11	Fixed to 15.
7:4	MFR_PWM_MUX10	Fixed to 15.
3:0	MFR_PWM_MUX9	Fixed to 15.

MFR_CP_SET (C4h)

The MFR_CP_SET command on Page 1 sets the phase redundancy and GPIO-related parameters.

Command	MFR_CP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	1	1	1	1								GPIO_PG1_SEL				

Bits	Bit Name	Description
15	MFR_PWM_MUX12_ MSB	Fixed to 1.
14	MFR_PWM_MUX11_ MSB	Fixed to 1.
13	MFR_PWM_MUX10_ MSB	Fixed to 1.
12	MFR_PWM_MUX9_ MSB	Fixed to 1.
11	MFR_CB_DETECT_EN	Enables redundant phase protection detection by detecting the current imbalance. 1'b0: Disabled 1'b1: Enabled
10:7	MFR_PH_FAULT_TIME2	If the current-sense voltage (V_{CS}) is below the low limit (-450mV) for the interval set by MFR_PH_FAULT_TIME2, the related phase is considered abnormal. If MFR_CR_DETECT_TIME_SEL, bit[1] = 1, then this register is 2μs/LSB. If MFR_CR_DETECT_TIME_SEL, bit[1] = 0, then this register is 20μs/LSB.
6	HYST_EN	Fixed to 0.
5	MFR_EN_HL_SEL	1'b0: EN_L1/2 pin is active high 1'b1: EN_L1/2 pin is active low

4:2	GPIO_PG1_SEL	3'b000: PG pin = 1 or 0, determined by MFR_GPIO_FORCE (B5h on Page 1), bit[12] 3'b001: PG pin = FAULT# 3'b010: PG pin = Rail 1 or rail 2 power good (PG), determined by MFR_PG_SEL (B5h on Page 1), bit[3] 3'b011: PG pin = OCP_L 3'b100: PG pin = DRMOS_FAULT# 3'b101: PG pin = OC_WARN# 3'b110: PG pin = VRHOT# 3'b111: PG pin = the internal PG signal is determined by B5h (on Page 0 and Page 1), bit[3]
1	MFR_DBG_VINUVLO	Fixed to 0.
0	MFR_APS_SD_MODE	1'b0: Independent inductor mode 1'b1: Coupling inductor mode

MFR_SD_VID_SET (C5h)

The MFR_SD_VID command on Page 1 sets the Hi-Z shutdown voltage level. It is only effective when VID slews down to 0V.

Command	MFR_SD_VID_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				MFR_VID_OFF					MFR_SD_VID							

Bits	Bit Name	Description
15	READ_VIN_BLOCK_EN	Enables the READ_VIN block CS ripple detection function. 1'b0: Disabled 1'b1: Enabled
14:13	READ_VIN_BLOCK_TH	Sets the READ_VIN threshold in block CS ripple detect function. If READ_VIN drops below the set level, CS ripple detection is disabled. 2'b00: 8V 2'b01: 9V 2'b10: 10V 2'b11: 11V
12:8	MFR_VID_OFF	Sets the minimum operating V_{REF} for both rails. If the target VID falls below the value set by MFR_VID_OFF, the associated rail DVIDs down to 0V and de-asserts the PG signal. 1 VID_STEP/LSB. VID_STEP is set by MFR_VOUT_LOOP_CTRL (B2h) bit [15:14].
7:0	MFR_SD_VID	Set the PWM Hi-Z shutdown voltage level for both rails. If the VID-DAC output falls below the Hi-Z shutdown voltage level, the output enters PWM Hi-Z shutdown. 1 VID_STEP/LSB. VID_STEP is set by MFR_VOUT_LOOP_CTRL (B2h), bits[15:14].

MFR_SR_MAX (C6h)

The MFR_SR_MAX command on Page 1 sets the maximum DVID slew rate in AVSBus mode.

Command	MFR_SR_MAX															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	MFR_SR_MAX						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	MFR_SR_MAX	Sets the AVSBus DVID slew rate limit. Select the resolution with MFR_SR_RES (A1h on Page 0), bit[0].

MFR_AVS_SET2 (C7h)

The MFR_AVS_SET2 command on Page 1 sets the AVSBus parameters.

Command	MFR_AVS_SET2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			1		MFR_AVS_THH_SET						MFR_AVS_THL_SET					

Bits	Bit Name	Description
15	MFR_AVS_EN	Enables AVSBus mode. 1'b0: Disabled 1'b1: Enabled
14	MFR_AVS_VDDIO_EN	1'b0: Set the AVS CMP threshold using the DACs 1'b1: Set the AVS CMP threshold using the VDDIO voltage and resistor divider
13	AVSBUS_MODE	Fixed to 1.
12	MFR_AVS_DAC_EN	1'b0: Set the AVS CMP threshold using the VDDIO voltage and resistor divider 1b1: Set the AVS CMP threshold using the DACs
11:6	MFR_AVS_THH_SET	0V to 2.56V. 40mV/LSB.
5:0	MFR_AVS_THL_SET	0V to 2.56V. 40mV/LSB.

MFR_AVS_SET (C8h)

The MFR_AVS_SET command on Page 1 sets the AVSBus interface parameters when MFR_VR_CONFIG3 (A2h on Page 0), bit[9] = 0.

Command	MFR_AVS_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			MFR_ACLL_SEL			X	MFR_AVS_ADDR_R2				MFR_AVS_ADDR_R1					

Bits	Bit Name	Description
15	MFR_PMBUS_SVI_LL_SEL_R2	Fixed to 1.
14	MFR_PMBUS_SVI_LL_SEL_R1	Fixed to 1.
13:11	MFR_ACLL_SEL	Fixed to 0.
10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	MFR_AVS_ADDR_R2	Set the rail 2 AVSBus slave address.
5:2	MFR_AVS_ADDR_R1	Set the rail 1 AVSBus slave address.
1	MFR_AVS_ADDR_EN_R2	1'b0: Rail 2 does not follow AVSBus commands 1'b1: Rail 2 follows AVSBus commands when OPERATION_R2 is 0xB0
0	MFR_AVS_ADDR_EN_R1	1'b0: Rail 1 does not follow AVSBus commands 1'b1: Rail 1 follows AVSBus commands when OPERATION_R1 is 0xB0

MFR_AVS_SET (C8h)

The MFR_AVS_SET command on Page 1 sets the SVI2 interface parameters when MFR_VR_CONFIG3 (A2h on Page 0), bit[9] = 1.

Command	MFR_AVS_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			MFR_ACLL_SEL			SVI2_TIMEOUT										

Bits	Bit Name	Description
15	MFR_PMBUS_SVI_LL_SEL_R2	Selects the load line for PMBus or SVI2 mode. It is for rail 2 only. 1'b0: SVI2 load line mode, The load line slope is determined by the SVI2 command 1'b1: PMBus load line mode
14	MFR_PMBUS_SVI_LL_SEL_R1	Selects the load line for PMBus or SVI2 mode. It is for rail 1 only. 1'b0: SVI2 load line mode. The load line slope is determined by the SVI2 command 1'b1: PMBus load line mode
13:11	MFR_ACLL_SEL	Fixed to 0.
10:7	SVI2_TIMEOUT	Sets the SVI2 bus wait timeout time. 0.5μs/LSB.
6:5	MFR_DECAY_MODE	Sets the activation criteria for decay mode on both rails. 2'b00: VID decay mode does not activate under any condition 2'b01: VID decay mode activates when PSI0_L is asserted (PSI0_L = 0) 2'b10: VID decay mode activates when both PSI0_L and PSI1_L are asserted (PSI0_L = 0, PSI1_L = 0)
4:2	MFR_DECAY_LENGTH	Sets both rails' V_{REF} minimum hold time for each VID step in decay mode. 100ns/LSB.
1	VBOOT_SVI2_EN	Selects the method to obtain the VBOOT value. 1'b0: Read the VBOOT value set by SVD, SVC, during VDD33 start-up 1'b1: Read the VBOOT value set by SVD, SVC, during VDD33 start-up when EN is no
0	VBOOT_SEL	1'b0: VBOOT set by 21h (on Page 0), bit[7:0]. 6.25mV/LSB 1'b1: VBOOT is set by SVD and SVC pins

MFR_AVS_WARN_MASK (C9h)

The AVS_WARN_MASK command on Page 1 sets the AVSBus warning mask related parameters.

Command	MFR_AVS_WARN_MASK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X					

Bits	Bit Name	Description
15:5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4	AVS_WARN_MASK_VRSETTLE	Masks the VR unsettle flag. This triggers a slave to issue the status response frame to the CPU. 1'b0: Not masked 1'b1: Masked

3	AVS_WARN_MASK_OC	Masks the over-current (OC) warning flag. This triggers a slave to issue the status response frame to the CPU. 1'b0: Not masked 1'b1: Masked
2	AVS_WARN_MASK_UV	Masks the under-voltage (UV) warning flag. This triggers a slave to issue the status response frame to the CPU. 1'b0: Not masked 1'b1: Masked
1	AVS_WARN_MASK_OP	Masks the over-power (OP) warning flag. This triggers a slave to issue the status response frame to the CPU. 1'b0: Not masked 1'b1: Masked
0	AVS_WARN_MASK_OT	Masks the over-temperature (OT) warning flag. This triggers a slave to issue the status response frame to the CPU. 1'b0: Not masked 1'b1: Masked

MFR_PMB_SET (CAh)

The MFR_PMB_SET command on Page 1 sets the PMBus high and low thresholds.

Command	MFR_PMB_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	MFR_PMB_THH_SET						MFR_PMB_THL_SET					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	MFR_PMB_THH_SET	0V to 2.56V. 40mV/LSB.
5:0	MFR_PMB_THL_SET	0V to 2.56V. 40mV/LSB.

MFR_OSR_SET_R1 (CBh)

The MFR_OSR_SET_R1 command on Page 1 sets the overshoot reduction (OSR) related parameters. It is for rail 1 only.

Command	MFR_OSR_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	0	0		MFR_OSR_FILTER_R1						MFR_OSR_BLANKTIME_R1						

Bits	Bit Name	Description
15	DBG_WD	Fixed to 0.
14	MFR_OSR_MODE	Fixed to 0.
13	MFR_OSR_EN_R1	Enables the overshoot reduction (OSR) function. This function can reduce the V_{OUT} overshoot when the load is released. 1'b0: Disabled 1'b1: Enabled
12:7	MFR_OSR_FILTER_R1	Sets the minimum overshoot reduction (OSR) time. 5ns/LSB.

6:0	MFR_OSR_BLANKTIME_R1	Sets the blanking time between two effective overshoot reduction (OSR) events. 10ns/LSB.

MFR_OSR_SET_R2 (CCh)

The MFR_OSR_SET_R2 command on Page 1 sets the overshoot reduction (OSR) related parameters. It is for rail 2 only.

Command	MFR_OSR_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	0	0		MFR_OSR_FILTER_R2						MFR_OSR_BLANKTIME_R2						

Bits	Bit Name	Description
15:14	MFR_WD_SET	Fixed to 0.
13	MFR_OSR_EN_R2	Enables the overshoot reduction (OSR) function. This function can reduce the V_{OUT} overshoot when the load is released. 1'b0: Disabled 1'b1: Enabled
12:7	MFR_OSR_FILTER_R2	Sets the minimum overshoot reduction (OSR) time. 5ns/LSB.
6:0	MFR_OSR_BLANKTIME_R2	Sets the blanking time between two effective overshoot reduction (OSR) events. 10ns/LSB.

READ_CS1_R2 (D0h)

The READ_CS1_R2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS1 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS1_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS1_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS1_R2	Returns the ADC-sensed voltage on rail 2's CS1 pin. 3.125mV/LSB.

READ_CS2_R2 (D1h)

The READ_CS2_R2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS2 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS2_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS2_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS2_R2	Returns the ADC-sensed voltage on rail 2's CS2 pin. 3.125mV/LSB.

READ_CS3_R2 (D2h)

The READ_CS3_R2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS3 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS3_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS3_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS3_R2	Returns the ADC-sensed voltage on rail 2's CS3 pin. 3.125mV/LSB.

READ_CS4_R2 (D3h)

The READ_CS4_R2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS4 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS4_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS4_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS4_R2	Returns the ADC-sensed voltage on rail 2's CS4 pin. 3.125mV/LSB.

READ_CS5_R2 (D4h)

The READ_CS5_R2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS5 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS5_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS5_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS5_R2	Returns the ADC-sensed voltage on rail 2's CS5 pin. 3.125mV/LSB.

READ_CS6_R2 (D5h)

The READ_CS6_R2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS6 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS6_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS6_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS6_R2	Returns the ADC-sensed voltage on rail 2's CS6 pin. 3.125mV/LSB.

READ_CS7_R2 (D6h)

The READ_CS7_R2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS7 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS7_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS7_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS7_R2	Returns the ADC-sensed voltage on rail 2's CS7 pin. 3.125mV/LSB.

READ_CS8_R2 (D7h)

The READ_CS8_R2 command on Page 1 returns the ADC-sensed average voltage on rail 2's CS8 pin in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS8_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_CS8_R2									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	READ_CS8_R2	Returns the ADC-sensed voltage on rail 2's CS1 pin. 3.125mV/LSB.

DIE_TEMP_SENSE (D8h)

The DIE_TEMP_SENSE command on Page 1 returns the die temperature's ADC value.

Command	DIE_TEMP_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	DIE_TEMP_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that reads are always 0.
9:0	DIE_TEMP_SENSE	Returns the die temperature's ADC value. 1.5625mV/LSB. Convert the read value to the actual die temperature (in °C) with the following equation: $$T_{DIE\_TEMP}(°C) = \frac{D8h[9:0] \times 1.5625mV - 275mV}{3}$$

FAULT_REPORT0 (D9h)

The FAULT_REPORT0 command on Page 1 returns some protection information for the MP2882. This information is lost after the device shuts down.

Command	FAULT_REPORT0															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	X	X	X					

Bits	Bit Name	Description
15:5	RESERVED	Unused. X indicates that reads are always 0.
4	TSENS2_DIGITAL_ FAULT	Indicates whether a TSENS2 digital fault has occurred. 1'b0: No TSENS2 digital fault has occurred 1'b1: A TSENS2 digital fault has occurred
3	OTP_DIE	Indicates whether chip over-temperature protection (OTP) has occurred. 1'b0: No chip OTP has occurred 1'b1: Chip OTP has occurred
2	VIN_UVP	V_{IN} under-voltage (UV) fault indicator. If V_{IN} drops below the UV fault limit, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
1	VIN_OVP	V_{IN} over-voltage (OV) fault indicator. If V_{IN} exceeds the OV fault limit (55h on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
0	VIN_UVLO	V_{IN} under-voltage lockout (UVLO) fault indicator. If V_{IN} exceeds the VIN UVLO fault limit, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: V_{IN} is below VIN_OFF 1'b1: V_{IN} is above VIN_ON

FAULT_REPORT1 (DAh)

The FAULT_REPORT1 command on Page 1 returns some protection information for the MP2882. This information is lost after the device shuts down.

Command	FAULT_REPORT1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X								X							

Bits	Bit Name	Description
15	RESERVED_R2	Unused. X indicates that reads are always 0.
14	DRMOS_FAULT_R2	Rail 2 DrMOS fault indicator. 1'b0: No DrMOS fault has occurred 1'b1: A DrMOS fault has occurred. This includes a phase redundancy fault

13	OTP_R2	Rail 2 V_{OUT} over-temperature protection (OTP) indicator. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
12	OCP_TDC_R2	Rail 2 V_{OUT} over-current protection (OCP_TDC) fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred 1'b1: A V_{OUT} OC_TDC fault has occurred
11	OCP_SPIKE_R2	Rail 2 V_{OUT} over-current protection (OCP_SPIKE) fault indicator. 1'b0: No V_{OUT} OCP_SPIKE fault has occurred 1'b1: A V_{OUT} OCP_SPIKE fault has occurred
10	UVP_VID_R2	Rail 2 V_{OUT} VID under-voltage protection (UVP) indicator. 1'b0: No V_{OUT} VID UVP fault has occurred 1'b1: A V_{OUT} VID UVP fault has occurred
9	OVP_VID_R2	Rail 2 V_{OUT} VID over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} VID OVP fault has occurred 1'b1: A V_{OUT} VID OVP fault has occurred
8	OVP_ABS_R2	Rail 2 V_{OUT} ABS OVP indicator. 1'b0: No V_{OUT} ABS OVP fault has occurred 1'b1: A V_{OUT} ABS OVP fault has occurred
7	RESERVED_R1	Unused. X indicates that reads are always 0.
6	DRMOS_FAULT_R1	Rail 1 DrMOS fault indicator. 1'b0: No DrMOS fault has occurred 1'b1: A DrMOS fault has occurred. This includes a phase redundancy fault
5	OTP_R1	Rail 1 V_{OUT} OTP indicator. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
4	OCP_TDC_R1	Rail 1 V_{OUT} OCP_TDC fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred 1'b1: A V_{OUT} OC_TDC fault has occurred
3	OCP_SPIKE_R1	Rail 2 V_{OUT} OCP_SPIKE fault indicator. 1'b0: No V_{OUT} OCP_SPIKE fault has occurred 1'b1: A V_{OUT} OCP_SPIKE fault has occurred
2	UVP_VID_R1	Rail 1 VOUT VID UVP indicator. 1'b0: No V_{OUT} VID UVP fault has occurred 1'b1: A V_{OUT} VID UVP fault has occurred
1	OVP_VID_R1	Rail 1 V_{OUT} VID OVP indicator. 1'b0: No V_{OUT} VID OVP fault has occurred 1'b1: A V_{OUT} VID OVP fault has occurred
0	OVP_ABS_R1	Rail 1 V_{OUT} ABS OVP indicator. 1'b0: No V_{OUT} ABS OVP fault has occurred 1'b1: A V_{OUT} ABS OVP fault has occurred

FAULT_REPORT2 (DBh)

The FAULT_REPORT2 command on Page 1 returns some protection information for the MP2882. This information is lost after the device shuts down.

Command	FAULT_REPORT2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH1				PWM_FAULT_PH2				PWM_FAULT_PH3				PWM_FAULT_PH4			

Bits	Bit Name	Description
15:12	PWM_FAULT_PH1	Intelli-Phase™ fault type indication for phase 1 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM_FAULT_PH2	Intelli-Phase™ fault type indication for phase 2 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM_FAULT_PH3	Intelli-Phase™ fault type indication for phase 3 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM_FAULT_PH4	Intelli-Phase™ fault type indication for phase 4 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULT_REPORT3 (DCh)

The FAULT_REPORT3 command on Page 1 returns some protection information for the MP2882. This information is lost after the device shuts down.

Command	FAULT_REPORT3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH5				PWM_FAULT_PH6				PWM_FAULT_PH7				PWM_FAULT_PH8			

Bits	Bit Name	Description
15:12	PWM_FAULT_PH5	Intelli-Phase™ fault type indication for phase 5 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

11:8	PWM_FAULT_PH6	Intelli-Phase™ fault type indication for phase 6 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM_FAULT_PH7	Intelli-Phase™ fault type indication for phase 7 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM_FAULT_PH8	Intelli-Phase™ fault type indication for phase 8 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULT_REPORT4 (DDh)

The FAULT_REPORT4 command on Page 1 returns some protection information for the MP2882. This information is lost after the device shuts down.

Command	FAULT_REPORT4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH9				PWM_FAULT_PH10				PWM_FAULT_PH11				PWM_FAULT_PH12			

Bits	Bit Name	Description
15:12	PWM_FAULT_PH9	Intelli-Phase™ fault type indication for phase 9 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM_FAULT_PH10	Intelli-Phase™ fault type indication for phase 10 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM_FAULT_PH11	Intelli-Phase™ fault type indication for phase 11 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

3:0	PWM_FAULT_PH12	Intelli-Phase™ fault type indication for phase 12 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULT_REPORT5 (DEh)

The FAULT_REPORT5 command on Page 1 returns some protection information for the MP2882. This information is lost after the device shuts down.

Command	FAULT_REPORT5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH13				PWM_FAULT_PH14				PWM_FAULT_PH15				PWM_FAULT_PH16			

Bits	Bit Name	Description
15:12	PWM_FAULT_PH13	Intelli-Phase™ fault type indication for phase 13 on rail 1 or phase 8 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM_FAULT_PH14	Intelli-Phase™ fault type indication for phase 14 on rail 1 or phase 7 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM_FAULT_PH15	Intelli-Phase™ fault type indication for phase 15 on rail 1 or phase 6 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM_FAULT_PH16	Intelli-Phase™ fault type indication for phase 16 on rail 1 or phase 5 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULT_REPORT6 (DFh)

The FAULT_REPORT6 command on Page 1 returns some protection information for the MP2882. This information is lost after the device shuts down.

Command	FAULT_REPORT6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH4_R2				PWM_FAULT_PH3_R2				PWM_FAULT_PH2_R2				PWM_FAULT_PH1_R2			

Bits	Bit Name	Description
15:12	PWM_FAULT_PH4_R2	Intelli-Phase™ fault type indication for phase 4 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM_FAULT_PH3_R2	Intelli-Phase™ fault type indication for phase 3 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM_FAULT_PH2_R2	Intelli-Phase™ fault type indication for phase 2 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM_FAULT_PH1_R2	Intelli-Phase™ fault type indication for phase 1 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULT_TIME0 (E0h)

The FAULT_TIME0, FAULT_TIME1, and FAULT_TIME2 commands on Page 1 record the time information if a fault occurs.

Command	FAULT_TIME0															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	FAULT_TIME0															

Bits	Bit Name	Description
15:0	FAULT_TIME0	Records and saves the time when the first fault occurs using 3 storage cells: FAULT_TIME0, FAULT_TIME1, and FAULT_TIME2. When writing to FAULT_TIME0, the data sets stored in FAULT_TIME1 and FAULT_TIME 2 are reset simultaneously. FAULT_TIME0 saves the year, date, and month information. FAULT_TIME1 is the 8MSB of the accumulator. FAULT_TIME2 is the 16LSB of the accumulator. The write data is 16 bits to record the time information with DD (day), MM (month), and YY (year). Once the accumulator starts to work, FAULT_TIME0 cannot be modified via this register, and it must be changed via the NVM. 1sec/step.

FAULT_TIME1 (E1h)

The FAULT_TIME0, FAULT_TIME1 and FAULT_TIME2 commands on Page 1 record the time information if a fault occurs. FAULT_TIME1 is the 8MSB of the accumulator.

Command	FAULT_TIME1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	FAULT_TIME1							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	FAULT_TIME1	Records and stores the time when a fault occurs. FAULT_TIME0 saves the year, date, and month information. FAULT_TIME1 is the 8MSB of the accumulator. FAULT_TIME2 is the 16LSB of the accumulator. The timer starts to work during start-up. When writing to FAULT_TIME0, the data sets stored in FAULT_TIME1 and FAULT_TIME 2 are reset simultaneously.

FAULT_TIME2 (E2h)

The FAULT_TIME0, FAULT_TIME1 and FAULT_TIME2 commands on Page 1 record the time information if a fault occurs. FAULT_TIME2 is the 16LSB of the accumulator.

Command	FAULT_TIME2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	FAULT_TIME2															

Bits	Bit Name	Description
15:0	FAULT_TIME2	Records and stores the time when a fault occurs. FAULT_TIME0 saves the year, date, and month information. FAULT_TIME1 is the 8MSB of the accumulator. FAULT_TIME2 is the 16LSB of the accumulator. The timer starts to work during start-up. When writing to FAULT_TIME0, the data sets stored in FAULT_TIME1 and FAULT_TIME 2 are reset simultaneously.

FAULT_IMON1_SENSE (E3h)

The FAULT_IMON1_SENSE command on Page 1 records the IMON1-sensed value when the first fault occurs.

Command	FAULT_IMON1_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	FAULT_IMON1_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	FAULT_IMON1_SENSE	Returns the IMON1 value when the first fault occurs.

FAULT_IMON2_SENSE (E4h)

The FAULT_IMON2_SENSE command on Page 1 records the IMON2-sensed value when the first fault occurs.

Command	FAULT_IMON2_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	FAULT_IMON2_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	FAULT_IMON2_SENSE	Returns the IMON2 value when the first fault occurs.

FAULT_VDIFF1_SENSE (E5h)

The FAULT_VDIFF1_SENSE command on Page 1 records the VDIFF1-sensed value when the first fault occurs.

Command	FAULT_VDIFF1_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	FAULT_VDIFF1_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	FAULT_VDIFF1_SENSE	Returns the VDIFF1 value when the first fault occurs.

FAULT_VDIFF2_SENSE (E6h)

The FAULT_VDIFF2_SENSE command on Page 1 records the VDIFF2-sensed value when the first fault occurs.

Command	FAULT_VDIFF2_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	FAULT_VDIFF2_SENSE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X that indicates that writes are ignored and reads are always 0.
9:0	FAULT_VDIFF2_SENSE	Returns the VDIFF2 value when the first fault occurs.

FAULT_VIN_SENSE (E7h)

The FAULT_VIN_SENSE command on Page 1 records the V_{IN}-sensed value when the first fault occurs.

Command	FAULT_VIN_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits	Bit Name	Description
15:10	RESERVED	Unused. X that indicates that writes reads are always 0.
9:0	FAULT_VIN_SENSE	Returns the V_{IN} value when the first fault occurs.

FAULT_FIRST_RECORD (E8h)

The FAULT_FIRST_RECORD command on Page 1 records the first protection type. For example, if over-current protection (OCP) occurs and is followed by under-voltage protection (UVP) and V_{IN} under-voltage lockout (UVLO), then OCP is recorded to this register.

Command	FAULT_FIRST_RECORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15	VIN_UVLO	Indicates whether the first fault is V_{IN} under-voltage lockout (UVLO). 1'b0: V_{IN} UVLO is not the first fault 1'b1: V_{IN} UVLO is the first fault
14	VIN_OVP	Indicates whether the first fault is V_{IN} over-voltage protection (OVP). 1'b0: V_{IN} OVP is not the first fault 1'b1: V_{IN} OVP is the first fault
13	TSENS2_DIGI_FAULT	Indicates whether the first fault is a TSENS2 digital fault. 1'b0: A TSENS2 digital fault is not the first fault 1'b1: A TSENS2 digital fault is the first fault
12	TSENS2_FAULT	Indicates whether the first fault is a TSENS2 fault. 1'b0: TSENS2 is not the first fault 1'b1: TSENS2 is the first fault
11	TSENS1_FAULT	Indicates whether the first fault is a TSENS1 fault. 1'b0: TSENS1 is not the first fault 1'b1: TSENS1 is the first fault
10	OTP_DIE	Indicates whether the first fault is chip over-temperature protection (OTP). 1'b0: Chip OTP is not the first fault 1'b1: Chip OTP is the first fault
9	OTP_R2	Indicates whether the first fault is rail 2 OTP. 1'b0: An OTP fault on rail 2 is not the first fault 1'b1: An OTP fault on rail 2 is the first fault
8	OTP_R1	Indicates whether the first fault is rail 1 OTP. 1'b0: An OTP fault on rail 1 is not the first fault 1'b1: An OTP fault on rail 1 is the first fault
7	UVP_R2	Indicates whether the first fault is rail 2 V_{OUT} under-voltage protection (UVP). 1'b0: A V_{OUT} UVP fault on rail 2 is not the first fault 1'b1: A V_{OUT} UVP fault on rail 2 is the first fault
6	UVP_R1	Indicates whether the first fault is rail 1 V_{OUT} UVP. 1'b0: A V_{OUT} UVP fault on rail 1 is not the first fault 1'b1: A V_{OUT} UVP fault on rail 1 is the first fault

5	OVP_R2	Indicates whether the first fault is rail 2 V_{OUT} OVP. 1'b0: A V_{OUT} OVP fault on rail 2 is not the first fault 1'b1: A V_{OUT} OVP fault on rail 2 is the first fault
4	OVP_R1	Indicates whether the first fault is rail 1 V_{OUT} OVP. 1'b0: A V_{OUT} OVP fault on rail 1 is not the first fault 1'b1: A V_{OUT} OVP fault on rail 1 is the first fault
3	OCP_R2	Indicates whether the first fault is rail 2 V_{OUT} over-current protection (OCP_TDC). 1'b0: A V_{OUT} OCP_TDC fault on rail 2 is not the first fault 1'b1: A V_{OUT} OCP_TDC fault on rail 2 is the first fault
2	OCP_R1	Indicates whether the first fault is rail 1 V_{OUT} OCP_TDC. 1'b0: A V_{OUT} OCP_TDC fault on rail 1 is not the first fault 1'b1: A V_{OUT} OCP_TDC fault on rail 1 is the first fault
1	DRMOS_FAULT_R2	Indicates whether the first fault is a rail 2 DrMOS fault. 1'b0: A DrMOS fault on rail 2 is not the first fault 1'b1: A DrMOS fault on rail 2 is the first fault
0	DRMOS_FAULT_R1	Indicates whether the first fault is a rail 1 DrMOS fault. 1'b0: A DrMOS fault on rail 1 is not the first fault 1'b1: A DrMOS fault on rail 1 is the first fault

FAULT_RECORD0 (E9h)

The FAULT_RECORD0 command on Page 1 records if a fault occurred on rail 1 or rail 2 when the MP2882 was last turned on.

Command	FAULT_RECORD0															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	X	X						

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5	RESERVED	Reserved.
4	TSENS2_DIGI_FAULT	TSENS2 digital fault indicator. 1'b0: No TSENS2 digital fault 1'b1: A TSENS2 digital fault has occurred
3	OTP_DIE	Chip over-temperature protection (OTP) indicator. 1'b0: No chip OTP has occurred 1'b1: Chip OTP has occurred
2	VIN_UVP	V_{IN} under-voltage (UV) fault indicator. If the sensed V_{IN} drops below the UV limit, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
1	VIN_OVP	V_{IN} over-voltage (OV) fault indicator. If V_{IN} exceeds the VIN_OV fault limit (55h on Page 0), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred

0	VIN_UVLO	V_{IN} under-voltage lockout (UVLO) indicator. If V_{IN} drops below VIN_OFF, this bit is set. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: V_{IN} has exceeded VIN_ON 1'b1: V_{IN} is below VIN_OFF

FAULT_RECORD1 (EAh)

The FAULT_RECORD1 command on Page 1 records if a fault occurred on rail 1 or rail 2 when the MP2882 was last turned on.

Command	FAULT_RECORD1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X								X							

Bits	Bit Name	Description
15	RESERVED_R2	Unused. X indicates that writes are ignored and reads are always 0.
14	DRMOS_FAULT_R2	Rail 2 DrMOS fault indicator. 1'b0: No DrMOS fault has occurred 1'b1: A DrMOS fault has occurred. This includes a phase redundancy fault
13	OTP_R2	Rail 2 V_{OUT} over-temperature protection (OTP) indicator. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred
12	OCP_TDCR2	Rail 2 V_{OUT} over-current protection (OCP_TDC) fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred 1'b1: A V_{OUT} OC_TDC fault has occurred
11	OCP_SPIKER2	Rail 2 V_{OUT} over-current protection (OCP_SPIKE) fault indicator. 1'b0: No V_{OUT} OCP_SPIKE fault has occurred 1'b1: A V_{OUT} OCP_SPIKE fault has occurred
10	UVP_VID_R2	Rail 2 VOUT VID under-voltage protection (UVP) indicator. 1'b0: No V_{OUT} VID UVP fault has occurred 1'b1: A V_{OUT} VID UVP fault has occurred
9	OVP_VID_R2	Rail 2 V_{OUT} VID over-voltage protection (OVP) indicator. 1'b0: No V_{OUT} VID OVP fault has occurred 1'b1: A V_{OUT} VID OVP fault has occurred
8	OVP_ABS_R2	Rail 2 V_{OUT} ABS OVP indicator. 1'b0: No V_{OUT} ABS OVP fault has occurred 1'b1: A V_{OUT} ABS OVP fault has occurred
7	RESERVED_R1	Unused. X indicates that writes are ignored and reads are always 0.
6	DRMOS_FAULT_R1	Rail 1 DrMOS fault indicator. 1'b0: No DrMOS fault has occurred 1'b1: A DrMOS fault has occurred. This includes a phase redundancy fault
5	OTP_R1	Rail 1 V_{OUT} OTP indicator. 1'b0: No OTP fault has occurred 1'b1: An OTP fault has occurred

4	OCP_TDCR1	Rail 1 V_{OUT} OCP_TDC fault indicator. 1'b0: No V_{OUT} OC_TDC fault has occurred 1'b1: A V_{OUT} OC_TDC fault has occurred
3	OCP_SPIKER1	Rail 2 V_{OUT} OCP_SPIKE fault indicator. 1'b0: No V_{OUT} OCP_SPIKE fault has occurred 1'b1: A V_{OUT} OCP_SPIKE fault has occurred
2	UVP_VID_R1	Rail 1 V_{OUT} VID UVP indicator. 1'b0: No V_{OUT} VID UVP fault has occurred 1'b1: A V_{OUT} VID UVP fault has occurred
1	OVP_VID_R1	Rail 1 V_{OUT} VID OVP indicator. 1'b0: No V_{OUT} VID OVP fault has occurred 1'b1: A V_{OUT} VID OVP fault has occurred
0	OVP_ABS_R1	Rail 1 V_{OUT} ABS OVP indicator. 1'b0: No V_{OUT} ABS OVP fault has occurred 1'b1: A V_{OUT} ABS OVP fault has occurred

FAULT_RECORD2 (EBh)

The FAULT_RECORD2 command on Page 1 records the first time fault type happened on rail1 and rail2 for the MP2882 happened in the last time.

Command	FAULT_RECORD2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH1				PWM_FAULT_PH2				PWM_FAULT_PH3				PWM_FAULT_PH4			

Bits	Bit Name	Description
15:12	PWM_FAULT_PH1	Intelli-Phase™ fault type indication for phase 1 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM_FAULT_PH2	Intelli-Phase™ fault type indication for phase 2 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM_FAULT_PH3	Intelli-Phase™ fault type indication for phase 3 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM_FAULT_PH4	Intelli-Phase™ fault type indication for phase 4 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULT_RECORD3 (ECh)

The FAULT_RECORD3 command on Page 1 records the first time fault type happened on rail1 and rail2 for the MP2882 happened in the last time.

Command	FAULT_RECORD3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH5				PWM_FAULT_PH6				PWM_FAULT_PH7				PWM_FAULT_PH8			

Bits	Bit Name	Description
15:12	PWM_FAULT_PH5	Intelli-Phase™ fault type indication for phase 5 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM_FAULT_PH6	Intelli-Phase™ fault type indication for phase 6 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM_FAULT_PH7	Intelli-Phase™ fault type indication for phase 7 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM_FAULT_PH8	Intelli-Phase™ fault type indication for phase 8 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

FAULT_RECORD4 (EDh)

The FAULT_RECORD3 command on Page 1 records the first time fault type happened on rail1 and rail2 for the MP2882 happened in the last time.

Command	FAULT_RECORD4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH9				PWM_FAULT_PH10				PWM_FAULT_PH11				PWM_FAULT_PH12			

Bits	Bit Name	Description
15:12	PWM_FAULT_PH9	Intelli-Phase™ fault type indication for phase 9 on rail 1. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM_FAULT_PH10	Intelli-Phase™ fault type indication for phase 10 on rail 1.

		4’b0000: No fault 4’b0001: VIN-SW short protection 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
7:4	PWM_FAULT_PH11	Intelli-Phase™ fault type indication for phase 11 on rail 1. 4’b0000: No fault 4’b0001: VIN-SW short protection 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
3:0	PWM_FAULT_PH12	Intelli-Phase™ fault type indication for phase 12 on rail 1. 4’b0000: No fault 4’b0001: VIN-SW short protection 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection

FAULT_RECORD5 (EFh)

The FAULT_RECORD5 command on Page 1 records the first time fault type happened on rail1 and rail2 for the MP2882 happened in the last time.

Command	FAULT_RECORD5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH13				PWM_FAULT_PH14				PWM_FAULT_PH15				PWM_FAULT_PH16			

Bits	Bit Name	Description
15:12	PWM_FAULT_PH13	Intelli-Phase™ fault type indication for phase 13 on rail 1 or phase 8 on rail 2. 4’b0000: No fault 4’b0001: VIN-SW short protection 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
11:8	PWM_FAULT_PH14	Intelli-Phase™ fault type indication for phase 14 on rail 1 or phase 7 on rail 2. 4’b0000: No fault 4’b0001: VIN-SW short protection 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
7:4	PWM_FAULT_PH15	Intelli-Phase™ fault type indication for phase 15 on rail 1 or phase 6 on rail 2. 4’b0000: No fault 4’b0001: VIN-SW short protection 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection
3:0	PWM_FAULT_PH16	Intelli-Phase™ fault type indication for phase 16 on rail 1 or phase 5 on rail 2. 4’b0000: No fault 4’b0001: VIN-SW short protection 4’b0010: Current limit protection 4’b0100: Over-temperature protection 4’b1000: SW-PGND short protection

FAULT_RECORD6 (EFh)

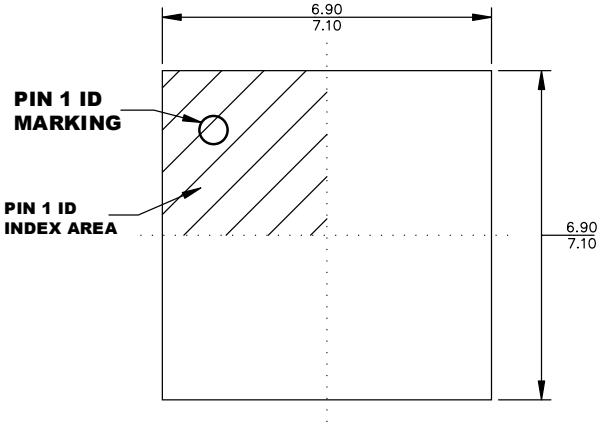
The FAULT_RECORD5 command on Page 1 records the first time fault type happened on rail1 and rail2 for the MP2882 happened in the last time.

Command	FAULT_RECORD6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM_FAULT_PH4_R2				PWM_FAULT_PH3_R2				PWM_FAULT_PH2_R2				PWM_FAULT_PH1_R2			

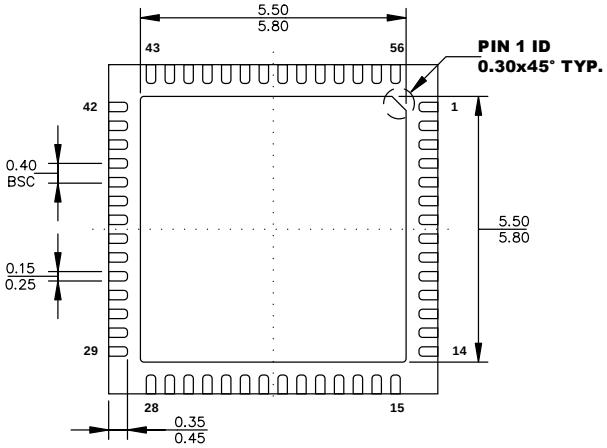
Bits	Bit Name	Description
15:12	PWM_FAULT_PH4_R2	Intelli-Phase™ fault type indication for phase 4 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM_FAULT_PH3_R2	Intelli-Phase™ fault type indication for phase 3 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM_FAULT_PH2_R2	Intelli-Phase™ fault type indication for phase 2 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM_FAULT_PH1_R2	Intelli-Phase™ fault type indication for phase 1 on rail 2. 4'b0000: No fault 4'b0001: VIN-SW short protection 4'b0010: Current limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

PACKAGE INFORMATION

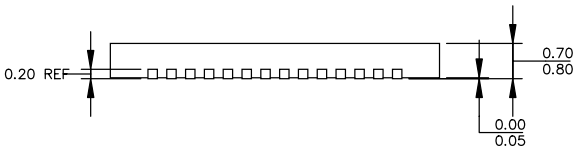
TQFN-56 (7mmx7mm)



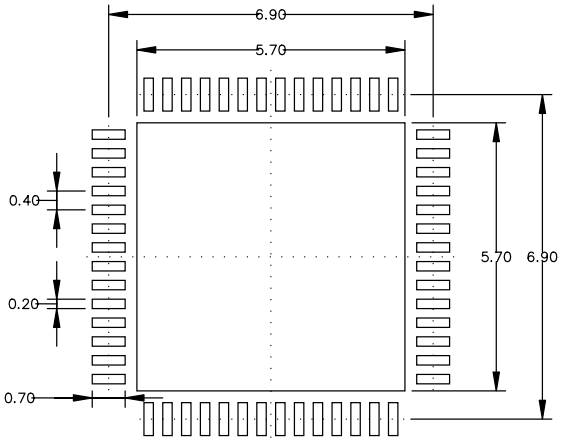
TOP VIEW



BOTTOM VIEW



SIDE VIEW

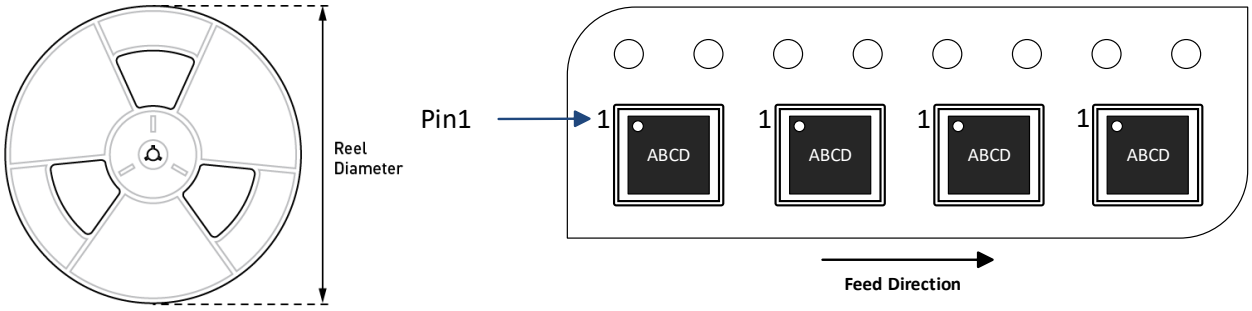


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2882GQNT-xxxx–Z	TQFN-56 (7mmx7mm)	2500	N/A	N/A	N/A	13in	16mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/4/2021	Initial Release	-