MP2853

Dual-Loop, Digital, Multi-Phase Controller with PMBus™ Interface for AMD SVI2

The Future of Analog IC Technology

DESCRIPTION

The MP2853 is a dual-loop, digital, multi-phase controller that provides power for the core of the AMD SVI 2.0 platform. The MP2853 can work with MPS Intelli-Phase products to complete the multi-phase voltage regulator (VR) solution with minimal external components. The MP2853 can be configured with up to 4-phase operation for Rail 1 and up to 2-phase operation for Rail 2.

The MP2853 provides an on-chip EEPROM to store and restore device configurations. Device configurations and fault parameters can be programmed easily or monitored via the PMBus™/I²C interface. The MP2853 can monitor and report output current through the CS output from Intelli-Phase products.

The MP2853 is based on a unique, digital, multi-phase, non-linear control to provide fast transient response to the load transient with minimal output capacitors. With only one power-loop control method for both steady state and load transient, the power loop compensation is very easy to configure.

The MP2853 is available in a QFN-40 (5mmx5mm) package.

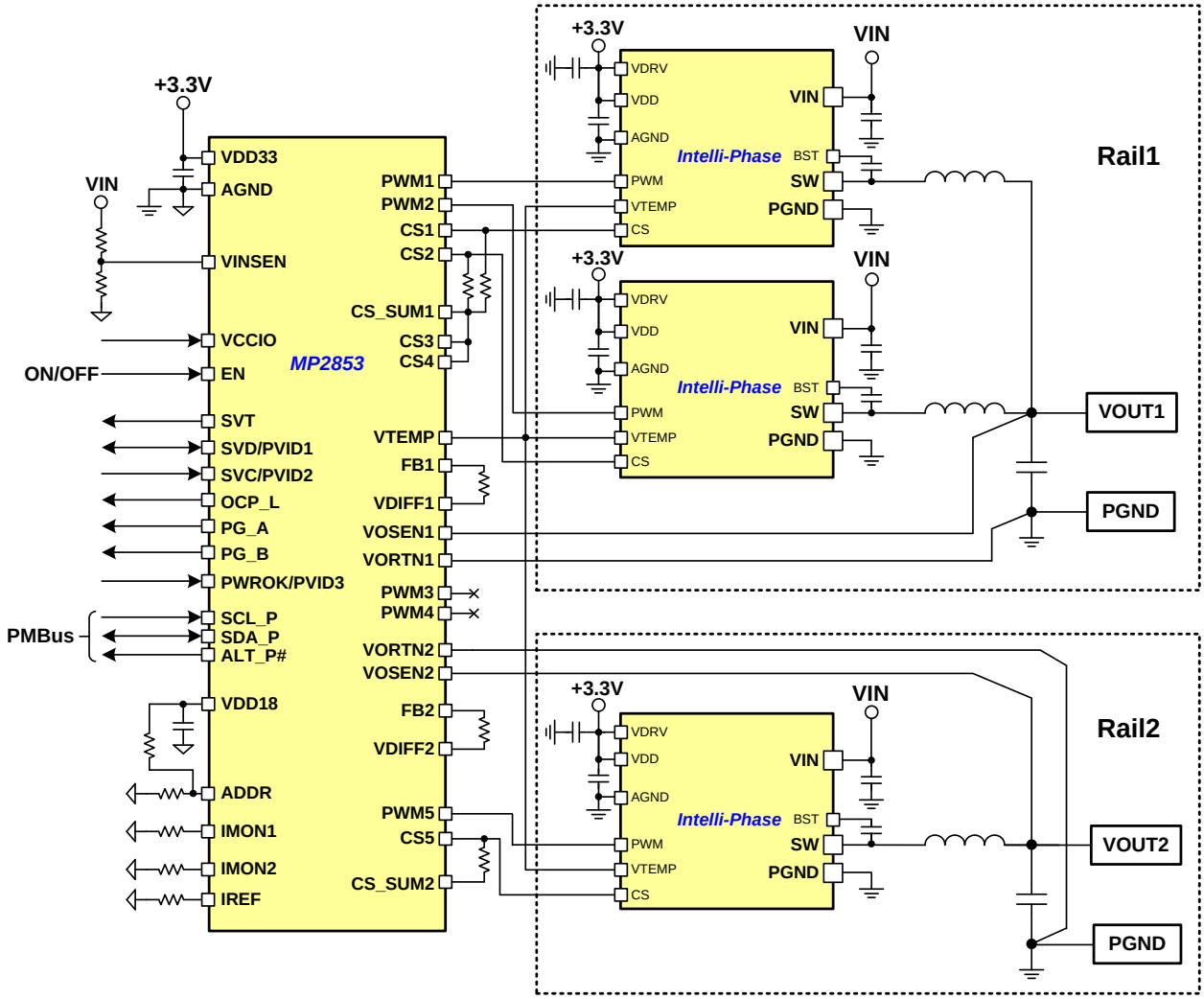
FEATURES

- Multi-Phase, Dual-Output, Digital Controller
- AMD SVI 2.0 Compliant
- Supports 3-Bit PVID Mode
- PMBus™/I²C Compliant (1MHz Bus Speed)
- Pin Programmable for PMBus™ Address
- Built-In EEPROM to Store Custom Configurations
- Switching Frequency Range from 200kHz to 3MHz
- Digital Load-Line Regulation
- Over-Clocking Mode by Adding Offset to Output Voltage
- Automatic Loop Compensation
- Fewer External Components than a Conventional Analog Controller
- Best Transient Performance with Non-Linear Digital Control
- Flexible Phase Assignment for Dual Rails
- Auto-Phase Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing with Programmable Offsets for Thermal Balance
- Input and Output Voltage, Current, and Power Monitoring
- Regulator Temperature Monitoring
- V_{IN} UVLO, Output OVP/UVP, OCP_TDC/OCP_SPIKE, OTP with No Action, Latch, Retry, or Hiccup Options
- Detection for Intelli-Phase MOSFET Fault Type
- Auto-Recording VR Fault Type to EEPROM
- Available in an RoHS Compliant QFN-40 (5mmx5mm) Package

APPLICATIONS

- AMD Fusion CPU/GPU Core Power
- DDR
- Telecom and Networking Systems
- Base Stations

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2853GU-xxxx**	QFN-40 (5mmx5mm)	*See Below*

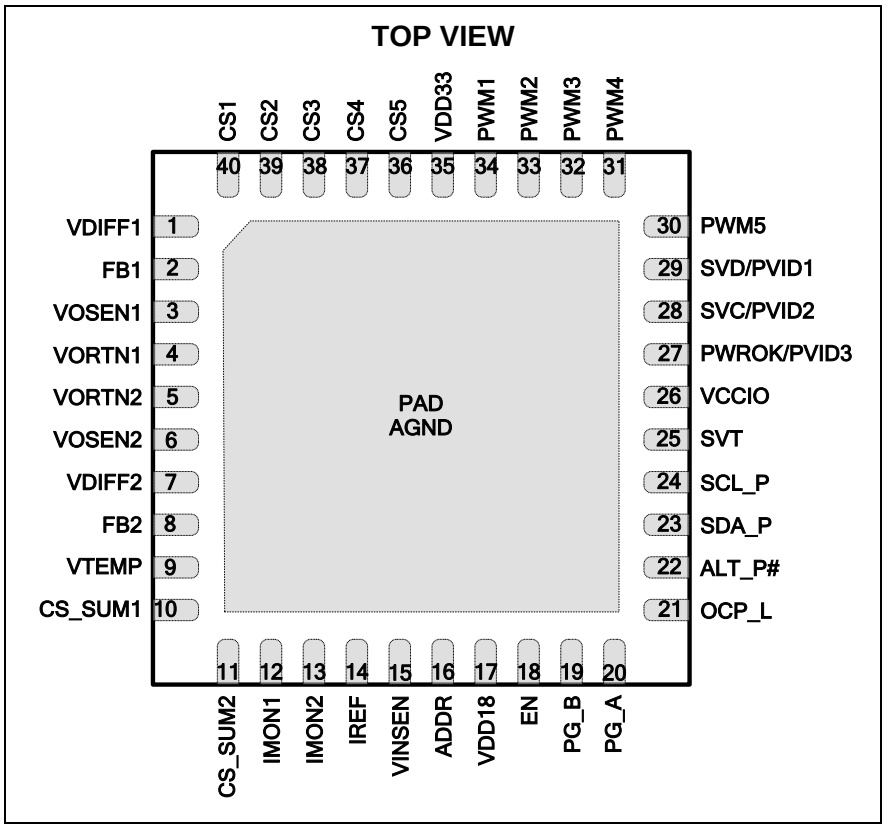
* For Tape & Reel, add suffix –Z (e.g. MP2853GU-xxxx–Z)
** "xxxx" is the configuration code identifier for the register settings stored in the EEPROM. To create a unique value for this code, please contact an MPS FAE.

TOP MARKING

MPSYYWW
MP2853
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2853: First six digits of the part number
LLLLLLL: Lot number

PACKAGE REFERENCE



QFN-40 (5mmx5mm)

ABSOLUTE MAXIMUM RATINGS (1)

VDD33 .....-0.3V to +4.0V
VDD18 .....-0.3V to +2.2V
CS1/2/3/4/5, PWM1/2/3/4/5, FB1/2, VDIFF1/2, VOSEN1/2, VORTN1/2, PWROK, PG_A, PG_B, OCP_L, SCL_P, SDA_P, ALT_P#, EN, VCCIO, SVC, SVD, SVT, VTEMP.....-0.3V to +4.0V
IMON1/2, IREF, VINSEN, ADDR.....
.....-0.3V to +2.2V
CS_SUM1/2.....-0.3V to +2.0V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (2)..... 3.47W

Recommended Operating Conditions (3)

Supply voltage (VDD33) .....+3.0V to 3.6V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-40 (5mmx5mm) .....36……..5…..°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 6-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD33 = 3.3V, EN = 3.3V, T_A = -40°C to +125°C, current going into the pin is positive.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Remote Sense Amplifier						
Bandwidth (5)	$GBW_{(RSA)}$			20		MHz
VORTN1/2 current	$I_{RTN1,2}$	EN = 1V, VOSEN1/2 = 3V, VORTN1/2= 0V	-60	-40		µA
VOSEN1/2 current	$I_{VOSEN1,2}$	EN = 1V, VOSEN1/2 = 3V, VORTN1/2 = 0V		40	60	µA
Oscillator						
Frequency	f_{OSC}	V_{IREF} = 1.23V, R_{IREF} = 61.9kΩ T_A = 25°C	1.4	1.47	1.55	MHz
Enable (EN)						
Input low voltage	$V_{IL(EN)}$				0.8	V
Input high voltage	$V_{IH(EN)}$		2			V
Enable high leakage	$I_{IH(EN)}$	EN = 3.3V			5	µA
OCP_L, PG_A, PG_B						
Output low voltage at I_{OL}	V_{OL}	Sink current 4mA	0		0.2	V
Off-state leakage current	I_{LKG}	Apply 3.3V on pin			1	µA
IMON1, IMON2 Output						
Current gain	I_{MON}/I_{CS_SUM}	I_{CS_SUM} = 2mA		1/16		µA/µA
I_{MON}/I_{CS_SUM} accuracy		I_{CS_SUM} = 2mA	-1		1	%
PWM Comparator (Rail 1/2) (5)						
Propagation delay	t_{PD}			10		ns
Common mode range			0		1.6	V
VFB- Window Comparator (Rail 1/2, VFB = VDAC - 25mV)						
Propagation delay (5)	t_{PD}			10		ns
Common mode range			0		1.6	V
VFB+ Window Comparator (Rail 1/2, VFB = VDAC + 20mV)						
Propagation delay (5)	t_{PD}			10		ns
Common mode range			0		1.6	V
UVP, OVP Comparator (Rail 1/2, Protection)						
Under-voltage threshold	$V_{TH\ (UV)}$	Relative to VID DAC output voltage, V_{REF}	-300	-325	-350	mV
Over-voltage threshold	$V_{TH\ (OV)}$	Relative to VID DAC output voltage, V_{REF}	300	325	350	mV
CS Fault Comparator (CS1 ~ CS5, Protection)						
CS fault threshold	$V_{TH\ (CS\ FLT)}$		120	170	220	mV
VTEMP Fault Comparator (Protection)						
VTEMP fault threshold	$V_{TH\ (VTEMP\ FLT)}$		2	2.2	2.4	mV

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, T_A = -40°C to +125°C, current going into the pin is positive.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM Outputs (PWM1 ~ PWM5)						
Output low voltage	$V_{OL\ (PWM)}$	$I_{PWM(SINK)}$ = 400µA		100	200	mV
Output high voltage	$V_{OH\ (PWM)}$	$I_{PWM(SOURCE)}$ = -400µA	3.1	VDD33 - 0.02		V
Rise and fall time (5)		C = 10pF		10		ns
PWM tri-state leakage		PWM = 1.5V, EN = 0V	-1		1	µA
PWM fault detection source current (5)	$I_{source(PWM)}$	Enter PWM fault detect mode		150		µA
VDD33 Supply						
Supply current	I_{VDD33}	EN = high or programmed as regular power mode		34	37	mA
		EN = 0 and programmed as low power mode		110	700	µA
VDD33 UVLO threshold voltage rising	VDD_{VTH}	VDD33 is rising		2.86	2.95	V
VDD33 UVLO threshold voltage falling	VDD_{VTL}	VDD33 is falling	2.65	2.82		V
VDD33 UVLO hysteresis	VDD_{HYS}			40		mV
1.8V Regulator						
1.8V regulator output voltage	VDD18	I_{VDD18} = 0mA	1.782	1.8	1.818	V
1.8V regulator load capability	I_{VDD18}	VOL = VDD18 - 40mV		30		mA
SVI Interface (5)						
VCCIO operating range	VCCIO		1.14		1.95	V
Input high voltage	V_{IH_DC}	SVC, SVD, PWROK	0.7 (VCCIO)		VCCIO	
	V_{IH_AC}	SVC, SVD, PWROK			VCCIO + 0.5	V
Input low voltage	V_{IL_DC}	SVC, SVD, PWROK	0		0.35 (VCCIO)	V
	V_{IL_AC}	SVC, SVD, PWROK	-0.5			V
Input hysteresis voltage	$V_{TH\ HYS}$	SVC, SVD, PWROK	0.1 (VCCIO)			V
Output high voltage	V_{OH_DC}	SVT	VCCIO - 0.2		VCCIO	V
Output low voltage	V_{OL_DC}	SVT	0		0.2	V
Input leakage	$I_{L\ (VR)}$	SVC, SVD, PWROK	-100		100	µA

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, T_A = -40°C to +125°C, current going into the pin is positive.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SVI Interface (5)						
Output leakage high impedance	$I_{OZ(VR)}$	SVD	-100		100	µA
Output current when driving V_{OH}	I_{OH}	SVT	4			mA
Input current when driving V_{OL}	I_{OL}	SVC, SVD	4			mA
Pad capacitance	C_{PAD}	SVC, SVD, SVT			4	pF
Input pin capacitance	C_{PIN}	SVC, SVD			5	pF
ADC						
Voltage range			0		1.6	V
ADC resolution				10		bits
DNL					1	LSB
Sample rate (5)				780		kHz
VID-DAC (Reference Voltage for Rail 1/2)						
Range	FS_{ADC}			1.55		V
Resolution/LSB	Δ_{ADC}			6.25		mV
Max output voltage slew rate (5)				50		mV/µs
V_{OUT} DC Loop DAC (V_{OUT} Calibration for Rail 1/2) (5)						
Range	FS_{DAC_VO}			350		mV
Resolution	Δ_{DAC_VO}			8		bits
OCP_PHASE DAC (Rail 1/2 Protection)						
Range	FS_{DAC_PRT}	Adjustable via the PMBus™	0.17		2.72	V
Resolution/LSB	Δ_{DAC_PRT}			10		mV
OCP_SPIKE DAC (Rail1/2 OCP_SPIKE Protection) (5)						
Range	FS_{DAC_PRT}	Adjustable via the PMBus™			80	µA
Resolution/LSB	Δ_{DAC_PRT}			1.25		µA
OCP_TDC DAC (Rail1/2 OCP_TDC Protection) (5)						
Range	FS_{DAC_PRT}	Adjustable via the PMBus™			80	µA
Resolution/LSB	Δ_{DAC_PRT}			1.25		µA

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 3.3V, T_A = -40°C to +125°C, current going into the pin is positive.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PMBus™ DC Characteristics (ALT_P, SDA_P, SCL_P)						
Input high voltage	V_{IH}	SCL_P, SDA_P	2.1			V
Input low voltage	V_{IL}	SCL_P, SDA_P			0.8	V
Input leakage current		SCL_P, SDA_P, ALT_P	-10		10	µA
Output low voltage	V_{OL}	ALT_P, sink 2mA			400	mV
Maximum voltage	V_{MAX}	Transient voltage including ringing	-0.3	3.3	3.6	V
Pin capacitance (5)	C_{PIN}				10	pF
PMBus™ Timing Characteristics (1MHz) (5) (6)						
Operating frequency range			10		1000	kHz
Bus free time		Between stop and start condition	0.5			µs
Holding time			0.26			µs
Repeated start condition set-up time			0.26			µs
Stop condition set-up time			0.26			µs
Data hold time			0			ns
Data set-up time			50			ns
Clock low time-out			25		35	ms
Clock low period			0.5			µs
Clock high period			0.26		50	µs
Clock/data fall time					120	ns
Clock/data rise time					120	ns

NOTES:

5) Guaranteed by design or characterization data, not tested in production.

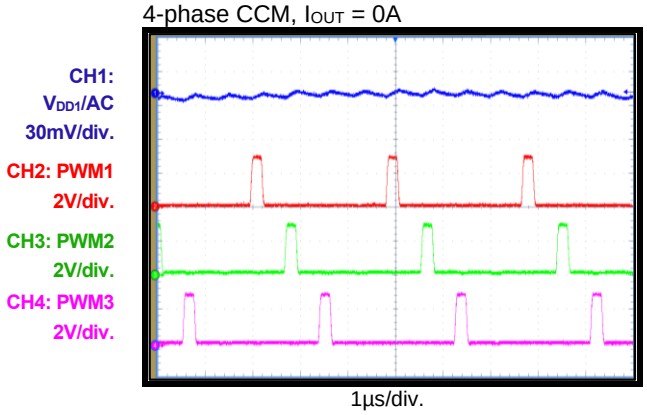
6) The device supports 100kHz, 400kHz, and 1MHz bus speeds. The PMBus™ timing parameters in this table are for operation at 1MHz. If the PMBus™ operating frequency is 100kHz and 400kHz, refer to the SMBus specification for timing parameters.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{DD1} = V_{DD2} = 1V, F_{SW1} = F_{SW2} = 700kHz, VDD33 = 3.3V, 4 + 1 phase mode, T_A = 25°C, unless otherwise noted.

Steady State

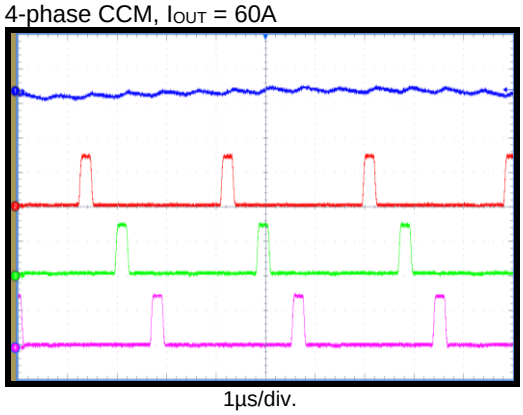
V_{IN} = 12V, V_{DD1} = 1V, F_{SW1} = 700kHz, 4-phase CCM, I_{OUT} = 0A



1µs/div.

Steady State

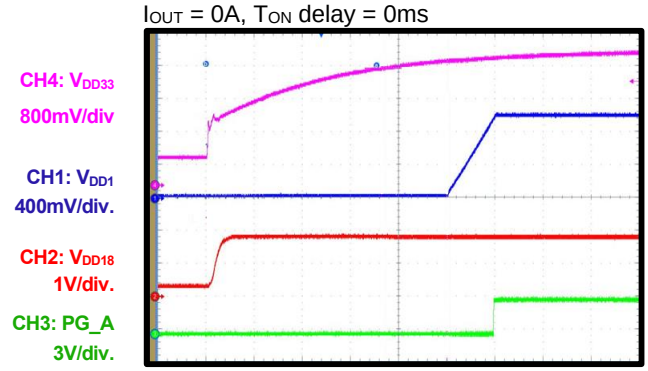
V_{IN} = 12V, V_{DD1} = 1V, F_{SW1} = 700kHz, 4-phase CCM, I_{OUT} = 60A



1µs/div.

VDD33 Power On

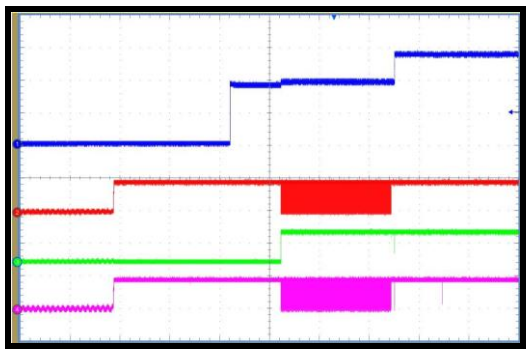
V_{IN} = 12V, V_{DD1} = 1V, soft-start time=1ms, I_{OUT} = 0A, T_{ON} delay = 0ms



1ms/div.

Boot-Up Sequence in SVI Mode

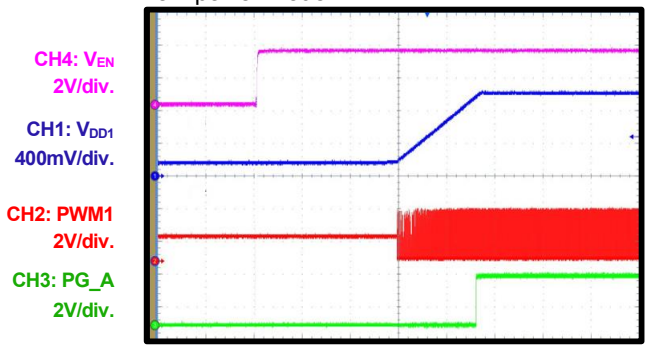
V_{BOOT} = 0.9V



200ms/div.

EN Power On

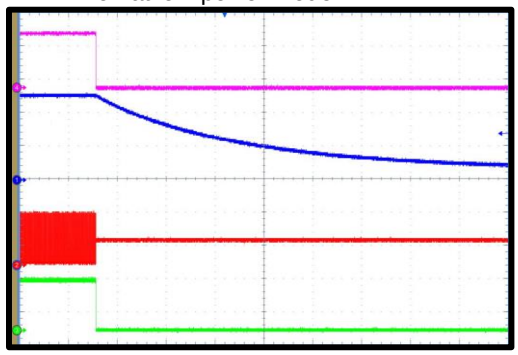
V_{IN} = 12V, V_{DD1} = 1V, soft-start time = 1ms, Low-power mode



500µs/div.

EN Power Off

V_{IN} = 12V, V_{DD1} = 1V, Io = 0A, EN Hi-Z off at low-power mode



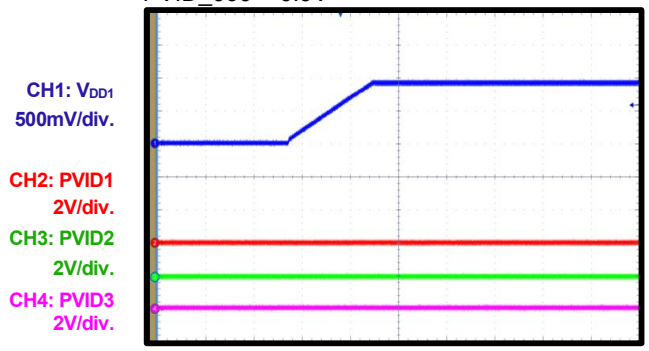
1s/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{DD1} = V_{DD2} = 1V, F_{SW1} = F_{SW2} = 700kHz, VDD33 = 3.3V, 4 + 1 phase mode, T_A = 25°C, unless otherwise noted.

PVID Mode Boot-Up

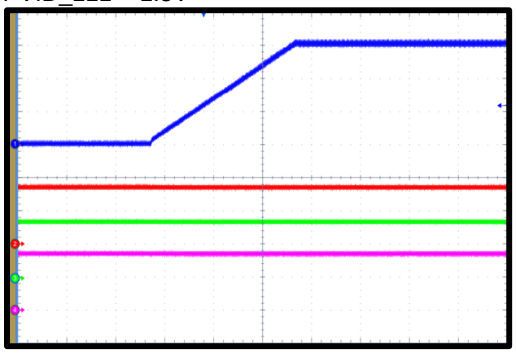
V_{IN} = 12V, PVID1 = PVID2 = PVID3 = 0,
PVID_000 = 0.9V



500µs/div.

PVID Mode Boot-Up

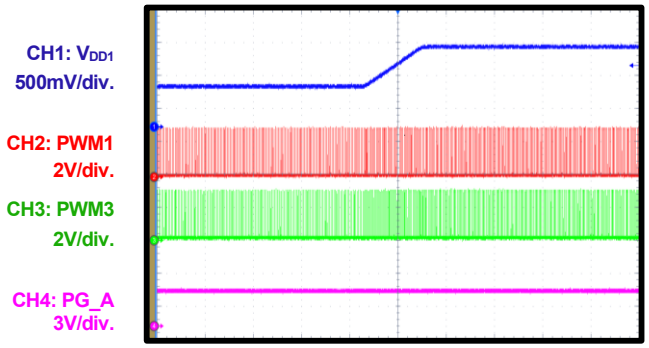
V_{IN} = 12V, PVID1 = PVID2 = PVID3 = 1,
PVID_111 = 1.5V



500µs/div.

DVID Up

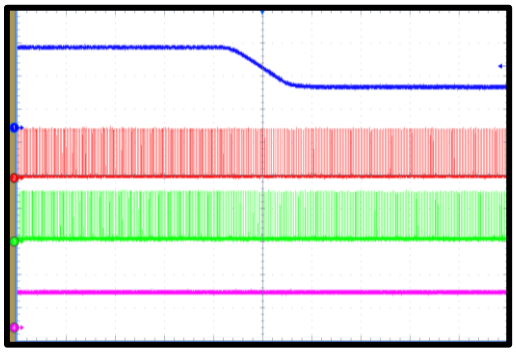
DVID from 0.6V to 1.2V, SR = 10.4mV/µs



500µs/div.

DVID Down

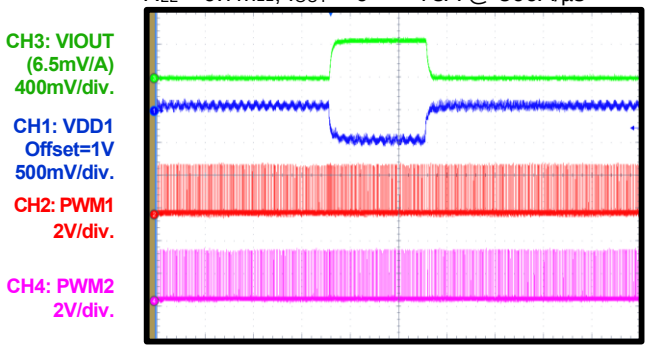
DVID from 1.2V to 0.6V, SR = 10.4mV/µs



50µs/div.

Load Transient with DC Load Line

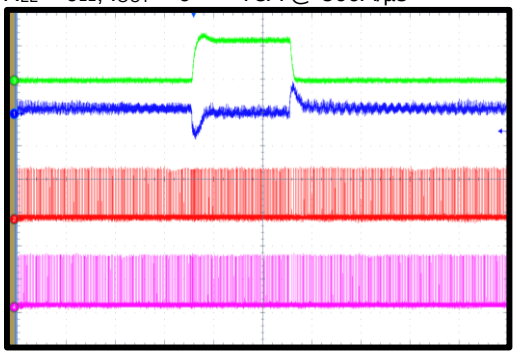
V_{IN} = 12V, V_{DD1} = 1V, F_{SW1} = 700kHz,
R_{LL} = 0.7mΩ, I_{OUT} = 0 <-> 73A @ 500A/µs



50µs/div.

Load Transient with AC Load Line

V_{IN} = 12V, V_{DD1} = 1V, F_{SW1} = 700kHz,
R_{LL} = 0Ω, I_{OUT} = 0 <-> 73A @ 500A/µs



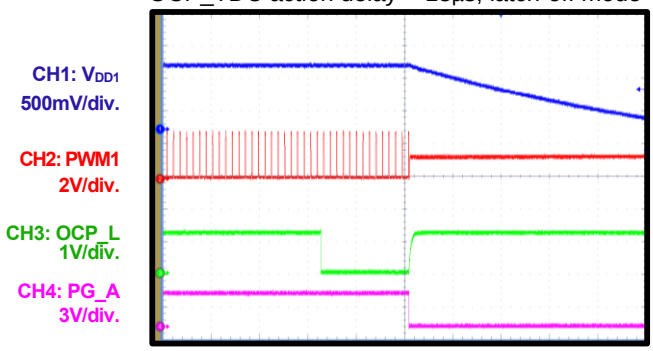
50µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{DD1} = V_{DD2} = 1V, F_{SW1} = F_{SW2} = 700KHz, VDD33 = 3.3V, 4 + 1 phase mode, T_A = +25°C, unless otherwise noted.

OCP_TDC Protection

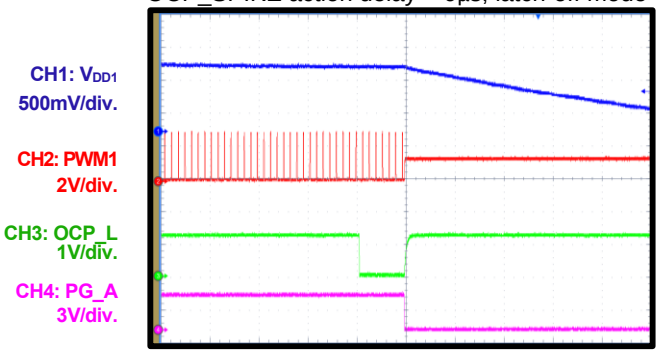
V_{IN} = 12V, V_{DD1} = 1V, OCP_TDC = 60A,
OCP_TDC action delay = 18µs, latch-off mode



10µs/div.

OCP_SPIKE Protection

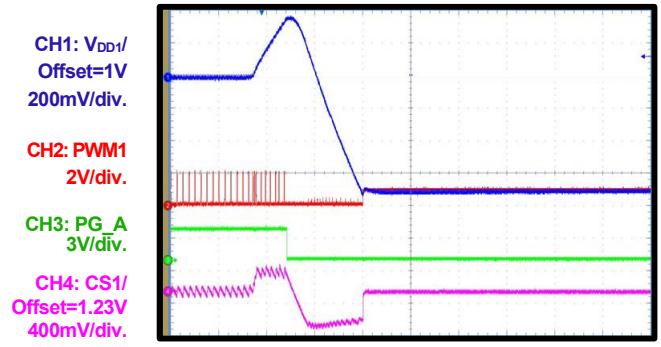
V_{IN} = 12V, V_{DD1} = 1V, OCP_SPIKE = 120A,
OCP_SPIKE action delay = 9µs, latch-off mode



10µs/div.

OVP

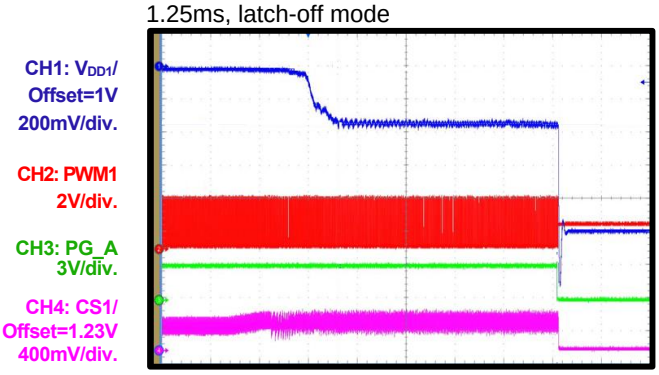
V_{IN} = 12V, V_{DD1} = 1V, latch-off mode



10µs/div.

UVP

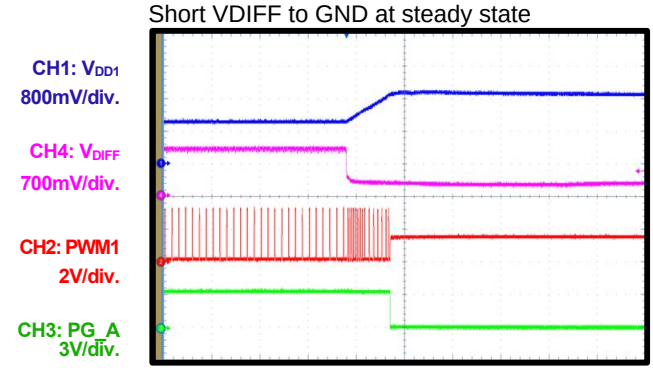
V_{IN} = 12V, V_{DD1} = 1V, UVP blanking time = 1.25ms, latch-off mode



2ms/div.

VDIFF SCP

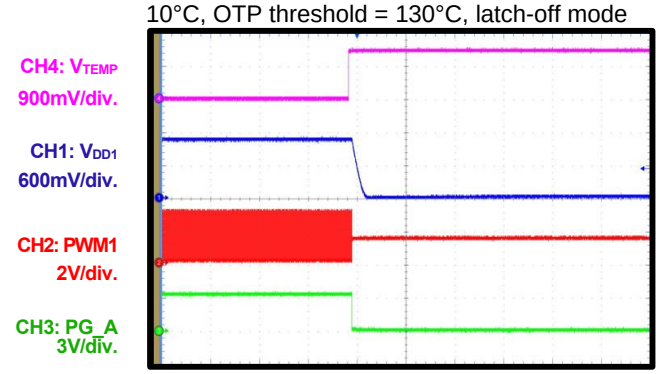
V_{IN} = 12V, V_{DD1} = 1V,
Short VDIFF to GND at steady state



10µs/div.

OTP

V_{IN} = 12V, V_{DD1} = 1V, T_J = (100°C/V) * V_{TEMP} + 10°C, OTP threshold = 130°C, latch-off mode



500µs/div.

PIN FUNCTIONS

Package Pin #	Name	Type (7)	Description
1	VDIFF1	A [O]	**Output of the differential remote sense amplifier for Rail 1.**
2	FB1	A [I/O]	**Feedback of Rail 1.** FB1 sources a current proportional to the sensed output current (I_{DROOP1}). This current flows through the resistor (R_{DROOP1}) between FB1 and VDIFF1 to create a voltage drop proportional to the load current. Select the resistor between VDIFF1 and FB1 to set a proper load line for Rail 1.
3	VOSEN1	A [I]	**Positive remote voltage sense input of Rail 1.** VOSEN1 is connected to the VR output voltage directly at the load and should be routed with VORTN1 differentially.
4	VORTN1	A [I]	**Remote voltage sensing return input of Rail 1.** VORTN1 is connected to ground directly at the load and should be routed differentially with VOSEN1.
5	VORTN2	A [I]	**Remote voltage sensing return input of Rail 2.** VORTN2 is connected to ground directly at the load and should be routed differentially with VOSEN2.
6	VOSEN2	A [I]	**Positive remote voltage sense input of Rail 2.** VOSEN2 is connected to the VR output voltage directly at the load and should be routed differentially with VORTN2.
7	VDIFF2	A [O]	**Output of the differential remote sense amplifier for Rail 2.**
8	FB2	A [I/O]	**Feedback of Rail 2.** FB2 sources a current proportional to the sensed output current (I_{DROOP2}). This current flows through the resistor (R_{DROOP2}) between FB2 and VDIFF2 to create a voltage drop proportional to the load current. Select a resistor between VDIFF2 and FB2 to set a proper load line for Rail 2.
9	VTEMP	A [I]	**Analog signal from the VR to the controller.** VTEMP indicates the maximum temperature of the power stage. The MP2853 supports temperature sensing from the Intelli-Phase. All VTEMP pins of the power stage tie together to produce the maximum value of the VTEMP bus.
10	CS_SUM1	A [I]	**Rail 1 total phase current sensing input.** CS_SUM1 is used for Rail 1 load-line and over-current protections. Connect the Rail 1 active phase CS signals together to CS_SUM1 through the current sense resistors.
11	CS_SUM2	A [I]	**Rail 2 total phase current sensing input.** CS_SUM2 is used for Rail 2 load-line and over-current protections. Connect the Rail 2 active phase CS signals together to CS_SUM2 through the current sense resistors.
12	IMON1	A [I/O]	**Analog total average current sensing signal of Rail 1.** IMON1 sources a current proportional to the sensed total average current from CS_SUM1. IMON1 is used for Rail 1 load current reporting.
13	IMON2	A [I/O]	**Analog total average current sensing signal of Rail 2.** IMON2 sources a current proportional to the sensed total average current from CS_SUM2. IMON2 is used for Rail 2 load current reporting.
14	IREF	A [I/O]	**Internal bias current set.** Connect a 61.9kΩ 1% accuracy resistor to AGND.
15	VINSEN	A [I]	**Input voltage sensing.**
16	ADDR	A [I]	**PMBus™ address setting.**
17	VDD18	Power	**1.8V LDO output.** VDD18 provides a power supply for the internal digital circuit. Connect a 1μF bypass capacitor to AGND.
18	EN	D [I]	**Enable control for both rails.**

PIN FUNCTIONS *(continued)*

Package Pin #	Name	Type	Description
19	PG_B	D [O]	**Power good indication B.** PG_B is an open-drain output. PG_B asserts when the output voltage of Rail 1 or Rail 2 is in regulation. The PMBus™ command MFR_VR_CONFIG4 (0Eh, Page 0) bit[0] sets the association of PG_A and a rail number. When bit[0] = 0, PG_B asserts when the Rail 2 output voltage is in regulation. When bit[0] = 1, PG_B asserts when the Rail 1 output voltage is in regulation.
20	PG_A	D [O]	**Power good indication A.** PG_A is an open-drain output. PG_A asserts when the output voltage of Rail 1 or Rail 2 is in regulation. The PMBus™ command MFR_VR_CONFIG4 (0Eh, Page 1) bit[0] sets the association of PG_A and a rail number. When bit[0] = 0, PG_A asserts when the Rail 1 output voltage is in regulation. When bit[0] = 1, PG_A asserts when the Rail 2 output voltage is in regulation.
21	OCP_L	D [O]	**Open-drain output.** OCP_L is the voltage regulator over-current logic output. OCP_L is active low.
22	ALT_P#	D [O]	**PMBus™ alert.** ALT_P# is an open-drain output. ALT_P# asserts low when a warning occurs.
23	SDA_P	D [I/O]	**PMBus™ data.**
24	SCL_P	D [I]	**PMBus™ clock.**
25	SVT	D [O]	**Push-pull output.** SVT is the SVI telemetry signal from the VR controller to the CPU.
26	VCCIO	A [I]	**Processor memory interface power rail.** VCCIO serves as the reference for the processor I/O signals including PWROK, SVD, SVC, and SVT. VCCIO is also used to power SVT.
27	PWROK	D [I]	**System-wide power good signal.** PWROK indicates that all voltage planes and free-running clocks are within specification if PWROK is high.
	PVID3		**PVID mode port 3.**
28	SVC	D [I]	**Serial VID clock from the CPU.** SVC frequency is in the range of 3.3 to 20MHz.
	PVID2		**PVID mode port 2.**
29	SVD	D [I]	**Serial VID data signal between the CPU and VR controller.**
	PVID1		**PVID mode port 1.**
30	PWM5	D [O]	**Tri-state logic-level PWM outputs.** Each output is connected to the PWM input of the Intelli-Phase.
31	PWM4	D [O]	
32	PWM3	D [O]	
33	PWM2	D [O]	
34	PWM1	D [O]	
35	VDD33	Power	**3.3V power supply input.** Connect a 1µF bypass capacitor to AGND.
36	CS5	A [I]	**Phase 5 current sense input.**
37	CS4	A [I]	**Phase 4 current sense input.**
38	CS3	A [I]	**Phase 3 current sense input.**
39	CS2	A [I]	**Phase 2 current sense input.**
40	CS1	A [I]	**Phase 1 current sense input.**
PAD	AGND	A [I/O]	**Analog ground.**

NOTE:

7) A = analog. D = digital. I = input. O = output. I/O = bidirectional.

BLOCK DIAGRAM

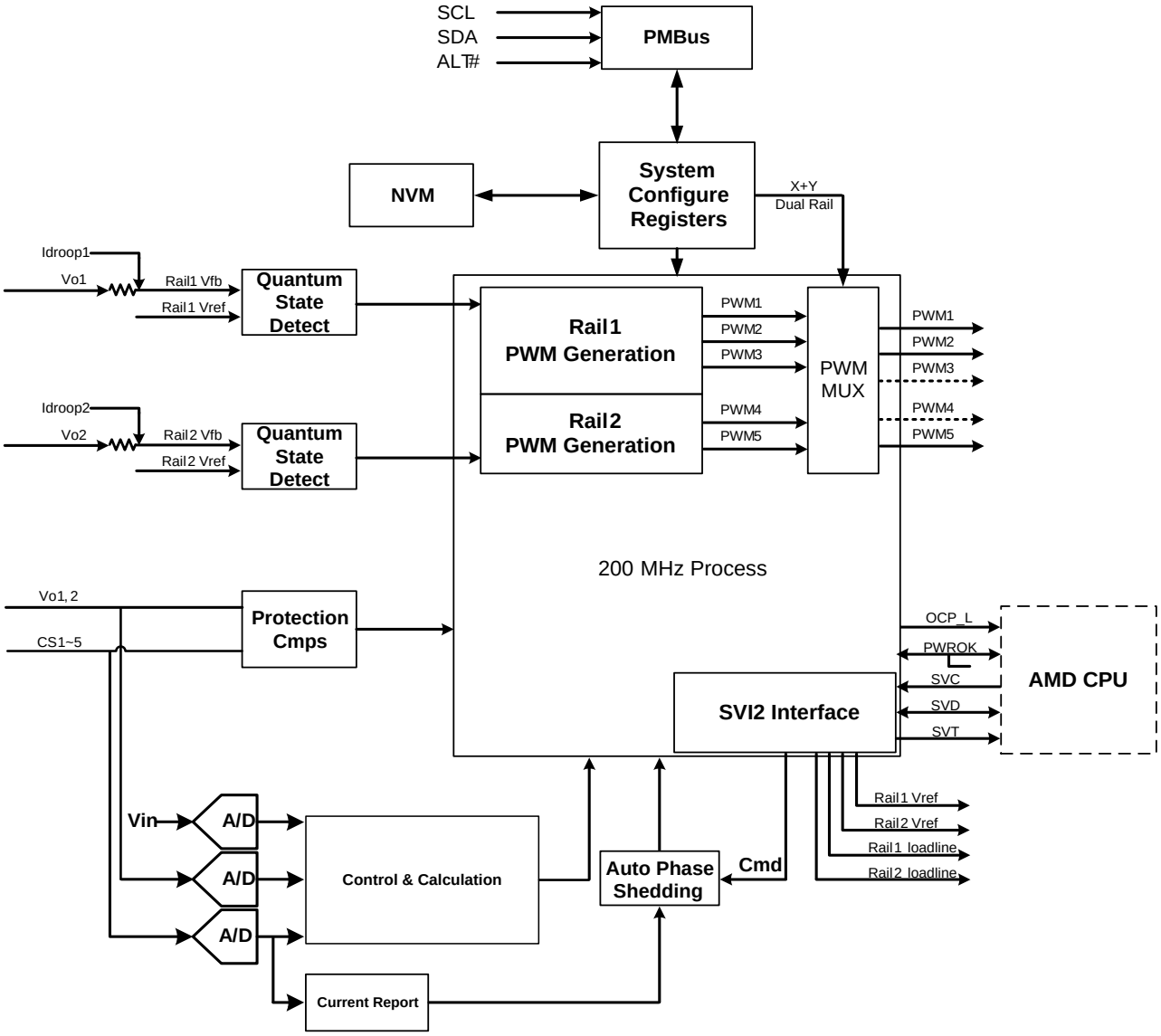


Figure 1: Functional Block Diagram

OPERATION

The MP2853 is a dual-output, digital, multi-phase, SVI2.0-compliant, voltage regulator (VR) controller for AMD microprocessors. The MP2853 can implement adaptive phase shedding and phase adding according to the load current to improve overall VR efficiency. The MP2853 contains precision DAC and ADC, a differential remote voltage sense amplifier, fast comparators, current sense amplifiers, internal slope compensation, digital load-line setting, PWRGD monitor, temperature monitor, PMBus™ and SVI2.0 interface, and EEPROM for custom configuration.

Fault protection features include V_{IN} under-voltage lockout (UVLO); over-current protection based on TDC (OCP_TDC); over-current protection based on ICCSPIKE, EDC, and ICCMAX (OCP_SPIKE); cycle-by-cycle phase-current limitation (OCP_PHASE), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MP2853 can also detect the fault type of the Intelli-Phase when a protection occurs. The MP2853 records all faults into the EEPROM automatically in case the power supply shuts off while the fault is occurring.

PWM Control and Switching Frequency

The MP2853 applies a unique, digital, pulse-width modulation (PWM) control to provide fast load transient response and easy loop compensation. The switching frequency can be set with the PMBus™ command FREQUENCY_SWITCH (33h).

The PWM on time of each phase updates in real-time according to the input voltage, output voltage, and the phase switching frequency adaptively as shown in Equation (1):

$$T_{on} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_s} \quad (1)$$

Where V_{OUT} is the real time output voltage, V_{IN} is the input voltage, and F_S is the switching frequency set by the PMBus™ command FREQUENCY_SWITCH (33h).

Dual-Rail Phase Configuration

The MP2853 is a dual-output controller and can be configured as a different phase number application via the PMBus™ command MFR_PHASE_PSI_CFG (C0h, Page 0) bit[6:4] (see Table 1).

Table 1: Phase Number Configuration and Active PWM Pins

MFR_PHASE_PSI_CFG (C0h, Page 0) bit[6:4]	Active PWM Pins	
	Rail 1	Rail 2
3'b000	PWM1~3	PWM4~5
3'b001	PWM1~2	PWM4~5
3'b010	PWM1~3	PWM5
3'b011	PWM1~2	PWM5
3'b100	PWM1	PWM5
3'b111	PWM1~4	PWM5

Refer to the MFR_PHASE_PSI_CFG (C0h, Page 0) section on page 58 for more information.

Any unused PWM pin enters tri-state, and the active phase interleaves automatically. Float the unused PWM pins, and connect the unused CS pins to CS_SUM. For example, when the MP2853 is configured to 3+1 mode by setting MFR_PHASE_PSI_CFG (C0h) = 0x20, the PWM4 is floating and in Hi-Z output. Connect CS4 to CS_SUM1 or CS_SUM2.

If Rail 2 of the MP2853 is unused, follow the steps below in the circuit design:

1. Connect VOSEN2, VORTN2, and IMON2 to AGND.
2. Short VFB2 and VDIFF2 together.
3. Float the unused PWM pins.
4. Connect the unused CS pins to CS_SUM2.
5. Assign PG_A to Rail 1.
6. Float PG_B.

EEPROM Operation

The MP2853 uses the EEPROM to store application configuration parameters. The default values are pre-programmed at the factory. The data can be programmed again using the STORE_USER_ALL command (15h) via the PMBus™. The configuration is restored from the EEPROM during the power-on sequence or by receiving the RESTORE_USER_ALL command (16h) from the PMBus™ (see Figure 2).

The operation of the EEPROM can be accomplished easily with MPS GUI software. The EEPROM can be subject to more than 100,000 erase/write cycles.

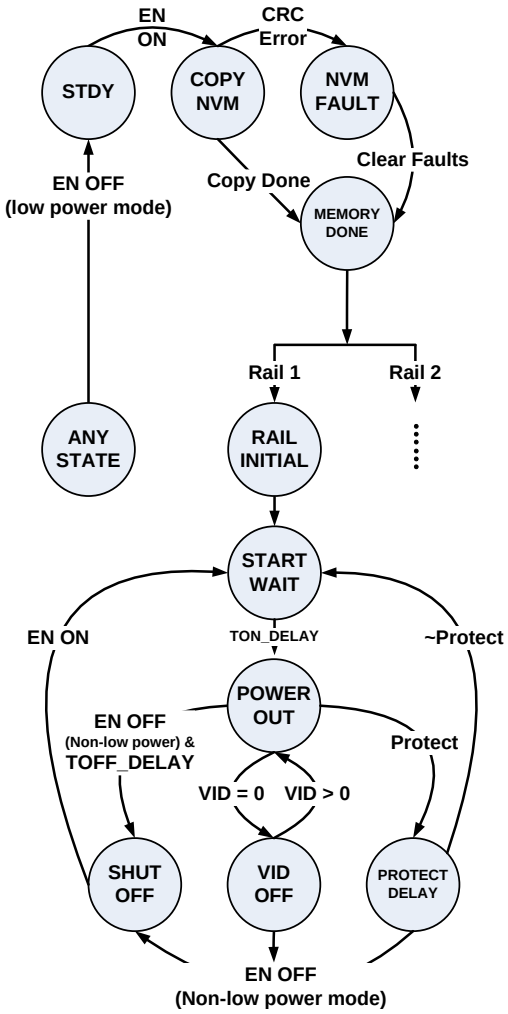


Figure 2: System State Machine

Power-On EEPROM Fault

The MP2853 is supplied by a +3.3V voltage. The internal LDO produces a +1.8V voltage for the digital circuit. The system is reset by the internal power-on reset (POR) signal. After the system exits POR, the data in the EEPROM is restored to the operating registers to initialize the VR operation. This restore and initialization process takes about 1.5ms, typically.

If the data from the EEPROM is checked as invalid by the cyclic redundancy check (CRC) during the system initialization process, the system enters an EEPROM fault state without outputting power or waiting for an error clear command.

Clear the EEPROM fault and start up the device again using the following steps:

1. Store the configuration into the EEPROM with the PMBus™ command STORE_USER_ALL (15h).
2. Clear the EEPROM fault via the PMBus™ command CLEAR_EEPROM_FAULTS (FFh).
3. Send the PMBus™ command CLEAR_FAULT (03h).

Alternatively, the EEPROM fault can be cleared and the device can power up again using the following steps:

1. Store the configuration into the EEPROM with the PMBus™ command STORE_USER_ALL (15h).
2. Restart with a VDD33 power recycle or low power mode EN toggle.

Wait State

After the system initialization, the MP2853 begins the T_{ON} delay period and the soft-start process. The MP2853 enters the corresponding wait state if any of the following conditions occur:

1. Protection is triggered (such as the sensed input voltage is under the VIN_UVLO_ON threshold) or the sensed temperature is above the OTP point. The MP2853 enters a protection mode to wait for the fault to clear. The device enters the protect delay state (12.5ms) before the next power-on restart cycle.
2. The operation off command is received via the PMBus™. The MP2853 enters the shutoff state until it receives the operation on command from the PMBus™ master.
3. VID command off. The MP2853 is in the VID off state and there is no PWM output until the VID command is higher than the off level. The MP2853 begins the soft-start process immediately after exiting the VID off state.
4. EN off. The MP2853 is shut down.

Enable (EN) Control and Low-Power Mode

The MP2853 can be enabled through EN and the PMBus™ operation command (01h). The output is enabled when both EN = 1 and the OPERATION command are set to on. Generally, the OPERATION command is on by the default setting register OPERATON (01h) = 0x80, so the MP2853 begins working when EN pulls high.

The MP2853 can be factory-programmed to low-power mode or regular-power mode.

In low-power mode, when EN is low, the PMBus™ communication is disabled, and the quiescent current is reduced to 150μA. In regular-power mode, the PMBus™ communication is available, and the EEPROM is live when EN is low. Low-power mode is factory-programmable only.

Start-Up Sequence

The start-up sequence in SVI2 VID mode is shown in Figure 3.

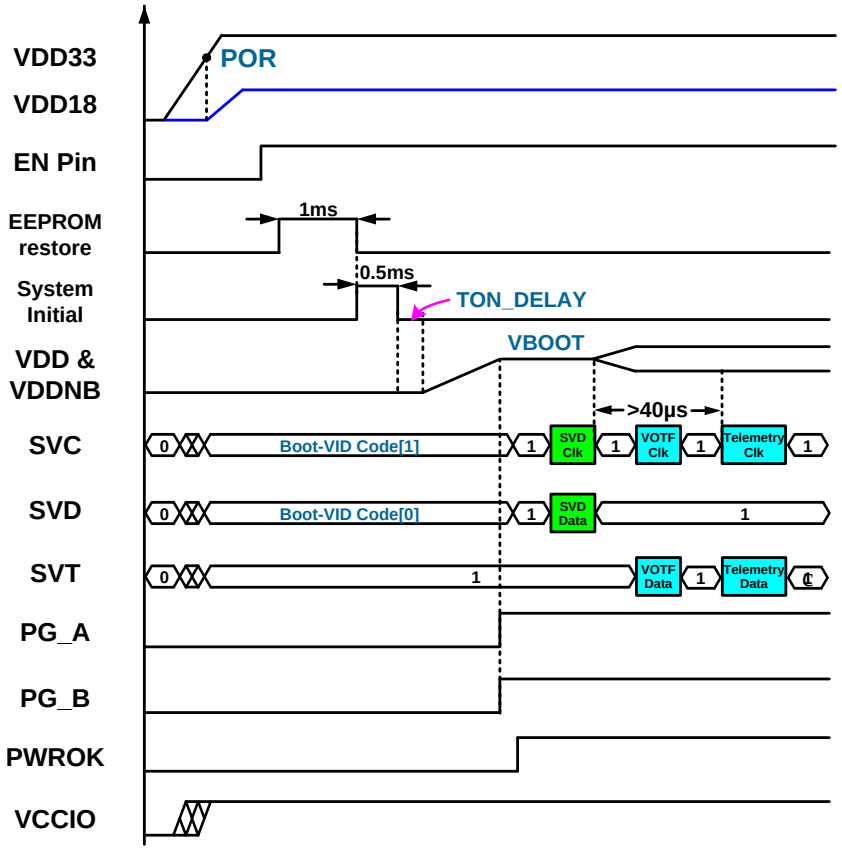


Figure 3: VR Start-Up Sequence in SVI2 VID Mode

The start-up sequence is listed below:

1. The MP2853 VDD33 supply rises above its UVLO threshold and the internal LDO generates a 1.8V power supply for the digital circuit.
2. The platform I/O voltage supply output (VCCIO) ramps up. The system should guarantee that VCCIO is within the specification and that SVC and SVD are driven to the BOOT_VID value for at least 10μs prior to EN being asserted to the MP2853.
3. EN of the MP2853 is pulled high. The configuration in the EEPROM begins transferring to the operating registers within 1ms. During this period, PWM1/5 is detected to check whether to disable Rail 1 or Rail 2 or not for debug mode.
4. The MP2853 is initialized within 500μs, which includes boot voltage, soft-start ramping slew rate, switching frequency, trim settings, PMBus™ address, protection level and mode.

5. The VR ramps to the boot voltage, which is set by the BOOT_VID code. The relationship between the boot voltage and the BOOT_VID code is defined in Table 2 according to the AMD SVI2 spec.

Table 2: AMD SVI2 V_{BOOT} and BOOT_VID Code

SVC	SVD	V_{BOOT} (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

6. The MP2853 asserts PG_A and PG_B of VDD1 and VDD2 for the system.
7. After all power rails are ready, and the free-running clocks in the system are within specification, the system asserts PWROK.
8. The CPU holds BOOT_VID for at least 10µs after PWROK is asserted.
9. The MP2853 serial VID interface (SVI) bus is active and idle.
10. The CPU may issue 0/1/2 SVD packets. Each rail may ramp to the start-up voltage or remain at the boot voltage.
11. For some CPUs, the start-up voltage is higher than the BOOT_VID voltage. For other CPUs, the start-up voltage may be lower than the BOOT_VID voltage. If the start-up voltage is higher than the BOOT_VID voltage, the MP2853 sends a VOTF Complete signal when the last rail finishes the upward voltage slew.
12. The VR can send a telemetry packet in default mode 40µs after the stop bit of the second SVD packet.

Shutdown

The MP2853 enters the shutdown state through the following methods:

1. EN pulls low. The MP2853 provides EN low-power mode and regular-power mode options. In EN low-power mode, both rails enter Hi-Z shutdown, and the chip consumes minimum power. In regular-power mode, both rails can be configured as Hi-Z shutdown or soft shutdown by command MFR_VR_CONFIG2 (F7h, Page 0) bit[6]. The PMBus™ communication is live in regular-power mode when EN is low.
2. The PMBus™ OPERATION command is off. The OPERATION can be programmed with soft-off or Hi-Z off. At OPERATION soft-off, the VR shuts down softly with the programmed slew rate. At command Hi-Z off, the PWM enters Hi-Z state to turn off the high-side and low-side MOSFETs (HS-FET, LS-FET).
3. UVP, V_{IN} UVLO, OCP_SPIKE, OCP_TDC, OTP turn off all phases immediately by forcing PWM into Hi-Z state.
4. OVP forces PWM low to turn off all HS-FETs and turn on all LS-FETs to discharge the output capacitor until the output voltage falls below the reverse-voltage protection (RVP) level (300mV).

If the MP2853 is in the protect-delay state and the OPERATION command is off or EN is pulled low in regular-power mode, the MP2853 switches to the shut-off state and waits for the system to restart. This can restart the MP2853 when the protection mode is set to latch mode. If the protection is cleared in hiccup or retry mode, the MP2853 can reboot after 12.5ms without toggling EN.

If a fault occurs on any rail, the VR de-asserts that rail's PG signal and allows that rail's output to drop to zero relative to GND without any undershoot.

Voltage Reference

The MP2853 has two 8-bit VID-DACs, which provide the reference voltage (V_{REF}) for the individual output. V_{REF} is in a VID format with 6.25mV per step and ranges from 0 to 1.55V.

The MP2853 provides three different VID control modes: SVI VID mode, PMBus™ VID mode, and PVID mode. This means that the input of the VID-DAC may be from the SVI, PMBus™ interface, or 3-bit PVID selection (see Figure 4).

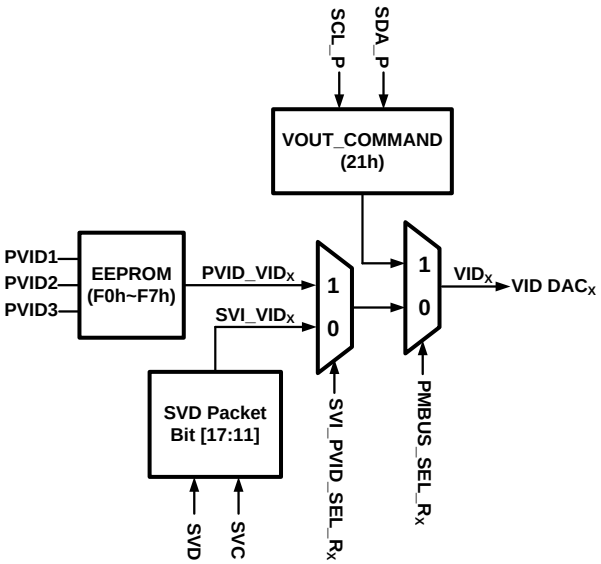


Figure 4: VID Control

Where x = 1 is Rail 1, and x = 2 is Rail 2.

Output Voltage Setting and Sensing

The voltage at the load is sensed with a differential voltage sense amplifier for each rail. This type of sensing provides better load regulation. The sensed output voltages are used for loop compensation and output voltage monitoring via the PMBus™ interface and SVI interface. The gain of the differential amplifiers can be programmed to unity gain or half gain with PMBus™ command MFR_VR_CONFIG (D0h) bit[5] and bit[3].

With unity gain, V_{REF} is equal to VID, and the maximum VID voltage is limited to 1.55V, which is the maximum VID-DAC output voltage.

With half gain, V_{REF} is equal to half of VID, and the maximum VID voltage is extended to 3V. The half gain can be used to support over-clocked applications and POL applications with a 1.55 - 3V output voltage.

When V_{OUT} ≤ 3V, connect the remote sense amplifier input pins (VOSEN and VORTN) to the output at the load directly.

When V_{OUT} > 3V, the output voltage must be divided to the reference voltage within 1.55V. Figure 5 shows the typical connections for V_{OUT} > 3V when remote sensing is applied.

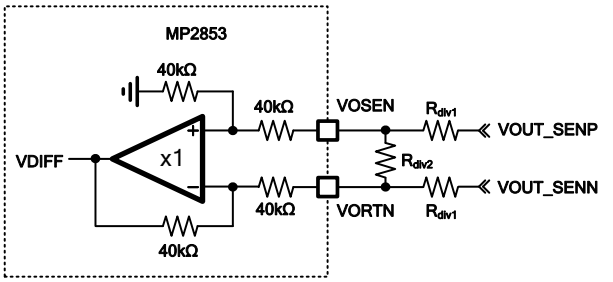


Figure 5: Output Divider Connections when Remote Sense is Applied

VOUT_SENP and VOUT_SENN are from the load and must be routed as a differential pair on quiet areas. Calculate the voltage divider ratio in Figure 5 with Equation (2):

$$K_R = \frac{V_{DIFF}}{V_{OUT}} = \frac{1}{(\frac{1}{R_{div1}} + \frac{2}{R_{div2}} + \frac{1}{40K}) \times R_{div1}} \quad (2)$$

K_R must be programmed into the MP2853 by the PMBus™ command VOUT_SCALE_LOOP (29h) with Equation (3):

$$VOUT\_SCALE\_LOOP = 2^7 \times K_R \quad (3)$$

Where VOUT_SCALE_LOOP is the programmed value in register VOUT_SCALE_LOOP (29h). The controller uses Equation (3) to determine the reference voltage.

The reference voltage is 6.25mV per step. Any voltage outside of the 6.25mV per step value is rounded down to the closest value. To minimize the output voltage DC setting error, match the real output divider ratio by R_{DIV1} and R_{DIV2} and the PMBus™ setting ratio by the command VOUT_SCALE_LOOP (29h). Design a V_{REF} value close to multiples of 6.25mV. Calculate the reference voltage in the MP2853 with Equation (4):

$$V_{REF} = \begin{cases} \frac{VOUT\_SCALE\_LOOP}{2^7} \times V_{OUT} & 29h \neq 0 \\ V_{OUT} & 29h = 0 \end{cases} \quad (4)$$

Refer to the VOUT_SCALE_LOOP (29h) section for more information.

To prevent the output voltage from going out of regulation, ensure that VOSEN is lower than the maximum allowed sensing voltage (VDD33 - 0.3V) at any time.

For output voltage designs above the VOSEN specification, connect the output divider as shown in Figure 6. VORTN is connected to AGND directly to disable remote sensing.

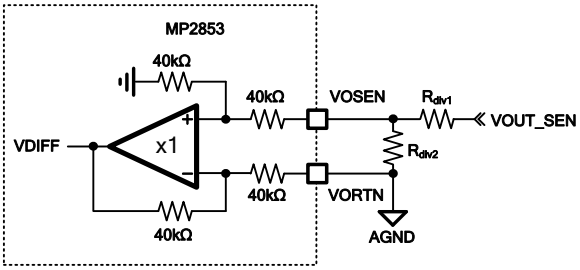


Figure 6: Output Divider Connections when Remote Sense is not Applied

Calculate the voltage divider ratio in Figure 6 with Equation (5):

$$K_R = \frac{V_{DIFF}}{V_{OUT}} = \frac{1}{(\frac{1}{R_{div1}} + \frac{1}{R_{div2}} + \frac{1}{80K}) \times R_{div1}} \quad (5)$$

Inductor Current Sensing

The MP2853 works with MPS' Intelli-Phase to sense the phase inductor current and the total current (see Figure 7a and Figure 7b). The cycle-by-cycle current information is used for phase-current balancing or thermal balancing, OCP, and adaptive voltage positioning (output-voltage droop).

The resistor (R_{CS}) is connected from CS to CS_SUM. CS_SUM is a 1.23V constant voltage and can sink or source current to provide voltage shifts that meet the operating voltage range of CS.

Different types of Intelli-Phase products have different operating voltage ranges for CS (V_{CS_MIN} and V_{CS_MAX}). Refer to each Intelli-Phase's datasheet to determine the minimum and maximum operating voltage ranges. Determine a proper R_{CS} value with Equation (6):

$$V_{CS\_MIN} < I_{LOAD} \times K_{CS} \times R_{CS} + 1.23V < V_{CS\_MAX} \quad (6)$$

By working with the Intelli-Phase, the MP2853 does not need to use temperature compensation and impendence matching as a traditional DCR sensing to achieve an accurate current sense.

In Figure 7a, the MP2853 is configured as a 3+2 operation. Connect CS4 to CS_SUM2 with R_{CS}. In Figure 7b, the MP2853 is configured as a 4+1 operation. Connect CS4 to CS_SUM1 with R_{CS}.

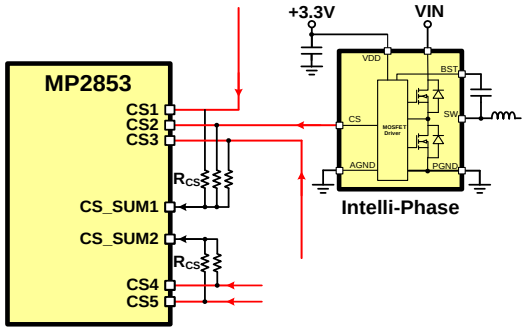


Figure 7a: Phase Current Sense (3+2)

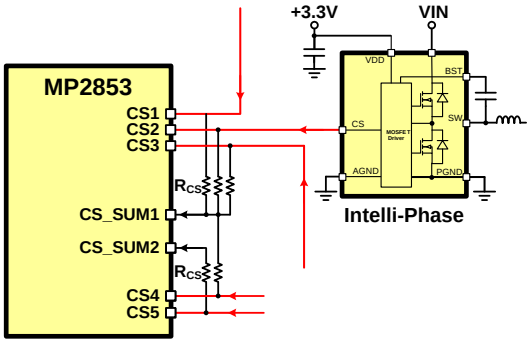


Figure 7b: Phase Current Sense (4+1)

Total Current Sensing

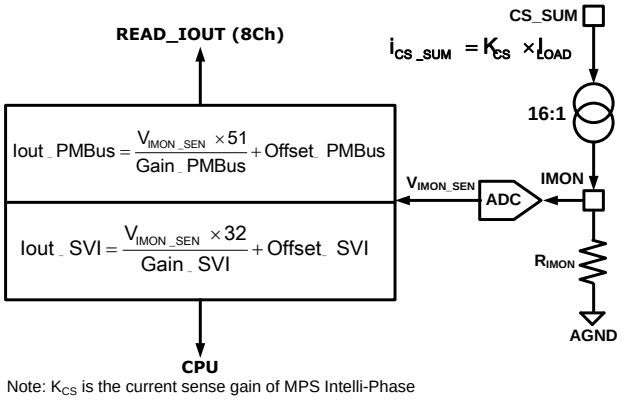
The total current is summed from CS_SUM and a 1/16 proportional current emerges to IMON. Connect a resistor from IMON to ground to generate a voltage proportional to the output current. The IMON voltage is sampled, calculated, and converted to an output current (I_{OUT}). The sensed I_{OUT} is reported to the SVI2 processor through the SVT line. I_{OUT} is also returned with the PMBus™ command READ_IOUT (8Ch).

If the auto-phase shedding function is enabled via the PMBus™, the total current report is used to determine whether to enter or exit phase-shedding mode to flatten the overall efficiency over the operating current range.

The MP2853 provides a user-programmable scaling factor and a user-programmable current offset. The programmable parameters allow users to match the IMON scaling to the design's voltage regulator tolerance band (VRTOB)

calculation. This provides the most accurate current reporting across the entire load range and maximizes the performance of the CPU turbo. The scaling factor can also be reduced or offset to under-report the total current to the CPU for better performance. Figure 8 shows the MP2853 IMON sense and report block diagram.

In Figure 8, the GAIN_PMBus register value (IOUT_CAL_CFG (C5h)) converts the ADC sensed V_{IMON} value to direct mode with 0.25A/LSB. The GAIN_SVI register value (IOUT_VR_CAL (ADh)) converts the sensed V_{IMON} value to the SVI2 current reported format (FFh = load current between IDDSPIKE and OCP_SPIKE), which is reported to the CPU. The detailed calculation of the register value is given in the MP2853 application note and spreadsheet.



Note: K_{CS} is the current sense gain of MPS Intelli-Phase

Figure 8: Current Sense and Report

Active-Voltage Positioning (AVP)

The MP2853 supports active voltage positioning (AVP) operation by connecting a droop resistor (R_{DROOP}) between VDIFF and V_{FB}. The internal total current sensing circuit produces a droop current source (I_{DROOP}) with a default of 5/32 of the current sensing signal from CS_SUM. I_{DROOP} flows to R_{DROOP} from FB to VDIFF (see Figure 9).

With this function, the output voltage drops gradually as the load current increases. This is also known as the load line. The load-line slope with 5/32 current sense gain, which is also referred as initial load line slope, can be calculated with Equation (7):

$$R_{LL\_INI} = \frac{5}{32} \times K_{CS} \times R_{DROOP} \quad (7)$$

Where R_{LL_INI} is the initial load line slope (in Ω), K_{CS} is the current sense gain of the Intelli-Phase (in A/A), and R_{DROOP} is the droop resistor (in Ω).

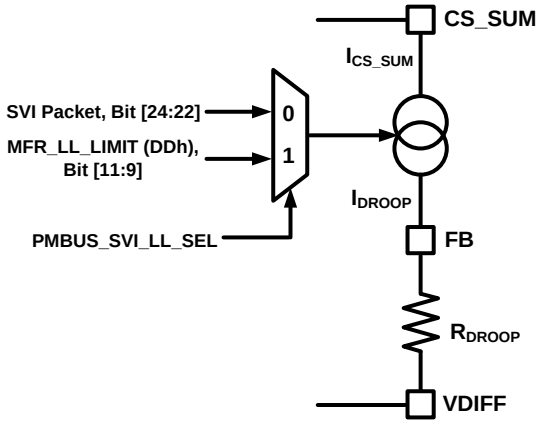


Figure 9: Load Line Circuit

The MP2853 provides eight levels of load-line slope trim with SVI2 interface or PMBus™ interface. Table 3 shows the load-line level definition. The PMBus™ command MFR_LL_LIMIT_SET (DDh) bit[12] defines the load-line slope controlled by the SVI2 interface or PMBus™ interface. When bit[12] = 0, the load-line slope is determined by SVI2 SVD packet bit[24:22]. When bit[12] = 1, the PMBus™ command MFR_LL_LIMIT_SET (DDh) bit[11:9] sets the load-line slope value.

Refer to the MFR_LL_LIMIT_SET (DDh) section for more information.

Table 3: 8-Level Load-Line Slope Definition

SVD Packet Bit[24:22] or MFR_LL_LIMIT_SET (DDh) Bit[11:9]	Load-Line Slope
3'b000	0
3'b001	0.6 * R_{LL_INI}
3'b010	0.8 * R_{LL_INI}
3'b011	R_{LL_INI}
3'b100	1.2 * R_{LL_INI}
3'b101	1.4 * R_{LL_INI}
3'b110	1.6 * R_{LL_INI}
3'b111	1.8 * R_{LL_INI}

Dynamic Voltage Identification (DVID)

The MP2853 supports dynamical output voltage transitions by changing the VID code with SVI2 interface, PMBus™ interface, and PVID toggling. This concept is commonly referred to as dynamic voltage identification (DVID). Consequently, the output voltage can be changed without having to reset the controller or the load chip. In SVI VID mode, the DVID is active after PWROK asserts. In PMBus™ VID mode and PVID mode, the DVID is active after V_{OUT} is settled. The V_{OUT} change can either step upwards or downwards. The DVID slew rate is set with the PMBus™ command TON_RISE (61h). Calculate the DVID slew rate with Equation (8):

$$SlewRate = \frac{12.5mV}{(VID\_SR\_CNT + 3) \times 50ns} \quad (8)$$

Where VID_SR_CNT is a sub-register in TON_RISE (61h), which ranges from 0 to 2047. The reference voltage transition slew rate ranges from 0.122 - 50mV/µs.

Refer to the PMBus™ TON_RISE (61h) section on page 48 for more information.

The MP2853 applies an advanced digital control method to improve the output voltage performance when VID ramps up and down.

Ramping Upward

When the output voltage ramps upward, the inductor current becomes higher to charge the output capacitors. This current introduces a large, positive, droop voltage and lowers the output voltage.

When V_{REF} ramping ends, the output voltage may be smaller than the minimum regulation tolerance budget (TOB).

The MP2853 can ramp up more VID steps automatically than the target VID and fall back to fasten the output voltage to rise into the regulation tolerance budget.

In SVI VID mode, when DVID up ends, the MP2853 issues a VOTF completion packet through SVT to indicate to the processor that the V_{OUT} slew up is completed.

Ramping Downward

When the output voltage ramps downward, the inductor current becomes smaller to discharge the output capacitors. The output capacitors continue discharging when ramping ends and may lead to an output voltage undershoot.

The MP2853 applies a low-pass filter for the VID-DAC to smooth out the reference voltage when the output voltage is ramping downward.

Figure 10 shows the output voltage when VID ramps upward after the previous VID finishes ramping downward.

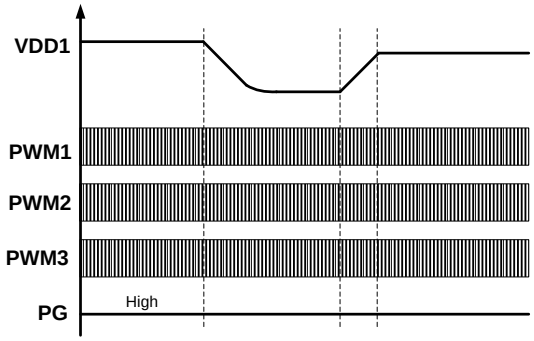


Figure 10: VID Ramping Downward ➔ VID Ramping Upward

VID Decay Mode

In SVI VID mode, when the VID codes are lower than the current VID level, the MP2853 checks the state of the power state bits (PSI0_L/PSI1_L) in the SVI command. If the power state bits are not active, the controller begins stepping the regulator output to the new VID target with the DVID slew rate. If the power state bits are active, the controller can decay the output voltage with a natural output current discharging and step the VID-DAC output down to the target VID. This allows the controller to recover quickly and move to a high VID code if commanded. The activation criteria of decay mode can be configured by the MFR_DECAY_SET (C9h) register (see Table 4).

Table 4: Decay Mode Configuration Registers

MFR_DECAY_SET (C9h) Bit[1:0]	Decay Mode
2'b00	Never decays
2'b01	PSI0 asserts
2'b10	Both PSI0 and PSI1 assert

Power State Change with SVI

The SVI can switch the VR to different power states to achieve high efficiency at light-load condition. The VR optimizes its power loss to flatten the efficiency curve over the operating current range with power state commands issued by the processor.

In full-phase mode, all phases run in continuous conduction mode (CCM). When the power state indicates a PSI0, only one phase is running with synchronous switching, and the other phases are in tri-state. When the power state indicates a PSI1, only one phase is running in diode emulation mode, and the switching frequency falls automatically due to the light-load condition.

When the dynamic VID transition is issued by a DVID command, the power state of the related rail changes to full-phase mode. After the output is regulated to the new target voltage, the power state enters the new power state issued by the processor from full-phase mode.

Auto-Phase Shedding (APS)

The MP2853 provides an auto-phase shedding (APS) function to improve efficiency when there are no forced power state indicators. In 2-phase operation, the VR works at 2-phase CCM in heavy load and 1-phase CCM in light load to optimize efficiency. The VR enters 1-phase discontinuous conduction mode (DCM) at extremely light load to reduce the switching loss further (see Figure 11).

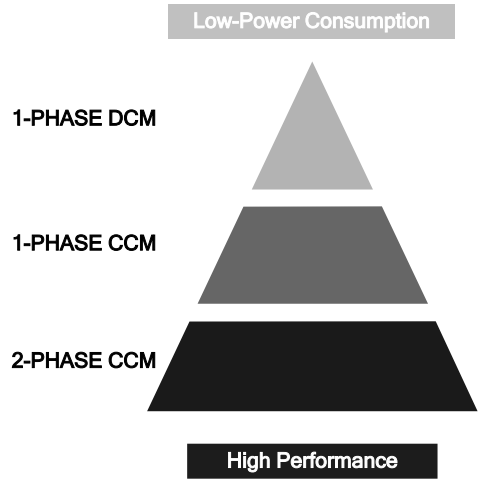


Figure 11: APS Function Diagram in 2-Phase Operation

The APS function is implanted by comparing the sensed load current with each power state current threshold. The MP2853 provides two types of registers to configure the auto-phase shedding function. Rail 1 has two registers for the phase shedding level: MFR_AUTO_PS (C7h, Page 0) and MFR_23PHASE_LOW (C8h, Page 0). Rail 2 has one register for the phase shedding level: MFR_AUTO_PS (C7h, Page 1). Each rail has four bits in register MFR_AUTO_PS to program the hysteresis value to prevent the converter from changing the power state back and forth at a steady load current. Figure 12 shows the APS current thresholds setting from 3-phase CCM to 2-phase CCM. Refer to the PMBus™ register MFR_AUTO_PS (C7h) and MFR_23PHASE_LOW (C8h) sections on page 64 for more information.

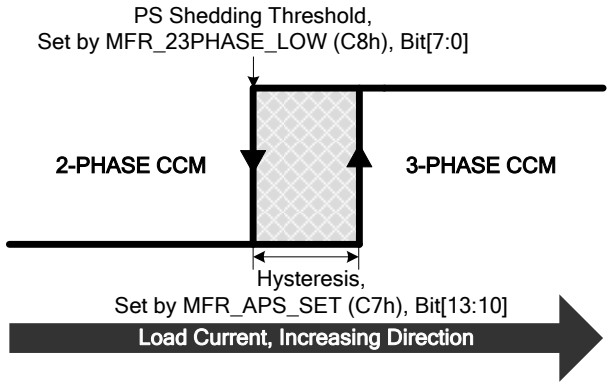


Figure 12: APS Threshold Setting

In addition to the sensed output current comparison, the MP2853 provides three conditions to exit APS immediately and run in full-phase CCM operation to accelerate the load transient response and reduce the output voltage undershoot:

1. The DVID process makes the controller run with full-phase CCM. After the output voltage is settled to the target value, a new power state is determined by the load current.
2. The load step-up causing the VFB- window trip triggers full-phase CCM to reduce the output voltage undershoot.
3. Once the phase current exceeds the per-phase over-current limit, the MP2853 runs with the full-phase number.

Phase Current Balancing/Thermal Balancing

The phase current is sensed and calculated with the current reference in the current loop. Each phase's PWM on time is adjusted individually to balance the currents accordingly.

The MP2853 applies Σ-Δ modulation and delay line-loop technology in the current balance modulation to increase the resolution of the current balance modulation and reduce PWM jitter greatly. The time resolution of the digital system is 5ns. By applying Σ-Δ modulation and DLL technology, the digital PWM resolution can be increased to 0.08ns.

Each current balance loop can also include a programmable phase current offset to achieve thermal balance among the phases. The phase has a greater cooling capability due to better proximity to air flow, allowing the phase to take more phase current by increasing the phase current reference with the offset to keep the phase thermal more balanced. The bandwidth of the current proportional-integral (PI) loop is relatively lower than the output voltage feedback loop and barely impacts the output voltage.

Input Voltage Sensing

The input power supply voltage is sampled at VINSEN with a resistor divider (see Figure 13). The sensed input voltage is used for PWM on-time calculation, V_{IN} UVLO, V_{IN} OVP fault protection, and input voltage monitoring.

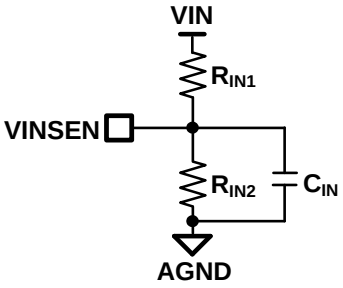


Figure 13: Input Voltage Sensing Connection

In designs, the divided voltage on VINSEN should not exceed the ADC sampling range (1.6V) at the maximum input voltage. Connect a 1 - 10nF ceramic capacitor from VINSEN to AGND as the input sense filtering capacitor (C_{IN}). Program the input voltage sensing divider ratio into the MP2853 with the PMBus™ command MFR_VIN_SCALE_LOOP (D4h).

Calculate the ratio (K_{IN}) with Equation (9):

$$K_{IN} = \frac{R_{IN2}}{R_{IN1} + R_{IN2}} = \frac{VIN\_SCALE\_LOOP}{2^{10}} \quad (9)$$

Where VIN_SCALE_LOOP is the decimal value in register MFR_VIN_SCALE_LOOP (D4h). In designs, match the resistor setting K_{IN} and PMBus™ setting value to improve the input voltage sensing accuracy.

Refer to the PMBus™ MFR_VIN_SCALE_LOOP (D4h) section on page 71 for more information.

Temperature Sensing

The MP2853 measures the temperature of the power stage by connecting all Intelli-Phase VTEMP pins (see Figure 14). The VTEMP voltage of the MP2853 indicates the highest junction temperature of all Intelli-Phase devices in the VR power system. The sensed temperature is used for over-temperature fault protection.

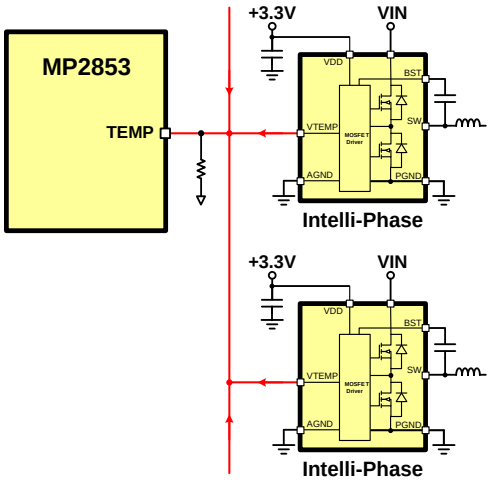


Figure 14: External Temperature Sense

VTEMP of the Intelli-Phase is a voltage output proportional to the junction temperature. Generally, the junction temperature can be calculated with Equation 10):

$$T_{JUNCTION}(°C) = a \times V_{TEMP} + b \quad (10)$$

Where V_{TEMP} is the voltage on the Intelli-Phase VTEMP pin (in V), a is the temperature sense gain (in °C/V), and b is the temperature sense offset (in °C). Refer to the datasheet of the Intelli-Phase for more information on the a and b values.

Fault Monitoring and Protections

The MP2853 supports various fault monitoring and protections described below.

V_{IN} UVLO and OVP

The VR shuts off immediately by setting the PWM tri-state output if the sensed input voltage is below the VIN_OFF threshold. The VR restarts again when the sensed input voltage is above the VIN_ON threshold. The V_{IN} UVLO threshold is programmable with the PMBus™ command VIN_ON (35h) and VIN_OFF (36h) with 0.25V/LSB.

The MP2853 provides two types of V_{IN} OVP: latch-off mode and auto-retry mode. In latch-off mode, the VR latches off immediately if the input voltage is above the V_{IN} OVP threshold. In auto-retry mode, the VR tri-state shuts off when the sensed input voltage is above the V_{IN} OVP threshold and tries to restart when the input voltage falls below the V_{IN} OVP threshold.

V_{IN} OVP mode is programmable with the PMBus™ command MFR_PRT_CONFIG (DCh, Page 0) bit[7]. The V_{IN} OVP threshold is set with the PMBus™ command VIN_OV_FAULT_LIMIT (55h, Page 0).

Over-Current Protection (OCP)

The MP2853 uses a triple OCP mechanism with three types of thresholds to protect the processor and power stage from over-current.

The first type, OCP_TDC, is a time- and current-based threshold that refers to the TDC level. OCP_TDC should trip when the total inductor current sensed by CS_SUM1/2 exceeds the OCP_TDC threshold for the OCP_TDC blanking time. After OCP_TDC of either rail is triggered, OCP_L asserts. OCP_TDC can be programmed to no action, hiccup, retry six times, or latch-off mode via the PMBus™.

The second type, OCP_SPIKE, is a protection based on the ICCSPIKE/TDC/ICCMAX level. Once the total inductor current sensed by CS_SUM1/2 exceeds the OCP_SPIKE threshold for the OCP_SPIKE blanking time, OCP_SPIKE is triggered. When OCP_SPIKE of either rail is triggered, OCP_L asserts. OCP_SPIKE can be programmed to no action, hiccup, retry six times, or latch-off mode via the PMBus™.

The total current is sensed by CS_SUM1/2 with a 1/40 current gain. The OCP_SPIKE and OCP_TDC thresholds can be programmed by individual registers.

After OCP_L asserts, the MP2853 provides a delay time before shutting down the VR. This delay time is called an action delay. If the sensed load current does not decrease below the OCP threshold after the action delay time expires, the MP2853 shuts down the VR and de-asserts PG to protect the processor and power stage.

The blanking time or action delay time of OCP_TDC and OCP_SPIKE can be programmed individually with PMBus™ commands. Table 5 shows the programming range of the blanking time and action delay time.

Table 5: OCP Timing Parameters

Parameter	Min	Max	Unit
OCP_TDC blanking time	20	5100	µs
OCP_SPIKE blanking time	0.2	3	µs
OCP_TDC action delay	0	31	µs
OCP_SPIKE action delay	0	15	µs

The third type, OCP_PHASE, is a current-based limitation threshold. The MP2853 monitors the phase current cycle-by-cycle. When the phase current exceeds the OCP_PHASE threshold at the PWM off time, the PWM remains low to discharge the inductor current below the setting threshold. If the present phase PWM on signal is blocked for more than 80ns, the PWM on signal is skipped for this cycle, and the next phase is turned on directly to regulate the output voltage. If the load current continues rising, the output voltage drops, and the inductor current is limited. OCP_PHASE is implemented with UVP, generally. The OCP_PHASE threshold is PMBus™-programmable with the command MFR_OCP_PHASE_LIMIT (DAh). Refer to the PMBus™ MFR_OCP_PHASE_LIMIT (DAh) section on page 74 for more information.

Under-Voltage Protection (UVP)

If the output voltage is below V_{REF} - 325mV for the UVP blanking time, the system triggers UVP and immediately shuts down by turning off all phases (see Figure 15).

Normally, UVP can be triggered when the per-phase OCP current limit is reached, and the PWM signals are blocked by the per-phase OC signals (see Figure 16).

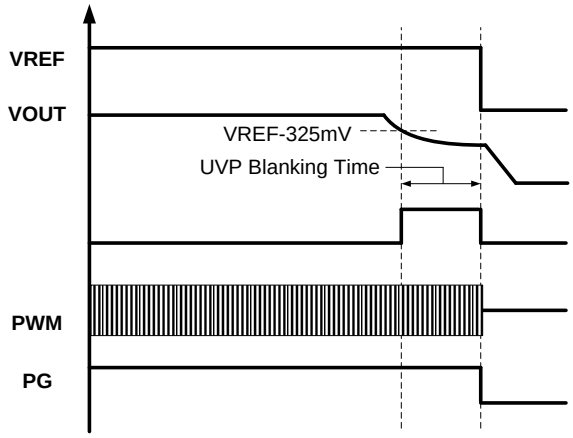


Figure 15: Under-Voltage Protection

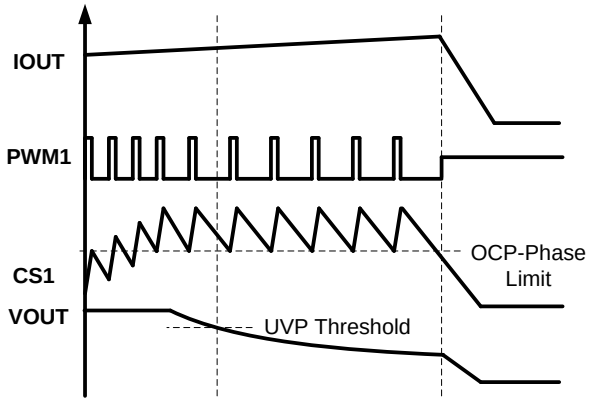


Figure 16: UVP Triggered when Per-Phase Current is Limited by OCP_PHASE

Over-Voltage Protection (OVP)

If the output voltage is above VO_OVP_LIMIT (V_{REF} + 325mV) for the OVP blanking time, the system triggers OVP and turns on all LS-FETs immediately to reduce the output voltage.

The OVP signals are blanked during the soft start and soft shutdown processes to prevent a false trigger by a pre-biased condition. The OVP signals are also blanked in decay mode.

If V_{OUT} > VOUT_OVP_LIMIT, V_{OUT} OVP occurs, the LS-FET is turned on to decrease V_{OUT} until it drops back to its normal level, and the fault state is latched. If V_{OUT} < VO_RVP_LIMIT (300mV), V_{OUT} reverse-voltage protection (RVP) occurs, and the LS-FET is turned off to prevent V_{OUT} from becoming negative.

Figure 17 shows the OVP waveforms of the MP2853.

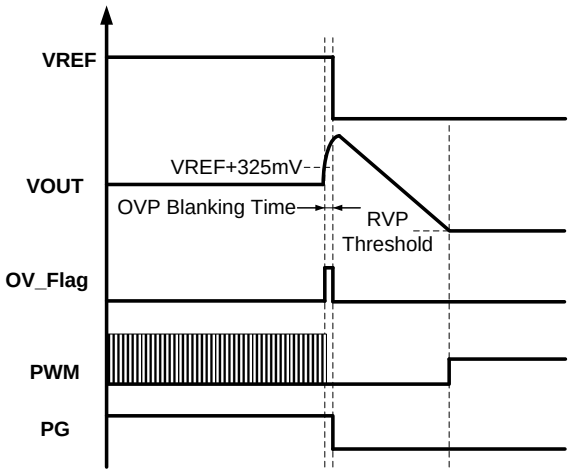


Figure 17: OVP Waveform

OCP_TDC, OCP_SPIKE, UVP, and OVP Modes

OCP_TDC, OCP_SPIKE, V_{OUT} UVP, and OVP can be programmed to no action, hiccup, retry six times, or latch-off mode via the PMBus™.

The controller takes no action in no action mode and continues switching until another protection is tripped. The fault indication bit in register MFR_FAULTS1 (84h) are not set in no action mode.

In hiccup mode, the controller shuts down the VR to disable the output and attempts to restart after a 12.5ms protection delay time.

In retry six times mode, the VR restarts six times at most at 12.5ms intervals. If the fault is removed within the six retries, the VR resumes normal operation. If the fault remains after six retries, the VR shuts down until the VDD33 power cycles, EN is toggled, or the PMBus™ command on is sent.

In latch mode, the VR shuts down until the VDD33 power cycles, EN is toggled, or the PMBus™ command on is sent.

Reverse-Voltage Protection (RVP)

A large reverse inductor current may cause negative output voltages that can harm the processor and other output components. The MP2853 provides RVP with no additional system cost.

When OVP occurs, all LS-FETs are forced on to discharge the voltage of the output capacitors quickly. The inductor current becomes very negative, which can discharge the voltage of the output capacitors negative enough to destroy the load without RVP.

With the RVP function, when the VOSEN voltage falls below 300mV after OVP, the MP2853 triggers RVP by latching all PWM outputs to tri-state. The reverse inductor current can quickly reset to 0A by dissipating the energy in the inductor to the input DC voltage source through the forward-biased body diode of the HS-FETs. The RVP function after OVP is shown in Figure 17.

Over-Temperature Warning and Protection

When the sensed temperature is above the over-temperature warning threshold set in register MFR_VRHOT_SET (D9h, Page 1), OCP_L asserts.

When the sensed temperature is above the over-temperature fault threshold, the controller shuts down the VR to disable the output. The controller can be programmed to either latch-off mode or auto-retry mode. In latch-off mode, the VR shuts down at OTP until the power cycles, EN toggles, or a command on turns it back on. In auto-retry mode, the VR shuts down at OTP and attempts to restart when the temperature falls below the OTP recovery threshold. The PMBus™ command MFR_OTP_SET (D9h, Page 0) programs the over-temperature threshold and responds to OTP.

EEPROM Fault

If the data in the EEPROM is checked as invalid by the CRC, then the system enters the EEPROM fault state and waits for the error to be cleared.

Communication Failure

A data transmission fault occurs when information is not transferred between the devices properly. There are several data transmission faults, listed below:

- Sending too few data
- Reading too few data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The data transmission faults assert ALT_P#. The CLEAR_FAULTS command de-asserts ALT_P#. If the faults still remain, ALT_P# asserts again.

VDIFF Short-Circuit Protection (SCP)

The MP2853 supports VDIFF short-circuit protection (SCP) to prevent the VR from over-voltage when VDIFF is shorted to GND by a fault. The VDIFF short circuit can be enabled with the PMBus™ command MFR_VDIFF_SCP_SET (ABh) bit[3]. This bit is active when boot-up starts. When a VDIFF short circuit is detected, the associated rail is shut down immediately, and the fault is reported with MFR_FAULTS1 (84h) bit[7] for Rail 1 and bit[12] for Rail 2.

VDIFF short circuit is only recommended when no external remote sensing divider is applied.

VTEMP and CS Fault Detection

The MP2853 supports VTEMP fault and CS fault detection. When the MP2853 detects that the voltage on VTEMP is above 2.2V or any CS pin is pulled down to 170mV, the VTEMP fault or CS fault is active, and the MP2853 starts the Intelli-Phase fault type detection. The MPS Intelli-Phase supports fault reporting either by pulling FAULT# low (like in the MP86945A) or pulling VTEMP high to 3.3V (like in the MP86936). The Intelli-Phase FAULT# pin can be connected to CS or VTEMP of the controller and the Intelli-Phase to shut down the VR and monitor the fault type when an Intelli-Phase fault occurs.

Figure 18a shows an Intelli-Phase fault type detection when working with the MP86945A. The FAULT# signal of each MP86945A is tied to its own CS pin. When a fault occurs on any MP86945A, its FAULT# signal asserts and pulls CS low.

Figure 18b shows an Intelli-Phase fault type detection when working with the MP86936.

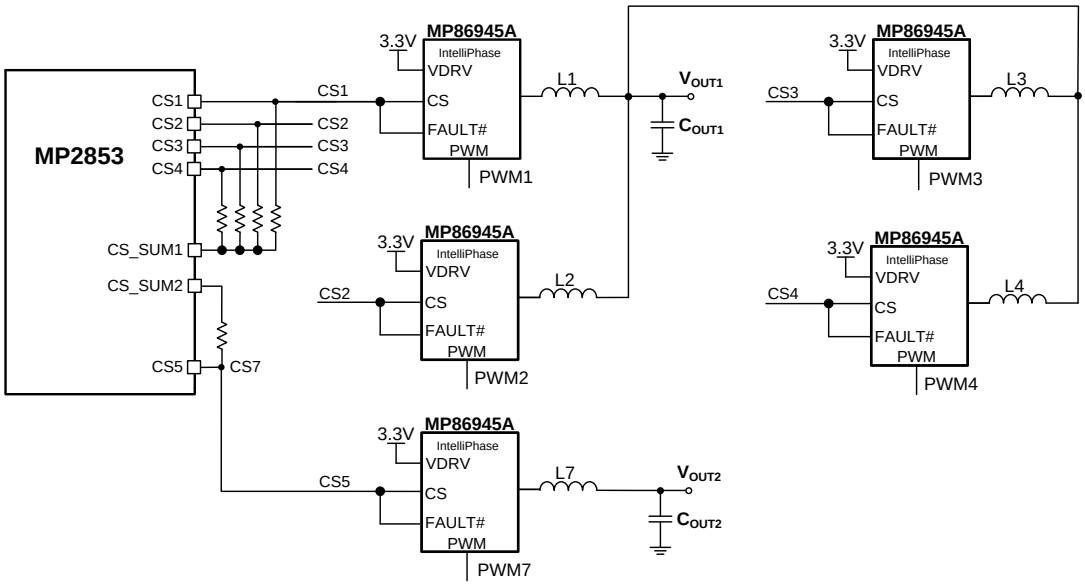


Figure 18a: Fault Detection from each CS of the MP86945A

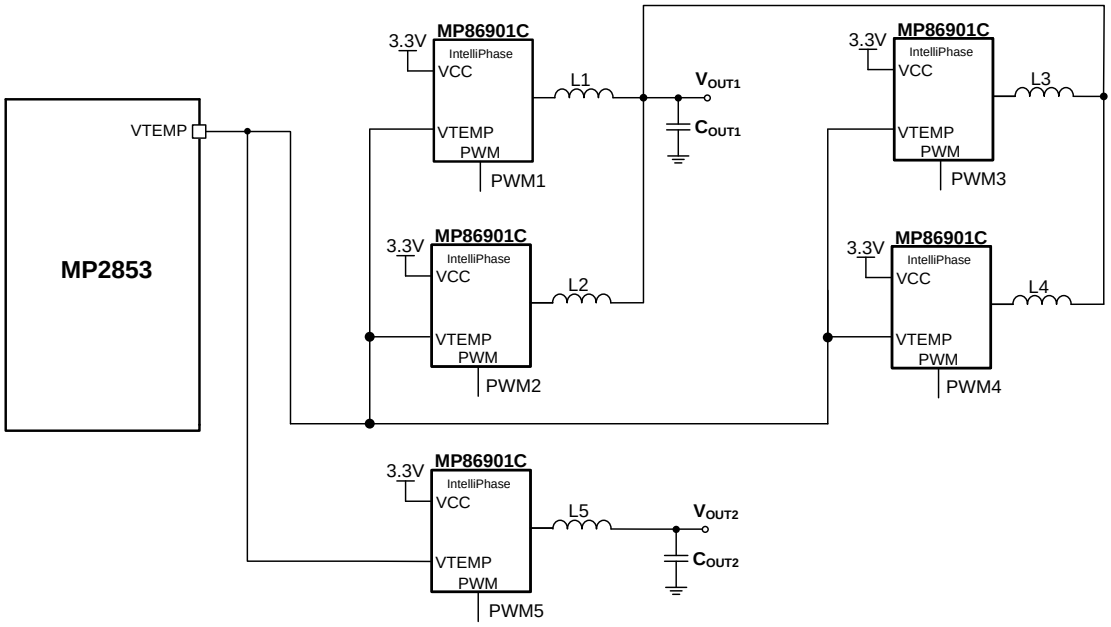


Figure 18b: Fault Detection from VTEMP of the MP86901C

Intelli-Phase Fault Detection

The MP2853 can detect the fault of the Intelli-Phase. There are several types of Intelli-Phase faults:

- Current limit
- Over-temperature
- LS-FET short
- HS-FET short

Intelli-Phase can support some or all of the faults protections above and report the fault type through the PWM pin. Refer to the datasheet of the Intelli-Phase for specific details.

The MP2853 scans the PWM fault after any of the following faults occurs: V_{IN} UVLO, V_{IN} OVP, OTP, V_{OUT} UVP, V_{OUT} OVP, OCP_TDC, OCP_SPIKE, VDIFF short to GND, VTEMP fault, and CS fault if fault protection and PWM fault detection are both enabled.

As shown in Figure 19, when any of the above faults occur, the MP2853 shuts off the associated rail(s) and starts the Intelli-Phase fault type scan for related rail(s) by sensing the voltage on PWM. Faults are reported to Page 0's registers MFR_FAULT1 (84h), MFR_FAULT2 (85h), and MFR_FAULT3 (86h). Faults are recorded to the EEPROM (Page 29's registers EDh, EEh, and EFh) when fault recording to the EEPROM is enabled. The last fault event is stored. To achieve fault storing into the EEPROM, the EN signal should be kept high for at least 20ms after the fault occurs.

The related registers mentioned below are used to program the behavior of fault detection and recording in case an Intelli-Phase fault occurs.

1. EN of the fault protections with individual fault protection registers.
2. EN of ADC to sample the fault type from all PWM pins of the Intelli-Phase ((MFR_PRT_CONFIG (DCh) bit[5:4]).
3. EN to record the fault to the EEPROM ((MFR_PRT_CONFIG (DCh) bit[8]).

If the fault stored in the EEPROM is enabled, the last event of the fault triggered is recorded to Page 29's registers EDh, EEh, and EFh. The detail of the fault type is shown in the description of registers EDh, EEh, and EFh on page 118. The EN signal must be keep high for at least 20ms after the fault occurs.

To clear the recorded fault in the EEPROM register, 0x0000 must be written to these registers (EDh, EEh, and EFh, Page 29). This is a direct access to the EEPROM registers. The time required for each write command is 5ms.

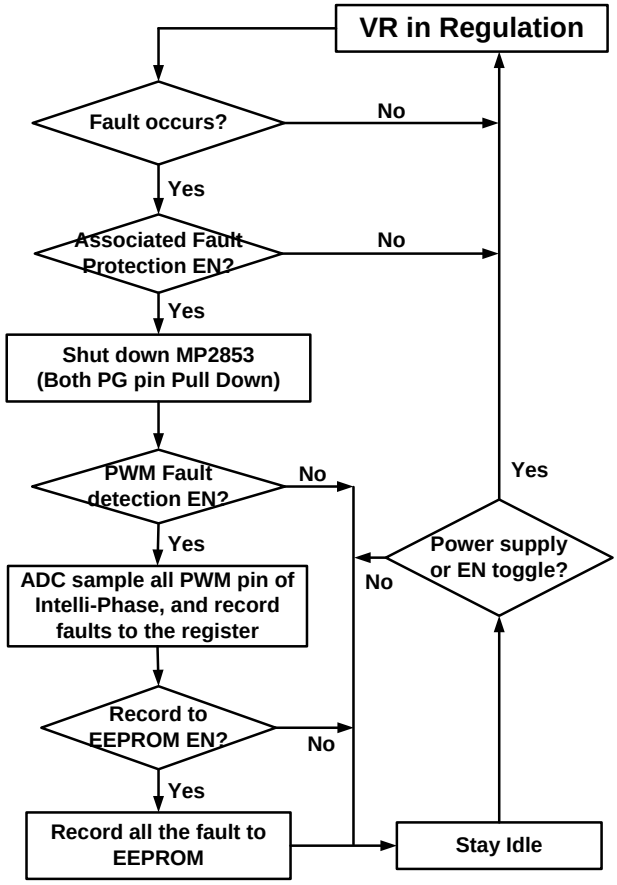


Figure 19: Flow Chart of Intelli-Phase Fault Detection

PMBUS™/I²C INTERFACE

General Description

The power management bus (PMBus™) is an open-standard, power-management protocol that defines a means of communicating with power conversion and other devices. The PMBus™ is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. This is based on the principles of I²C operation.

The MP2853 supports PMBus™/I²C transmission with PEC. Figure 20a shows the supported PMBus™/I²C transmission structure without PEC.

Figure 20b shows the supported PMBus™/I²C transmission structure with PEC.

There are five kinds of transmission structures:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

To read or write the registers of the MP2853, the PMBus™ or I²C command must be compliant with the byte number of the register in the table of PMBus™ commands for Rail 1 or Rail 2.

The MP2853 supports 100kHz, 400kHz, and 1MHz bus timing requirements. Timing and electrical characteristics of the PMBus™ can be found in the Electrical Characteristics section on page 8, or in the PMB Power Management Protocol Specification, part 1, revision 1.3 available at http://PMBus.org.

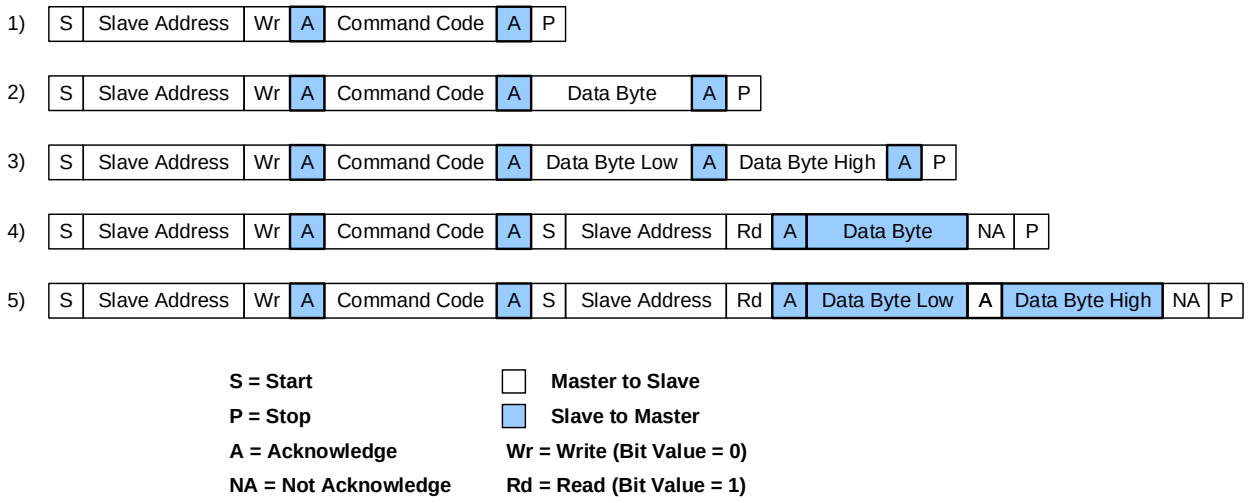


Figure 20a: Supported PMBus™/I²C Transmission Structure without PEC

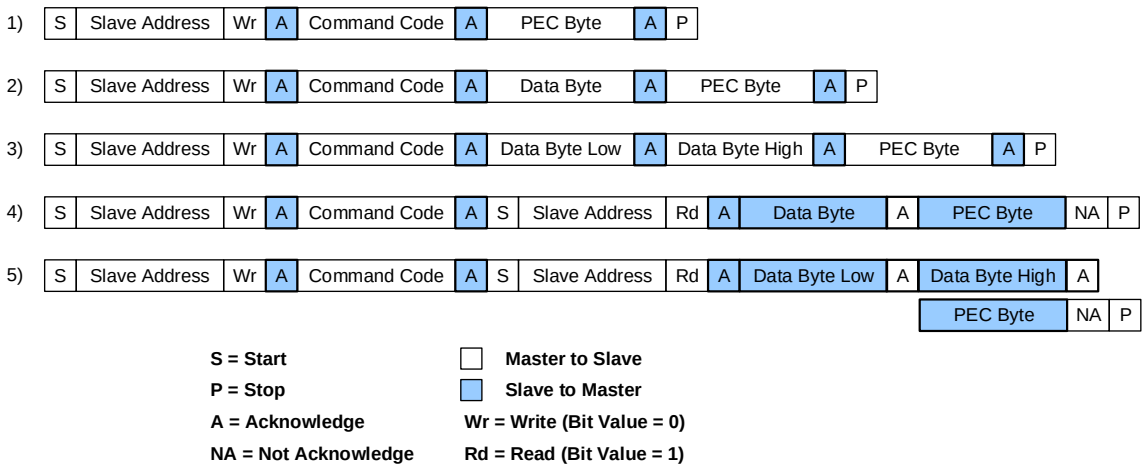


Figure 20b: Supported PMBus™/I²C Transmission Structure with PEC

PMBus™/I²C Address

To support multiple VR devices used with the same PMBus™ interface, the MP2853 provides PMBus™ address programming either by ADDR or by register MFR_ADDR_PMBUS (EDh, Page 0).

The PMBus™ address is a 7-bit code and ranges from 0x00 to 0x7F. The 3MSB bit is set by the register. The 4LSB bit address can be set by the register or by the ADDR voltage.

Register MFR_ADDR_PMBUS (EDh, Page 0) is used to program or store the PMBus™ address. Bit[7] sets the PMBus™ address 4LSB bit configuration mode. When bit[7] = 0, the 4LSB bit is determined by the ADDR voltage and stored in register EDh bit[3:0].

The ADDR voltage can be programmed by a resistor divider from VDD18 to AGND, and the midpoint of the divider is connected to ADDR. Figure 21 shows the recommended connections for ADDR. Table 6 shows the resistor values for different PMBus™ addresses.

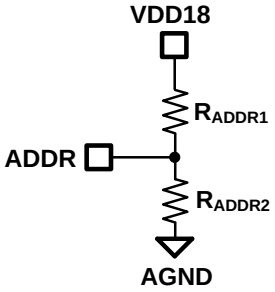


Figure 21: ADDR Circuit Design

Table 6: Pin Configuration for PMBus™ Address

PMBus™ Address	V_{ADDR} (V)	R_{ADDR1} (kΩ) 1%	R_{ADDR2} (kΩ) 1%
20h	0	-	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

The addresses in Table 7 are reserved by the PMBus™/I²C protocol. They must not be used or assigned to the MP2853.

Table 7: Reserved PMBus™ Address

PMBus™ Address Bit[6:0]	WR Bit[0]	Comment
000 0000	0	General call address
000 0000	1	Start byte
000 0001	X	CBUS address
000 0010	X	Address reserved for different bus format
000 0011	X	Reserved
000 01XX	X	Reserved
010 1000	X	Reserved for ACCESS bus host
011 0111	X	Reserved for ACCESS bus host default address
111 10XX	X	10-bit slave addressing
111 11XX	X	Reserved
000 1000	X	Host
000 1100	X	Alert response address
110 0001	X	PMBus™ device default address

Data and Numerical Formats

The MP2853 uses a direct format internally to represent real-world values such as voltage, current, temperature, time, etc.

All numbers with no suffix in this document are a decimal unless explicitly designated otherwise.

Numbers in binary format are indicated by the prefix “n’b”, where n is the binary count. For example, 3’b000 indicates a 3-bit binary data. The data is 000.

The suffix “h” indicates a hexadecimal format, which is generally used for the register address number in this document.

The symbol “0x” indicates a hexadecimal format, which is used for the value in the register. For example, 0x88 is a 1-byte number whose decimal value is 136.

PMBus™/I²C Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults listed below:

- Sending too few data
- Reading too few data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The data transmission faults assert ALT_P#. The CLEAR_FAULTS (03h) command de-asserts ALT_P#, but if the faults still remain, ALT_P# asserts again.

PMBus™/I²C Reporting and Status Monitoring

The MP2853 supports real-time monitoring for the VR operation parameters and status with PMBus™ and SVI interface. Table 8 lists the monitored parameters.

Table 8: PMBus™ Monitored Parameters

Parameter	PMBus™
Output voltage	6.25mV/LSB
Output current	0.25A/LSB
Temperature	1°C
Input voltage	0.25V/LSB
OVP	✓
UVP	✓
OCP	✓
OTP	✓
V_{IN} UVLO	✓
V_{IN} OV	✓
VDIFF SCP	✓
CS fault	✓
VTEMP fault	✓
CML	✓

SVI2.0 Interface

The MP2853 supports all SVI 2.0 commands. The AMD SVD packet structure is shown in Figure 22. Table 9 shows the SVI 2.0 commands.

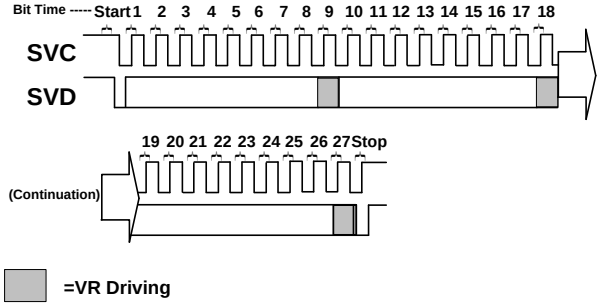


Figure 22: SVD Packet Structure

Table 9: SVD Packet from CPU to VR

Bit	Description
1:5	Always 11000b
6	VDD1 domain selector bit
7	VDD2 domain selector bit
8	Always 0b
9	Acknowledge bit
10	PSI0_L
11:17	VID code bits [7:1]
18	Acknowledge bit
19	VID code bits [0]
20	PSI1_L
21	TFN
22:24	Load line slope trim [2:0]
25:26	Offset trim [1:0]
27	Acknowledge bit

Table 10 shows the definition of the PSI0_L and PSI1_L bits.

Table 10: PSI0_L and PSI1_L Definition

Function	Description
PSI0_L	Power state indicates level 0. When this signal is asserted (active low), the processor is in a low enough power state for the MP2853 to take action to boost efficiency by dropping the phases to 1-phase CCM.
PSI1_L	Power state indicates level 1. When this signal is asserted (active low) together with PSI0_L asserted, the processor is in a low enough power state for the MP2853 to take additional action to boost efficiency by forcing the only working phase into diode emulation mode.

The TFN bit and the core and Northbridge domain selector bits are used by the processor to change the functionality of the telemetry (see Table 11).

Table 11: TFN = 1 Truth Table

VDD1	VDD2	Description
0	1	Telemetry is in voltage and current mode. Therefore, the voltage and current are sent for VDD1 and VDD2 domains by the controller.
0	0	Telemetry is in voltage mode only. Only the voltage of the VDD1 and VDD2 domains is sent by the controller.
1	0	Telemetry is disabled.
1	1	Reserved.

In SVI VID mode, the MP2853 uses the PMBus™ command MFR_VR_CONFIG4 (0Eh, Page 0) bit[0] to assign the internal rail numbers to the VDD1 and VDD2 domains.

When bit[0] = 0, Rail 1 is assigned to VDD1, while Rail 2 is assigned to VDD2. PG_A asserts when the MP2853's Rail 1 power is in regulation. PG_B asserts when the MP2853's Rail 2 power is in regulation. The PMBus™ command READ_VOUT (8Bh, Page 0) returns the output voltage of Rail 1, and READ_VOUT (8Bh, Page 1) returns the output voltage of Rail 2. SVT reports the V_{OUT}/I_{OUT} of Rail 1 to VDD1, and reports the V_{OUT}/I_{OUT} of Rail 2 to VDD2.

When bit[0] = 1, Rail 2 is assigned to VDD1, while Rail 1 is assigned to VDD2. PG_A asserts when the MP2853 Rail 2 power is in regulation, PG_B asserts when the MP2853 Rail 1 power is in regulation. The PMBus™ command READ_VOUT (8Bh, Page 0) returns the output voltage of Rail 2, and READ_VOUT (8Bh, Page 1) returns the output voltage of Rail 1. SVT reports the V_{OUT}/I_{OUT} of Rail 2 to VDD1, and reports the V_{OUT}/I_{OUT} of Rail 1 to VDD2.

Refer to the MFR_VR_CONFIG4 (0Eh, Page 0) section on page 42 for more information.

PVID Mode

The MP2853 supports 3-bit PVID mode to control V_{OUT} by setting the PMBUS_SEL_R_X bit in register D0h and the SVI_PVID_SEL_R_X bits in register C4h (see Figure 4).

The PVID mode pins (PVID1, PVID2, and PVID3) are muxed from SVD, SVC, and PWROK. In PVID mode, SVI communication is disabled. When any of the PVID pins toggle, the corresponding PVID_VID value is read from the EEPROM as the new target VID. There are eight types of PVID voltages with eight different combinations of H/L of PVID1, PVID2, and PVID3. These PVID voltage values should be pre-programmed into the EEPROM via the PMBus™.

The register F0h~F7h in EEPROM Page 29 (write 0x29 to register PAGE (00h)) is for PVID voltage programming with 6.25mV/LSB. In Page 29, the PMBus™ can read or write the PVID voltages via Table 12. The PVID voltage can be executed by toggling the PVID pins.

Table 12: PVID_VID in EEPROM

PVID3 PWROK	PVID2 (SVC)	PVID1 (SVD)	PVID Voltage	EEPROM ADDRESS	
				VID Rail 1	VID Rail 2
L	L	L	PVID_000	F0h[15:8]	F0h[7:0]
L	L	H	PVID_001	F1h[15:8]	F1h[7:0]
L	H	L	PVID_010	F2h[15:8]	F2h[7:0]
L	H	H	PVID_011	F3h[15:8]	F3h[7:0]
H	L	L	PVID_100	F4h[15:8]	F4h[7:0]
H	L	H	PVID_101	F5h[15:8]	F5h[7:0]
H	H	L	PVID_110	F6h[15:8]	F6h[7:0]
H	H	H	PVID_111	F7h[15:8]	F7h[7:0]

In PVID mode, the power good flag asserts after the VBOOT VID target is reached and de-asserts when EN is pull low or the protection is triggered to shut down the VR.

VID Offset for Over-Clocking

The MP2853 can add an offset voltage to the VID command. Register MFR_OFFSET_SET (DFh) is for offset setting (6.25mV/LSB).

Refer to the MFR_OFFSET_SET (DFh) section on page 78 for more information.

The special VID offset (DFh bit[14:7]) is applied for all VID modes (i.e.: SVI, PMBus™, or PVID mode).

The initial offset (DFh bit[6:0]) is applied to SVI mode only.

The target output voltage is the sum of the VID and the offset. The offset is not applied at 0V VID command. When the 0V VID command is received, the target output voltage is 0V.

The maximum output voltage is limited by the VOUT_MAX setting.

If the output voltage range is higher than 1.55V, the ½x VDIFF gain must be enabled to allow the voltage to exceed 1.55V up to 3.0V.

With a regular VDIFF gain (1x, default value), the maximum output voltage is up to 1.55V.

Changing the offset value on-the-fly acts the same as dynamic VID operation. The ramping up/down voltage slew rate is the same as dynamic VID voltage slew rate.

SVI Debug Mode

The MP2853 provides a debug mode with PWM1/5. In debug mode, if PWM1 is pulled up to 3.3V with a resistor, Rail 1 is disabled, and the associated PG signal can either assert immediately or de-assert. If PWM5 is pulled up to 3.3V with a resistor, Rail 2 is disabled, and the associated PG signal can either assert immediately or de-assert. Any VID codes sent to the disabled rail are ignored by the VR. This debug feature can help debug the hardware platform more easily.

The debug mode and the PG behavior can be programmed with the PMBus™ command MFR_VR_CONFIG (D0h, Page 0) bit[13] and bit[12]. Refer to the MFR_VR_CONFIG (D0h, Page 0) section for more information.

SERIAL VID CODES

SVID[7:0]	Voltage (V)		SVID[7:0]	Voltage (V)		SVID[7:0]	Voltage (V)		SVID[7:0]	Voltage (V)	
0000_0000	1.55000		0010_0000	1.35000		0100_0000	1.15000		0110_0000	0.95000	
0000_0001	1.54375		0010_0001	1.34375		0100_0001	1.14375		0110_0001	0.94375	
0000_0010	1.53750		0010_0010	1.33750		0100_0010	1.13750		0110_0010	0.39750	
0000_0011	1.53125		0010_0011	1.33125		0100_0011	1.13125		0110_0011	0.93125	
0000_0100	1.52500		0010_0100	1.32500		0100_0100	1.12500		0110_0100	0.92500	
0000_0101	1.51875		0010_0101	1.31875		0100_0101	1.11875		0110_0101	0.91875	
0000_0110	1.51250		0010_0110	1.31250		0100_0110	1.11250		0110_0110	0.91250	
0000_0111	1.50625		0010_0111	1.30625		0100_0111	1.10625		0110_0111	0.90625	
0000_1000	1.50000		0010_1000	1.30000		0100_1000	1.10000		0110_1000	0.90000	
0000_1001	1.49375		0010_1001	1.29375		0100_1001	1.09375		0110_1001	0.89375	
0000_1010	1.48750		0010_1010	1.28750		0100_1010	1.08750		0110_1010	0.88750	
0000_1011	1.48125		0010_1011	1.28125		0100_1011	1.08125		0110_1011	0.88125	
0000_1100	1.47500		0010_1100	1.27500		0100_1100	1.07500		0110_1100	0.87500	
0000_1101	1.46875		0010_1101	1.26875		0100_1101	1.06875		0110_1101	0.86875	
0000_1110	1.46250		0010_1110	1.26250		0100_1110	1.06250		0110_1110	0.86250	
0000_1111	1.45625		0010_1111	1.25625		0100_1111	1.05625		0110_1111	0.85625	
0001_0000	1.45000		0011_0000	1.25000		0101_0000	1.05000		0111_0000	0.85000	
0001_0001	1.44375		0011_0001	1.24375		0101_0001	1.04375		0111_0001	0.84375	
0001_0010	1.43750		0011_0010	1.25750		0101_0010	1.03750		0111_0010	0.83750	
0001_0011	1.43125		0011_0011	1.23125		0101_0011	1.03125		0111_0011	0.83125	
0001_0100	1.42500		0011_0100	1.22500		0101_0100	1.02500		0111_0100	0.82500	
0001_0101	1.41875		0011_0101	1.21875		0101_0101	1.01875		0111_0101	0.81875	
0001_0110	1.41250		0011_0110	1.21250		0101_0110	1.01250		0111_0110	0.81250	
0001_0111	1.40625		0011_0111	1.20625		0101_0111	1.00625		0111_0111	0.80625	
0001_1000	1.40000		0011_1000	1.20000		0101_1000	1.00000		0111_1000	0.80000	
0001_1001	1.39375		0011_1001	1.19375		0101_1001	0.99375		0111_1001	0.79375	
0001_1010	1.38750		0011_1010	1.18750		0101_1010	0.98750		0111_1010	0.78750	
0001_1011	1.38125		0011_1011	1.18125		0101_1011	0.98125		0111_1011	0.78125	
0001_1100	1.37500		0011_1100	1.17500		0101_1100	0.97500		0111_1100	0.77500	
0001_1101	1.36875		0011_1101	1.16875		0101_1101	0.96875		0111_1101	0.76875	
0001_1110	1.36250		0011_1110	1.16250		0101_1110	0.96250		0111_1110	0.76250	
0001_1111	1.35625		0011_1111	1.15625		0101_1111	0.95625		0111_1111	0.75625	

SERIAL VID CODES *(continued)*

SVID[7:0]	Voltage (V)		SVID[7:0]	Voltage (V)		SVID[7:0]	Voltage (V)		SVID[7:0]	Voltage (V)	
1000_0000	0.75000		1010_0000	0.55000		1100_0000	0.35000	*	1110_0000	0.15000	*
1000_0001	0.74375		1010_0001	0.54375		1100_0001	0.34375	*	1110_0001	0.14375	*
1000_0010	0.73750		1010_0010	0.53750		1100_0010	0.33750	*	1110_0010	0.13750	*
1000_0011	0.73125		1010_0011	0.53125		1100_0011	0.33125	*	1110_0011	0.13125	*
1000_0100	0.72500		1010_0100	0.52500		1100_0100	0.32500	*	1110_0100	0.12500	*
1000_0101	0.71875		1010_0101	0.51875		1100_0101	0.31875	*	1110_0101	0.11875	*
1000_0110	0.71250		1010_0110	0.51250		1100_0110	0.31250	*	1110_0110	0.11250	*
1000_0111	0.70625		1010_0111	0.50625		1100_0111	0.30625	*	1110_0111	0.10625	*
1000_1000	0.70000		1010_1000	0.50000	*	1100_1000	0.30000	*	1110_1000	0.10000	*
1000_1001	0.69375		1010_1001	0.49375	*	1100_1001	0.29375	*	1110_1001	0.09375	*
1000_1010	0.68750		1010_1010	0.48750	*	1100_1010	0.28750	*	1110_1010	0.08750	*
1000_1011	0.68125		1010_1011	0.42125	*	1100_1011	0.28125	*	1110_1011	0.08125	*
1000_1100	0.67500		1010_1100	0.47500	*	1100_1100	0.27500	*	1110_1100	0.07500	*
1000_1101	0.66875		1010_1101	0.46875	*	1100_1101	0.26875	*	1110_1101	0.06875	*
1000_1110	0.66250		1010_1110	0.46250	*	1100_1110	0.26250	*	1110_1110	0.06250	*
1000_1111	0.65625		1010_1111	0.45625	*	1100_0111	0.25625	*	1110_1111	0.05625	*
1001_0000	0.65000		1011_0000	0.45000	*	1101_0000	0.25000	*	1111_0000	0.05000	*
1001_0001	0.64375		1011_0001	0.44375	*	1101_0001	0.24375	*	1111_0001	0.04375	*
1001_0010	0.63750		1011_0010	0.43750	*	1101_0010	0.23750	*	1111_0010	0.03750	*
1001_0011	0.63125		1011_0011	0.43125	*	1101_0011	0.23125	*	1111_0011	0.03125	*
1001_0100	0.62500		1011_0100	0.42500	*	1101_0100	0.22500	*	1111_0100	0.02500	*
1001_0101	0.61875		1011_0101	0.41875	*	1101_0101	0.21875	*	1111_0101	0.01875	*
1001_0110	0.61250		1011_0110	0.41250	*	1101_0110	0.21250	*	1111_0110	0.01250	*
1001_0111	0.60625		1011_0111	0.40625	*	1101_0111	0.20625	*	1111_0111	0.00625	*
1001_1000	0.60000		1011_1000	0.40000	*	1101_1000	0.20000	*	1111_1000	OFF	*
1001_1001	0.59375		1011_1001	0.39375	*	1101_1001	0.19375	*	1111_1001	OFF	*
1001_1010	0.58750		1011_1010	0.38750	*	1101_1010	0.18750	*	1111_1010	OFF	*
1001_1011	0.58125		1011_1011	0.38125	*	1101_1011	0.18125	*	1111_1011	OFF	*
1001_1100	0.57500		1011_1100	0.37500	*	1101_1100	0.17500	*	1111_1100	OFF	*
1001_1101	0.56875		1011_1101	0.36875	*	1101_1101	0.16875	*	1111_1101	OFF	*
1001_1110	0.56250		1011_1110	0.36250	*	1101_1110	0.16250	*	1111_1110	OFF	*
1011_1111	0.55625		1011_1111	0.35625	*	1101_1111	0.15625	*	1111_1111	OFF	*

* Indicates TOB is 80mV for this VID code.

PMBUS™ COMMANDS FOR PAGE 0 AND PAGE 1

Command Code	Command Name	Type	Bytes	Page 0	Page 1
00h	PAGE	r/w	1	✓	✓
01h	OPERATION	r/w	1	✓	✓
03h	CLEAR_FAULTS	Send	0	✓	
0Ch	CONFIG_REV_USER	r/w	2		✓
0Eh	MFR_VR_CONFIG4	r/w	2	✓	
15h	STORE_USER_ALL	Send	0	✓	
16h	RESTORE_USER_ALL	Send	0	✓	
21h	VOUT_COMMAND	r/w	2	✓	✓
22h	VOUT_TRIM	r/w	2	✓	✓
24h	VOUT_MAX	r/w	2	✓	✓
25h	VOUT_MARGIN_HIGH	r/w	2	✓	✓
26h	VOUT_MARGIN_LOW	r/w	2	✓	✓
29h	VOUT_SCALE_LOOP	r/w	2	✓	✓
2Ch	MFR_SLOPE_SW_INI	r/w	1	✓	✓
33h	FREQUENCY_SWITCH	r/w	2	✓	✓
35h	VIN_ON	r/w	2	✓	
36h	VIN_OFF	r/w	2	✓	
55h	VIN_OV_FAULT_LIMIT	r/w	2	✓	
60h	TON_DELAY	r/w	2	✓	✓
61h	TON_RISE	r/w	2	✓	✓
64h	TOFF_DELAY	r/w	2	✓	✓
65h	TOFF_FALL	r/w	2	✓	✓
84h	MFR_FAULTS1	r	2	✓	
85h	MFR_FAULTS2	r	2	✓	
86h	MFR_FAULTS3	r	2	✓	
87h	MFR_CML	r	1	✓	
88h	READ_VIN	r	2	✓	
8Bh	READ_VOUT	r	2	✓	✓
8Ch	READ_IOUT	r	2	✓	✓
8Dh	READ_TEMPERATURE	r	2	✓	
A6h	MFR_SD_VID	r/w	1	✓	✓
A8h	MFR_PSI_TRIM	r/w	2	✓	✓
A9h	MFR_PG_RDL	r/w	2	✓	✓
ABh	MFR_VDIFF_SCP_SET	r/w	1	✓	
ACh	VOUT_VR_CAL	r/w	2	✓	✓
ADh	IOUT_VR_CAL	r/w	2	✓	✓
C0h	MFR_PHASE_PSI_CFG	r/w	1	✓	
	MFR_PSI_SET	r/w	1		✓
C2h	MFR_OCP_SET	r/w	2	✓	✓
C3h	MFR_DELAY_SET	r/w	2	✓	✓

PMBUS™ COMMANDS FOR PAGE 0 AND PAGE 1 *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1
C4h	MFR_VR_CONFIG3	r/w	2	✓	
C5h	IOUT_CAL_CFG	r/w	2	✓	✓
C6h	MFR_RES_DROOP_0P2	r/w	1	✓	✓
C7h	MFR_AUTO_PS	r/w	2	✓	✓
C8h	MFR_23PHASE_LOW	r/w	2	✓	
C9h	MFR_DECAY_SET	r/w	1	✓	✓
CAh	MFR_CUR_OFFSET	r/w	1	✓	✓
CBh	MFR_BOOT_SR	r/w	2	✓	✓
CCh	MFR_OCPSPIKE_12PS_LEVEL	r/w	2	✓	✓
CDh	MFR_OCPSPIKE_34PS_LEVEL	r/w	2	✓	
CEh	MFR_OCPTDC_12PS_LEVEL	r/w	2	✓	✓
CFh	MFR_OCPTDC_34PS_LEVEL	r/w	2	✓	
D0h	MFR_VR_CONFIG	r/w	2	✓	
D1h	MFR_CS_OFFSET	r/w	2	✓	✓
D2h	MFR_TEMP_CAL	r/w	2	✓	
D3h	MFR_CUR_GAIN	r/w	2	✓	✓
D4h	MFR_VIN_SCALE_LOOP	r/w	1	✓	
D5h	MFR_VID_OFF	r/w	2		✓
D6h	MFR_OCP_ACTIONDELAY	r/w	2	✓	✓
D7h	MFR_OVP_SET	r/w	2	✓	✓
D8h	MFR_UVP_SET	r/w	2	✓	✓
D9h	MFR_OTP_SET	r/w	2	✓	
	MFR_VRHOT_SET	r/w	2		✓
DAh	MFR_OCP_PHASE_LIMIT	r/w	2	✓	✓
DBh	MFR_ADP_CTRL	r/w	2	✓	✓
DCh	MFR_PRT_CONFIG	r/w	2	✓	
	MFR_EEPROM_WP	r/w	2		✓
DDh	MFR_LL_LIMIT_SET	r/w	2	✓	✓
DEh	MFR_SLOPE_SR_URS	r/w	1	✓	✓
DFh	MFR_OFFSET_SET	r/w	2	✓	✓
E0h	MFR_OSR_SET	r/w	2	✓	
E1h	MFR_BLANK_ TIME	r/w	2	✓	
	MFR_PWM_MIN_TIME	r/w	2		✓
E2h	MFR_SLOPE_SR_2PS	r/w	2	✓	✓
E3h	MFR_SLOPE_CNT_2PS	r/w	2	✓	✓
E4h	MFR_SLOPE_SR_1PS	r/w	2	✓	✓
E5h	MFR_SLOPE_CNT_1PS	r/w	2	✓	✓
E6h	MFR_SLOPE_SR_0P5PS	r/w	2	✓	✓
E7h	MFR_SLOPE_CNT_0P5PS	r/w	2	✓	✓
E8h	MFR_SLOPE_SR_4PS	r/w	2	✓	
E9h	MFR_SLOPE_CNT_34PS	r/w	2	✓	

PMBUS™ COMMANDS FOR PAGE 0 AND PAGE 1 *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1
EAh	MFR_SLOPE_SR_3PS	r/w	2	✓	
ECh	MFR_TRIM_34PS	r/w	2	✓	
EDh	MFR_ADDR_PMBUS	r/w	2	✓	
	MFR_LAST_FAULTS1	r	2		✓
EEh	MFR_LAST_FAULTS2	r	2		✓
EFh	VENDOR_ID	r/w	2	✓	
	MFR_LAST_FAULTS3	r	2		✓
F0h	PRODUCT_ID	r/w	1	✓	
F1h	CONFIG_ID	r/w	1	✓	
F2h	PRODUCT_REV_MPS	r/w	1	✓	
F3h	INTELLI-PHASE_CS_GAIN	r/w	1	✓	
F6h	MFR_SAMP_LPF	r/w	1	✓	
F7h	MFR_VR_CONFIG2	r/w	2	✓	
F9h	MFR_TIMEOUT	r/w	2	✓	
FFh	CLEAR_EEPROM_FAULTS	Send	0	✓	

PMBUS™ COMMANDS FOR EEPROM (PAGE 29)

Command Code	Command Name	Type	Bytes	Page 29
EDh	MFR_STORE_FAULTS1	ROM	2	✓
EEh	MFR_STORE_FAULTS2	ROM	2	✓
EFh	MFR_STORE_FAULTS3	ROM	2	✓
F0h	PVID_VID1	ROM	2	✓
F1h	PVID_VID2	ROM	2	✓
F2h	PVID_VID3	ROM	2	✓
F3h	PVID_VID4	ROM	2	✓
F4h	PVID_VID5	ROM	2	✓
F5h	PVID_VID6	ROM	2	✓
F6h	PVID_VID7	ROM	2	✓
F7h	PVID_VID8	ROM	2	✓

PAGE 0 REGISTER MAP

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor through only one physical address for both rails and test mode.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PAGE							

Bits	Bit Name	Description
7:0	PAGE	8'b 0000 0000: Page 0, all commands address Rail 1 unless otherwise noted. 8'b 0000 0001: Page 1, all commands address Rail 2 unless otherwise noted. 8'b 0000 0010: Page 2, all commands address test mode. 8'b 0010 1000: Page 28, all commands address to EEPROM register Page 0. 8'b 0010 1001: Page 29, all commands address to EEPROM register Page 1. Others: ineffective input.

OPERATION (01h)

The OPERATION command on Page 0 is used to turn the Rail 1 output on and off in conjunction with input from EN. OPERATION is also used to set the output voltage to the upper or lower margin voltages. Rail 1 remains in the command operating mode until a subsequent OPERATION command or a state altering EN changes Rail 1 to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	OPERATION_MODE							

Bits	Bit Name	Description
7:0	OPERATION_MODE	Sets the operation mode for Rail 1. 8'b 00xx xxxx: Hi-Z off 8'b 01xx xxxx: soft off 8'b 1000 xxxx: normal on 8'b 1001 xxxx: margin low 8'b 1010 xxxx: margin high The value of "x" does not matter.

For example, when sending OPERATION (01h) = 0x40 via the PMBus™, the Rail 1 V_{OUT} shuts down softly. When sending OPERATION (01h) = 0x90 via the PMBus™, Rail 1 changes to a margin-low output voltage level with a dynamic VID (DVID) slew rate. When sending OPERATION (01h) = 0xA0 via the PMBus™, Rail 1 changes to a margin-high output voltage level with a DVID slew rate.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear the system fault after system initialization ends. This command is write only. There is no data byte for this command.

CLEAR_FAULTS is effective for both rails regardless of the PAGE command value. Faults include V_{IN} UVLO, V_{IN} OVP, OTP, output OVP, UVP, OCP_TDC, OCP_SPIKE, VDIFF SCP protections, PMBus™ communication faults, and EEPROM faults. CLEAR_FAULTS can only clear faults after an OPERATION command off cycle. Once CLEAR_FAULTS is sent, the faults listed above on both rails are cleared, and the fault bits in register MFR_FAULTS1~3 (84h~86h) are reset if the associated fault is removed.

MFR_VR_CONFIG4 (0Eh)

The MFR_VR_CONFIG4 command is used to set MP2853 rails assignments in SVI mode, T_{ON} limitation, and AC load-line regulation bandwidth.

Command	MFR_VR_CONFIG4															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	X				

Bits	Bit Name	Description
15:4	RESERVED	Unused. Always set to 0.
3	AC_LL_BW_SEL_R2	Selects the bandwidth of the AC load line regulation loop (for Rail 2 only). 1'b0: 25kHz 1'b1: 50kHz
2	AC_LL_BW_SEL_R1	Selects the bandwidth of the AC load line regulation loop (for Rail 1 only). 1'b0: 25kHz 1'b1: 50kHz
1	TON_LIMIT_EN	The final T_{ON} is determined by TON_set + ΔTon_fs_loop + ΔTon_CB_loop, where Ton_set is determined by the switching frequency set in register FREQUENCY_SWITCH (33h), V_{IN}, and V_{OUT}; ΔTon_fs_loop is the T_{ON} component regulated by the frequency loop; and ΔTon_CB_loop is the T_{ON} component regulated by the current balance loop. This bit is the enable bit to limit the final T_{ON} to the minimum on time (TON_MIN) and hold the frequency loop and current balance loop simultaneously when the calculated final T_{ON} < 0. TON_MIN is set in register MFR_PWM_MIN_TIME (E1h, Page 1). Set this bit to 1 for normal operation. 1'b0: disables the PWM on time limitation when the final T_{ON} < 0 1'b1: enables the PWM on time limitation to TON_MIN when the final T_{ON} < 0
0	SVI_RAIL_ASSIGN	Assigns the MP2853 rail number, PG indication, and output voltage/current report registers to AMD SVI2's VDD1 and VDD2 domain. 1'b0: VDD1 = Rail 1, VDD2 = Rail 2. PG_A asserts when MP2853 Rail 1 is in regulation. PG_B asserts when MP2853 Rail 2 is in regulation. READ_VOUT (8Bh, Page 0) returns the output voltage of Rail 1. READ_VOUT (8Bh, Page 1) returns the output voltage of Rail 2. In SVI VID mode, SVT reports the V_{OUT}/I_{OUT} of Rail 1 to VDD1 and V_{OUT}/I_{OUT} of Rail 2 to VDD2. 1'b1: VDD1 = Rail 2, VDD2 = Rail 1. PG_A asserts when the MP2853 Rail 2 power is ready. PG_B asserts when the MP2853 Rail 1 power is ready. READ_VOUT (8Bh, Page 0) returns the output voltage of Rail 2. READ_VOUT (8Bh, Page 1) returns the output voltage of Rail 1. In SVI VID mode, SVT reports the V_{OUT}/I_{OUT} of Rail 2 to VDD1 and V_{OUT}/I_{OUT} of Rail 1 to VDD2. It is only recommended to select 0 or 1 in SVI2 VID mode. In PMBus™ VID mode and PVID mode, always set this bit to 0.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus™ device to copy the Page 0 and Page 1 values in the operating memory to the matching locations in the EEPROM. Any items in the operating memory that do not have matching locations in the EEPROM are ignored.

This command can be used while the device is outputting power. This command is write only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus™ device to copy the Page 0 and Page 1 value of the EEPROM to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the EEPROM. Any items in the EEPROM that do not have matching locations in the operating memory are ignored.

Do not use this command while the device is outputting power or the command will be ignored. This command is write only. There is no data byte for this command.

VOUT_COMMAND (21h)

The VOUT_COMMAND on Page 0 works together with the VDIFF1/2 divider to set the Rail 1 VID-DAC output voltage in PMBus™ VID mode (i.e.: the reference voltage (V_{REF}) of Rail 1 in PMBus™ VID mode). The DAC output voltages range from 0 to 1.55V. For Rail 1, the VDIFF1/2 divider is controlled by command MFR_VR_CONFIG (D0h) bit[3]. When bit[3] = 0, V_{REF} is equal to VOUT_COMMAND. When bit[3] = 1, V_{REF} is half of VOUT_COMMAND.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_VID							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7:0	VOUT_VID	Sets the Rail 1 reference voltage (VID-DAC output voltage) in PMBus™ VID mode. 6.25mV/LSB.

VOUT_TRIM (22h)

The VOUT_TRIM command on Page 0 is used to apply an offset value to the Rail 1 remote sense amplifier output. VOUT_TRIM is generally used by end users to trim the output voltage at the time the PMBus™ device is assembled into the end user's system. This command can also be used to fine-tune the output voltage when the designed V_{REF} is out of the 6.25mV step.

Command	VOUT_TRIM															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	VREF_TRIM_2/3/4PHASE					VREF_TRIM_1PHASE_CCM					VREF_TRIM_1PHASE_DCM				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
14:10	VREF_TRIM_ 2/3/4PHASE	Adds a fixed offset over remote sense amplifier output at 2-, 3-, or 4-phase operation. (1.56/K_{VDIFF}) mV/LSB (K_{VDIFF} is the IC internal VDIFF divider ratio). For Rail 1, K_{VDIFF} is controlled by command MFR_VR_CONFIG (D0h) bit[3]. When bit[3] = 0, K_{VDIFF} = 1. When bit[3] = 1, K_{VDIFF} = 0.5. This bit is in two's complement format. Bit[3] is the sign bit. The voltage list below shows the direct value and real-world value. 4'b0000: 0mV 4'b0001: +(1.56/K_{VDIFF}) mV 4'b0111: +(10.92/ K_{VDIFF}) mV 4'b1000: -(12.48/ K_{VDIFF}) mV 4'b1001: -(10.92/ K_{VDIFF}) mV 4'b1111: -(1.56/ K_{VDIFF}) mV
9:5	VREF_TRIM_1PHASE_ CCM	Adds a fixed offset over remote sense amplifier output at 1-phase CCM operation. (1.56/K_{VDIFF}) mV/LSB (K_{VDIFF} is the IC internal VDIFF divider ratio). For Rail 1, K_{VDIFF} is controlled by command MFR_VR_CONFIG (D0h) bit[3]. When bit[3] = 0, K_{VDIFF} = 1. When bit[3] = 1, K_{VDIFF} = 0.5. This bit is in two's complement format. Bit[3] is the sign bit. The voltage list below shows the direct value and real-world value. 4'b0000: 0mV 4'b0001: +(1.56/K_{VDIFF}) mV 4'b0111: +(10.92/ K_{VDIFF}) mV 4'b1000: -(12.48/ K_{VDIFF}) mV 4'b1001: -(10.92/ K_{VDIFF}) mV 4'b1111: -(1.56/ K_{VDIFF}) mV
4:0	VREF_TRIM_1PHASE_ DCM	Adds a fixed offset over remote sense amplifier output at 1-phase DCM operation. (1.56/K_{VDIFF}) mV/LSB (K_{VDIFF} is the IC internal VDIFF divider ratio). For Rail 1, K_{VDIFF} is controlled by command MFR_VR_CONFIG (D0h) bit[3]. When bit[3] = 0, K_{VDIFF} = 1. When bit[3] = 1, K_{VDIFF} = 0.5. This bit is in two's complement format. Bit[3] is the sign bit. The voltage list below shows the direct value and real-world value. 4'b0000: 0mV 4'b0001: +(1.56/K_{VDIFF}) mV 4'b0111: +(10.92/ K_{VDIFF}) mV 4'b1000: -(12.48/ K_{VDIFF}) mV 4'b1001: -(10.92/ K_{VDIFF}) mV 4'b1111: -(1.56/ K_{VDIFF}) mV

VOUT_MAX (24h)

The VOUT_MAX command on Page 0 sets the Rail 1 maximum VID value. The Rail 1 VID is limited to VOUT_MAX if the programmed initial VID plus the offset is higher. This command is effective in SVI VID mode, PMBus™ VID mode, and PVID mode.

Command	VOUT_MAX															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	VOUT_MAX								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:0	VOUT_MAX	Sets the Rail 1 maximum VID value. This bit is used to limit the sum of the initial VID plus the offset. The offset includes an initial offset and special offset programmed by command MFR_OFFSET (DFh). 6.25mV/LSB.

VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command sets the Rail 1 margin high reference voltage at which the output is to be changed when the OPERATION command is set to margin high. This command is effective in PMBus™ VID mode only.

Command	VOUT_MARGIN_HIGH															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_MARGIN_HIGH							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7:0	VOUT_MARGIN_HIGH	Sets the Rail 1 margin high state reference voltage level. 6.25mV/LSB.

VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command sets the Rail 1 margin low reference voltage level at which the output is to be changed when the OPERATION command is set to margin low. This command is effective in PMBus™ VID mode only.

Command	VOUT_MARGIN_LOW															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_MARGIN_LOW							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7:0	VOUT_MARGIN_LOW	Sets the Rail 1 margin low state reference voltage level. 6.25mV/LSB.

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command on Page 0 sets the Rail 1 output voltage to the V_{REF} dividing ratio when an external output divider is applied.

Command	VOUT_SCALE_LOOP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	VOUT_SCALE_LOOP						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	VOUT_SCALE_LOOP	Sets the Rail 1 output voltage to the V_{REF} dividing ratio. V_{REF} ranges from 0 to 1.55V.

The VOUT_SCALE_LOOP can be calculated with Equation (11):

$$VOUT\_SCALE\_LOOP = \begin{cases} 128 \times \dfrac{V_{REF}}{K_{VDIFF} \times V_{OUT}} & V_{REF} \neq K_{VDIFF} \times V_{OUT} \\ 0 & V_{REF} = K_{VDIFF} \times V_{OUT} \end{cases} \quad (11)$$

Where V_{REF} is the reference voltage (in V), K_{VDIFF} is the internal VDIFF dividing ratio controlled by command MFR_VR_CONFIG (D0h) bit[3] (in V/V), and V_{OUT} is the target output voltage (in V).

For example, to support a 5V output voltage, set command MFR_VR_CONFIG (D0h) bit[3] = 0, select V_{REF} = 0.82V, and VOUT_SCALE_LOOP (29h) = 0x0015.

MFR_ SLOPE_SW_INI (2Ch)

The MFR_SLOPE_SW_INI command sets the Rail 1 initial slope compensation before the first pulse-width modulation (PWM) pulse during soft start. The initial slope compensation is used to eliminate the group pulse at soft start-up.

Command	MFR_ SLOPE_SW_INI							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	X		CURRENT_SOURCE_INI					

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6	SLOPE_INI_EN	Enables the soft-start initial slope compensation. The initial slope compensation is used to eliminate the group pulse at the beginning of soft start. 1'b0: disables soft start initial slope compensation 1'b1: enable soft start initial slope compensation
5:0	CURRENT_SOURCE_ INI	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

The initial slope compensation can be calculated with Equation (12):

$$V_{SLOPE\_INI} = 0.845 \times CURRENT\_SOURCE\_INI \quad (12)$$

Where V_{SLOPE_INI} is the initial slope voltage (in mV), and CURRENT_SORCE_INI is the register value in MFR_SLOPE_SW_INI.

In the design, set the slope amplitude voltage (V_{SLOPE_INI}) equal to 1.5~2 times the steady state slope voltage. For the steady state slope voltage calculation, refer to register MFR_SR_SLOPE_2PS (E2h) on page 79 for more information.

FREQUENCY_SWITCH (33h)

The FREQUENCY_SWITCH command on Page 0 is used to set the switching frequency for Rail 1. The switching frequency setting range is from 200kHz to 5.11MHz (with 10kHz per step).

Command	FREQUENCY_SWITCH															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	SWITCH_FREQUENCY								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:0	SWITCH_FREQUENCY	Sets the Rail 1 switching frequency from 200 - 5110kHz. 10kHz/LSB.

For example, to achieve a 500kHz switching frequency, set FREQUENCY_SWITCH (33h) = 0x0032.

VIN_ON (35h)

The VIN_ON command is used to set the V_{IN} UVLO rising threshold.

Command	VIN_ON															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	VIN_ON						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	VIN_ON	Sets the V_{IN} UVLO rising threshold. 0.25V/LSB.

For example, when the V_{IN} UVLO rising threshold is 8V, then set VIN_ON (35h) = 0x0020.

VIN_OFF (36h)

The VIN_OFF command is used to set the V_{IN} UVLO falling threshold.

Command	VIN_OFF															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	VIN_OFF						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	VIN_OFF	Sets the V_{IN} UVLO falling threshold. 0.25V/LSB.

For example, when the V_{IN} UVLO falling threshold is 7V, then set VIN_OFF (36h) = 0x001C.

VIN_OV_ FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command is used to set the V_{IN} OVP threshold. The MP2853 provides two different methods for achieving V_{IN} OVP: latch-off mode and auto-retry mode. In latch-off mode, the power regulation system latches down once the input voltage exceeds the VIN_OV threshold. An OPERATION command, EN toggle, or VDD33 power cycle is required to restart the power system. In auto-retry mode, the power regulation system shuts off when the sense input voltage exceeds the VIN_OV threshold and soft restarts when the sensed V_{IN} falls below the V_{IN} OVP threshold.

Command	VIN_OV_FAULT_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	VIN_OV						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	VIN_OV	Sets the V_{IN} OVP threshold. 0.25V/LSB.

For example, to get a 16V V_{IN} OVP threshold, set VIN_OV_FAULT_LIMIT (55h) = 0x0040.

TON_DELAY (60h)

The TON_DELAY command on Page 0 is used to set the Rail 1 power-on delay time.

Command	TON_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TON_DELAY															

Bits	Bit Name	Description
15:0	TON_DELAY	Sets the Rail 1 power-on delay time. The power-on delay time begins when the system initialization is completed. When the T_{ON} delay time is over, Rail 1 begins soft start. 100μs/LSB.

For example, to get a 10ms T_{ON} delay time, set TON_DELAY (60h) = 0x0064.

TON_RISE (61h)

The TON_RISE command on Page 0 is used to set the Rail 1 reference voltage slew rate at dynamic VID (DVID) transition up or down and margin high transition.

Command	TON_RISE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	VID_SR_CNT										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
10:0	VID_SR_CNT	Sets the duration time for each V_{REF} step. The time can be calculated with: $(VID\_SR\_CNT + 3) \times 50ns$ Note that the register setting with 5'LSB = 5'b11111 is ineffective. For example, do not set the register value to 0x001F, 0x003F, 0x005F, 0x007F, etc. 50ns/LSB.

Figure 23 shows the definition of sub-registers in TON_RISE.

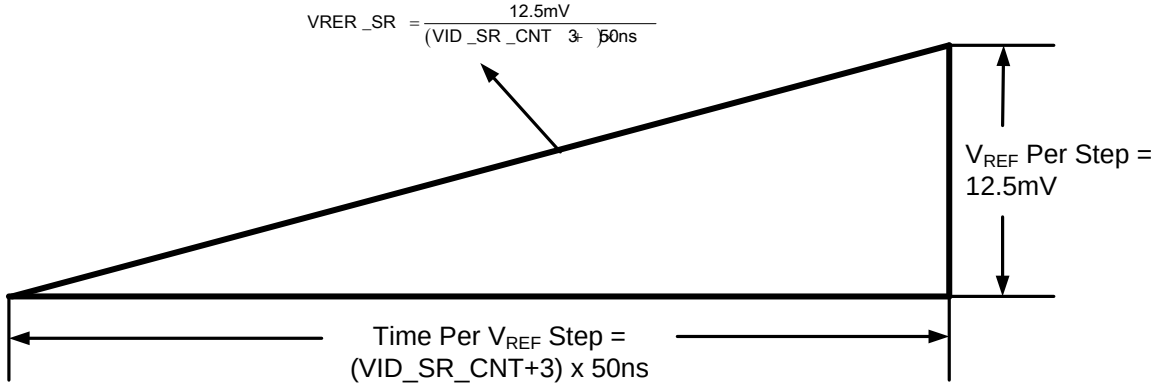


Figure 23: Dynamic VID Slew Rate Definition

The output voltage DVID slew rate can be calculated with Equation (13):

$$VOUT\_DVID\_SR = \frac{12.5mV}{(VID\_SR\_CNT + 3) \times 50ns} \times \frac{1}{K_{R1}} \quad (13)$$

Where K_{R1} is the Rail 1 output resistive divider ratio.

TOFF_DELAY (64h)

The TOFF_DELAY command on Page 0 is used to set the Rail 1 power-off delay time. The power-off delay time is effective only at the OPERATION command soft-off and EN soft-off process.

Command	TOFF_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TOFF_DELAY															

Bits	Bit Name	Description
15:0	TOFF_DELAY	Sets the Rail 1 power-off delay time at OPERATION command soft off. 100μs/LSB.

TOFF_FALL (65h)

The TOFF_FALL command is used to set the reference voltage transition down slew rate at soft-off and margin low transition. The sub-register definition is same as in Figure 23. The slew rate also can be calculated with Equation (13).

Command	TOFF_FALL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	VID_SR_CNT										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
10:0	VID_SR_CNT	Sets the duration time for each V_{REF} step. The time can be calculated with: $(VID\_SR\_CNT + 3) \times 50ns$ Note that the register setting with 5'LSB = 5'b11111 is ineffective. For example, do not set the register value to 0x001F, 0x003F, 0x005F, 0x007F, etc. 50ns/LSB.

MFR_FAULTS1 (84h)

The MFR_FAULTS1 command is used to return the VR operation faults at the present power cycle. MFR_FAULTS1 is a read-only command. Each fault bit represents a fault type. The fault bits are all in latch mode. Once set, this command can only be reset with a command off or non-low power mode EN off with a CLEAR_FAULT command, or low-power mode EN toggle, or VDD33 power recycle.

Command	MFR_FAULTS1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
12	VDIFF_SC_R2	Rail 2 VDIFF short to GND fault indication bit. 1'b0: no VDIFF short to GND fault 1'b1: VDIFF short to GND fault has occurred on Rail 2
11	OCP_TDC_R2	Rail 2 OCP_TDC fault indication bit. 1'b0: no OCP_TDC fault on Rail 2 1'b1: OCP_TDC fault has occurred on Rail 2
10	OCP_SPIKE _R2	Rail 2 OCP_SPIKE fault indication bit. 1'b0: no OCP_SPIKE fault on Rail 2 1'b1: OCP_SPIKE fault has occurred on Rail 2
9	VOUT_UV _R2	Rail 2 V_{OUT} under-voltage (UV) fault indication bit. This bit is set when the Rail 2 V_{OUT} UVP blanking time ends and the V_{OUT} UV still exists. 1'b0: no V_{OUT} UV fault on Rail 2 1'b1: V_{OUT} UV fault has occurred on Rail 2
8	VOUT_OV _R2	Rail 2 V_{OUT} over-voltage (OV) fault indication bit. This bit is set when the Rail 2 V_{OUT} OVP blanking time ends and the V_{OUT} OV still exists. 1'b0: no V_{OUT} OV fault on Rail 2 1'b1: V_{OUT} OV fault has occurred on Rail 2
7	VDIFF_SC_R1	Rail 1 VDIFF short to GND fault indication bit. 1'b0: no VDIFF short to GND fault on Rail 1 1'b1: VDIFF short to GND fault has occurred on Rail 1
6	OCP_TDC_ R1	Rail 1 OCP_TDC fault indication bit. 1'b0: no OCP_TDC fault on Rail 1 1'b1: OCP_TDC fault has occurred on Rail 1
5	OCP_SPIKE_ R1	Rail 1 OCP_SPIKE fault indication bit. 1'b0: no OCP_SPIKE fault on Rail 1 1'b1: OCP_SPIKE fault has occurred on Rail 1
5	VOUT_UV _R1	Rail 1 V_{OUT} UV fault indication bit. This bit is set when the Rail 1 V_{OUT} UVP blanking time ends and the V_{OUT} UV still exists. 1'b0: no V_{OUT} UV fault on Rail 1 1'b1: V_{OUT} UV fault has occurred on Rail 1
3	VOUT_OV _R1	Rail 1 V_{OUT} OV fault indication bit. This bit is set when the Rail 1 V_{OUT} OVP blanking time ends and the V_{OUT} OV still exists. 1'b0: no V_{OUT} OV fault on Rail 1 1'b1: V_{OUT} OV fault has occurred on Rail 1
2	OT_FLT	Over-temperature (OT) fault indication bit. 1'b0: no OT fault has occurred 1'b1: OT fault has occurred
1	VIN_OV	V_{IN} OV fault indication bit. 1'b0: no V_{IN} OV fault has occurred 1'b1: V_{IN} OV fault has occurred
0	VIN_UV	V_{IN} UV fault indication bit. 1'b0: no V_{IN} UV fault has occurred 1'b1: V_{IN} UV fault has occurred

For example, if MFR_FAULTS = 0002H, then a V_{IN} OV fault has occurred.

MFR_FAULTS2 (85h)

The MFR_FAULTS2 command is used to monitor the fault type of the Intelli-Phase. This command is effective only when the Intelli-Phase supports this function. Refer to the Intelli-Phase datasheet for more information.

The Intelli-Phase fault type indication is latched once a fault occurs and can be cleared by sending a CLEAR_FAULTS (03h) PMBus™ command.

Command	MFR_FAULTS2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	PHASE1_FAULT_TYPE				PHASE2_FAULT_TYPE				PHASE3_FAULT_TYPE			

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
11:8	FAULT_TYPE_PHASE1	Intelli-Phase fault type indication of phase 1. 4’b0000: no fault 4’b0001: VIN-SW short 4’b0010: current limit protection 4’b0100: over-temperature protection 4’b1000: SW-PGND short protection
7:4	FAULT_TYPE_PHASE2	Intelli-Phase fault type indication of phase 2. 4’b0000: no fault 4’b0001: VIN-SW short 4’b0010: current limit protection 4’b0100: over-temperature protection 4’b1000: SW-PGND short protection
3:0	FAULT_TYPE_PHASE3	Intelli-Phase fault type indication of phase 3. 4’b0000: no fault 4’b0001: VIN-SW short 4’b0010: current limit protection 4’b0100: over-temperature protection 4’b1000: SW-PGND short protection

MFR_FAULTS3 (86h)

MFR_FAULTS3 is used to monitor the fault type of the Intelli-Phase and fault status of CS. This command is effective only when the Intelli-Phase supports this function. Refer to the Intelli-Phase datasheet for more information.

The Intelli-Phase fault type indication is latched once a fault occurs and can be cleared by sending a CLEAR_FAULT (03h) PMBus™ command.

The CS fault flag is set and latched when the MP2853 detects that CS has been pulled low and can be reset by a VDD33 power recycle or regular power mode EN toggle.

Command	MFR_FAULTS3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X						PHASE4_FAULT_TYPE				PHASE5_FAULT_TYPE			

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
12	CS5_FAULT_FLAG	CS5 fault indicator. This bit shows a 1 when CS5 is pulled low. The MP2853 CS fault detection is enabled by setting MFR_VR_CONFIG3 (C4h) bit[10] = 1. 1'b0: no CS fault 1'b1: CS fault has occurred
11	CS4_FAULT_FLAG	CS4 fault indicator. This bit shows a 1 when CS4 is pulled low. The MP2853 CS fault detection is enabled by setting MFR_VR_CONFIG3 (C4h) bit[10] = 1. 1'b0: no CS fault 1'b1: CS fault has occurred
10	CS3_FAULT_FLAG	CS3 fault indicator. This bit shows a 1 when CS3 is pulled low. The MP2853 CS fault detection is enabled by setting MFR_VR_CONFIG3 (C4h) bit[10] = 1. 1'b0: no CS fault 1'b1: CS fault has occurred
9	CS2_FAULT_FLAG	CS2 fault indicator. This bit shows a 1 when CS2 is pulled low. The MP2853 CS fault detection is enabled by setting MFR_VR_CONFIG3 (C4h) bit[10] = 1. 1'b0: no CS fault 1'b1: CS fault has occurred. Intelli-Phase CS fault type indication of phase 2. 1'b0: no CS fault 1'b1: CS fault has occurred. Only effective when the Intelli-Phase has this function.
8	CS1_FAULT_FLAG	CS1 fault indicator. This bit indicates a 1 when CS1 is pulled low. The MP2853 CS fault detection is enabled by setting MFR_VR_CONFIG3 (C4h) bit[10] = 1. 1'b0: no CS fault 1'b1: CS fault has occurred. Intelli-Phase CS fault type indication of phase 1. 1'b0: no CS fault 1'b1: CS fault has occurred. Only effective when the Intelli-Phase has this function.
7:4	PHASE4_FAULT_TYPE_PHASE4	Intelli-Phase fault type indication of phase 4. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
3:0	PHASE5_FAULT_TYPE_PHASE5	Intelli-Phase fault type indication of phase 5. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection

MFR_CML (87h)

The MFR_CML command returns the PMBus™ command/data communication fault and EEPROM fault status. This command is also used to indicate the present PMBus™ command for the EEPROM or the operating memory. MFR_CML is a read-only command. The fault bits except bit[0] are latched. Once the fault bit is set and latched, CLEAR_EEPROM_FAULTS (FFh) is required to reset the fault.

Command	MFR_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function					X			

Bits	Bit Name	Description
7	CML_INVALID_CMD	Indicates an invalid PMBus™ command. 1'b0: no invalid PMBus™ command has been received 1'b1: an invalid PMBus™ command has been received
6	CML_INVALID_DATA	Indicates invalid PMBus™ data. 1'b0: no invalid PMBus™ data has been received 1'b1: invalid PMBus™ data has been received
5	PEC_ERROR	Indicates a PEC error. 1'b0: no PEC error 1'b1: a PEC error has occurred
4	EEPROM_FLT	EEPROM fault indication. 1'b0: no EEPROM fault has occurred 1'b1: an EEPROM fault has occurred
3	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
2	CMD_FLT_BLK	Indicates that the EEPROM command has been rejected. 1'b0: no EEPROM command has been rejected 1'b1: an EEPROM command has been rejected since the controller is storing the fault type in the EEPROM.
1	CML_OTHERS	Other PMBus™ communication fault indication bit. Latched. 1'b0: no other PMBus™ communication fault has occurred 1'b1: a PMBus™ communication fault not listed above has occurred
0	EEPROM_CMD_SIG	EEPROM operation indication bit. Live. 1'b0: PMBus™ command is not for the EEPROM 1'b1: PMBus™ command is addressing to the EEPROM

READ_VIN (88h)

The READ_VIN command is used to return the input voltage in a direct format.

Command	READ_VIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	X	X	READ_VIN						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	READ_VIN	Returns the input voltage in direct format. 0.25V/LSB.

For example, if READ_VIN = 0x0030, then the sensed input voltage is 12V.

READ_VOUT (8Bh)

The READ_VOUT command on Page 0 is used to return the voltage between VOSEN and VORTN (VOSEN - VORTN) in 6.25mV/LSB. The PMBus™ command MFR_VR_CONFIG4 (0Eh, Page 0) bit[0] determines the voltage at which the rail is returned by READ_VOUT (8Bh, Page 0). When bit[0] = 0, READ_VOUT (8Bh, Page 0) returns the VOSEN1 - VORTN1 voltage of Rail 1. When bit[0] = 1, READ_VOUT (8Bh, Page 0) returns the VOSEN2 - VORTN2 voltage of Rail 2.

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	READ_VOUT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:0	READ_VOUT	Returns the differential voltage between VOSEN and VORTN (VOSEN - VORTN). 6.25mV/LSB.

The reported output voltage can be calculated with Equation (14):

$$VOUT\_REPORT = \frac{6.25 \times 10^{-3} \times READ\_VOUT}{K_R} \quad (14)$$

Where VOUT_REPORT is the PMBus™ reported output voltage (in V), READ_VOUT is the register value (in decimals), and K_R is the output resistive divider ratio of the associated rail determined by MFR_VR_CONFIG4 (0Eh, Page 0) bit[0]. READ_VOUT in the MP2853 can be calculated with Equation (17).

For example, if READ_VOUT = 0x00A0, K_R is 1, and the monitored output voltage is 1V.

READ_IOUT (8Ch)

The READ_IOUT command on Page 0 returns the average load current of Rail 1.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	READ_IOUT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:0	READ_IOUT	Returns the load current of Rail 1. 0.25A/LSB.

For example, when READ_IOUT = 0x0020, then the Rail 1 load current report is 8A.

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command is used to return the power stage temperature. The MP2853 monitors the power stage temperature by sensing the voltage on VTEMP and converts it into a direct format inside the device. To convert VTEMP to a temperature, set the temperature sense gain and offset with command MFR_TEMP_CAL (D2h). Refer to the Page 0 command MFR_TEMP_CAL (D2h) for more information.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	X	READ_TEMPERATURE							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7:0	READ_TEMPERATURE	Monitors the temperature of the power stage. 1℃/LSB.

For example, when READ_TEMPERATURE = 0x0064, the junction temperature of the hottest Intelli-Phase on the VTEMP bus is 100°C.

MFR_SD_VID (A6h)

The MFR_SD_VID command on Page 0 sets the Rail 1 Hi-Z shutdown voltage level. This command is only effective when VID slews down to 0V. VID slewing down to 0 can be caused by DVID to 0V or a target VID lower than MFR_VID_OFF (D5h), OPERATION command off, or EN soft off. Once the VID-DAC output is lower than the Hi-Z shutdown voltage level, the output enters PWM Hi-Z shutdown mode (see Figure 24). The output voltage is discharged by the load current.

Command	MFR_SD_VID							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_SD_VID						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	MFR_SD_VID	Sets the PWM Hi-Z shuts down the voltage level. Once the Rail 1 VID-DAC output is lower than the Hi-Z shutdown voltage level, the output enters PWM Hi-Z shutdown mode. 6.25mV/LSB.

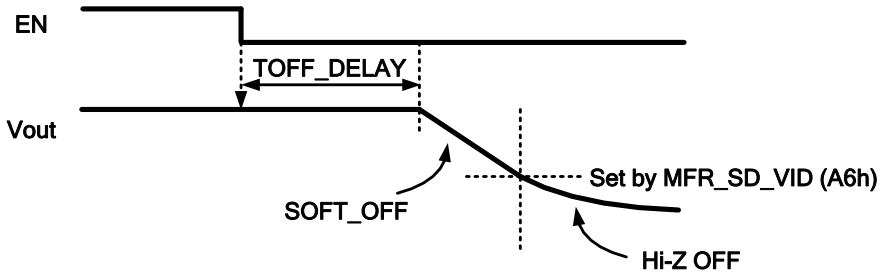


Figure 24: EN Soft-Off to Hi-Z Off Level

MFR_PSI_TRIM (A8h)

When the DC loop is disabled, the actual V_{OUT} of the MP2853 can be calculated with Equation (15):

$$V_{OUT} = \frac{V_{REF} + V_{SLOPE}}{K_R} + \frac{\Delta V_{OUT}}{2} \quad (15)$$

Where V_{REF} is the reference voltage (in V), V_{SLOPE} is the slope voltage (in V), ΔV_{OUT} is the output voltage ripple (in V), and K_R is the output voltage external divider.

The MP2853 provides a reference voltage trim (V_{TRIM}) to make the actual output voltage close the design target without DC loop calibration. V_{TRIM} is implemented by adding a negative offset over V_{REF}. In designs, design V_{TRIM} to be equal to the voltage shift caused by V_{SLOPE} and the V_{OUT} ripple. When the VR is transitioning between different power states, V_{TRIM} makes the DC loop output constant between different power states, smoothing the output voltage when the power state changes.

The MFR_PSI_TRIM command on Page 0 is used to trim the reference voltage at 2-phase and 1-phase CCM and 1-phase DCM for Rail 1.

Command	MFR_PSI_TRIM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	VTRIM_1PS_DCM				X	VTRIM_1PS_CCM				X	VTRIM_2PS_CCM				X

Bits	Bit Name	Description
15, 10, 5, 0	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
14:11	VTRIM_1PS_DCM	Sets the reference voltage trim for 1-phase DCM. 2.3mV/LSB.
9:4	VTRIM_1PS_CCM	Sets the reference voltage trim for 1-phase CCM. 2.3mV/LSB.
4:1	VTRIM_2PS_CCM	Sets the reference voltage trim for 2-phase CCM. 2.3mV/LSB.

MFR_PG_RDL (A9h)

The MFR_ PG_RDL command on Page 0 is used to set the Rail 1 power good delay time. This command is effective at PG non-SVI mode only, with MFR_VR_CONFIG3 (C4h) bit[3] = 1. In PG SVI mode with MFR_VR_CONFIG3 (C4h) bit[3] = 0, PG asserts high when V_{REF} reaches the boot-up voltage level.

Command	MFR_PG_RDL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	PG_DELAY_TIME									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:0	PG_DELAY_TIME	Sets the Rail 1 PG asserting high delay time. 5μs/LSB.

MFR_VDIFF_SCP_SET (ABh)

The MFR_VDIFF_SCP_SET command on Page 0 is used to set the VDIFF short to ground protection for both Rail 1 and Rail 2. For VDIFF SCP, when the MP2853 detects VOSEN - VDIFF > 500mV and lasts for a set delay time, the MP2853 disables the PWM outputs of the issued rail to protect the output.

Command	MFR_VDIFF_SCP_SET							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	EN			

Bits	Bit Name	Description
7:4	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
3	VDIFF_SCP_EN	Enable bit for VDIFF short to GND detection and detection. 1'b0: disables VDIFF short to GND protection 1'b1: enables VDIFF short to GND protection
2:0	SCP_BLANK_TIME	Sets the VDIFF SCP trigger delay time. There is a 200ns offset for the delay time, so the final trigger delay is (SCP_DELAY_TIME) * 400ns + 200ns. 400ns/LSB.

VOUT_VR_CAL (ACh)

The VOUT_VR_CAL command on Page 0 is used to set the gain from the ADC sensed VOSEN1 - VORTN1 voltage to the SVI2 V_{OUT} telemetry and V_{OUT} report in register READ_VOUT (8Bh). VOUT_VR_CAL also sets an offset on the output voltage SVI2 telemetry and V_{OUT} report in register READ_VOUT (8Bh). VOUT_VR_CAL is for MP2853 Rail 1 output voltage reporting only.

Command	VOUT_VR_CAL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	OFFSET						GAIN							

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
13:8	OFFSET	Adds an offset to the SVI2 V_{OUT} telemetry and V_{OUT} report in register READ_VOUT (8Bh). This bit is for the Rail 1 output voltage report only. This bit is in two's complement format. Bit[13] is the sign bit. (6.25/K_{VDIFF}) mV/LSB. The voltage list below shows the direct value and real-world value. 6'b 00 0000: 0mV 6'b 00 0001: +(6.25/K_{VDIFF}) mV 6'b 01 1111: +(193.75/K_{VDIFF}) mV 6'b 10 0000: -(200/K_{VDIFF}) mV 6'b 10 0001: -(193.75/K_{VDIFF}) mV 6'b 11 1111: -(6.25/K_{VDIFF}) mV
7:0	GAIN	Sets the gain from the ADC sensed VOSEN - VORTN voltage to the SVI2 V_{OUT} telemetry and V_{OUT} report in register READ_VOUT (8Bh). This bit is for the Rail 1 output voltage report only. In the MP2853, set GAIN = 0x40 to get the correct VOSEN - VORTN voltage report.

The output voltage reporting data to the SVI2 processor is shown in Equation (16):

$$V_{OUT\ SVI\ REPORT} = 504 - \left[\frac{1023 \times (V_{OSEN} - V_{ORTN})}{1.6} \times \frac{GAIN}{2^8} + OFFSET \right] \quad (16)$$

The output voltage reporting data to the SVI2 processor is shown in Equation (17):

$$READ\_VOUT = \frac{1023 \times (V_{OSEN} - V_{ORTN})}{1.6} \times \frac{GAIN}{2^8} + OFFSET \quad (17)$$

Where $V_{OUT\ SVI\ REPORT}$ is the output reporting data from the VR to the SVI processor, READ_VOUT is the decimal value in register READ_VOUT (8Bh), V_{OSEN} and V_{ORTN} are the voltages at VOSEN and VORTN (in V), and GAIN and OFFSET are the values in the VOUT_VR_CAL (ACh) register. The reporting format follows the V_{OUT} telemetry format in the AMD SVI2 specification.

IOUT_VR_CAL (ADh)

The IOUT_VR_CAL command on Page 0 is used to set the gain and offset for the Rail 1 I_{OUT} telemetry to the SVI2 processor. IOUT_VR_CAL is effective for SVI2 telemetry only.

Command	IOUT_VR_CAL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OFFSET							GAIN								

Bits	Bit Name	Description
15:9	OFFSET	Adds an offset to the I_{OUT} telemetry data to the processor. This bit is in two's complement format. Bit[15] is the sign bit. The resolution is determined by the maximum report current defined by 0xFF. The voltage list below shows the direct value and real-world value. 7'b 000 0000: 0 7'b 000 0001: 1 7'b 011 1111: 63 7'b 100 0000: -64 7'b 100 0001: -63 7'b 111 1111: -1
8:0	GAIN	Sets the gain for the Rail 1 I_{OUT} telemetry to the SVI2 processor.

The current report to the SVI2 processor is shown in Equation (18):

$$I_{OUT\ SVI\ REPORT} = 1.279 \times \frac{I_{OUT} \times K_{CS} \times R_{IMON}}{GAIN} + OFFSET \quad (18)$$

Where I_{OUT} is the output current (in A), K_{CS} is the current sense gain of Intelli-Phase (in μA/A), R_{IMON} is the resistor at IMON (in kΩ), and GAIN and OFFSET are the values in IOUT_VR_CAL (ADh) (in decimal).

With Equation (18), the GAIN can be calculated with Equation (19):

$$GAIN = 5.016 \times 10^{-3} \times I_{OUT\_FFh} \times K_{CS} \times R_{IMON} \quad (19)$$

Where I_{OUT_FFh} is the SVI2 max report current to FFh (in A).

MFR_PHASE_PSI_CFG (C0h)

The MFR_PHASE_PSI_CFG command is used to set the phase assignment for both rails or force Rail 1 to a given power state in debug mode.

Command	MFR _PHASE_PSI_CFG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_PAHSE_CFG				MFR_PSI_SET		

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:4	MFR_PAHSE_CFG	Sets the phase assignment for both rails. 3'b000: 3+2 mode 3'b001: 2+2 mode 3'b010: 3+1 mode 3'b011: 2+1 mode 3'b100: 1+1 mode 3'b111: 4+1 mode
3	FORCE_ACTIVE_ PHASE_NUM_EN	Enable bit to force the power state for Rail 1. When set to 1, then the forced power state on Rail 1 is enabled, and the power state is determined by bit[2:0] in register MFR_PHASE_PSI_CFG (C0h). Set this bit to 0 during normal operation. 1'b0: disables forced power state 1'b1: enables forced power state
2:0	MFR_PSI_SET	Rail 1 forced power state setting. This bit is only effective when bit[3] = 1. When the forced phase number is higher than the set in bit[6:4], run with the phase count set in bit[6:4]. 3'b000: 1-phase DCM 3'b001: 1-phase CCM 3'b010: 2-phase CCM 3'b011: 3-phase CCM 3'b100: 4-phase CCM others: 1-phase CCM

For example, when MFR_PHASE_CONFIG = 0x7A, the MP2853 is configured to 4+1 mode, which means PWM1, PMW2, PWM3, and PWM4 are assigned to Rail 1, and PWM5 is assigned to Rail 2.

MFR_OCP_SET (C2h)

The MFR_OCP_SET command on Page 0 is used to set the Rail 1 OCP_TDC and OCP_SPIKE behavior mode and blanking times.

Command	MFR_OCP_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function				MFR_OCPTDC_TRIGDELAY									MFR_OCPSPIKE_ TRIGDELAY			

Bits	Bit Name	Description
15:14	MFR_OCP_MODE	Selects the protection mode for both OCP_TDC and OCP_SPIKE. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
13	MFR_OCPTDC_EN	Enables Rail 1 OCP_TDC protection. 1'b0: disables OCP_TDC protection 1'b1: enables OCP_TDC protection
12:5	MFR_OCPTDC_ TRIGDELAY	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for the OCP_TDC blanking time. 20µs/LSB.
4	MFR_OCPSPIKE_EN	Enables OCP_SPIKE protection. 1'b0: disables OCP_SPIKE protection 1'b1: enables OCP_SPIKE protection
3:0	MFR_OCPSPIKE_ TRIGDELAY	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for the OC_-SPIKE blanking time. 200ns/LSB.

Figure 25 shows the OCP_TDC action when OC occurs and the definition of OCP_TDC trigger delay and action delay time. OCP_SPIKE takes action similarly.

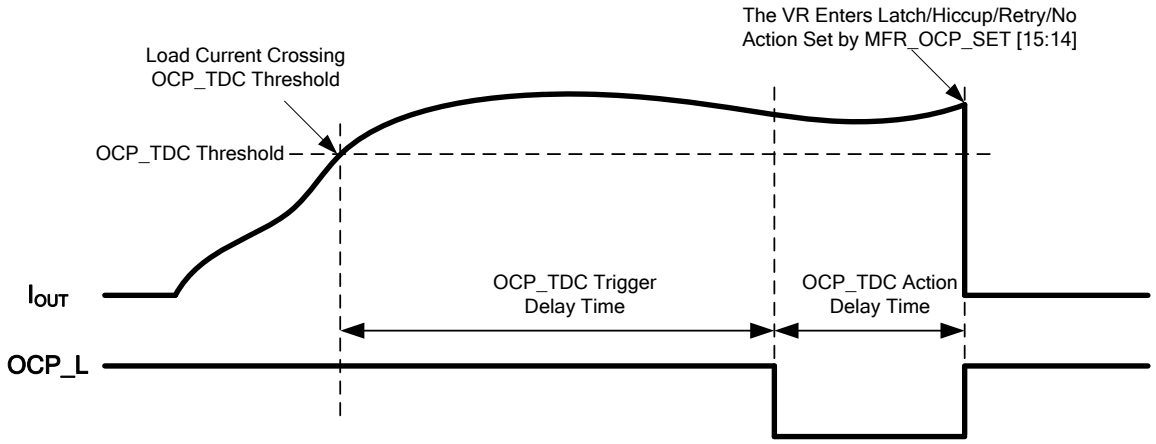


Figure 25: OCP_TDC Action

MFR_DELAY_SET (C3h)

The MFR_DELAY_SET is used to set the VID slew-up droop component resetting delay time and the VOTF delay time after VID slew-up ends.

Command	MFR_DELAY_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	MFR_DROOPFALL_DEALY					MFR_VOTF_DELAY							

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
12:8	MFR_DROOPFALL_ DELAY	Sets the delay time between V_{REF} reaching the target VID + DROOP_VID and V_{REF} falling back to the target VID. Set this bit to 1μs in general applications. 200ns/LSB.
7:0	MFR_VOTF_DELAY	Sets the delay time from V_{REF} reaching the target VID to the VR issuing a VOTF completion packet to the processor. 100ns/LSB.

MFR_VR_CONFIG3 (C4h)

The MFR_VR_CONFIG3 command is used to configure the basic functions of the MP2853.

Command	MFR_VR_CONFIG3															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15	SVI_PVID_SEL_R2	Selects PVID or SVI2 mode for Rail 2. This bit is effective only when MFR_VR_CONFIG (D0h) bit[14] = 0. 1'b0: SVI mode. VID follows the SVI2 VID table on page 35. 1'b1: PVID mode. VID is determined by PVID3, PVID2, and PVID1.
14	SVI_PVID_SEL_R1	Selects PVID or SVI2 mode for Rail 1. This bit is effective only when MFR_VR_CONFIG (D0h) bit[15] = 0. 1'b0: SVI mode. VID follows SVI2 mode. 1'b1: PVID mode. VID is determined by PVID3, PVID2, and PVID1.
13	EEPROM_RESTORE_ EN	Permits the EEPROM to copy when the system is outputting power. Only enable this function in EEPROM debug mode. Set this bit to 0 during normal operation. 1'b0: disables EEPROM copy when the system is outputting power 1'b1: enables EEPROM copy when the system is outputting power
12	DAC_CMP_R2_EN	Enable bit for smooth transition when a DVID down is pre-empted by a DVID up. For Rail 2 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: disables the Rail 2 V_{REF} filter function in continuous DVID down and up 1'b1: enables the Rail 2 V_{REF} filter function in continuous DVID down and up
11	DAC_CMP_R1_EN	Enable bit for smooth transition when a DVID down is pre-empted by a DVID up. For Rail 1 only. Enable this bit to avoid a V_{OUT} dip. 1'b0: disables the Rail 1 V_{REF} filter function in continuous DVID down and up 1'b1: enables the Rail 1 V_{REF} filter function in continuous DVID down and up
10	CSPIN_FAULT_ DETECT_EN	Enable bit to use CS as the Intelli-Phase fault indication signal. For some Intelli-Phase devices, CS can report an Intelli-Phase fault type. When this function is enabled, the MP2853 detects the fault by monitoring the voltage level at CS. Enable this bit only when the Intelli-Phase supports the CS fault detection function. 1'b0: disables CS as the Intelli-Phase fault indication signal 1'b1: enables CS as the Intelli-Phase fault indication signal

Bits	Bit Name	Description
9	VTEMPPIN_FAULT_ DETECT_EN	Enable bit to use VTEMP as the Intelli-Phase fault indication signal. When this function is enabled, the MP2853 detects the fault by monitoring the voltage at VTEMP. Enable this bit only when the Intelli-Phase supports fault reporting from its VTEMP. 1'b0: disables VTEMP as the Intelli-Phase fault indication signal 1'b1: enables VTEMP as the Intelli-Phase fault indication signal
8	OVP_DVID_DIS OCP_SPIKE_DVID_DIS OCP_TDC_DVID_DIS	Used to disable V_{OUT} OVP, OCP_SPIKE, and OCP_TDC during the DVID process. 1'b0: enables OVP, OVP_SPIKE, and OCP_TDC during DVID 1'b1: disables OVP, OCP_SPIKE, and OCP_TDC during DVID
7:6	ULTRASONIC_FS-MIN_SEL	Sets the minimum switching frequency at ultrasonic mode (USM). 2'b00: 25kHz 2'b01: 33kHz 2'b10: 48kHz 2'b11: 89kHz
5	EEPROM_MODE_SEL	The MP2853 provides a debug mode for the EEPROM. This bit is for engineering test mode use only and is not for customer use. Setting this bit to 0 may destroy the EEPROM. Set EEPROM to normal mode for normal operation. 1'b0: EEPROM debug mode 1'b1: EEPROM normal mode
4	IDROOP_TRIM_FROM_ EEPROM_EN	The MP2853 supports an 8-level load line. For each load-line level, the gain ATE value is stored in the EEPROM and can be read from the EEPROM to get a precise load-line control for each level. 1'b0: disables reading the load-line gain trim value from the EEPROM 1'b1: enables reading the load-line gain trim value from the EEPROM
3	PG_MODE_SEL	The MP2853 provides two types of PG indicating modes: SVI mode and non-SVI mode. In PG SVI mode, PG indicates high immediately when the reference voltage reaches the boot-up voltage level. The PG delay time in command MFR_PG_RDL (A9h) is ineffective. In PG non-SVI mode, PG asserts when V_{REF} rises above 90% of the boot-up voltage level and a PG delay time later. The PG delay time can be programmed with command MFR_PG_RDL (A9h). 1'b0: SVI mode 1'b1: non-SVI mode
2	RESERVED	Reserved. Fixed to 1.
1	MFR_TFN=0_FUNC_ SEL	SVT telemetry functionality selection bit when TFN = 0 in the SVD packet. TFN is a bit in the SVD packet, which is used to instruct the telemetry functionality of the VR. Default is 0 in SVI2 mode. Refer to the AMD SVI2 spec for more information. 1'b0: keeps the telemetry functionality as the former TFN = 1 SVD packet 1'b1: disables the SVT telemetry when TFN = 0
0	MFR_CRC_ERROR_EN	Enables the EEPROM CRC to stop the VR output. Enables the CRC check. 1'b0: disables the EEPROM CRC 1'b1: enables the EEPROM CRC

IOUT_CAL_CFG (C5h)

The IOUT_CAL_CFG command on Page 0 is used to set the gain and offset for the Rail 1 output current reporting to the register READ_IOUT (8Ch, Page 0).

Command	IOUT_CAL_CFG															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OFFSET						GAIN									

Bits	Bit Name	Description
15:10	OFFSET	Sets the negative offset of the Rail 1 output current reporting in register READ_IOUT (8Ch, Page 0). $READ\_IOUT = 4 \times (IOUT - OFFSET \times 0.5)$ Where READ_IOUT is the decimal value in register READ_IOUT (8Ch, Page 0). OFFSET is set to 0 by default. 0.5A/LSB.
9:0	GAIN	Sets the gain from the IMON1 voltage to the Rail 1 output current reporting in register READ_IOUT (8Ch, Page 0). The MP2853 senses the Rail 1 output current by sampling the voltage on IMON1 with a high-accuracy ADC. GAIN is used to convert the IMON1 voltage to a direct I_{OUT} format and return it with command READ_IOUT (8Ch, Page 0).

The GAIN calculating formula is shown in Equation (20):

$$GAIN = 0.51 \times K_{CS} \times R_{IMON} \quad (20)$$

Where K_{CS} is the Intelli-Phase current sense gain (in μA/A), and R_{IMON} is the resistor from IMON to GND (in kΩ).

MFR_RES_DROOP_0P2 (C6h)

The MFR_RES_DROOP_0P2 command on Page 0 is used to set 20% of the initial load-line resistor. For Rail 1 only.

Command	MFR_RES_DROOP_0P2							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_RES_DROOP_0P2			

Bits	Bit Name	Description
7:4	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
3:0	MFR_RES_DROOP_0P2	Sets 20% of initial load-line resistor for Rail 1. 0.1mΩ/LSB.

For example, if the initial load line of Rail 1 is 2mΩ, set MFR_RES_DROOP_0P2 (C6h) = 0x04h.

MFR_AUTO_PS (C7h)

The MFR_AUTO_PS command on Page 0 is used to set the Rail 1 auto-phase shedding (APS) threshold and hysteresis. Refer to the Auto-Phase Shedding section on page 23 for more information.

Command	MFR_AUTO_PS															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	MFR_PH_HYS				MFR_1PHASE_LOW						MFR_DCM_LOW			

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
13:10	MFR_PH_HYS	Sets the current hysteresis value for APS. 0.5A/LSB.
9:4	MFR_1PHASE_LOW	Sets the phase shedding load level from 2-phase CCM to 1-phase CCM. 0.5A/LSB.
3:0	MFR_DCM_LOW	Sets the phase shedding load level from 1-phase CCM to 1-phase DCM. 0.5A/LSB

MFR_23PHASE_LOW (C8h)

The MFR_23PHASE_LOW command on Page 0 is used to set the phase shedding load level for 4-, 3-, and 2-phase operation when APS is enabled.

Command	MFR_23PHASE_LOW															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_3PHASE_LOW								MFR_2PHASE_LOW							

Bits	Bit Name	Description
15:8	MFR_3PHASE_LOW	Sets phase shedding load level from 4-phase CCM to 3-phase CCM. 0.5A/LSB
7:0	MFR_2PHASE_LOW	Sets phase shedding load level from 3-phase CCM to 2-phase CCM. 0.5A/LSB.

MFR_DECAY_SET (C9h)

The MFR_DECAY_SET command on Page 0 is used to set the activation criteria of decay mode in SVI2 mode. Refer to the AMD Serial VID Interface 2.0 (SVI2) Specification Rev 1.07 section on page 22 for more information.

Command	MFR_DECAY_SET							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X				

Bits	Bit Name	Description
7:4	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
3:2	MFR_DECAY_MODE	Sets the activation criteria of decay mode for both rails. 2'b00: VID decay mode does not activate under any condition 2'b01: VID decay mode activates whenever PSI0_L is asserted (PSI0_L = 0). 2'b10: VID decay mode activates whenever both PSI0_L and PSI1_L are asserted (PSI0_L = 0, PSI1_L = 0).
1:0	MFR_DECAY_LENGTH	Sets the Rail 1 reference voltage minimum holding time for each VID step in decay mode. 100ns/LSB.

MFR_CUR_OFFSET (CAh)

The MP2853 provides OCP_PHASE protection to limit the per-phase valley current. OCP_PHASE is implanted by monitoring and comparing the cycle-by-cycle sensed CS current with a current reference. The MP2853 provides the command MFR_OCP_PHASE_LIMIT (DAh) to program the OCP_PHASE limit in a direct current format. This command also provides two registers, MFR_CUR_OFFSET (CAh) and MFR_CUR_GAIN (D3h), to calculate the OCP_PHASE limit in a direct current format to the internal OCP_PHASE comparator reference signal. The command MFR_CUR_OFFSET is used to set the offset for the OCP_PHASE calculation.

Command	MFR_CUR_OFFSET							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_CUR_OFFSET						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	MFR_CUR_OFFSET	Sets the calculation offset for Rail 1 OCP_PHASE limit setting. Calculate the MFR_CUR_OFFSET with: $\text{MFR\_CUR\_OFFSET} = \frac{10086}{\text{MFR\_CUR\_GAIN}}$ Where MFR_CUR_GAIN is the value in register MFR_CUR_GAIN (D3h).

MFR_BOOT_SR (CBh)

The MFR_BOOT_SR command on Page 0 is used to set the Rail 1 boot-up voltage slew rate when Rail 1 is turned on.

Command	MFR_BOOT_SR															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	VID_SR_CNT										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
10:0	VID_SR_CNT	Sets the duration time for each V_{REF} step. The time can be calculated with: $(\text{VID\_SR\_CNT} + 3) \times 50\text{ns}$ Note that the register setting with 5'LSB = 5'b11111 is ineffective. For example, do not set the register value to 0x001F, 0x003F, 0x005F, 0x007F, etc. 50ns/LSB.

The definition of VID_SR_VID is shown in Figure 23. The boot-up voltage slew rate can be calculated with Equation (13).

MFR_OCPSPIKE_12PS_LEVEL (CCh)

The MFR_OCPSPIKE_12PS_LEVEL command on Page 0 is used to set the Rail 1 OCP_SPIKE current level at 1- and 2-phase operation.

Command	MFR_OCPSPIKE_12PS_LEVEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_OCPSPIKE_2PS_LEVEL						MFR_OCPSPIKE_1PS_LEVEL					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
11:6	MFR_OCPSPIKE_2PS_LEVEL	Sets the Rail 1 OCP_SPIKE current level at 2-phase operation. (40/K_{CS}) A/LSB Where K_{CS} is the Intelli-Phase current sense gain (in µA/A).
5:0	MFR_OCPSPIKE_1PS_LEVEL	Sets the Rail 1 OCP_SPIKE current level at 1-phase operation. (40/K_{CS}) A/LSB Where K_{CS} is the Intelli-Phase current sense gain (in µA/A).

MFR_OCPSPIKE_34PS_LEVEL (CDh)

The MFR_OCPSPIKE_34PS_LEVEL command on Page 0 is used to set the Rail 1 OCP_SPIKE current level at 3- and 4-phase operation.

Command	MFR_OCPSPIKE_34PS_LEVEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_OCPSPIKE_4PS_LEVEL						MFR_OCPSPIKE_3PS_LEVEL					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
11:6	MFR_OCPSPIKE_4PS_LEVEL	Sets the Rail 1 OCP_SPIKE current level at 4-phase operation. (40/K_{CS}) A/LSB Where K_{CS} is the Intelli-Phase current sense gain (in µA/A).
5:0	MFR_OCPSPIKE_3PS_LEVEL	Sets the Rail 1 OCP_SPIKE current level at 3-phase operation. (40/K_{CS}) A/LSB Where K_{CS} is the Intelli-Phase current sense gain (in µA/A).

MFR_OCPTDC_12PS_LEVEL (CEh)

The MFR_OCPTDC_12PS_LEVEL command on Page 0 is used to set the Rail 1 OCP_TDC current level at 1- and 2-phase operation.

Command	MFR_OCPTDC_12PS_LEVEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_OCPTDC_2PS_LEVEL						MFR_OCPTDC_1PS_LEVEL					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
11:6	MFR_OCPTDC_2PS_ LEVEL	Sets the Rail 1 OCP_TDC current level at 2-phase operation. (40/K_{CS}) A/LSB Where K_{CS} is the Intelli-Phase current sense gain (in µA/A).
5:0	MFR_OCPTDC_1PS_ LEVEL	Sets the Rail 1 OCP_TDC current level at 1-phase operation. (40/K_{CS}) A/LSB Where K_{CS} is the Intelli-Phase current sense gain (in µA/A).

MFR_OCPTDC_34PS_LEVEL (CFh)

The MFR_OCPTDC_34PS_LEVEL command on Page 0 is used to set the Rail 1 OCP_TDC current level at 3- and 4-phase operation.

Command	MFR_OCPTDC_34PS_LEVEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_OCPTDC_4PS_LEVEL						MFR_OCPTDC_3PS_LEVEL					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
11:6	MFR_OCPTDC_4PS_ LEVEL	Sets the Rail 1 OCP_TDC current level at 4-phase operation. (40/KCS) A/LSB Where KCS is the Intelli-Phase current sense gain (in µA/A).
5:0	MFR_OCPTDC_3PS_ LEVEL	Set the Rail 1 OCP_TDC current level at 3-phase operation. (40/KCS) A/LSB Where KCS is the Intelli-Phase current sense gain (in µA/A).

MFR_VR_CONFIG (D0h)

The MFR_VR_CONFIG command is used to configure the basic functions of the MP2853.

Command	MFR_VR_CONFIG															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15	PMBUS_SEL _R1	Sets V_{OUT} VID mode to PMBus™ mode or non-PMBus™ mode. For Rail 1 only. 1'b0: non-PMBus™ mode (SVID or PVID mode) 1'b1: PMBus™ mode
14	PMBUS_SEL _R2	Sets V_{OUT} VID mode to PMBus™ mode or non-PMBus™ mode. For Rail 2 only. 1'b0: non-PMBus™ mode (SVID or PVID mode) 1'b1: PMBus™ mode
13	FORCE_PG_HIGH_EN	Enable bit to force PG high at SVI debug mode. When set to 1, after detecting if any rails are in debug mode, the associated PG signal for the rail is forced high. This bit is only effective in PG SVI mode.(If PWM1 is pulled up to 3.3V, Rail 1 is in debug mode. If PWM5 is pulled up to 3.3V, Rail 2 is in debug mode. 1'b0: disables forced PG high at debug mode 1'b1: enables forced PG high at debug mode
12	SVI_DEBG_MODE_EN	Enable bit for SVI debug mode. Set this bit to 1. If PWM1 is pulled up to 3.3V, Rail 1 is in debug mode, and the output is disabled. If PWM5 is pulled up to 3.3V, Rail 2 is in debug mode, and the output is disabled. The PG signal of the disabled rail can be forced high if MFR_VR_CONFIG (D0h) bit[13] = 1. 1'b0: disables debug mode 1'b1: enables debug mode
11	MPHASE_IBALANCE _EN	Auto-current balancing loop enable bit. This bit is effective in multi-phase operation. 1'b0: disables current balance between multiple phases 1'b1: enables current balance between multiple phases
10	DCLOOP_DCM_R2_EN	Enables DC loop calibration at 1-phase DCM to achieve the best V_{OUT} regulation. For Rail 2 only. 1'b0: disables DC loop at DCM for Rail 2 1'b1: enables DC loop at DCM for Rail 2
9	DCLOOP_DCM_R1_EN	Enables DC loop calibration at 1-phase DCM to achieve the best V_{OUT} regulation. For Rail 2 only. 1'b0: disables DC loop at DCM for Rail 2 1'b1: enables DC loop at DCM for Rail 2
8	DCLOOP_R2_EN	Enables DC loop calibration for Rail 2. This bit is effective for both DCM and CCM. To enable the DC loop at DCM, set both bit[10] and bit[8] to 1'b1. 1'b0: disables DC loop for Rail 2 1'b1: enables DC loop for Rail 2
7	DCLOOP_R1_EN	Enables DC loop calibration for Rail 1. This bit is effective for both DCM and CCM. To enable the DC loop at DCM, set both bit[9] and bit[7] to 1'b1. 1'b0: disables DC loop for Rail 1 1'b1: enables DC loop for Rail 1
6	VIN_CAL_TON_EN	Updates the PWM on time with real-time input voltage enable bit. Once this function is enabled, T_{ON} changes with V_{IN} to keep the switching frequency constant with different V_{IN} values. 1'b0: T_{ON} updates with real-time V_{IN} 1'b1: T_{ON} updates with real-time V_{IN}

Bits	Bit Name	Description
5	VDIFF_1/2DIVIDER_R2_EN	VDIFF1/2 divider enabled bit. For Rail 2 only. When the VDIFF1/2 divider is enabled, the output of the remote sense amplifier is connected to VDIFF through a 1/2 divider. Figure 26 shows the connection from the output remote sense to VFB. Enable the VDIFF1/2 divider when the output voltage is higher than 1.55V, the maximum VID-DAC output range. This bit can be used to support over-clocking when V_{OUT} ≥ 1.55V. With the VDIFF1/2 divider enabled, the maximum output voltage that the MP2853 can support is 3V without external VOSEN scale loop. 1'b0: disables VDIFF1/2 divider for Rail 2 1'b1: enables VDIFF1/2 divider for Rail 2
4	TON_REDUCTION_DCM_R2_EN	Enables T_{ON} 1/4 reduction under DCM for Rail 2. When T_{ON} reduction is enabled, the on time is reduced by 1/4 at 1-phase DCM to reduce the output voltage ripple. 1'b0: disables T_{ON} reduction under DCM for Rail 2 1'b1: enables T_{ON} reduction under DCM for Rail 2
3	VDIFF_1/2DIVIDER_R1_EN	VDIFF1/2 divider enabled bit. For Rail 2 only. When the VDIFF 1/2 divider is enabled, the output of the remote sense amplifier is connected to VDIFF through a 1/2 divider. Enable the VDIFF1/2 sensing divider when the output voltage is higher than 1.55V, the maximum VID-DAC output range. This bit can be used to support over-clocking when V_{OUT} ≥ 1.55V. With the VDIFF1/2 divider enabled, the maximum output voltage that the MP2853 can support is 3.1V. 1'b0: disables VDIFF1/2 divider for Rail 1 1'b1: enables VDIFF1/2 divider for Rail 1
2	TON_REDUCTION_DCM_R1_EN	Enables T_{ON} 1/4 reduction under DCM for Rail 1. When T_{ON} reduction is enabled, the on time is reduced by 1/4 at 1-phase DCM to reduce the output voltage ripple. 1'b0: disables T_{ON} reduction under DCM for Rail 1 1'b1: enables T_{ON} reduction under DCM for Rail 1
1	FS_LOOP_EN	Switching frequency loop enable bit. The frequency loop is used to keep the switching frequency flat and equals the setting value at different input voltage and load current values. This bit is active for both rails. 1'b0: disables the frequency loop 1'b1: enables the frequency loop
0	ULTRASONIC_EN	USM enable bit at DCM. This bit is active for both rails. USM is used to limit the switching frequency above 25kHz at DCM when set to 1. 1'b0: disables ultrasonic mode 1'b1: enables ultrasonic mode

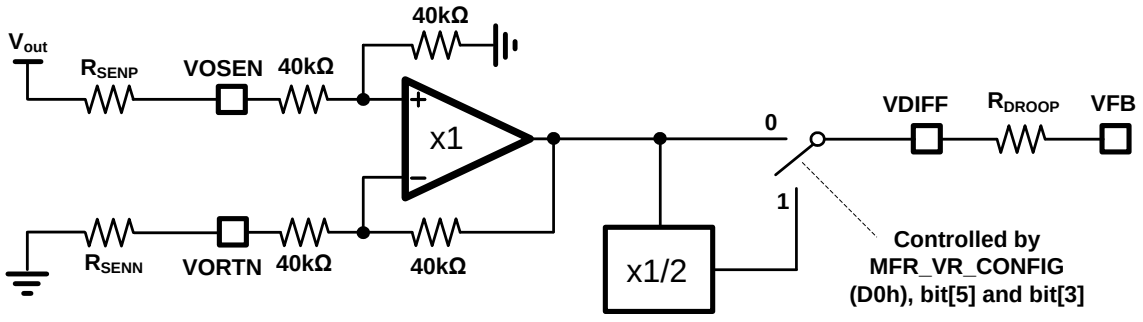


Figure 26: The MP2853 Connection from Remote Sense to VFB

MFR_CS_OFFSET (D1h)

The MFR_CS_OFFSET command is used to set the CS sense offset to achieve thermal balance in multi-phase operation.

Command	MFR_CS_OFFSET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_CS_OFFSET3					MFR_CS_OFFSET2				

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:5	MFR_CS_OFFSET3	Sets the offset voltage on CS3 in the current balance loop. This bit is in two's complement format. Bit[9] is the sign bit. The voltage list below shows the direct value and real-world value. 5'b 0 0000: 0 5'b 0 0001: +6.256mV 5'b 0 1111: +93.84mV 5'b 1 0000: -100.096mV 5'b 1 0001: -93.84mV 5'b 1 1111: -6.256mV
4:0	MFR_CS_OFFSET2	Sets the offset voltage on CS2 in the current balance loop. This bit is in two's complement format. Bit[4] is the sign bit. The voltage list below shows the direct value and real-world value. 5'b 0 0000: 0 5'b 0 0001: +6.256mV 5'b 0 1111: +93.84mV 5'b 1 0000: -100.096mV 5'b 1 0001: -93.84mV 5'b 1 1111: -6.256mV

MFR_TEMP_CAL (D2h)

The MFR_TEMP_CAL command is used to convert the VTEMP voltage into Intelli-Phase junction temperature in a direct format. The temperature is returned to register READ_TEMPERATURE (8Dh).

Command	MFR_TEMP_CAL															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	TEMP_OFFSET					TEMP_GAIN							

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
12:8	TEMP_OFFSET	Sets the offset for the temperature calculation (1°C/LSB).
7:0	TEMP_GAIN	Sets the gain for the temperature calculation (1°C/LSB).

TEMP_GAIN and TEMP_OFFSET are used to program the junction temperature gain and offset of VTEMP into the MP2853. Generally, the Intelli-Phase junction temperature can be calculated with Equation (21):

$$T_{JUNCTION}(°C) = a \times V_{TEMP\_SENSE} + b \quad (21)$$

Where VTEMP is the voltage on the MP2853 VTEMP (in V), a is the temperature sense gain (in °C/V), and b is the temperature sense offset (in °C).

TEMP_GAIN and TEMP_OFFSET are determined by MFR_TEMP_OFFSET = b and MFR_TEMP_GAIN = 1.6 * a. For example, if a = 100 and b = 10, set MFR_TEMP_CAL (D2h) = 0x0AA0.

Refer to the Intelli-Phase datasheet for more information on a and b.

MFR_CUR_GAIN (D3h)

The MFR_CUR_GAIN command on Page 0 is used to set the gain for the Rail 1 OCP_PHASE limit calculation. Refer to the MFR_CUR_OFFSET (CAh) section on page 65 for more information.

Command	MFR_CUR_GAIN															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_CUR_GAIN									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:0	MFR_CUR_GAIN	Sets the Rail 1 OCP_PHASE limit calculating gain. The gain can be calculated with: $CS\_GAIN = 8.2 \times K_{CS} \times R_{CS}$ Where K_{CS} is the multi-phase current sense gain (in μA/A), and R_{CS} is the value of the CS resistor (in kΩ).

MFR_VIN_SCALE_LOOP (D4h)

The MFR_VIN_SCALE_LOOP command is used to program the input voltage sense divider ratio into the MP2853. The MP2853 senses the voltage on VINSEN and converts it into an input voltage. The sensed V_{IN} is used to calculate T_{ON} and V_{IN} OVP.

Command	MFR_VIN_SCALE_LOOP							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VIN_SCALE_LOOP							

Bits	Bit Name	Description
7:0	VIN_SCALE_LOOP	Sets the input voltage sense divider ratio with: $MFR\_VIN\_SCALE\_LOOP = 2^{10} \times \frac{R_{IN2}}{R_{IN1} + R_{IN2}}$

For example, select R_{IN1} = 54.9kΩ and R_{IN2} = 4.99kΩ, and then set MFR_VIN_SCALE_LOOP (D4h) = 0x55.

MFR_OCP_ACTIONDELAY (D6h)

The MFR_OCP_ACTIONDELAY command on Page 0 is used to set the action delay time of OCP_TDC and OCP_SPIKE. For Rail 1 only.

Command	MFR_OCP_ACTIONDELAY															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	OCPTDC_ACTION_DELAY					OCPSPIKE_ACTION_ DELAY			

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:4	OCPTDC_ACTION_ DELAY	Sets the action delay time for OCP_TDC protection. Refer to the OCP_TDC section on page 25 for more information. 1µs/LSB.
3:0	OCPSPIKE_ACTION_ DELAY	Sets the action delay time for OCP_SPIKE protection. Refer to the OCP_SPIKE section on page 25 for more information. 1µs/LSB.

MFR_OVP_SET (D7h)

The MFR_OVP_SET command on Page 0 is used to set the Rail 1 output OVP mode and blanking time.

Command	MFR_OVP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X				OVP_BLANKING_TIME					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8	VFB+_WINDOW_EN	Enable bit for VFB+ window detection. When V_{FB} > V_{REF} + 20mV, the MP2853 holds the DC loop calibration, current balance loop, and frequency loop for a given time. If the VR is in APS mode, it exits APS and runs with full-phase CCM. 1'b0: VFB+ window is disabled 1'b1: VFB+ window is enabled
7:6	OVP_MODE	Sets the V_{OUT} OVP1 mode. There are four modes available. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
5:0	OVP_BLANKING_TIME	Sets the V_{OUT} OVP blanking time. An OVP fault occurs if the sensed VDIFF exceeds the OVP threshold for the OVP blanking time. 100ns/LSB.

MFR_UVP_SET (D8h)

The MFR_UVP_SET command on Page 0 is used to set the Rail 1 V_{OUT} UVP mode and blanking time.

Command	MFR_UVP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X				UVP_BLANKING_TIME					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8	VFB-_WINDOW_EN	VFB- window enable bit. The VFB- window is a VFB - 25mV threshold and can be used to expedite the load transient response in APM mode. 1'b0: VFB- window is disabled 1'b1: VFB- window is enabled
7:6	UVP_MODE	Sets the V_{OUT} UVP protection action mode. There are four modes available. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
5:0	UVP_BLANKING_TIME	Sets the V_{OUT} UVP blanking time. A UVP fault occurs if the sensed VDIFF falls below the UVP threshold for the UVP blanking time. 20µs/LSB.

MFR_OTP_SET (D9h)

The MFR_OTP_SET command sets the OTP threshold and retry hysteresis.

Command	MFR_OTP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function		OTP_HYS							OTP_LIMIT							

Bits	Bit Name	Description
15	OTP_MODE	Mode selection bit for the MP2853. The MP2853 can be programmed to latch off until a power cycle, EN toggle, or command on. The device can also be programmed to shut down and attempt to restart when the monitored temperature drops below the OTP_LIMIT-OTP threshold value. 1'b0: latch-off mode 1'b1: auto-retry mode
14:8	OTP_HYS	Sets the OTP retry hysteresis. When the OTP action mode in command MFR_PRT_CONFIG (DCh) is programmed to retry mode, the MP2853 tries to restart when the sensed temperature on VTEMP falls below OTP_LIMIT-OTP_HYS. 1°C/LSB.
7:0	OTP_LIMIT	Sets the over-temperature threshold. When the sensed temperature on VTEMP exceeds OTP_LIMIT, the MP2853 shuts off both rails immediately. 1°C/LSB.

For example, when MFR_OTP_SET = 0x9E82, the MP2853 trips OTP and shuts off when the sensed T_J of the power stage is higher than 130°C. The MP2853 resumes operation when the sensed T_J falls below 100°C.

MFR_OCP_PHASE_LIMIT (DAh)

The MFR_OCP_PHASE_LIMIT command on Page 0 is used to set the valley current limit thresholds for each phase assigned to Rail 1. OCP_PHASE is a single-phase valley current limitation threshold. The MP2853 monitors the phase current cycle-by-cycle. When the phase current exceeds the OCP_PHASE threshold at the PWM off time, PWM remains low to discharge the inductor current below the set threshold. OCP_PHASE works with V_{OUT} UVP to protect the power stage from over-current. If the output current rises above the OCP_PHASE limit, the output voltage will drop because the PWM off time is extended.

Command	MFR_OCP_PHASE_LIMIT															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X		OCP_PHASE_LIMIT						

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7	OCP_PHASE_SS_EN	Enable bit for the OCP_PHASE limitation during the soft-start stage. 1'b0: enable the OCP_PHASE limitation at the soft-start stage 1'b1: disables the OCP_PHASE limitation at the soft-start stage
6:0	OCP_PHASE_LIMIT	Sets the OCP_PHASE valley current-limit threshold. 1A/LSB.

MFR_ADP_CTRL (DBh)

The MFR_ADP_CTRL command is used to set the APS-related behaviors.

Command	MFR_ADP_CTRL															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15:12	OCP_PHASE_CNT_ EXITAPS	Sets the period count delay from the OCP_PHASE trigger to the APS exit. 100ns/LSB with 50ns offset.
11	MPHASE_OCP_ EXITAPS_EN	Enables OCP_PHASE protection exiting APS at any power sate. 1'b0: disables OCP_PHASE signal triggering any phase to full-phase operation 1'b1: enables OCP_PHASE signal triggering any phase to full-phase operation
10	FS INCREASE_ EXITAPS_R1_EN	Enable the Rail 1 frequency increasing condition to the APS exit. 1'b0: disables Rail 1 FS increases to APS exit 1'b1: enables Rail 1 FS increases to APS exit
9	1PHASE_OCP_ EXITAPS_EN	Enables OCP_PHASE protection exiting APS at 1-phase DCM/CCM only. 1'b0: disables the OCP per-phase signal triggering 1-phase DCM/CCM to full-phase operation 1'b1: enables the OCP per-phase signal triggering 1-phase DCM/CCM to full-phase operation
8	VFB<VID-25mV_ EXITAPS_R1_EN	Enables Rail 1 V_{FB} < VID - 25mV to enter full-phase operation. 1'b0: disables Rail 1 V_{FB} < VID - 25mV to enter full-phase operation 1'b1: enables Rail 1 V_{FB} < VID - 25mV to enter full-phase operation
7:2	APS_DELAY_TIME_ CNT	Sets the phase shedding delay time. When the reported load current is consecutively below the APS threshold for APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE, the controller enters APS mode and sheds the phase count automatically according to the load current.
1	ENTER_APS_MODE_ SELECT	Sets the phase shedding action mode for Rail 1. 1'b0: sheds to the target phase number phase-by-phase with a programmable delay time 1'b1: sheds to the target phase number once with a 16μs delay
0	MFR_APS_EN	Enables Rail 1 auto-phase shedding mode. 1'b0: disables Rail 1 APS mode 1'b1: enables Rail 1 APS mode

MFR_PRT_CONFIG (DCh)

MFR_PRT_CONFIG is used to set the protection configuration.

Command	MFR_PRT_CONFIG															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8	FAULT_RECORD_ EEPROM_EN	The MP2853 records the fault status into the EEPROM automatically and helps with fault checking at the engineering debug stage. To enable the Rail 1 fault record into the EEPROM function, set bit[8] and bit[4] to 1'b1. To enable Rail 2 fault record into the EEPROM function, set bit[8] and bit[5] to 1'b1. To preserve the EEPROM's operating lifetime, disable the fault record into the EEPROM at normal operation. Default is 0. 1'b0: disables fault recording into the EEPROM 1'b1: enables fault recording into the EEPROM
7	VIN_OVP_MODE	Sets the V_{IN} OVP mode. 1'b0: auto-retry mode. The MP2853 shuts off the output power when V_{IN} > V_{IN} OVP threshold. The MP2853 restarts when V_{IN} < V_{IN} OVP threshold with a 12.5ms delay time. 1'b1: latch mode. The MP2853 latches down when V_{IN} > V_{IN} OVP threshold. After V_{IN} falls below the OVP threshold, a VDD33 power cycle, EN toggle, command on cycle, or V_{IN} UVLO is required for the device to restart.
6	FAULT_ACT_BOTH-RAILS_EN	Enable bit for both rails reacting to a fault event when a fault occurs on any rail. 1'b0: disables fault shutdown of both rails. Only the fault rail takes action for the fault event. 1'b1: enables fault shutdown of both rails. Both rails respond to the fault and follow the fault rail's protection mode (no action, hiccup, latch off, or retry six times). PG of the non-fault rail indicates low after a 2μs delay unless the fault rail's protection mode is no action. Enable this bit in SVI2 mode.
5	PWM_PIN_FAULT_ DETECT_R2_EN	Enables the PWM pin to be used as the Intelli-Phase fault type indicator and record the fault type into the EEPROM. For Rail 2 only. For some Intelli-Phase products, PWM can report the Intelli-Phase fault type. When this function is enabled, the MP2853 monitors the voltage on PWM to detect the fault type after the VR shuts down. 1'b0: disables PWM as the Intelli-Phase fault type indicator 1'b1: enables PWM as the Intelli-Phase fault type indicator
4	PWM_PIN_FAULT_ DETECT_R1_EN	Enables the PWM pin to be used as the Intelli-Phase fault type indicator and record the fault type into the EEPROM. For Rail 1 only. For some Intelli-Phase products, PWM can report the Intelli-Phase fault type. When this function is enabled, the MP2853 monitors the voltage on PWM to detect the fault type after the VR shuts down. 1'b0: disables PWM as the Intelli-Phase fault type indicator 1'b1: enables PWM as the Intelli-Phase fault type indicator
3	OTP_EN	OTP enable bit. 1'b0: enables over-temperature protection 1'b1: disable over-temperature protection
2	RECORD_TEMP_EN	Enable bit for storing and latching the temperature sense value in register READ_TEMPERATURE (8Dh) after a VTEMP fault occurs. This bit is only effective when VTEMP fault detection is enabled. 1'b0: enables hold of the temperature sense value 1'b1: disables hold of the temperature sense value
1:0	DISABLE_VIN_ PROTECTION	Disables V_{IN} UVLO and OV protections at debug mode. Set this bit to 00 in normal operation. 2'b00: enables V_{IN} related protections 2'b11: disables V_{IN} OV and UVLO protections

MFR_LL_LIMIT_SET (DDh)

The MFR_LL_LIMIT_SET command on Page 0 sets the load-line configuration for Rail 1.

Command	MFR_LL_LIMIT_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15:13	AC_DROOP	Sets the AC droop current value. In the MP2853, the initial droop current is defined with: $I_{DROOP\_INI} = \frac{5}{32} \times I_{CS\_SUM}$ Where I_{DROOP_INI} is the initial droop current, and I_{CS_SUM} is the current in CS_SUM (in μA). The MP2853 provides eight levels of AC droop. AC droop injection is ineffective automatically when DC droop ≠ 0. Always connect a ≥200Ω resistor from V_{FB} to VDIFF to generate the AC droop. 3'b000: 0 3'b001: 0.6 x I_{DROOP_INI} 3'b010: 0.8 x I_{DROOP_INI} 3'b011: 1.0 x I_{DROOP_INI} 3'b100: 1.2 x I_{DROOP_INI} 3'b101: 1.4 x I_{DROOP_INI} 3'b110: 1.6 x I_{DROOP_INI} 3'b111: 1.8 x I_{DROOP_INI}
12	PMBUS_SVI_LL_SEL	Enable bit to force the digital load line via the PMBus™. 1'b0: SVI mode. The load-line slope is determined by the SVI2 telemetry packet 1'b1: PMBus™ mode. The load-line slope is determined by the load-line level bit[11:9].
11:9	PMBUS_LL_LEVEL	Sets the PMBus™ load-line slope (DC droop) level. This bit is active when bit[12] = 1. The MP2853 provides eight levels of DC droop. 3'b000: 0 3'b001: 0.6 x I_{DROOP_INI} 3'b010: 0.8 x I_{DROOP_INI} 3'b011: 1.0 x I_{DROOP_INI} 3'b100: 1.2 x I_{DROOP_INI} 3'b101: 1.4 x I_{DROOP_INI} 3'b110: 1.6 x I_{DROOP_INI} 3'b111: 1.8 x I_{DROOP_INI}
8:3	250mV_LL_LIMIT_ OFFSET	Offset setting for 250mV droop calculation. 0.4mV/LSB.
2:0	TIME_INTERVAL_PER_ LOAD_LINE_STEP	Sets the time interval for each load-line step change. 1μs/LSB.

MFR_SLOPE_SR_URS (DEh)

The MFR_SLOPE_SR_URS command on Page 0 is used to set the slope compensation slew rate for Rail 1 in USM. This slope compensation takes action before each PWM on pulse when the switching cycle is limited to 40μs.The slope capacitance is fixed with 3.9pF.

Command	MFR_SLOPE_SR_URS							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	CURRENT_SOURCE						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	CURRENT_SOURCE	Sets the current source value for slope voltage generation in USM. 0.25μA/LSB.

In general designs, set CURRENT_SOURCE = 2 to make the PWM on-pulse stable in USM.

MFR_OFFSET_SET (DFh)

The MFR_OFFSET_SET command on Page 0 is used to set the Rail 1 special offset and initial offset. Refer to the AMD Series VID Interface 2.0 (SVI2) specification Rev 1.07 on page 41 to page 42 for more information.

Command	MFR_OFFSET_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	SPECIAL_OFFSET								INITIAL_OFFSET						

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
14:7	SPECIAL_OFFSET	Adds a positive offset over the initial VID to support output voltages higher than 1.55V. The special offset is effective for SVI VID mode, PMBus™ VID mode, and PVID mode. The special offset is used for CPU over-clocking. 6.25mV/LSB.
6:0	INITIAL_OFFSET	Adds a negative or positive offset over the initial VID to tune the output voltage. This bit is effective in SVI2 VID mode only. 6.25mV/LSB. This bit is in two's complement format. The voltage list below shows the direct value and real-world value. 7'b 000 0000: 0 7'b 000 0001: +6.25mV 7'b 011 1111: +393.75mV 7'b 100 0000: -400mV 7'b 100 0001: -393.75mV 7'b 111 1111: -6.25mV

MFR_OSR_SET (E0h)

The MFR_OSR_SET command is used for overshoot reduction.

Command	MFR_OSR_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X								X						

Bits	Bit Name	Description
15:14, 6	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
13	OSR_EN	Enables the overshoot reduction function. This function can reduce the V_{OUT} overshoot at the load release. 1'b0: disables the overshoot reduction function 1'b1: enables the overshoot reduction function
[12:7]	OSR_FLAG_BLANK_ TIME	Sets the OSR flag blanking time once OSR is ineffective after the OSR_FLAG filter time ends and OSR flat resets. 20ns/LSB.
[5:0]	OSR_FLAG_FILTER_ TIME	Sets the minimum effective time of the OSR flag once VFB > VREF + 25mV (VFB+ window) and the OSR flag is set. 5ns/LSB.

MFR_BLANK_TIME (E1h)

The MFR_BLANK_TIME command is used to set the minimum time between two neighboring PWMs in multi-phase operation. The blanking time makes the system stable by limiting the multi-phase maximum frequency at the transient conditions. The blanking time is recommended to be higher than 80ns in dual-phase operation. The blanking time is also used to set the slope compensation voltage initiation point. Refer to the MFR_SLOPE_SR_2PS (E2h, Page 0) for more information.

Command	MFR_BLANK_TIME															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	BLANKING_TIME					

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
5:0	BLANKING_TIME	Sets the minimum time between two neighboring phases in dual-phase operation and sets the slope compensation initiation point. 5ns/LSB.

MFR_SLOPE_SR_2PS (E2h)

Slope compensation is used to provide enough noise immunity for PWM generation and make the PWM switches stable.

Slope compensation is generated by a PMBus™-programmable current source and a PMBus™-programmable capacitor. Figure 27 shows a slope voltage curve inside the MP2853 using a 2-phase operation.

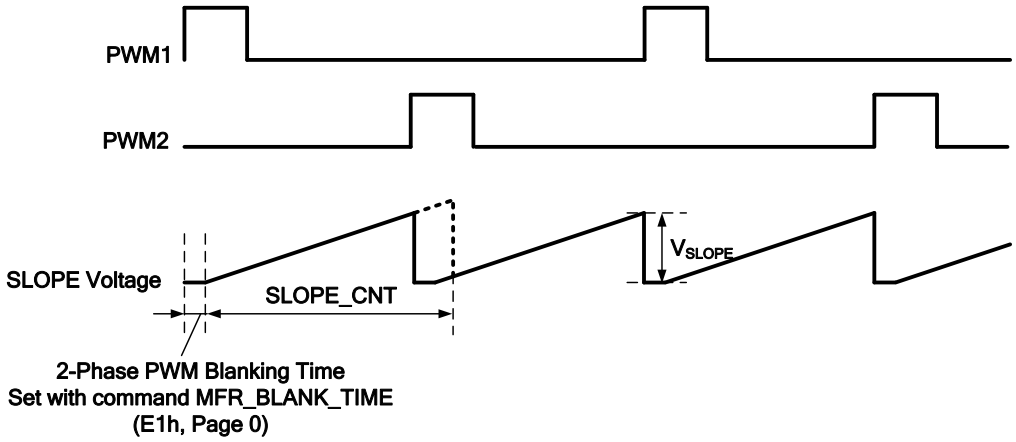


Figure 27: Slope Voltage at 2-Phase CCM Power State

The slope slew rate can be calculated with Equation (22):

$$SLOPE\_SR = 16892 \times \frac{CURRENT\_SOURCE}{(16 - CAP)} \quad (22)$$

Where SLOPE_SR is the slope voltage slew rate (in V/s), CURRENT_SOURCE is a PMBus™ register to program the current value for slope voltage generation (in decimals), and CAP is a PMBus™ register to program the capacitance for slope voltage generation (in decimals).

The MP2853 provides registers for each power state to program CURRENT_SOURCE and CAP independently. For each CCM power sate, the slope voltage amplitude (V_{SLOPE}) can be calculated with Equation (23):

$$V_{SLOPE} = SLOPE\_SR_{@n-PS} \times (\frac{T_{SW}}{n} - t_{BLANK}) \quad (23)$$

Where $SLOPE\_SR_{@n-PS}$ is the slope voltage slew rate at n-phase CCM operation (in V/s), n is the active phase number, T_{SW} is the single-phase switching period set with command FREQUENCY_SWITCH (33h) (in s), and t_{BLANK} is the PWM blanking time set with command MFR_BLANK_TIME (E1h) (in s).

In general designs, a slope voltage amplitude (V_{SLOPE}) of 20mV to 30mV is used to cover all potential T_{ON}, L, and C_{OUT} variations. Lower slope voltages result in faster load transient responses, while higher slope voltage lead to better noise immunity and less PWM jittering.

The MP2853 also provides a PMBus™-programmable slope clamp time. The clamp time is used to limit the slope voltage when the switching off-time is too long (i.e.: DCM operation or output load release transient). This off-time should cover the regular PWM switching off-time. The slope voltage is clamped once the clamp timer expires, which means there is no more slope compensation. To ensure enough time margin for slope compensation in 1-, 2-, 3-, or 4-phase CCM, design the slope clamp timer with 130% of the switching off-time as shown in Equation (24):

$$t_{SLOPE\_CLAMP} = 1.3 \times \left(\frac{T_{SW}}{n} - t_{BLANK} \right) \quad (24)$$

Where t_{SLOPE_CLAMP} is the slope clamping timer (in s), n is the active phase number, T_{SW} is the single-phase switching period (in s), and t_{BLANK} is the PWM blanking time set with command MFR_BLANK_TIME (E1h) (in s).

The command MFR_SLOPE_SR_2PS on Page 0 is used to set the slope compensation slew rate at 2-phase CCM. For Rail 1 only.

Command	MFR_SLOPE_SR_2PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:6	CAP	Sets the capacitance for slope compensation at 2-phase CCM. The capacitance can be calculated with: $(16-\text{CAP})\times 1.85\text{pF}$ 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation at 2-phase CCM. The current source can be calculated with: $\text{CURRENT\_SOURCE}\times 0.25\mu\text{A}$ 0.25μA/LSB.

MFR_SLOPE_CNT_2PS (E3h)

The command MFR_SLOPE_CNT_2PS on Page 0 is used to set the slope voltage clamp time at 2-phase CCM.

Command	MFR_SLOPE_CNT_2PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	SLOPE_CNT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:0	SLOPE_CNT	Sets the slope clamp timer for 2-phase CCM. 5ns/LSB.

MFR_SLOPE_SR_1PS (E4h)

The MFR_SLOPE_SR_1PS command on Page 0 is used to set the slew rate of slope compensation for Rail 1 1-phase CCM.

Command	MFR_SLOPE_SR_1PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:6	CAP	Sets the capacitance for slope compensation at 1-phase CCM. The capacitance can be calculated with: $(16-CAP)\times 1.85pF$ 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation at 1-phase CCM. The current source can be calculated with: $CURRENT\_SOURCE\times 0.25\mu A$ 0.25μA/LSB.

MFR_SLOPE_CNT_1PS (E5h)

The MFR_SLOPE_CNT_1PS command on Page 0 is used to set the slope voltage clamp time at 1-phase CCM.

Command	MFR_SLOPE_CNT_1PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:0	SLOPE_CNT	Sets the slope clamp timer for 1-phase CCM. 5ns/LSB.

MFR_SLOPE_SR_0P5PS (E6h)

The MFR_SLOPE_SR_0P5PS command on Page 0 is used to set the slope compensation slew rate for Rail 1 1-phase DCM.

Command	MFR_SLOPE_SR_0P5PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:6	CAP	Sets the capacitance for slope compensation at 1-phase DCM. The capacitance can be calculated with: $(16-CAP)\times 1.85pF$ 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation at 1-phase DCM. The current source can be calculated with: $CURRENT\_SOURCE\times 0.25\mu A$ 0.25μA/LSB.

MFR_SLOPE_CNT_0P5PS (E7h)

The MFR_SLOPE_CNT_0P5PS command on Page 0 is used to set the slope voltage clamp time at 1-phase DCM. The slope voltage at DCM is slightly different in CCM. At 1-phase DCM, the off-time is increased to reduce switching frequency as the load current reduces. The slope voltage clamp time should be long enough to avoid the period of SW node freewheeling when the zero-current detection (ZCD) turns off the LS-FET to transition the SW node to Hi-Z (see Figure 28).

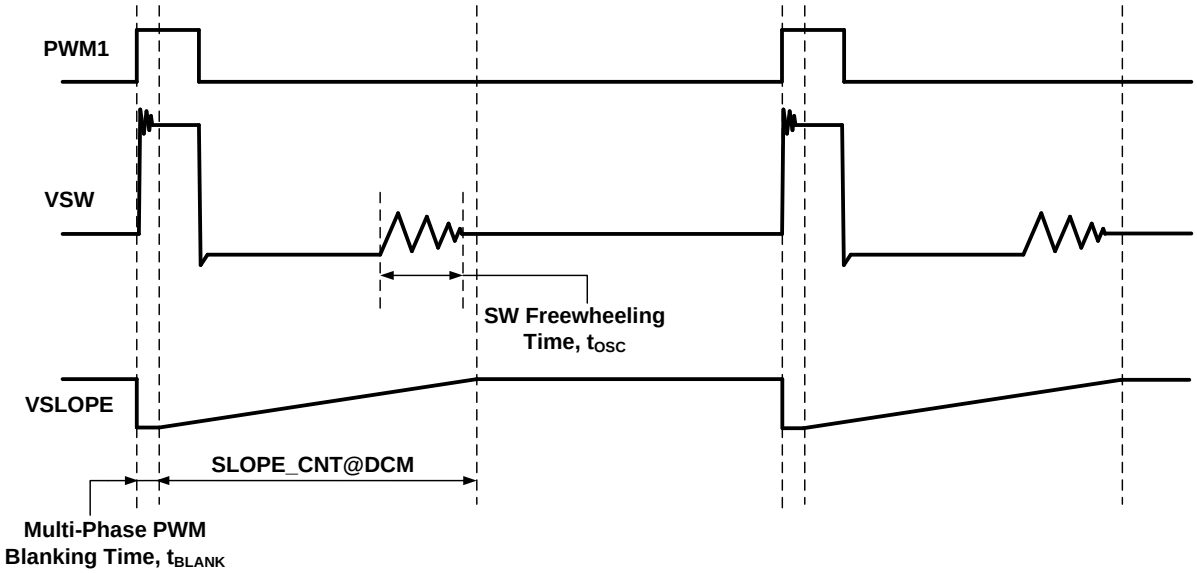


Figure 28: Slope Voltage Compensation at DCM

In general, it is recommended to design the slope clamp time for DCM operation with Equation (25):

$$t_{SLOPE\_CLAMP@DCM} = 1.1 \times \left(T_{SW} - t_{BLANK} + t_{SW\_OSC} \right) \quad (25)$$

Where $t_{SLOPE\_CLAMT@DCM}$ is the slope clamp time at 1-phase DCM (in s), T_{SW} is the single-phase switching period set with command FREQUENCY_SWITCH (33h) (in s), t_{BLANK} is the PWM blanking time set with command MFR_BLANK_TIME (E1h) (in s), and t_{SW_OSC} is the switch node freewheeling time (in s).

The V_{SLOPE} at DCM is determined by the real-time switching frequency. V_{SLOPE} at DCM can be calculated with the Equation (26):

$$V_{SLOPE@DCM} = \begin{cases} V_{SLOPE\_SR@DCM} \times \left(T_{SW\_DCM} - t_{BLANK} \right) & T_{SW\_DCM} < T_{SLOPE\_CLAMP@DCM} \\ V_{SLOPE\_SR@DCM} \times T_{SLOPE\_CLAMP@DCM} & T_{SW\_DCM} \geq T_{SLOPE\_CLAMP@DCM} \end{cases} \quad (26)$$

In designs, set the slope voltage amplitude at DCM from 20mV to 30mV.

Command	MFR_SLOPE_CNT_0P5PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	SLOPE_CNT					

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
5:0	SLOPE_CNT	Sets the slope clamp timer for 1-phase DCM. 80ns/LSB.

MFR_SLOPE_SR_4PS (E8h)

The MFR_SLOPE_SR_4PS command on Page 0 is used to set the slope compensation slew rate for Rail 1 4-phase CCM.

Command	MFR_SLOPE_SR_4PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:6	CAP	Sets the capacitance for slope compensation at 4-phase CCM. The capacitance can be calculated with: $(16-\text{CAP})\times 1.85\text{pF}$ 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation at 4-phase CCM. The current source can be calculated with: $\text{CURRENT\_SOURCE}\times 0.25\mu\text{A}$ 0.25μA/LSB.

MFR_SLOPE_CNT_34PS (E9h)

The MFR_SLOPE_CNT_34PS command on Page 0 is used to set the slope voltage clamp time at 3- or 4-phase CCM.

Command	MFR_SLOPE_CNT_34S															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	SLOPE_CNT_3PS								SLOPE_CNT_4PS							

Bits	Bit Name	Description
15:8	SLOPE_CNT_3PS	Sets the slope clamp timer for 3-phase CCM. 5ns/LSB.
7:0	SLOPE_CNT_4PS	Sets the slope clamp timer for 4-phase CCM. 5ns/LSB.

MFR_SLOPE_SR_3PS (EAh)

The MFR_SLOPE_SR_3PS command on Page 0 is used to set the slope compensation slew rate for Rail 1 3-phase CCM.

Command	MFR_SLOPE_SR_3PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:6	CAP	Sets the capacitance for slope compensation at 3-phase CCM. The capacitance can be calculated with: $(16-CAP)\times 1.85pF$ 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation at 3-phase CCM. The current source can be calculated with: $CURRENT\_SOURCE\times 0.25\mu A$ 0.25μA/LSB.

MFR_TRIM_34PS (ECh)

The MFR_TRIM_34PS command on Page 0 is used to trim the output voltage at 3-phase CCM and 4-phase CCM of Rail 1.

Command	MFR_TRIM_34PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	VTRIM_3PS_CCM				X	VTRIM_4PS_CCM				X

Bits	Bit Name	Description
15:10, 5, 0	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:6	VTRIM_3PS_CCM	Sets the reference voltage trim for 3-phase CCM. 2.3mV/LSB.
4:1	VTRIM_4PS_CCM	Sets the reference voltage trim for 4-phase CCM. 2.3mV/LSB.

MFR_ADDR_PMBUS (EDh)

The MFR_ ADDR_PMBUS command is used to set the PMBus™ address.

Command	MFR_ADDR_PMBUS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X		ADDR_MSB			ADDR_LSB			

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7	ADDR_CONFIG_MODE	Sets the PMBus™ address 4LSB setting mode. 1'b0: sets the PMBus™ 4LSB by the ADDR voltage 1'b1: sets the PMBus™ 4LSB by the register
6:4	ADDR_MSB	Sets the 3MSB of the PMBus™ address. Ranges from 0 to 7.
3:0	ADDR_LSB	Sets or returns the 4LSB of the PMBus™ address. When bit [7] = 1'b0, the PMBus™ address 4LSB is set by the ADDR voltage. Bit[3:0] returns the PMBus™ 4LSB address. When bit [7] = 1'b1, the 4LSB of the PMBus™ is set with bit[3:0].

For example, when MFR_ADDR_PMBUS (EDh) = 0x00A0, the PMBus™ address is 20h, and 4LSB is set from register. When MFR_ADDR_PMBUS (EDh) = 0x0020, the PMBus™ address is 20h, and 4LSB is set by the ADDR voltage.

VENDOR_ID (EFh)

The VENDOR_ID command sets the unique identity for the VR vendors. The default is 0x25.

Command	VENDOR_ID							
Format	Unsigned Binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VENDOR_ID							

Bits	Bit Name	Description
7:0	VENDOR_ID	Returns the vendor ID of the MP2853. The value is fixed at 0x25.

PRODUCT_ID (F0h)

The PRODUCT_ID command sets the unique identity for the VR vendors. The default is 0x83.

Command	PRODUCT_ID							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PRODUCT_ID							

Bits	Bit Name	Description
7:0	PRODUCT_ID	Returns the product ID of the MP2853. The value is fixed at 0x83.

CONFIG_ID (F1h)

CONFIG_ID provides the configuration code identifier for the register settings stored in the EEPROM. MPS provides four digital codes (“xxxx”) for each application. The MP2853 full part number includes these four digits as a suffix (i.e.: MP2853GU-xxxx). Each “x” represents a hexadecimal value between 0 and F. The higher two digits are fixed at “00.” The lower two digits are set in register CONFIG_ID (F1h).

Command	CONFIG_ID							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	CONFIG_ID							

Bits	Bit Name	Description
7:0	CONFIG_ID	Sets the lower two digits of the configuration code ID.

For example, if CONFIG_ID (F1h) = 0x11, the configuration ID is 0011, and the full part number is MP2853GU-0011. When using the MPS MP2853 GUI to configure the device, if the CONFIG_ID in the configuration file does not match the value in the pre-programmed EEPROM, the configuration file cannot load into the device.

PRODUCT_REV_MPS (F2h)

The PRODUCT_DATA_CODE command is used to track the silicon revision of the MP2853.

Command	PRODUCT_REV_MPS							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PRODUCT_REV_MPS							

Bits	Bit Name	Description
7:0	PRODUCT_REV_MPS	Sets the MP2853 silicon revision tracking number. 8’b 0000 0000: rev 0 8’b 0000 0001: rev 2 8’b 0000 0010: rev 4 8’b 0000 0011: rev 5

INTELLI-PHASE_CS_GAIN (F3h)

The INTELLI-PHASE_CS_GAIN command is used to set the Intelli-Phase current sense gain.

Command	INTELL-PHASE_CS_GAIN							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	INTELLI-PHASE_CS_GAIN_R1				INTELLI-PHASE_CS_GAIN_R2			
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	INTELLI-PHASE_CS_GAIN_R1				INTELLI-PHASE_CS_GAIN_R2			

Bits	Bit Name	Description
7:4	INTELLI-PHASE_CS_ GAIN_R1	Sets the current sense gain of the Intelli-Phase for Rail 1. 4'b0000: 8.5μA/A 4'b0001: 9.7μA/A 4'b0010: 10μA/A 4’b0011: 5μA/A others: reserved
3:0	INTELLI-PHASE_CS_ GAIN_R2	Sets the current sense gain of the Intelli-Phase for Rail 2. 4'b0000: 8.5μA/A 4'b0001: 9.7μA/A 4'b0010: 10μA/A 4’b0011: 5μA/A others: reserved

MFR_SAMP_LPF (F6h)

The MFR_SAMP_LPF command is used to set the filter parameters for V_{OUT} and I_{OUT} PMBus™ reporting. The setting in MFR_SAMP_LPF is effective for both rails.

Command	MFR_SAMP_LPF							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X					

Bits	Bit Name	Description
7:5	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
4	VO_REPORT_FILTER	Sets the filter parameter of the V_{OUT} report to the SVI2 telemetry and V_{OUT} report in register READ_VOUT (8Ch). 1'b0: no V_{OUT} report filter 1'b1: two-point moving average filter
3	PWM_TRI-STATE_MODE	Sets the PWM tri-state output setting. 1'b0: Hi-Z mode 1'b1: middle voltage (VDD33/2)
2	IO_SVI_REPORT_ FILTER	Sets the filter parameter of the I_{OUT} SVI2 telemetry. 1'b0: no V_{OUT} report filter 1'b1: two-point moving average filter
1:0	IO_PMBUS_REPORT_ FILTER	Sets the filter parameter of output current reporting in register READ_IOUT (8Ch). 2'b00: no I_{OUT} report filter 2'b01: two-point moving average filter 2'b10: four-point moving average filter 2'b11: eight-point moving average filter

MFR_VR_CONFIG2 (F7h)

The MFR_ VR_CONFIG2 is used to configure some basic functions of the MP2853.

Command	MFR_VR_CONFIG2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15	SLOPE_ COMPENSATION_SET	Slope compensation initiation time mode bit. On the MP2853, slope compensation can be initiated after the PWM blanking time ends or after the PWM on time ends. 1’b0: slope compensation initiates after PWM blanking time ends 1’b1: slope compensation initiates after PWM on time ends
14:13	MFR_BG_CHOP_ MODE	Selects the frequency of the band gap chop. Default is 500kHz. 2’b00: disables band gap chop 2’b01: 125kHz 2’b10: 250kHz 2’b11: 500kHz
12:10	DVIDUP_STEP_NUM_ R2	Sets the extra VID steps count for Rail 2 when DVID is up. The extra VID steps are used to compensate the droop voltage drop caused by the output capacitor charging during DVID up. 3’b000: no steps rise 3’b001: one VID step rises 3’b010: two VID steps rise 3’b011: three VID steps rise 3’b100: four VID steps rise 3’b101: five VID steps rise 3’b110: six VID steps rise 3’b111: seven VID steps rise

Bits	Bit Name	Description
9:7	DVIDUP_STEP_NUM_R1	Sets the extra VID steps count for Rail 1 when DVID is up. The extra VID steps are used to compensate for the droop voltage drop caused by the output capacitor charging during DVID up. 3'b000: no steps rise 3'b001: one VID step rises 3'b010: two VID steps rise 3'b011: three VID steps rise 3'b100: four VID steps rise 3'b101: five VID steps rise 3'b110: six VID steps rise 3'b111: seven VID steps rise
6	EN_OFF_MODE_SEL	Sets the EN power-off mode. This bit is not effective in low-power mode (register MFR_CONFIG4 (0Dh) bit[0] = 0). In low-power mode, EN always Hi-Z powers off the converter. 1'b0: Hi-Z off 1'b1: soft off
5:4	VIDDAC_FILTER_R2_SEL	Selects the filter for VID-DAC of Rail 2. 2'b00: adds a 1μs filter while VID2 is ramping down 2'b01: adds a 3μs filter while VID2 is ramping down 2'b10: adds a 5μs filter while VID2 is ramping down 2'b11: adds a 7μs filter while VID2 is ramping down
3	VIDDAC_FILTER_R1&2_EN	Adds a VID-DAC filter when DVID downward can avoid the output voltage undershoot. 1'b0: disables the VID-DAC filter for both rails 1'b1: enables the VID-DAC filter for both rails
2:1	VIDDAC_FILTER_R1_SEL	Selects the filter for VID-DAC of Rail 1. 2'b00: adds a 1μs filter while VID1 is ramping down 2'b01: adds a 3μs filter while VID1 is ramping down 2'b10: adds a 5μs filter while VID1 is ramping down 2'b11: adds a 7μs filter while VID1 is ramping down
0	DEALY_LINE_LOOP_EN	Enables the delay line loop can reduce the PWM jitter sharply when the frequency loop is applied. 1'b0: disables the delay line loop 1'b1: enables the delay line loop

MFR_TIMEOUT (F9h)

The MFR_TIMEOUT command sets the wait timeout value for PMBus™ and SVI communication.

Command	MFR_TIMEOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	PMBUS_TIMEOUT				SVI_TIMEOUT			

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7:4	PMBUS_TIMEOUT	Sets the PMBus™ communication wait timeout time. 1.6ms/LSB. The final PMBus™ timeout time can be calculated with: $1.6ms \times PMBUS\_TIMEOUT + 1.5ms$
3:0	SVI_TIMEOUT	Sets the SVI communication wait timeout time. 0.5μs/LSB.

CLEAR_EEPROM_FAULTS (FFh)

The CLEAR_EEPROM_FAULTS command is used to clear the EEPROM CRC fault that occurs during the copy EEPROM process. This is a write only command. There is no data byte for this command.

PAGE 1 REGISTER MAP

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor through only one physical address for both rails and test mode.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PAGE							

Bits	Bit Name	Description
7:0	PAGE	8’b 0000 0000: Page 0, all commands address Rail 1 unless otherwise noted. 8’b 0000 0001: Page 1, all commands address Rail 2 unless otherwise noted. 8’b 0010 1000: Page 28, all commands address to EEPROM register Page 0. 8’b 0010 1001: Page 29, all commands address to EEPROM register Page 1. Others: ineffective input

OPERATION (01h)

The OPERATION command on Page 1 is used to turn the Rail 2 output on and off in conjunction with input from EN. OPERATION is also used to set the output voltage to the upper or lower margin voltages. Rail 2 remains in the command operating mode until a subsequent OPERATION command or a state altering EN changes Rail 2 to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	OPERATION_MODE							

Bits	Bit Name	Description
7:0	OPERATION_MODE	Sets the operation mode for Rail 2. 8’b 00xx xxxx: Hi-Z off 8’b 01xx xxxx: soft off 8’b 1000 xxxx: normal on 8’b 1001 xxxx: margin low 8’b 1010 xxxx: margin high The value of “x” does not matter.

For example, when sending OPERATION (01h) = 0x40 via the PMBus™, the Rail 2 V_{OUT} shuts down softly. When sending OPERATION (01h) = 0x90 via the PMBus™, Rail 2 changes to a margin-low output voltage level with a dynamic VID (DVID) slew rate. When sending OPERATION (01h) = 0xA0 via the PMBus™, Rail 2 changes to a margin-high output voltage level with a DVID slew rate.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear the system fault after system initialization ends. This command is write only. There is no data byte for this command.

CLEAR_FAULTS is effective for both rails regardless of the PAGE command value. Faults include V_{IN} UVLO, V_{IN} OVP, OTP, output OVP, UVP, OCP_TDC, OCP_SPIKE, VDIFF SCP protections, PMBus™ communication faults, and EEPROM faults. CLEAR_FAULTS can only clear faults after an OPERATION command off cycle. Once CLEAR_FAULTS is sent, the faults listed above on both rails are cleared, and the fault bits in register MFR_FAULTS1 (84h) are reset if the associated fault is removed.

CONFIG_REV_USER (0Ch)

The CONFIG_REV_USER command on Page 1 is used to track the product revision.

Command	CONFIG_REV_USER															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	X				

Bits	Bit Name	Description
15:4	RESERVED	Unused. Always set to 0.
3:0	CONFIG_REV_USER	Tracks the product revision from 0 to 15. For MPS fab, the default is 4'b0000 unless another value is requested by the customer.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus™ device to copy the Page 0 and Page 1 values in the operating memory to the matching locations in the EEPROM. Any items in the operating memory that do not have matching locations in the EEPROM are ignored.

This command can be used while the device is outputting power. This command is write only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus™ device to copy the Page 0 and Page 1 value of the EEPROM to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the EEPROM. Any items in the EEPROM that do not have matching locations in the operating memory are ignored.

Do not use this command while the device is outputting power or the command will be ignored. This command is write only. There is no data byte for this command.

VOUT_COMMAND (21h)

The VOUT_COMMAND on Page 1 works together with the VDIFF1/2 divider to set the Rail 2 VID-DAC output voltage in PMBus™ VID mode (i.e.: the reference voltage (V_{REF}) of Rail 2 in PMBus™ VID mode). The DAC output voltages range from 0 to 1.55V. For Rail 2, the VDIFF1/2 divider is controlled by command MFR_VR_CONFIG (D0h) bit[3]. When bit[3] = 0, V_{REF} is equal to VOUT_COMMAND. When bit[3] = 1, V_{REF} is half of VOUT_COMMAND.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_VID							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7:0	VOUT_VID	Sets the Rail 2 reference voltage (VID-DAC output voltage) in PMBus™ VID mode. 6.25mV/LSB.

VOUT_TRIM (22h)

The VOUT_TRIM command on Page 1 is used to apply an offset value to the Rail 2 remote sense amplifier output. VOUT_TRIM is generally used by end users to trim the output voltage at the time the PMBus™ device is assembled into the end user's system. This command can also be used to fine tune the output voltage when the designed V_{REF} is out of the 6.25mV step.

Command	VOUT_TRIM															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	VREF_TRIM_2PHASE					VREF_TRIM_1PHASE_CCM					VREF_TRIM_1PHASE_DCM				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
14:10	VREF_TRIM_2PHASE	Adds a fixed offset over remote sense amplifier output at 2-phase operation. (1.56/K_{VDIFF}) mV/LSB Where K_{VDIFF} is the IC internal VDIFF divider ratio. For Rail 2, K_{VDIFF} is controlled by command MFR_VR_CONFIG (D0h) bit[3]. When bit[3] = 0, K_{VDIFF} = 1. When bit[3] = 1, K_{VDIFF} = 0.5. This bit is in two's complement format. Bit[3] is the sign bit. The voltage list below shows the direct value and real-world value. 4'b0000: 0mV 4'b0001: +(1.56/K_{VDIFF}) mV 4'b0111: +(10.92/ K_{VDIFF}) mV 4'b1000: -(12.48/ K_{VDIFF}) mV 4'b1001: -(10.92/ K_{VDIFF}) mV 4'b1111: -(1.56/ K_{VDIFF}) mV
9:5	VREF_TRIM_1PHASE_CCM	Adds a fixed offset over remote sense amplifier output at 1-phase CCM operation. (1.56/K_{VDIFF}) mV/LSB Where K_{VDIFF} is the IC internal VDIFF divider ratio. For Rail 2, K_{VDIFF} is controlled by command MFR_VR_CONFIG (D0h) bit[3]. When bit[3] = 0, K_{VDIFF} = 1. When bit[3] = 1, K_{VDIFF} = 0.5. This bit is in two's complement format. Bit[3] is the sign bit. The voltage list below shows the direct value and real-world value. 4'b0000: 0mV 4'b0001: +(1.56/K_{VDIFF}) mV 4'b0111: +(10.92/ K_{VDIFF}) mV 4'b1000: -(12.48/ K_{VDIFF}) mV 4'b1001: -(10.92/ K_{VDIFF}) mV 4'b1111: -(1.56/ K_{VDIFF}) mV
4:0	VREF_TRIM_1PHASE_DCM	Adds a fixed offset over remote sense amplifier output at 1-phase DCM operation. (1.56/K_{VDIFF}) mV/LSB Where K_{VDIFF} is the IC internal VDIFF divider ratio. For Rail 2, K_{VDIFF} is controlled by command MFR_VR_CONFIG (D0h) bit[3]. When bit[3] = 0, K_{VDIFF} = 1. When bit[3] = 1, K_{VDIFF} = 0.5. This bit is in two's complement format. Bit[3] is the sign bit. The voltage list below shows the direct value and real-world value. 4'b0000: 0mV 4'b0001: +(1.56/K_{VDIFF}) mV 4'b0111: +(10.92/ K_{VDIFF}) mV 4'b1000: -(12.48/ K_{VDIFF}) mV 4'b1001: -(10.92/ K_{VDIFF}) mV 4'b1111: -(1.56/ K_{VDIFF}) mV

VOUT_MAX (24h)

The VOUT_MAX command on Page 1 sets the Rail 2 maximum VID voltage. The Rail 2 VID is limited to VOUT_MAX if the programmed VID plus the offset are higher. This command is effective in SVI VID mode, PMBus™ VID mode, and PVID mode.

Command	VOUT_MAX															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	VOUT_MAX								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:0	VOUT_MAX	Sets the Rail 2 maximum VID plus the offset voltage. This bit is used to limit the sum of the initial VID plus the offset, initial offset, and special offset. 6.25mV/LSB.

VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command sets the Rail 2 margin high reference voltage to which the output is to be changed when the OPERATION command is set to margin high. This command is effective in PMBus™ VID mode only.

Command	VOUT_MARGIN_HIGH															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_MARGIN_HIGH							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7:0	VOUT_MARGIN_HIGH	Sets the Rail 2 margin high state reference voltage level. 6.25mV/LSB.

VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command sets the Rail 2 margin low reference voltage level at which the output is to be changed when the OPERATION command is set to margin low. This command is effective in PMBus™ VID mode only.

Command	VOUT_MARGIN_LOW															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_MARGIN_LOW							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7:0	VOUT_MARGIN_LOW	Sets the Rail 2 margin low state reference voltage level. 6.25mV/LSB.

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command on Page 1 sets the Rail 2 output voltage to the V_{REF} dividing ratio when an external output divider is applied. Use Equation (11) to calculate VOUT_SCALE_LOOP. Use MFR_VR_CONFIG (D0h) bit[5] to determine K_{VDIFF}.

Command	VOUT_SCALE_LOOP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	VOUT_SCALE_LOOP						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	VOUT_SCALE_LOOP	Sets the Rail 2 output voltage to the V_{REF} dividing ratio. V_{REF} ranges from 0 to 1.55V.

For example, to support a 5V output voltage, set command MFR_VR_CONFIG (D0h) bit[5] = 0, select V_{REF} = 0.82V, and VOUT_SCALE_LOOP (29h) = 0x0015.

MFR_ SLOPE_SW_INI (2Ch)

The MFR_SLOPE_SW_INI command sets the Rail 2 initial slope compensation before the first PWM pulse during soft start. The initial slope compensation is used to eliminate the group pulse at the beginning of the soft start. The initial slope compensation can be calculated with Equation (12).

Command	MFR_ SLOPE_SW_INI							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	X	EN	CURRENT_SOURCE_INI					

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6	SLOPE_INI_EN	Enables the soft-start initial slope compensation. The initial slope compensation is used to eliminate the group pulse at the beginning of soft start. 1'b0: disables soft start initial slope compensation 1'b1: enables soft start initial slope compensation
5:0	CURRENT_SOURCE_ INI	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

FREQUENCY_SWITCH (33h)

The FREQUENCY_SWITCH command on Page 1 is used to set the switching frequency for Rail 2. The switching frequency range is from 200kHz to 5.11MHz (with 10kHz per step).

Command	FREQUNCY_SWITCH															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	SWITCH_FREQUENCY								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:0	SWITCH_FREQUENCY	Sets the Rail 2 switching frequency from 200 - 5110kHz. 10kHz/LSB.

For example, to achieve a 500kHz switching frequency, set FREQUENCY_SWITCH = 0x0032.

TON_DELAY (60h)

The TON_DELAY command on Page 1 is used to set the Rail 2 power-on delay time.

Command	TON_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TON_DELAY															

Bits	Bit Name	Description
15:0	TON_DELAY	Sets the Rail 2 power-on delay time. The power-on delay time begins when the system initialization is completed. When the T_{ON} delay time is over, Rail 2 begins soft start. 100μs/LSB.

For example, to get a 10ms T_{ON} delay time, set TON_DELAY (60h) = 0x0064.

TON_RISE (61h)

The TON_RISE command on Page 1 is used to set the Rail 2 reference voltage slew rate at dynamic VID (DVID) transition up or down and margin transition. Use Equation (13) to calculate the Rail 2 DVID slew rate.

Command	TON_RISE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	VID_SR_CNT										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
10:0	VID_SR_CNT	Sets the duration time for each V_{REF} step. The time can be calculated with: $(\text{VID\_SR\_CNT} + 3) \times 50\text{ns}$ Note that the register setting with 5'LSB = 5'b11111 is ineffective. For example, do not set the register value to 0x001F, 0x003F, 0x005F, 0x007F, etc. 50ns/LSB.

TOFF_DELAY (64h)

The TOFF_DELAY command on Page 1 is used to set the Rail 2 power-off delay time. The power-off delay time is effective only at the OPERATION command soft-off and EN soft-off process.

Command	TOFF_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TOFF_DELAY															

Bits	Bit Name	Description
15:0	TOFF_DELAY	Sets the Rail 2 power-off delay time at OPERATION command soft off. 100μs/LSB.

TOFF_FALL (65h)

The TOFF_FALL command is used to set the reference voltage transition down slew rate at soft-off and margin low transition. The sub-register definition is same as in Figure 23. The slew rate also can be calculated with Equation (13).

Command	TOFF_FALL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	VID_SR_CNT										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
10:0	VID_SR_CNT	Sets the duration time for each V_{REF} step. The time can be calculated with: $(\text{VID\_SR\_CNT}+3)\times 50\text{ns}$ Note that the register setting with 5'LSB = 5'b11111 is ineffective. For example, do not set the register value to 0x001F, 0x003F, 0x005F, 0x007F, etc. 50ns/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 1 is used to return the voltage between VOSEN and VORTN (VOSEN - VORTN) in 6.25mV/LSB. The PMBus™ command MFR_VR_CONFIG4 (0Eh, Page 0) bit[0] determines the voltage at which the rail is returned by READ_VOUT (8Bh, Page 1). When bit[0] = 0, READ_VOUT (8Bh, Page 1) returns the VOSEN2 - VORTN2 voltage of Rail 2. When bit[0] = 1, READ_VOUT (8Bh, Page 1) returns the VOSEN1 - VORTN1 voltage of Rail 1.

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	READ_VOUT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:0	READ_VOUT	Returns the differential voltage between VOSEN and VORTN (VOSEN - VORTN). 6.25mV/LSB.

The PMBus™ command READ_VOUT reported output voltage can be calculated with Equation (14). The calculated value of READ_VOUT in the MP2853 is shown in Equation (17).

READ_IOUT (8Ch)

The READ_IOUT command on Page 1 returns the average load current of Rail 2.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	READ_IOUT								
Bits	Bit Name					Description										
15:9	RESERVED					Unused. X indicates that writes are ignored and always read as 0.										
8:0	READ_IOUT					Returns the load current of Rail 2. 0.25A/LSB.										

MFR_SD_VID (A6h)

The MFR_SD_VID command on Page 1 sets the Rail 2 Hi-Z shutdown voltage level. This command is only effective when VID slews down to 0V. VID slewing down to 0 can be caused by DVID to 0V or a VID lower than MFR_VID_OFF (D5h), OPERATION command off, or EN soft off. Once the VID-DAC output is lower than the Hi-Z shutdown voltage level, the output enters PWM Hi-Z shutdown mode. The output voltage is discharged by the load current.

Command	MFR_SD_VID							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_SD_VID						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	MFR_SD_VID	Sets the PWM Hi-Z shuts down the voltage level. Once the Rail 2 VID-DAC output is lower than the Hi-Z shutdown voltage level, the output enters PWM Hi-Z shutdown mode. 6.25mV/LSB.

MFR_PSI_TRIM (A8h)

The MFR_ PSI_TRIM command on Page 1 is used to trim the reference voltage at 2-phase and 1-phase CCM and 1-phase DCM for Rail 2.

Command	MFR_PSI_TRIM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	VTRIM_1PS_DCM				X	VTRIM_1PS_CCM				X	VTRIM_2PS_CCM				X

Bits	Bit Name	Description
15, 10, 5, 0	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
14:11	VTRIM_1PS_DCM	Sets the reference voltage trim for 1-phase DCM. 2.3mV/LSB.
9:4	VTRIM_1PS_CCM	Sets the reference voltage trim for 1-phase CCM. 2.3mV/LSB.
4:1	VTRIM_2PS_CCM	Sets the reference voltage trim for 2-phase CCM. 2.3mV/LSB.

MFR_PG_RDL (A9h)

The MFR_ PG_RDL command on Page 1 is used to set the Rail 2 power good delay time. This command is effective at PG non-SVI mode only, with MFR_VR_CONFIG3 (C4h) bit[3] = 1. In PG SVI mode with MFR_VR_CONFIG3 (C4h) bit[3] = 0, PG asserts high when V_{REF} reaches the boot-up voltage level.

Command	MFR_PG_RDL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	PG_DELAY_TIME									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:0	PG_DELAY_TIME	Sets the Rail 2 PG asserting high delay time. 5μs/LSB.

VOUT_VR_CAL (ACh)

The VOUT_VR_CAL command on Page 1 is used to set the gain from the ADC sensed VOSEN2 - VORTN2 voltage to SVI2 V_{OUT} telemetry and V_{OUT} report in register READ_VOUT (8Bh). VOUT_VR_CAL also sets an offset on the output voltage SVI2 telemetry and V_{OUT} report in register READ_VOUT (8Bh). This command is dedicated for MP2853 Rail 2 output voltage reporting only.

Command	VOUT_VR_CAL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	OFFSET						GAIN							

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
13:8	OFFSET	Adds an offset to the SVI2 V_{OUT} telemetry and V_{OUT} report in register READ_VOUT (8Bh). This bit is for the Rail 2 output voltage report only. OFFSET is in two's complement format. Bit[13] is the sign bit. (6.25/K_{VDIFF}) mV/LSB. The voltage list below shows the direct value and real-world value. 6'b 00 0000: 0mV 6'b 00 0001: +(6.25/K_{VDIFF}) mV 6'b 01 1111: +(193.75/K_{VDIFF}) mV 6'b 10 0000: -(200/K_{VDIFF}) mV 6'b 10 0001: -(193.75/K_{VDIFF}) mV 6'b 11 1111: -(6.25/K_{VDIFF}) mV
7:0	GAIN	Sets the gain from the ADC sensed VOSEN - VORTN voltage to the SVI2 V_{OUT} telemetry and V_{OUT} report in register READ_VOUT (8Bh). This bit for the Rail 2 output voltage report only. In the MP2853, set GAIN = 0x40 to get the correct VOSEN - VORTN voltage report.

Use Equation (16) to calculate the SVI2 VOUT report from the VR to the processor. Use Equation (17) to calculate the value in the register READ_VOUT (8Bh).

IOUT_VR_CAL (ADh)

The IOUT_VR_CAL command on Page 1 is used to set the gain and offset for the Rail 2 I_{OUT} telemetry to the SVI2 processor. Use Equation (18) to calculate the IOUT SVI2 report with GAIN and OFFSET. The GAIN can be calculated with Equation (19).

Command	IOUT_VR_CAL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OFFSET							GAIN								

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
15:9	OFFSET	Add an offset to the I_{OUT} telemetry data to the processor. This bit is in two's complement format. Bit[15] is the sign bit. The resolution is determined by the maximum report current defined by 0xFF. The voltage list below shows the direct value and real-world value. 7'b 000 0000: 0 7'b 000 0001: 1 7'b 011 1111: 63 7'b 100 0000: -64 7'b 100 0001: -63 7'b 111 1111: -1
8:0	GAIN	Sets the gain for the Rail 2 I_{OUT} telemetry to the SVI2 processor.

MFR _PSI_SET (C0h)

The MFR_PHASE_PSI_CONFIG command is used to set the phase assignment for both rails or force Rail 2 at a given power state mode.

Command	MFR _PSI_SET							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	EN	MFR_PSI_SET	

Bits	Bit Name	Description
7:3	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
2	FORCE_ACTIVE_ PHASE_NUM_EN	Enable bit to force the power state for Rail 2. When set to 1, then the forced power sate on Rail 2 is enabled, and the power sate is determined by bit[2:0] in register MFR_PSI_SET (C0h, Page 1). Set this bit to 0 during normal operation. 1'b0: disables forced power state 1'b1: enables forced power state
1:0	MFR_PSI_SET	Rail 2 forced power state setting. This bit is only effective when bit[3] = 1. When the forced phase number is higher than the set in bit[6:4], run with the phase count set in bit[6:4]. 2'b00: 1-phase DCM 2'b01: 1-phase CCM 2'b10: 2-phase CCM others: 1-phase CCM

MFR_OCP_SET (C2h)

The MFR_OCP_SET command on Page 1 is used to set the Rail 2 OCP_TDC and OCP_SPIKE behavior mode and blanking times.

Command	MFR_OCP_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MODE		EN	MFR_OCPTDC_TRIGDELAY								EN	MFR_OCPSPIKE_ TRIGDELAY			

Bits	Bit Name	Description
15:14	MFR_OCP_MODE	Selects the protection mode for both OCP_TDC and OCP_SPIKE. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
13	MFR_OCPTDC_EN	Enable bit for OCP_TDC protection. 1'b0: disables OCP_TDC protection 1'b1: enables OCP_TDC protection
12:5	MFR_OCPTDC_ TRIGDELAY	Sets the OCP_TDC fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_TDC threshold for the OCP_TDC blanking time. 20µs/LSB.
4	MFR_OCPSPIKE_EN	Enable bit for OCP_SPIKE protection. 1'b0: disables OCP_SPIKE protection 1'b1: enables OCP_SPIKE protection
3:0	MFR_OCPSPIKE_ TRIGDELAY	Sets the OCP_SPIKE fault blanking time. The OCP_L signal asserts if the sensed inductor current exceeds the OCP_SPIKE threshold for an OCP_SPIKE blanking time. 200ns/LSB.

MFR_DELAY_SET (C3h)

The MFR_DELAY_SET is use to set the VID slew-up droop component resetting delay time and the VOTF delay time after VID slew-up ends.

Command	MFR_DELAY_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	MFR_DROOPFALL_DEALY					MFR_VOTF_DELAY							

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
12:8	MFR_DROOPFALL_ DELAY	Sets the delay time between V_{REF} reaching the target VID + DROOP_VID and V_{REF} falling back to the target VID. Set this bit to 1µs in general applications. 200ns/LSB.
7:0	MFR_VOTF_DELAY	Sets the delay time from V_{REF} reaching the target VID to the VR issuing a VOTF completion packet to the processor. 100ns/LSB.

IOUT_CAL_CFG (C5h)

The IOUT_CAL_CFG command on Page 1 is used to set the gain and offset for the Rail 2 output current reporting to register READ_IOUT (8Ch, Page 1).

Command	IOUT_CAL_CFG															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OFFSET						GAIN									

Bits	Bit Name	Description
15:10	OFFSET	Sets the negative offset of the Rail 2 output current reporting in register READ_IOUT (8Ch, Page 1). $READ\_IOUT = 4 \times (IOUT - OFFSET \times 0.5)$ Where READ_IOUT is the decimal value in register READ_IOUT (8Ch, Page 1). OFFSET is set to 0 by default. 0.5A/LSB.
9:0	GAIN	Sets the gain from the IMON2 voltage to the Rail 1 output current reporting in register READ_IOUT (8Ch, Page 1). The MP2853 senses the Rail 2 output current by sampling the voltage on IMON2 with a high-accuracy ADC. GAIN is used to convert the IMON2 voltage to a direct I_{OUT} format and return it with command READ_IOUT (8Ch, Page 1). Use Equation (20) to calculate GAIN.

MFR_RES_DROOP_0P2 (C6h)

The MFR_RES_DROOP_0p2 command on Page 1 is used to set 20% of the initial load-line resistor. For Rail 2 only.

Command	MFR_RES_DROOP_0P2							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_RES_DROOP_0P2			

Bits	Bit Name	Description
7:4	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
3:0	MFR_RES_DROOP_0P2	Sets 20% of the initial load-line resistor for Rail 2. 0.1mΩ/LSB.

For example, if the initial load line of Rail 2 is 2mΩ, set MFR_RES_DROOP_0P2 (C6h) = 0x04h.

MFR_AUTO_PS (C7h)

The MFR_AUTO_PS command on Page 1 is used to set the Rail 2 auto-phase shedding (APS) threshold and hysteresis. Refer to the Auto-Phase Shedding section on page 23 for more information.

Command	MFR_AUTO_PS															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	MFR_PH_HYS				MFR_1PHASE_LOW						MFR_DCM_LOW			

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
13:10	MFR_PH_HYS	Sets the current hysteresis value for APS. 0.5A/LSB.
9:4	MFR_1PHASE_LOW	Sets the phase shedding load level from 2-phase CCM to 1-phase CCM. 0.5A/LSB.
3:0	MFR_DCM_LOW	Sets the phase shedding load level from 1-phase CCM to 1-phase DCM. 0.5A/LSB.

MFR_DECAY_SET (C9h)

The MFR_DECAY_SET command on Page 1 is used to set the activation criteria of decay mode in SVI2 mode. Refer to the AMD Serial VID Interface 2.0 (SVI2) Specification Rev 1.07 section on page 22 for more information.

Command	MFR_DECAY_SET							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X		

Bits	Bit Name	Description
7:2	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
1:0	MFR_DECAY_LENGTH	Sets the Rail 2 reference voltage minimum holding time for one VID step in decay mode. 100ns/LSB.

MFR_CUR_OFFSET (CAh)

The MP2853 provides OCP_PHASE protection to limit the per-phase valley current. OCP_PHASE is implanted by monitoring and comparing the cycle-by-cycle sensed CS current with a current reference. The MP2853 provides the command MFR_OCP_PHASE_LIMIT (DAh) to program the OCP_PHASE limit in a direct current format. This command also provides two registers, MFR_CUR_OFFSET (CAh) and MFR_CUR_GAIN (D3h), to convert the direct current format to internal analog logic signals. The command MFR_CUR_OFFSET is used to set the offset for the OCP_PHASE limitation calculation.

Command	MFR_CUR_OFFSET							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_CUR_OFFSET						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	MFR_CUR_OFFSET	Sets the calculation offset for Rail 2 OCP_PHASE limit setting. Calculate the MFR_CUR_OFFSET with: $\text{MFR\_CUR\_OFFSET} = \frac{10086}{\text{MFR\_CUR\_GAIN}}$ Where MFR_CUR_GAIN is the value in register MFR_CUR_GAIN (D3h).

MFR_BOOT_SR (CBh)

The MFR_BOOT_SR command on Page 1 is used to set the Rail 2 boot-up voltage slew rate when Rail 2 is turned on.

Command	MFR_BOOT_SR															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	VID_SR_CNT										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
10:0	VID_SR_CNT	Sets the duration time for each V_{REF} step. The time can be calculated with: $(VID\_SR\_CNT + 3) \times 50ns$ Note that the register setting with 5'LSB = 5'b11111 is ineffective. For example, do not set the register value to 0x001F, 0x003F, 0x005F, 0x007F, etc. 50ns/LSB.

The definition of VID_SR_VID is shown in Figure 23. The boot-up voltage slew rate can be calculated with Equation (13).

MFR_OCPSPIKE_12PS_LEVEL (CCh)

The MFR_OCPSPIKE_12PS_LEVEL command on Page 1 is used to set the Rail 2 OCP_SPIKE current level at 1- and 2-phase operation.

Command	MFR_OCPSPIKE_12PS_LEVEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_OCPSPIKE_2PS_LEVEL						MFR_OCPSPIKE_1PS_LEVEL					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
11:6	MFR_OCPSPIKE_2PS_LEVEL	Sets the Rail 2 OCP_SPIKE current level at 2-phase operation. (40/K_{CS}) A/LSB. The final OCP_SPIKE register value can be calculated with : $MFR\_OCPSPIKE\_2PS\_LEVEL = \frac{OCP\_SPIKE\_2PS \times K_{CS}}{40} + 4$ Where OCP_SPIKE_2PS is the OCP_SPIKE valley current threshold at 2-phase operation (in A), and K_{CS} is the Intelli-Phase current sense gain (in μA/A).
5:0	MFR_OCPSPIKE_1PS_LEVEL	Sets the Rail 2 OCP_SPIKE current level at 1-phase operation. (40/K_{CS}) A/LSB. The final OCP_SPIKE register value can be calculated with: $MFR\_OCPSPIKE\_1PS\_LEVEL = \frac{OCP\_SPIKE\_1PS \times K_{CS}}{40} + 4$ Where OCP_SPIKE_1PS is the OCP_SPIKE valley current threshold at 1-phase operation (in A), K_{CS} is the Intelli-Phase current sense gain (in μA/A).

MFR_OCPTDC_12PS_LEVEL (CEh)

The MFR_OCPTDC_12PS_LEVEL command on Page 1 is used to set the Rail 2 OCP_TDC current level at 1- and 2-phase operation.

Command	MFR_OCPTDC_12PS_LEVEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_OCPTDC_2PS_LEVEL						MFR_OCPTDC_2PS_LEVEL					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
11:6	MFR_OCPTDC_2PS_LEVEL	Sets the Rail 2 OCP_TDC current level at 2-phase operation. (40/K_{CS}) A/LSB. $MFR\_OCPTDC\_2PS\_LEVEL = \frac{OCP\_TDC\_2PS \times K_{CS}}{40} + 4$ Where OCP_TDC_1PS is the OCP_TDC valley current threshold at 2-phase operation (in A), and K_{CS} is the Intelli-Phase current sense gain (in μA/A).
5:0	MFR_OCPTDC_1PS_LEVEL	Sets the Rail 2 OCP_TDC current level at 1-phase operation. (40/K_{CS}) A/LSB. $MFR\_OCPTDC\_1PS\_LEVEL = \frac{OCP\_TDC\_1PS \times K_{CS}}{40} + 4$ Where OCP_TDC_1PS is the OCP_TDC valley current threshold at 1-phase operation (in A), and K_{CS} is the Intelli-Phase current sense gain (in μA/A).

MFR_CS_OFFSET (D1h)

The MFR_CS_OFFSET command is used to set the CS sense offset to achieve thermal balance in multi-phase operation.

Command	MFR_CS_OFFSET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	MFR_CS_OFFSET4				

Bits	Bit Name	Description
15:5	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
4:0	MFR_CS_OFFSET4	Sets the offset voltage on CS4 in the current balance loop. This bit is in two's complement format. Bit[4] is the sign bit. The voltage list below shows the direct value and real-world value. 5'b 0 0000: 0 5'b 0 0001: +6.256mV 5'b 0 1111: +93.84mV 5'b 1 0000: -100.096mV 5'b 1 0001: -93.84mV 5'b 1 1111: -6.256mV

MFR_CUR_GAIN (D3h)

The MFR_CUR_GAIN command on Page 1 is used to set the gain for the Rail 2 OCP_PHASE limit calculation. Refer to the MFR_CUR_OFFSET (CAh) section for more information.

Command	MFR_CUR_GAIN															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_CS_GAIN									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:0	MFR_CS_GAIN	Sets the Rail 2 OCP_PHASE limit calculating gain. The gain can be calculated with: $CS\_GAIN = 8.2 \times K_{CS} \times R_{CS}$ Where K_{CS} is the multi-phase current sense gain (in μA/A), and R_{CS} is the value of the CS resistor (in kΩ).

MFR_VID_OFF (D5h)

The MFR_VID_OFF command on Page 1 is used to set the minimum operating V_{REF} for both rails. If the target VID (at either SVI, PVID, or PMBus™ mode) is lower than the value in MFR_VID_OFF, the associate rail transitions from VID down to 0V.

Command	MFR_VID_OFF															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	MFR_VID_OFF				

Bits	Bit Name	Description
15:5	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
4:0	MFR_VID_OFF	Sets the minimum operating V_{REF} for both rails. If the target VID (at either SVI, PVID, or PMBus™ mode) is lower than the value in MFR_VID_OFF, the associate rail transitions from VID down to 0V. 6.25mV/LSB.

MFR_OCP_ACTIONDELAY (D6h)

The MFR_OCP_ACTIONDELAY command on Page 1 is used to set the action delay time of OCP_TDC and OCP_SPIKE. For Rail 2 only.

Command	MFR_OCP_ACTIONDELAY															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	OCPTDC_ACTION_DELAY					OCPSPIKE_ACTION_ DELAY			

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:4	OCPTDC_ACTION_ DELAY	Sets the action delay time for OCP_TDC protection. Refer to the OCP_TDC section on page 25 for more information. 1μs/LSB.
3:0	OCPSPIKE_ACTION_ DELAY	Sets the action delay time for OCP_SPIKE protection. Refer to the OCP_SPIKE section on page 25 for more information. 1μs/LSB.

MFR_OVP_SET (D7h)

The MFR_OVP_SET command on Page 1 is used to set the Rail 2 output OVP mode and blanking time.

Command	MFR_OVP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X				OVP_BLANKING_TIME					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8	VFB+_WINDOW_EN	Enable bit for VFB+ window detection. When V_{FB} > V_{REF} + 20mV, the MP2853 holds the DC loop calibration, current balance loop, and frequency loop for a given time. If the VR is in APS mode, it exits APS and runs with full-phase CCM. 1'b0: VFB+ window is disabled 1'b1: VFB+ window is enabled
7:6	OVP_MODE	Set V_{OUT} OVP1 mode. There are four modes available. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
5:0	OVP_BLANKING_TIME	Sets the V_{OUT} OVP blanking time. An OVP fault occurs if the sensed V_{DIFF} exceeds the OVP threshold for an OVP blanking time. 100ns/LSB.

MFR_UVP_SET (D8h)

The MFR_UVP_SET command on Page 1 is used to set the Rail 2 V_{OUT} UVP mode and blanking time.

Command	MFR_UVP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X				UVP_BLANKING_TIME					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8	VFB-_WINDOW_EN	VFB- window enable bit. The VFB- window is a V_{FB} - 25mV threshold and can be used to expedite the load transient response in APM mode. 1'b0: VFB- window is disabled 1'b1: VFB- window is enabled
7:6	UVP_MODE	Sets the V_{OUT} UVP action mode. There are four modes available. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
5:0	UVP_BLANKING_TIME	Sets the V_{OUT} UVP blanking time. A UVP fault occurs if the sensed VDIFF falls below the UVP threshold for the UVP blanking time. 20µs/LSB.

MFR_VRHOT_SET (D9h)

The MFR_VRHOT_SET command sets the over-temperature warning limit. When the junction temperature monitored through VTEMP is higher than the OT warning limit, the OCP_L signal asserts.

Command	MFR_VRHOT_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X		VRHOT_LIMIT							

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8	VRHOT _EN	Over-temperature warning detection enable bit. 1'b0: disables over-temperature warning function 1'b1: enables over-temperature warning function
7:0	VRHOT_LIMIT	Sets the over-temperature warning limit. 1°C/LSB.

MFR_OCP_PHASE_LIMIT (DAh)

The MFR_OCP_PHASE_LIMIT command on Page 1 is used to set the valley current limit thresholds for each phase assigned to Rail 2. OCP_PHASE is a single-phase valley current limitation threshold. The MP2853 monitors the phase current cycle-by-cycle. When the phase current exceeds the OCP_PHASE threshold at the PWM off time, PWM remains low to discharge the inductor current below the set threshold. OCP_PHASE works with V_{OUT} UVP to protect the power stage from over-current. If the output current rises above the OCP_PHASE limit, output voltage drops because the PWM off time is extended.

Command	MFR_OCP_PHASE_LIMIT															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	OCP_PHASE_LIMIT						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	OCP_PHASE_LIMIT	Sets the OCP_PHASE valley current limit threshold. 1A/LSB.

MFR_ADP_CTRL (DBh)

The MFR_ADP_CTRL command is used to set APS-related behaviors.

Command	MFR_ADP_CTRL															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
10	FS INCREASE_ EXITAPS_R2_EN	Enables the Rail 2 frequency increasing condition to the APS exit. 1'b0: disables Rail 2 FS increase to APS exit 1'b1: enables Rail 2 FS increase to APS exit
9	1PHASE_OCP_ EXITAPS_EN	Enables OCP_PHASE exiting APS at 1-phase DCM/CCM only. 1'b0: disables the OCP per-phase signal triggering 1-phase DCM/CCM to full-phase operation 1'b1: enables the OCP per-phase signal triggering 1-phase DCM/CCM to full-phase operation.
8	VFB<VID-25mV_ EXITAPS_R2_EN	Enables Rail 2 V_{FB} < VID - 25mV to enter full-phase operation. 1'b0: disables Rail 2 V_{FB} < VID - 25mV to enter full-phase operation 1'b1: enables Rail 2 V_{FB} < VID - 25mV to enter full-phase operation
7:2	APS_DELAY_TIME_ CNT	Sets the phase shedding delay time. When the reported load current is consecutively below the APS threshold for APS_DELAY_TIME_CNT x IOUT_REPORT_CYCLE, the controller enters APS mode and sheds the phase count automatically according to the load current.
1	ENTER_APS_MODE_ SELECT	Sets the phase shedding action mode for Rail 2. 1'b0: sheds to the target phase number phase-by-phase with a programmable delay time 1'b1: sheds to the target phase number once with a 16μs delay
0	MFR_APS_EN	Enables Rail 2 auto-phase shedding mode. 1'b0: disables Rail 2 APS mode 1'b1: enables Rail 2 APS mode

MFR_EEPROM_WP (DCh)

The MFR_EEPROM_WP command is used to enable the EEPROM write protection.

Command	MFR_EEPROM_WP															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	EEPROM Write Protection							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
7:0	FAULT_RECORD_ EEPROM_EN	Enable bit for EEPROM write protection. 0x00: disables EEPROM to write 0x63: enables EEPROM to write

MFR_LL_LIMIT_SET (DDh)

The MFR_LL_LIMIT_SET command on Page 1 sets the load-line configuration for Rail 2.

Command	MFR_LL_LIMIT_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15:13	AC_DROOP	Sets the AC droop current value. In the MP2853, the initial droop current is defined with : $I_{DROOP\_INI} = \frac{5}{32} \times I_{CS\_SUM}$ Where I_{DROOP_INI} is the initial droop current, and I_{CS_SUM} is the current in CS_SUM (in μA). The MP2853 provides eight levels of AC droop. AC droop injection is ineffective automatically when the DC droop ≠ 0. Always connect a ≥200Ω resistor from V_{FB} to VDIFF to generate the AC droop. 3'b000: 0 3'b001: 0.6 x I_{DROOP_INI} 3'b010: 0.8 x I_{DROOP_INI} 3'b011: 1.0 x I_{DROOP_INI} 3'b100: 1.2 x I_{DROOP_INI} 3'b101: 1.4 x I_{DROOP_INI} 3'b110: 1.6 x I_{DROOP_INI} 3'b111: 1.8 x I_{DROOP_INI}
12	PMBUS_SVI_LL_SEL	Load line PMBus™ and SVI mode selection bit. 1'b0: SVI load-line mode. The load-line slope is determined by the SVI2 telemetry packet. 1'b1: PMBus™ load-line mode. The load-line slope is determined by the load-line level setting bit[11:9].
11:9	PMBUS_LL_LEVEL	Sets the PMBus™ load-line slope (DC droop) level. This bit is active when bit[12] = 1. The MP2853 provides eight levels of DC droop. 3'b000: 0 3'b001: 0.6 x I_{DROOP_INI} 3'b010: 0.8 x I_{DROOP_INI} 3'b011: 1.0 x I_{DROOP_INI} 3'b100: 1.2 x I_{DROOP_INI} 3'b101: 1.4 x I_{DROOP_INI} 3'b110: 1.6 x I_{DROOP_INI} 3'b111: 1.8 x I_{DROOP_INI}
8:3	250mV_LL_LIMIT_ OFFSET	Offset setting for 250mV droop calculation. 0.4mV/LSB.
2:0	TIME_INTERVAL_PER_ LOAD_LINE_STEP	Sets the time interval for each load-line step change. 1μs/LSB.
11:9	PMBUS_LL_LEVEL	Sets the PMBus™ load-line slope (DC droop) level. This bit is active when bit[12] = 1. The MP2853 provides eight levels of DC droop. 3'b000: 0 3'b001: 0.6 x I_{DROOP_INI} 3'b010: 0.8 x I_{DROOP_INI} 3'b011: 1.0 x I_{DROOP_INI} 3'b100: 1.2 x I_{DROOP_INI} 3'b101: 1.4 x I_{DROOP_INI} 3'b110: 1.6 x I_{DROOP_INI} 3'b111: 1.8 x I_{DROOP_INI}

MFR_SLOPE_SR_URS (DEh)

The MFR_SLOPE_SR_URS command on Page 1 is used to set the slope compensation slew rate for Rail 2 in USM. This slope compensation takes action before each PWM on pulse when the switching cycle is limited to 40µs. The slope capacitance is fixed with 3.9pF.

Command	MFR_SLOPE_SR_URS							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	CURRENT_SOURCE						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
6:0	CURRENT_SOURCE	Sets the current source value for slope voltage generation in USM. 0.25µA/LSB.

In general designs, set CURRENT_SOURCE = 2 to make the PWM on-pulse stable in USM.

MFR_OFFSET_SET (DFh)

The MFR_OFFSET_SET command on Page 1 is used to set the Rail 2 special offset and initial offset. Refer to the AMD Series VID Interface 2.0 (SVI2) specification Rev 1.07 section on page 41 to page 42 for more information.

Command	MFR_OFFSET_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	SPECIAL_OFFSET								INITIAL_OFFSET						

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
14:7	SPECIAL_OFFSET	Adds a positive offset over the initial VID to support higher output voltages. The initial VID can be determined by SVI communication, PMBus™ VID, and PVID. The special offset is used for CPU over-clocking. 6.25mV/LSB.
6:0	INITIAL_OFFSET	Adds a negative or positive offset over the initial VID to tune the output voltage. This bit is effective at SVI2 VID mode only. 6.25mV/LSB. This bit is in two's complement format. The voltage list below shows the direct value and real-world value. 7'b 000 0000: 0 7'b 000 0001: +6.25mV 7'b 011 1111: +393.75mV 7'b 100 0000: -400mV 7'b 100 0001: -393.75mV 7'b 111 1111: -6.25mV

MFR_OSR_SET (E0h)

The MFR_OSR_SET is used for overshoot reduction.

Command	MFR_OSR_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X								X						

Bits	Bit Name	Description
15:14, 6	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
13	OSR_EN	Enables the overshoot reduction function. This function can reduce the V_{OUT} overshoot at the load release. 1'b0: disables the overshoot reduction function 1'b1: enables the overshoot reduction function
[12:7]	OSR_FLAG_BLANK_TIME	Sets the OSR flag blanking time once OSR is ineffective after the OSR_FLAG filter time ends and OSR flat resets. 20ns/LSB.
[5:0]	OSR_FLAG_FILTER_TIME	Sets the minimum effective time of the OSR flag once $V_{FB} > V_{REF}$ + 25mV (VFB+ window) and OSR flag set. 5ns/LSB.

MFR_PWM_MIN_TIME (E1h)

The MFR_PWM_MIN_TIME command on Page 1 is used to set the PWM minimum on and off time.

Command	MFR_PWM_MIN_TIME															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	MIN_ON				MIN_OFF				

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:5	PWM_MIN_ON_TIME	Sets the PWM minimum on time for both rails. 5ns/LSB.
4:0	PWM_MIN_OFF_TIME	Sets the PWM minimum off time for both rails. 5ns/LSB.

MFR_SLOPE_SR_2PS (E2h)

The command MFR_SLOPE_SR_2PS on Page 1 is used to set the slope compensation slew rate at 2-phase CCM. For Rail 2 only.

Command	MFR_SLOPE_SR_2PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:6	CAP	Sets the capacitance for slope compensation at 2-phase CCM. The capacitance can be calculated with: $(16 - CAP) \times 1.85pF$ 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation at 2-phase CCM. The current source can be calculated with: $CURRENT\_SOURCE \times 0.25\mu A$ 0.25μA/LSB.

MFR_SLOPE_CNT_2PS (E3h)

The command MFR_SLOPE_CNT_2PS on Page 1 is used to set the slope voltage clamp time at 2-phase CCM.

Command	MFR_SLOPE_CNT_2PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	SLOPE_CNT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:0	SLOPE_CNT	Sets the slope clamp timer for 2-phase CCM. 5ns/LSB.

MFR_SLOPE_SR_1PS (E4h)

The MFR_SLOPE_SR_1PS command on Page 1 is used to set the slew rate of slope compensation for Rail 2 1-phase CCM.

Command	MFR_SLOPE_SR_1PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:6	CAP	Sets the capacitance for slope compensation at 1-phase CCM. The capacitance can be calculated with: $(16-CAP)\times 1.85pF$ 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation at 1-phase CCM. The current source can be calculated with: $CURRENT\_SOURCE\times 0.25\mu A$ 0.25μA/LSB.

MFR_SLOPE_CNT_1PS (E5h)

The MFR_SLOPE_CNT_1PS command on Page 1 is used to set the slope voltage clamp time at 1-phase CCM.

Command	MFR_SLOPE_CNT_1PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:0	SLOPE_CNT	Sets the slope clamp timer for 1-phase CCM. 5ns/LSB.

MFR_SLOPE_SR_0P5PS (E6h)

The MFR_SLOPE_SR_0P5PS command on Page 1 is used to set the slope compensation slew rate for Rail 2 1-phase DCM.

Command	MFR_SLOPE_SR_0P5PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
9:6	CAP	Sets the capacitance for slope compensation at 1-phase CCM. The capacitance can be calculated with: $(16-CAP)\times 1.85pF$ 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation at 1-phase CCM. The current source can be calculated with: $CURRENT\_SOURCE\times 0.25\mu A$ 0.25μA/LSB.

MFR_SLOPE_CNT_0P5PS (E7h)

The MFR_SLOPE_CNT_0P5PS command on Page 1 is used to set the slope voltage clamp time at 1-phase DCM.

Command	MFR_SLOPE_CNT_0P5PS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	SLOPE_CNT					

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
5:0	SLOPE_CNT	Sets the slope clamp timer for 1-phase DCM. 80ns/LSB.

MFR_LAST_FAULTS1 (EDh)

The MFR_LAST_FAULTS1 command returns the fault type of the previous power cycle. Enable the fault type to be recorded into the EEPROM by setting MFR_PRT_CONFIG (DCh) bit[8], bit[5], and bit[4] to 1. The fault type is stored into the EEPROM automatically when a fault occurs. The fault type is restored into MFR_LAST_FAULTS1 (EDh), MFR_LAST_FAULTS2 (EEh), and MFR_LAST_FAULTS3 (EFh) at the power-on EEPROM copy process.

Command	MFR_LAST_FAULTS1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
12	VDIFF_SC_R2	Rail 2 VDIFF short to GND fault indication bit. 1'b0: no VDIFF short to GND fault 1'b1: VDIFF short to GND fault has occurred on Rail 2
11	OCP_TDC_R2	Rail 2 OCP_TDC fault indication bit. 1'b0: no OCP_TDC fault on Rail 2 1'b1: OCP_TDC fault has occurred on Rail 2
10	OCP_SPIKE_R2	Rail 2 OCP_SPIKE fault indication bit. 1'b0: no OCP_SPIKE fault on Rail 2 1'b1: OCP_SPIKE fault has occurred on Rail 2
9	VOUT_UV_R2	Rail 2 V_{OUT} UV fault indication bit. This bit is set when the Rail 2 V_{OUT} UVP blanking time ends and V_{OUT} UV remains. 1'b0: no V_{OUT} UV fault on Rail 2 1'b1: V_{OUT} UV fault has occurred on Rail 2
8	VOUT_OV_R2	Rail 2 V_{OUT} OV fault indication bit. This bit is set when the Rail 2 V_{OUT} OVP blanking time ends and V_{OUT} OV remains. 1'b0: no V_{OUT} OV fault on Rail 2 1'b1: V_{OUT} OV fault has occurred on Rail 2
7	VDIFF_SC_R1	Rail 1 VDIFF short to GND fault indication bit. 1'b0: no VDIFF shorting to GND fault on Rail 1 1'b1: VDIFF shorting to GND fault has occurred on Rail 1
6	OCP_TDC_R1	Rail 1 OCP_TDC fault indication bit. 1'b0: no OCP_TDC fault on Rail 1 1'b1: OCP_TDC fault has occurred on Rail 1
5	OCP_SPIKE_R1	Rail 1 OCP_SPIKE fault indication bit. 1'b0: no OCP_SPIKE fault on Rail 1 1'b1: OCP_SPIKE fault has occurred on Rail 1
4	VOUT_UV_R1	Rail 1 V_{OUT} UV fault indication bit. This bit is set when the Rail 1 V_{OUT} UVP blanking time ends and V_{OUT} UV still remains. 1'b0: no V_{OUT} UV fault on Rail 1 1'b1: V_{OUT} UV fault has occurred on Rail 1
3	VOUT_OV_R1	Rail 1 V_{OUT} OV fault indication bit. This bit is set when the Rail 1 V_{OUT} OVP blanking time ends and V_{OUT} OV still exists. 1'b0: no V_{OUT} OV fault on Rail 1 1'b1: V_{OUT} OV fault has occurred on Rail 1
2	OT_FLT	Over-temperature fault indication bit. 1'b0: no OT fault has occurred 1'b1: OT fault has occurred
1	VIN_OV	V_{IN} OV fault indication bit. 1'b0: no V_{IN} OV fault has occurred 1'b1: V_{IN} OV fault has occurred
0	VIN_UV	V_{IN} UV fault indication bit. 1'b0: no V_{IN} UV fault has occurred 1'b1: V_{IN} UV fault has occurred

MFR_LAST_FAULTS2 (EEh)

The MFR_LAST_FAULTS2 command returns the Intelli-Phase fault type of the previous power cycle.

Command	MFR_LAST_FAULTS2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	PHASE1_FAULT_TYPE				PHASE2_FAULT_TYPE				PHASE3_FAULT_TYPE			

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
11:8	PHASE1_FAULT_TYPE	Intelli-Phase fault type indication of phase 1. 4’b0000: no fault 4’b0001: VIN-SW short 4’b0010: current limit protection 4’b0100: over-temperature protection 4’b1000: SW-PGND short protection
7:4	PHASE2_FAULT_TYPE	Intelli-Phase fault type indication of phase 2. 4’b0000: no fault 4’b0001: VIN-SW short 4’b0010: current limit protection 4’b0100: over-temperature protection 4’b1000: SW-PGND short protection
3:0	PHASE3_FAULT_TYPE	Intelli-Phase fault type indication of phase 3. 4’b0000: no fault 4’b0001: VIN-SW short 4’b0010: current limit protection 4’b0100: over-temperature protection 4’b1000: SW-PGND short protection

MFR_LAST_FAULTS3 (EFh)

The MFR_LAST_FAULTS3 command records last the fault type of the Intelli-Phase and fault status of CS. This command is only effective when the Intelli-Phase supports this function. Refer to the Intelli-Phase datasheet for more information.

Command	MFR_LAST_FAULTS3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X						PHASE4_FAULT_TYPE				PHASE5_FAULT_TYPE			
_+RBits	Bit Name				Description											
15:13	RESERVED				Unused. X indicates that writes are ignored and always read as 0.											
12	CS5_FAULT_FLAG				CS5 fault indicator. 1’b0: no CS fault 1’b1: CS fault has occurred											
11	CS4_FAULT_FLAG				CS4 fault indicator. 1’b0: no CS fault 1’b1: CS fault has occurred											

Bits	Bit Name	Description
10	CS3_FAULT_FLAG	CS3 fault indicator. 1'b0: no CS fault 1'b1: CS fault has occurred
9	CS2_FAULT_FLAG	CS2 fault indicator. 1'b0: no CS fault 1'b1: CS fault has occurred
8	CS1_FAULT_FLAG	CS1 fault indicator. 1'b0: no CS fault 1'b1: CS fault has occurred
7:4	PHASE4_FAULT_TYPE	Intelli-Phase fault type indication of phase 4. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
3:0	PHASE5_FAULT_TYPE	Intelli-Phase fault type indication of phase 5. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection

CLEAR_EEPROM_FAULTS (FFh)

The CLEAR_EEPROM_FAULTS command is used to clear the EEPROM CRC fault that occurs during the copy EEPROM process. This is a write only command. There is no data byte for this command.

PAGE 29 REGISTER MAP

MFR_STORE_FAULTS1 (EDh)

The MFR_STORE_FAULTS1 command on Page 29 stores the fault type in the EEPROM. To clear the fault bits, write 0x0000 to this command and wait 5ms.

Command	MFR_STORE_FAULTS1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
12	VDIFF_SC_R2	Rail 2 VDIFF short to GND fault indication bit. 1'b0: no VDIFF short to GND fault 1'b1: VDIFF short to GND fault has occurred on Rail 2
11	OCP_TDC_R2	Rail 2 OCP_TDC fault indication bit. 1'b0: no OCP_TDC fault on Rail 2 1'b1: OCP_TDC fault has occurred on Rail 2
10	OCP_SPIKE_R2	Rail 2 OCP_SPIKE fault indication bit. 1'b0: no OCP_SPIKE fault on Rail 2 1'b1: OCP_SPIKE fault has occurred on Rail 2
9	VOUT_UV_R2	Rail 2 V_{OUT} UV fault indication bit. This bit is set when the Rail 2 V_{OUT} UVP blanking time ends and V_{OUT} UV remains. 1'b0: no V_{OUT} UV fault on Rail 2 1'b1: V_{OUT} UV fault has occurred on Rail 2
8	VOUT_OV_R2	Rail 2 V_{OUT} OV fault indication bit. This bit is set when the Rail 2 V_{OUT} OVP blanking time ends and V_{OUT} OV remains. 1'b0: no V_{OUT} OV fault on Rail 2 1'b1: V_{OUT} OV fault has occurred on Rail 2
7	VDIFF_SC_R1	Rail 1 VDIFF short to GND fault indication bit. 1'b0: no VDIFF short to GND fault on Rail 1 1'b1: VDIFF short to GND fault has occurred on Rail 1
6	OCP_TDC_R1	Rail 1 OCP_TDC fault indication bit. 1'b0: no OCP_TDC fault on Rail 1 1'b1: OCP_TDC fault has occurred on Rail 1
5	OCP_SPIKE_R1	Rail 1 OCP_SPIKE fault indication bit. 1'b0: no OCP_SPIKE fault on Rail1 1'b1: OCP_SPIKE fault has occurred on Rail 1
4	VOUT_UV_R1	Rail 1 V_{OUT} UV fault indication bit. This bit is set when the Rail 1 V_{OUT} UVP blanking time ends and V_{OUT} UV remains. 1'b0: no V_{OUT} UV fault on Rail 1 1'b1: V_{OUT} UV fault has occurred on Rail 1
3	VOUT_OV_R1	Rail 1 V_{OUT} OV fault indication bit. This bit is set when the Rail 1 V_{OUT} OVP blanking time ends and the V_{OUT} OV remains. 1'b0: no V_{OUT} OV fault on Rail 1 1'b1: V_{OUT} OV fault has occurred on Rail 1
2	OT_FLT	Over-temperature fault indication bit. 1'b0: no OT fault has occurred 1'b1: OT fault has occurred

Bits	Bit Name	Description
1	VIN_OV	V_{IN} OV fault indication bit. 1'b0: no V_{IN} OV fault has occurred 1'b1: V_{IN} OV fault has occurred
0	VIN_UV	V_{IN} UV fault indication bit. 1'b0: no V_{IN} UV fault has occurred 1'b1: V_{IN} UV fault has occurred

MFR_STORE_FAULTS2 (EEh)

The MFR_STORE_FAULTS2 command on Page 29 stores the fault type in the EEPROM. To clear the fault bits, write 0x0000 to this command and wait 5ms.

Command	MFR_STORE_FAULTS2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	X	X	X	X	PHASE1_FAULT_TYPE				PHASE2_FAULT_TYPE				PHASE3_FAULT_TYPE			

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
11:8	PHASE1_FAULT_TYPE	Intelli-Phase fault type indication of phase 1. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
7:4	PHASE2_FAULT_TYPE	Intelli-Phase fault type indication of phase 2. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
3:0	PHASE3_FAULT_TYPE	Intelli-Phase fault type indication of phase 3. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection

MFR_STORE_FAULTS3 (EFh)

The MFR_STORE_FAULTS3 command on Page 29 stores the fault type in the EEPROM. To clear the fault bits, write 0x0000 to this command and wait 5ms.

Command	MFR_STORE_FAULTS3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	X	X	X						PHASE4_FAULT_TYPE				PHASE5_FAULT_TYPE			

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
12	CS5_FAULT_FLAG	CS5 fault indicator. 1'b0: no CS fault 1'b1: CS fault has occurred
11	CS4_FAULT_FLAG	CS4 fault indicator. 1'b0: no CS fault 1'b1: CS fault has occurred
10	CS3_FAULT_FLAG	CS3 fault indicator. 1'b0: no CS fault 1'b1: CS fault has occurred
9	CS2_FAULT_FLAG	CS2 fault indicator. 1'b0: no CS fault 1'b1: CS fault has occurred
8	CS1_FAULT_FLAG	CS1 fault indicator. 1'b0: no CS fault 1'b1: CS fault has occurred
7:4	PHASE4_FAULT_TYPE	Intelli-Phase fault type indication of phase 4. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
3:0	PHASE5_FAULT_TYPE	Intelli-Phase fault type indication of phase 5. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection

PVID_VID1 (F0h)

The PVID_VID1 command on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode.

Command	PVID_VID1															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID_VID1_R1								PVID_VID1_R2							

Bits	Bit Name	Description
15:8	PVID_VID1_R1	Sets the Rail 1 PVID voltage when PVID1/PVID2/PVID3 = 3'b000. 6.25mV/LSB.
7:0	PVID_VID1_R2	Sets the Rail 2 PVID voltage when PVID1/PVID2/PVID3 = 3'b000. 6.25mV/LSB.

PVID_VID2 (F1h)

The PVID_VID2 command on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode.

Command	PVID_VID2															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID_VID2_R1								PVID_VID2_R2							

Bits	Bit Name	Description
15:8	PVID_VID2_R1	Sets the Rail 1 PVID voltage when PVID1/PVID2/PVID3 = 3’b001. 6.25mV/LSB.
7:0	PVID_VID2_R2	Sets the Rail 2 PVID voltage when PVID1/PVID2/PVID3 = 3’b001. 6.25mV/LSB.

PVID_VID3 (F2h)

The PVID_VID3 command on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode.

Command	PVID_VID3															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID_VID3_R1								PVID_VID3_R2							

Bits	Bit Name	Description
15:8	PVID_VID3_R1	Sets the Rail 1 PVID voltage when PVID1/PVID2/PVID3 = 3’b010. 6.25mV/LSB.
7:0	PVID_VID3_R2	Sets the Rail 2 PVID voltage when PVID1/PVID2/PVID3 = 3’b010. 6.25mV/LSB.

PVID_VID4 (F3h)

The PVID_VID4 command on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode.

Command	PVID_VID4															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID_VID4_R1								PVID_VID4_R2							

Bits	Bit Name	Description
15:8	PVID_VID4_R1	Sets the Rail 1 PVID voltage when PVID1/PVID2/PVID3 = 3’b011. 6.25mV/LSB.
7:0	PVID_VID4_R2	Sets the Rail 2 PVID voltage when PVID1/PVID2/PVID3 = 3’b011. 6.25mV/LSB.

PVID_VID5 (F4h)

The PVID_VID5 command on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode.

Command	PVID_VID5															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID_VID5_R1								PVID_VID5_R2							

Bits	Bit Name	Description
15:8	PVID_VID5_R1	Sets the Rail 1 PVID voltage when PVID1/PVID2/PVID3 = 3’b100. 6.25mV/LSB.
7:0	PVID_VID5_R2	Sets the Rail 2 PVID voltage when PVID1/PVID2/PVID3 = 3’b100. 6.25mV/LSB.

PVID_VID6 (F5h)

The PVID_VID6 command on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode.

Command	PVID_VID6															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID_VID6_R1								PVID_VID6_R2							

Bits	Bit Name	Description
15:8	PVID_VID6_R1	Sets the Rail 1 PVID voltage when PVID1/PVID2/PVID3 = 3’b101. 6.25mV/LSB.
7:0	PVID_VID6_R2	Sets the Rail 2 PVID voltage when PVID1/PVID2/PVID3 = 3’b101. 6.25mV/LSB.

PVID_VID7 (F6h)

The PVID_VID7 command on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode.

Command	PVID_VID7															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID_VID7_R1								PVID_VID7_R2							

Bits	Bit Name	Description
15:8	PVID_VID7_R1	Sets the Rail 1 PVID voltage when PVID1/PVID2/PVID3 = 3’b110. 6.25mV/LSB.
7:0	PVID_VID7_R2	Sets the Rail 2 PVID voltage when PVID1/PVID2/PVID3 = 3’b110. 6.25mV/LSB.

PVID_VID8 (F7h)

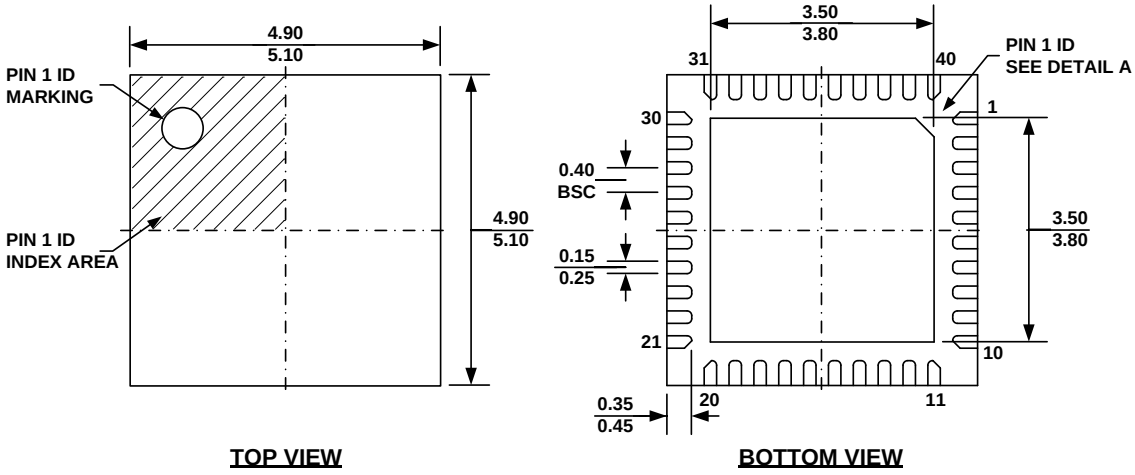
The PVID_VID8 command on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode.

Command	PVID_VID8															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID_VID8_R1								PVID_VID8_R2							

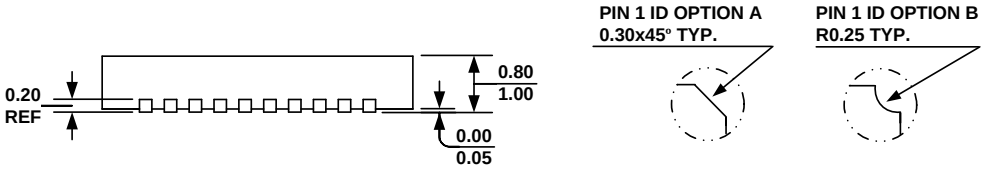
Bits	Bit Name	Description
15:8	PVID_VID8_R1	Sets the Rail 1 PVID voltage when PVID1/PVID2/PVID3 = 3’b111. 6.25mV/LSB.
7:0	PVID_VID8_R2	Sets the Rail 2 PVID voltage when PVID1/PVID2/PVID3 = 3’b111. 6.25mV/LSB.

PACKAGE INFORMATION

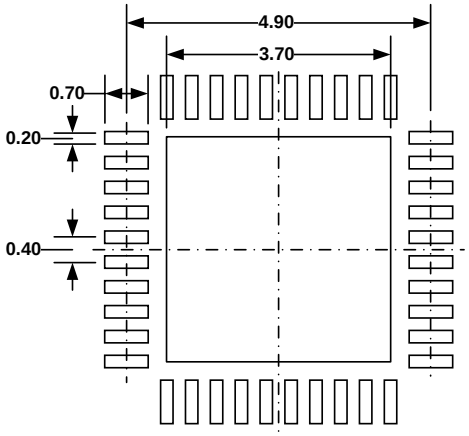
QFN-40 (5mmx5mm)



TOP VIEW **BOTTOM VIEW**



SIDE VIEW **DETAIL A**



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHE-1.
5) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	08/01/2017	Initial Release	-
1.1	12/17/2021	Minor formatting updates.	1
		Changed the oscillator frequency limit and added the 25°C condition.	5
		Changed the EC test condition from EN = 1V to EN = 3.3V.	5–8