DESCRIPTION
The MP28257 is a fully-integrated, synchronous, step-down, switch-mode converter with a programmable frequency. It offers a very compact solution that can provide up to 4A of continuous output current over a wide input supply range with excellent load and line regulation, and can operate at high efficiency over a wide output current load range.

Constant-on-time control mode provides fast transient response and eases loop stabilization.

Protections include short-circuit protection, over-current protection, over-voltage protection, under-voltage protection, and thermal shutdown.

The MP28257 requires a minimal number of readily-available standard external components.

The device is available in a space saving 2mmx3mm QFN12 package that complies with ROHS.

FEATURES
- Wide 4.2V-to-20V Operating Input Range
- 4A Continuous Output Current
- Internal 120mΩ High-Side, 50mΩ Low-Side Power MOSFETs
- Stable with Ceramic Output Capacitors
- Proprietary Switching Loss-Reduction Technology
- Power-Good Indicator
- Soft Startup/Shutdown
- Programmable Switching Frequency
- SCP, OCP, OVP, UVP Protection and Thermal Shutdown
- Output Adjustable from 0.815V to 13V
- Available in a 2mmx3mm QFN12 Package

APPLICATIONS
- Networking Systems
- Distributed Power Systems

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are Registered Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION

![Typical Application Diagram](image-url)
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>OCP Protection</th>
<th>Package</th>
<th>Top Marking</th>
<th>Free Air Temperature (TA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP28257DD*</td>
<td>Latch-off Mode</td>
<td>QFN12 (2x3mm)</td>
<td>ABF</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP28257DD–Z).
  For RoHS Compliant Packaging, add suffix –LF (e.g. MP28257DD–LF–Z)

PACKAGE REFERENCE

<table>
<thead>
<tr>
<th>GND</th>
<th>SW</th>
<th>BST</th>
<th>VCC</th>
<th>EN</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>SW</td>
<td>IN</td>
<td>FREQ</td>
<td>FB</td>
<td>PG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage \( V_{IN} \) ........................................ 22V

\( V_{SW} \) ........................................ -0.3V to \( (V_{IN} + 0.3V) \)

\( V_{BST} \) ........................................ \( V_{SW} + 6V \)

All other pins ........................................ -0.3V to +6V

Continuous Power Dissipation \( (T_A = 25°C) \) (2)

QFN12 (2x3mm) ........................................ 1.8W

Junction Temperature .............................. 150°C

Lead Temperature ........................................ 260°C

Storage Temperature..................................... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage \( V_{IN} \) ........................................ 4.2V to 20V

Output Voltage \( V_{OUT} \) ................................. 0.815V to 13V

Maximum Junction Temp. \( (T_J) \) ..................... 125°C

Thermal Resistance (4) \( \theta_{JA} \) \( \theta_{JC} \)

QFN12 (2x3mm) ........................................ 70 ....... 15 ... °C/W

Notes:
1) Exceeding these ratings may damage the device.

2) The maximum allowable power dissipation is a function of the
   maximum junction temperature \( T_J \) (MAX), the junction-to-
   ambient thermal resistance \( \theta_{JA} \), and the ambient temperature
   \( T_A \). The maximum allowable continuous power dissipation at
   any ambient temperature is calculated by \( P_D \) (MAX) = \( (T_J \)
   (MAX)-\( T_A \))\( \theta_{JA} \). Exceeding the maximum allowable power
   dissipation will cause excessive die temperature, and the
   regulator will go into thermal shutdown. Internal thermal
   shutdown circuitry protects the device from permanent
   damage.

3) The device is not guaranteed to function outside of its
   operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

NOT RECOMMENDED FOR NEW DESIGNS
REFER TO MP2384
## ELECTRICAL CHARACTERISTICS

\( V_{IN} = 12V, T_A = 25°C, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current (shutdown)</td>
<td>( I_{IN} )</td>
<td>( V_{EN} = 0V )</td>
<td>1</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Supply current (quiescent)</td>
<td>( I_{IN} )</td>
<td>( V_{EN} = 2V, V_{FB} = 0.9V )</td>
<td>360</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>HS switch-on resistance (5)</td>
<td>( H_{SRDS-ON} )</td>
<td></td>
<td>120</td>
<td></td>
<td></td>
<td>m( \Omega )</td>
</tr>
<tr>
<td>LS Switch-on resistance (5)</td>
<td>( L_{SRDS-ON} )</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>m( \Omega )</td>
</tr>
<tr>
<td>Switch leakage</td>
<td>( S_{W_{UKG}} )</td>
<td>( V_{EN} = 0V, V_{SW} = 0V )</td>
<td>0</td>
<td>10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Current limit</td>
<td>( I_{LIMIT} )</td>
<td>After Soft-Start Time-out</td>
<td>5.5</td>
<td>7</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>One-shot on time</td>
<td>( t_{ON} )</td>
<td>( R_7 = 300k\Omega, V_{OUT} = 1.2V )</td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Minimum off time</td>
<td>( t_{OFF} )</td>
<td></td>
<td>130</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Fold-back off time (5)</td>
<td>( t_{FB} )</td>
<td>( I_{LIMIT} = 1 )</td>
<td>4.5</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td>OCP hold-off time (5)</td>
<td>( t_{OC} )</td>
<td>( I_{LIMIT} = 1 )</td>
<td>50</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Feedback voltage</td>
<td>( V_{FB} )</td>
<td>( T_A = 25°C )</td>
<td>807</td>
<td>815</td>
<td>823</td>
<td>mV</td>
</tr>
<tr>
<td>Feedback voltage</td>
<td>( V_{FB} )</td>
<td>( T_A = -40°C to 85°C )</td>
<td>803</td>
<td></td>
<td>827</td>
<td>mV</td>
</tr>
<tr>
<td>Feedback current</td>
<td>( I_{FB} )</td>
<td>( V_{FB} = 800mV )</td>
<td>10</td>
<td>50</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Soft start time</td>
<td>( t_{SS} )</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>EN rising threshold</td>
<td>( E_{N_{RISING}} )</td>
<td></td>
<td>1.05</td>
<td>1.35</td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td>EN threshold hysteresis</td>
<td>( E_{N_{HYSTERESIS}} )</td>
<td></td>
<td>500</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>EN input current</td>
<td>( I_{EN} )</td>
<td>( V_{EN} = 2V )</td>
<td>2</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>EN Input Current</td>
<td>( I_{EN} )</td>
<td>( V_{EN} = 0V )</td>
<td>0</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Power-good rising threshold</td>
<td>( P_{G_{RISING}} )</td>
<td>Power-good</td>
<td>90</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Power-good falling threshold</td>
<td>( P_{G_{FALLING}} )</td>
<td>Fault condition</td>
<td>85</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Power-good delay</td>
<td>( P_{GTd} )</td>
<td></td>
<td>500</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Power-good sink current</td>
<td>( I_{PG} )</td>
<td>( PG = 0.4V )</td>
<td>4</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Power-good Leakage Current</td>
<td>( I_{PG_{LEAK}} )</td>
<td>( V_{PG} = 3.3V )</td>
<td>10</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>VIN under-voltage lockout threshold rising</td>
<td>( I_{NUV_{Vth}} )</td>
<td></td>
<td>3.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIN under-voltage lockout threshold hysteresis</td>
<td>( I_{NUV_{HYSTERESIS}} )</td>
<td></td>
<td>300</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Thermal shutdown (5)</td>
<td>( T_{SD} )</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal shutdown hysteresis (5)</td>
<td>( T_{SD-HYSTERESIS} )</td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:**

5) Guaranteed by design.
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>QFN12 (2x3mm) Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>IN</td>
<td>Supply Voltage. The MP28257 operates from a 4.2V to 20V input rail. C1 decouples the input rail. Use wide PCB traces and multiple vias to make the connection.</td>
</tr>
<tr>
<td>1, 11, 12</td>
<td>GND</td>
<td>System Ground. Reference ground for the regulated output voltage. These pins require special consideration during PCB layout.</td>
</tr>
<tr>
<td>2, 10, Exposed Pad</td>
<td>SW</td>
<td>Switch Output. Connect with wide PCB traces.</td>
</tr>
<tr>
<td>3</td>
<td>BST</td>
<td>Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.</td>
</tr>
<tr>
<td>4</td>
<td>VCC</td>
<td>Internal Bias Supply. Decouple with a 1µF ceramic capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>5</td>
<td>EN</td>
<td>EN = 1 to enable the MP28257. For automatic start-up, connect EN pin to VIN with a pull-up resistor.</td>
</tr>
<tr>
<td>7</td>
<td>FB</td>
<td>Feedback. Sets the output voltage when connected to the tap of an external resistor divider, connected between output and GND.</td>
</tr>
<tr>
<td>8</td>
<td>FREQ</td>
<td>Frequency. Set during CCM operation. Connect a resistor R7 to IN to set the switching frequency. Decouple with a 1nF capacitor.</td>
</tr>
<tr>
<td>6</td>
<td>PG</td>
<td>Power-Good Output. The output of this pin is an open drain that goes high if the output voltage is higher than 90% of the nominal voltage. There is a 0.5ms delay between when the feedback exceeds 90% to when the PG pin goes high.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $L = 2\mu$H, $T_A = 25^\circ C$, unless otherwise noted.

### Efficiency vs. Load Current
- $V_{IN} = 5V$
- $V_{IN} = 12V$
- $V_{IN} = 15V$

![Efficiency vs. Load Current](image)

### Line Regulation
- $I_{OUT} = 4A$
- $V_{IN}$

![Line Regulation](image)

### Load Regulation
- $V_{IN} = 16V$
- $V_{IN} = 12V$

![Load Regulation](image)

### Case Temp Rise
- $T_A = 27.4^\circ C$
- $V_{IN} = 21V$
- $V_{IN} = 12V$

![Case Temp Rise](image)

### Frequency vs. Temperature
- $R_{SW} = 274\Omega$
- $I_{OUT} = 4A$

![Frequency vs. Temperature](image)

### Frequency vs. Input Voltage
- $R_{SW} = 274\Omega$
- $I_{OUT} = 4A$

![Frequency vs. Input Voltage](image)
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $L = 2\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

**Input/Output Voltage Ripple**

- $I_{OUT} = 4A$
- $V_{IN}/AC$ : 100mV/div.
- $V_{OUT}/AC$ : 10mV/div.
- $V_{OUT}$ : 1V/div.
- $V_{SW}$ : 5V/div.
- $I_{L}$ : 5A/div.

**Start up through VIN**

- $I_{OUT} = 0A$
- $V_{IN}$ : 10V/div.
- $V_{SW}$ : 10V/div.
- $I_{L}$ : 1A/div.
- $V_{OUT}$ : 1V/div.

**Shutdown through VIN**

- $I_{OUT} = 0A$
- $V_{IN}$ : 10V/div.
- $V_{SW}$ : 2V/div.
- $I_{L}$ : 1A/div.
- $V_{OUT}$ : 1V/div.

**Start up through EN**

- $I_{OUT} = 4A$
- $V_{IN}$ : 5V/div.
- $V_{SW}$ : 5V/div.
- $I_{L}$ : 5A/div.
- $V_{OUT}$ : 1V/div.

**Shutdown through EN**

- $I_{OUT} = 0A$
- $V_{IN}$ : 5V/div.
- $V_{SW}$ : 10V/div.
- $I_{L}$ : 5A/div.
- $V_{OUT}$ : 1V/div.

NOT RECOMMENDED FOR NEW DESIGNS

REFER TO MP2384
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $L = 2\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

**Transient**

- $I_{OUT} = 0.4A \sim 4A @ 2.5A/\mu s$
- $F_{SW}=500kHz$, $C_{OUT}=2\times22\mu F$

**NOT RECOMMENDED FOR NEW DESIGNS**

REFER TO MP2384
Figure 1: Functional Block Diagram
OPERATION

PWM Operation

The MP28257 is a fully-integrated, synchronous, rectified, step-down switch converter. The device uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON whenever the feedback voltage ($V_{FB}$) is lower than the reference voltage ($V_{REF}$)—a low $V_{FB}$ indicates insufficient output voltage. The input voltage and the frequency-set resistor determine the ON period as follows:

$$t_{ON}(\text{ns}) = \frac{9.3 \times R_s (\text{k}\Omega)}{\frac{V_{IN}(\text{V})}{0.4} - 40}\text{ns} \quad (1)$$

After the ON period elapses, the HS-FET enters the OFF state. By cycling the HS-FET between the ON and OFF states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its OFF state to minimize the conduction loss.

Shoot-through occurs when there is both the HS-FET and LS-FET are turned on at the same time, causing a dead short between input and GND. Shoot-through dramatically reduces efficiency, and the MP28257 avoids this by internally generating a dead-time (DT) between when the HS-FET is off and the LS-FET is on, and when the LS-FET is off and the HS-FET is on. The device enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

Heavy-Load Operation

During heavy-load operation—when the output current is high—the MP28257 enters continuous-conduction mode (CCM) where the HS-FET and LS-FET repeat the on/off operation described for PWM operation, the inductor current never goes to zero, and the switching frequency ($f_{SW}$) is fairly constant. Figure 2 shows the timing diagram during this operation.

Light-Load Operation

During light-load operation—when the output current is low—the MP28257 automatically reduces the switching frequency to maintain high efficiency, and the inductor current drops near zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high Z). The current modulator controls the LS-FET and limits the inductor current to around -1mA as shown in Figure 3. Hence, the output capacitors discharge slowly to GND through LS-FET, $R_1$, and $R_2$. This operation greatly improves device efficiency when the output current is low.

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (2)$$

The device reverts to PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.
The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. The bootstrap capacitor is charges from VCC through N1 (Figure 4): N1 turns on when the LS-FET turns on, and turns off when the LS-FET turns off.

Switching Frequency
The MP28257 uses COT control because there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R7. The duty ratio is kept as \( V_{OUT}/V_{IN} \), and the switching frequency is fairly constant over the input voltage range. The switching frequency can be determined with the following equation:

\[
T_{SW} (kHz) = \frac{10^n}{9.3 \times R_7 (k\Omega) \times \frac{V_{IN}(V)}{V_{OUT}(V)} - 0.4 + t_{DELAY} (ns)}
\]

Where \( T_{DELAY} \) is the comparator delay, and equals approximately 40ns.

The MP28257 is optimized to operate at a high switching frequency for high efficiency. The high switching frequency makes it possible to use small-sized LC filter components to save system PCB space.

Jitter and FB Ramp Slope
Jitter occurs in both PWM and skip modes when noise in the \( V_{FB} \) ripple propagates a delay to the HS-FET driver, as shown in Figures 5 and 6.

Ramp with Large ESR Cap
In the case of POSCAP or other types of capacitor with larger ESR is applied as output capacitor. The ESR ripple dominates the output ripple, and the slope on the FB is quite ESR related. Figure 7 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. Turn to application information section for design steps with large ESR caps.
To realize the stability when no external ramp is used, usually the ESR value should be chosen as follow:

\[ R_{ESR} \geq \frac{T_{SW} + T_{ON}}{0.7 \times \pi \times C_{OUT}} \] (4)

\( T_{SW} \) is the switching period.

**Ramp with small ESR Cap**

When the output capacitors are ceramic ones, the ESR ripple is not high enough to stabilize the system, and external ramp compensation is needed. Skip to application information section for design steps with small ESR caps.

\[ \frac{1}{2 \pi F_{SW} \times C_{4}} < \frac{1}{5} \left( \frac{R_{4} \times R_{2}}{R_{1} + R_{2}} + R_{9} \right) \] (5)

where:

\[ I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \] (6)

And the \( V_{RAMP} \) on the \( V_{FB} \) can then be estimated as:

\[ V_{RAMP} = \frac{V_{IN} - V_{OUT}}{R_{4} \times C_{4}} \times T_{ON} \times \frac{R_{4} / R_{9}}{R_{4} / R_{9} + R_{9}} \] (7)

The downward slope of the \( V_{FB} \) ripple then follows:

\[ V_{SLOPE1} = -\frac{V_{RAMP}}{T_{OFF}} = -\frac{V_{OUT}}{R_{4} \times C_{4}} \] (8)

As can be seen from equation 8, if there is instability in PWM mode, we can reduce either \( R_{4} \) or \( C_{4} \). If \( C_{4} \) can not be reduced further due to limitation from equation 5, then we can only reduce \( R_{4} \). For a stable PWM operation, the \( V_{SLOPE1} \) should be design follow equation 9.

\[ -V_{SLOPE1} \geq \frac{T_{SW} + T_{ON}}{2 \times L \times C_{OUT}} \times V_{OUT} + \frac{I_{O} \times 10^{-3}}{T_{SW} - T_{ON}} \] (9)

\( I_{O} \) is the load current.

In skip mode, the downward slope of the \( V_{FB} \) ripple is the same whether the external ramp is used or not. Figure 9 shows the simplified circuit of the skip mode when both the HS-FET and LS-FET are off.

**Figure 8—Simplified Circuit in PWM Mode with External Ramp Compensation**

Figure 8 shows a simplified external ramp compensation (\( R_{4} \) and \( C_{4} \)) for PWM mode, with HS-FET off. Chose \( R_{1}, R_{2}, R_{9} \) and \( C_{4} \) of the external ramp to meet the following condition:

\[ \frac{1}{\pi F_{SW} \times C_{4}} < \frac{1}{5} \left( \frac{R_{4} \times R_{2}}{R_{1} + R_{2}} + R_{9} \right) \] (5)

**Figure 9—Simplified Circuit in skip Mode**

The downward slope of the \( V_{FB} \) ripple in skip mode can be determined as follow:

\[ V_{SLOPE2} = \frac{-V_{REF}}{\left( R_{O} \right) \times C_{OUT}} \] (10)

where \( R_{O} \) is the equivalent load resistor.

As described in Figure 6, \( V_{SLOPE2} \) in the skip mode is lower than that is in the PWM mode, so it is reasonable that the jitter in the skip mode is larger. If one wants a system with less jitter during light load condition, the values of the \( V_{FB} \) resistors should not be too big, however, that will decrease the light load efficiency.

When using a large-ESR capacitor on, the output, add a ceramic capacitor with a value of 10\( \mu \)F or less to in parallel to minimize the effect of ESL.

**Soft Start/Stop**

MP28257 employs a soft-start/stop (SS) mechanism to ensure a smooth output during power up and power shut-down. When the EN pin goes high, the internal SS voltage slowly ramps up. The output voltage smoothly ramps up with the SS voltage. Once SS voltage rises
above the VREF, it continues to ramp up while the PWM comparator only compares the VREF and the FB voltage. At this point, the soft-start finishes and it enters steady state operation. The SS time is set about 1ms internally.

When the EN pin goes low, an internal current source discharges the internal SS voltage. Once the SS voltage falls below the VREF, the PWM comparator will only compare the VREF to the SS voltage. The output voltage then decreases smoothly with the SS voltage until the voltage level zeros out.

**Power-Good (PG)**

The PG pin is the open drain of a MOSFET that connects to VCC or some other voltage source through a resistor (e.g., 100kΩ). The MOSFET turns on with the application of an input voltage so that the PG pin is pulled to GND before SS is ready. After FB voltage reaches 90% of VREF, the PG pin is pulled high after a 0.5ms delay.

When the FB voltage drops to 70% of VREF, the PG pin will be pulled low.

**Over-Current Protection (OCP) and Short-Circuit Protection (SCP)**

MP28257 has cycle-by-cycle over-current limit control. It monitors the inductor current during the ON state. Once the inductor current exceeds the current limit, the HS-FET turns off and the OCP timer—set at 50μs—starts. The OCP triggers. If the inductor current reaches or exceeds the current limit every cycle if in those the 50μs, the device enters latch-off mode.

The MP28257 SCP triggers when dead shorts occur—when the inductor current exceeds the current limit and the FB voltage is lower than 50% of the VREF—and will trigger the OCP. The MP28257 needs power cycle to restart after it triggers OCP or SCP.

**Over/Under-Voltage Protection (OVP/UVP)**

MP28257 monitors the output voltage through a resistor-divided FB voltage to detect over- and under-voltage on the output. When the FB voltage is higher than 125% of the VREF, it triggers the OVP. Once it triggers the OVP, the LS-FET is always on while the HS-FET is off. It needs to power cycle to turn on again. Conversely, the UVP triggers when the FB voltage falls below 50% of VREF (0.815V). Usually UVP accompanies a drop in the current limit and this results in SCP.

**UVLO Protection**

MP28257 has under-voltage lock-out (UVLO) protection. The MP28257 powers up when the input voltage exceeds the UVLO rising threshold voltage. It shuts off when the input voltage falls below the UVLO falling threshold voltage. This is non-latch protection.

**Thermal Shutdown**

The MP28257 employs thermal shutdown by internally monitoring the junction temperature of the IC. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is non-latch protection. There is about 25°C hysteresis. Once the junction temperature drops around 125°C, it initiates a soft start.
APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Caps

For applications that electrolytic capacitor or POS capacitor with a controlled output of ESR is set as output capacitors. The output voltage is set by feedback resistors R1 and R2. As Figure 10 shows.

![Simplified Circuit of POS Capacitor](image)

**Figure 10—Simplified Circuit of POS Capacitor**

First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when Vo is low, etc.,1.05V, and a smaller R2 when Vo is high. Then R1 is determined as follow with the output ripple considered:

\[
\frac{V_{OUT} - \frac{1}{2} \Delta V_{OUT}}{R_1} = \frac{V_{REF} - V_{OUT}}{R_2}
\]

(11)

\(\Delta V_{OUT}\) is the output ripple determined by equation 20.

Setting the Output Voltage-Small ESR Caps

![Simplified Circuit of Ceramic Capacitor](image)

**Figure 11—Simplified Circuit of Ceramic Capacitor**

When low ESR ceramic capacitor is used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4. The output voltage is influenced by ramp voltage \(V_{RAMP}\) besides R divider as shown in Figure 11. The \(V_{RAMP}\) can be calculated as shown in equation 7. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when Vo is low, etc.,1.05V, and a smaller R2 when Vo is high. And the value of R1 then is determined as follow:

\[
R_1 = \frac{V_{FB\text{(AVG)}} - \frac{1}{2} V_{RAMP}}{V_{REF} + \frac{1}{2} V_{RAMP}} \cdot \frac{R_2}{R_1 + R_2}
\]

(12)

\(V_{FB\text{(AVG)}}\) is the average value on the FB, \(V_{FB\text{(AVG)}}\) varies with the Vin, Vo, and load condition, etc., its value on the skip mode would be lower than that of the PWM mode which means the load regulation is strictly related to the \(V_{FB\text{(AVG)}}\). Also the line regulation is related to the \(V_{FB\text{(AVG)}}\). If one wants to get a better load or line regulation, a lower \(V_{RAMP}\) is suggested once it meets equation 9.

For PWM operation, \(V_{FB\text{(AVG)}}\) value can be deduced from equation 13.

\[
V_{FB\text{(AVG)}} = V_{REF} + \frac{1}{2} V_{RAMP} \times \frac{R_1}{R_2} + \frac{R_1}{R_2 + R_3}
\]

(13)

Usually, R9 is set to 0Ω, and it can also be set following equation 14 for a better noise immunity. It should also set to be 5 timers smaller than R1//R2 to minimize its influence on \(V_{RAMP}\).

\[
R_3 = \frac{1}{2\pi \times C_4 \times 2F_{SW}}
\]

(14)

Using equation 12 to calculate the output voltage can be complicated. To simplify the calculation of R1 in equation 12, a DC-blocking capacitor Cdc can be added to filter the DC influence from R4 and R9. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using equation 15 for PWM mode operation.

\[
R_1 = \frac{(V_{OUT} - V_{REF} - \frac{1}{2} V_{RAMP})}{V_{REF} + \frac{1}{2} V_{RAMP}} R_2
\]

(15)

Cdc is suggested to be at least 10 times larger than C4 for better DC blocking performance, and should also not larger than 0.47uF considering start up performance. In case one wants to use...
larger Cdc for a better FB noise immunity, combined with reduced R1 and R2 to limit the Cdc in a reasonable value without affecting the system start up. Be noted that even when the Cdc is applied, the load and line regulation are still Vramp related.

\[
\Delta V_{\text{IN}} = \frac{I_{\text{OUT}}}{f_{\text{SW}} \times C_{\text{IN}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \quad (18)
\]

Under worst-case conditions where \( V_{\text{IN}} = 2V_{\text{OUT}} \):

\[
\Delta V_{\text{IN}} = \frac{1}{4} \times \frac{I_{\text{OUT}}}{f_{\text{SW}} \times C_{\text{IN}}} \quad (19)
\]

**Output Capacitor**

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

\[
\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{8 \times f_{\text{SW}} \times C_{\text{OUT}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) + \frac{1}{8 \times f_{\text{SW}} \times C_{\text{OUT}}} \quad (20)
\]

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

\[
\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{f_{\text{SW}} \times C_{\text{OUT}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \quad (21)
\]

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4 following equation 5, 8 and 9.

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value around 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

\[
\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{f_{\text{SW}} \times L \times C_{\text{OUT}}} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \quad (22)
\]

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4 following equation 5, 8 and 9.

Maximum output capacitor limitation should be also considered in design application. MP28258 has an around 1ms soft-start time period. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value \( C_{o_{\text{MAX}}} \) can be limited approximately by:

\[
C_{o_{\text{MAX}}} = (I_{\text{LIM.AVG}} - I_{\text{OUT}}) \times T_{\text{ss}} / V_{\text{OUT}} \quad (23)
\]
Where, $I_{\text{LIM_AVG}}$ is the average start-up current during soft-start period. $T_{ss}$ is the soft-start time.

**Inductor**

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{\text{OUT}}}{I_{\text{SW}} \times \Delta I} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right)$$  \hspace{1cm} (24)

Where $\Delta I$ is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{\text{LP}} = I_{\text{OUT}} + \frac{V_{\text{OUT}}}{2f_{\text{SW}} \times L} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right)$$  \hspace{1cm} (25)

**Recommend Design Example**

Some design examples and recommended maximum output capacitor value with typical outputs are provided below when the ceramic capacitors is applied with $R_{9}=0\,\text{ohm}$:

### Table 1: 1.2V VOUT (L = 2$\mu$H)

<table>
<thead>
<tr>
<th>$V_{\text{IN}}$ (V)</th>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$C_{1}$</th>
<th>$R_{7}$ (Ω)</th>
<th>$R_{4}$ (Ω)</th>
<th>$C_{4}$ (F)</th>
<th>$R_{1}$ (Ω)</th>
<th>$R_{2}$ (Ω)</th>
<th>$F_{\text{SW}}$ (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>1.2</td>
<td>10μF*1</td>
<td>300k</td>
<td>499k</td>
<td>220p</td>
<td>12.1k</td>
<td>24.3k</td>
<td>450k</td>
</tr>
<tr>
<td>5</td>
<td>1.2</td>
<td>10μF*1</td>
<td>300k</td>
<td>390k</td>
<td>220p</td>
<td>12.1k</td>
<td>24.3k</td>
<td>440k</td>
</tr>
<tr>
<td>3.3</td>
<td>1.2</td>
<td>10μF*1</td>
<td>300k</td>
<td>243k</td>
<td>220p</td>
<td>12.1k</td>
<td>24.3k</td>
<td>435k</td>
</tr>
</tbody>
</table>

Note: For 1.8V $V_{\text{OUT}}$ from 3.3V $V_{\text{IN}}$, a larger $C_{1}$ is recommended to sustain maximum 4A load.

### Table 2: 1.8V VOUT (L = 2$\mu$H)

<table>
<thead>
<tr>
<th>$V_{\text{IN}}$ (V)</th>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$C_{1}$</th>
<th>$R_{7}$ (Ω)</th>
<th>$R_{4}$ (Ω)</th>
<th>$C_{4}$ (F)</th>
<th>$R_{1}$ (Ω)</th>
<th>$R_{2}$ (Ω)</th>
<th>$F_{\text{SW}}$ (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>1.8</td>
<td>10μF*1</td>
<td>402k</td>
<td>499k</td>
<td>220p</td>
<td>30.1k</td>
<td>24.3k</td>
<td>480k</td>
</tr>
<tr>
<td>5</td>
<td>1.8</td>
<td>10μF*1</td>
<td>402k</td>
<td>390k</td>
<td>220p</td>
<td>30.1k</td>
<td>24.3k</td>
<td>460k</td>
</tr>
<tr>
<td>3.3</td>
<td>1.8</td>
<td>10μF*2</td>
<td>402k</td>
<td>280k</td>
<td>220p</td>
<td>30.1k</td>
<td>24.3k</td>
<td>450k</td>
</tr>
</tbody>
</table>

### Table 3: 2.5V VOUT (L = 4.2$\mu$H)

<table>
<thead>
<tr>
<th>$V_{\text{IN}}$ (V)</th>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$C_{1}$</th>
<th>$R_{7}$ (Ω)</th>
<th>$R_{4}$ (Ω)</th>
<th>$C_{4}$ (F)</th>
<th>$R_{1}$ (Ω)</th>
<th>$R_{2}$ (Ω)</th>
<th>$F_{\text{SW}}$ (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>2.5</td>
<td>10μF*1</td>
<td>500k</td>
<td>439k</td>
<td>390p</td>
<td>21.5k</td>
<td>10k</td>
<td>500k</td>
</tr>
<tr>
<td>5</td>
<td>2.5</td>
<td>10μF*1</td>
<td>500k</td>
<td>439k</td>
<td>390p</td>
<td>21.5k</td>
<td>10k</td>
<td>500k</td>
</tr>
</tbody>
</table>

### Table 4: 3.3V VOUT (L = 6.5$\mu$H)

<table>
<thead>
<tr>
<th>$V_{\text{IN}}$ (V)</th>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$C_{1}$</th>
<th>$R_{7}$ (Ω)</th>
<th>$R_{4}$ (Ω)</th>
<th>$C_{4}$ (F)</th>
<th>$R_{1}$ (Ω)</th>
<th>$R_{2}$ (Ω)</th>
<th>$F_{\text{SW}}$ (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>3.3</td>
<td>10μF*1</td>
<td>680k</td>
<td>470k</td>
<td>330p</td>
<td>31.6k</td>
<td>10k</td>
<td>500k</td>
</tr>
<tr>
<td>5</td>
<td>3.3</td>
<td>10μF*1</td>
<td>680k</td>
<td>470k</td>
<td>330p</td>
<td>31.6k</td>
<td>10k</td>
<td>500k</td>
</tr>
</tbody>
</table>

### Table 5: 5V VOUT (L = 8.8$\mu$H)

<table>
<thead>
<tr>
<th>$V_{\text{IN}}$ (V)</th>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$C_{1}$</th>
<th>$R_{7}$ (Ω)</th>
<th>$R_{4}$ (Ω)</th>
<th>$C_{4}$ (F)</th>
<th>$R_{1}$ (Ω)</th>
<th>$R_{2}$ (Ω)</th>
<th>$F_{\text{SW}}$ (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>5</td>
<td>10μF*1</td>
<td>1M</td>
<td>750k</td>
<td>330p</td>
<td>53.6k</td>
<td>10k</td>
<td>500k</td>
</tr>
</tbody>
</table>

The detailed application schematic is shown in Figure 13 when large ESR caps are used, and Figure 14 and Figure 15 when low ESR caps are applied. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.
Typical Application Schematic

Figure 13—Typical Application Schematic with No External Ramp

Figure 14—Typical Application Schematic with Low ESR Ceramic Capacitor

Figure 15—Typical Application Schematic with Low ESR Ceramic Capacitor and DC Blocking Capacitor.
Layout Recommendation

1) The high current paths (GND, IN, and SW) should be placed very close to the device with short, wide, and direct traces.

2) Put the input capacitors as close to the IN and GND pins as possible.

3) Put the decoupling capacitor as close to the Vcc and GND pins as possible.

4) Keep the switching node SW short and away from the feedback network.

5) The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.

6) Keep the BST voltage path (BST, C3, and SW) as short as possible.

7) Four-layer layout is recommended to achieve better thermal performance.
PACKAGE INFORMATION

QFN12 (2x3mm)

NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX
4) JEDEC REFERENCE DRAWING IS JEDEC MO-220
5) DRAWING IS NOT TO SCALE

RECOMMENDED LAND PATTERN

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