DESCRIPTION

The MP28257 is a fully-integrated, synchronous, step-down, switch-mode converter with a programmable frequency. It offers a very compact solution that can provide up to 4A of continuous output current over a wide input supply range with excellent load and line regulation, and can operate at high efficiency over a wide output current load range.

Constant-on-time control mode provides fast transient response and eases loop stabilization.

Protection includes short-circuit protection, over-current protection, over-voltage protection, under-voltage protection, and thermal shutdown.

The MP28257 requires a minimal number of readily-available standard external components.

The device is available in a space saving 2mmx3mm QFN12 package that complies with ROHS.

FEATURES

- Wide 4.2V-to-20V Operating Input Range
- 4A Continuous Output Current
- Internal 120mΩ High-Side, 50mΩ Low-Side Power MOSFETs
- Stable with Ceramic Output Capacitors
- Proprietary Switching Loss-Reduction Technology
- Power-Good Indicator
- Soft Startup/Shutdown
- Programmable Switching Frequency
- SCP, OCP, OVP, UVP Protection and Thermal Shutdown
- Output Adjustable from 0.81V to 13V
- Available in a 2mmx3mm QFN12 Package

APPLICATIONS

- Networking Systems
- Distributed Power Systems

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**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>OCP Protection</th>
<th>Package</th>
<th>Top Marking</th>
<th>Free Air Temperature (T_A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP28257DD*</td>
<td>Latch-off Mode</td>
<td>QFN12 (2x3mm)</td>
<td>ABF</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP28257DD–Z).
For RoHS Compliant Packaging, add suffix –LF (e.g. MP28257DD–LF–Z)

**PACKAGE REFERENCE**

![TOP VIEW Diagram]

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage $V_{IN}$ .................................. 22V

$V_{SW}$ ........................................... -0.3V to ($V_{IN}$ + 0.3V)

$V_{BST}$ ........................................... $V_{SW}$+6V

All other pins .................................. -0.3V to +6V

Continuous Power Dissipation (T_A = 25°C) 1.8W

Junction Temperature .......................... 150°C

Lead Temperature ............................... 260°C

Storage Temperature ..................... -65°C to +150°C

**Recommended Operating Conditions**

Supply Voltage $V_{IN}$ ......................... 4.2V to 20V

Output Voltage $V_{OUT}$ .................... 0.815V to 13V

Maximum Junction Temp. (T_J) ................. 125°C

**Thermal Resistance**

QFN12 (2x3mm) .......................... $\theta_{JA}$ 70........ 15... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D (MAX)} = (T_J (MAX) - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
## ELECTRICAL CHARACTERISTICS

\( V_{IN} = 12\text{V}, \; T_A = 25^\circ\text{C}, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current (shutdown)</td>
<td>( I_{IN} )</td>
<td>( V_{EN} = 0\text{V} )</td>
<td>1</td>
<td></td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>Supply current (quiescent)</td>
<td>( I_{IN} )</td>
<td>( V_{EN} = 2\text{V}, ; V_{FB} = 0.9\text{V} )</td>
<td>360</td>
<td></td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>HS switch-on resistance (^{(b)})</td>
<td>( HS_{RDS-ON} )</td>
<td></td>
<td>120</td>
<td>m( \Omega )</td>
<td></td>
<td></td>
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<tr>
<td>LS Switch-on resistance (^{(b)})</td>
<td>( LS_{RDS-ON} )</td>
<td></td>
<td>50</td>
<td>m( \Omega )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switch leakage</td>
<td>( SW_{LKG} )</td>
<td>( V_{EN} = 0\text{V}, ; V_{SW} = 0\text{V} ) or 12V</td>
<td>0</td>
<td>10</td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>Current limit (5)</td>
<td>( I_{LIMIT} )</td>
<td>After Soft-Start Time-out</td>
<td>5.5</td>
<td>7</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>One-shot on time</td>
<td>( t_{ON} )</td>
<td>( R_7 = 300\text{k}\Omega, ; V_{OUT} = 1.2\text{V} )</td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Minimum off time</td>
<td>( t_{OFF} )</td>
<td></td>
<td>130</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Fold-back off time (^{(5)})</td>
<td>( t_{FB} )</td>
<td>( I_{LIMIT} = 1 )</td>
<td>4.5</td>
<td></td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td>OCP hold-off time (^{(5)})</td>
<td>( t_{OC} )</td>
<td>( I_{LIMIT} = 1 )</td>
<td>50</td>
<td></td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td>Feedback voltage</td>
<td>( V_{FB} )</td>
<td>( T_A = 25^\circ\text{C} )</td>
<td>807</td>
<td>815</td>
<td>823</td>
<td>mV</td>
</tr>
<tr>
<td>Feedback voltage</td>
<td>( V_{FB} )</td>
<td>( T_A = -40^\circ\text{C} ) to 85°C</td>
<td>803</td>
<td></td>
<td>827</td>
<td>mV</td>
</tr>
<tr>
<td>Feedback current</td>
<td>( I_{FB} )</td>
<td>( V_{FB} = 800\text{mV} )</td>
<td>10</td>
<td>50</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Soft start time</td>
<td>( t_{SS} )</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>EN rising threshold (^{(5)})</td>
<td>( EN_{Vth-Hi} )</td>
<td></td>
<td>1.05</td>
<td>1.35</td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td>EN threshold hysteresis (^{(5)})</td>
<td>( EN_{Vth-Hys} )</td>
<td></td>
<td>500</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>EN input current</td>
<td>( I_{EN} )</td>
<td>( V_{EN} = 2\text{V} )</td>
<td>2</td>
<td></td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>EN Input Current</td>
<td>( I_{EN} )</td>
<td>( V_{EN} = 0\text{V} )</td>
<td>0</td>
<td></td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>Power-good rising threshold (^{(5)})</td>
<td>( PG_{Vth-Hi} )</td>
<td>Power-good</td>
<td>90</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Power-good falling threshold (^{(5)})</td>
<td>( PG_{Vth-Lo} )</td>
<td>Fault condition</td>
<td>85</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Power-good delay (^{(5)})</td>
<td>( PG_{TD} )</td>
<td></td>
<td>500</td>
<td></td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td>Power-good sink current (^{(5)})</td>
<td>( I_{PG} )</td>
<td>( PG = 0.4\text{V} )</td>
<td>4</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Power-good leakage current (^{(5)})</td>
<td>( I_{PG \text{LEAK}} )</td>
<td>( V_{PG} = 3.3\text{V} )</td>
<td>10</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>VIN under-voltage lockout threshold rising (^{(5)})</td>
<td>( I_{INU\text{Vth}} )</td>
<td></td>
<td>3.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIN under-voltage lockout threshold hysteresis (^{(5)})</td>
<td>( I_{INU\text{VHYS}} )</td>
<td></td>
<td>300</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Thermal shutdown (^{(b)})</td>
<td>( T_{SD} )</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal shutdown hysteresis (^{(5)})</td>
<td>( T_{SD-HYS} )</td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

### Note:

5) Guaranteed by design.
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>IN</td>
<td>Supply Voltage. The MP28257 operates from a 4.2V to 20V input rail. C1 decouples the input rail. Use wide PCB traces and multiple vias to make the connection.</td>
</tr>
<tr>
<td>1, 11, 12</td>
<td>GND</td>
<td>System Ground. Reference ground for the regulated output voltage. These pins require special consideration during PCB layout.</td>
</tr>
<tr>
<td>2, 10, Exposed Pad</td>
<td>SW</td>
<td>Switch Output. Connect with wide PCB traces.</td>
</tr>
<tr>
<td>3</td>
<td>BST</td>
<td>Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.</td>
</tr>
<tr>
<td>4</td>
<td>VCC</td>
<td>Internal Bias Supply. Decouple with a 1μF ceramic capacitor as close to the pin as possible.</td>
</tr>
<tr>
<td>5</td>
<td>EN</td>
<td>EN = 1 to enable the MP28257. For automatic start-up, connect EN pin to VIN with a pull-up resistor.</td>
</tr>
<tr>
<td>7</td>
<td>FB</td>
<td>Feedback. Sets the output voltage when connected to the tap of an external resistor divider, connected between output and GND.</td>
</tr>
<tr>
<td>8</td>
<td>FREQ</td>
<td>Frequency. Set during CCM operation. Connect a resistor R7 to IN to set the switching frequency. Decouple with a 1nF capacitor.</td>
</tr>
<tr>
<td>6</td>
<td>PG</td>
<td>Power-Good Output. The output of this pin is an open drain that goes high if the output voltage is higher than 90% of the nominal voltage. There is a 0.5ms delay between when the feedback exceeds 90% to when the PG pin goes high.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

\( V_{\text{IN}} = 12V, \; V_{\text{OUT}} = 1.2V, \; L = 2\mu \text{H}, \; T_A = 25^\circ \text{C}, \) unless otherwise noted.

- **Efficiency vs. Load Current**
  - \( F_{\text{SW}} = 500\text{kHz} \)
  - \( V_{\text{IN}} = 5V, \; F_{\text{SW}} = 550\text{kHz}, \; L = 3.3\mu \text{H} \)

- **Line Regulation**
  - \( I_{\text{OUT}} = 4\text{A} \)

- **Load Regulation**
  - \( V_{\text{IN}} = 16V, 12V \)

- **Case Temp Rise**
  - \( T_a = +27.4^\circ \text{C} \)
  - \( V_{\text{IN}} = 21V, 12V \)

- **Frequency vs. Temperature**
  - \( R_{\text{SW}} = 274k\Omega, \; I_{\text{OUT}} = 4\text{A} \)

- **Frequency vs. Input Voltage**
  - \( R_{\text{SW}} = 274k\Omega, \; I_{\text{OUT}} = 4\text{A} \)
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

\( V_{\text{IN}} = 12V, \ V_{\text{OUT}} = 1.2V, \ L = 2\mu\text{H}, \ T_A = 25^\circ\text{C}, \) unless otherwise noted.

- **Input/Output Voltage Ripple**
  - \( I_{\text{OUT}} = 4A \)

- **Start up through VIN**
  - \( I_{\text{OUT}} = 0A \)

- **Start up through VIN**
  - \( I_{\text{OUT}} = 4A \)

- **Shutdown through VIN**
  - \( I_{\text{OUT}} = 0A \)

- **Shutdown through VIN**
  - \( I_{\text{OUT}} = 4A \)

- **Start up through EN**
  - \( I_{\text{OUT}} = 0A \)

- **Start up through EN**
  - \( I_{\text{OUT}} = 4A \)

- **Shutdown through EN**
  - \( I_{\text{OUT}} = 0A \)

- **Shutdown through EN**
  - \( I_{\text{OUT}} = 4A \)

- **VOUT**
  - 1V/div.

- **VIN**
  - 10V/div.

- **VSW**
  - 10V/div.

- **IL**
  - 5A/div.

- **1\mu\text{div.}**
  - 1\mu\text{div.}

- **400\mu\text{div.}**
  - 400\mu\text{div.}

- **2\text{ms/div.}**
  - 2\text{ms/div.}

- **400\mu\text{div.}**
  - 400\mu\text{div.}

- **200\mu\text{div.}**
  - 200\mu\text{div.}

- **400\mu\text{div.}**
  - 400\mu\text{div.}
Typical Performance Characteristics (continued)

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $L = 2\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

**Transient**

- $I_{OUT} = 0.4A-4A$ @ 2.5A/μs
- $F_{SW} = 500kHz$, $C_{OUT} = 2*22\mu F$

**Transient**

- $I_{OUT} = 0.4A-4A$ @ 2.5A/μs
- $F_{SW} = 500kHz$, $C_{OUT} = 2*22\mu F$
Figure 1: Functional Block Diagram
OPERATION

PWM Operation
The MP28257 is a fully-integrated, synchronous, rectified, step-down switch converter. The device uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON whenever the feedback voltage ($V_{FB}$) is lower than the reference voltage ($V_{REF}$)—a low $V_{FB}$ indicates insufficient output voltage. The input voltage and the frequency-set resistor determine the ON period as follows:

$$t_{ON}(\text{ns}) = \frac{9.3 \times R_f (\text{k} \Omega)}{V_{IN}(\text{V}) - 0.4} + 40 \text{ns}$$  \hspace{1cm} (1)

After the ON period elapses, the HS-FET enters the OFF state. By cycling the HS-FET between the ON and OFF states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its OFF state to minimize the conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are turned on at the same time, causing a dead short between input and GND. Shoot-through dramatically reduces efficiency, and the MP28257 avoids this by internally generating a dead-time (DT) between when the HS-FET is off and the LS-FET is on, and when the LS-FET is off and the HS-FET is on. The device enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

Heavy-Load Operation
During heavy-load operation—when the output current is high—the MP28257 enters continuous-conduction mode (CCM) where the HS-FET and LS-FET repeat the on/off operation described for PWM operation, the inductor current never goes to zero, and the switching frequency ($f_{SW}$) is fairly constant. Figure 2 shows the timing diagram during this operation.

Light-Load Operation
During light-load operation—when the output current is low—the MP28257 automatically reduces the switching frequency to maintain high efficiency, and the inductor current drops near zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high Z). The current modulator controls the LS-FET and limits the inductor current to around -1mA as shown in Figure 3. Hence, the output capacitors discharge slowly to GND through LS-FET, $R_1$, and $R_2$. This operation greatly improves device efficiency when the output current is low.

![Figure 2: Heavy-Load Operation](image)

![Figure 3: Light-Load Operation](image)

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as during heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current—as the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero, and can be determined using the following equation:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}}$$  \hspace{1cm} (2)

The device reverts to PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.
The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. The bootstrap capacitor is charges from VCC through N1 (Figure 4): N1 turns on when the LS-FET turns on, and turns off when the LS-FET turns off.

Switching Frequency
The MP28257 uses COT control because there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R7. The duty ratio is kept as $V_{OUT}/V_{IN}$, and the switching frequency is fairly constant over the input voltage range. The switching frequency can be determined with the following equation:

$$f_{SW} (kHz) = \frac{10^6}{9.3 \times R_7 (\kappa\Omega) \times V_{IN} (V) - 0.4 \times V_{OUT} (V) + t_{DELAY} (ns)}$$

(3)

Where $T_{DELAY}$ is the comparator delay, and equals approximately 40ns.

The MP28257 is optimized to operate at a high switching frequency a high efficiency. The high switching frequency makes it possible to use small-sized LC filter components to save system PCB space.

RAMP Compensation
Jitter occurs in both PWM and skip modes when noise in the $V_{FB}$ ripple propagates a delay to the HS-FET driver, as shown in Figures 5 and 6. Jitter can affect system stability, with a noise immunity proportional to the steepness of the $V_{FB}$’s downward slope. However, the $V_{FB}$ ripple does not directly affect noise immunity.

Figure 5: Jitter in PWM Mode

When using ceramic output capacitors, the ESR ripple is not sufficient to stabilize the system, and the system requires external ramp compensation.

Figure 6: Jitter in Skip Mode

Figure 7 shows a simplified external ramp compensator (R4 and C4) for PWM mode, with HS-FET off. Chose R1, R2, and C4 of the external ramp to meet the following condition:

$$\frac{1}{2\pi \times f_{SW} \times C_4} < \frac{1}{5} \times \left(\frac{R_1 \times R_2}{R_1 + R_2}\right)$$

(4)
Where:

\[ I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \]  

The downward slope of the \( V_{FB} \) ripple can be estimated as:

\[ V_{SLOPE1} = -\frac{V_{OUT}}{R_4 \times C_4} \]  

Reducing either \( R4 \) or \( C4 \), as seen from equation (6), can control some of the instability in PWM mode. If the condition from equation (4) prevents reductions to \( C4 \), then only reduce \( R4 \). \( V_{SLOPE1} \) has an expected range between 20V/ms to 40V/ms based on bench experiments.

The external ramp is not necessary for other types of capacitors with higher ESR such as POSCAPs.

\[ V_{SLOPE2} = \frac{-V_{REF}}{(R_1 + R_2) \times C_{OUT}} \]  

Figure 9: Simplified Circuit in Skip Mode

To keep the system stable during light load condition, use FB resistors in the range of 5k\( \Omega \) to 50k\( \Omega \). Keep the \( V_{SLOPE2} \) value between 0.4mV/ms to 0.8mV/ms.

Soft Start/Stop

MP28257 employs a soft-start/stop (SS) mechanism to ensure a smooth output during power up and power shut-down. When the EN pin goes high, the internal SS voltage slowly ramps up. The output voltage smoothly ramps up with the SS voltage. Once SS voltage rises above the \( V_{REF} \), it continues to ramp up while the PWM comparator only compares the \( V_{REF} \) and the FB voltage. At this point, the soft-start finishes and it enters steady state operation. The SS time is set about 1ms internally.

When the EN pin goes low, an internal current source discharges the internal SS voltage. Once the SS voltage falls below the \( V_{REF} \), the PWM comparator will only compare the \( V_{REF} \) to the SS voltage. The output voltage then decreases smoothly with the SS voltage until the voltage level zeros out.

Power-Good (PG)

The PG pin is the open drain of a MOSFET that connects to VCC or some other voltage source through a resistor (e.g., 100k\( \Omega \)). The MOSFET turns on with the application of an input voltage
so that the PG pin is pulled to GND before SS is ready. After FB voltage reaches 90% of V$_{\text{REF}}$, the PG pin is pulled high after a 0.5ms delay.

When the FB voltage drops to 70% of V$_{\text{REF}}$, the PG pin will be pulled low.

**Over-Current Protection (OCP) and Short-Circuit Protection (SCP)**

MP28257 has cycle-by-cycle over-current limit control. It monitors the inductor current during the ON state. Once the inductor current exceeds the current limit, the HS-FET turns off and the OCP timer—set at 50$\mu$s—starts. The OCP triggers. If the inductor current reaches or exceeds the current limit every cycle if in those the 50$\mu$s, the device enters latch-off mode.

The MP28257 SCP triggers when dead shorts occur—when the inductor current exceeds the current limit and the FB voltage is lower than 50% of the V$_{\text{REF}}$—and will trigger the OCP. The MP28257 needs power cycle to restart after it triggers OCP or SCP.

**Over/Under-Voltage Protection (OVP/UVP)**

MP28257 monitors the output voltage through a resistor-divided FB voltage to detect over- and under-voltage on the output. When the FB voltage is higher than 125% of the V$_{\text{REF}}$, it triggers the OVP. Once it triggers the OVP, the LS-FET is always on while the HS-FET is off. It needs to power cycle to turn on again. Conversely, the UVP triggers when the FB voltage falls below 50% of V$_{\text{REF}}$ (0.815V). Usually UVP accompanies a drop in the current limit and this results in SCP.

**UVLO Protection**

MP28257 has under-voltage lock-out (UVLO) protection. The MP28257 powers up when the input voltage exceeds the UVLO rising threshold voltage. It shuts off when the input voltage falls below the UVLO falling threshold voltage. This is non-latch protection.

**Thermal Shutdown**

The MP28257 employs thermal shutdown by internally monitoring the junction temperature of the IC. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is non-latch protection. There is about 25°C hysteresis. Once the junction temperature drops around 125°C, it initiates a soft start.
APPLICATION INFORMATION

Setting the Output Voltage
The output voltage is set by using a resistive voltage divider from the output voltage to the FB pin.

The use of low-ESR ceramic output capacitors requires adding an external voltage ramp to the FB through R4 and C4. Choose an R2 value between 5kΩ and 40kΩ, then determine R1 using the following equation:

\[ R_1 = \frac{1}{V_{REF} + \frac{1}{2}V_{RAMP}} - 1 \]

\[ R_2 \times (V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP}) \times R_4 \]

Using the V_RAMP value derived from equation (16). For example feedback resistor values and output voltages, see the design example section on page 15.

Input Capacitor
The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Use capacitors with X5R and X7R ceramic dielectrics because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

\[ I_{CIN} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \]

The worst-case condition occurs at V_IN = 2V_OUT, where:

\[ I_{CIN} = \frac{I_{OUT}}{2} \]

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows:

\[ \Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \]

Under worst-case conditions where V_IN = 2V_OUT:

\[ \Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \]

Output Capacitor
The output capacitor is required to maintain the DC output voltage. Ceramic or POSCON capacitors are recommended. The output voltage ripple can be estimated as:

\[ \Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \]

Where R_{ESR} is ESR value of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and is the primary contributor to the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

\[ \Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \]

The output voltage ripple caused by ESR is very small for ceramic capacitors, so it needs an external ramp to stabilize the system. The voltage ramp is expected to be around 30mV. The external ramp can be generated through resistor R4 and capacitor C4, using the following equation:

\[ V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{R_4 \times C_4} \]

The C4 should meet the following requirement:

\[ \frac{1}{2\pi \times f_{SW} \times C_4} < \frac{1}{5} \times \left( \frac{R_2}{R_1 + R_2} \right) \]

In the case of POSCON capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system, and does not require an external ramp. A minimum ESR value of 12mΩ is recommended to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:
\[ \Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{f_{\text{SW}}} \times L (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \times R_{\text{ESR}} \]  

(18)Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

\[ L = \frac{V_{\text{OUT}}}{f_{\text{SW}} \times \Delta I_L} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \]  

(19)Where \( \Delta I_L \) is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

\[ I_{\text{LP}} = I_{\text{OUT}} + \frac{V_{\text{OUT}}}{2f_{\text{SW}} \times L} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \]  

(20)

Design Example

Some design examples with typical outputs are provided below:

**Table 1: 1.2V VOUT (L = 2\( \mu \)H)**

<table>
<thead>
<tr>
<th>( I_{\text{IN}} ) (V)</th>
<th>( V_{\text{OUT}} ) (V)</th>
<th>( C1 ) (F)</th>
<th>( R7 ) (( \Omega ))</th>
<th>( R4 ) (( \Omega ))</th>
<th>( R3 ) (( \Omega ))</th>
<th>( R2 ) (( \Omega ))</th>
<th>( R1 ) (( \Omega ))</th>
<th>( F_{\text{SW}} ) (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12             1.2             10( \mu )F*1         300k          499k          220p          12.1k           24.3k          450k</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>5              1.2             10( \mu )F*1         300k          390k          220p          12.1k           24.3k          440k</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>3.3            1.2             10( \mu )F*1         300k          243k          220p          12.1k           24.3k          435k</td>
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</tbody>
</table>

Note: For 1.8V \( V_{\text{OUT}} \) from 3.3V \( I_{\text{IN}} \), a larger \( C1 \) is recommended to sustain maximum 4A load.

**Table 2: 1.8V VOUT (L = 2\( \mu \)H)**

<table>
<thead>
<tr>
<th>( I_{\text{IN}} ) (V)</th>
<th>( V_{\text{OUT}} ) (V)</th>
<th>( C1 ) (F)</th>
<th>( R7 ) (( \Omega ))</th>
<th>( R4 ) (( \Omega ))</th>
<th>( R3 ) (( \Omega ))</th>
<th>( R2 ) (( \Omega ))</th>
<th>( R1 ) (( \Omega ))</th>
<th>( F_{\text{SW}} ) (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12             1.8             10( \mu )F*1         402k          499k          220p          30.1k           24.3k          480k</td>
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</tr>
<tr>
<td>5              1.8             10( \mu )F*1         402k          390k          220p          30.1k           24.3k          460k</td>
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<td></td>
</tr>
<tr>
<td>3.3            1.8             10( \mu )F*2         402k          280k          220p          30.1k           24.3k          450k</td>
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</tbody>
</table>

**Table 3: 2.5V VOUT (L = 4.2\( \mu \)H)**

<table>
<thead>
<tr>
<th>( I_{\text{IN}} ) (V)</th>
<th>( V_{\text{OUT}} ) (V)</th>
<th>( C1 ) (F)</th>
<th>( R7 ) (( \Omega ))</th>
<th>( R4 ) (( \Omega ))</th>
<th>( R3 ) (( \Omega ))</th>
<th>( R2 ) (( \Omega ))</th>
<th>( R1 ) (( \Omega ))</th>
<th>( F_{\text{SW}} ) (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12             2.5             10( \mu )F*1         500k          453k          390p          21.5k           10k            500k</td>
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</tr>
<tr>
<td>5              2.5             10( \mu )F*1         500k          453k          390p          21.5k           10k            500k</td>
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</table>

**Table 4: 3.3V VOUT (L = 6.5\( \mu \)H)**

<table>
<thead>
<tr>
<th>( I_{\text{IN}} ) (V)</th>
<th>( V_{\text{OUT}} ) (V)</th>
<th>( C1 ) (F)</th>
<th>( R7 ) (( \Omega ))</th>
<th>( R4 ) (( \Omega ))</th>
<th>( R3 ) (( \Omega ))</th>
<th>( R2 ) (( \Omega ))</th>
<th>( R1 ) (( \Omega ))</th>
<th>( F_{\text{SW}} ) (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12             3.3             10( \mu )F*1         680k          470k          330p          31.6k           10k            500k</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>5              3.3             10( \mu )F*1         680k          470k          330p          31.6k           10k            500k</td>
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</tbody>
</table>

**Table 5: 5V VOUT (L = 8.8\( \mu \)H)**

<table>
<thead>
<tr>
<th>( I_{\text{IN}} ) (V)</th>
<th>( V_{\text{OUT}} ) (V)</th>
<th>( C1 ) (F)</th>
<th>( R7 ) (( \Omega ))</th>
<th>( R4 ) (( \Omega ))</th>
<th>( R3 ) (( \Omega ))</th>
<th>( R2 ) (( \Omega ))</th>
<th>( R1 ) (( \Omega ))</th>
<th>( F_{\text{SW}} ) (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12             5               10( \mu )F*1         1M            750k          330p          53.6k            10k            500k</td>
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</tbody>
</table>

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.
Layout Recommendation

1) The high current paths (GND, IN, and SW) should be placed very close to the device with short, wide, and direct traces.

2) Put the input capacitors as close to the IN and GND pins as possible.

3) Put the decoupling capacitor as close to the VCC and GND pins as possible.

4) Keep the switching node SW short and away from the feedback network.

5) The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.

6) Keep the BST voltage path (BST, C3, and SW) as short as possible.

7) Four-layer layout is recommended to achieve better thermal performance.

Figure 10: Typical Application Circuit

V\textsubscript{IN}=12V, V\textsubscript{OUT}=1.2V, I\textsubscript{OUT}=4A
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NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX
4) JEDEC REFERENCE DRAWING IS JEDEC MO220
5) DRAWING IS NOT TO SCALE

PACKAGE INFORMATION

QFN12 (2x3mm)

TOP VIEW

SIDE VIEW

BOTTOM VIEW

RECOMMENDED LAND PATTERN