MP28256

21V, 3A 500kHz Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP28256 is a synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 3A continuous output current over a wide input supply range with excellent load and line regulation. The MP28256 has synchronous mode operation for higher efficiency over output current load range.

Current mode operation provides fast transient response and eases loop stabilization. Full protection features include OCP and thermal shut down.

The MP28256 requires a minimum number of readily available standard external components and is available in a space saving QFN14 (3x4mm) package.

FEATURES

- Wide 4.5V to 21V Operating Input Range
- 0.6V internal reference with 2% accuracy
- 3A Output Current
- Low Rds(ON) Internal Power MOSFETs
- Fixed 500kHz Switching Frequency
- Frequency SYNC from 300kHz to 2MHz External Clock
- External Soft Start
- OCP and Thermal Shutdown
- Separate EN and SYNC pins
- Available in a QFN14 (3x4mm) Package.

APPLICATIONS

- DSL Modems
- Cable Modems
- Set Top Boxes

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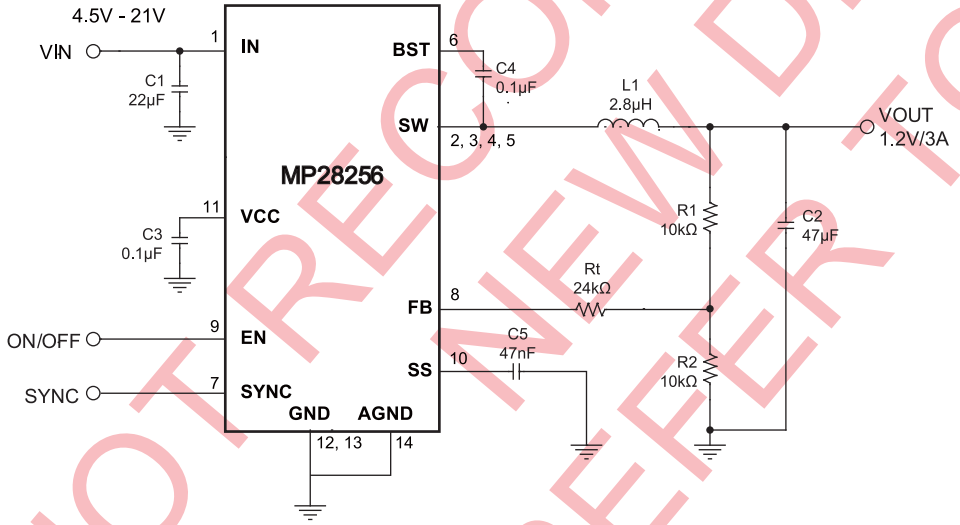
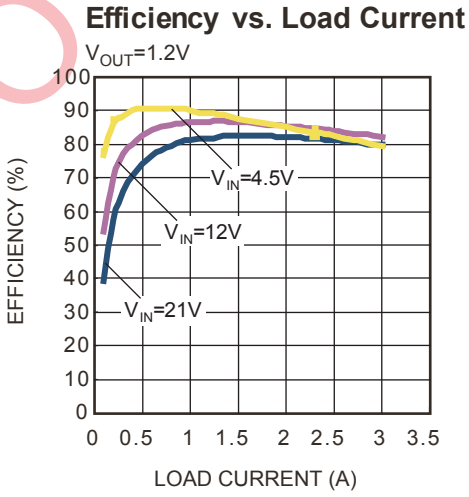
TYPICAL APPLICATION





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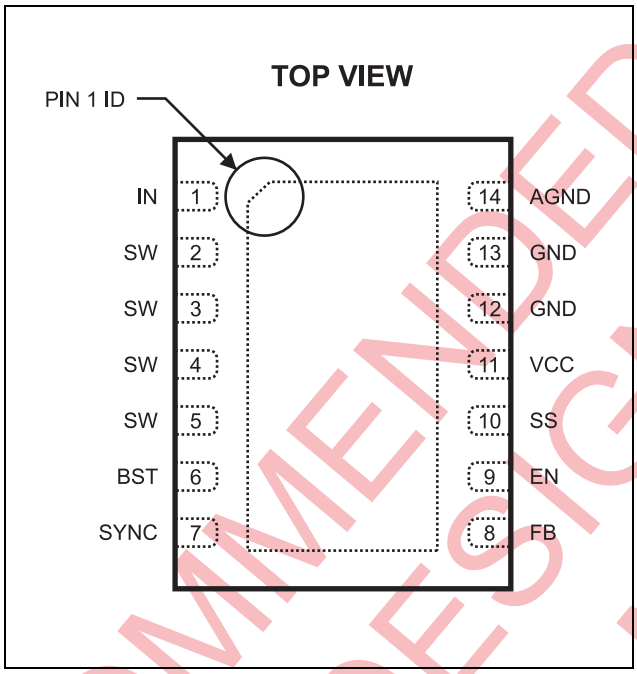
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP28256EL	QFN14 (3x4mm)	28256	-20°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP28256EL–Z);
For RoHS, compliant packaging, add suffix –LF (e.g. MP28256EL–LF–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 22V
V_{SW} ..... -0.3V to 23V
V_{BST} ..... V_{SW} + 6V
All Other Pins..... -0.3V to 6V
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Continuous Power Dissipation (T_A = +25°C) (2)
..... 2.6W
Junction Temperature..... 150°C
Operating Temperature..... -20°C to +85°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 21V
Output Voltage V_{OUT}..... 0.6V to 18V
Maximum Junction Temp. (T_J) ..... +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
QFN14 (3x4mm)	48	11 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		1		μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		0.7		mA
HS Switch On Resistance	HS_{RDS-ON}			120		mΩ
LS Switch On Resistance	LS_{RDS-ON}			20		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0.1	1	μA
Current Limit	I_{LIMIT}	D=40%	4.2			A
Oscillator Frequency	F_{SW}	V_{FB}=750mV	425	500	575	kHz
Minimum On Time	T_{ON-MIN}			80		ns
Maximum Duty Cycle	D_{MAX}	V_{FB} = 750mV	85	90		%
Sync Frequency Range	F_{SYNC}		0.3		2	MHz
Feedback Voltage	V_{FB}		591	603	615	mV
Feedback Current	I_{FB}	V_{FB} = 600mV		10	50	nA
EN Rising Threshold	$V_{EN\ RISING}$		1.1	1.3	1.6	V
EN Threshold Hysteresis	$V_{EN\ HYS}$			0.4		V
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0V		0.1		μA
SYNC Input High Level	V_{HI}		1.8			V
SYNC Input Low Level	V_{LO}				0.4	V
SYNC Input Current	I_{SYNC}	V_{SYNC}=6V		0.01	0.1	μA
Soft-start current	I_{SS}	V_{SS}=0		10		μA
V_{IN} Under Voltage Lockout Threshold Rising	$INUV_{Vth}$		3.8	4.0	4.2	V
V_{IN} Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			880		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		Icc=5mA		5		%
Thermal Shutdown	T_{SD}			150		°C

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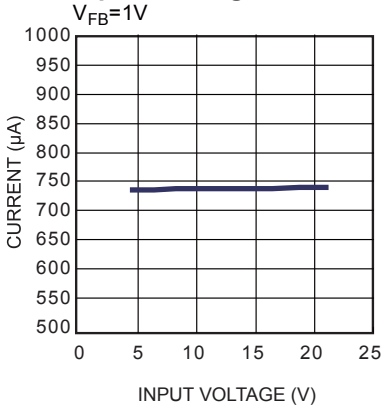
TYPICAL PERFORMANCE CHARACTERISTICS

Performance curves are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.8µH, T_A = +25ºC, unless otherwise noted.

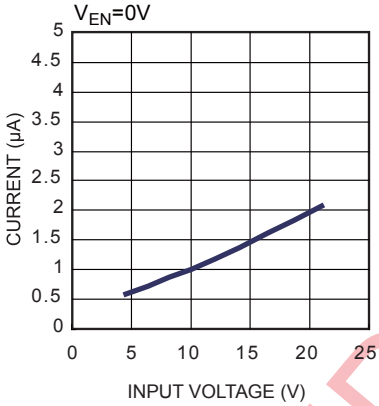
Enable Supply Current vs. Input Voltage

V_{FB}=1V

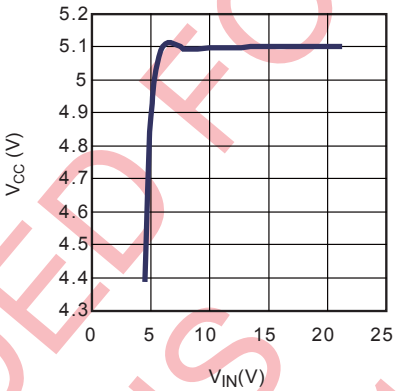


Disabled Supply Current vs. Input Voltage

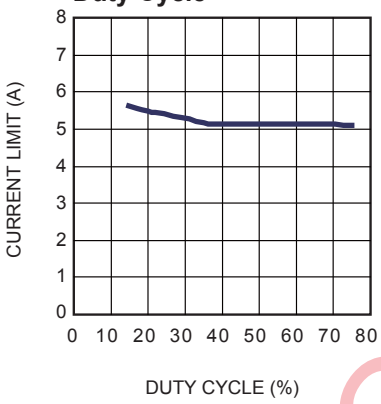
V_{EN}=0V



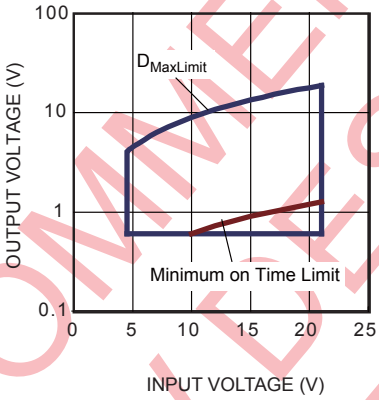
Vcc Regulator Line Regulation



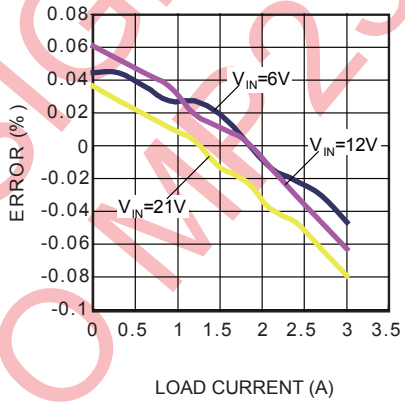
Current Limit vs. Duty Cycle



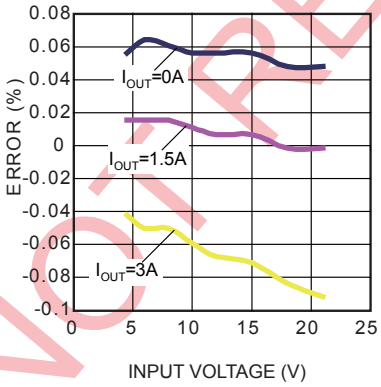
Operating Range



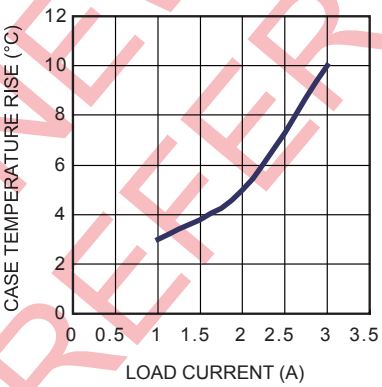
Load Regulation



Line Regulation



Case Temperature Rise vs. Output Current



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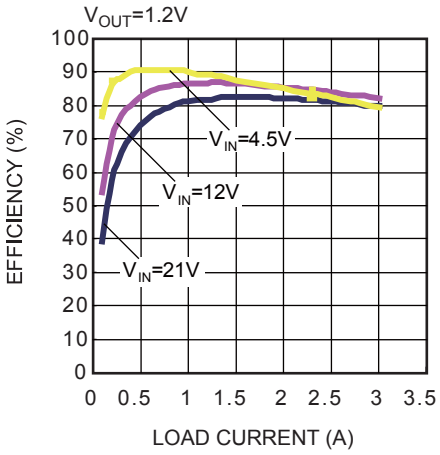
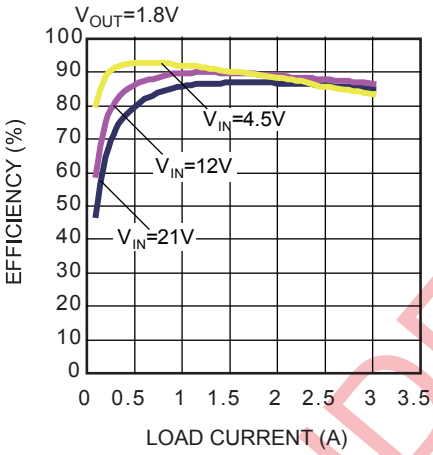
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.8µH, T_A = +25ºC, unless otherwise noted.

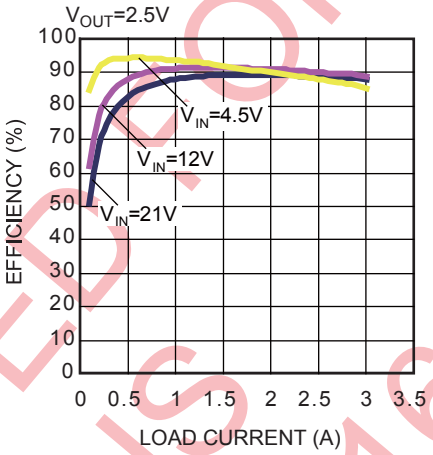
Efficiency



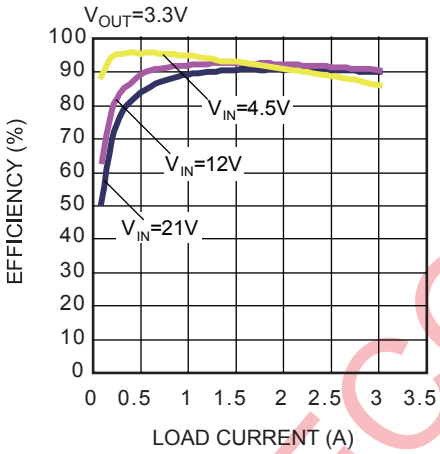
Efficiency



Efficiency



Efficiency



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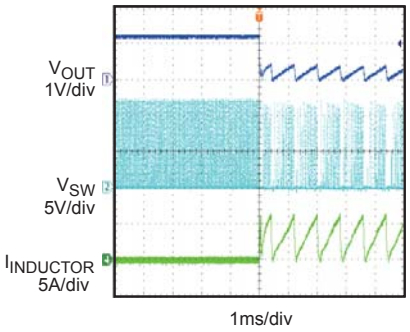
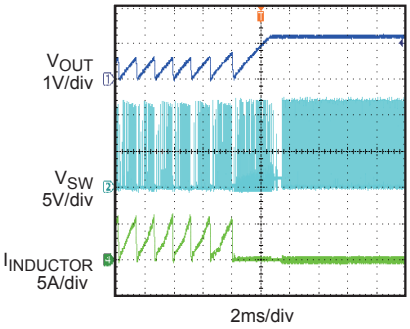
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.8µH, T_A = +25ºC, unless otherwise noted.

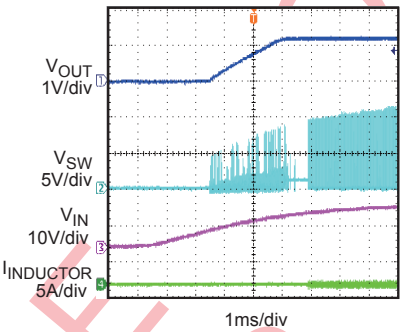
Short Entry



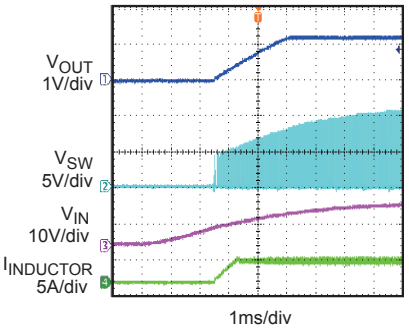
Short Recovery



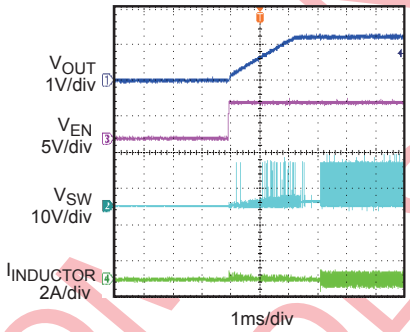
Power Up without Load



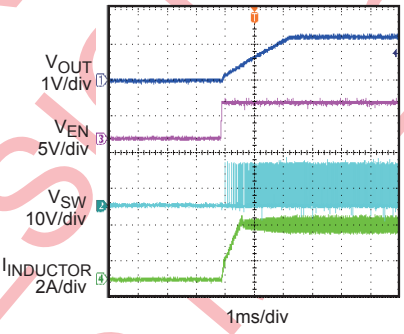
Power Up with 3A Load



Enable Startup without Load

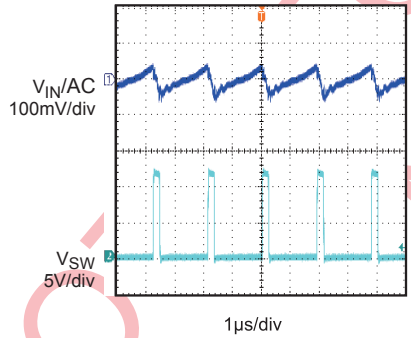


Enable Startup with 3A Load



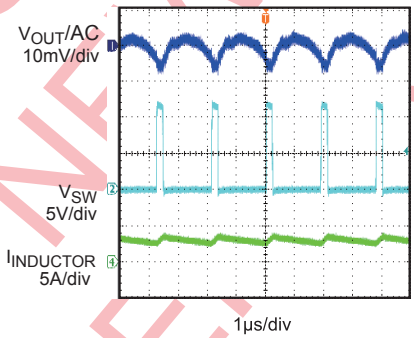
Input Ripple Voltage

I_{OUT}=3A



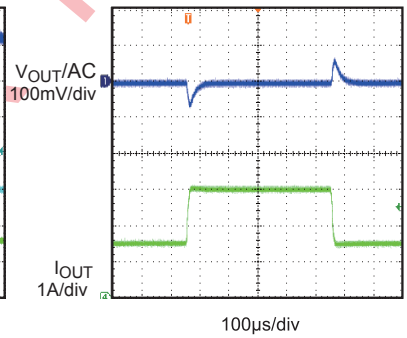
Output Ripple Voltage

I_{OUT}=3A



Load Transient Response

I_{OUT}=1.5A-3A



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PIN FUNCTIONS

QFN14 (3x4mm) Pin #	Name	Description
1	IN	Supply Voltage. The MP28256 operates from a +4.5V to +21V input rail. C1 is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2,3,4,5	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
6	BST	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.
7	SYNC	This pin serves as frequency synchronous clock input.
8	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 100mV.
9	EN	EN=1 to enable the MP28256. For automatic start-up, connect EN pin to VIN with 100kHz resistor. There is an internal 1mΩ pull-down resistor at EN pin.
10	SS	Soft Start. Connect an external capacitor to program the soft start time for the switch mode regulator.
11	VCC	Bias Supply. Decouple with 0.1μF~0.22μF cap. And the capacitance should be no more than 0.22μF.
12,13	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
14	AGND	Signal Ground. AGND is not internally connected to System Ground, make sure AGND connected to system Ground in PCB layout.
	Exposed Pad	No Internal Connection. It is recommended to connect exposed pad to GND plane for optimal thermal performance.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2310

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OPERATION

The MP28256 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve more than 3A continuous output current over a wide input supply range with excellent load and line regulation.

The MP28256 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.6V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases, a 0.1uF ceramic capacitor for decoupling purpose is required.

Enable Control

The MP28256 has a dedicated Enable control pin (EN). By pulling it high or low, the IC can be enabled and disabled by EN. Tie EN to VIN through a resistor for automatic start up. To disable the part, EN must be pulled low.

Frequency Synchronizing

The MP28256 can be synchronized to external clock range from 300 kHz up to 2MHz through the SYNC pin. The internal clock rising edge is synchronized to the external clock rising edge.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP28256 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is a consistent 3.2V.

External Soft-Start

The soft start time can be adjusted by connecting a capacitor from this pin to ground. When the soft-start period starts, an internal 10uA current source begins charging the external capacitor. During soft-start, the voltage on the soft-start capacitor is connected to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.6V. At this point the reference voltage takes over at the no inverting error amplifier input. The soft-start time can be calculated as follows:

$$t_{SS}(ms) = \frac{0.6V \times C_{SS}(nF)}{10\mu A}$$

If the output of the MP28256 is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

Over-Current-Protection

The MP28256 has hiccup over current limit when the inductor current peak value exceeds the set current limit threshold. When output voltage drops below 70% of the reference, and inductor current exceeds the current limit at the meantime, MP28256 will be hiccup. This is especially useful to ensure system safety under fault condition. The latch-off function is disabled during soft-start duration.

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Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, C4, L1 and C2 (Figure 2). If (VIN-VSW) is more than 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4.

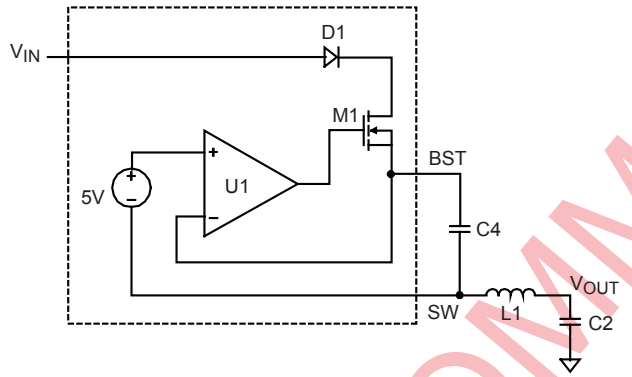

Figure 2—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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BLOCK DIAGRAM

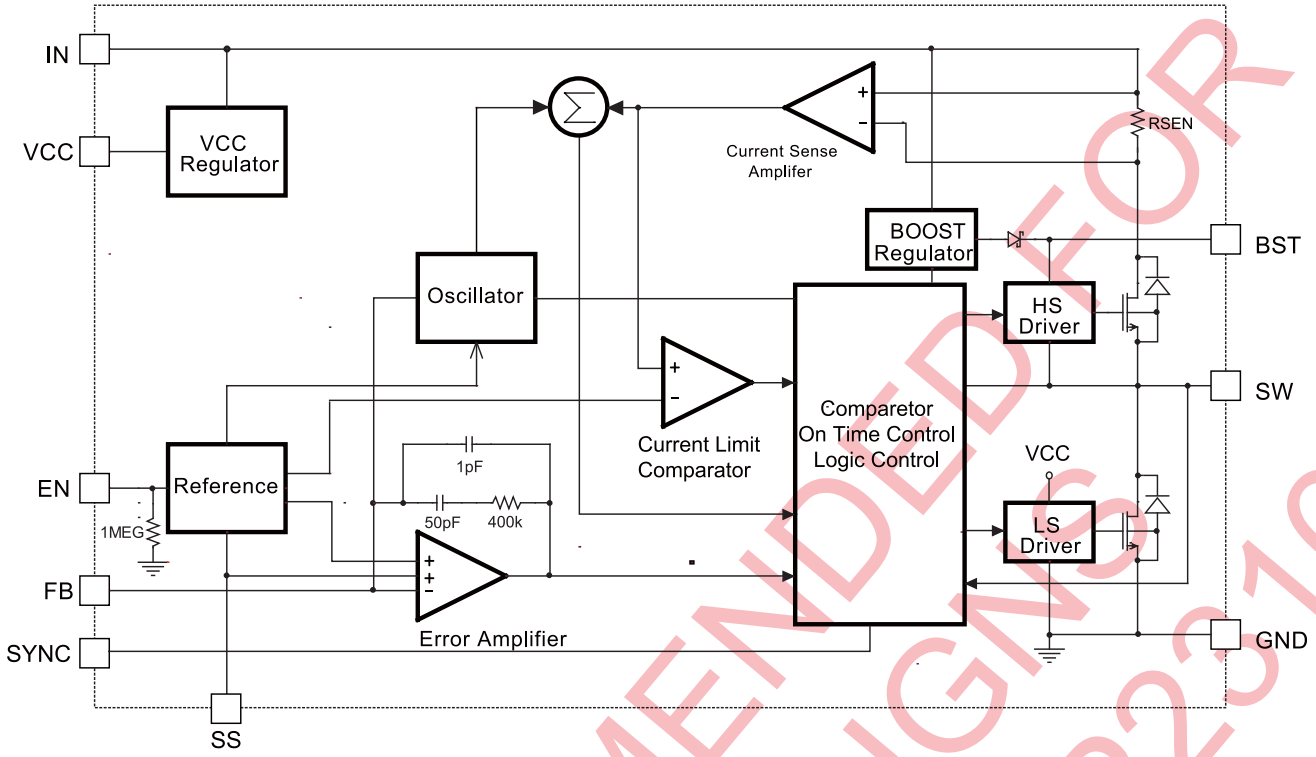

Figure 3—Block Function Diagram

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 to be around 10kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1}$$

The T-type network is highly recommended when Vo is low, as Figure 4 shows.

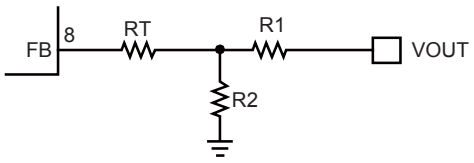

Figure 4— T-type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)
1.05	7.5(1%)	10(1%)	24.9(1%)
1.2	10(1%)	10(1%)	24.9(1%)
1.8	10(1%)	4.99(1%)	24.9(1%)
2.5	10(1%)	3.16(1%)	24.9(1%)
3.3	10(1%)	2.20(1%)	24.9(1%)
5	10(1%)	1.36(1%)	24.9(1%)

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22μF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

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$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP28256 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BST diode is recommended from the VCC pin to BST pin, as shown in Figure 5.

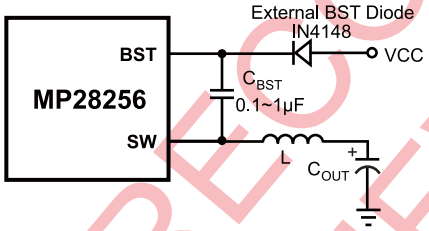

Figure 5—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

PC Board Layout

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

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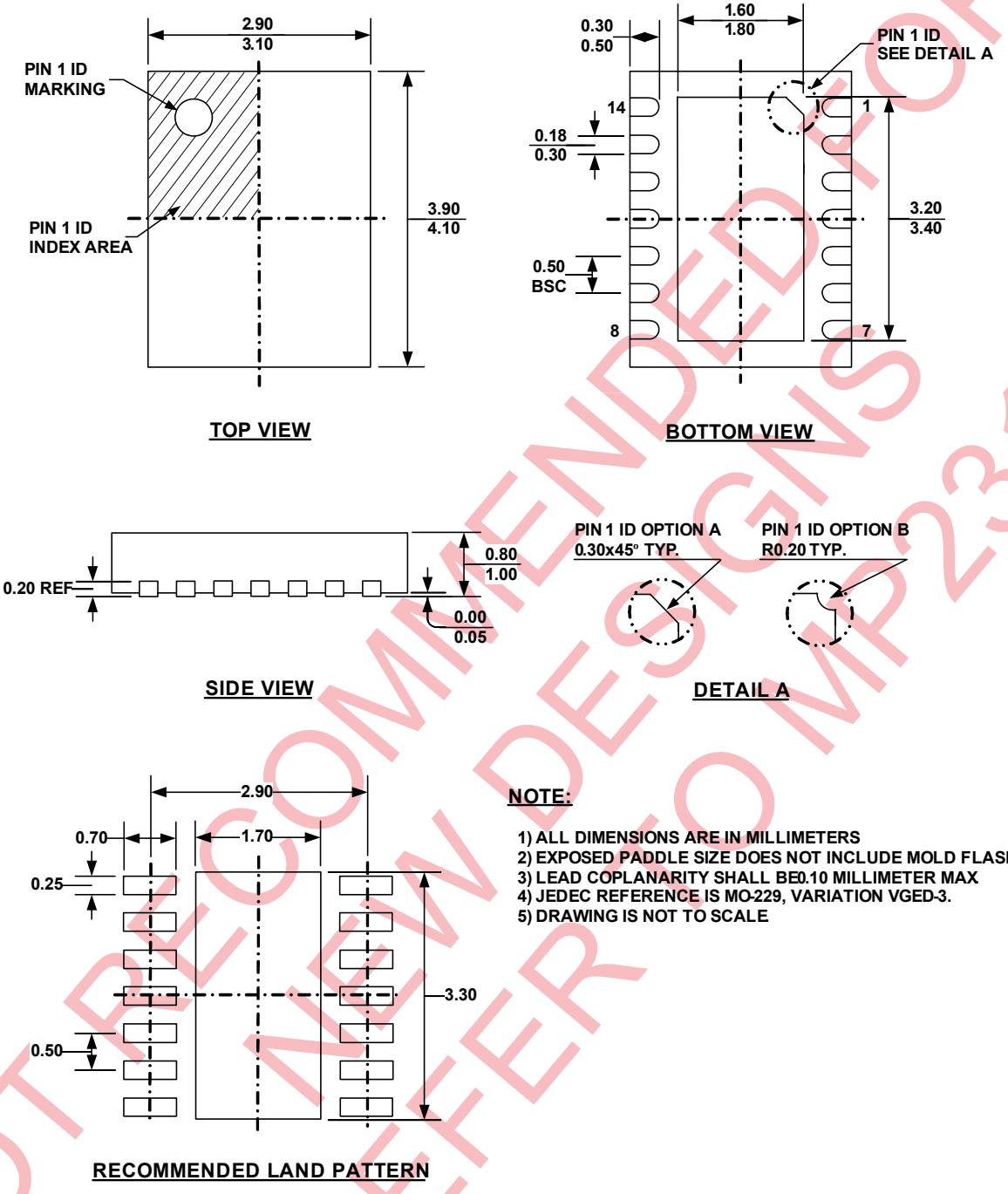
PACKAGE INFORMATION

QFN14 (3x4mm)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETER MAX
4) JEDEC REFERENCE IS MO-229, VARIATION VGED-3.
5) DRAWING IS NOT TO SCALE

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