DESCRIPTION
The MP28167 is a synchronous, 4-switch, integrated buck-boost converter, capable of regulating the output voltage across a 2.8V to 22V wide input voltage range with high efficiency.

The MP28167 uses constant-on-time control in buck mode and constant-off-time control in boost mode, providing fast load transient response as well as smooth buck-boost mode transient. The MP28167 provides forced PWM switching mode and programmable output CC (constant current) limit, which supports flexible design for different applications.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MP28167 is available in a 16-pin QFN (3mmx3mm) package.

FEATURES
- Wide 2.8V to 22V Operating Input Voltage Range
- Fixed 5V Output Voltage
- 3A Output Current or 4A Input Current
- 130mV Line Drop Compensation
- 500kHz Fixed Switching Frequency
- Forced PWM Switching Mode
- Four Low R_{DS(on)} Internal Buck Power MOSFETs
- Adjustable Accurate CC Output Current Limit with Internal Sensing FET
- Output Over-Voltage Hiccup Protection
- Output Short-Circuitry Hiccup Protection
- Over-Temperature Shutdown
- EN Shutdown Discharge Function
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS
- Buck-Boost Bus Supply

TYPICAL APPLICATION

Efficiency vs. Output Current

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7\mu H, R_{DC} = 19.7m\Omega
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP28167GQ</td>
<td>QFN-16 (3mmx3mm)</td>
<td>See Below</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP28167GQ–Z).

TOP MARKING

BJHY
LLL

BJH: Product code of MP28167GQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

QFN-16 (3mmx3mm)
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN</td>
<td><strong>Supply voltage.</strong> IN is the drain of the internal power device and provides power to the entire chip. The MP28167 operates from a 2.8V to 22V input voltage. A capacitor (C&lt;sub&gt;IN&lt;/sub&gt;) is required to prevent large voltage spikes from appearing at the input. Place C&lt;sub&gt;IN&lt;/sub&gt; as close to the IC as possible.</td>
</tr>
<tr>
<td>2, 11</td>
<td>GND</td>
<td><strong>Power ground.</strong> GND is the reference ground of the regulated output voltage. GND requires extra care during PCB layout. Connect GND with copper traces and vias.</td>
</tr>
<tr>
<td>3</td>
<td>EN</td>
<td><strong>On/off control for entire chip.</strong> Drive EN high to turn on the chip. Drive EN low or float EN to turn off the device. EN has an internal 2MΩ pull-down resistor to ground.</td>
</tr>
<tr>
<td>4, 8</td>
<td>NC</td>
<td><strong>No connection.</strong> These pins should be connected to GND.</td>
</tr>
<tr>
<td>5</td>
<td>RSV1</td>
<td><strong>Reserved pin.</strong> This pin cannot be floated. It can be tied to GND or VCC.</td>
</tr>
<tr>
<td>6</td>
<td>RSV2</td>
<td><strong>Reserved pin.</strong> This pin cannot be floated. It can be tied to GND or VCC.</td>
</tr>
<tr>
<td>7</td>
<td>OC</td>
<td><strong>Output constant current limit set pin.</strong></td>
</tr>
<tr>
<td>9</td>
<td>VCC</td>
<td><strong>Internal 3.65V LDO regulator output.</strong> Decouple VCC with a 1µF capacitor.</td>
</tr>
<tr>
<td>10</td>
<td>AGND</td>
<td><strong>Analog ground.</strong> Connect AGND to GND.</td>
</tr>
<tr>
<td>12</td>
<td>OUT</td>
<td><strong>Output power pin.</strong> Place the output capacitor close to OUT and GND.</td>
</tr>
<tr>
<td>13</td>
<td>BST2</td>
<td><strong>Bootstrap.</strong> Connect a 0.1µF capacitor between SW2 and BST2 to form a floating supply across the high-side switch driver.</td>
</tr>
<tr>
<td>14</td>
<td>SW2</td>
<td><strong>Switching node of the second half-bridge.</strong> Connect one end of the inductor to SW2 for the current to run through the bridge.</td>
</tr>
<tr>
<td>15</td>
<td>SW1</td>
<td><strong>Switching node of the first half-bridge.</strong> Connect one end of the inductor to SW1 for the current to run through the bridge.</td>
</tr>
<tr>
<td>16</td>
<td>BST1</td>
<td><strong>Bootstrap.</strong> Connect a 0.1µF capacitor between SW1 and BST1 to form a floating supply across the high-side switch driver.</td>
</tr>
</tbody>
</table>
ABSOLUTE MAXIMUM RATINGS (1)
Supply voltage ($V_{IN}, V_{OUT}$) ..................................... 24V
$V_{SW1, SW2}$ .......................................................... -0.3V (-7V for <10ns) to $V_{IN} + 0.3V$ (26V for <10ns)
$V_{BST1, BST2}$ .......................................................... $V_{SWx} + 4V$
$V_{EN}$ ................................................................. -0.3V to +24V
All other pins ....................................................... -0.3V to +4V
Continuous power dissipation ($T_A = +25^\circ C$) (2) (4)
................................................................. 4.8W
Junction temperature ............................................. 150°C
Lead temperature .................................................. 260°C
Storage temperature ...................................... -65°C to +150°C

Recommended Operating Conditions (3)
Operation input voltage range ........2.8V to 22V
Output voltage range ......................... Fixed 5V
Output current .............................................. 3A continuous current or 4A input current
Operating junction temp ($T_J$) ....... -40°C to +125°C

Thermal Resistance $\theta_{JA} \theta_{JC}$
QFN-16 (3mmx3mm)
EV28167-Q-00A (4) .................. 26 ...... 3...°C/W
JESD51-7 (5) .......................... 50 ...... 12...°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV28167-Q-00A, 4-layer-PCB, 64mmx64mm.
5) Measured on JESD51-7, 4-layer PCB. The value of $\theta_{JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
### ELECTRICAL CHARACTERISTICS

V\textsubscript{IN} = 12V, V\textsubscript{EN} = 5V, T\textsubscript{J} = -40°C to +125°C (\textsuperscript{6}), typical value is tested at T\textsubscript{J} = +25°C, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current (shutdown)</td>
<td>I\textsubscript{IN}</td>
<td>V\textsubscript{EN} = 0V</td>
<td>0</td>
<td>3</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Supply current (quiescent)</td>
<td>I\textsubscript{Q}</td>
<td>Remove inductor, add 5.8V to V\textsubscript{OUT}</td>
<td>1</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>EN rising threshold</td>
<td>V\textsubscript{EN,Rising}</td>
<td></td>
<td>1.0</td>
<td>1.10</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>EN hysteresis</td>
<td>V\textsubscript{EN,Falling}</td>
<td></td>
<td>65</td>
<td>110</td>
<td>160</td>
<td>mV</td>
</tr>
<tr>
<td>EN to ground resistance</td>
<td>R\textsubscript{EN}</td>
<td>V\textsubscript{EN} = 2V</td>
<td>2</td>
<td></td>
<td>MΩ</td>
<td></td>
</tr>
<tr>
<td>EN on to V\textsubscript{OUT} &gt; 90% delay</td>
<td>T\textsubscript{Delay}</td>
<td>See Figure 7</td>
<td></td>
<td>500</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>VCC regulator</td>
<td>V\textsubscript{CC}</td>
<td></td>
<td>3.3</td>
<td>3.65</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>VCC load regulation</td>
<td>V\textsubscript{CC,LOG}</td>
<td>I\textsubscript{CC} = 10mA</td>
<td></td>
<td>1</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>V\textsubscript{IN} under-voltage lockout threshold rising</td>
<td>V\textsubscript{IN,UVLO}</td>
<td></td>
<td>2.50</td>
<td>2.65</td>
<td>2.8</td>
<td>V</td>
</tr>
<tr>
<td>V\textsubscript{IN} under-voltage lockout threshold hysteresis</td>
<td>V\textsubscript{UVLO,HYS}</td>
<td></td>
<td>95</td>
<td>160</td>
<td>205</td>
<td>mV</td>
</tr>
</tbody>
</table>

#### Power Converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS switch on resistance</td>
<td>R\textsubscript{DSON HS}</td>
<td>Switch A, D</td>
<td>25</td>
<td>40</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>LS switch on resistance</td>
<td>R\textsubscript{DSON LSB}</td>
<td>Switch B, C</td>
<td>21</td>
<td>35</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>V\textsubscript{OUT}</td>
<td></td>
<td>-1.5%</td>
<td>5.0</td>
<td>+1.5%</td>
<td>V</td>
</tr>
<tr>
<td>Output discharge resistance</td>
<td>R\textsubscript{DIS}</td>
<td></td>
<td>60</td>
<td>100</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Switch leakage</td>
<td>S\textsubscript{WKG}</td>
<td>V\textsubscript{EN} = 0V, V\textsubscript{SW1, SW2} = 22V, T\textsubscript{J} = +25°C</td>
<td></td>
<td>1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{EN} = 0V, V\textsubscript{SW1, SW2} = 22V, T\textsubscript{J} = -40°C to +125°C</td>
<td></td>
<td>5</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>Oscillator frequency</td>
<td>f\textsubscript{S}</td>
<td>T\textsubscript{J} = +25°C</td>
<td>-20%</td>
<td>530</td>
<td>20%</td>
<td>kHz</td>
</tr>
<tr>
<td>Minimum on time (^\textsuperscript{(7)})</td>
<td>t\textsubscript{ON,MINT}</td>
<td>Switch A, B, C, D</td>
<td>160</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Maximum duty cycle</td>
<td>D\textsubscript{MAX}</td>
<td>Buck mode, F\textsubscript{REQ} = 500kHz</td>
<td>85</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Minimum duty cycle (^\textsuperscript{(8)})</td>
<td>D\textsubscript{MIN}</td>
<td>Boost mode, F\textsubscript{REQ} = 500kHz</td>
<td>15</td>
<td></td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

#### Protection

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output over-voltage protection</td>
<td>V\textsubscript{OVP,R}</td>
<td></td>
<td>150</td>
<td>160</td>
<td>170</td>
<td>%</td>
</tr>
<tr>
<td>Output OVP recovery</td>
<td>V\textsubscript{OVP,F}</td>
<td></td>
<td>130</td>
<td>140</td>
<td>150</td>
<td>%</td>
</tr>
<tr>
<td>Low-side B valley limit</td>
<td>I\textsubscript{LIMIT2}</td>
<td>Switch B</td>
<td>6</td>
<td>8</td>
<td>10</td>
<td>A</td>
</tr>
<tr>
<td>Low-side C peak current limit</td>
<td>I\textsubscript{LIMIT3}</td>
<td>Switch C</td>
<td></td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Output average current (^\textsuperscript{(8)})</td>
<td>I\textsubscript{OUT,LIM2}</td>
<td>V\textsubscript{OUT} = 5V, over 0-125°C temp range</td>
<td>-5%</td>
<td>3.5</td>
<td>+5%</td>
<td>A</td>
</tr>
<tr>
<td>Output UV threshold</td>
<td>V\textsubscript{UVP}</td>
<td>20μs deglitch, UV falling</td>
<td>45%</td>
<td>50%</td>
<td>55%</td>
<td>V\textsubscript{REF}</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN} = 12\text{V}$, $V_{EN} = 5\text{V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ *(6)*, typical value is tested at $T_J = +25^\circ\text{C}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal shutdown rising threshold <em>(7)</em></td>
<td>$T_{STD}$</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal hysteresis <em>(7)</em></td>
<td>$T_{STD,HYS}$</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

Notes:

6) All min/max parameters are tested at $T_J = 25^\circ\text{C}$. Limits over temperature are guaranteed by design, characterization, and correlation.
7) Guarantee by engineering sample characterization.
8) Guaranteed by characterization.
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 4.7\mu\text{H}$, $T_{A} = 25^\circ\text{C}$, unless otherwise noted.

**Efficiency vs. Output Current**

$V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 4.7\mu\text{H}$, $R_{DC} = 19.7\text{m}\Omega$

**Output Line Drop Compensation vs. Output Current**

**Thermal Rising vs. Output Current**

$V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $I_{OUT} = 0\text{A}$ to $3\text{A}$

**Recommended Maximum $I_{OUT}$ vs. $V_{IN}$ with 120µF Low-ESR $C_{OUT}$ Capacitor**

**Output Voltage vs. Temperature**
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 4.7\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

VIN UVLO Rising and Falling Threshold vs. Temperature

EN Rising and Falling Threshold vs. Temperature

Buck Valley Current Limit vs. Temperature

Output Voltage UVP Threshold vs. Temperature
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Vin = 12V, Vout = 5V, L = 4.7µH, TA = 25°C, test waveform is based on Figure 9, unless otherwise noted.

VIN Start-Up
Load = 0A

VIN Power Off
Load = 0A

EN Pin Enable
Load = 0A
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12\, \text{V}, \, V_{OUT} = 5\, \text{V}, \, T_A = 25^\circ \text{C}, \, L = 4.7\, \mu\text{H}$, test waveform is based on Figure 9, unless otherwise noted.

**EN Pin Disable**

**Load = 0A**

- CH1: $V_{OUT}$
  - 5V/div.
- CH2: $V_{SW1}$
  - 10V/div.
- CH3: $V_{SW2}$
  - 5V/div.
- CH4: $I_L$
  - 5A/div.

2ms/div.

**Load = 3A**

- CH1: $V_{OUT}$
  - 5V/div.
- CH2: $V_{SW1}$
  - 10V/div.
- CH3: $V_{SW2}$
  - 5V/div.
- CH4: $I_L$
  - 5A/div.

200μs/div.

**Steady State**

$V_{OUT} = 5\, \text{V}, \, \text{load} = 0\, \text{A}$

- CH1: $V_{OUT}$/AC
  - 50mV/div.
- CH2: $V_{SW1}$
  - 10V/div.
- CH3: $V_{SW2}$
  - 5V/div.
- CH4: $I_L$
  - 1A/div.

1μs/div.

**Load = 3A**

- CH1: $V_{OUT}$/AC
  - 50mV/div.
- CH2: $V_{SW1}$
  - 10V/div.
- CH3: $V_{SW2}$
  - 5V/div.
- CH4: $I_L$
  - 2A/div.

1μs/div.

**Load Transient**

$V_{IN} = 12\, \text{V}, \, V_{OUT} = 5\, \text{V}, \, 0\, \text{A to 3A}, \, 150\, \text{mA/μs}$

- CH1: $V_{OUT}$/AC
  - 500mV/div.
- CH4: $I_{OUT}$
  - 2A/div.

400μs/div.

**Load = 1.5A**

- CH1: $V_{OUT}$/AC
  - 200mV/div.
- CH4: $I_{OUT}$
  - 1A/div.

400μs/div.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

\( V_{\text{IN}} = 12\, \text{V}, V_{\text{OUT}} = 5\, \text{V}, T_A = 25^\circ\text{C}, L = 4.7\, \mu\text{H} \), test waveform is based on Figure 9, unless otherwise noted.

Load Transient

\( V_{\text{IN}} = 12\, \text{V}, V_{\text{OUT}} = 5\, \text{V}, 1.5\, \text{A to} 3\, \text{A}, 150\, \text{mA/\mu s} \)

SCP Entry with Hiccup Mode

SCP Recovery with Hiccup Mode

CC Current Limit Entry (Test with CV Mode of Electronic Load)

CC Current Limit Steady State

VOUT OVP with Hiccup Mode
Figure 1: Functional Block Diagram
OPERATION

The MP28167 is a 4-switch, integrated buck-boost converter that can work in constant-on-time (COT) mode with fixed frequency, which provides fast transient response for buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency over the full input range and smooth transient between different modes.

Figure 1 shows the functional block diagram, and the following sections describe the detail function.

Buck-Boost Operation

The MP28167 can regulate its output to be above, equal to, or below the input voltage. Figure 2 shows the 1-inductor, 4-switch power structure, which operates in buck mode, boost mode, or buck-boost mode with different $V_{IN}$ inputs (see Figure 3).

Buck Mode ($V_{IN} > V_{OUT}$)

When the input voltage is significantly higher than the output voltage, the MP28167 works in buck mode. In buck mode, SWA and SWB switch for the buck regulation, while SWC is off and SWD remains on to conduct the inductor current.

SWA works with COT control logic and SWB turns on as a complement to SWA. In each cycle, SWB turns on to conduct the inductor current. When the inductor current drops to the COMP voltage, SWB turns off and SWA turns on. SWA turns on for a fixed period and then turns off, after which SWB turns on again and repeats. The COMP signal is the EA output from $V_{OUT}$ feedback and the internal FB reference voltage. Figure 4 shows the buck work waveform.

Boost Mode ($V_{IN} < V_{OUT}$)

When the input voltage is significantly lower than the output voltage, the MP28167 works in boost mode. In boost mode, SWC and SWD switch for boost regulation, while SWB is off and SWA remains on to conduct the inductor current.

SWC remains off with constant-off-time in each period, while SWD turns on as a complement to SWC to boost the inductor current to output. In each cycle, SWC turns on to conduct the inductor current. When the inductor current reaches the COMP voltage, SWC turns off and SWD turns on. SWC turns off with one fixed off period before it turns on again. During this period, SWD turns on for the current freewheel. Figure 5 shows the boost work waveform.
**Buck-Boost Mode (VIN ≈ VOUT)**

When \( V_{IN} \) is close to \( V_{OUT} \), the converter may not be able to provide enough energy to work in buck mode due to SWA’s minimum off time, or the converter may supply too much power to \( V_{OUT} \) in boost mode due to SWC’s minimum on time. The MP28167 uses buck-boost control to regulate the output in these conditions.

In buck mode, if \( V_{IN} \) drops and the SWA off period is close to the buck minimum off time, buck-boost mode is engaged. When the next cycle starts after the SWA and SWD on period (buck HS-FET on period), boost starts with SWA and SWC on (boost LS-FET on). Then, SWA and SWD turn on again for the rest of the boost period (boost HS-FET on).

After the boost period elapses, the buck period starts and SWB and SWD remain on until the inductor current drops to the COMP voltage. Then SWA and SWD turn on next until the boost period starts. This repeated process in which the buck and boost switching work with one interval period is called buck-boost mode.

In boost mode, if \( V_{IN} \) rises and the SWC on period is close to the boost minimum on time, buck-boost mode is engaged. After the boost constant-off-time period (SWA and SWD on), SWB and SWD remain on until the inductor current signal drops to the COMP voltage, just like a buck off period control.

After the inductor current signal triggers the COMP voltage, SWA and SWD turn on for the buck on time, which is followed by one boost switching (SWA and SWC on), and buck and boost repeat switching work with one interval. Figure 6 shows the buck-boost waveform for both \( V_{IN} > V_{OUT} \) and \( V_{IN} < V_{OUT} \) conditions.

**Working Mode – FCCM (or Forced PWM) Mode**

The MP28167 works in forced PWM mode with fixed frequency. In FCCM conditions, the buck on time and boost off time are determined by an internal circuit to get a fixed frequency based on the \( V_{IN}/V_{OUT} \) ratio. When the load decreases, the average input current drops and the inductor current may go to negative from \( V_{OUT} \) to \( V_{IN} \) during the off time (SWD on). This forces the inductor current to work in continuous mode with fixed frequency, and can produce a lower \( V_{OUT} \) ripple.

**Internal VCC Regulator**

The 3.65V internal regulator powers most of the internal circuitries. This regulator takes \( V_{IN} \) and operates in the full \( V_{IN} \) range. When \( V_{IN} \) exceeds 3.65V, the output of the regulator is in full regulation. If \( V_{IN} \) is less than 3.65V, the output decreases with \( V_{IN} \). The VCC requires an external 1\( \mu \)F ceramic decoupling capacitor.

**Enable Control (EN)**

The MP28167 has an enable control (EN). Pull EN high to enable the IC. Pull EN low or float to disable the IC.

**Under-Voltage Lockout (UVLO)**

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage, and enables or disables the whole IC.
Internal Soft Start (SS)
The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 3.65V. When SS is lower than \( V_{\text{REF}} \), the error amplifier uses SS as the reference. When SS is higher than \( V_{\text{REF}} \), the error amplifier uses \( V_{\text{REF}} \) as the reference.

If the output of the MP28167 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage (see Figure 7).

![Figure 7: EN On to VOUT > 90% Delay](image)

Output Constant Current Limit (OCP)
The MP28167 has a constant current limit control loop to limit the output average current. The current information is sensed from switches A, B, C, and D. Then an average algorithm is used to calculate the output current.

When the output current exceeds the current-limit threshold, the output voltage starts to drop. If \( V_{\text{OUT}} \) drops below the under-voltage (UV) threshold (typically 50% below the reference), the MP28167 enters hiccup mode. The part stops switching and recovers automatically with 12.5% duty cycles.

Over-Voltage Protection (OVP)
The MP28167 monitors a resistor-divided feedback voltage to detect output over-voltage. When the feedback voltage exceeds 160% of the target voltage, the OVP comparator output goes high and the output to ground discharge resistor turns on.

The OUT pin has an absolute OVP function. Once the OUT voltage exceeds the absolute OVP threshold (23V), the MP28167 stops switching and turns on the output to ground discharge resistor.

Start-Up and Shutdown
If both \( V_{\text{IN}} \) and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Several events can shut down the chip: EN low, \( V_{\text{IN}} \) low, and thermal shutdown. In shutdown, the signaling path is blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rails are pulled down. The floating driver is not subject to this shutdown command.

Output Discharge
The MP28167 has an output discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO or EN is off), and the discharge path turns off when \( V_{\text{OUT}} < 50\text{mV} \) or the 50ms maximum timer is reached.

Thermal Shutdown (TSD)
Thermal shutdown prevents the part from operating at exceedingly high temperatures.

When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled. This is a non-latch protection.
APPLICATION INFORMATION

Component Selection

The Over-Current Limit Set (RSET)

The MP28167 current-limit value should be greater than the normal maximum load current, allowing the tolerances in the current-sense value. The current limit can be determined with Equation (1):

\[ R_{SET} (\text{k}\Omega) = \frac{75.24}{I_{\text{limit}(A)}} \]  

This also provides the theory result.

Table 1 lists the recommended ILIM setting resistor and capacitor values, based on the EVB.

<table>
<thead>
<tr>
<th>R_OC (kΩ)</th>
<th>C_OC (nF)</th>
<th>I_LIMIT (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>75</td>
<td>6.8</td>
<td>0.98</td>
</tr>
<tr>
<td>64.9</td>
<td>6.8</td>
<td>1.15</td>
</tr>
<tr>
<td>54.9</td>
<td>8.2</td>
<td>1.37</td>
</tr>
<tr>
<td>44.2</td>
<td>10</td>
<td>1.72</td>
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<tr>
<td>37.4</td>
<td>12</td>
<td>2.04</td>
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<td>15</td>
<td>2.54</td>
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<td>21.5</td>
<td>22</td>
<td>3.56</td>
</tr>
<tr>
<td>15</td>
<td>33</td>
<td>5.11</td>
</tr>
</tbody>
</table>

Selecting the Inductor

As one buck-boost topology circuit, the inductor must support buck applications with the maximum input voltage, and boost applications with the minimum input voltage. Two critical inductance values can be determined, according to the buck mode and boost mode current ripples, using Equation (2) and Equation (3):

\[ L_{\text{MIN-BUCK}} = \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{V_{\text{IN(MAX)}} \times f_{\text{REQ}} \times \Delta I_L} \]  

\[ L_{\text{MIN-BOOST}} = \frac{V_{\text{IN(MIN)}} \times (V_{\text{OUT}} - V_{\text{IN(MIN)}})}{V_{\text{OUT}} \times f_{\text{REQ}} \times \Delta I_L} \]  

Where \( f_{\text{REQ}} \) is the switching frequency and \( \Delta I_L \) is the peak-to-peak inductor current ripple. As a rule of thumb, the peak-to-peak ripple can be set at 10% to 40% of the inductor current. The minimum inductor value for the application must be higher than both the Equation (2) and Equation (3) results.

In addition to the inductance value, to avoid saturation, the inductor must support the peak current, based on Equation (4) and Equation (5):

\[ I_{\text{PEAK-BUCK}} = I_{\text{OUT}} + \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{2 \times V_{\text{IN(MAX)}} \times f_{\text{REQ}} \times L} \]  

\[ I_{\text{PEAK-BOOST}} = \frac{V_{\text{OUT}} \times I_{\text{OUT}} + V_{\text{IN(MIN)}} \times (V_{\text{OUT}} - V_{\text{IN(MIN)}})}{2 \times V_{\text{OUT}} \times f_{\text{REQ}} \times L} \]  

Where \( \eta \) is the estimated efficiency of the MP28167.

Input and Output Capacitor Selection

It is recommended to use ceramic capacitors plus electrolytic capacitors for the input and output capacitors, in order to filter input and output ripple current and obtain stable operation.

The input capacitor requires enough capacitance to absorb the input switching current. For most applications, a 100µF electrolytic capacitor plus a 22µF ceramic capacitor is sufficient.

The output capacitor stabilizes the DC output voltage. Low-ESR capacitors with enough capacitance to limit the output voltage ripple are preferred. Refer to application schematic for more detail.
PCB Layout Guidelines (9)

Efficient PCB layout is critical for successful operation and thermal dissipation. For best results, refer to Figure 8 and the guidelines below:

1. Place the ceramic $C_{\text{IN}}$ and $C_{\text{OUT}}$ capacitors close to the IC’s VIN-to-GND and OUT-to-GND pins, respectively.

2. Use a large copper plane for PGND. Add multiple vias to improve thermal dissipation. Connect AGND to PGND.

3. Use short, direct, and wide traces to connect OUT. Adding vias under the IC and then routing the OUT trace on both PCB layers is highly recommended.

4. Place a large copper plane for SW1, SW2.

5. Place the VCC decoupling capacitor as close to VCC as possible.

Note:

9) The recommended layout is based on the Typical Application Circuit on page 18.
TYPICAL APPLICATION CIRCUITS

Figure 9: Typical Application Circuit for 2.8V-22V IN, 5V OUT, 3A Output Current or 4A Input Current

Figure 10: Typical Application Circuit for 2.8V-22V IN, 5V OUT, 3A Output Current or 4A Input Current
PACKAGE INFORMATION

QFN-16 (3mmx3mm)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

NOTE:
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

RECOMMENDED LAND PATTERN

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