



# MP2710

## 500mA, 1-Cell, Li-Ion Battery Charger with Power-Path Management, 1mA Termination, <0.5 $\mu$ A Battery Leakage Current, I<sup>2</sup>C Interface

### DESCRIPTION

The MP2710 is a highly integrated, single-cell, Li-ion/Li-polymer battery charger with system power-path management (PPM) for space-restricted, portable applications. The MP2710 takes input power from either an AC adapter or a USB port to supply the system load and charge the battery simultaneously. The charger features pre-charge (PRE.C), fast current (CC) and constant voltage (CV) regulation, as well as charge termination, and auto-recharge.

The PPM function ensures continuous power to the system by automatically selecting the input, battery, or both to power the system. This function features a low-dropout (LDO) regulator from the input to the system and a 100m $\Omega$  switch from the battery to the system. PPM separates the charge current ( $I_{CHG}$ ) from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2710 provides system short-circuit protection (SCP) by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged due to an exceedingly high current. On-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage ( $V_{BATT}$ ) drops below the configurable battery UVLO threshold. This prevents the Li-ion battery from being over-discharged. An integrated I<sup>2</sup>C control interface allows the MP2710 to configure the charging parameters, such as the input current limit ( $I_{IN\_LIMIT}$ ), minimum input voltage regulation ( $V_{IN\_MIN}$ ),  $I_{CHG}$ , battery regulation voltage, safety timer, and battery UVLO.

The MP2710 is available in a WLCSP-9 (1.85mmx1.85mm) package.

### FEATURES

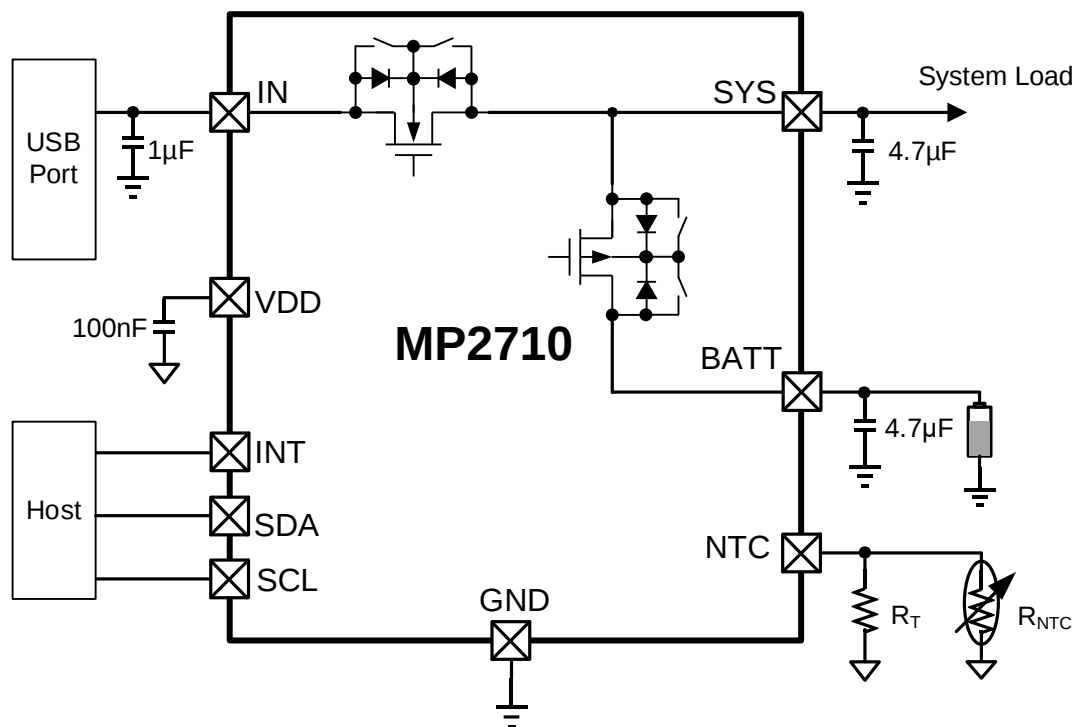
- 4.35V to 5.5V Operating Input Voltage ( $V_{IN}$ ) Range
- Up to 21V Sustainable  $V_{IN}$
- Configurable Charge Current ( $I_{CHG}$ ) from 8mA to 456mA with 2mA/step
- 1mA Termination Current
- $\pm 0.5\%$  Charge Voltage Accuracy
- 700 $\mu$ A Input Quiescent Current ( $I_{IN\_Q}$ )
- Low-Power Mode to Reduce Battery Consumption
- Configurable JEITA Profile for Battery Temperature Protection
- No Negative Temperature Coefficient (NTC) Resistor Divider Requirement to Save Battery Current ( $I_{BATT}$ )
- Dedicated Pin to Control Shipping Mode and System Reset
- Shipping Mode Entry via I<sup>2</sup>C or Analog Pin
- Shipping Mode Exit by  $V_{IN}$  Plug-In or Analog Pin
- <350nA Battery Leakage Current in Shipping Mode
- I<sup>2</sup>C Interface for Setting Charging Parameters and Status Reporting
- Built-In Robust Charging Protection:
  - Battery Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Watchdog Monitoring via the I<sup>2</sup>C
- Available in a WLCSP-9 (1.85mmx1.85mm) Package

### APPLICATIONS

- TWS Earbuds
- Fitness Accessories
- Internet of Things (IoT)
- Smartwatches

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# TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number*      | Package               | Top Marking | MSL Rating |
|-------------------|-----------------------|-------------|------------|
| MP2710GC-xxxx**   | WLCSP (1.85mmx1.85mm) | See Below   | 1          |
| MP2710GC-0000***  |                       |             |            |
| MP2710GC-0001**** |                       |             |            |
| EVKT-MP2710       | Evaluation kit        |             |            |

\* For Tape & Reel, add suffix -Z (e.g. MP2710GC-xxxx-Z).

\*\* “xxxx” is the register setting option. Contact an MPS FAE to obtain an “xxxx” value.

\*\*\* “0000” is the factory default for entering shipping mode by software. This content can be viewed in the I<sup>2</sup>C register map.

\*\*\*\* “0001” is the factory default for entering shipping mode by hardware.

## TOP MARKING

**MA**  
**Y**  
**LLL**

MA: Product code of MP2710GC

Y: Year code

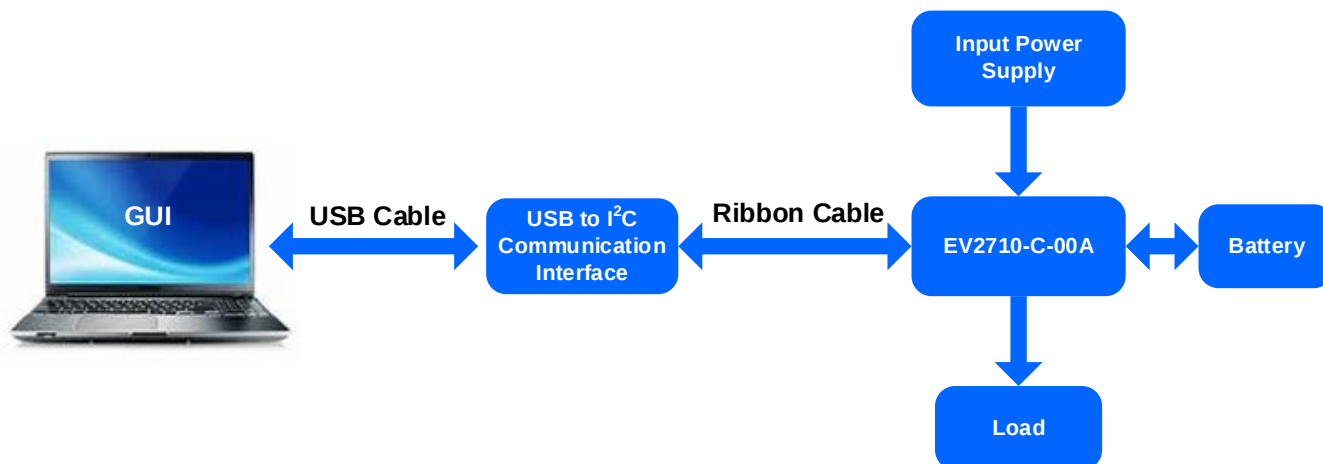
LLL: Lot number

## EVALUATION KIT EVKT-MP2710

EVKT-MP2710 kit contents (items below can be ordered separately):

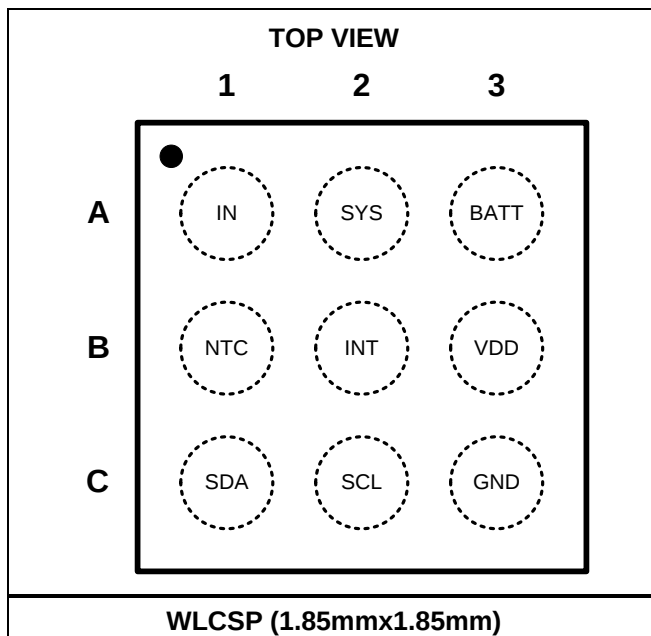
| # | Part Number         | Item                                                                                              | Quantity |
|---|---------------------|---------------------------------------------------------------------------------------------------|----------|
| 1 | EV2710-C-00A        | MP2710 evaluation board                                                                           | 1        |
| 2 | EVKT-USB2I2C-02-BAG | Includes one USB to I <sup>2</sup> C communication interface, one USB cable, and one ribbon cable | 1        |
| 3 | Online resources    | Include datasheet, user guide, product brief, and GUI                                             | 1        |

Order directly from [MonolithicPower.com](http://MonolithicPower.com) or our distributors.



**Figure 1: EVKT-MP2710 Evaluation Kit Set-Up**

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name | Description                                                                                                                                                                                                                                                                                                |
|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A1    | IN   | <b>Input power.</b> Connect a ceramic capacitor from IN to GND, placed as close to the IC as possible.                                                                                                                                                                                                     |
| A2    | SYS  | <b>System power supply.</b> Connect a ceramic capacitor from SYS to GND, placed as close to the IC as possible.                                                                                                                                                                                            |
| A3    | BATT | <b>Battery pin.</b> Connect a ceramic capacitor from BATT to GND, placed as close to the IC as possible.                                                                                                                                                                                                   |
| B1    | NTC  | <b>Temperature sense input.</b> Connect a negative temperature coefficient (NTC) thermistor to the NTC pin. Place a 91kΩ resistor in parallel with the thermistor to ensure that the NTC voltage (V <sub>NTC</sub> ) is within the operating range. If the NTC function is not used, remove this resistor. |
| B2    | INT  | <b>Interrupt output.</b> The INT pin sends a charging status and fault interrupt signal to the host. INT is also used to disconnect the system from the battery.                                                                                                                                           |
| B3    | VDD  | <b>Internal control power supply.</b> Connect a 100nF ceramic capacitor from VDD to GND. No external load is allowed.                                                                                                                                                                                      |
| C1    | SDA  | <b>I<sup>2</sup>C interface data.</b> Connect SDA to the logic rail using a 10kΩ resistor.                                                                                                                                                                                                                 |
| C2    | SCL  | <b>I<sup>2</sup>C interface clock.</b> Connect SCL to the logic rail using a 10kΩ resistor.                                                                                                                                                                                                                |
| C3    | GND  | <b>Ground.</b>                                                                                                                                                                                                                                                                                             |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

IN.....-0.3V to +21V  
SYS.....-0.3V to +5.3V (5.5V for 500μs)  
All other pins .....-0.3V to +6V  
Junction temperature (T<sub>J</sub>) .....150°C  
Lead temperature .....260°C  
Continuous power dissipation (T<sub>A</sub> = 25°C) <sup>(2)</sup>  
..... 0.88W  
Storage temperature ..... -65°C to +150°C

## ESD Ratings

Human body model (HBM) ..... 2000V  
Charged-device model (CDM).....750V

## Recommended Operating Conditions <sup>(3)</sup>

Input voltage (V<sub>IN</sub>) .....4.35V to 5.5V  
Input current (I<sub>IN</sub>).....Up to 500mA  
Discharge current (I<sub>DSCHG</sub>).....Up to 3.2A  
Charge current (I<sub>CHG</sub>) .....Up to 456mA  
Battery voltage (V<sub>BATT</sub>) ..... up to 4.545V  
Operating junction temp (T<sub>J</sub>) .... -40°C to +125°C

**Thermal Resistance <sup>(4)</sup>**      **θ<sub>JA</sub>**      **θ<sub>JC</sub>**  
WLCSP (1.85mmx1.85mm).... 114 ..... 12... °C/W

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) / θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on a JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

V<sub>IN</sub> = 5V, V<sub>BATT</sub> = 3.8V, T<sub>A</sub> = 25°C, unless otherwise noted.

| Parameter                                                                   | Symbol                   | Condition                                                                                                                | Min  | Typ  | Max  | Units |
|-----------------------------------------------------------------------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| <b>Input Source and Battery Protection</b>                                  |                          |                                                                                                                          |      |      |      |       |
| Input voltage (V <sub>IN</sub> ) under-voltage lock-out (UVLO) threshold    | V <sub>IN_UVLO</sub>     | V <sub>IN</sub> falling                                                                                                  | 3.15 | 3.25 | 3.35 | V     |
| V <sub>IN</sub> UVLO hysteresis                                             |                          | V <sub>IN</sub> rising                                                                                                   |      | 150  |      | mV    |
| V <sub>IN</sub> over-voltage protection (OVP) threshold                     | V <sub>IN_OVP</sub>      | V <sub>IN</sub> rising                                                                                                   | 5.85 | 6    | 6.15 | V     |
| V <sub>IN</sub> OVP hysteresis                                              |                          |                                                                                                                          |      | 350  |      | mV    |
| V <sub>IN</sub> vs. battery voltage (V <sub>BATT</sub> ) headroom threshold | V <sub>HDRM</sub>        | V <sub>IN</sub> rising vs. V <sub>BATT</sub>                                                                             | 80   | 130  | 170  | mV    |
| V <sub>IN</sub> vs. V <sub>BATT</sub> headroom hysteresis                   |                          |                                                                                                                          |      | 90   |      | mV    |
| Battery voltage <sup>(5)</sup>                                              | V <sub>BATT</sub>        |                                                                                                                          |      |      | 4.5  | V     |
| Battery UVLO threshold                                                      | V <sub>BATT_UVLO</sub>   | V <sub>BATT</sub> falling, REG01h[2:0] = 000                                                                             | 2.28 | 2.4  | 2.48 | V     |
|                                                                             |                          | V <sub>BATT</sub> falling, REG01h[2:0] = 100                                                                             | 2.66 | 2.76 | 2.86 | V     |
|                                                                             |                          | V <sub>BATT</sub> falling, REG01h[2:0] = 111                                                                             | 2.93 | 3.03 | 3.13 | V     |
| Battery UVLO hysteresis                                                     |                          | V <sub>BATT_UVLO</sub> = 2.76V                                                                                           |      | 190  |      | mV    |
| Battery OVP threshold                                                       | V <sub>BATT_OVP</sub>    | Rising, above V <sub>BATT_REG</sub>                                                                                      |      | 130  |      | mV    |
| Battery OVP hysteresis                                                      |                          |                                                                                                                          |      | 60   |      | mV    |
| <b>Power-Path Management (PPM)</b>                                          |                          |                                                                                                                          |      |      |      |       |
| Regulated system output voltage (V <sub>SYS_REG</sub> ) accuracy            | V <sub>SYS_REG_ACC</sub> | V <sub>IN</sub> = 5.5V, R <sub>SYS</sub> = 100Ω, I <sub>CHG</sub> = 0A, REG07h[3:0] = 0000, V <sub>SYS_REG</sub> = 4.2V  | 4.1  | 4.2  | 4.3  | V     |
|                                                                             |                          | V <sub>IN</sub> = 5.5V, R <sub>SYS</sub> = 100Ω, I <sub>CHG</sub> = 0A, REG07h[3:0] = 1001, V <sub>SYS_REG</sub> = 4.65V | 4.55 | 4.65 | 4.75 | V     |
|                                                                             |                          | V <sub>IN</sub> = 5.5V, R <sub>SYS</sub> = 100Ω, I <sub>CHG</sub> = 0A, REG07h[3:0] = 1111, V <sub>SYS_REG</sub> = 4.95V | 4.85 | 4.95 | 5.05 | V     |
| Input current (I <sub>IN</sub> ) limit                                      | I <sub>IN_LIMIT</sub>    | REG00h[3:0] = 0000, I <sub>IN_LIMIT</sub> = 50mA                                                                         | 30   | 40   | 50   | mA    |
|                                                                             |                          | REG00h[3:0] = 0011, I <sub>IN_LIMIT</sub> = 140mA                                                                        | 112  | 126  | 140  | mA    |
|                                                                             |                          | REG00h[3:0] = 1001, I <sub>IN_LIMIT</sub> = 320mA                                                                        | 275  | 300  | 320  | mA    |
|                                                                             |                          | REG00h[3:0] = 1111, I <sub>IN_LIMIT</sub> = 500mA                                                                        | 440  | 470  | 500  | mA    |
| Minimum Input Voltage Regulation                                            | V <sub>IN_MIN</sub>      | REG00h[7:4] = 0000, V <sub>IN_REG</sub> = 3.88V                                                                          | 3.68 | 3.88 | 4.18 | V     |
|                                                                             |                          | REG00h[7:4] = 0110, V <sub>IN_REG</sub> = 4.36V                                                                          | 4.1  | 4.36 | 4.62 | V     |
|                                                                             |                          | REG00h[7:4] = 1001, V <sub>IN_REG</sub> = 4.6V                                                                           | 4.34 | 4.6  | 4.86 | V     |
|                                                                             |                          | REG00h[7:4] = 1111, V <sub>IN_REG</sub> = 5.08V                                                                          | 4.88 | 5.08 | 5.35 | V     |
| IN to SYS turn-on resistance                                                | R <sub>ON_Q1</sub>       | V <sub>IN</sub> = 5V, I <sub>SYS</sub> = 100mA                                                                           |      | 290  |      | mΩ    |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 5V, V<sub>BATT</sub> = 3.8V, T<sub>A</sub> = 25°C, unless otherwise noted.

| Parameter                                      | Symbol                | Condition                                                                                                                                                                  | Min | Typ                 | Max | Units |
|------------------------------------------------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------------------|-----|-------|
| Input quiescent current                        | I <sub>IN_Q</sub>     | V <sub>IN</sub> = 5V, EN_HIZ = 0, CE = low, charging enabled, I <sub>CHG</sub> = 0A, I <sub>SYS</sub> = 0A                                                                 |     | 700                 | 780 | μA    |
|                                                |                       | V <sub>IN</sub> = 5V, EN_HIZ = 0, CE = high, charging disabled                                                                                                             |     | 450                 | 520 | μA    |
|                                                |                       | V <sub>IN</sub> = 5V, EN_HIZ = 1                                                                                                                                           |     | 150                 | 200 | μA    |
| Battery quiescent current                      | I <sub>BATT_Q</sub>   | V <sub>IN</sub> = 5V, CE = L, I <sub>SYS</sub> = 0A, charging complete, V <sub>BATT</sub> = 4.35V                                                                          |     | 15                  | 20  | μA    |
|                                                |                       | V <sub>IN</sub> = GND, CE = H, I <sub>SYS</sub> = 0A, V <sub>BATT</sub> = 4.35V, low-power mode: NTC disabled, BATTOCP disabled, INT interrupt disabled, watchdog disabled |     | 1.5                 | 3   | μA    |
|                                                |                       | V <sub>IN</sub> = GND, CE = H, I <sub>SYS</sub> = 0A, V <sub>BATT</sub> = 4.35V, active mode, NTC disabled, watchdog disabled                                              |     | 7.2                 | 8.2 | μA    |
|                                                |                       | V <sub>IN</sub> = GND, CE = H, I <sub>SYS</sub> = 0A, V <sub>BATT</sub> = 4.35V, active mode, NTC disabled, watchdog enabled                                               |     | 15                  |     | μA    |
|                                                |                       | V <sub>BATT</sub> = 4.5V, V <sub>IN</sub> = V <sub>SYS</sub> = GND, shipping mode                                                                                          |     |                     | 350 | nA    |
| Battery FET on resistance                      | R <sub>ON_Q2</sub>    | V <sub>IN</sub> < 2V, V <sub>BATT</sub> = 3.5V, I <sub>SYS</sub> = 100mA                                                                                                   |     | 100                 |     | mΩ    |
| Battery FET discharge current limit            | I <sub>DSCHG</sub>    | REG0Dh[3:0] = 0001, I <sub>DSCHG</sub> = 400mA                                                                                                                             | 370 | 490                 | 585 | mA    |
|                                                |                       | REG0Dh[3:0] = 1001, I <sub>DSCHG</sub> = 2000mA                                                                                                                            |     | 2400 <sup>(5)</sup> |     |       |
| SYS reverse to BATT switch leakage             |                       | V <sub>SYS</sub> = 4.65V, V <sub>IN</sub> = 5V, V <sub>BATT</sub> = GND, EN_HIZ = 1, CE = H, charging disabled                                                             |     |                     | 100 | nA    |
| Ideal diode forward voltage in supplement mode | V <sub>FWD</sub>      | I <sub>DSCHG</sub> = 50mA                                                                                                                                                  |     | 30                  |     | mV    |
| Shipping Mode                                  |                       |                                                                                                                                                                            |     |                     |     |       |
| Enter shipping mode deglitch time              | t <sub>ESM_DGL</sub>  | REG06h[5] is set from 0 to 1, REG0Ah[5:4] = 00                                                                                                                             |     | 1                   |     | sec   |
| Exit shipping mode deglitch time               | t <sub>EXSM_DGL</sub> | Exit shipping mode by V <sub>IN</sub> plug-in, REG0Ah[2] = 0                                                                                                               |     | 80                  |     | ms    |
|                                                |                       | Exit shipping mode by pulling INT low                                                                                                                                      |     | 2                   |     | sec   |
| Auto-Reset Mode                                |                       |                                                                                                                                                                            |     |                     |     |       |
| Reset deglitch by INT                          | t <sub>RST_DGL</sub>  | REG01h[7:6] = 00                                                                                                                                                           |     | 8                   |     | sec   |
|                                                |                       | REG01h[7:6] = 10                                                                                                                                                           |     | 16                  |     | sec   |
| Battery FET off duration                       | t <sub>RST_DUR</sub>  | REG01h[5] = 0                                                                                                                                                              |     | 2                   |     | sec   |
|                                                |                       | REG01h[5] = 1                                                                                                                                                              |     | 4                   |     | sec   |

**ELECTRICAL CHARACTERISTICS (continued)****V<sub>IN</sub> = 5V, V<sub>BATT</sub> = 3.8V, T<sub>A</sub> = 25°C, unless otherwise noted.**

| Parameter                                                        | Symbol                | Condition                                                                         | Min   | Typ  | Max   | Units |
|------------------------------------------------------------------|-----------------------|-----------------------------------------------------------------------------------|-------|------|-------|-------|
| <b>Battery Charger</b>                                           |                       |                                                                                   |       |      |       |       |
| Battery charging regulation voltage                              | V <sub>BATT_REG</sub> | REG04h[7:2] = 000000, V <sub>BATT_REG</sub> = 3.6V, T <sub>A</sub> = 0°C to 85°C  | 3.578 | 3.6  | 3.622 | V     |
|                                                                  |                       | REG04h[7:2] = 101000, V <sub>BATT_REG</sub> = 4.2V                                | 4.179 | 4.2  | 4.221 | V     |
|                                                                  |                       | REG04h[7:2] = 101000, V <sub>BATT_REG</sub> = 4.2V, T <sub>A</sub> = 0°C to 85°C  | 4.175 | 4.2  | 4.225 | V     |
|                                                                  |                       | REG04h[7:2] = 110010, V <sub>BATT_REG</sub> = 4.38V, T <sub>A</sub> = 0°C to 85°C | 4.354 | 4.38 | 4.404 | V     |
|                                                                  |                       | REG04h[7:2] = 111110, V <sub>BATT_REG</sub> = 4.53V, T <sub>A</sub> = 0°C to 85°C | 4.506 | 4.53 | 4.556 | V     |
| Fast-charge current                                              | I <sub>CC</sub>       | REG02h[7:0] = 00000000, I <sub>CC</sub> = 8mA                                     | 7.6   | 8    | 8.6   | mA    |
|                                                                  |                       | REG02h[7:0] = 00011100, I <sub>CC</sub> = 58mA                                    | 53    | 58   | 63    | mA    |
|                                                                  |                       | REG02h[7:0] = 00110000, I <sub>CC</sub> = 98mA                                    | 91    | 98   | 105   | mA    |
|                                                                  |                       | REG02h[7:0] = 10000011, I <sub>CC</sub> = 264mA                                   | 246   | 264  | 280   | mA    |
|                                                                  |                       | REG02h[7:0] = 11100011, I <sub>CC</sub> = 456mA                                   | 420   | 456  | 484   | mA    |
| Pre-charge current                                               | I <sub>PRE</sub>      | REG03h[7:4] = 0000, I <sub>PRE</sub> = 1mA                                        | 0.82  | 1.08 | 1.37  | mA    |
|                                                                  |                       | REG03h[7:4] = 0001, I <sub>PRE</sub> = 3mA                                        | 2.55  | 3    | 3.45  | mA    |
|                                                                  |                       | REG03h[7:4] = 0101, I <sub>PRE</sub> = 11mA                                       | 9.8   | 11   | 12.2  | mA    |
|                                                                  |                       | REG03h[7:4] = 1111, I <sub>PRE</sub> = 31mA                                       | 28    | 31   | 34    | mA    |
| Charge termination current threshold                             | I <sub>TERM</sub>     | REG03h[3:0] = 0000, I <sub>TERM</sub> = 1mA                                       | 0.82  | 1.08 | 1.37  | mA    |
|                                                                  |                       | REG03h[3:0] = 0001, I <sub>TERM</sub> = 3mA                                       | 2.55  | 3    | 3.45  | mA    |
|                                                                  |                       | REG03h[3:0] = 0101, I <sub>TERM</sub> = 11mA                                      | 9.8   | 11   | 12.2  | mA    |
|                                                                  |                       | REG03h[3:0] = 1111, I <sub>TERM</sub> = 31mA                                      | 28    | 31   | 34    | mA    |
| Termination deglitch time                                        | t <sub>TERM_DGL</sub> |                                                                                   |       | 3.2  |       | sec   |
| Pre-charge to fast charge threshold                              | V <sub>BATT_PRE</sub> | V <sub>BATT</sub> rising, REG05h[0] = 1, V <sub>BATT_PRE</sub> = 3V               | 2.9   | 3    | 3.1   | V     |
| Pre-charge to fast charge hysteresis                             |                       |                                                                                   |       | 90   |       | mV    |
| Battery auto-recharge threshold                                  | V <sub>RECH</sub>     | Below V <sub>BATT_REG</sub> , REG04h[0] = 0                                       | 60    | 100  | 140   | mV    |
|                                                                  |                       | Below V <sub>BATT_REG</sub> , REG04h[0] = 1                                       | 160   | 200  | 240   |       |
| Battery auto-recharge delay time                                 | t <sub>RECH_DGL</sub> |                                                                                   |       | 200  |       | ms    |
| <b>Thermal Protection</b>                                        |                       |                                                                                   |       |      |       |       |
| Junction temperature (T <sub>J</sub> ) regulation <sup>(5)</sup> | T <sub>J_REG</sub>    | THERMAL_LIMIT = 120°C                                                             |       | 120  |       | °C    |
| Thermal shutdown threshold <sup>(5)</sup>                        | T <sub>SD</sub>       |                                                                                   |       | 150  |       | °C    |
| Thermal shutdown hysteresis <sup>(5)</sup>                       |                       |                                                                                   |       | 20   |       | °C    |
| NTC bias current                                                 | I <sub>NTC</sub>      |                                                                                   | 48.4  | 50   | 51    | μA    |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 5V, T<sub>A</sub> = 25°C, unless otherwise noted.

| Parameter                                  | Symbol              | Condition               | Min  | Typ  | Max  | Units |
|--------------------------------------------|---------------------|-------------------------|------|------|------|-------|
| NTC cold temperature rising threshold      | V <sub>COLD</sub>   |                         | 1040 | 1050 | 1060 | mV    |
| NTC cold temperature rising hysteresis     |                     |                         |      | 20   |      | mV    |
| NTC cooler temperature rising threshold    | V <sub>COOLER</sub> |                         | 743  | 751  | 759  | mV    |
| NTC cooler temperature rising hysteresis   |                     |                         |      | 25   |      | mV    |
| NTC cool temperature rising threshold      | V <sub>COOL</sub>   |                         | 625  | 632  | 639  | mV    |
| NTC cool temperature rising hysteresis     |                     |                         |      | 25   |      | mV    |
| NTC warm temperature falling threshold     | V <sub>WARM</sub>   |                         | 228  | 233  | 238  | mV    |
| NTC warm temperature falling hysteresis    |                     |                         |      | 25   |      | mV    |
| NTC hot temperature falling threshold      | V <sub>HOT</sub>    |                         | 193  | 199  | 205  | mV    |
| NTC hot temperature falling hysteresis     |                     |                         |      | 25   |      | mV    |
| <b>Logic I/O Pin Characteristics</b>       |                     |                         |      |      |      |       |
| Logic low voltage                          | V <sub>L</sub>      |                         |      |      | 0.4  | V     |
| Logic high voltage                         | V <sub>H</sub>      |                         | 1.3  |      |      | V     |
| <b>I<sup>2</sup>C Interface (SDA, SCL)</b> |                     |                         |      |      |      |       |
| Input high voltage                         | V <sub>IH</sub>     |                         | 1.3  |      |      | V     |
| Input low voltage                          | V <sub>IL</sub>     |                         |      |      | 0.4  | V     |
| Output low voltage                         | V <sub>OL</sub>     | I <sub>SINK</sub> = 5mA |      |      | 0.4  | V     |
| I <sup>2</sup> C clock frequency           | f <sub>SCL</sub>    |                         |      |      | 400  | kHz   |
| <b>Clock Frequency and Watchdog Timer</b>  |                     |                         |      |      |      |       |
| Clock frequency                            | f <sub>CLK</sub>    |                         |      | 131  |      | kHz   |
| Watchdog timer                             | t <sub>WDT</sub>    | REG05h[6:5] = 11        |      | 160  |      | sec   |

**Note:**

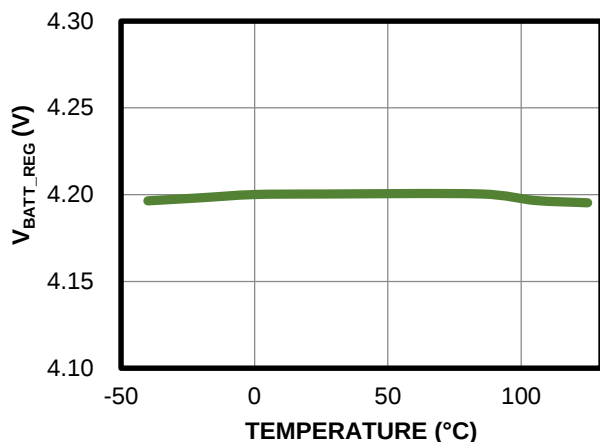
5) Guaranteed by design.

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5V$ ,  $I_{IN\_LIMIT} = 500mA$ ,  $I_{CC} = 128mA$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

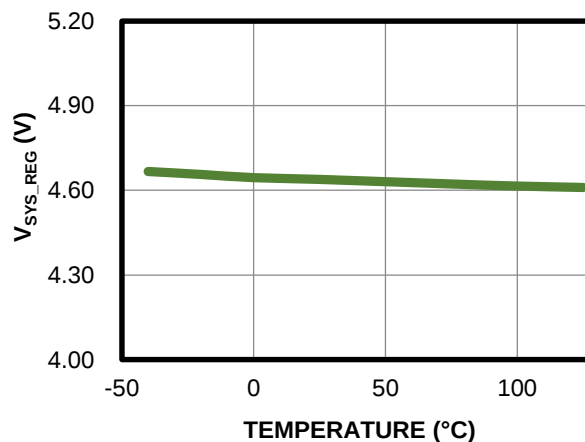
**Battery Regulation Voltage vs. Temperature**

$V_{BATT\_REG} = 4.2V$

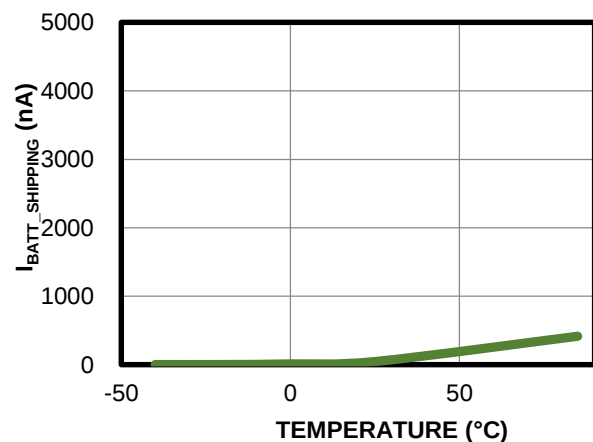


**System Regulation Voltage vs. Temperature**

$V_{SYS\_REG} = 4.65V$

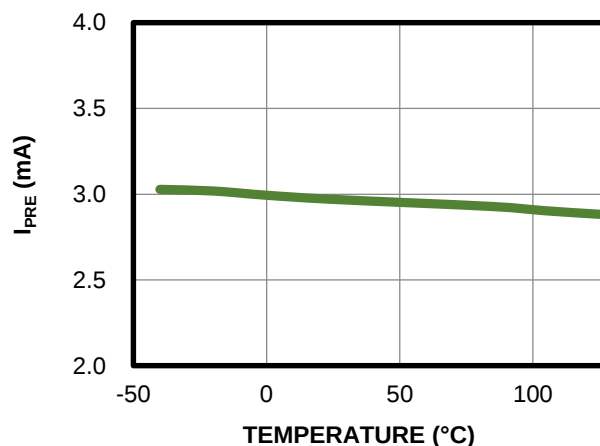


**Battery Current in Shipping Mode vs. Temperature**



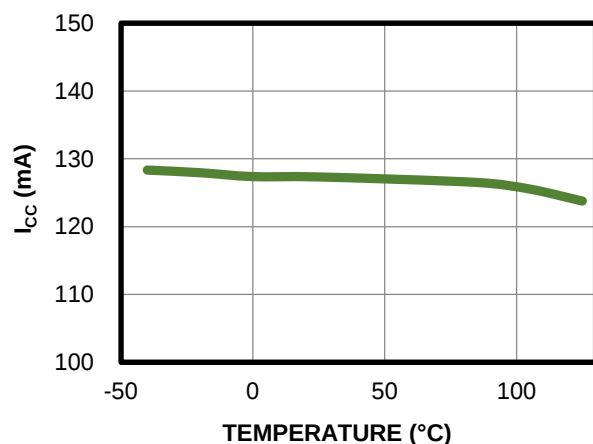
**Pre-Charge Current vs. Temperature**

$I_{PRE} = 3mA$



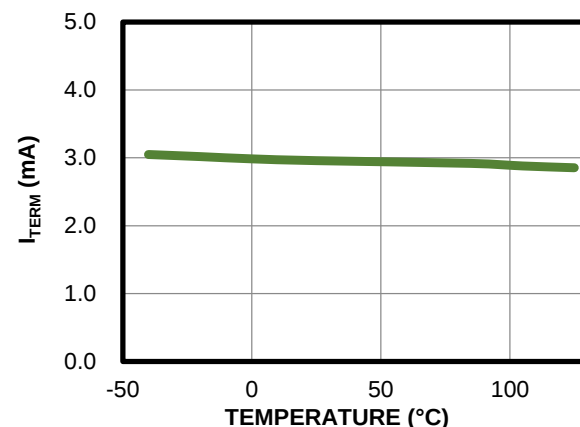
**Fast-Charge Current vs. Temperature**

$I_{CC} = 128mA$



**Battery Termination Current vs. Temperature**

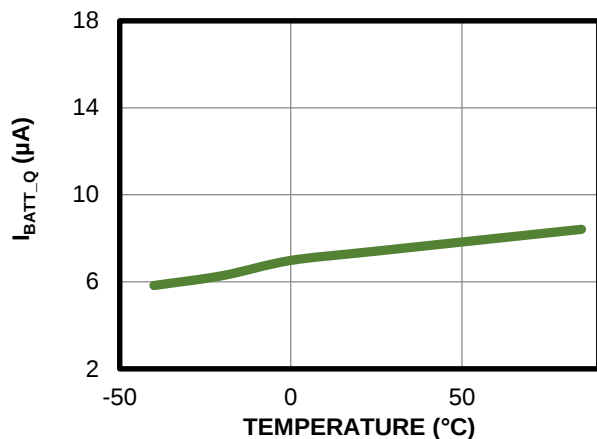
$I_{TERM} = 3mA$



# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

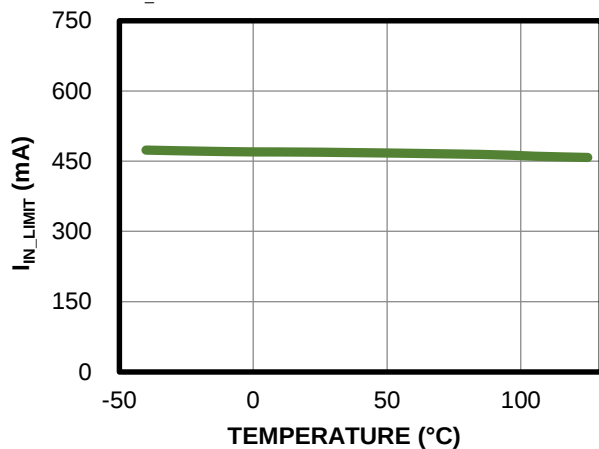
$V_{IN} = 5V$ ,  $I_{IN\_LIMIT} = 500mA$ ,  $I_{CC} = 128mA$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

**Battery Quiescent Current vs. Temperature**



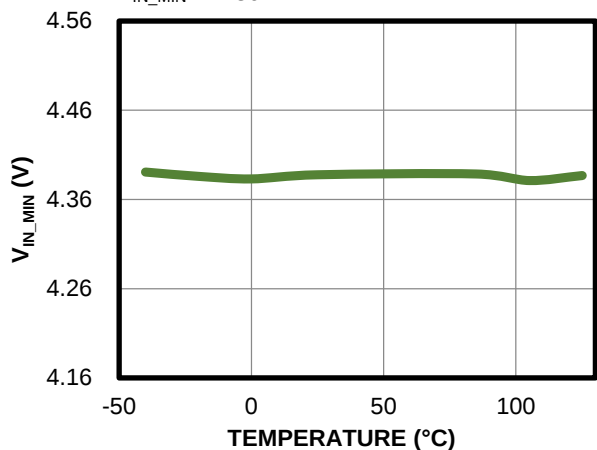
**Input Current Limit vs. Temperature**

$I_{IN\_LIMIT} = 500mA$



**Minimum Input Voltage vs. Temperature**

$V_{IN\_MIN} = 4.36V$



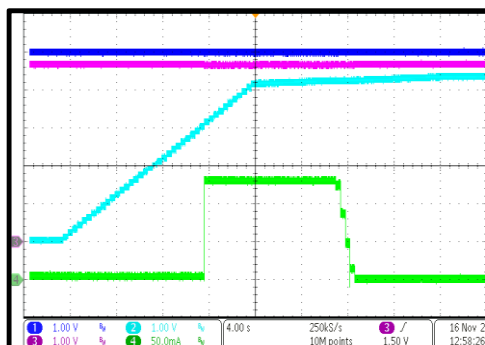
# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 5V$ ,  $I_{IN\_LIMIT} = 500mA$ ,  $I_{CC} = 128mA$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

## Battery Charge Curve

$I_{SYS} = 0A$

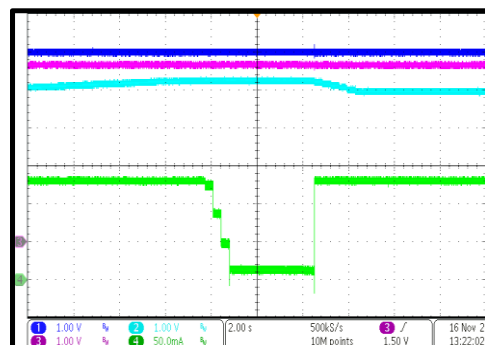
CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$



## Auto-Recharge

$I_{SYS} = 0A$

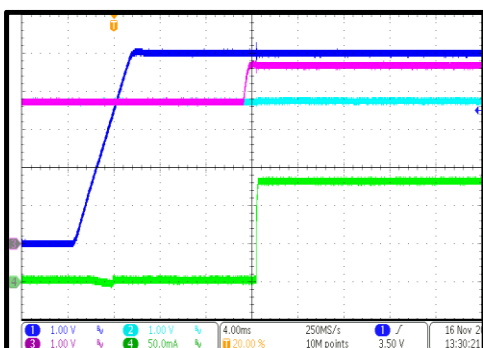
CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$



## Start-Up

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

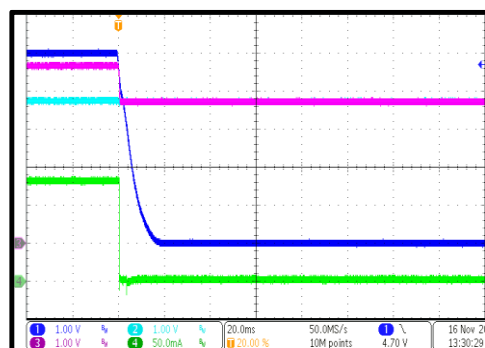
CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$



## Shutdown

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

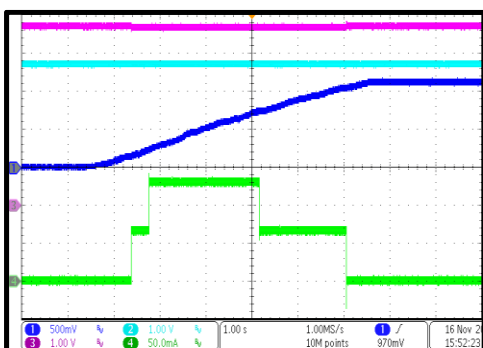
CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$



## NTC Rising

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

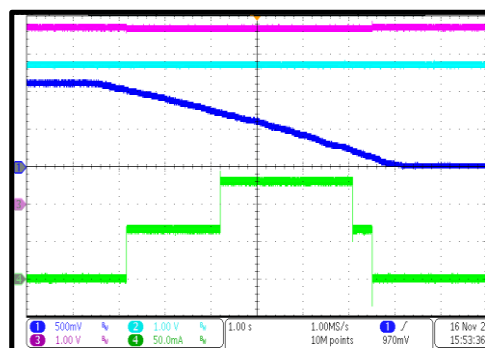
CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$



## NTC Falling

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$



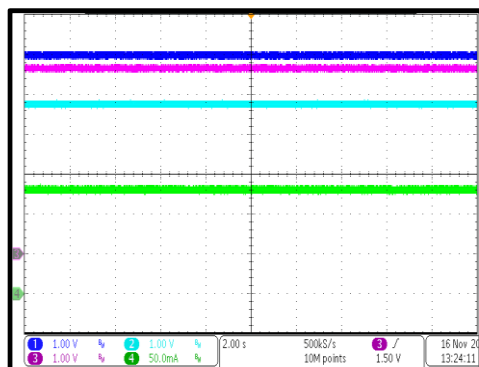
# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 5V$ ,  $I_{IN\_LIMIT} = 500mA$ ,  $I_{CC} = 128mA$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

## CC Charge Steady State

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$

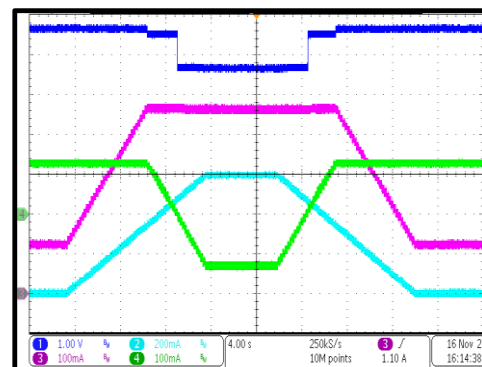


## Input Current Limit-Based PPM

$V_{BATT} = 3.7V$

CH4:  $I_{BATT}$

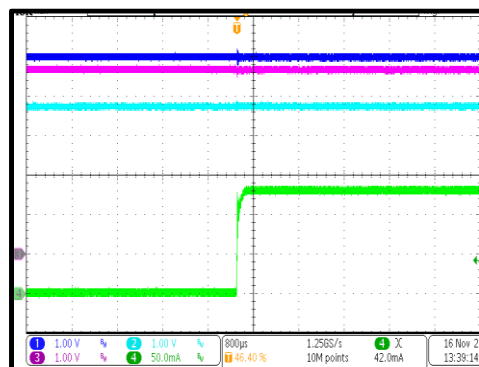
CH1:  $V_{SYS}$   
CH2:  $I_{SYS}$   
CH3:  $I_{IN}$



## Charge Enabled

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

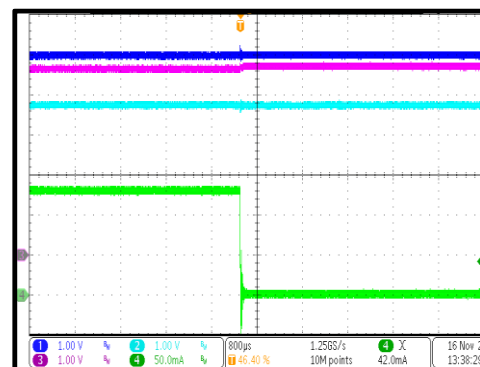
CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$



## Charge Disabled

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

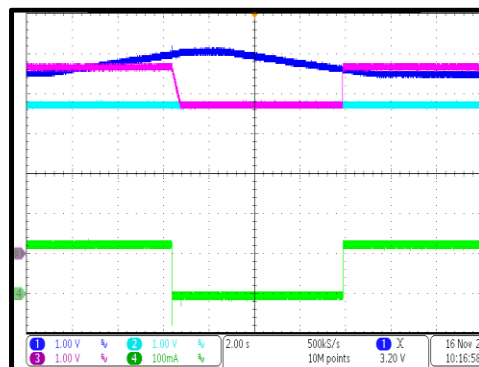
CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$



## $V_{IN}$ OVP

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

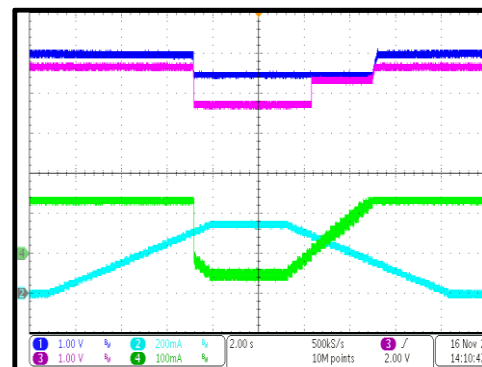
CH1:  $V_{IN}$   
CH2:  $V_{BATT}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$



## $V_{IN}$ Regulation-Based PPM

$V_{IN} = 5V/300mA$ ,  $V_{BATT} = 3.7V$

CH1:  $V_{IN}$   
CH3:  $V_{SYS}$   
CH4:  $I_{BATT}$   
CH2:  $I_{SYS}$



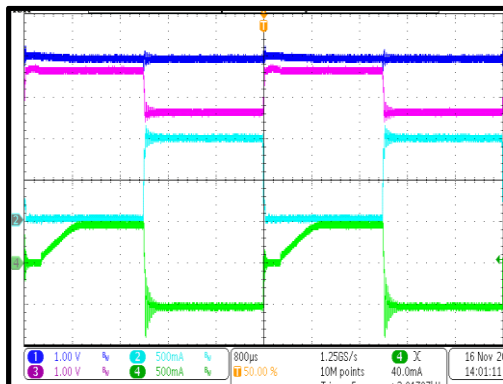
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 5V$ ,  $I_{IN\_LIMIT} = 500mA$ ,  $I_{CC} = 128mA$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

## SYS Load Transient

$V_{IN} = 5V$ ,  $V_{BATT} = 3.7V$ ,  $I_{CC} = 456mA$ ,  
 $I_{SYS} = 0A$  to  $1A$

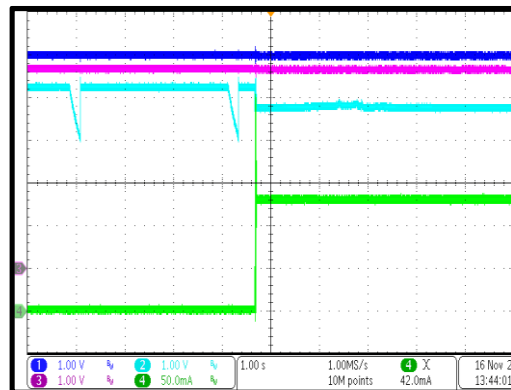
CH1:  $V_{IN}$   
 CH2:  $I_{SYS}$   
 CH3:  $V_{SYS}$   
 CH4:  $I_{BATT}$



## Battery Insertion

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

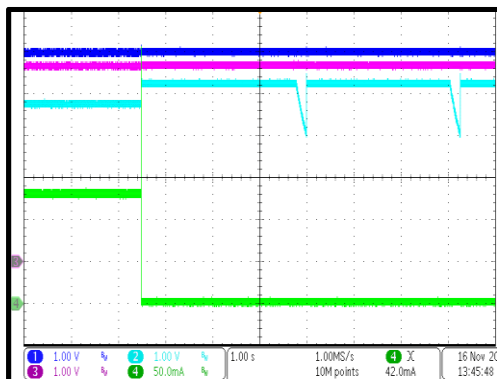
CH1:  $V_{IN}$   
 CH2:  $V_{BATT}$   
 CH3:  $V_{SYS}$   
 CH4:  $I_{BATT}$



## Battery Removal

$V_{BATT} = 3.7V$ ,  $I_{SYS} = 0A$

CH1:  $V_{IN}$   
 CH2:  $V_{BATT}$   
 CH3:  $V_{SYS}$   
 CH4:  $I_{BATT}$



## FUNCTIONAL BLOCK DIAGRAM

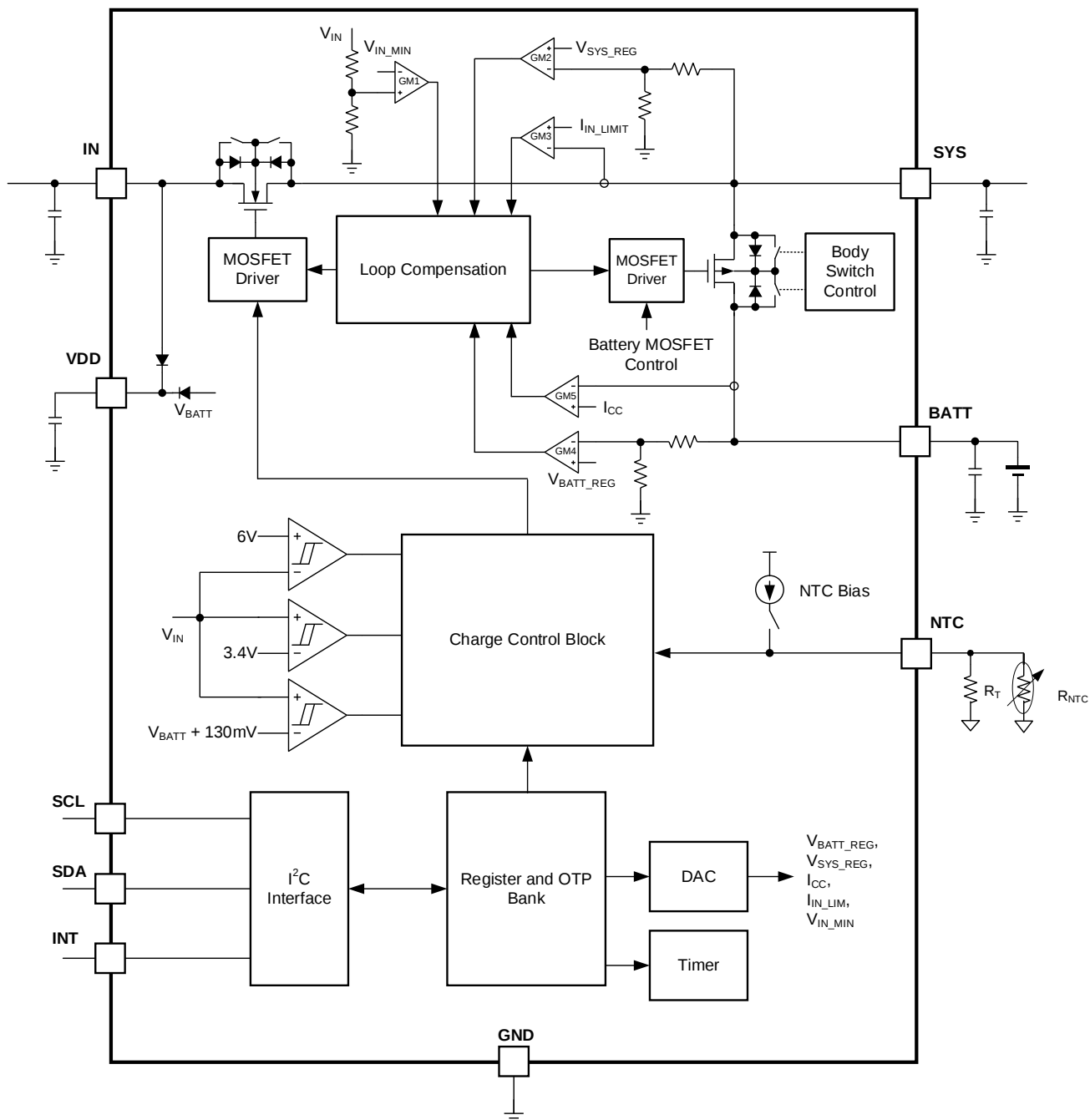


Figure 2: Functional Block Diagram

## OPERATION

The MP2710 is an I<sup>2</sup>C-controlled, single-cell, Li-ion/Li-polymer battery charger with complete power-path management (PPM). The full charging function includes constant current pre-charge, constant current fast charge (CC), and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in timer. PPM allows the input source to power the system and charge the battery simultaneously. The system load requirement always takes priority over the charge current ( $I_{CHG}$ ). When the input power is limited due to an input current limit ( $I_{IN\_LIMIT}$ ) or input voltage ( $V_{IN}$ ) limit, the IC reduces  $I_{CHG}$  automatically until the battery supplements the system load.

The IC integrates a 290mΩ low-dropout (LDO) MOSFET between the IN and SYS pins, as well as a 100mΩ battery MOSFET between the SYS and BATT pins.

In charge mode, the on-chip, 100mΩ battery MOSFET works as a fully featured linear charger with pre-charge, fast charge, CV charge, charge termination, auto-recharge, NTC monitoring, built-in timer control, and thermal protection.  $I_{CHG}$  can be configured via the I<sup>2</sup>C interface. The IC adjusts  $I_{CHG}$  when the die temperature exceeds the thermal regulation threshold (120°C by default).

In supplement mode, the 100mΩ battery MOSFET turns on to connect the battery to the system load while the input power is not sufficient to power the system load. When the input is removed, the 100mΩ battery MOSFET turns on fully to allow the battery to start up the system.

The system load is satisfied first, and then the remaining current is used to charge the smart PPM battery. The MP2710 reduces  $I_{CHG}$  or uses power from the battery to satisfy the system load when its demand exceeds the input power capacity.

If the battery is connected and the input source is missing, the IC operates in battery discharge mode; the low, 100mΩ battery MOSFET and low-power mode reduce battery current consumption.

Figure 3 shows PPM for the MP2710.

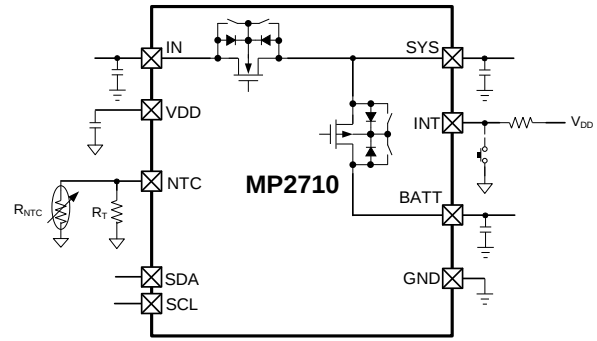


Figure 3: Power Path Management

Table 1 on page 17 shows the functions that are active for each operation mode. Each mode is discussed in detail in the following sections.

### Power Supply

The IC's internal bias circuit is powered from either IN or BATT, whichever has the higher voltage. When the IN voltage ( $V_{IN}$ ) or the BATT voltage ( $V_{BATT}$ ) exceeds its respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and battery MOSFET driver are active. The I<sup>2</sup>C interface is ready for communication, and all registers are reset to the default value. The host can access all of the registers.

### Input Over-Voltage Protection (OVP) and Under-Voltage Lockout (UVLO)

The MP2710 has an input over-voltage protection (OVP) threshold and an input UVLO threshold ( $V_{IN\_UVLO}$ ). When  $V_{IN}$  drops below  $V_{IN\_UVLO}$  or exceeds  $V_{IN\_OVP}$ , the LDO MOSFET (Q1) turns off immediately.

When  $V_{IN}$  is identified as a good source, a 10ms glitch filter becomes active. If  $V_{IN}$  is normal for 10ms, the system starts up; otherwise, Q1 remains off (see Figure 4).

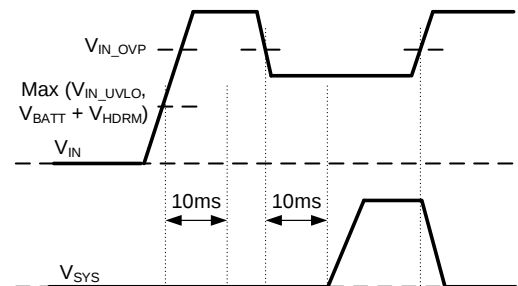


Figure 4: Input Power Detection

**Table 1: Function Availability in Different Operation Modes**

| Function                                       | Charge Mode | Battery Discharge Mode | Low-Power Mode | Shipping Mode |
|------------------------------------------------|-------------|------------------------|----------------|---------------|
| V <sub>IN</sub> OVP                            | Yes         | No                     | No             | No            |
| V <sub>IN</sub> UVLO                           | Yes         | No                     | No             | No            |
| Battery OCP                                    | Yes         | Yes                    | No             | No            |
| Battery UVLO                                   | Yes         | Yes                    | Yes            | No            |
| V <sub>IN</sub> dynamic power management (DPM) | If enabled  | No                     | No             | No            |
| I <sub>IN</sub> DPM                            | Yes         | No                     | No             | No            |
| Battery MOSFET                                 | Yes         | Yes                    | Yes            | No            |
| NTC                                            | If enabled  | No                     | No             | No            |
| Charging                                       | If enabled  | No                     | No             | No            |
| INT input                                      | Yes         | Yes                    | Yes            | Yes           |
| INT output                                     | Yes         | Yes                    | No             | No            |
| I <sup>2</sup> C                               | Yes         | Yes                    | Yes            | No            |
| Watchdog                                       | If enabled  | If enabled             | No             | No            |

### Power Path Management (PPM)

The MP2710 employs a power path structure consisting of a front-end LDO MOSFET (Q1) between the IN and SYS pins and a battery MOSFET (Q2) between the SYS and BATT pins. The battery MOSFET decouples the system from the battery, which allows for separate control between the system and the battery. The system has the priority to start up, even with a deeply discharged or missing battery. When input power is available, the system voltage (V<sub>SYS</sub>) is regulated to the regulated system output voltage (V<sub>SYS\_REG</sub>), which can be configured by register 07h, bits[3:0]. The LDO MOSFET and battery MOSFET can also be controlled via the I<sup>2</sup>C (see Table 2).

**Table 2: MOSFET Control via the I<sup>2</sup>C**

| MOSFET On/Off                | Hi-Z Mode and Charge Control |             |
|------------------------------|------------------------------|-------------|
|                              | Set EN_HIZ = 1               | Set CEB = 1 |
| LDO MOSFET                   | Off                          | X           |
| Battery MOSFET (charging)    | X                            | Off         |
| Battery MOSFET (discharging) | X                            | X           |

**Note:**

6) “X” means not affected by I<sup>2</sup>C control.

For V<sub>SYS</sub> control when V<sub>IN</sub> exceeds V<sub>SYS\_REG</sub>, V<sub>SYS</sub> is regulated to V<sub>SYS\_REG</sub>. When V<sub>IN</sub> is below V<sub>SYS\_REG</sub>, the LDO FET is fully on with I<sub>IN\_LIMIT</sub>.

### Battery Charge Profile

The MP2710 provides three main charging phases: pre-charge (PRE.C), fast-current (CC) charge, and constant-voltage (CV) charge (see Figure 5 on page 18).

1. **Phase 1 (pre-charge):** The MP2710 can safely pre-charge a deeply depleted battery until V<sub>BATT</sub> reaches the pre-charge to fast-charge threshold (V<sub>BATT\_PRE</sub>). The pre-charge current (I<sub>PRE</sub>) can be configured via REG03h, bits[7:4]. If V<sub>BATT</sub> does not reach V<sub>BATT\_PRE</sub> before the pre-charge timer (1hr) expires, the charge cycle stops, and a corresponding timeout fault signal is asserted.
2. **Phase 2 (fast charge):** When V<sub>BATT</sub> exceeds V<sub>BATT\_PRE</sub>, the MP2710 enters the fast-charge phase. The fast-charge current (I<sub>CC</sub>) can be configured via REG02h, bits[7:0].
3. **Phase 3 (constant-voltage charge):** When V<sub>BATT</sub> rises to the battery full voltage (V<sub>BATT\_REG</sub>) set via REG04h, bits[7:2], the charge mode changes from CC mode to CV mode, and I<sub>CHG</sub> decreases. Note that V<sub>SYS</sub> should exceed V<sub>BATT</sub> by at least 140mV when I<sub>CC</sub> is below 200mA.

The charge cycle completes when I<sub>CHG</sub> reaches the termination current threshold after a 3.2s termination deglitch time. The termination charge current threshold can be configured via register REG03h, bits[3:0].

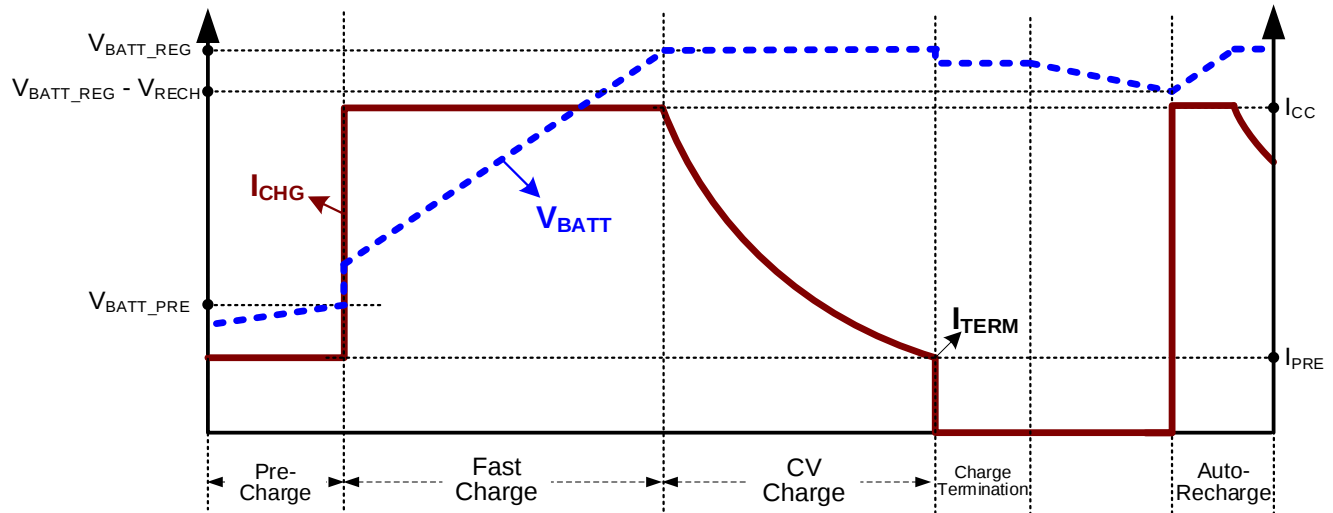


Figure 5: Battery Charge Profile

During the entire charging process, the actual  $I_{CHG}$  may be below the register setting due to other loop regulations, such as  $V_{IN}$  or  $I_{IN}$  dynamic power management (DPM) regulation or thermal regulation.

A new charge cycle starts when any of the following conditions are valid:

- The input power is recycled.
- Battery charging is enabled via the I<sup>2</sup>C.
- Auto-recharge kicks in.

Under the following conditions:

- No thermistor fault at NTC.
- No safety timer fault.
- No battery over-voltage (OV) event.
- The BATT FET is not forced off.

### Automatic Recharge

When a charge cycle completes, the battery may be discharged due to system consumption or self-discharge. When  $V_{BATT}$  discharges to below the recharge threshold and a valid input is still present, the MP2710 begins a new charging cycle automatically.

### Battery Over-Voltage Protection (OVP)

The MP2710 features a built-in battery OV limit (about 130mV above  $V_{BATT\_REG}$ ). When a battery OV fault occurs, the MP2710 suspends charging immediately and asserts a fault.

### Input Current-Based and Input Voltage-Based Power Path Management (PPM)

To meet the input source's (typically USB) maximum current limit specification, the MP2710 uses  $I_{IN}$ -based power management by monitoring  $I_{IN}$  continuously. The total  $I_{IN\_LIMIT}$  can be configured via the I<sup>2</sup>C to prevent the input source from being overloaded.

If the preset  $I_{IN\_LIMIT}$  exceeds the rating of the input source, back-up  $V_{IN}$ -based power management also works to prevent the input source from being overloaded. If either  $I_{IN\_LIMIT}$  or the  $V_{IN}$  limit is reached, Q1 between IN and SYS is regulated, limiting the total input power and dropping  $V_{SYS}$ . Once the system drops to the minimum values of ( $V_{SYS\_REG} - 100mV$ ) and ( $V_{IN} - 145mV$ ),  $I_{CHG}$  reduces to prevent  $V_{SYS}$  from dropping further.

$V_{IN}$ -based DPM regulates  $V_{IN}$  to its minimum voltage ( $V_{IN\_MIN}$ ) when the load is over the input power capacity. The  $V_{IN}$  limit function can be disabled via REG07h, bit[6].

### Battery Supplement Mode

$I_{CHG}$  is reduced to keep  $I_{IN}$  or  $V_{IN}$  regulated during DPM. If  $I_{CHG}$  is reduced to 0A, and the input source remains overloaded due to a heavy system load,  $V_{SYS}$  decreases. Once  $V_{SYS}$  drops to 30mV below  $V_{BATT}$ , the MP2710 enters battery supplement mode, and ideal diode mode is enabled. The battery MOSFET is regulated to keep ( $V_{BATT} - V_{SYS}$ ) at 22.5mV

when ( $I_{DSCHG} \times R_{ON\_BATT}$ ) is below 22.5mV. If ( $I_{DSCHG} \times R_{ON\_BATT}$ ) exceeds 22.5mV, the battery MOSFET fully turns on to maintain the ideal forward voltage. When the system load decreases and  $V_{SYS}$  exceeds ( $V_{BATT} + 20mV$ ), ideal diode mode is disabled. Figure 6 shows DPM and battery supplement mode.

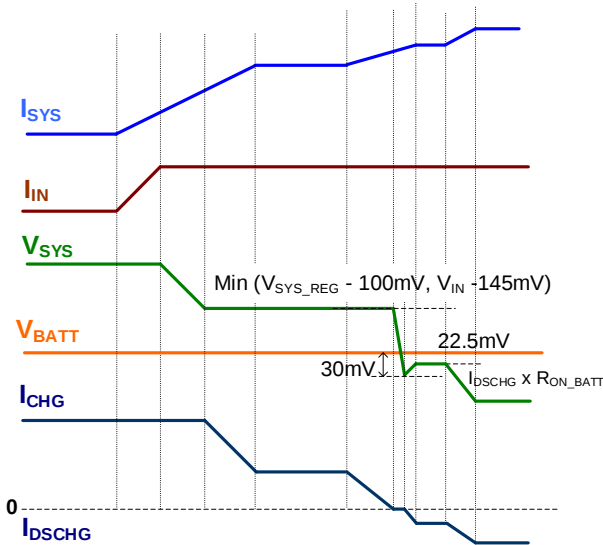


Figure 6: Dynamic Power Management and Battery Supplement

When  $V_{IN}$  is not available, the MP2710 operates in discharge mode, and the battery MOSFET is always fully on to reduce loss.

### Thermal Regulation and Thermal Shutdown

The MP2710 monitors the internal junction temperature ( $T_J$ ) continuously to maximize power delivery and avoid overheating the chip. When the internal  $T_J$  reaches the preset limit ( $T_{J\_REG}$ , 120°C by default), the IC reduces  $I_{CHG}$  to prevent higher power dissipation. The multiple thermal regulation thresholds between 60°C and 120°C help the system design meet the thermal requirements in different applications. The  $T_J$  regulation threshold can be set via REG07h, bits[5:4]. When  $T_J$  reaches 150°C, both Q1 and Q2 turn off.

### Negative Temperature Coefficient (NTC) Temperature Sensor

The MP2710 continuously monitors the battery's temperature by measuring the NTC pin voltage ( $V_{NTC}$ ), which is created by an internal precise NTC bias current flowing out of the NTC pin to the thermistor. The MP2710 compares this voltage to the internal threshold to determine which fault has occurred and to

take action accordingly. This current is only active when  $V_{IN}$  is present and can be disabled by writing 0 to the EN\_NTC bit.

The MP2710 monitors five battery temperatures: the hot battery temperature, the warm battery temperature, the cool battery temperature, the cooler battery temperature, and the cold battery temperature. These temperatures correspond to the  $V_{HOT}$ ,  $V_{WARM}$ ,  $V_{COOL}$ ,  $V_{COOLER}$ , and  $V_{COLD}$  thresholds in the Electrical Characteristics section on page 9. These thresholds can be adjusted via REG0Bh.

Figure 7 shows the NTC protection circuit.

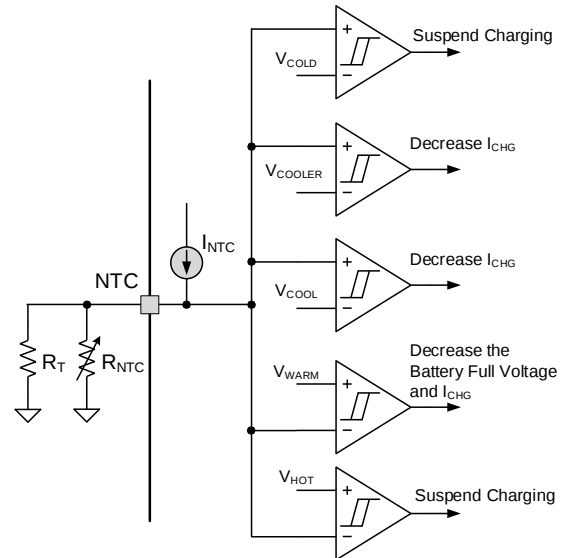


Figure 7: NTC Protection Circuit

$V_{NTC}$  can be up to 1.2V. Table 3 shows the default thresholds that the MP2710 supports with a 10kΩ NTC thermistor. For accurate temperature thresholds, a 10kΩ NTC thermistor with a 3435 B-constant should be used in parallel with a 91kΩ resistor.

Table 3: NTC Threshold for 10kΩ Thermistor

| $V_{NTC}$ (V) | Temperature (°C) |
|---------------|------------------|
| 0.146         | 60               |
| 0.233         | 45               |
| 0.751         | 10               |
| 1.049         | 0                |

Charging is suspended when  $V_{NTC} < V_{HOT}$  or  $V_{NTC} > V_{COLD}$ . The NTC actions can be configured by REG0Ch. Table 4 on page 20 shows the NTC actions.

Table 4: NTC Actions

| V <sub>NTC</sub>                                           | V <sub>BATT_REG</sub> | I <sub>CHG</sub> |
|------------------------------------------------------------|-----------------------|------------------|
| V <sub>HOT</sub> < V <sub>NTC</sub> < V <sub>WARM</sub>    | WARM_VSET             | WARM_ISET        |
| V <sub>COOL</sub> < V <sub>NTC</sub> < V <sub>COOLER</sub> | COOL_VSET             | COOL_ISET        |
| V <sub>COOLER</sub> < V <sub>NTC</sub> < V <sub>COLD</sub> | -                     | COOLER_ISET      |

Figure 8 shows the NTC protection action.

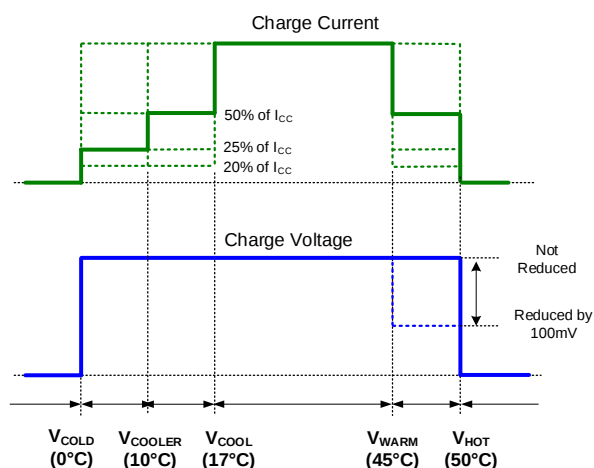


Figure 8: NTC Protection Action

When an NTC fault occurs, an interrupt is asserted and the fault bits are updated. The five adjustable temperature thresholds and the configured charge current's reduced value allow the user to easily meet the JEITA standard or a simpler I<sup>2</sup>C hot/cold function.

### Safety Timer

The MP2710 provides both a pre-charge and fast-charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. The safety timer is 1hr when V<sub>BATT</sub> is below V<sub>BATT\_PRE</sub>. The fast-charge safety timer starts when the battery enters fast-charge mode. The fast-charge safety timer can be configured via the I<sup>2</sup>C. The safety timer can also be disabled via the I<sup>2</sup>C.

The following actions can restart the safety timer:

- A new charge cycle begins.
- Write REG01h, bit[3] from 1 to 0 (charge is enabled).
- Write REG01h, bit[4] from 1 to 0 (Hi-Z is disabled).

### Watchdog Timer

The watchdog timer works in both charge and discharge mode. When the watchdog timer expires, most registers return to the default value (see the I<sup>2</sup>C Register Map section on page 27). When the watchdog timer runs out in both charge and discharge mode, both the LDO MOSFET and battery MOSFET turn off, and then turn on again automatically after 4s.

To save quiescent current (I<sub>Q</sub>) during discharge mode, the watchdog timer can be turned off by setting REG05h, bit[7] to 0.

If the watchdog timer (REG05h, bits[6:5]) is enabled, the host must reset the watchdog timer regularly by writing 1 to REG06h, bit[7] before the watchdog timer expires. The watchdog timer can also be configured or disabled by host control.

When REG05h, bits[6:5] are set to 00, the watchdog timer is disabled in both charge mode and discharge mode, regardless of REG05h, bit[7].

### Battery Discharge Mode

If the battery is connected and the input source is missing, the battery MOSFET is fully on when V<sub>BATT</sub> is above V<sub>BATT\_UVLO</sub>. The 100mΩ battery MOSFET minimizes conduction loss during battery discharging, and the battery I<sub>Q</sub> is as low as 8μA in this mode. The MP2710 has low-power mode, which is enabled by setting REG07h, bit[7] to 1. In this mode, the battery I<sub>Q</sub> can be as low as 1.5μA. The low on resistance and low I<sub>Q</sub> extend the battery run time.

### Over-Discharge Current Protection

The MP2710 has over-discharge current protection in discharge mode and supplement mode. Once the discharge current (I<sub>DSCHG</sub>) exceeds the configurable I<sub>DSCHG</sub> limit (2A by default), the battery MOSFET turns off after 60μs. The MP2710 enters hiccup mode as part of over-current protection (OCP). I<sub>DSCHG</sub> can be set high (3.2A) via the I<sup>2</sup>C. If I<sub>DSCHG</sub> goes high and reaches the internal fixed current limit (about 3.7A), the battery MOSFET turns off and hiccup mode begins immediately.

Similarly, when V<sub>BATT</sub> falls below the configurable V<sub>BATT\_UVLO</sub> (2.76V by default), the

battery MOSFET turns off to prevent over-discharge.

### System Short-Circuit Protection (SCP)

The MP2710 features system short-circuit protection (SCP) for both the IN to SYS path and the BATT to SYS path.

$V_{SYS}$  is monitored continuously. If  $V_{SYS}$  is below 1.5V, system SCP for both the IN to SYS path and the BATT to SYS path is active.  $I_{DSCHG}$  decreases to half of the original value.

For the IN to SYS path, once the input current ( $I_{IN}$ ) exceeds the protection threshold, both the LDO MOSFET and battery MOSFET turn off immediately, and the MP2710 enters hiccup mode. When the set  $I_{IN\_LIMIT}$  is reached,  $I_{IN}$  is regulated at  $I_{IN\_LIMIT}$ . Hiccup mode starts after a 60 $\mu$ s delay. The hiccup mode interval is 800 $\mu$ s.

For the BATT to SYS path, once  $I_{DSCHG}$  exceeds the protection threshold (3.7A), both the LDO MOSFET and battery MOSFET turn off immediately, and the MP2710 enters hiccup mode. When the battery  $I_{DSCHG}$  limit is reached, hiccup mode starts after 60 $\mu$ s. The hiccup mode interval is 800 $\mu$ s.

If a system short circuit occurs when both the input and battery are present, the protection mechanism of both paths works. The faster one of the two controls hiccup mode.

### Interrupt (INT) to Host

The MP2710 has an alert mechanism that outputs an interrupt signal via INT to notify the system about operation by outputting a 256 $\mu$ s low-state INT pulse.

All of the below events can trigger an INT output:

- A good input source is detected (PG\_STAT).
- Charging is complete.
- The charging status has changed.
- A REG09h fault has occurred (e.g. watchdog timer fault, thermal fault, safety timer fault, battery OVP fault, or NTC fault).

When a fault occurs, the MP2710 sends out an INT pulse and latches the fault state in REG09h. After the MP2710 exits the fault state, the fault bit is reset to 0 after the host reads REG09h. The NTC fault is not latched and always reports the current thermistor conditions.

The INT signal can be masked when the corresponding control bit is set by REG06h, bits[4:0]. When an INT condition is masked, this means that the INT pin signal (and register bit) is not triggered when the corresponding condition occurs. Masking INTs is useful when writing software code to avoid unnecessary interruptions due to these events.

### Battery Disconnect Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system to reset system power during application or to enter shipping mode. The MP2710 provides both system reset mode and shipping mode for different applications (see Table 5).

**Table 5: Shipping Mode Control**

| Items          | Enter Shipping Mode                                | Exit Shipping Mode  |                         |
|----------------|----------------------------------------------------|---------------------|-------------------------|
|                | Set FET_DIS = 1 (or Pull INT Low if SHIP_METH = 1) | Pull INT Low for 2s | V <sub>IN</sub> Plug-In |
| LDO MOSFET     | x                                                  | x                   | On (10ms later)         |
| Battery MOSFET | Off                                                | On                  | On (80ms later)         |

**Note:**

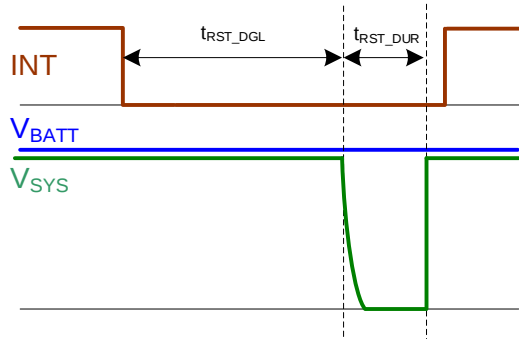
7) "x" means not affected.

The MP2710 pulls the INT pin low to reset the system. Once the logic at INT is set low for longer than the reset deglitch time ( $t_{RST\_DGL}$ ) (configurable via REG01h, bits[7:6]), the battery is disconnected from the system by turning off the battery MOSFET. The LDO MOSFET is

also turned off if  $V_{IN}$  is present. The off state lasts for the battery MOSFET off duration ( $t_{RST\_DUR}$ ) (configurable via REG01h, bit[5]). Then the battery MOSFET turns on

automatically, the LDO MOSFET turns on if  $V_{IN}$  is present, and the system starts up again.

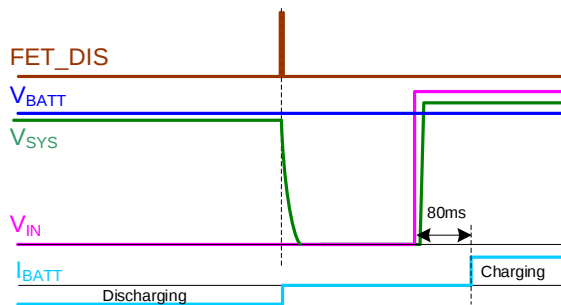
Figure 9 shows a system reset with only the battery.



**Figure 9: System Reset Mode**

There are two ways the MP2710 can enter shipping mode, which is selected by the SHIP\_METH OTP bit.

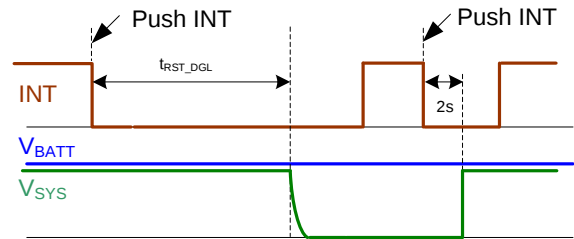
If SHIP\_METH = 0, the part enters shipping mode using software (the I<sup>2</sup>C). The IC enters shipping mode when the FET\_DIS bit is set to 1. The shipping mode entry delay can be configured via REG0Ah, bits[5:4]. The FET\_DIS bit refreshes to 0 after entering shipping mode. There are two ways to exit shipping mode. To exit shipping mode, either plug in  $V_{IN}$  for 80ms (configurable via REG0Ah, bit[2]), or pull the INT pin low for 2s. Figure 10 shows the part entering shipping mode via the I<sup>2</sup>C.



**Figure 10: Enter Shipping Mode via the I<sup>2</sup>C**

If SHIP\_METH = 1, the part enters shipping mode using hardware. Pull the INT pin low for 16s (configurable via REG01h, bits[7:6]) to have the IC enter shipping mode. To exit shipping mode, plug in  $V_{IN}$  for 80ms or pull the INT pin low again for 2s. Note that system reset mode is not available when SHIP\_METH = 1.

Figure 11 shows the part entering shipping mode via hardware.



**Figure 11: Enter Shipping Mode via Hardware**

Table 5 on page 21 shows the shipping mode control settings.

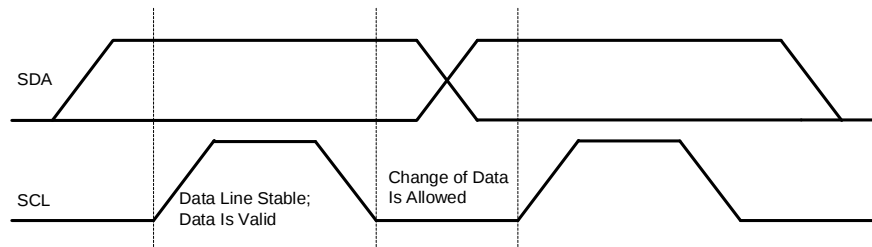
## SERIES INTERFACE

The IC uses an I<sup>2</sup>C-compatible interface for flexible charging parameters setting and instantaneous device status reporting. The I<sup>2</sup>C is a bidirectional, 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). The device can be considered a master or a slave when performing data transfers. A master device is the device that initiates a data transfer on the bus and generates the clock signals to permit the transfer. At that time, any device addressed is considered a slave device.

The MP2710 operates as a slave device with the address 08h receiving control inputs from the master device (e.g. a microcontroller or digital signal processor). The MP2710 ignores the general call address.

The I<sup>2</sup>C interface supports both standard mode (up to 100kbits) and fast mode (up to 400kbits). Both SDA and SCL are bidirectional lines that connect the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are high. The SDA and SCL pins are open drains.

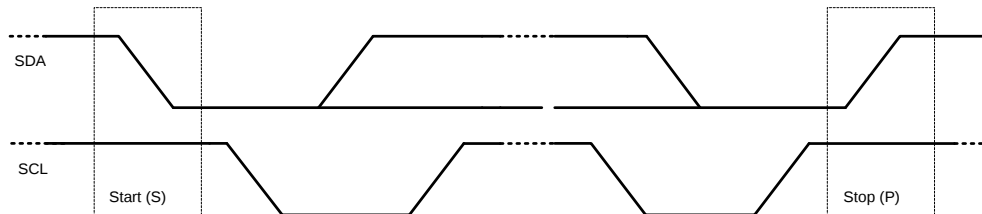
The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low. One clock pulse is generated for each data bit transferred (see Figure 12 on page 23).



**Figure 12: Bit Transfer on the I<sup>2</sup>C Bus**

All the transactions begin with a start (S) command and can be terminated by a stop (P) command. A start command is defined as a high to low transition on the SDA line while SCL is high. A stop command is defined as a low to high transition on the SDA line while SCL is high.

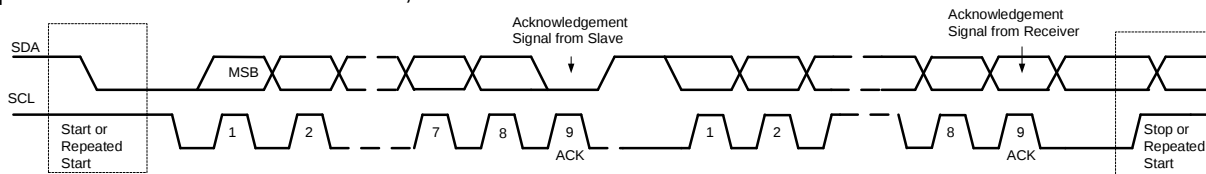
Start and stop commands are always generated by the master. The bus is considered busy after the start command, and free after the stop command (see Figure 13).



**Figure 13: Start and Stop Commands**

Every byte on the SDA line is 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold

the SCL clock line low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data, and the SCL clock line is released (see Figure 14).



**Figure 14: Data Transfer on the I<sup>2</sup>C Bus**

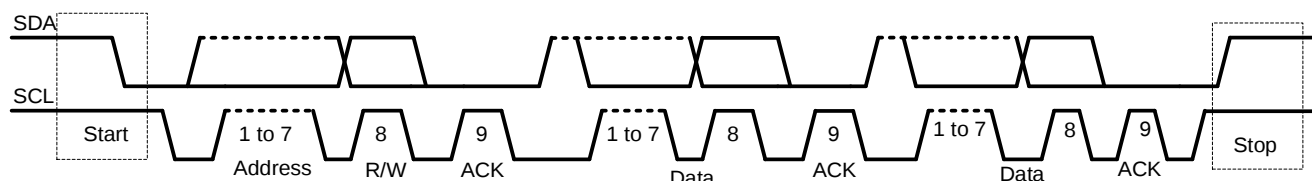
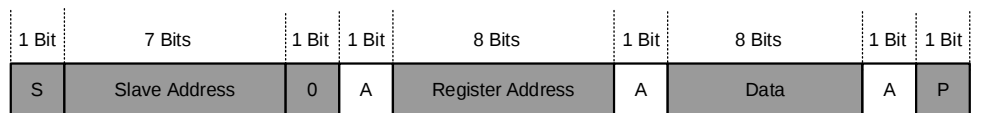
Acknowledgement takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the ninth clock pulse (acknowledge), are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low. The SDA line remains high during the ninth clock pulse. This is the not acknowledge (NACK) signal. The master can then generate either a stop to abort the transfer or a repeated start to start a new transfer.

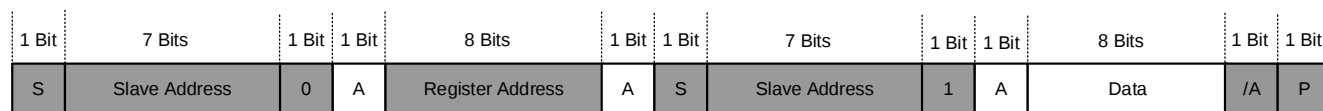
After the start command, a slave address is sent. This address is 7 bits long followed by the eighth data direction bit (R/W). A 0 indicates a transmission (write) and a 1 indicates a request for data (read). Figure 15 on page 24 shows a complete data transfer.

If the register address is not defined, the MP2710 sends back the NACK signal and enters an idle state.

The MP2710 supports single writes and single reads (see Figure 16 and Figure 17 on page 24).


**Figure 15: Complete Data Transfer**


From Master to Slave    
  From Slave to Master    
 A = Acknowledge (SDA Low)    
 S = Start    
 P = Stop

**Figure 16: Single Write**


From Master to Slave    
 A = Acknowledge (SDA Low)    
 S = Start  
 From Slave to Master    
 /A = Not Acknowledge (SDA High)    
 P = Stop

**Figure 17: Single Read**

## APPLICATION INFORMATION

### Selecting the NTC Sense Resistor

The MP2710 supports a 10kΩ NTC thermistor with a 3435 B-constant. Every internal threshold is divided from the reference voltage (1.2V) based on the precise 50μA current flowing through the 10kΩ NTC thermistor in parallel with the 91kΩ resistor (see Figure 18). Place a 91kΩ resistor in parallel with the 10kΩ NTC thermistor to generate an accurate temperature protection threshold. The threshold can be adjusted by configuring register REG0Bh.

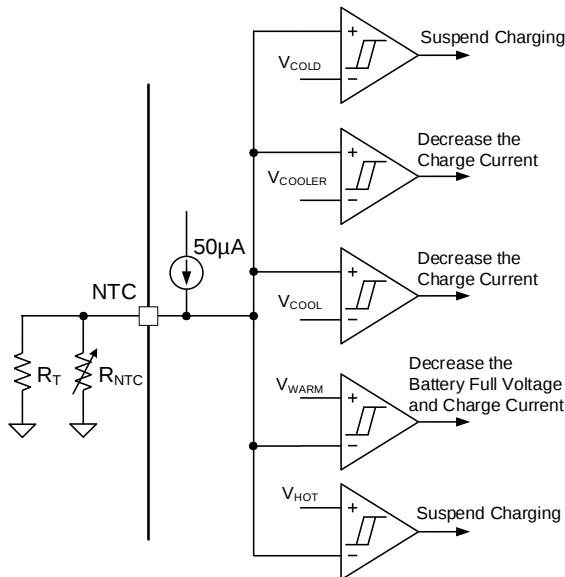


Figure 18: NTC Functional Block

### Selecting the External Capacitors

As with most LDO regulators, the MP2710 requires external capacitors for regulator stability and voltage spike immunity. The device is designed for portable applications requiring minimal board space and small components. Select the proper capacitors for optimal performance.

### Selecting the Input Capacitor

An input capacitor is required for stability. Connect a 1μF capacitor between the IN and GND pins for stable operation across the entire load current range. The output capacitance can exceed the input capacitance, as long as the input capacitance is at least 1μF.

### Selecting the Output Capacitor

The MP2710 is designed specifically to work with a very small ceramic output capacitor. A ≥4.7μF ceramic capacitor with X5R or X7R dielectrics is suitable for most applications. The output capacitor should be connected between the SYS and GND pins using a thick trace and small loop area.

### Selecting the BATT to GND Capacitor

A capacitor between the BATT and GND pins is also necessary for the MP2710. A ≥4.7μF ceramic capacitor with X5R or X7R dielectrics is suitable for most applications.

### Selecting the VDD to GND Capacitor

The capacitor between the VDD and GND pins is used to stabilize the VDD voltage ( $V_{DD}$ ) that powers the internal control and logic circuitry. The typical value of this capacitor is 100nF.

### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 19 and follow the guidelines below:

1. Place the external capacitors as close to the IC as possible to provide the smallest input inductance and ground impedance.
2. The PCB trace connecting the capacitor between VDD and GND is very important; place this capacitor as close to the IC as possible.
3. GND for the I<sup>2</sup>C wire should be clean; do place this wire close to GND.
4. Place SDA in parallel with SCL.

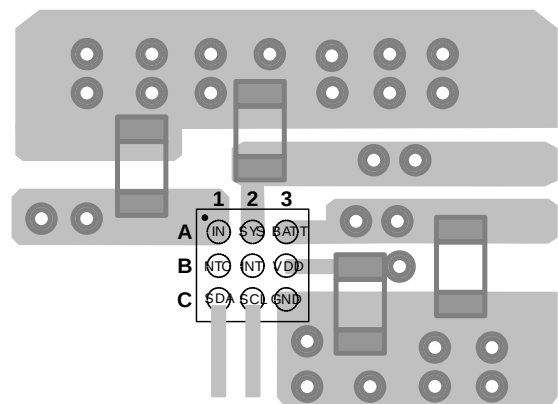


Figure 19: Recommended PCB Layout

# TYPICAL APPLICATION CIRCUIT

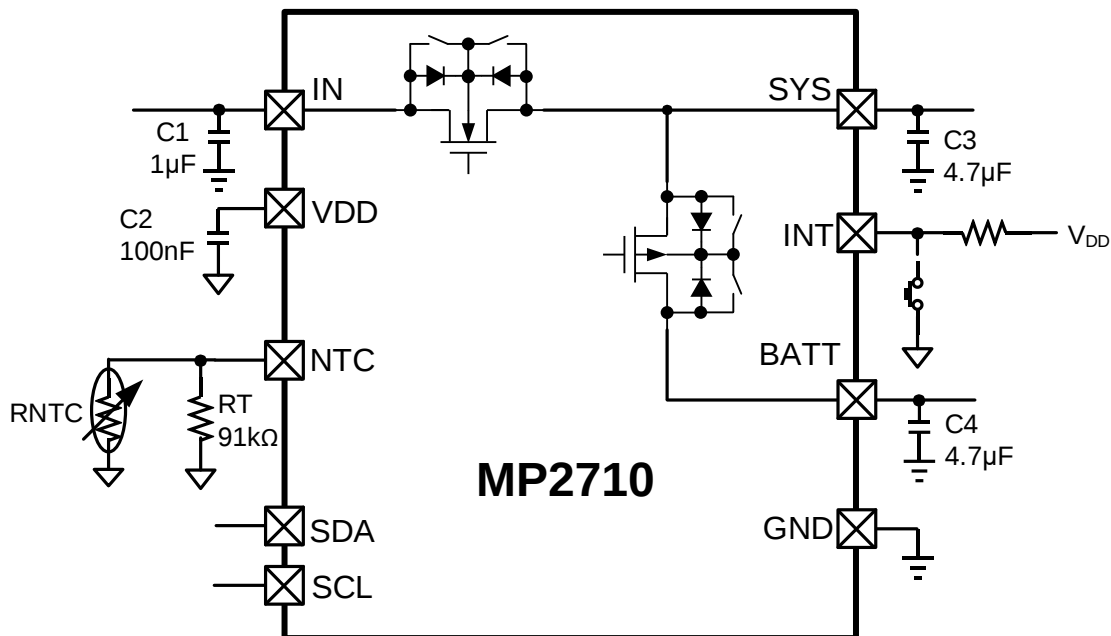


Figure 20: Typical Application Circuit

Table 6: Typical Application Circuit BOM

| Qty | Ref | Value | Description                        | Package | Manufacturer |
|-----|-----|-------|------------------------------------|---------|--------------|
| 1   | C1  | 1µF   | Ceramic capacitor, 25V, X5R or X7R | 0603    | Any          |
| 1   | C2  | 100nF | Ceramic capacitor, 16V, X5R or X7R | 0603    | Any          |
| 1   | C3  | 4.7µF | Ceramic capacitor, 16V, X5R or X7R | 0603    | Any          |
| 1   | C4  | 4.7µF | Ceramic capacitor, 16V, X5R or X7R | 0603    | Any          |

## I<sup>2</sup>C REGISTER MAP

IC Address: 08h (reserved some trim options)

| Register Name | Address | R/W | Description                                 |
|---------------|---------|-----|---------------------------------------------|
| REG00h        | 00h     | R/W | Input source control register.              |
| REG01h        | 01h     | R/W | Start-up configuration register.            |
| REG02h        | 02h     | R/W | Charge current control register.            |
| REG03h        | 03h     | R/W | Termination current.                        |
| REG04h        | 04h     | R/W | Charge voltage control register.            |
| REG05h        | 05h     | R/W | Charge termination/timer control register.  |
| REG06h        | 06h     | R/W | BATFET control and INT mask.                |
| REG07h        | 07h     | R/W | Low-power mode and system voltage register. |
| REG08h        | 08h     | R   | Status register.                            |
| REG09h        | 09h     | R   | Fault register.                             |
| REG0Ah        | 0Ah     | R/W | Shipping mode delay and NTC control.        |
| REG0Bh        | 0Bh     | R/W | NTC temperature threshold.                  |
| REG0Ch        | 0Ch     | R/W | NTC action.                                 |
| REG0Dh        | 0Dh     | R/W | Battery discharge current limit.            |

### REG00h

REG00h sets the VIN\_MIN threshold and IIN\_LIM limit of the input source in charge mode.

| Bit | Name        | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment                                                         |
|-----|-------------|-----|------------------|--------------|-----|-------------|-----------------------------------------------------------------|
| 7   | VIN_MIN [3] | 0   | Yes              | No           | R/W | 640mV.      | Offset: 3.88V<br>Range: 3.88V to 5.08V<br>Default: 4.36V (0110) |
| 6   | VIN_MIN [2] | 1   | Yes              | No           | R/W | 320mV.      |                                                                 |
| 5   | VIN_MIN [1] | 1   | Yes              | No           | R/W | 160mV.      |                                                                 |
| 4   | VIN_MIN [0] | 0   | Yes              | No           | R/W | 80mV.       |                                                                 |
| 3   | IIN_LIM [3] | 1   | Yes              | No           | R/W | 240mA.      | Offset: 50mA<br>Range: 50mA to 500mA<br>Default: 500mA (1111)   |
| 2   | IIN_LIM [2] | 1   | Yes              | No           | R/W | 120mA.      |                                                                 |
| 1   | IIN_LIM [1] | 1   | Yes              | No           | R/W | 60mA.       |                                                                 |
| 0   | IIN_LIM [0] | 1   | Yes              | No           | R/W | 30mA.       |                                                                 |

### REG01h

REG01h sets the start-up related controls, including the system reset deglitch time, IC enable, and battery under-voltage lockout (UVLO) threshold.

| Bit | Name                  | POR | Reset by REG_RST | Reset by WTD | R/W | Description                             | Comment                                                                                                                                                                                                      |
|-----|-----------------------|-----|------------------|--------------|-----|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | TRST_DGL[1]           | 1   | Yes              | No           | R/W | 00: 8s<br>01: 12s<br>10: 16s<br>11: 20s | The deglitch time for pulling INT low to reset system. After trst_dur, V <sub>sys</sub> recovers.<br><br>It is also the delay to enter shipping mode if EN_SHIP = 1 (via hardware).<br><br>Default: 16s (10) |
| 6   | TRST_DGL[0]           | 0   | Yes              | No           | R/W |                                         |                                                                                                                                                                                                              |
| 5   | TRST_DUR              | 0   | Yes              | No           | R/W | 0: 2s<br>1: 4s                          | Default: 2s (0)                                                                                                                                                                                              |
| 4   | EN_HIZ <sup>(8)</sup> | 0   | Yes              | Yes          | R/W | 0: Disabled<br>1: Enabled               | Default: Disabled (0)                                                                                                                                                                                        |

|   |               |   |     |     |     |                                         |                                                                                                                    |
|---|---------------|---|-----|-----|-----|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------|
| 3 | CEB           | 1 | Yes | Yes | R/W | 0: Charge enabled<br>1: Charge disabled | Charge configuration.<br>Default: Charge disabled (1)<br>OTP-configurable.                                         |
| 2 | VBATT_UVLO[2] | 1 | Yes | Yes | R/W | 360mV.                                  | Battery under-voltage<br>lockout (UVLO) threshold.<br>Offset: 2.4V<br>Range: 2.4V to 3.03V<br>Default: 2.76V (100) |
| 1 | VBATT_UVLO[1] | 0 | Yes | Yes | R/W | 180mV.                                  |                                                                                                                    |
| 0 | VBATT_UVLO[0] | 0 | Yes | Yes | R/W | 90mV.                                   |                                                                                                                    |

**Note:**

8) This bit only controls the on and off of the LDO MOSFET.

**REG02h**

REG02h sets the battery fast-charge current ( $I_{CC}$ ).

| Bit | Name    | POR | Reset by<br>REG_RST | Reset by<br>WTD | R/W | Description | Comment                                                                                                                                                                                                                   |
|-----|---------|-----|---------------------|-----------------|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | ICC [7] | 0   | Yes                 | Yes             | R/W | 256mA.      | Fast-charge current ( $I_{CC}$ )<br>setting.<br>Offset: 2mA<br>Range: 8mA to 456mA<br>Default: 128mA (00111111)<br>OTP-configurable.<br>Note: When $I_{CC} < 00000011$<br>(8mA), $I_{CC}$ is clamped at<br>00000011 (8mA) |
| 6   | ICC [6] | 0   | Yes                 | Yes             | R/W | 128mA.      |                                                                                                                                                                                                                           |
| 5   | ICC [5] | 1   | Yes                 | Yes             | R/W | 64mA.       |                                                                                                                                                                                                                           |
| 4   | ICC [4] | 1   | Yes                 | Yes             | R/W | 32mA.       |                                                                                                                                                                                                                           |
| 3   | ICC [3] | 1   | Yes                 | Yes             | R/W | 16mA.       |                                                                                                                                                                                                                           |
| 2   | ICC [2] | 1   | Yes                 | Yes             | R/W | 8mA.        |                                                                                                                                                                                                                           |
| 1   | ICC [1] | 1   | Yes                 | Yes             | R/W | 4mA.        |                                                                                                                                                                                                                           |
| 0   | ICC [0] | 1   | Yes                 | Yes             | R/W | 2mA.        |                                                                                                                                                                                                                           |

**REG03h**

REG03h sets the battery pre-charge current ( $I_{PRE}$ ) and charge termination current.

| Bit | Name      | POR | Reset by<br>REG_RST | Reset by<br>WTD | R/W | Description | Comment                                                                                                            |
|-----|-----------|-----|---------------------|-----------------|-----|-------------|--------------------------------------------------------------------------------------------------------------------|
| 7   | IPRE [3]  | 0   | Yes                 | Yes             | R/W | 16mA.       | Pre-charge current ( $I_{PRE}$ ).<br>Offset: 1mA<br>Range: 1mA to 31mA<br>Default: 3mA (0001)<br>OTP-configurable. |
| 6   | IPRE [2]  | 0   | Yes                 | Yes             | R/W | 8mA.        |                                                                                                                    |
| 5   | IPRE [1]  | 0   | Yes                 | Yes             | R/W | 4mA.        |                                                                                                                    |
| 4   | IPRE [0]  | 1   | Yes                 | Yes             | R/W | 2mA.        |                                                                                                                    |
| 3   | ITERM [3] | 0   | Yes                 | Yes             | R/W | 16mA.       | Termination current.<br>Offset: 1mA<br>Range: 1mA to 31mA<br>Default: 3mA (0001)<br>OTP-configurable.              |
| 2   | ITERM [2] | 0   | Yes                 | Yes             | R/W | 8mA.        |                                                                                                                    |
| 1   | ITERM [1] | 0   | Yes                 | Yes             | R/W | 4mA.        |                                                                                                                    |
| 0   | ITERM [0] | 1   | Yes                 | Yes             | R/W | 2mA.        |                                                                                                                    |

### REG04h

REG04h sets the battery voltage ( $V_{BATT}$ ) controls, including the battery charge regulation voltage and recharge threshold.

| Bit | Name          | POR | Reset by REG_RST | Reset by WTD | R/W | Description          | Comment                                                                                                             |
|-----|---------------|-----|------------------|--------------|-----|----------------------|---------------------------------------------------------------------------------------------------------------------|
| 7   | VBATT_REG [5] | 1   | Yes              | Yes          | R/W | 480mV.               | Battery regulation voltage.<br>Offset: 3.6V<br>Range: 3.6V to 4.545V<br>Default: 4.2V (101000)<br>OTP-configurable. |
| 6   | VBATT_REG [4] | 0   | Yes              | Yes          | R/W | 240mV.               |                                                                                                                     |
| 5   | VBATT_REG [3] | 1   | Yes              | Yes          | R/W | 120mV.               |                                                                                                                     |
| 4   | VBATT_REG [2] | 0   | Yes              | Yes          | R/W | 60mV.                |                                                                                                                     |
| 3   | VBATT_REG [1] | 0   | Yes              | Yes          | R/W | 30mV.                |                                                                                                                     |
| 2   | VBATT_REG [0] | 0   | Yes              | Yes          | R/W | 15mV.                |                                                                                                                     |
| 1   | RESERVED      | -   | -                | -            | -   | Reserved.            |                                                                                                                     |
| 0   | VRECH[0]      | 1   | Yes              | Yes          | R/W | 0: 100mV<br>1: 200mV | Battery recharge threshold (below $V_{BATT\_REG}$ ).<br>Default: 200mV (1)                                          |

### REG05h

REG05h sets the battery pre-charge threshold and the timer-related configurations, including timer enable, the watchdog timer, and the charge timer.

| Bit | Name         | POR | Reset by REG_RST | Reset by WTD | R/W | Description                                              | Comment                                                                                                                                                                         |
|-----|--------------|-----|------------------|--------------|-----|----------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | EN_WD_DISCHG | 0   | Yes              | No           | R/W | 0: Disabled<br>1: Enabled                                | Watchdog control in discharge mode.<br>Default: Disabled (0)                                                                                                                    |
| 6   | WATCHDOG [1] | 0   | Yes              | No           | R/W | 00: Disables the timer<br>01: 40s<br>10: 80s<br>11: 160s | I <sup>2</sup> C watchdog timer limit.<br>Default: 40s (01)<br>If bit[6:5] = 00, then the watchdog timer is disabled, regardless of whether bit[7] is set.<br>OTP-configurable. |
| 5   | WATCHDOG [0] | 1   | Yes              | No           | R/W |                                                          |                                                                                                                                                                                 |
| 4   | EN_TERM      | 1   | Yes              | Yes          | R/W | 0: Disabled<br>1: Enabled                                | Termination setting that determines whether termination is allowed.<br>Default: Enabled (1)                                                                                     |
| 3   | EN_TIMER     | 1   | Yes              | Yes          | R/W | 0: Disabled<br>1: Enabled                                | Safety timer setting.<br>Default: Enabled (1)                                                                                                                                   |
| 2   | CHG_TMR [1]  | 0   | Yes              | Yes          | R/W | 00: 3hrs<br>01: 5hrs<br>10: 8hrs<br>11: 12hrs            | Fast charge timer.<br>Default: 5hrs (01)                                                                                                                                        |
| 1   | CHG_TMR [0]  | 1   | Yes              | Yes          | R/W |                                                          |                                                                                                                                                                                 |
| 0   | VBATT_PRE    | 1   | Yes              | Yes          | R/W | 0: 2.8V<br>1: 3V                                         | Pre-charge to fast-charge threshold.<br>Default: 3V (1)                                                                                                                         |

## REG06h

REG06h sets the BATT\_FET control and INT mask.

| Bit | Name                     | POR | Reset by REG_RST | Reset by WTD | R/W | Description                                                                                                                       | Comment                                                                                                                     |
|-----|--------------------------|-----|------------------|--------------|-----|-----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| 7   | I2C_WATCHDOG_TIMER_RESET | 0   | Yes              | Yes          | R/W | 0: Normal<br>1: Reset                                                                                                             | Default: Normal (0)                                                                                                         |
| 6   | TMR2X_EN                 | 1   | Yes              | Yes          | R/W | 0: Disables the 2x extended safety timer during power-path management (PPM)<br>1: Enables the 2x extended safety timer during PPM | Default: Enables the 2x extended safety timer during PPM (1)                                                                |
| 5   | FET_DIS <sup>(9)</sup>   | 0   | Yes              | No           | R/W | 0: Enabled<br>1: Disabled                                                                                                         | Default: Enabled (0)                                                                                                        |
| 4   | PG_INT_CONTROL           | 0   | Yes              | Yes          | R/W | 0: On<br>1: Off                                                                                                                   | Default: On (0)                                                                                                             |
| 3   | EOC_INT_CONTROL          | 0   | Yes              | Yes          | R/W | 0: On<br>1: Off                                                                                                                   | Charge completed INT mask control.<br>Default: On (0)                                                                       |
| 2   | CHG_STATUS_INT_CONTROL   | 0   | Yes              | Yes          | R/W | 0: On<br>1: Off                                                                                                                   | Charging status change INT mask control (charging status includes not charging, pre-charge, and charge).<br>Default: On (0) |
| 1   | NTC_INT_CONTROL          | 0   | Yes              | Yes          | R/W | 0: On<br>1: Off                                                                                                                   | Default: On (0)                                                                                                             |
| 0   | BATTOVP_INT_CONTROL      | 0   | Yes              | Yes          | R/W | 0: On<br>1: Off                                                                                                                   | Default: On (0)                                                                                                             |

### Note:

9) This bit controls the on and off of the battery MOSFET, which includes charge and discharge.

## REG07H

REG07h sets the low-power mode control, IC temperature regulation threshold, and system voltage (V<sub>sys</sub>).

| Bit | Name       | POR | Reset by REG_RST | Reset by WTD | R/W | Description               | Comment                                              |
|-----|------------|-----|------------------|--------------|-----|---------------------------|------------------------------------------------------|
| 7   | LPM_EN     | 0   | Yes              | No           | R/W | 0: Disabled<br>1: Enabled | Low-power mode.<br>Default: Disabled (0)             |
| 6   | EN_VINLOOP | 0   | Yes              | Yes          | R/W | 0: Enabled<br>1: Disabled | Default: Enabled (0)                                 |
| 5   | TJ_REG [1] | 1   | Yes              | Yes          | R/W | 00: 60°C<br>01: 80°C      | Thermal regulation threshold.<br>Default: 120°C (11) |
| 4   | TJ_REG [0] | 1   | Yes              | Yes          | R/W | 10: 100°C<br>11: 120°C    |                                                      |

|   |              |   |     |    |     |        |                                                                                                                                      |
|---|--------------|---|-----|----|-----|--------|--------------------------------------------------------------------------------------------------------------------------------------|
| 3 | VSYS_REG [3] | 1 | Yes | No | R/W | 400mV. | System voltage (V <sub>sys</sub> ) regulation.<br>Offset: 4.2V<br>Range: 4.2V to 4.95V<br>Default: 4.65V (1001)<br>OTP-configurable. |
| 2 | VSYS_REG [2] | 0 | Yes | No | R/W | 200mV. |                                                                                                                                      |
| 1 | VSYS_REG [1] | 0 | Yes | No | R/W | 100mV. |                                                                                                                                      |
| 0 | VSYS_REG [0] | 1 | Yes | No | R/W | 50mV.  |                                                                                                                                      |

### REG08h

REG08h shows the operation status.

| Bit | Name           | POR | Reset by REG_RST | Reset by WTD | R/W | Description                                                                                        | Comment                            |
|-----|----------------|-----|------------------|--------------|-----|----------------------------------------------------------------------------------------------------|------------------------------------|
| 7   | WATCHDOG_FAULT | 0   | -                | -            | R   | 0: Normal<br>1: Watchdog timer expires                                                             | Default: Normal (0)                |
| 6   | RESERVED       | 0   | -                | -            | R   | Reserved.                                                                                          |                                    |
| 5   | CHG_STAT [1]   | 0   | -                | -            | R   | 000: Not charging<br>001: Pre-charge<br>010: CC charge<br>011: CV charge<br>100: Charging complete | Default: Not charging (000)        |
| 4   | CHG_STAT [1]   | 0   | -                | -            | R   |                                                                                                    |                                    |
| 3   | CHG_STAT [0]   | 0   | -                | -            | R   |                                                                                                    |                                    |
| 2   | PPM_STAT       | 0   | -                | -            | R   | 0: No PPM<br>1: In PPM                                                                             | Default: No PPM (0)                |
| 1   | PG_STAT        | 0   | -                | -            | R   | 0: Power failure<br>1: Power good                                                                  | Default: Power failure (0)         |
| 0   | THERM_STAT     | 0   | -                | -            | R   | 0: No thermal regulation<br>1: In thermal regulation                                               | Default: No thermal regulation (0) |

### REG09h

REG09h shows the operation faults.

| Bit | Name           | POR | Reset by REG_RST | Reset by WTD | R/W | Description                                                                                                                       | Comment                 |
|-----|----------------|-----|------------------|--------------|-----|-----------------------------------------------------------------------------------------------------------------------------------|-------------------------|
| 7   | REGISTER_RESET | 0   | Yes              | No           | R/W | 0: No fault<br>1: Reset                                                                                                           | Default: No fault (0)   |
| 6   | VIN_FAULT      | 0   | -                | -            | R   | 0: No fault<br>1: Input fault (OVP or bad source)                                                                                 | Default: No fault (0)   |
| 5   | THERM_SD       | 0   | -                | -            | R   | 0: No fault<br>1: Thermal shutdown                                                                                                | Default: No fault (0)   |
| 4   | BAT_FAULT      | 0   | -                | -            | R   | 0: No fault<br>1: Battery OVP                                                                                                     | Default: No fault (0)   |
| 3   | STMR_FAULT     | 0   | -                | -            | R   | 0: No fault<br>1: Safety timer expires                                                                                            | Default: No fault (0)   |
| 2   | NTC_FAULT [2]  | 0   | -                | -            | R   | 000: No fault<br>001: NTC hot fault<br>010: NTC warm fault<br>011: NTC cool fault<br>100: NTC cooler fault<br>101: NTC cold fault | Default: No fault (000) |
| 1   | NTC_FAULT [1]  | 0   | -                | -            | R   |                                                                                                                                   |                         |
| 0   | NTC_FAULT [0]  | 0   | -                | -            | R   |                                                                                                                                   |                         |

## REG0Ah

REG0Ah controls the shipping mode delay and NTC enable functions.

| Bit | Name        | POR | Reset by REG_RST | Reset by WTD | R/W | Description                          | Comment                                                                                             |
|-----|-------------|-----|------------------|--------------|-----|--------------------------------------|-----------------------------------------------------------------------------------------------------|
| 7:6 | RESERVED    | -   | -                | -            | -   | Reserved.                            |                                                                                                     |
| 5   | TESM_DGL[1] | 0   | Yes              | No           | R/W | 00: 1s<br>01: 2s<br>10: 4s<br>11: 8s | Enter shipping mode deglitch time.<br>Default: 1s (00)                                              |
| 4   | TESM_DGL[0] | 0   | Yes              | No           | R/W |                                      |                                                                                                     |
| 3   | RESERVED    | -   | -                | -            | -   | Reserved.                            |                                                                                                     |
| 2   | TEXSM_DGL   | 0   | Yes              | No           | R/W | 0: 80ms<br>1: 2s                     | Exit shipping mode delay time by V <sub>IN</sub> plug-in.<br>Default: 80ms (0)<br>OTP-configurable. |
| 1   | RESERVED    | -   | -                | -            | -   | Reserved.                            |                                                                                                     |
| 0   | EN_NTC      | 0   | Yes              | Yes          | R/W | 0: Disabled<br>1: Enabled            | Default: Disabled (0)<br>OTP- configurable.                                                         |

## REG0Bh

REG0Bh sets the different NTC thresholds.

| Bit | Name     | POR | Reset by REG_RST | Reset by WTD | R/W | Description                                                              | Comment                                                      |
|-----|----------|-----|------------------|--------------|-----|--------------------------------------------------------------------------|--------------------------------------------------------------|
| 7   | VHOT[1]  | 0   | Yes              | Yes          | R/W | 00: 146mV, 60°C<br>01: 170mV, 55°C<br>10: 181mV, 53°C<br>11: 199mV, 50°C | Hot threshold.<br>Default: 146mV (00)<br>OTP- configurable.  |
| 6   | VHOT[0]  | 0   | Yes              | Yes          | R/W |                                                                          |                                                              |
| 5   | VWARM[1] | 0   | Yes              | Yes          | R/W | 00: 199mV, 50°C<br>01: 233mV, 45°C<br>10: 248mV, 43°C<br>11: 322mV, 35°C | Warm threshold.<br>Default: 233mV (01)                       |
| 4   | VWARM[0] | 1   | Yes              | Yes          | R/W |                                                                          |                                                              |
| 3   | VCOOL[1] | 1   | Yes              | Yes          | R/W | 00: 534mV, 20°C<br>01: 591mV, 17°C<br>10: 632mV, 15°C<br>11: 751mV, 10°C | Cool threshold.<br>Default: 751mV (11)<br>OTP- configurable. |
| 2   | VCOOL[0] | 1   | Yes              | Yes          | R/W |                                                                          |                                                              |
| 1   | VCOOLER  | 1   | Yes              | Yes          | R/W | 0: 632mV, 15°C<br>1: 751mV, 10°C                                         | Cooler threshold.<br>Default: 751mV (1)                      |
| 0   | VCOLD    | 1   | Yes              | Yes          | R/W | 0: 982mV, 2°C<br>1: 1049mV, 0°C                                          | Cold threshold.<br>Default: 1049mV (1)                       |

### REG0Ch

REG0Ch sets the NTC action.

| Bit | Name                      | POR | Reset by REG_RST | Reset by WTD | R/W | Description                                                                                                                      | Comment                                                 |
|-----|---------------------------|-----|------------------|--------------|-----|----------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|
| 7   | COOL_VSET <sup>(10)</sup> | 0   | Yes              | Yes          | R/W | 0: No action<br>1: V <sub>BATT_REG</sub> - 100mV                                                                                 | Default: No action (0)                                  |
| 6   | WARM_VSET                 | 0   | Yes              | Yes          | R/W | 0: No action<br>1: V <sub>BATT_REG</sub> - 100mV                                                                                 | Default: No action (0)                                  |
| 5   | WARM_ISET[1]              | 0   | Yes              | Yes          | R/W | 00: No action<br>01: 50% of the charge current (I <sub>CHG</sub> )<br>10: 25% of I <sub>CHG</sub><br>11: 20% of I <sub>CHG</sub> | Warm action.<br>Default: 50% of I <sub>CHG</sub> (01)   |
| 4   | WARM_ISET[0]              | 1   | Yes              | Yes          | R/W |                                                                                                                                  |                                                         |
| 3   | COOL_ISET[1]              | 0   | Yes              | Yes          | R/W | 00: No action<br>01: 50% of I <sub>CHG</sub><br>10: 25% of I <sub>CHG</sub><br>11: 20% of I <sub>CHG</sub>                       | Cool action.<br>Default: 50% of I <sub>CHG</sub> (01)   |
| 2   | COOL_ISET[0]              | 1   | Yes              | Yes          | R/W |                                                                                                                                  |                                                         |
| 1   | COOLER_ISET[1]            | 0   | Yes              | Yes          | R/W | 00: No action<br>01: 50% of I <sub>CHG</sub><br>10: 25% of I <sub>CHG</sub><br>11: 20% of I <sub>CHG</sub>                       | Cooler action.<br>Default: 50% of I <sub>CHG</sub> (01) |
| 0   | COOLER_ISET[0]            | 1   | Yes              | Yes          | R/W |                                                                                                                                  |                                                         |

**Note:**

10) This bit is valid just when V<sub>COOL</sub> < V<sub>COOLER</sub>.

### REG0Dh

REG0Dh sets the battery discharge current limit.

| Bit | Name      | POR | Reset by REG_RST | Reset by WTD | R/W | Description | Comment                                                                                                                              |
|-----|-----------|-----|------------------|--------------|-----|-------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | RESERVED  | 0   | -                | -            | R   | Reserved.   |                                                                                                                                      |
| 3   | IDSCHG[3] | 1   | Yes              | Yes          | R/W | 1600mA      | BATT to SYS discharge current limit.<br>Offset: 200mA<br>Range: 400mA to 3.2A<br>Valid Range: 0001 to 1111<br>Default: 2000mA (1001) |
| 2   | IDSCHG[2] | 0   | Yes              | Yes          | R/W | 800mA       |                                                                                                                                      |
| 1   | IDSCHG[1] | 0   | Yes              | Yes          | R/W | 400mA       |                                                                                                                                      |
| 0   | IDSCHG[0] | 1   | Yes              | Yes          | R/W | 200mA       |                                                                                                                                      |

### REG0Eh

REG0Eh controls the system OVP enable, shipping mode method, and I<sup>2</sup>C communication address functions. This register is only for OTP use, and is available to customers to configure.

| Bit | Name      | POR | Reset by REG_RST | Reset by WTD | R/W | Description                      | Comment                  |
|-----|-----------|-----|------------------|--------------|-----|----------------------------------|--------------------------|
| 7   | YSOVP_EN  | 0   | -                | -            | R   | 0: Disabled<br>1: Enabled        | Default: Disabled (0)    |
| 6   | RESERVED  | 0   | -                | -            | R   | Reserved.                        |                          |
| 5   | SHIP_METH | 0   | -                | -            | R   | 0: By software<br>1: By hardware | Default: By software (0) |

|     |          |   |   |   |   |                                          |                                           |
|-----|----------|---|---|---|---|------------------------------------------|-------------------------------------------|
| 4   | ADDR[1]  | 0 | - | - | R | 00: 08h<br>01: 0Ah<br>10: 0Ch<br>11: 0Eh | Default: 08h (00)                         |
| 3   | ADDR[0]  | 0 | - | - | R |                                          |                                           |
| 2   | LP FUNC  | 0 | - | - | R | 0: Available<br>1: Not available         | Low-power mode.<br>Default: Available (0) |
| 1:0 | RESERVED | 0 | - | - | R | Reserved.                                |                                           |

## OTP REGISTER MAP

| Addr. | Bit[7]                               | Bit[6]   | Bit[5]    | Bit[4]  | Bit[3]                             | Bit[2]    | Bit[1] | Bit[0] |
|-------|--------------------------------------|----------|-----------|---------|------------------------------------|-----------|--------|--------|
| 01h   | -                                    |          |           |         | CEB                                | -         |        |        |
| 02h   | ICC: 8mA to 456mA, 2mA/step          |          |           |         |                                    |           |        |        |
| 03h   | IPRE: 1mA to 31mA, 2mA/step          |          |           |         | ITERM: 1mA to 31mA, 2mA/step       |           |        |        |
| 04h   | VBATT_REG: 3.6V to 4.545V, 15mV/step |          |           |         |                                    |           | -      |        |
| 05h   | -                                    | WATCHDOG |           | -       |                                    |           |        |        |
| 07h   | -                                    |          |           |         | VSYS_REG: 4.2V to 4.95V, 50mV/step |           |        |        |
| 0Ah   | -                                    |          |           |         |                                    | TEXSM_DGL |        | EN_NTC |
| 0Bh   | VHOT[1]                              | VHOT[0]  | -         |         | VCOOL[1]                           | VCOOL[0]  | -      |        |
| 0Eh   | SYSOVP_EN                            | -        | SHIP_METH | ADDR[1] | ADDR[0]                            | LP_FUNC   | -      | -      |

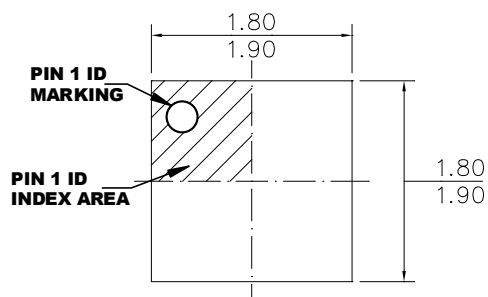
## OTP DEFAULT VALUES

**Table 7: OTP Default Values**

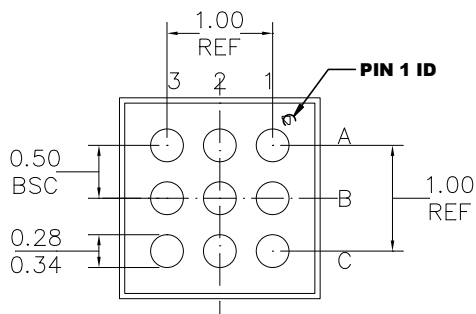
| OTP Items | Default Value |
|-----------|---------------|
| CEB       | Disabled      |
| ICC       | 128mA         |
| IPRE      | 3mA           |
| ITERM     | 3mA           |
| VBATT_REG | 4.2V          |
| WATCHDOG  | 40s           |
| VSYS_REG  | 4.65V         |
| TEXSM_DGL | 80ms          |
| EN_NTC    | Disabled      |
| VHOT      | 146mV         |
| VCOOL     | 751mV         |
| ADDR      | 08H           |
| LP_FUNC   | Available     |
| SYSOVP_EN | Disabled      |
| SHIP_METH | By software   |

# PACKAGE INFORMATION

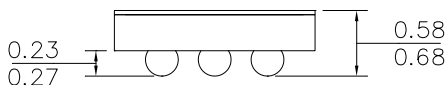
## WLCSP (1.85mmx1.85mm)



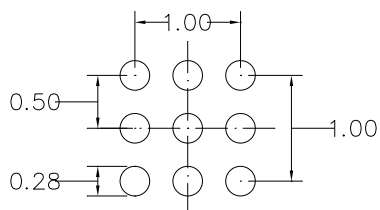
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

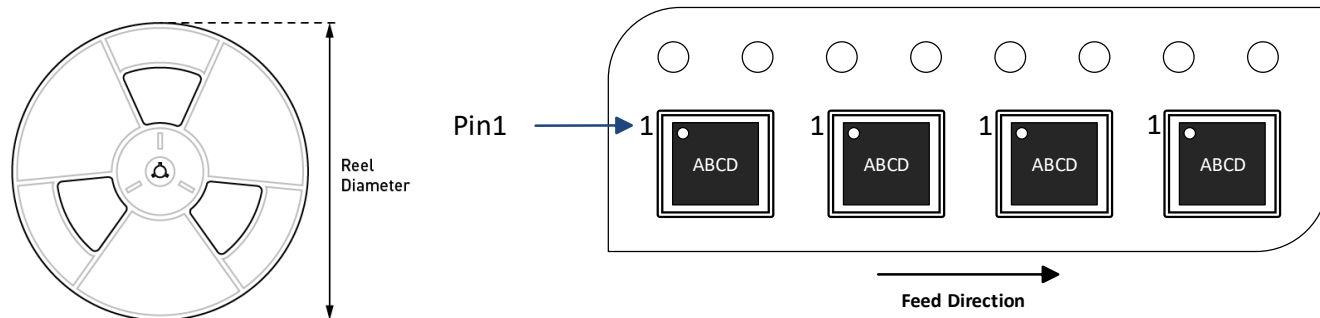


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
- 3) JEDEC REFERENCE IS MO-211.
- 4) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



| Part Number     | Package Description      | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-----------------|--------------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MP2710GC-xxxx-Z | WLCSP<br>(1.85mmx1.85mm) | 3000           | N/A            | N/A            | 7in           | 8mm                | 4mm                |

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 1/23/2024     | Initial Release | -             |

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