MP2345

26V, 2.5A, 600kHz, High-Efficiency, Synchronous, Step-Down Converter

DESCRIPTION

The MP2345 is a high-efficiency, synchronous, rectified, step-down, switch-mode converter with built-in internal power MOSFETs. It offers a very compact solution that achieves 2.5A of continuous output current with excellent load and line regulation over a wide input supply range.

The MP2345's switching edge is optimized for low EMI. SW anti-ringing is employed to address high-frequency radiation EMI issues.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MP2345 requires a minimal number of readily available, standard, external components and is available in a space-saving, 6-pin TSOT23 package.

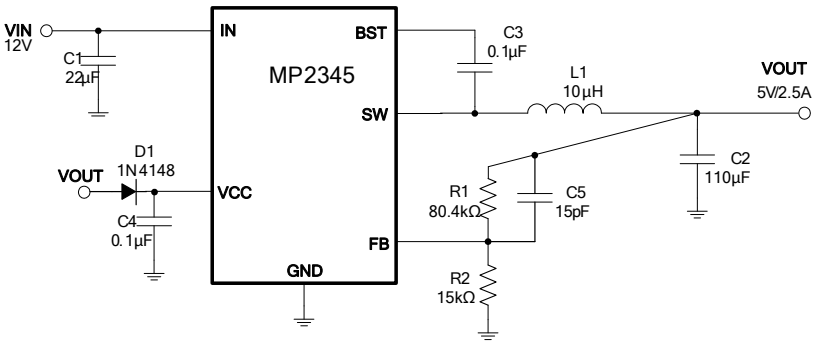
FEATURES

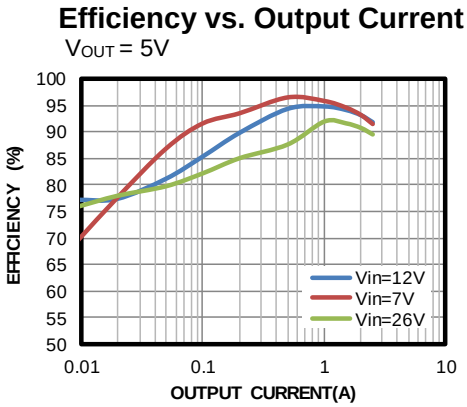
- Wide 7.5V to 26V Operating Input Range
- 2.5A Load Current
- 90mΩ/40mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Internal Power-Save Mode for Light Load
- 600kHz Fixed Switching Frequency at CCM
- Optimized for Low EMI
- Internal Soft Start
- Over-Current Protection (OCP) and Hiccup Mode
- Thermal Shutdown
- Output Adjustable from 3.3V
- Available in a TSOT23-6 Package

APPLICATIONS

- RF-Enabled Devices
- Stand-By Power Supply
- White Goods
- Flat-Panel Television and Monitors

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2345GJ	TSOT23-6	*See Below*

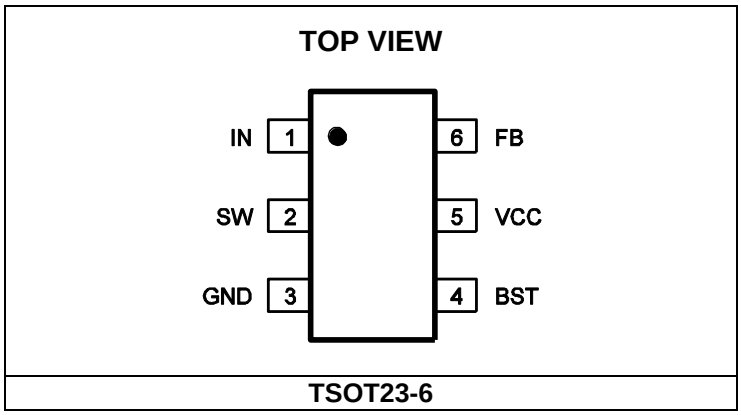
* For Tape & Reel, add suffix –Z (e.g. MP2345GJ–Z).

TOP MARKING

BGUY

BGU: Product code of MP2345GJ
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Supply voltage.** The MP2345 operates from a +7.5V to +26V input rail. C1 is needed to decouple the input rail. Connect using wide PCB traces.
2	SW	**Switch output.** Connect using wide PCB traces.
3	GND	**System ground.** GND is the reference ground of the regulated output voltage. GND requires special consideration during PCB layout. Connect GND with copper traces and vias.
4	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
5	VCC	**Internal LDO output.** Decouple VCC with a 0.1µF to 0.22µF capacitor. VCC can be biased by an external 5V output voltage through a diode.
6	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage. To prevent a current-limit runaway during a short-circuit fault condition, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 396mV.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +28V
V_{SW} .....-0.6V (-5V < 10ns) to +28V (30V < 10ns)
V_{BST} ..... V_{SW} + 6V
All other pins .....-0.3V to +6V
Continuous power dissipation (T_A = +25°C) (2)
..... 1.25W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 7.5V to 26V
Output voltage (V_{OUT})..... 3.3V to V_{IN} x D_{MAX}
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6		
EV2345-J-00A (5)	62	24 °C/W
JESD51-7 (6)	36	8 °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on EV2345-J-00A, 2-layer PCB, 64mmx48mm.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to 125°C [7], unless otherwise noted. Typical value is based on the average value when T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (quiescent)	I_q	V_{FB} = 1V		170		μA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 4V		90		mΩ
LS switch on resistance	LS_{RDS-ON}	VCC = 4V		40		mΩ
Switch leakage	SW_{LKG}				1	μA
Current limit	I_{LIMIT}	Duty cycle = 40%, T_J = 25°C	3.5	4.5	5.5	A
Oscillator frequency	f_{SW}	V_{FB} = 750mV	500	600	700	kHz
Foldback frequency	f_{FB}	V_{FB} = 200mV		0.2		f_{SW}
Maximum duty cycle	D_{MAX}	V_{FB} = 750mV		93		%
Minimum on time [8]	T_{ON_MIN}			90		ns
Feedback voltage	V_{FB}		775	791	807	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	50	nA
V_{IN} under-voltage lockout threshold rising	$INUV_{Vth}$		5.2	6.3	7.5	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			470		mV
VCC regulator	V_{CC}			4		V
VCC load regulation		I_{CC} = 5mA		1.5		%
Soft-start period	T_{SS}	10% to 90%	0.8	1.5	2.2	ms
Thermal shutdown [8]	T_{SD}			150		°C
Thermal hysteresis [8]	T_{SD_HYS}			20		°C

NOTES:

7) Not tested in production, and guaranteed by over-temperature correlation.

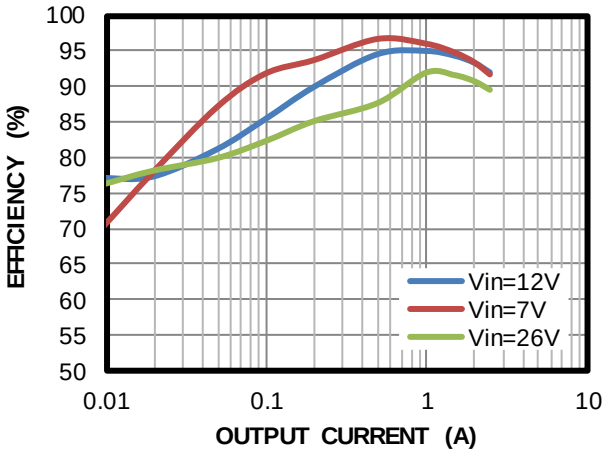
8) Guaranteed by design and characterization test.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

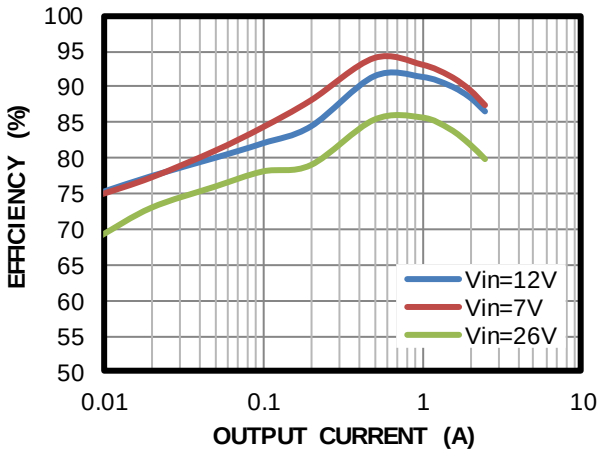
Efficiency vs. Output Current

V_{OUT} = 5V

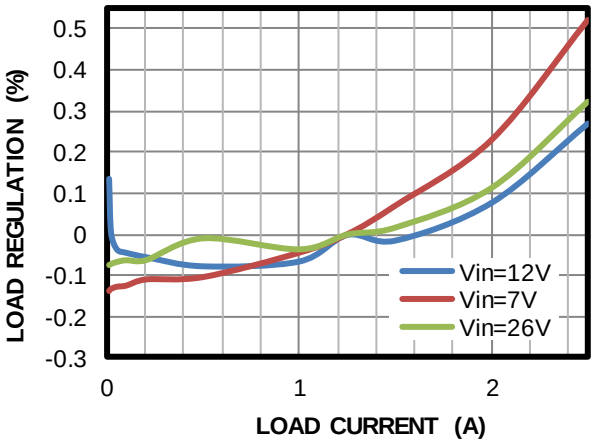


Efficiency vs. Output Current

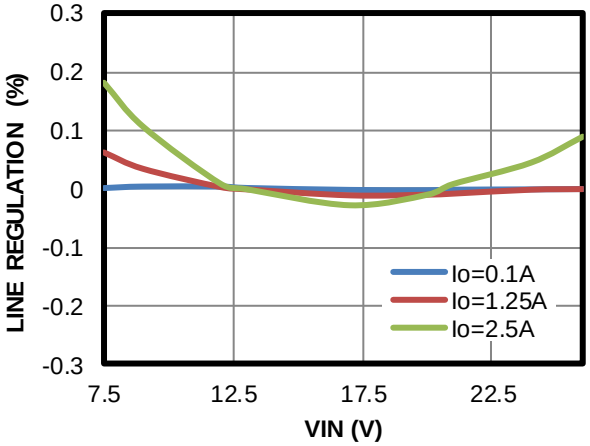
V_{OUT} = 3.3V



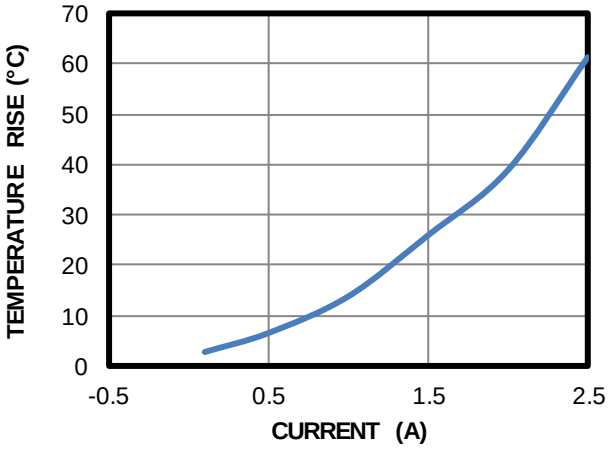
Load Regulation



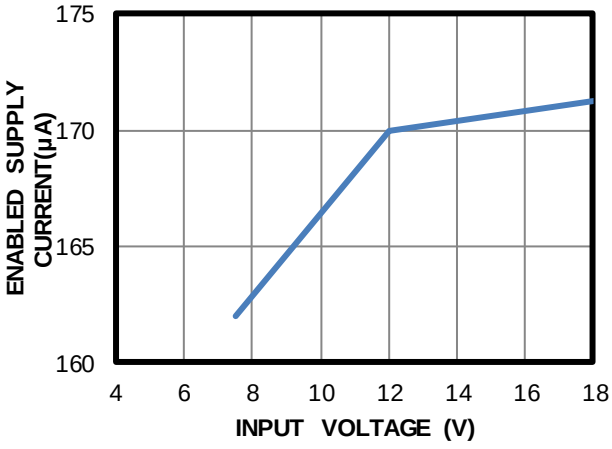
Line Regulation



Case Temperature Rise



Enabled Supply Current vs. Input Voltage

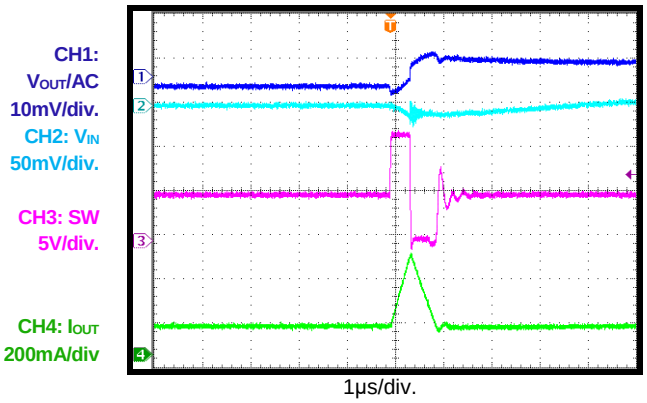


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

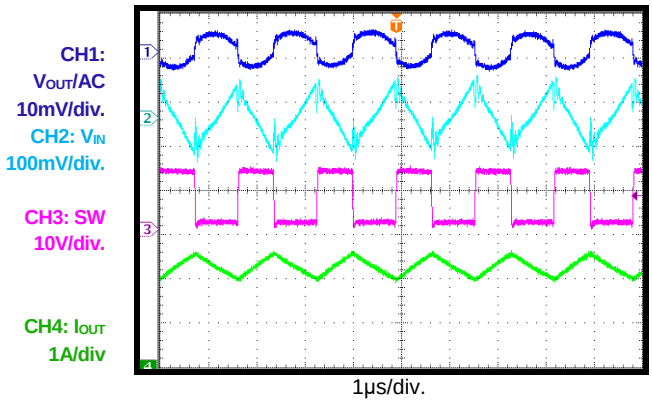
Input/Output Ripple

I_{OUT} = 0A



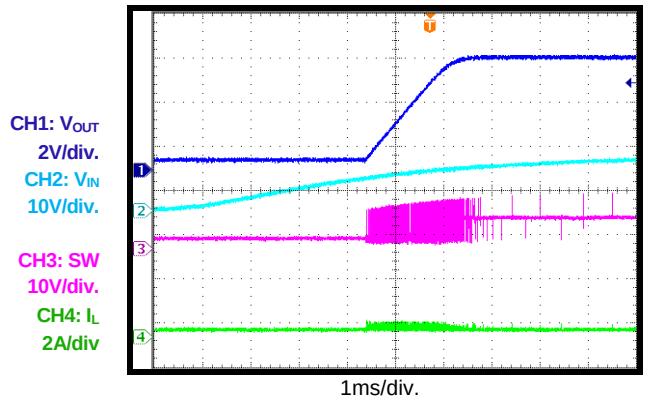
Input/Output Ripple

I_{OUT} = 2.5A



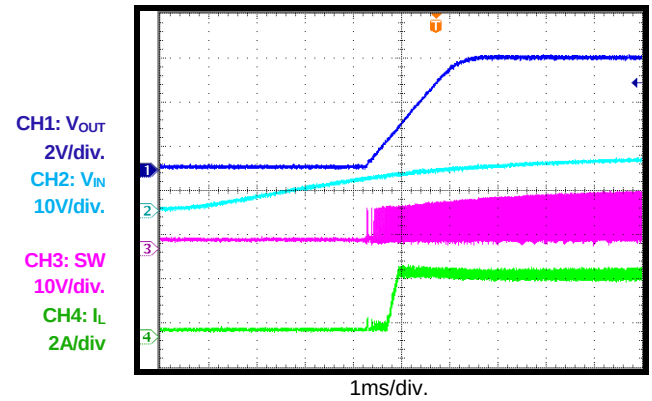
Start-Up through Input Voltage

I_{OUT} = 0A



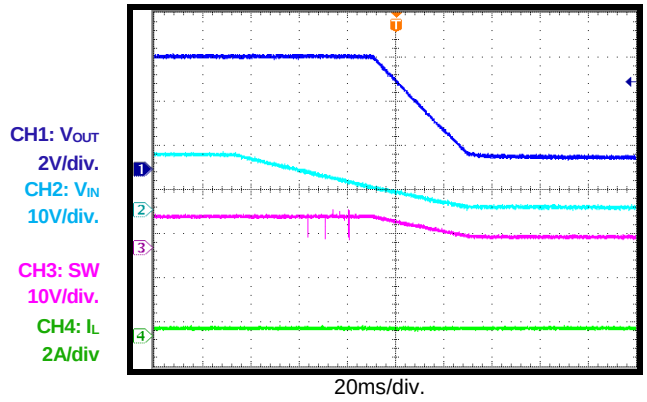
Start-Up through Input Voltage

I_{OUT} = 2.5A



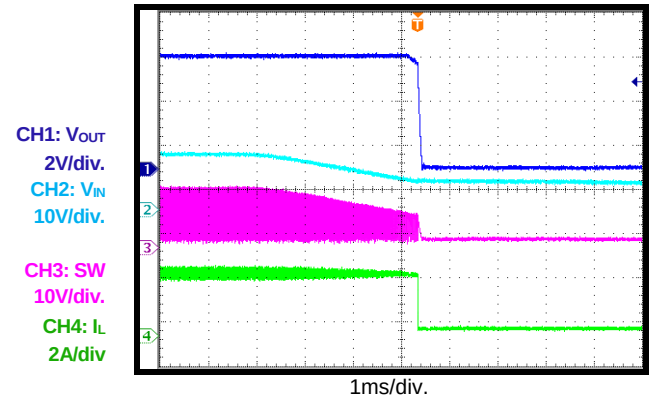
Shutdown through Input Voltage

I_{OUT} = 0A



Shutdown through Input Voltage

I_{OUT} = 2.5A

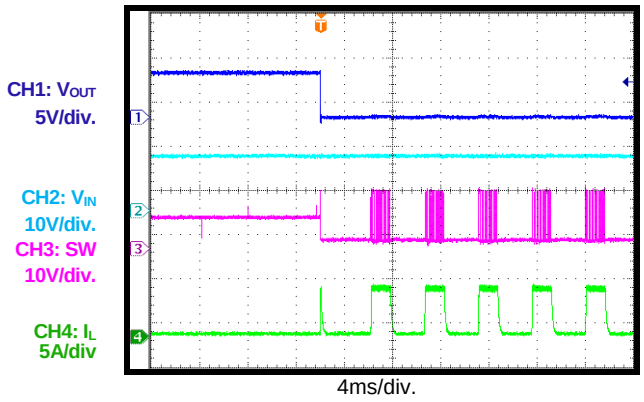


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

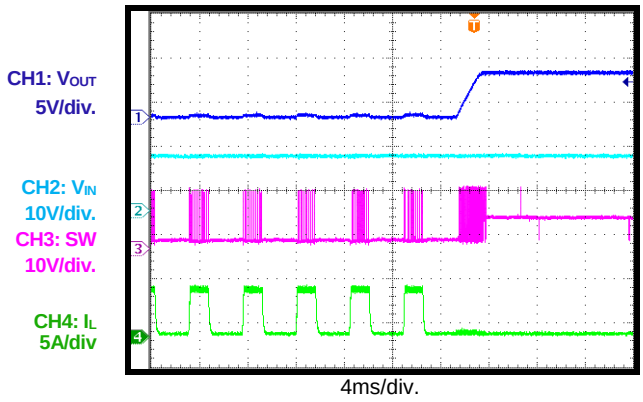
V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

OCP Entry

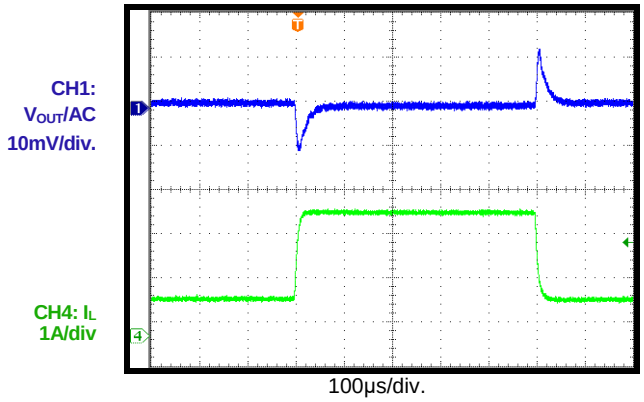
I_{OUT} = 0A



OCP Recovery



Load Transient Response



FUNCTIONAL BLOCK DIAGRAM

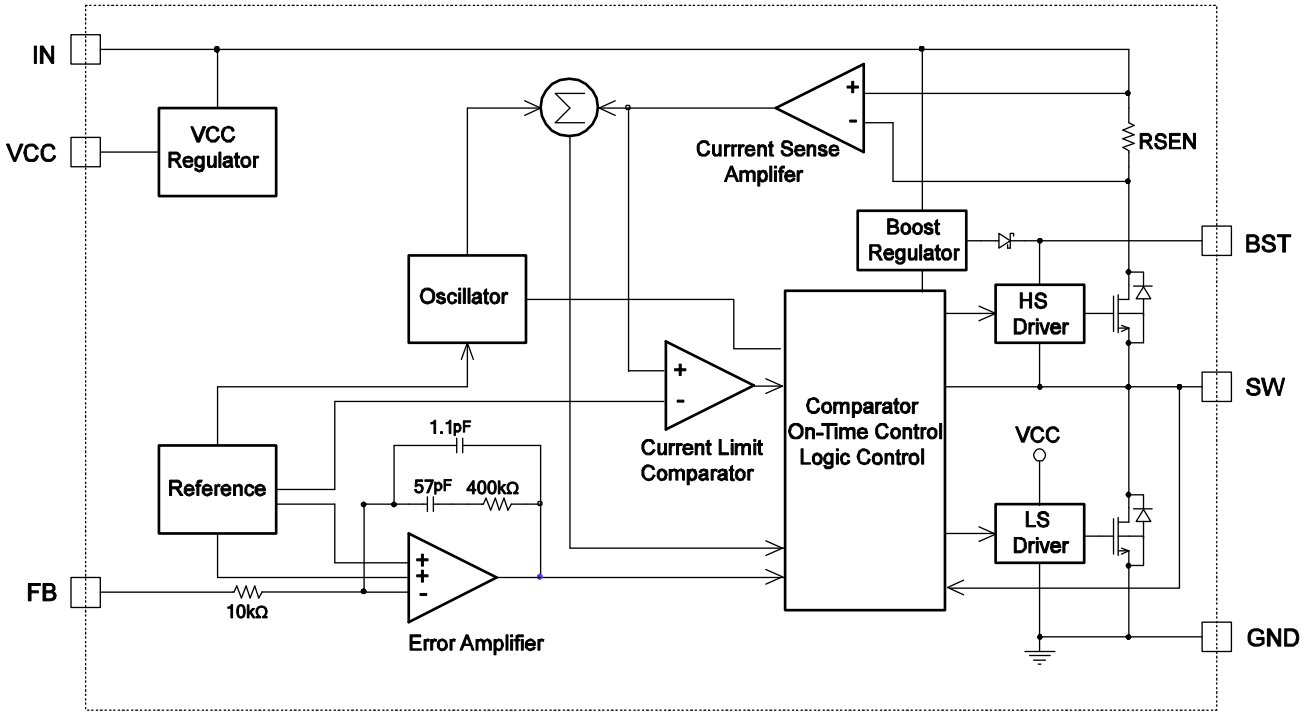


Figure 1: Functional Block Diagram

OPERATION

The MP2345 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in internal power MOSFETs. It offers a very compact solution that achieves 2.5A of continuous output current with excellent load and line regulation over a wide input supply range.

The MP2345 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. The internal clock initiates the pulse-width modulation (PWM) cycle. The integrated high-side power MOSFET (HS-FET) turns on, and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the current in the power MOSFET does not reach the current value set by COMP within 93% of one PWM period, the power MOSFET is forced off.

Internal VCC Regulator

Most of the internal circuitries are powered by the internal VCC regulator. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than its UVLO rising threshold, the output of the regulator is in full regulation. When V_{IN} is lower than its UVLO falling threshold, the internal VCC regulator shuts off. A 0.1µF ceramic capacitor is required for decoupling.

Error Amplifier (EA)

The error amplifier compares the FB voltage with the internal 0.791V reference (REF) and outputs a COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

AAM Operation

The MP2345 uses advanced asynchronous modulation (AAM) power-save mode for light loads. The AAM voltage is set at 0.4V internally. Under heavy-load conditions, V_{COMP} is higher than V_{AAM}. When the clock goes high, HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. The internal clock resets whenever V_{COMP} is higher than V_{AAM}.

Under light-load conditions, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM}, and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, and the MP2345 skips some pulses for pulse frequency modulation (PFM) mode, achieving light-load power save.

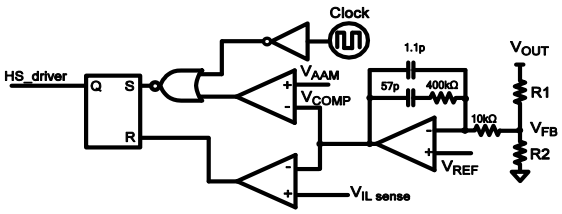


Figure 2: Simplified AAM Control Logic

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. When the input voltage is higher than the UVLO rising threshold, the MP2345 powers up. It shuts off when the input voltage is lower than the UVLO falling threshold. It also has non-latch protection.

Internal Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the 0.791V reference voltage. At this point, the reference voltage takes over. The soft-start time is set internally to be about 1.5ms from 10% to 90% of V_{OUT}.

Over-Current Protection (OCP) and Hiccup Mode

The MP2345 employs a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current-limit threshold. Meanwhile, the output voltage drops until FB is below the under-voltage (UV) threshold, typically 50% below the reference. Once UV is triggered, the MP2345 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output dead-shorts to ground. The average short-circuit current is greatly reduced to alleviate

thermal issues and to protect the regulator. The MP2345 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, the entire chip shuts down. When the temperature is below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, C3, L1, and C2 (see Figure 3). If V_{IN} - V_{SW} is more than 4V, U2 regulates M3 to maintain a 4V BST voltage across C3.

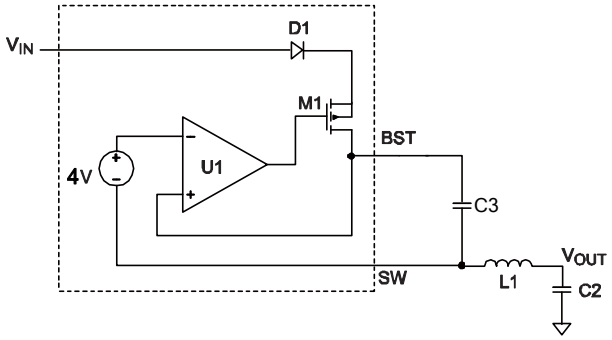


Figure 3: Internal Bootstrap Charging

Circuit Start-Up and Shutdown

If V_{IN} is higher than its UVLO threshold, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

In the shutdown procedure, the signaling path is first blocked to prevent any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor (R1) also sets the feedback loop bandwidth with the external compensation capacitor. Calculate R2 with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.791V} - 1} \quad (1)$$

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Lo (µH)
3.3	80.6	25.5	10
5	80.6	15	10

Selecting the Inductor

A 1µH to 22µH inductor with a DC current rating at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 30mΩ. For most designs, the inductance value can be derived from Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Set the inductor current at approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Under light-load conditions below 100mA, a larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated using Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 1µF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. For best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (7)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching

frequency, and causes the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

In tantalum and electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2345 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An optional, external diode may enhance the efficiency of the regulator. The conditions of the external diode are applied when the output voltage is 5V.

In this case, it is recommended to connect an external BST diode from V_{OUT} to BST (see Figure 4).

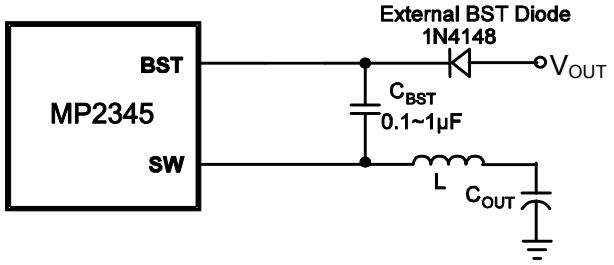


Figure 4: Optional External Bootstrap Diode Added to Enhance Efficiency

External VCC Diode

When V_{OUT} is 5V, an optional external diode from V_{OUT} to VCC may enhance the efficiency of the regulator (see Figure 5).

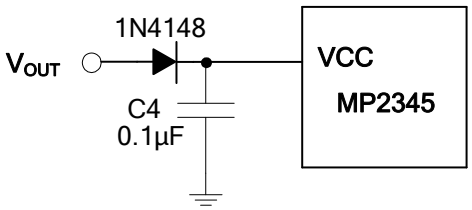


Figure 5: Optional External Diode Added to Enhance Efficiency

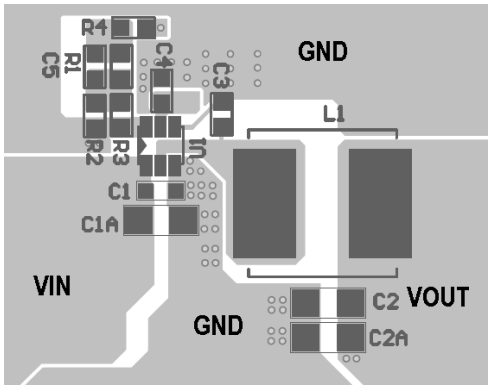
PCB Layout Guidelines (7)

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 6 and follow the guidelines below:

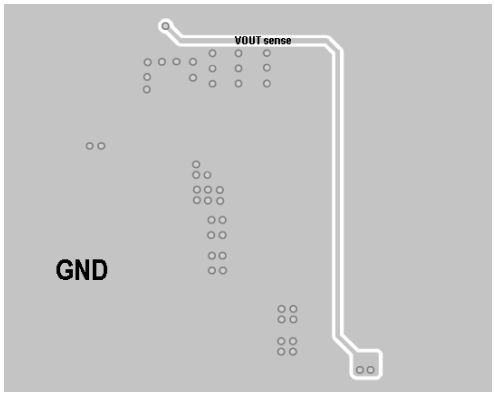
1. Keep the connection of the input ground and GND as short and wide as possible.
2. Connect the ground of the VCC capacitor to the IC's GND through multiple vias or wide traces.
3. Keep the connection between the input capacitor and IN as short and wide as possible.
4. Ensure that all feedback connections are short and direct.
5. Place the feedback resistors and compensation components as close to the chip as possible.
6. Route SW away from sensitive analog areas, such as FB.

NOTE:

9) The recommended layout is based on Figure 7: Typical Application Circuit.



Top Layer



Bottom Layer

Figure 6: Recommended PCB Layout

Design Example

Table 2 is a design example following the application guidelines for these specifications:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	5V
I_O	2.5A

Figure 7 and Figure 8 show the detailed application schematics. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 5. For more device applications, please see the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

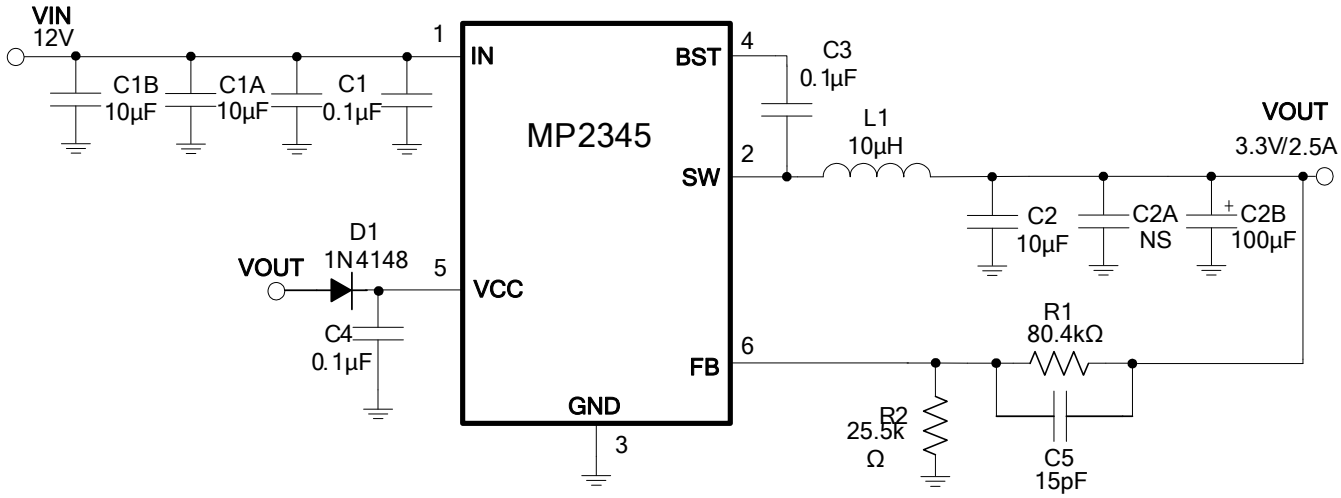


Figure 7: 3.3V/2.5A Output

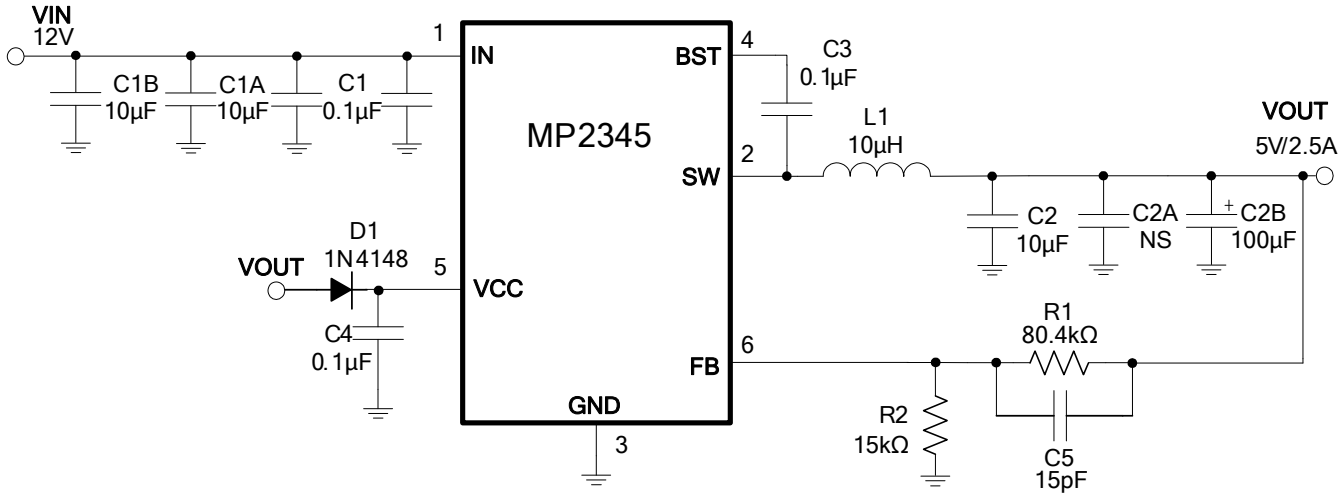
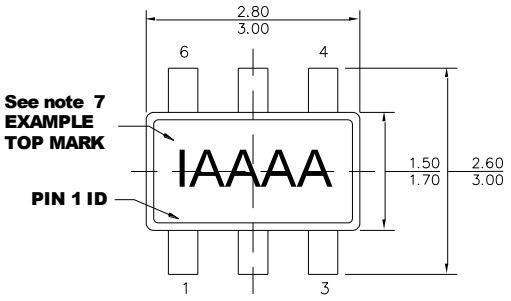


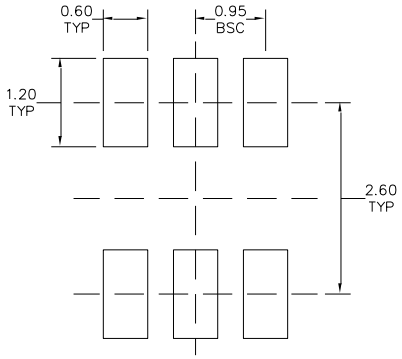
Figure 8: 5V/2.5A Output

PACKAGE INFORMATION

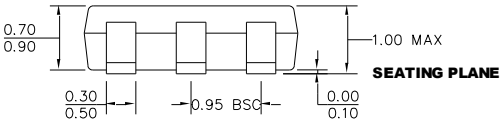
TSOT23-6



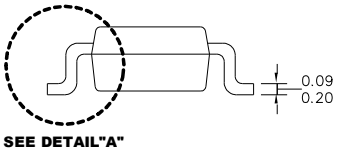
TOP VIEW



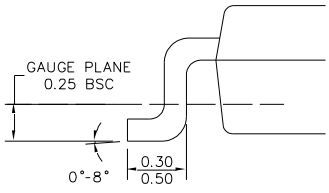
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO193, VARIATION AB.
6) DRAWING IS NOT TO SCALE
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)