MP2332C

18V, 2A, 650kHz, Synchronous Step-Down Converter with PG, SS, and Forced CCM

DESCRIPTION

The MP2332C is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP2332C offers a very compact solution that achieves 2A of continuous output current with excellent load and line regulation over a wide input range. The MP2332C uses synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP2332C requires a minimal number of readily available, standard, external components and is available in a space-saving SOT583 package.

FEATURES

- Wide 4.2V to 18V Operating Input Range
- 95mΩ/45mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 200μA Low I_Q
- High-Efficiency Synchronous Mode Operation
- Fast Load Transient Response
- 650kHz Switching Frequency
- Forced PWM Operation
- Programmable Soft-Start Time
- Power Good (PG) Indication
- Over-Current Protection (OCP) and Hiccup
- Pre-Bias Start-Up
- Thermal Shutdown
- Available in a SOT583 (1.6mmx2.1mm) Package

APPLICATIONS

- Game Consoles
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purposes

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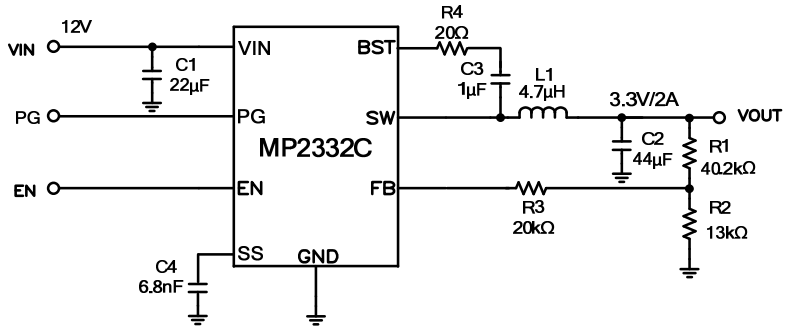
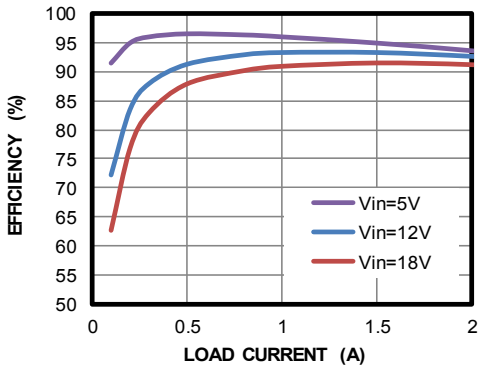
TYPICAL APPLICATION



Efficiency

V_{OUT} = 3.3V, L = 4.7μH, DCR = 19.5mΩ



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2332CGTL	SOT583 (1.6mmx2.1mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g.: MP2332CGTL–Z).

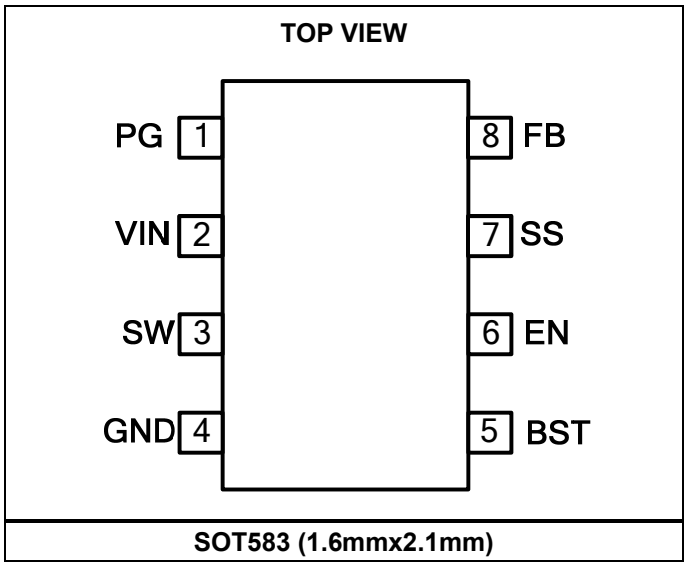
TOP MARKING

BDGY

LLL

BDG: Product code of MP2332CGTL
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



SOT583 (1.6mmx2.1mm)

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PIN FUNCTIONS

Package Pin #	Name	Description
1	PG	**Power good output.** The output of PG is an open drain. Decouple PG with a 1nF capacitor.
2	VIN	**Supply voltage.** The MP2332C operates from a 4.2V to 18V input rail. A capacitor (C1) is required to decouple the input rail. Connect VIN using a wide PCB trace.
3	SW	**Switch output.** Connect SW using a wide PCB trace.
4	GND	**System ground.** GND is the reference ground of the regulated output voltage and requires extra care during the PCB layout. Connect GND with copper traces and vias.
5	BST	**Bootstrap.** Connect a 1μF BST capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver.
6	EN	**Enable.** Drive EN high to enable the MP2332C. For automatic start-up, connect EN to VIN through a 604kΩ pull-up resistor.
7	SS	**Soft start.** Connect an external capacitor to SS program the soft-start time for the switch-mode regulator.
8	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 20V
V_{SW} ..... -0.3V (-6.5V for <10ns, -0.6V for <2μs) to 20V (21V for <10ns)
V_{BST} ..... V_{SW} + 5V
V_{EN} ..... -0.3V to 5V (2)
All other pins ..... -0.3V to 4V
Continuous power dissipation (T_A = +25°C) (3)(5) 2.2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 4.2V to 18V
Output voltage (V_{OUT}) ..... 0.8V to 0.9*V_{IN} or 13V max
Operating junction temp. (T_J) ..... -40°C to +125°C

Thermal Resistance

SOT583 (1.6mmx2.1mm)	θ_{JA}	θ_{JC}
EV2332C-TL-00A (5)	55	21 °C/W
JESD51-7 (6)	130	60 °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS max rating, please refer to the Enable Control section on page 12.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation on EV2332C Board at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV2332C-TL-00A, 2-layer PCB, 64mmx48mm.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application..

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (7), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			10	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.85V		200		μA
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 3.3V		95		mΩ
LS switch on resistance	$LS_{RDS(ON)}$			45		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V			1	μA
Low-side switching current limit OCP	$I_{LIMIT_LS_OC}$		2.5	3.5		A
Negative current limit (8)	I_{NC}	V_{OUT} = 3.3V, L = 1.5μH		-1.3		A
Oscillator frequency	f_{SW}	V_{FB} = 0.75V	485	650	815	kHz
Minimum on time (8)	T_{ON_MIN}			45		ns
Minimum off time (8)	T_{OFF_MIN}			190		ns
Feedback voltage	V_{REF}	T_J = +25°C	789	805	821	mV
Feedback current	I_{FB}			10	80	nA
Hiccup duty cycle (8)				25		%
EN rising threshold	V_{EN_RISING}		1.16	1.23	1.29	V
EN hysteresis	V_{EN_HYS}			100		mV
EN input current	I_{EN}	V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
EN turn off delay time	Tdenl			2		μs
VIN under-voltage lockout threshold rising	INUVVth			4		V
VIN under-voltage lockout threshold hysteresis	INUVHYS			400		mV
Power good rising threshold UV	PG_{UV_R}		87	92	97	$\%V_{REF}$
Power good falling threshold UV	PG_{UV_F}		82	87	92	$\%V_{REF}$
Power good rising threshold OV	PG_{OV_R}		115	120	125	$\%V_{REF}$
Power good falling threshold OV	PG_{OV_F}		102	107	112	$\%V_{REF}$
Power good rising delay				50		μs
Power good falling delay				35		μs
Power good sink current capability	V_{PG}	Sink 1mA		0.13	0.4	V
Power good leakage current	I_{PG_LEK}				3	μA
Soft-start current	Iss		5.3	7.3	9.3	μA
Thermal shutdown (8)				150		°C
Thermal hysteresis (8)				20		°C

NOTES:

7) Not tested in production. Guaranteed by over-temperature correlation.

8) Guaranteed by design and engineering sample characterization.

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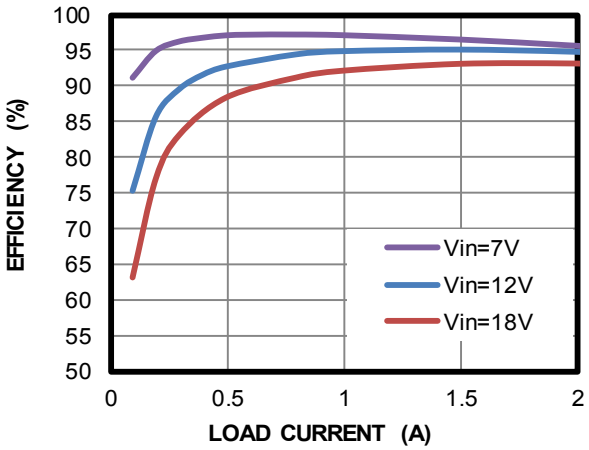
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 650kHz, unless otherwise noted.

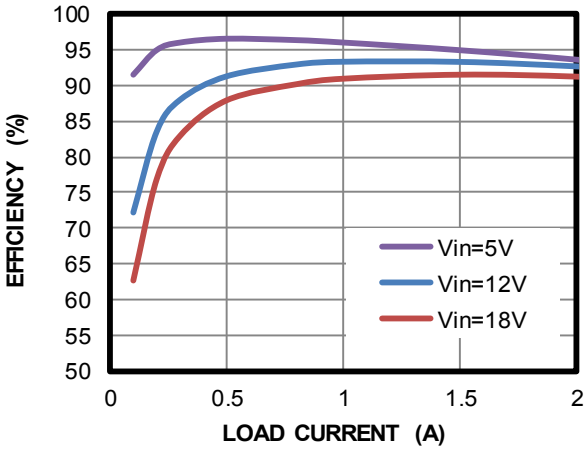
Efficiency

V_{OUT} = 5V, L = 6.5µH, DCR = 21.5mΩ



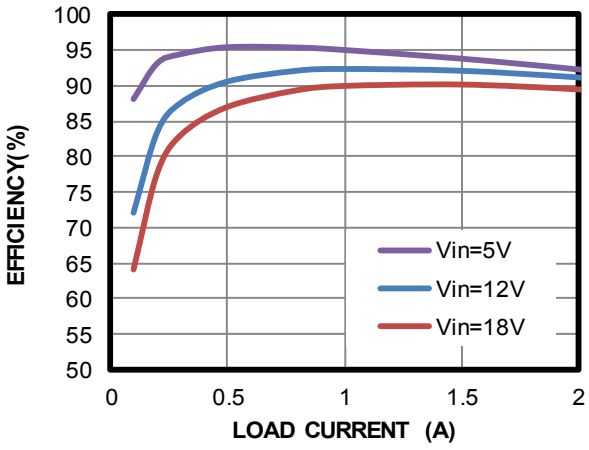
Efficiency

V_{OUT} = 3.3V, L = 4.7µH, DCR = 19.5mΩ



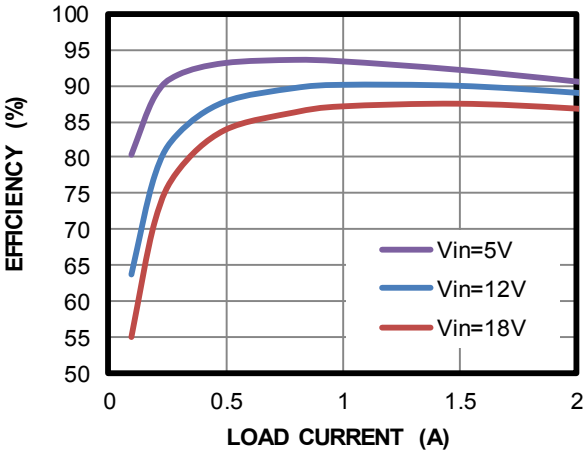
Efficiency

V_{OUT} = 2.5V, L = 3.3µH, DCR = 9mΩ



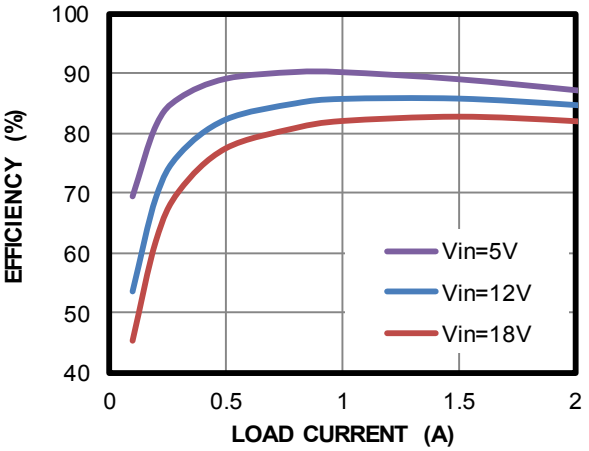
Efficiency

V_{OUT} = 1.8V, L = 3.3µH, DCR = 9mΩ



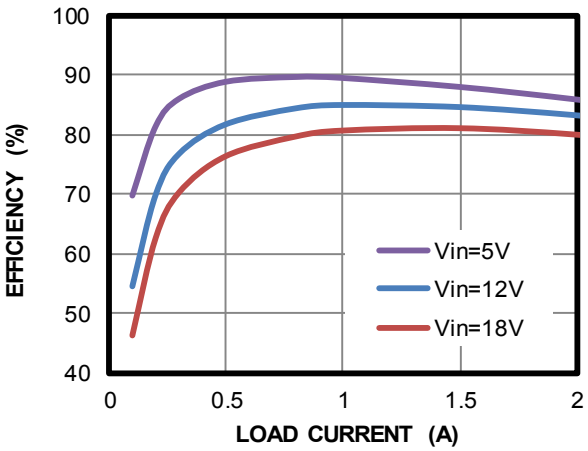
Efficiency

V_{OUT} = 1.2V, L = 2.2µH, DCR = 11.4mΩ



Efficiency

V_{OUT} = 1V, L = 1.5µH, DCR = 6.6mΩ



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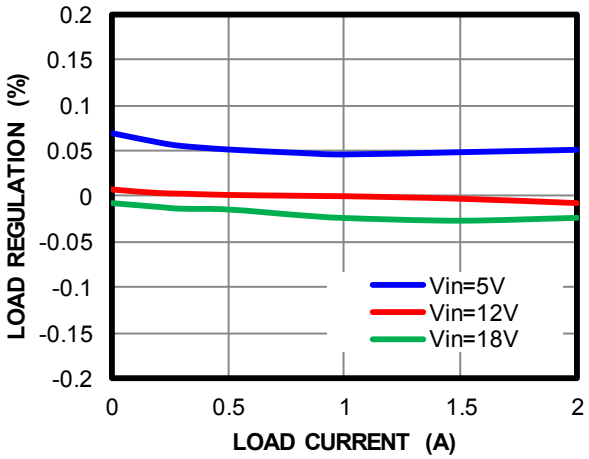
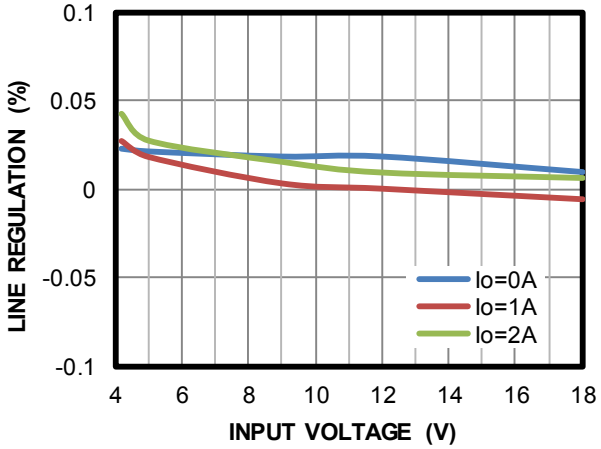
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 650kHz, unless otherwise noted.

Load Regulation

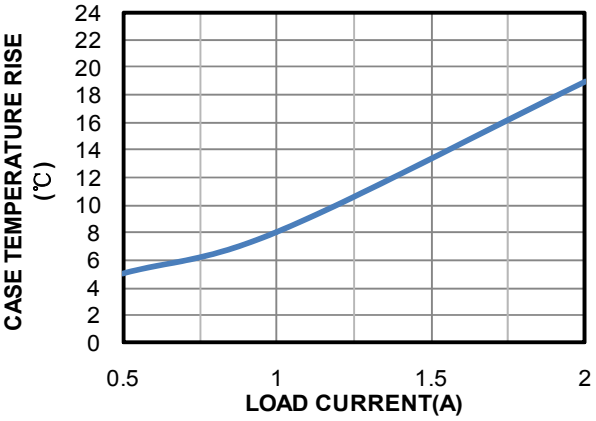


Line Regulation



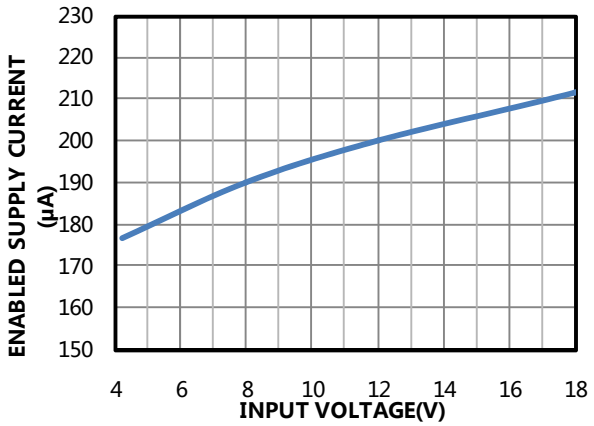
Case Temperature Rise vs. Load Current

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.5A to 2A



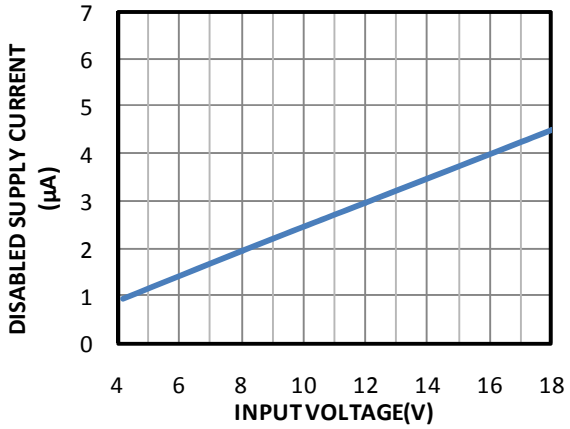
Enabled Supply Current vs. Input Voltage

V_{EN} = 2V, V_{FB} = 0.85V

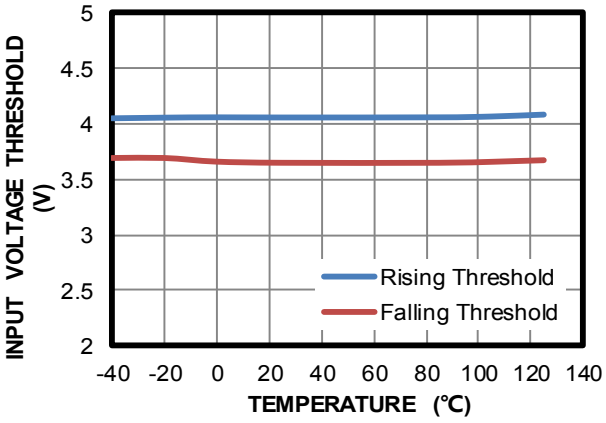


Disabled Supply Current vs. Input Voltage

V_{EN} = 0V



Input Voltage Threshold vs. Temperature



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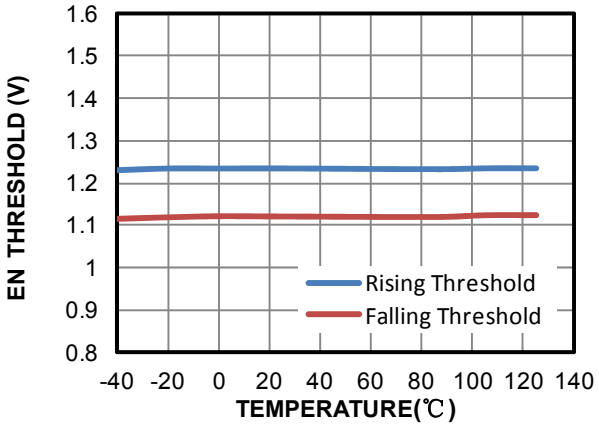
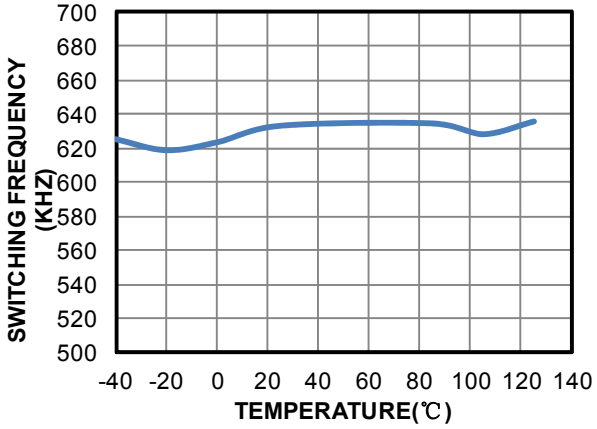
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 650kHz, unless otherwise noted.

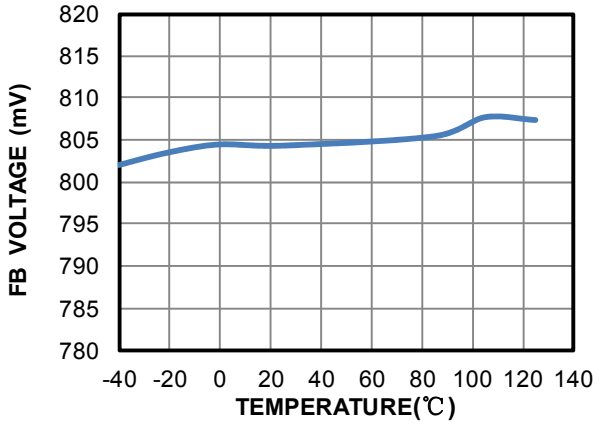
EN Threshold vs. Temperature



Switching Frequency vs. Temperature



FB Voltage vs. Temperature



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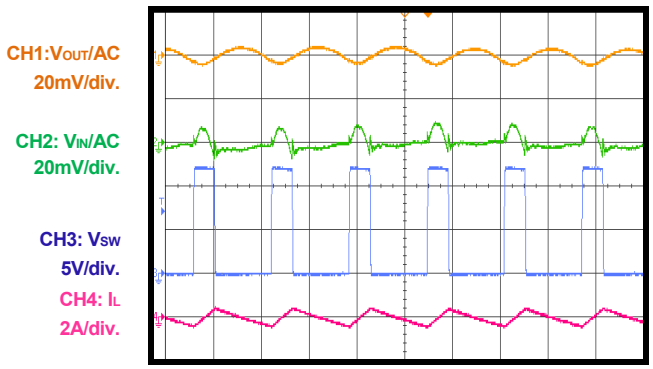
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 650kHz, unless otherwise noted.

Input/Output Ripple

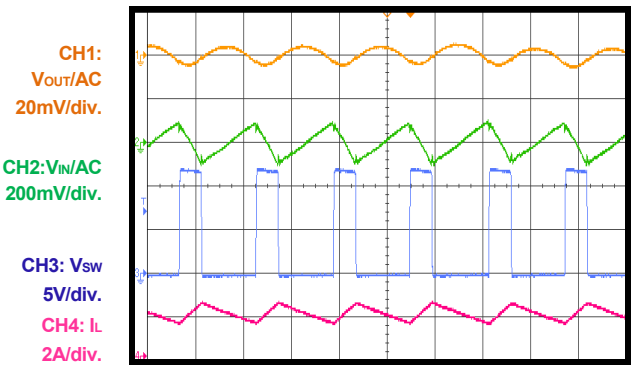
I_{OUT} = 0A



1µs/div.

Input/Output Ripple

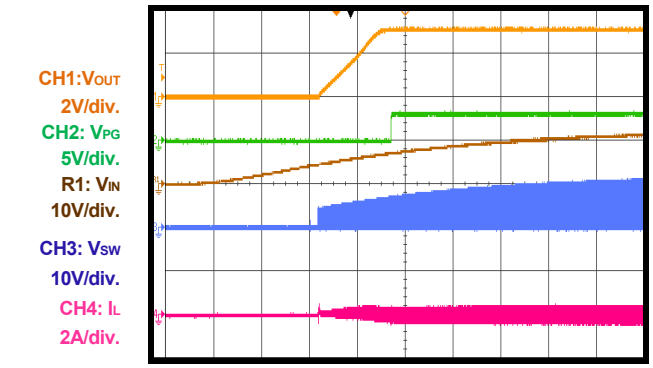
I_{OUT} = 2A



1µs/div.

Start-Up through Input Voltage

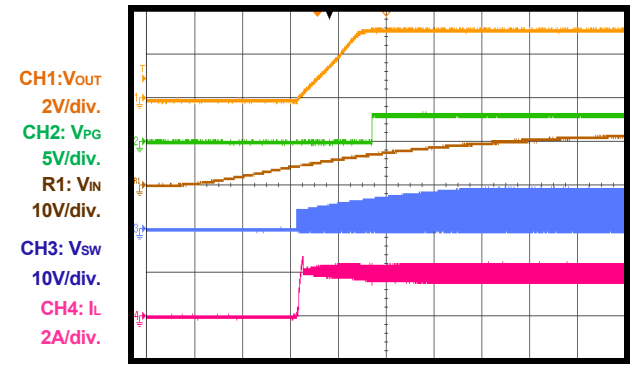
I_{OUT} = 0A



1ms/div.

Start-Up through Input Voltage

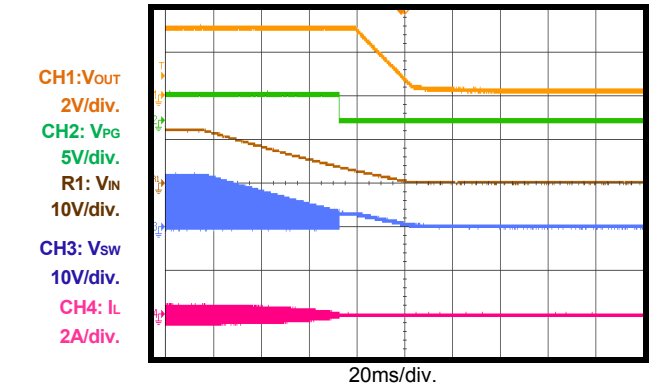
I_{OUT} = 2A



1ms/div.

Shutdown through Input Voltage

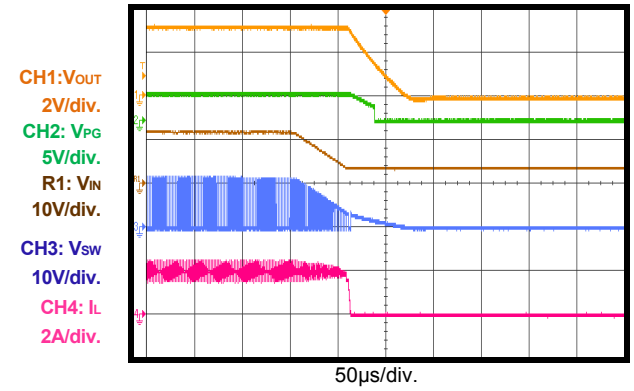
I_{OUT} = 0A



20ms/div.

Shutdown through Input Voltage

I_{OUT} = 2A



50µs/div.

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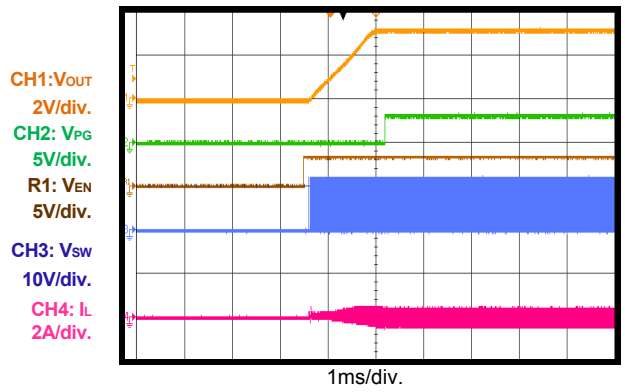
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 650kHz, unless otherwise noted.

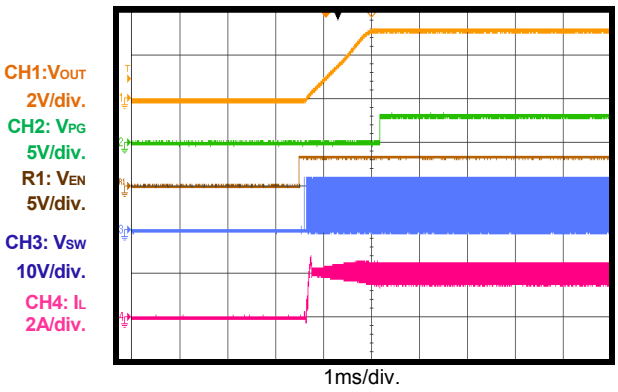
Start-Up through Enable

I_{OUT} = 0A



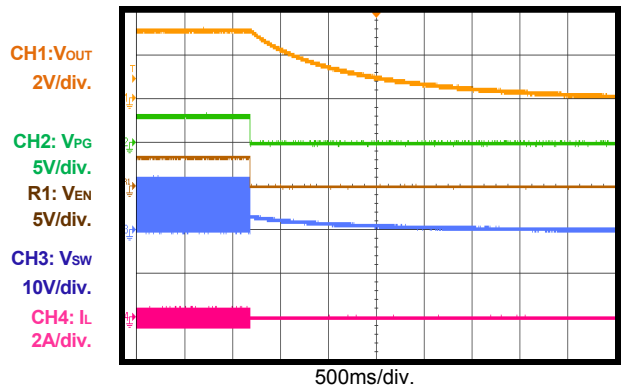
Start-Up through Enable

I_{OUT} = 2A



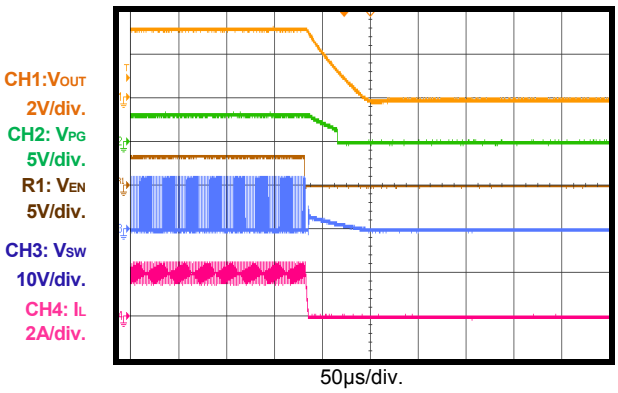
Shutdown through Enable

I_{OUT} = 0A



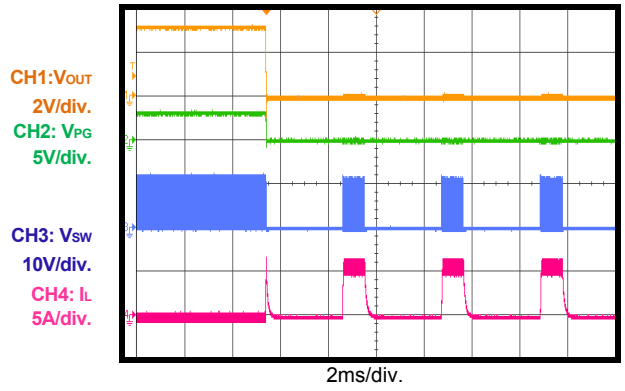
Shutdown through Enable

I_{OUT} = 2A



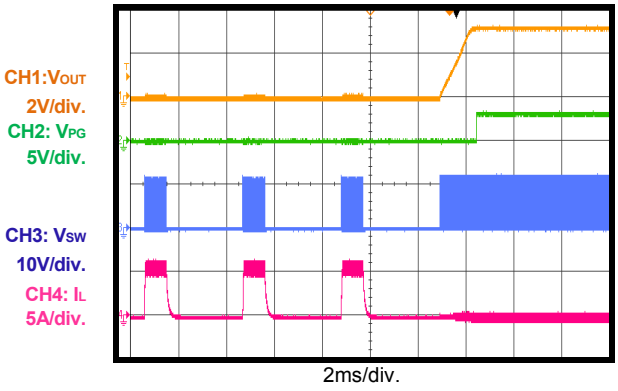
Short-Circuit Entry

I_{OUT} = 0A



Short-Circuit Recovery

I_{OUT} = 0A



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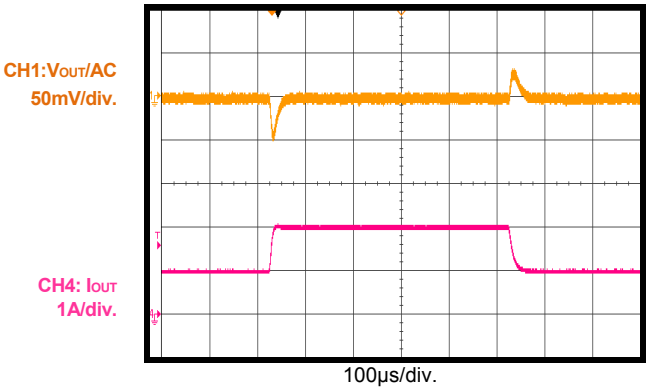
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 650kHz, unless otherwise noted.

Load Transient

I_{OUT} = 1 - 2A, slew rate is 2.5A/µs by CCDH E-load



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BLOCK DIAGRAM

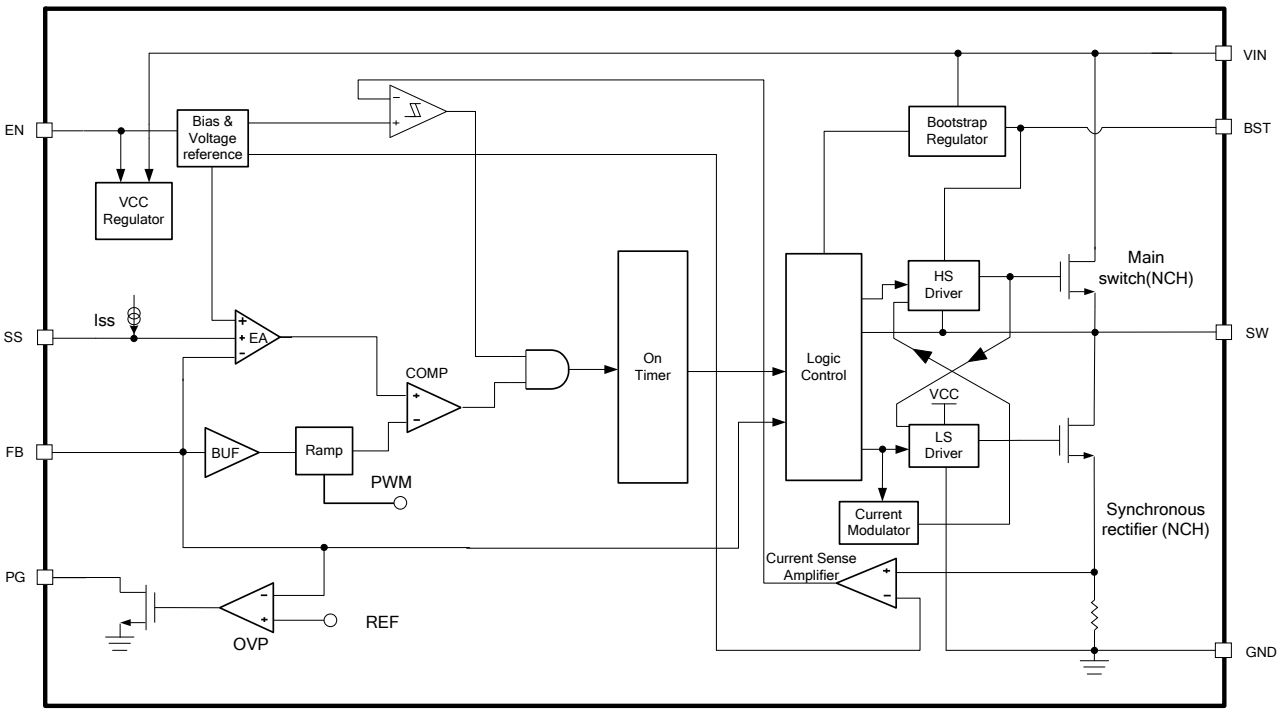

Figure 1: Functional Block Diagram

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OPERATION

The MP2332C is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). The HS-FET is turned on for a fixed interval determined by the one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range. After the on period elapses, the HS-FET is turned off until the next period begins. By repeating this operation, the converter regulates the output voltage.

The MP2332C operates in forced continuous conduction mode (CCM). The low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To prevent shoot-through, a dead time is generated internally between the HS-FET off and LS-FET on period, or the LS-FET off and HS-FET on period.

Enable Control (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current less than 40μA to prevent damage to the Zener diode. For example, when connecting a 604kΩ pull-up resistor to 12V V_{IN}, I_{Zener} = (12V - 2.8V) / (604kΩ + 35kΩ) = 14μA.

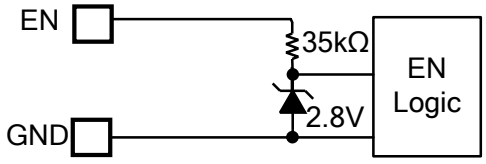

Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2332C UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4V, while its falling threshold is 3.6V.

Soft Start (SS)

The MP2332C employs a soft start (SS) mechanism to ensure smooth output ramping during power-up. When the MP2332C starts up, an internal current source (typically 7.3μA) charges up the SS capacitor to generate a soft-start voltage (V_{SS}). When V_{SS}/2 is below V_{REF}, V_{SS}/2 overrides V_{REF}. The error amplifier (EA) uses V_{SS}/2 as the reference. The output voltage ramps up smoothly. Once V_{SS}/2 rises above V_{REF}, the EA uses V_{REF} as the reference. At this point, the soft start finishes, and the MP2332C enters steady-state operation.

The SS capacitor value can be determined with Equation (1):

$$C_{ss}(nF) = \frac{T_{ss}(ms) \times I_{ss}(uA)}{2V_{REF}} \quad (1)$$

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP2332C has a valley-limit control. The inductor current is monitored during the LS-FET on state. When the sensed inductor current reaches the valley current limit, the LS limit comparator turns over, and the MP2332C enters over-current protection (OCP) mode. The HS-FET waits until the valley current limit is removed before turning on again. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold. Once UV is triggered, the MP2332C enters hiccup mode to restart the part periodically.

In OCP, the device attempts to recover from the over-current (OC) fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the OC condition still remains after the soft start ends, the device repeats this operation cycle until the OC condition is removed and the output rises back to the regulation level. OCP is a non-latch protection.

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Power Good (PG)

Power good (PG) indicates whether the output voltage is in the normal range or not compared to the internal reference voltage. PG is an open-drain structure and requires an external pull-up supply. During power-up, the power good output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce inrush current during start-up.

When the output voltage is higher than 92% and lower than 120% of the internal reference voltage and the soft start is finished, the power good signal is pulled high. When the output voltage is lower than 87% after the soft start finishes, the PG signal remains low. When the output voltage is higher than 120% of the internal reference, PG is switched low. The PG signal rises high again after the output voltage drops below 107% of the internal reference voltage.

The PG output is pulled low when EN UVLO, input UVLO, OCP, or over-temperature protection (OTP) is triggered.

Pre-Bias Start-Up

The MP2332C is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage, and $V_{SS}/2$ exceeds the sensed output voltage at FB, the part begins working normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. V_{IN} regulates the bootstrap capacitor voltage internally through D1, M1, R4, C3, L1, and C2 (see Figure 3). If V_{IN} - V_{SW} exceeds 3.3V, U2 regulates M1 to maintain a 3.3V BST voltage across C3.

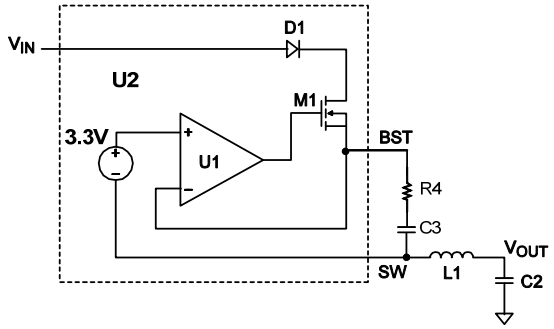

Figure 3: Internal Bootstrap Charger

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path initially to avoid any fault triggering. The internal supply rail is then pulled down.

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APPLICATION INFORMATION

Setting the Output Voltage

An external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably since a small R2 leads to considerable quiescent current loss, but a large R2 makes FB noise-sensitive. Typically, an R2 value between 5 - 30μA provides a good balance between system stability and no-load loss. Then determine R1 with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

The feedback circuit is shown in Figure 4.

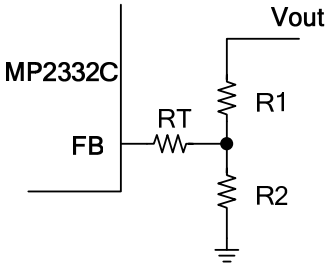

Figure 4: Feedback Network

Table 1 and Table 2 list the recommended parameters for common output voltages.

Table 1: Parameter Selection for Common Output Voltages, V_{IN} = 12V (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (μH)
1.0	33	133	120	1.5
1.2	40.2	82	75	2.2
1.5	40.2	45.3	47	2.2
1.8	40.2	32.4	36	3.3
2.5	40.2	19.1	24	3.3
3.3	40.2	13	20	4.7
5	40.2	7.68	15	6.5

NOTE:

9) Different output inductor values and output capacitor values may affect the selection of R1, R2, and RT. For additional component parameters, please refer to the Typical Application Circuits on page 17 to page 19.

Table 2: Parameter Selection for Common Output Voltages, V_{IN} = 5V

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (μH)
1.0	33	133	120	1.5
1.2	40.2	82	75	1.5
1.5	40.2	45.3	47	2.2
1.8	40.2	32.4	36	2.2
2.5	40.2	19.1	24	2.2
3.3	40.2	13	30	1.5
5(10)	40.2	7.68	15	2.2

NOTE:

10) For V_{OUT} = 5V, V_{IN} should be no lower than 6.5V.

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger inductor value results in less ripple current and a lower output ripple voltage. However, a larger inductor value also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30 - 60% of the maximum output current. The peak inductor current should be below the maximum switch current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic

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dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case scenario occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (9)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance.

For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The output voltage ripple caused by the ESR is very small. In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Choose a larger output capacitor for a better load transient response, but be sure to consider the maximum output capacitor limitation in the design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and will fail to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (12):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (12)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{ss} is the soft-start time.

PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 5 and follow the guidelines below.

1. Place the high-current paths (GND, VIN, and SW) as close to the device as possible with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short and away from the feedback network.

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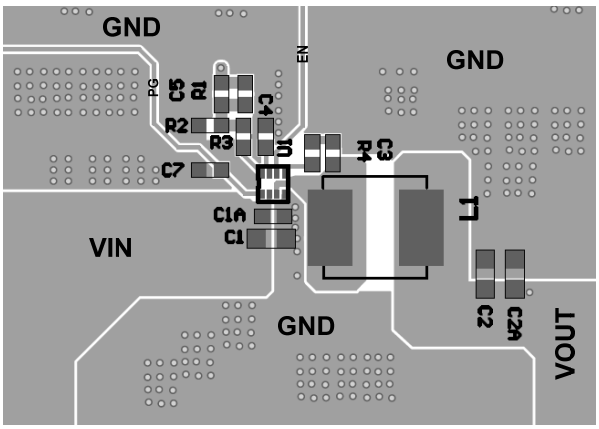

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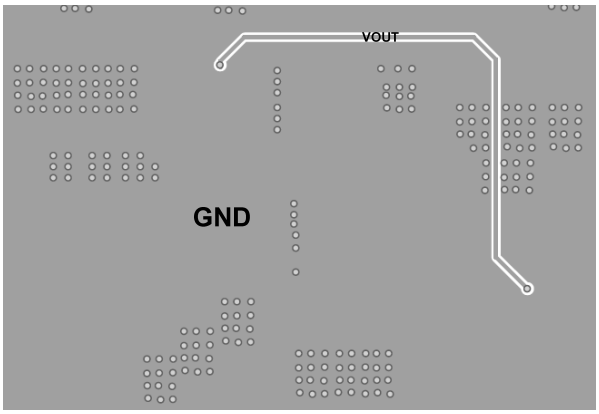

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Figure 5: Recommended Layout

Design Example

Table 3 shows a design example when ceramic capacitors are applied.

Table 3: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	2A

The detailed application schematics are shown in Figure 6 through Figure 12. The typical performance and waveforms are shown in the Typical Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUIT (11)

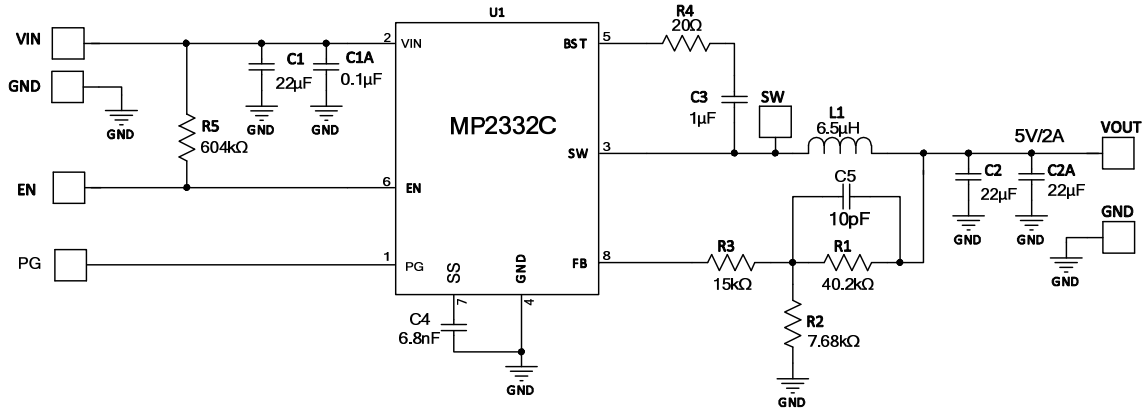

Figure 6: V_{IN} = 12V, V_{OUT} = 5V/2A

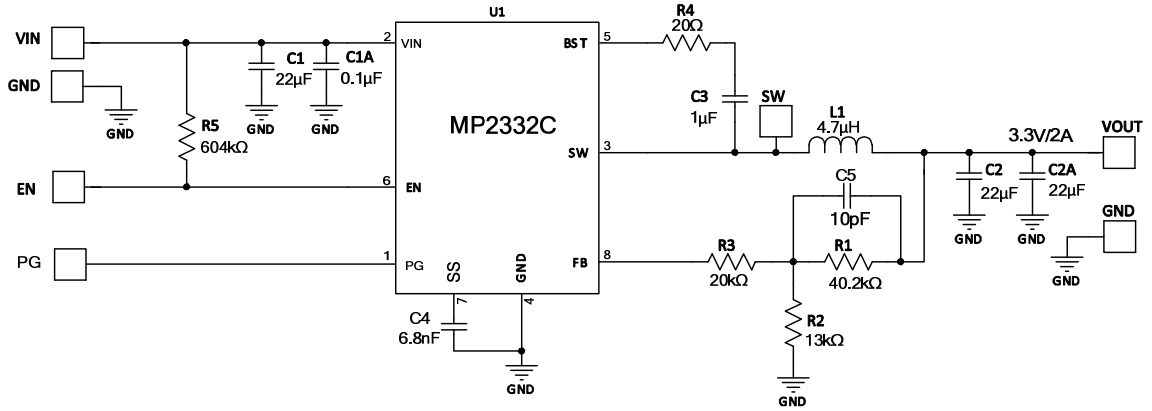

Figure 7: V_{IN} = 12V, V_{OUT} = 3.3V/2A

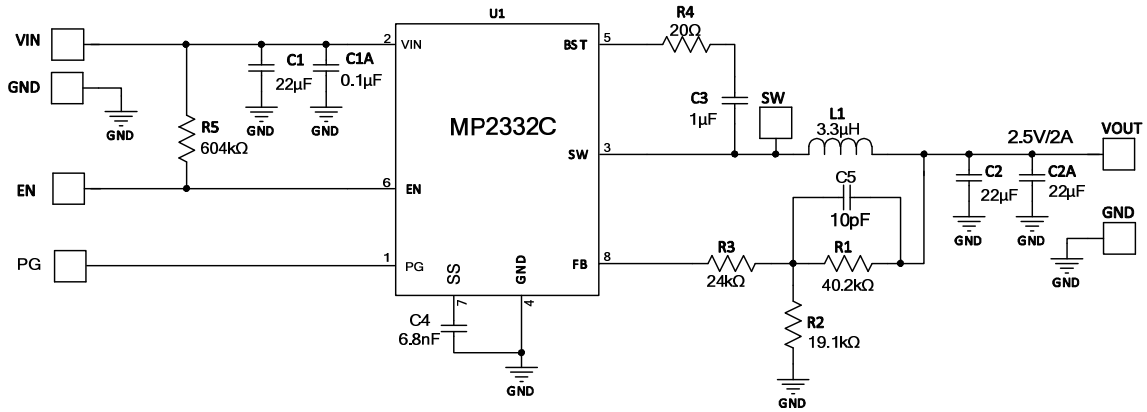

Figure 8: V_{IN} = 12V, V_{OUT} = 2.5V/2A

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TYPICAL APPLICATION CIRCUIT (11) *(continued)*

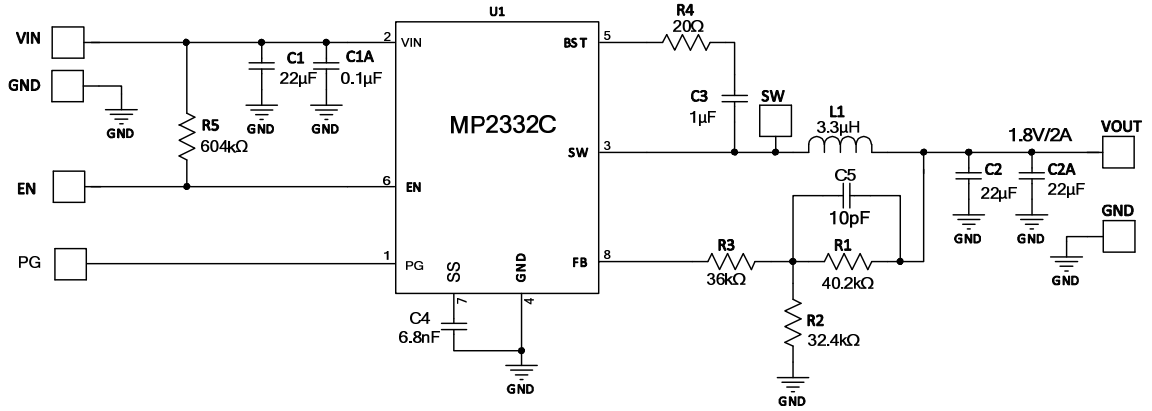

Figure 9: V_{IN} = 12V, V_{OUT} = 1.8V/2A

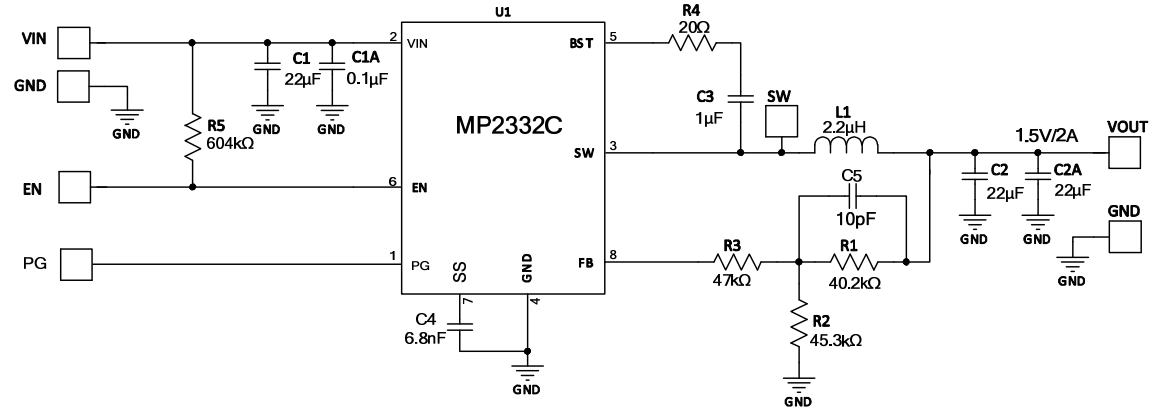

Figure 10: V_{IN} = 12V, V_{OUT} = 1.5V/2A

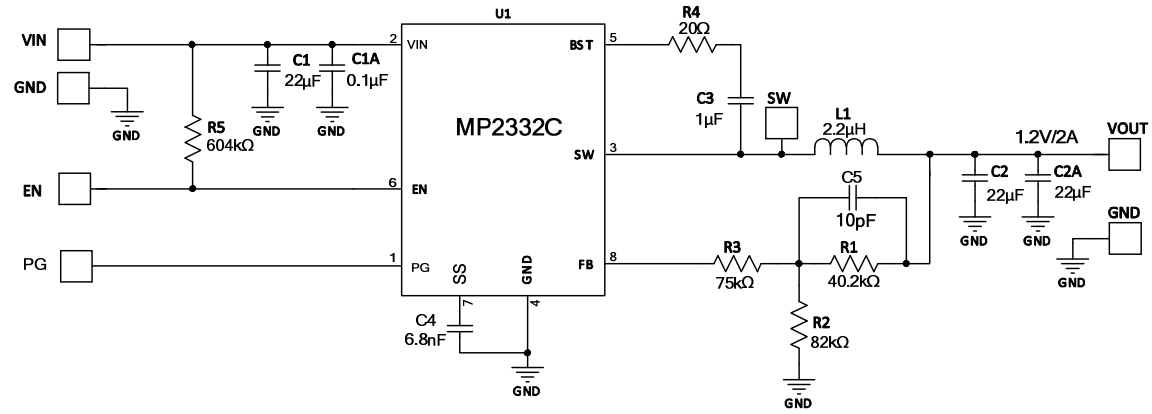

Figure 11: V_{IN} = 12V, V_{OUT} = 1.2V/2A

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TYPICAL APPLICATION CIRCUIT (11) *(continued)*

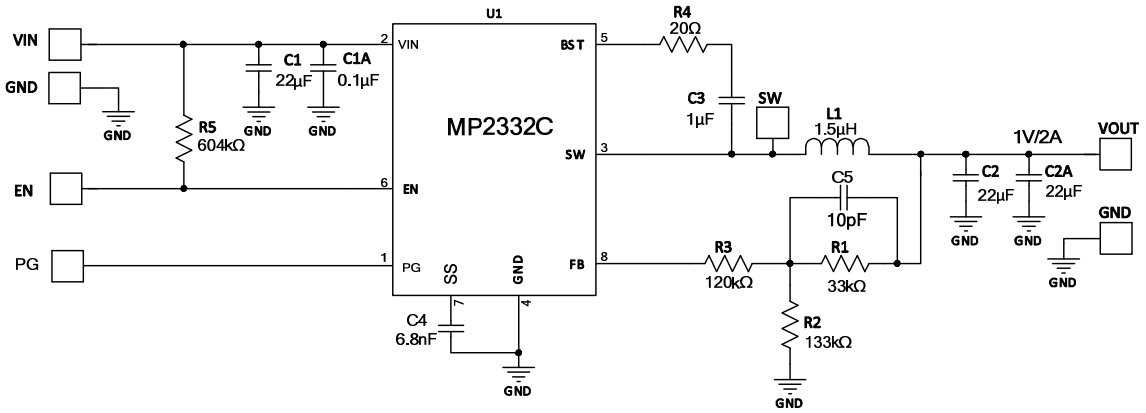

Figure 12: V_{IN} = 12V, V_{OUT} = 1V/2A

NOTE:

11) PG is an open drain. Is it recommend to pull PG to a 3.3V source through a pull-up resistor (e.g.: 100kΩ).

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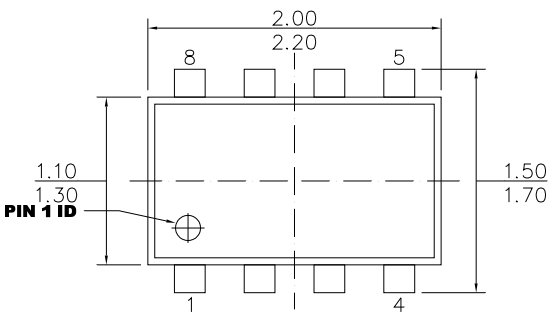
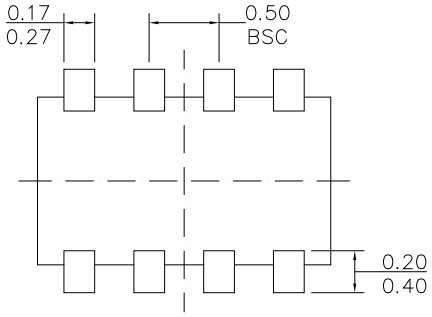
PACKAGE INFORMATION

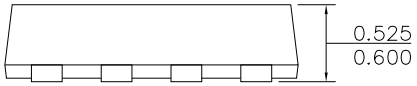
SOT583 (1.6mmx2.1mm)



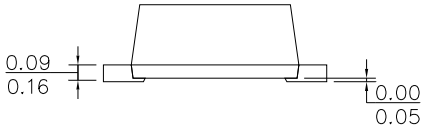
TOP VIEW



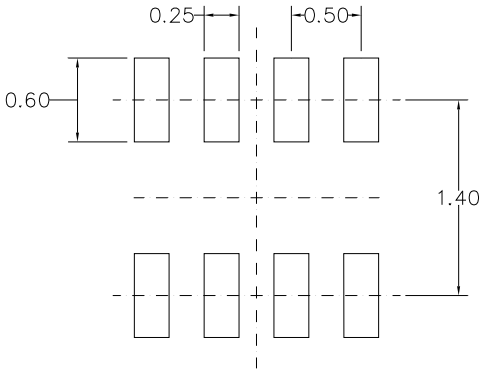
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING IS NOT TO SCALE.

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