MP2329

24V, 6.5A, Low I_Q, Synchronous, Buck Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2329 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. The MP2329 offers a super-compact solution that achieves 6.5A of continuous output current and 7.5A of peak output current over a wide input supply range.

The MP2329 operates at high efficiency over a wide output current load range based on MPS's proprietary switching loss reduction technique and internal low $R_{DS(ON)}$ power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop combined with the remote differential sense provides good load and line regulation.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The converter requires a minimal number of external components and is available in a QFN-11 (2mmx2mm) package.

FEATURES

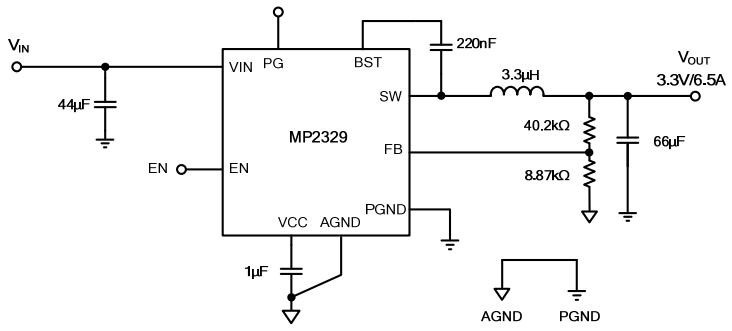
- Wide 4.5V to 24V Operating Input Range
- 105μA Low Quiescent Current
- 6.5A Continuous Output Current
- 7.5A Peak Output Current
- Adaptive Constant-On-Time (COT) Control for Fast Transient
- DC Auto-Tune Loop
- Low $R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Power Good (PG) Indication
- Fixed 700kHz Switching Frequency
- Stable with POSCAP and Ceramic Capacitors
- Internal Soft Start (SS)
- Output Discharge
- OCP, OVP, UVP, and Thermal Shutdown with Auto-Retry
- Available in a QFN-11 (2mmx2mm) Package
- The MPL-AL6050 Inductor Series Matches Best Performance

APPLICATIONS

- Security Cameras
- Portable Devices, XDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purposes

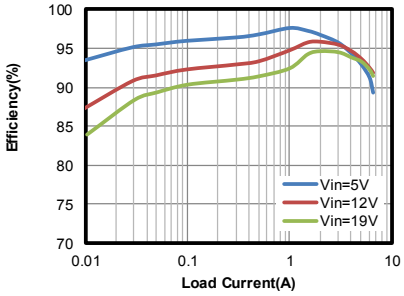
All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



Efficiency

V_{OUT} = 3.3V, L = 3.3μH, DCR = 9mΩ



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2329GG	QFN-11 (2mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g.: MP2329GG–Z)

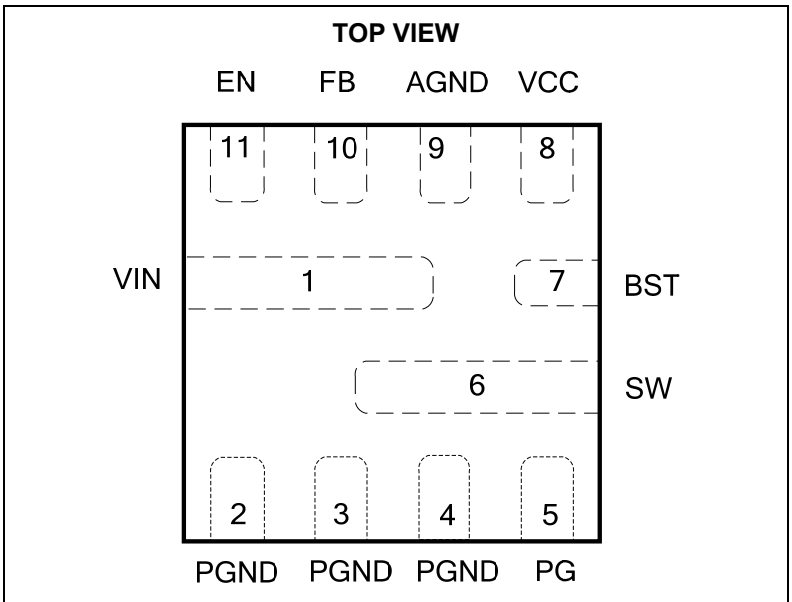
TOP MARKING

FZY

LLL

FZ: Product code of MP2329GG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-11 (2mmx2mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 26V
V_{SW} (DC)..... -1V to V_{IN} + 0.3V
V_{SW} (transient)..... -9V for <2ns,
-5V to V_{IN} + 4V for <25ns (2)
V_{BST}..... V_{SW} + 4.5V
All other pins ..... -0.3V to + 4.5V
Continuous power dissipation (T_A = +25°C) (3)(5)
QFN-11 (2mmx2mm)..... 3.6W
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature .....-65°C to +150°C

ESD Rating

Human-body model (HBM).....1.8KV
Charged-device model (CDM).....2KV

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 4.5V to 24V
Output voltage (V_{OUT})..... 0.6V to 13V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
EV2329-G-00A (5)	34	9	°C/W
QFN-11 (2mmx2mm) (6)	80	16	°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) Measured by using differential oscilloscope probe.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV2329-G-00A, 4-layer PCB.
6) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical value tested at T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (quiescent)	I_{IN}	V_{EN} = 3.3V, V_{FB} = 0.62V		105	145	µA
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			2	µA
MOSFET						
High-side switch on resistance	$HS_{RDS(ON)}$			36		mΩ
Low-side switch on resistance	$LS_{RDS(ON)}$			12		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	5	µA
Current Limit						
Low-side valley current limit	I_{LIMIT_LS}		6	7.5	9	A
Zero-crossing current	I_{ZCD}	V_{OUT} = 3.3V, Lo = 2.2µH	0	150	400	mA
Switching Frequency and Minimum Off Timer						
Switching frequency	F_S	V_{IN} = 12V, V_{OUT} = 3.3V	600	700	800	kHz
Minimum on time [8]	T_{ON_Min}			50		ns
Minimum off time [8]	T_{OFF_Min}			200		ns
Over-Voltage and Under-Voltage Protection (OVP, UVP)						
OVP threshold	V_{OVP}	V_{FB}	125%	130%	135%	V_{REF}
UVP-1 threshold	V_{UVP}	V_{FB}	70%	75%	80%	V_{REF}
UVP-1 hold off timer [8]	T_{OC}	V_{OUT} = 60% V_{REF}		32		µs
UVP-2 threshold	V_{UVP}	V_{FB}	45%	50%	55%	V_{REF}
Reference (REF) and Soft Start (SS)						
REF voltage	V_{REF}		590	600	610	mV
Soft-start time [8]	T_{SS}		1.1	1.7	2.3	ms
Enable (EN) and Under-Voltage Lockout (UVLO)						
Enable rising threshold	V_{EN_Rising}		1.15	1.25	1.35	V
Enable hysteresis	V_{EN_HYS}			150		mV
Enable input current	I_{EN}	V_{EN} = 3.3V		3.3		µA
VCC UVLO threshold rising	VCC_{Vth_R}		3.1	3.3	3.5	V
VCC UVLO threshold hysteresis	VCC_{HYS}			420		mV
VIN UVLO threshold rising	VIN_{VTH_R}		4.2	4.35	4.48	V
VIN UVLO threshold hysteresis	VIN_{HYS}			550		mV
VCC Regulator						
VCC voltage	V_{CC}		3.45	3.65	3.85	V
VCC load regulation	V_{CC_Reg}	I_{VCC} = 5mA		5		%
Thermal Protection						
Thermal shutdown [8]	T_{SD}			150		°C
Thermal shutdown hysteresis [8]	T_{SD_HYS}			25		°C

NOTES:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by engineering sample characterization.

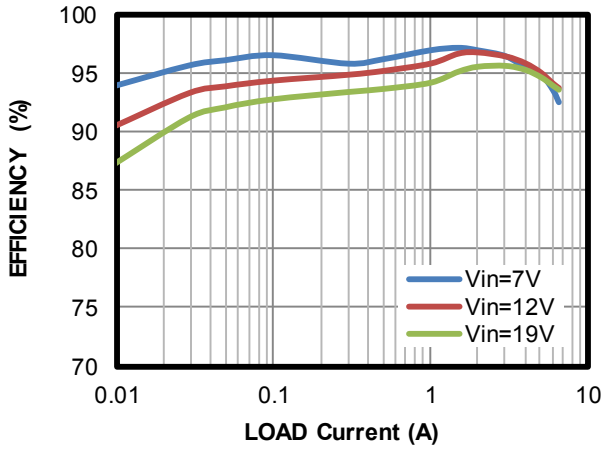
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = +25°C, unless otherwise noted.

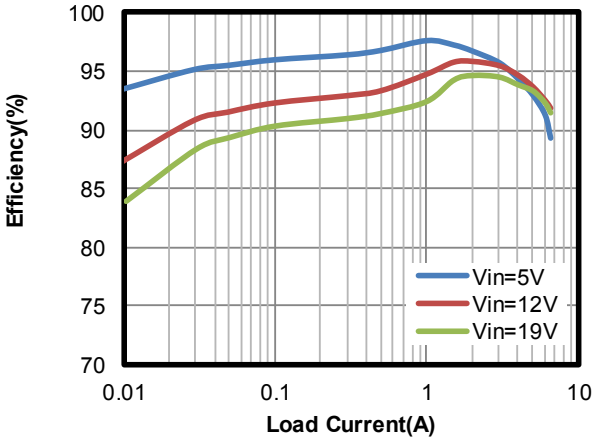
Efficiency

V_{OUT} = 5V, L = 3.3µH, DCR = 9mΩ



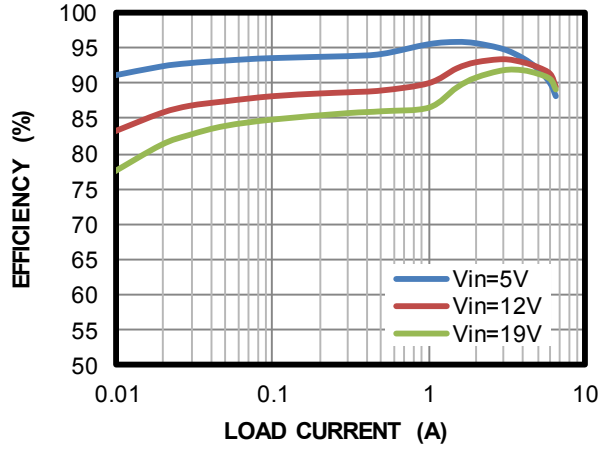
Efficiency

V_{OUT} = 3.3V, L = 3.3µH, DCR = 9mΩ



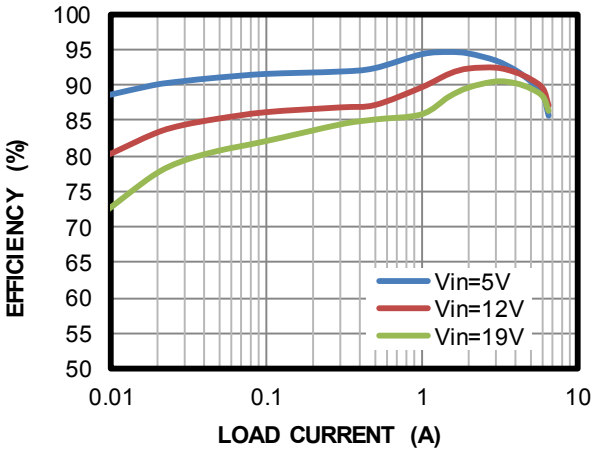
Efficiency

V_{OUT} = 2.5V, L = 2.2µH, DCR = 11.4mΩ



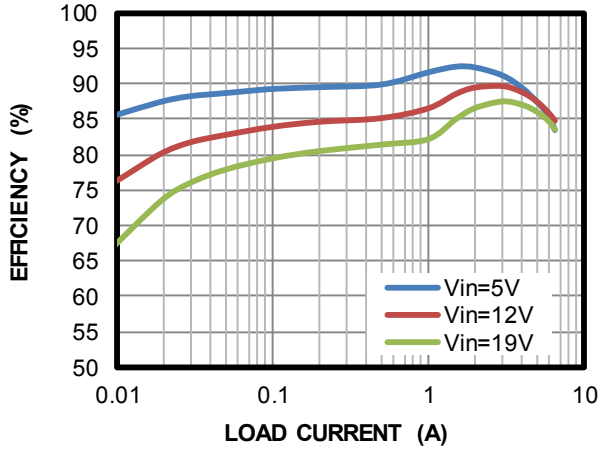
Efficiency

V_{OUT} = 1.8V, L = 2.2µH, DCR = 11.4mΩ



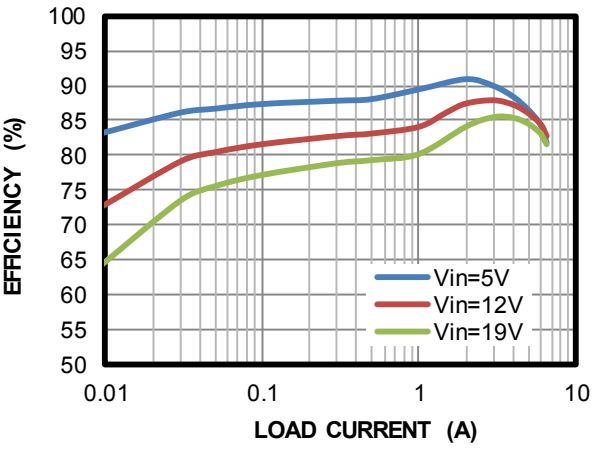
Efficiency

V_{OUT} = 1.2V, L = 1.5µH, DCR = 6.6mΩ



Efficiency

V_{OUT} = 1V, L = 1.5µH, DCR = 6.6mΩ

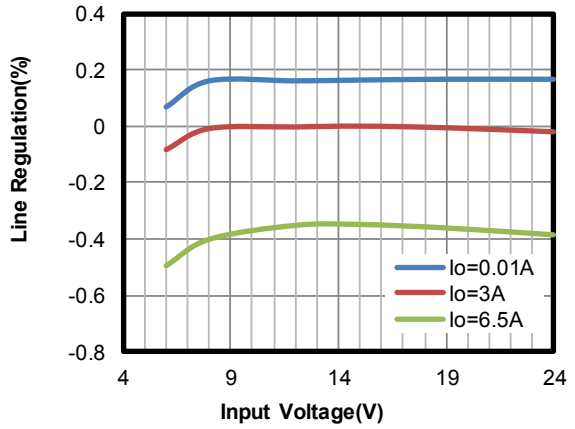


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

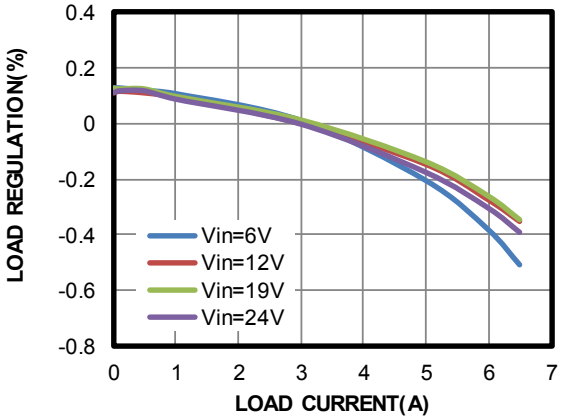
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = +25°C, unless otherwise noted.

Line Regulation

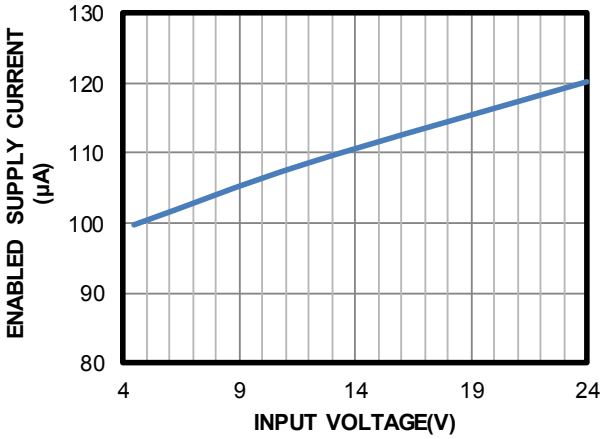


Load Regulation



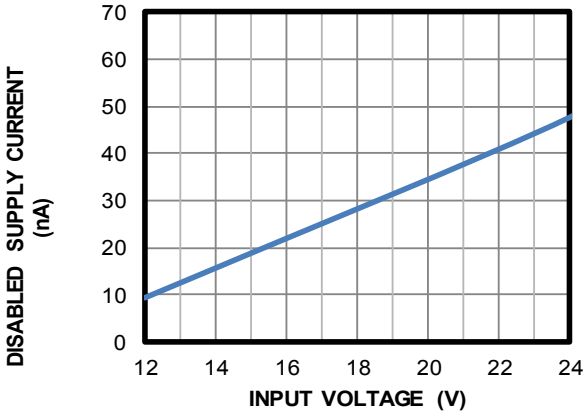
Enabled Supply Current vs. Input Voltage

V_{EN} = 3.3V, V_{FB} = 0.62V



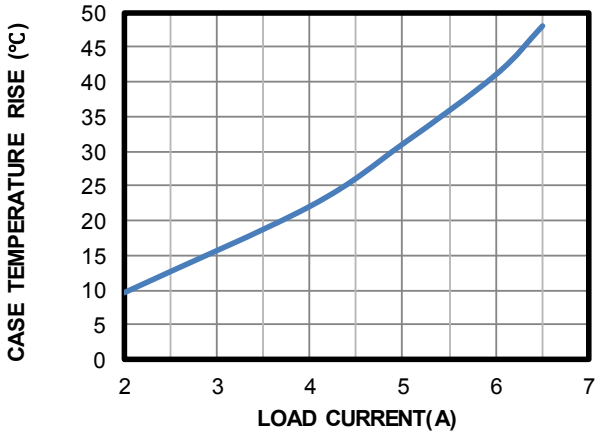
Disabled Supply Current vs. Input Voltage

V_{EN} = 0V

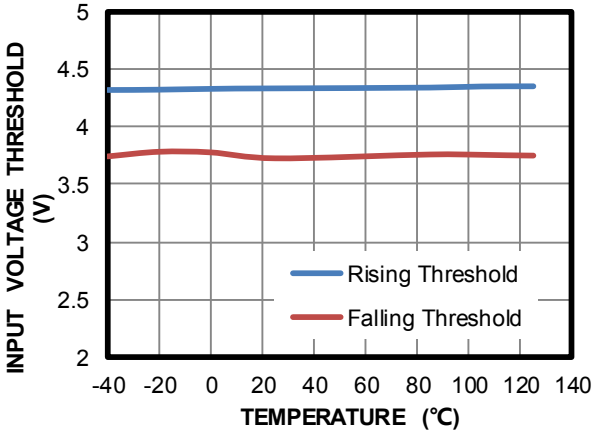


Case Temperature Rise vs. Load Current

V_{IN} = 19V, V_{OUT} = 3.3V



Input Voltage Threshold vs. Temperature

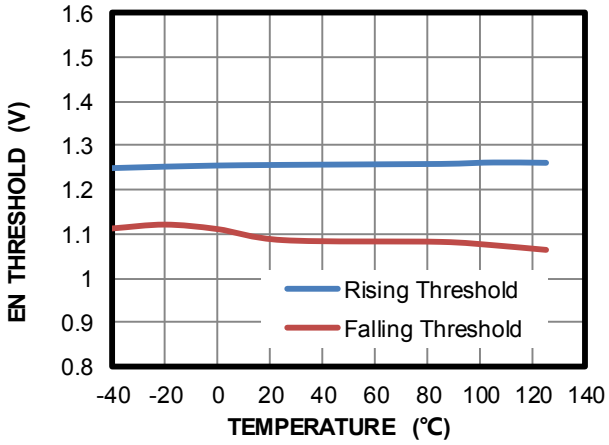


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

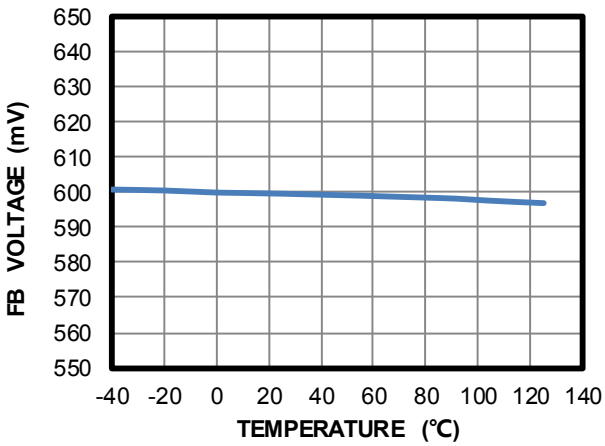
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = +25°C, unless otherwise noted.

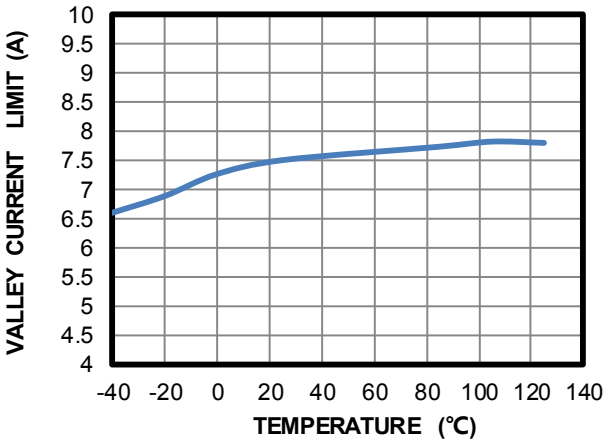
EN Threshold vs. Temperature



FB Voltage vs. Temperature



Valley Current Limit vs. Temperature



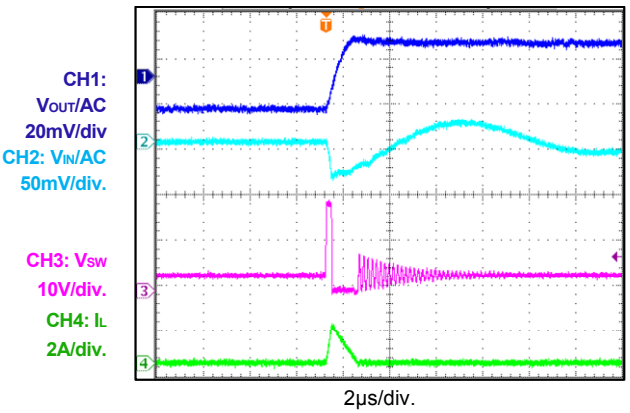
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = +25°C, unless otherwise noted.

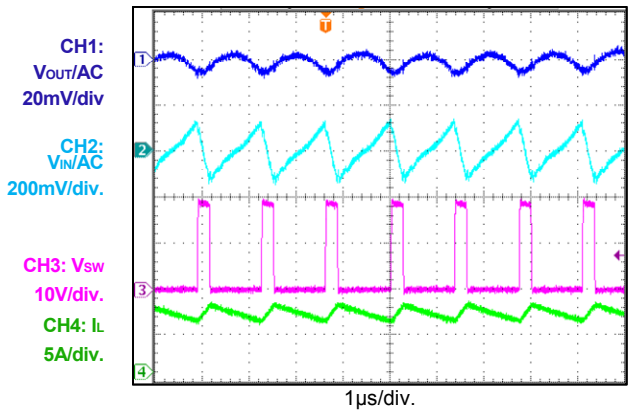
Input/Output Ripple

I_{OUT} = 0A



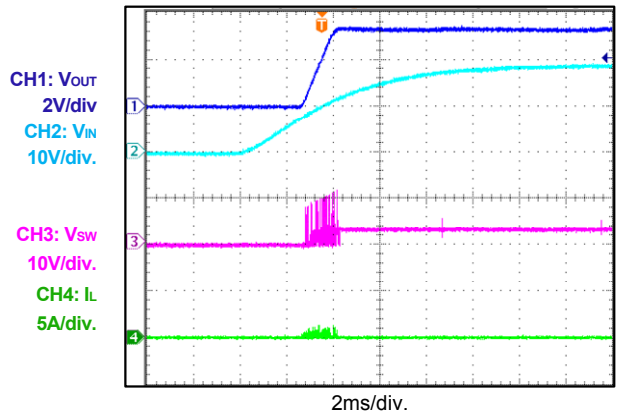
Input/Output Ripple

I_{OUT} = 6.5A



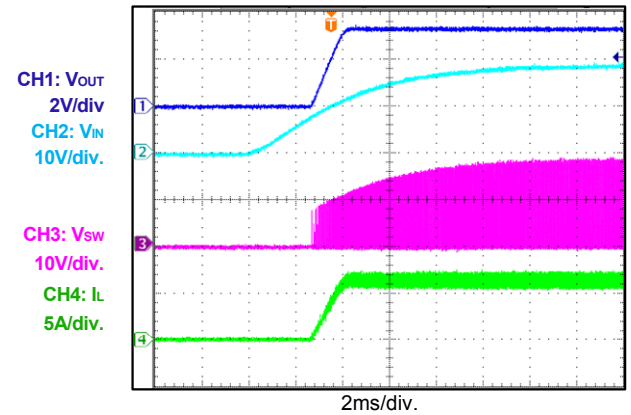
Start-Up through Input Voltage

I_{OUT} = 0A



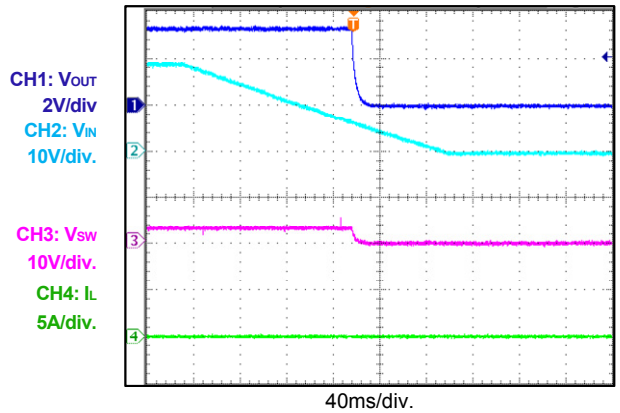
Start-Up through Input Voltage

I_{OUT} = 6.5A



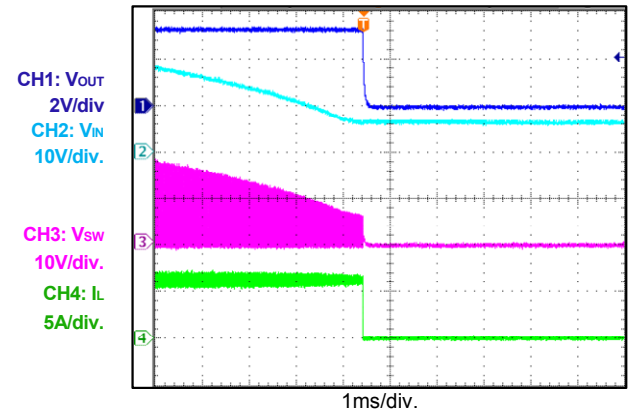
Shutdown through Input Voltage

I_{OUT} = 0A



Shutdown through Input Voltage

I_{OUT} = 6.5A



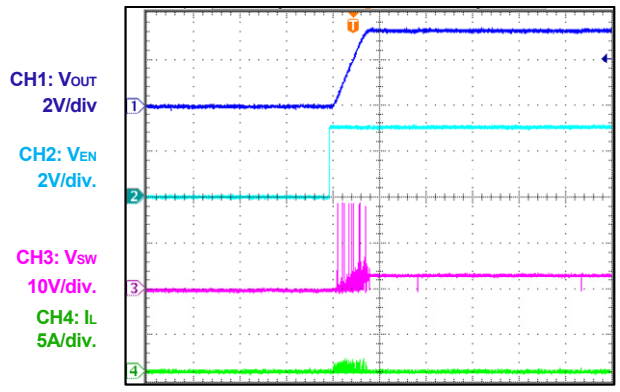
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = +25°C, unless otherwise noted.

Start-Up through Enable

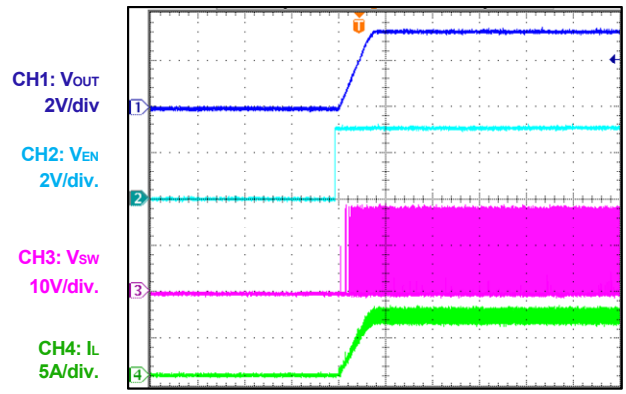
I_{OUT} = 0A



2ms/div.

Start-Up through Enable

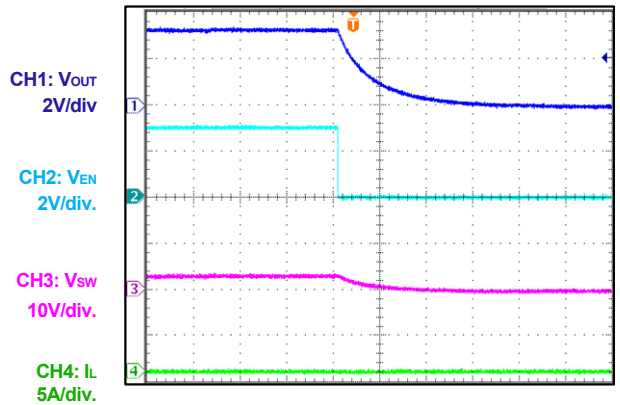
I_{OUT} = 6.5A



2ms/div.

Shutdown through Enable

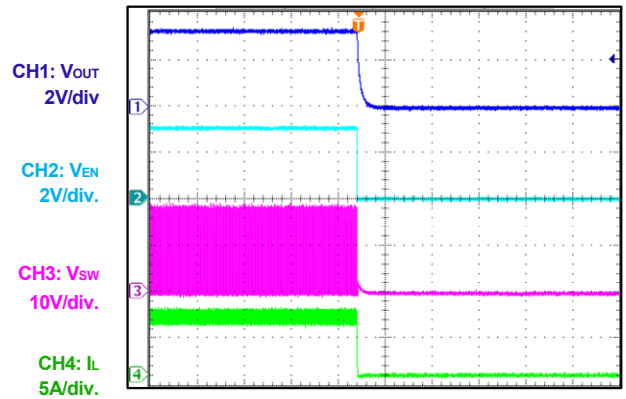
I_{OUT} = 0A



4ms/div.

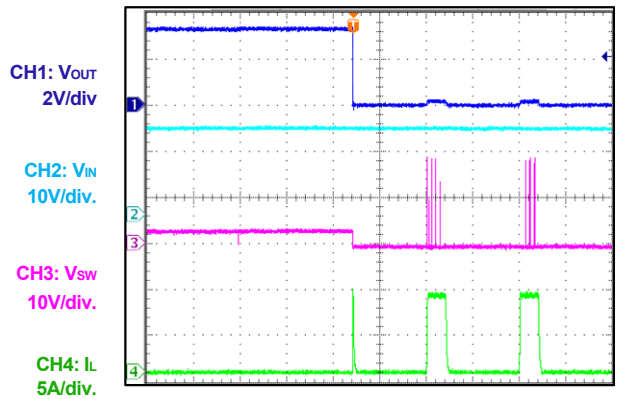
Shutdown through Enable

I_{OUT} = 6.5A



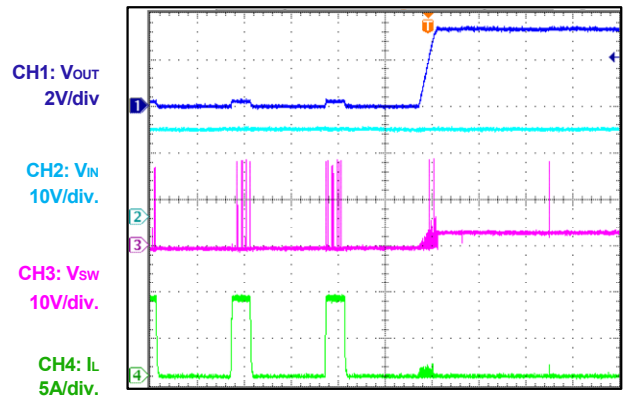
400µs/div.

Short-Circuit Entry



4ms/div.

Short-Circuit Recovery



4ms/div.

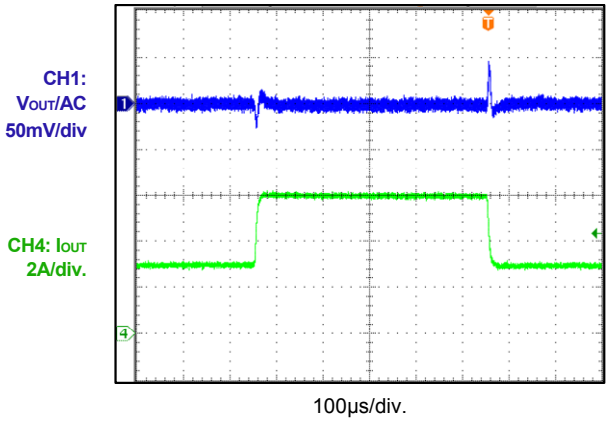
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = +25°C, unless otherwise noted.

Load Transient

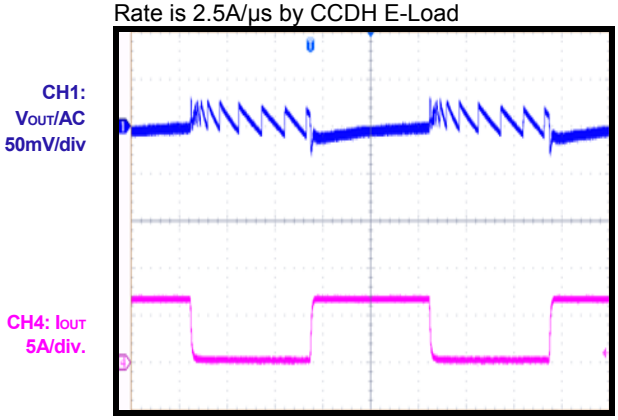
I_{OUT} = 3 - 6A



100µs/div.

Load Transient

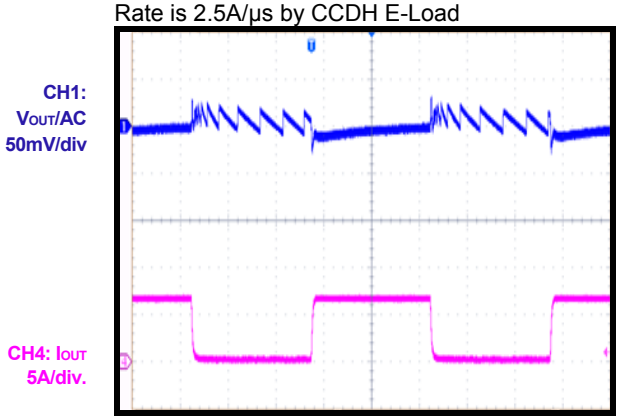
V_{OUT}=1V, I_{OUT} = 0 – 6.5A, C_{OUT}=22µF*4, Slew Rate is 2.5A/µs by CCDH E-Load



200µs/div.

Load Transient

V_{OUT}=1V, I_{OUT} = 0 – 6.5A, C_{OUT}=22µF*5, Slew Rate is 2.5A/µs by CCDH E-Load



200µs/div.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PIN FUNCTIONS

PIN #	Name	Description
1	VIN	**Supply voltage.** VIN supplies power for the internal MOSFET and regulator. The MP2329 operates from a +4.5V to +24V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for this input trace.
2 -4	PGND	**Power ground.** Use wide PCB traces and multiple vias to make the connection.
5	PG	**Power good output.** The output of PG is an open drain.
6	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the PWM duty cycle on time. The inductor current drives SW negative during the off time. The on resistance of the low-side switch and the internal diode fixes the negative voltage. Use wide and short PCB traces to make the connection.
7	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
8	VCC	**Internal VCC LDO output.** The driver and control circuits are powered by this voltage. Decouple VCC with a minimum 1μF ceramic capacitor placed as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
9	AGND	**Signal logic ground.** AGND is the Kelvin connection to PGND.
10	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage. Place the resistor divider as close to FB as possible. Avoid vias on the FB traces and keep the V_{SEN} trace far away from the SW node. Vias should also be avoided on the V_{SEN} trace.
11	EN	**Buck enable pin.** EN is a digital input that turns the buck regulator on or off. When the power supply of the control circuit is ready, drive EN high to turn on the buck regulator. Drive EN low to turn off the regulator. Connect EN to VIN through a resistive voltage divider for automatic start-up. Do not make the EN voltage over 4.5V at any time. Do not float EN.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

BLOCK DIAGRAM

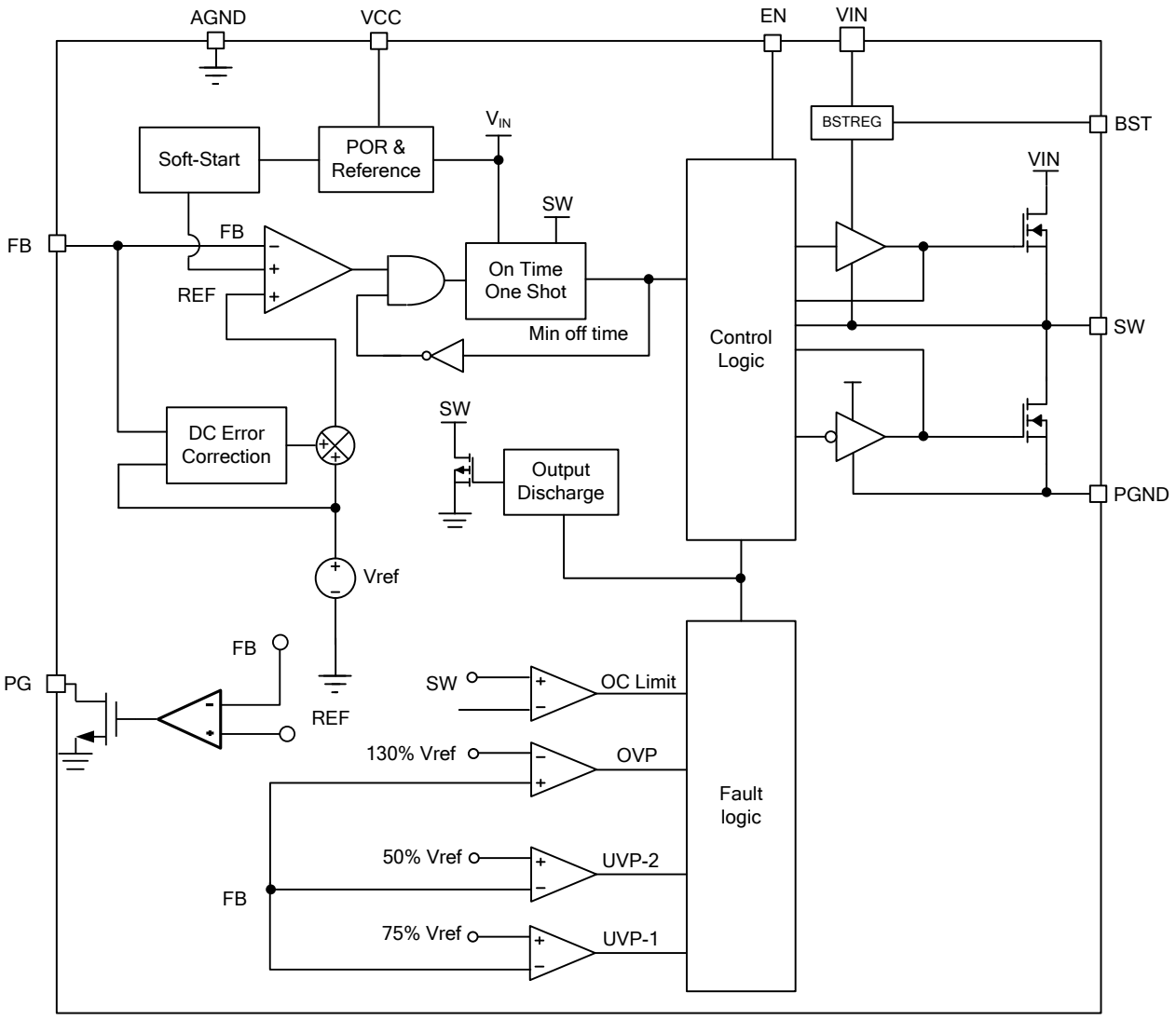


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

OPERATION

The MP2329 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide a fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation in this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead-time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until the next period.

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

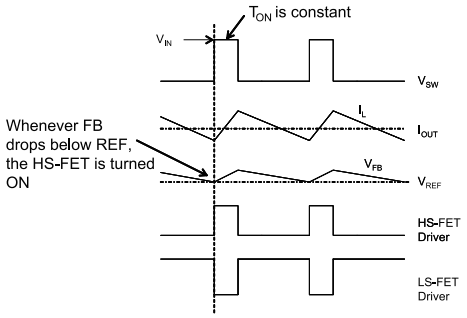


Figure 2: Heavy-Load Operation

Light-Load Operation

The inductor current decreases as the load decreases. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, V_{FB} does not reach V_{REF} while the inductor current is approaching zero. The LS-FET driver switches to tri-state (Hi-Z) whenever the inductor current reaches zero. As a result, light-load efficiency is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the MP2329 reduces the switching frequency naturally. High efficiency is then achieved at light load.

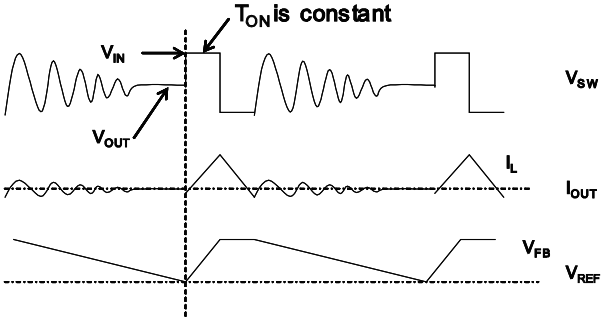


Figure 3: Light-Load Operation

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

As the output current increases from the light-load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, so the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_S \times V_{IN}} \quad (1)$$

The device reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Large Duty Cycle Operation

When V_{IN} is below 7V, V_{OUT} is above 4.2V, so the MP2329 reduces the switching frequency to about 280kHz to support large duty operation. If V_{OUT} is below 3.9V, the MP2329 switches back to a normal switching frequency.

Jitter and FB Ramp

Jitter occurs in both PWM and skip mode when noise in the V_{FB} ripple propagates a delay to the HS-FET driver (see Figure 4 and Figure 5). Jitter can affect system stability with noise immunity proportional to the steepness of V_{FB}'s downward slope, so the jitter in DCM is usually larger than that in CCM. However, the V_{FB} ripple does not affect noise immunity directly.

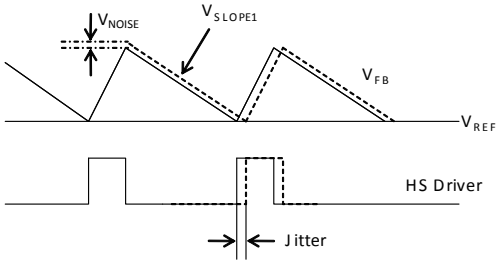


Figure 4: Jitter in PWM Mode

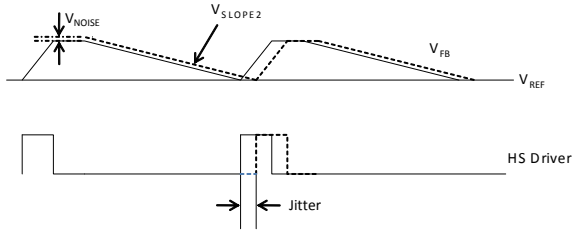


Figure 5: Jitter in Skip Mode

Operating with External Ramp Compensation

The MP2329 is usually able to support ceramic output capacitors without an external ramp. However, in some cases, the internal ramp may not be enough to stabilize the system or the jitter is too big, so external ramp compensation is needed. See the Application Information section on page 17 for design steps with external ramp compensation.

Configuring the EN Control

The enable pin (EN) is used to enable or disable the entire chip. Pull EN high to turn on the regulator. Pull EN low to turn off the regulator. Do not float EN.

For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. There is an internal 1MΩ resistor from EN to GND. To determine the automatic start-up voltage, calculate the values of the pull-up resistor (R_{UP} from VIN to EN) and the pull-down resistor (R_{DOWN} from EN to GND) with Equation (2):

$$V_{IN-START} = 1.25 \times \frac{R_{UP} + R_{DOWN}//1000K}{R_{DOWN}//1000K} (V) \quad (2)$$

For example, for R_{UP} = 150kΩ and R_{DOWN} = 51kΩ, set $V_{IN-START}$ to 5.11V.

The EN voltage must not exceed 4.5V max to avoid damaging the internal circuit.

Power Good (PG)

Power good (PG) indicates whether the output voltage is in the normal range compared to the internal reference voltage. PG is an open-drain structure and requires an external pull-up supply. During power-up, the PG output is pulled low. This indicates to the system to remain off and keeps the output load to a minimum. This helps reduce inrush current during start-up.

When the output voltage is higher than 95% and lower than 115% of the internal reference voltage and the soft start is finished, the PG signal is pulled high. When the output voltage is lower than 90% after the soft start finishes, the PG signal remains low. When the output voltage is higher than 115% of the internal reference, PG is switched low. PG signals back

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

to high after the output voltage drops below 105% of the internal reference voltage. The PG output is pulled low when either EN under-voltage lockout (UVLO), input UVLO, over-current protection (OCP), or over-temperature protection (OTP) is triggered.

Soft Start (SS)

The MP2329 employs a soft start (SS) mechanism to ensure a smooth output during power-up. When the MP2329 starts up, the internal V_{REF} ramps up gradually, so the output voltage ramps up smoothly as well. Once the reference voltage reaches the target value, the soft start finishes, and the MP2329 enters steady-state operation.

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

Over-Current Limit (OCL)

The MP2329 has a cycle-by-cycle over-current limiting control (OCL). The current-limit circuit employs a valley current-sensing algorithm. The MP2329 uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle, even if FB is lower than REF. Figure 6 shows the detailed operation of the valley current limit.

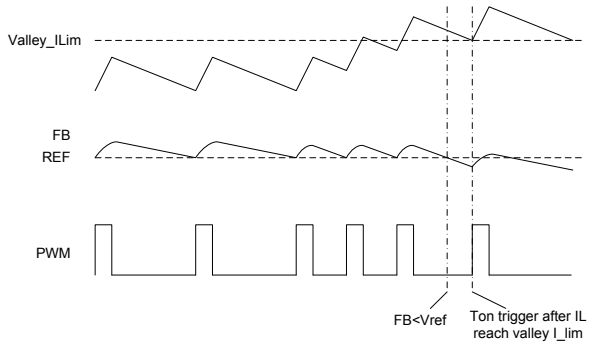


Figure 6: Valley Current-Limit Control

Since the comparison is done during the LS-FET on state, the over-current (OC) trip level sets the valley level of the inductor current.

The maximum load current at the over-current threshold (I_{OC}) can be calculated with Equation (3):

$$I_{OC} = I_limit + \frac{\Delta I_{inductor}}{2} \quad (3)$$

The OCL itself just limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, so the output voltage tends to fall off. Eventually, the current ends up crossing the under-voltage protection (UVP) threshold, and the MP2329 enters hiccup protection mode.

Over-/Under-Voltage Protection (OVP/UVP)

The MP2329 monitors a resistor-divided V_{FB} to detect over- and under-voltage. When V_{FB} becomes higher than 130% of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the circuit latches as the HS-FET driver turns off. A discharge MOSFET on SW turns on to discharge the output capacitor voltage.

When V_{FB} drops below 75% but remains higher than 50% of V_{REF}, the UVP-1 comparator output goes high, and the MP2329 enters hiccup mode if V_{FB} remains in this range for about 32µs. During this period, the valley current limit helps control the inductor current.

When V_{FB} drops below 50% of V_{REF}, the UVP-2 comparator output goes high, and the MP2329 enters hiccup mode directly after the comparator and logic delay.

Under-Voltage Lockout (UVLO) Protection

The MP2329 has two under-voltage lockout (UVLO) protections: VCC UVLO and V_{IN} UVLO. The MP2329 starts up only when both VCC and VIN exceed their respective UVLO thresholds. The MP2329 shuts down when either VCC is lower than the VCC falling threshold voltage or VIN is lower than the VIN falling threshold. Both UVLO protections are non-latch off.

If an application requires a higher UVLO, use EN to adjust the input voltage UVLO by using two external resistors (see Figure 7). Note that the EN voltage must not exceed the 4.5V maximum to avoid damaging the internal circuit.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

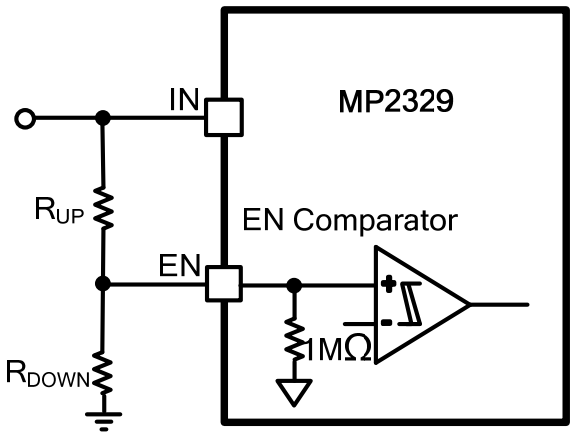


Figure 7: Adjustable UVLO

Thermal Shutdown

Thermal shutdown is employed in the MP2329. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150°C), the converter shuts off. This is a non-latch protection. There is a hysteresis of about 25°C. Once the junction temperature drops to about 125°C, a soft start is initiated.

Output Discharge

The MP2329 discharges the output when the controller is turned off by a protection function (UVP, OCP, OVP, UVLO, or thermal shutdown). The discharge resistor on the output is 40Ω, typically.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage without an External Ramp

The MP2329 has an internal ramp. When the internal compensation is sufficient for stable operation with ceramic output capacitors, the MP2329 does not require external ramp compensation. The output voltage is then set by feedback resistors R1 and R2 (see Figure 8).

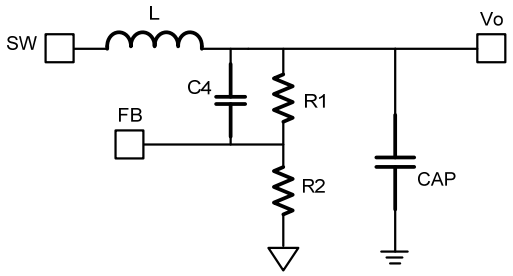


Figure 8: Simplified Circuit without External Ramp

First, choose a value for R2. R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, while a large R2 makes FB noise-sensitive. It is recommended to make R2 between 5 - 100kΩ. Considering the output ripple, determine R1 with Equation (4):

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (4)$$

C4 acts as a feed-forward capacitor to improve the transient. A larger C4 leads to better transient but more noise sensitivity.

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Parameters Selection for Common Output Voltages (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L (μH)
5	40.2	5.49	33	3.3
3.3	40.2	8.87	33	3.3
2.5	40.2	12.7	33	2.2
1.8	40.2	20	33	2.2
1.5	40.2	26.7	33	1.5
1.2	40.2	40.2	33	1.5
1	40.2	60.4	33	1.5

NOTE:

9) For additional component parameters, please refer to the "Typical Application Circuits" on page 21 to page 23.

Setting the Output Voltage with an External Ramp

If the system is not stable enough or the jitter is too large when ceramic capacitors are used in the output, an external voltage ramp should be added to FB through a resistor (R4) and capacitor (C4). Since an internal ramp is already added in the system, a 1MΩ (R4), 220pF (C4) ramp is sufficient for the ramp, typically.

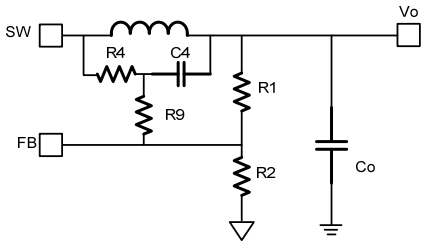


Figure 9: Simplified Circuit with External Ramp

Besides the R1 and R2 divider, the output voltage is also influenced by R4 (see Figure 9). R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, but a large R2 makes FB noise-sensitive. It is recommended to make R2 between 5 - 100kΩ. The value of R1 is then determined with Equation (5):

$$R_1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \cdot R_2 \quad (5)$$

Usually, R9 is set to 0Ω. To set a pole for better noise immunity, calculate R9 with Equation (6):

$$R_9 = \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (6)$$

It is recommended for R9 to be in the range of 100Ω to 1kΩ to reduce its influence on the ramp.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended since they are fairly stable with temperature fluctuations.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (7):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (8):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (10):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (10)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (11)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance.

For simplification, the output voltage ripple can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The output ripple can be approximated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (13)$$

The maximum output capacitor limitation should also be considered in the design application. The MP2329 has a soft-start time of about 1.7ms. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and fails to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (14):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (14)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{ss} is the soft-start time.

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30 - 50% of the maximum output current and to keep the peak inductor current below the maximum switch current limit. The inductance value can be calculated with Equation (15):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, including short current.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
Select family series (MPL-AL)	1.5μH to 3.3μH	MPS
MPL-AL6050-1R5	1.5μH	MPS
MPL-AL6050-2R2	2.2μH	MPS
MPL-AL6050-3R3	3.3μH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A four-layer layout is recommended for better thermal performance. For best results, refer to Figure 11 and follow the guidelines below.

1. Place the high current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitors as close to VIN and PGND as possible.
3. Place the decoupling capacitor as close to VCC and AGND as possible.
4. Keep the switching node (SW) short and away from the feedback network.
5. Keep the BST voltage path as short as possible.
6. Keep the VIN and PGND pads connected with a large copper to achieve better thermal performance.
7. Add several vias close to the VIN and PGND pads to help with thermal dissipation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

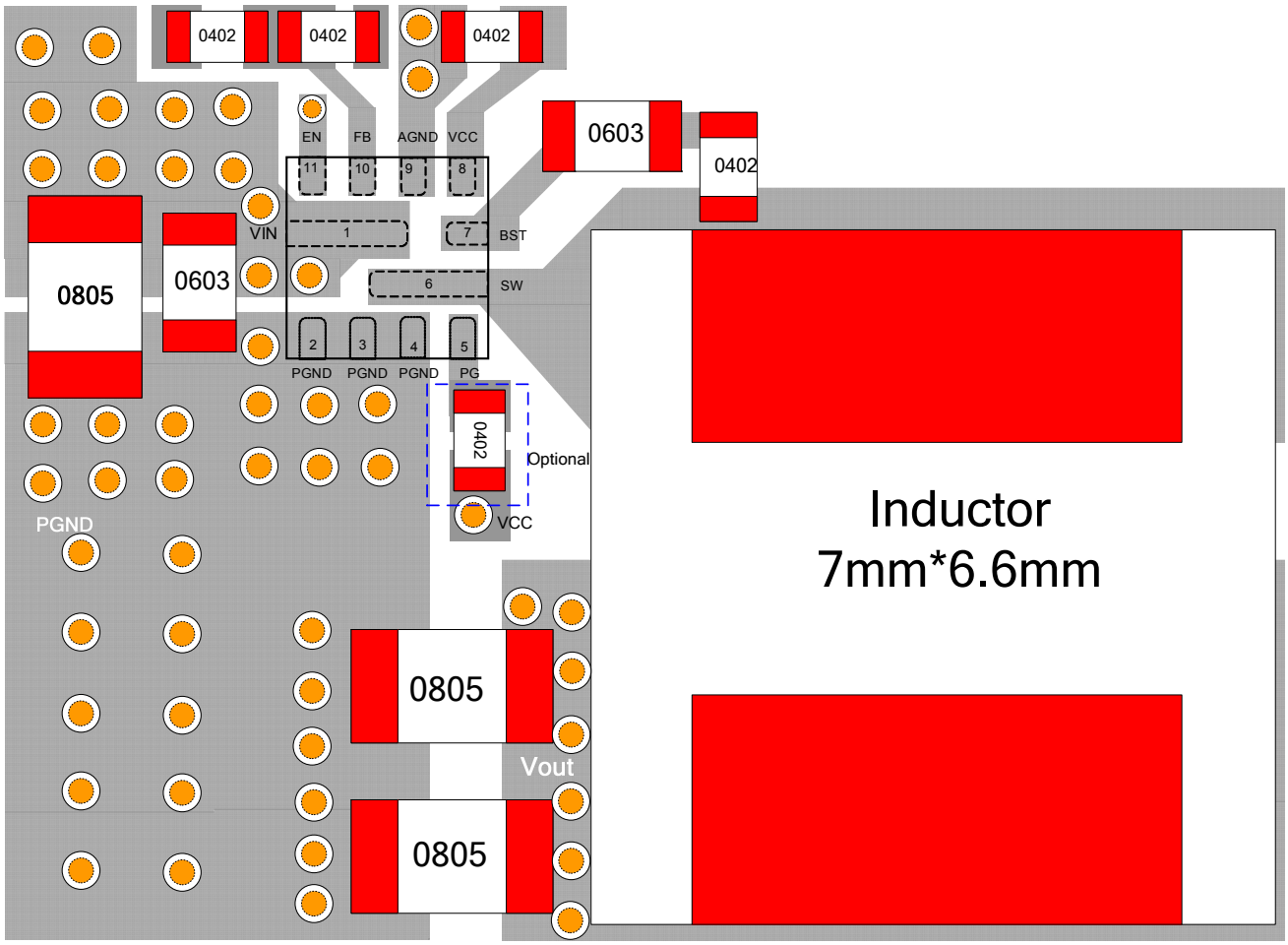


Figure 10: Recommended Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Design Example

Table 3 shows a design example when ceramic capacitors are applied.

Table 3: Design Example

V_{IN}	8V to 24V
V_{OUT}	3.3V
I_{OUT}	6.5A

The detailed application schematics are shown in Figure 11 through Figure 17. The typical performance and waveforms are shown in the Typical Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS (10)

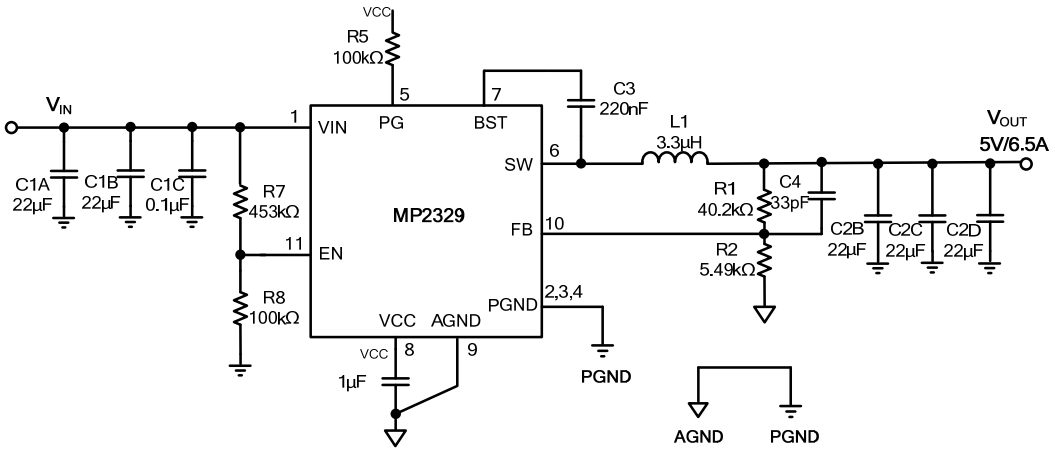


Figure 11: V_{IN} = 19V, V_{OUT} = 5V/6.5A

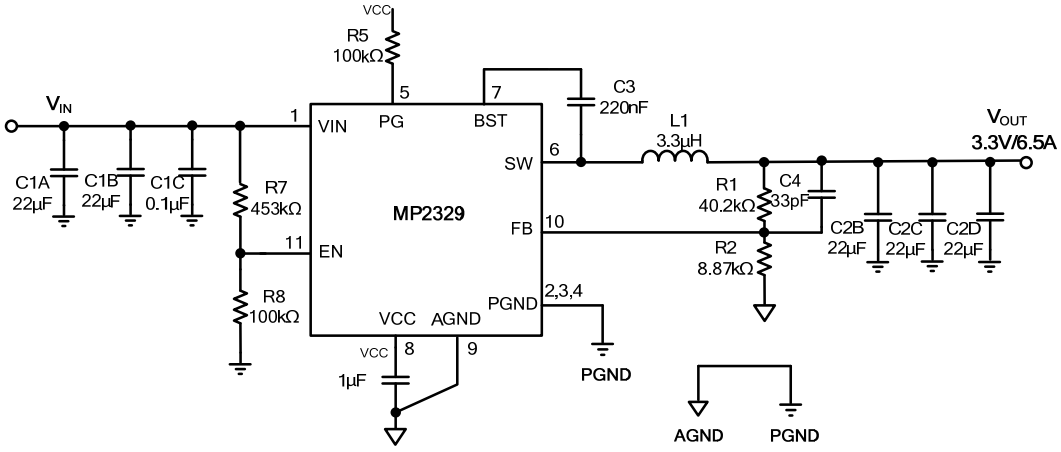


Figure 12: V_{IN} = 19V, V_{OUT} = 3.3V/6.5A

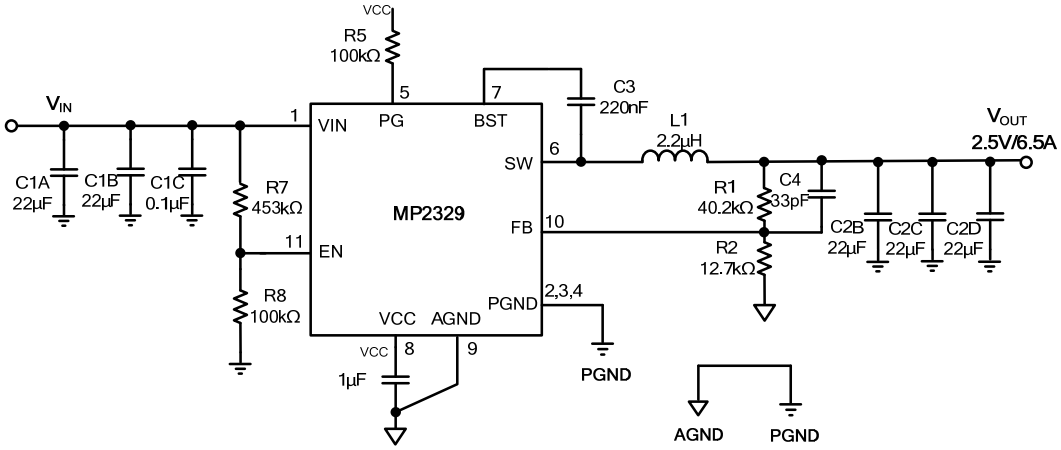


Figure 13: V_{IN} = 19V, V_{OUT} = 2.5V/6.5A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

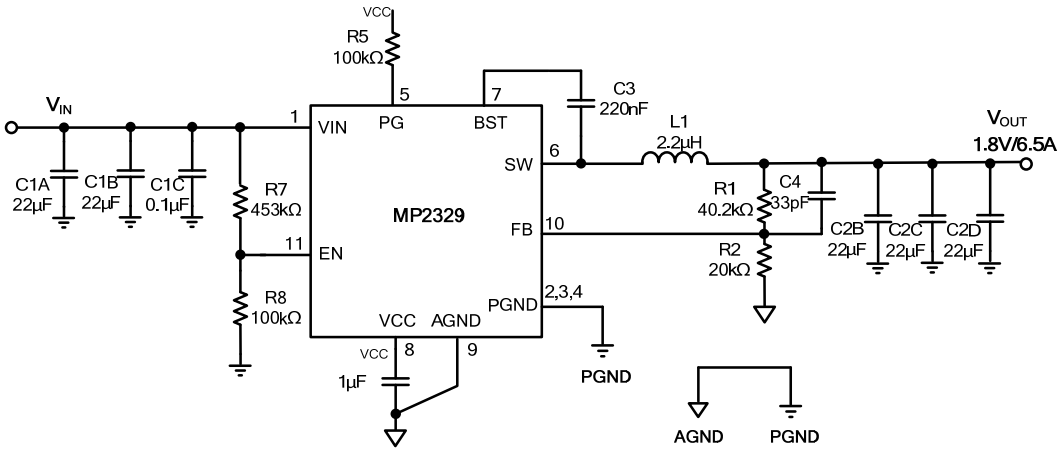


Figure 14: V_{IN} = 19V, V_{OUT} = 1.8V/6.5A

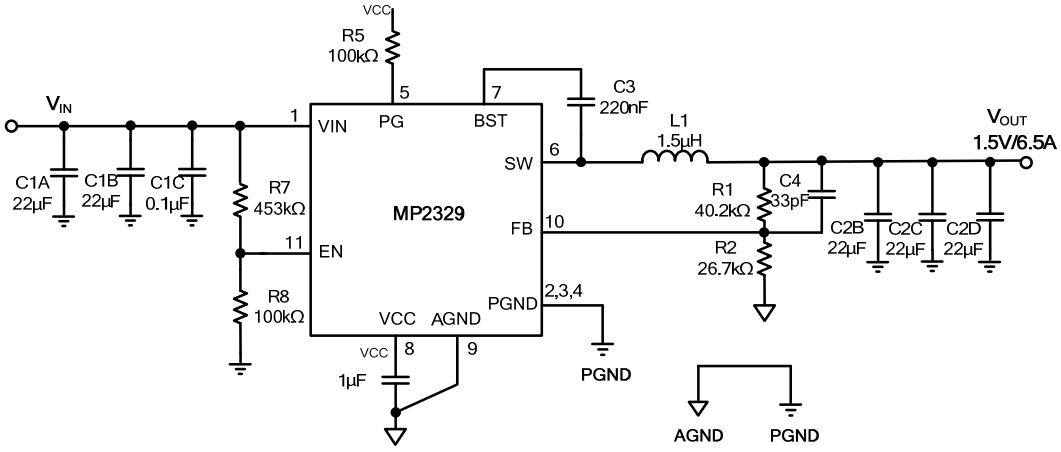


Figure 15: V_{IN} = 19V, V_{OUT} = 1.5V/6.5A

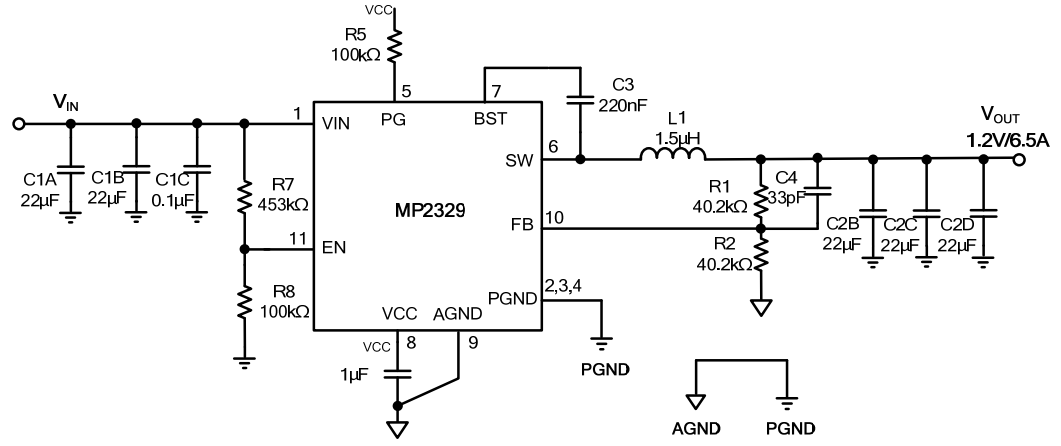


Figure 16: V_{IN} = 19V, V_{OUT} = 1.2V/6.5A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

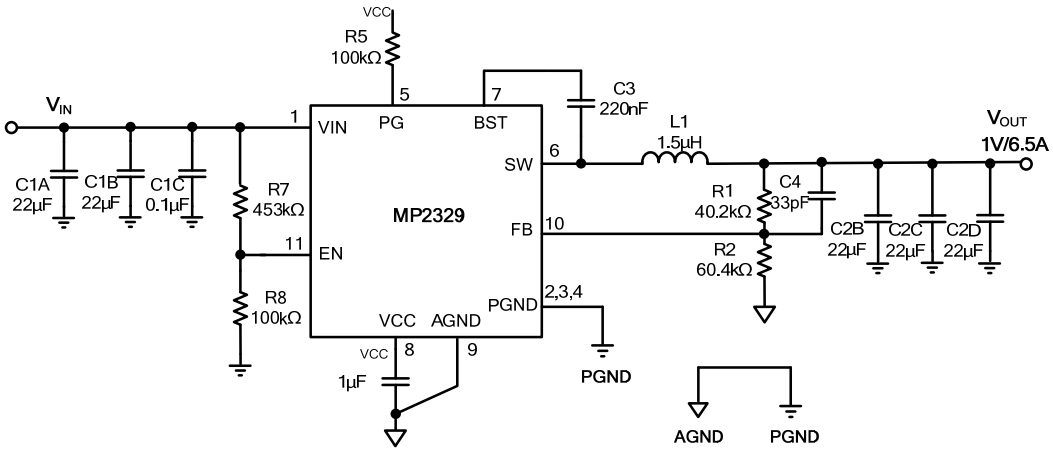


Figure 17: V_{IN} = 19V, V_{OUT} = 1V/6.5A

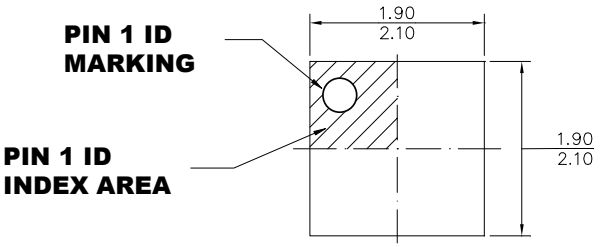
NOTE:

10) The EN resistor divider sets the VIN threshold to 7.5V. For 5V input applications, change the EN resistor accordingly.

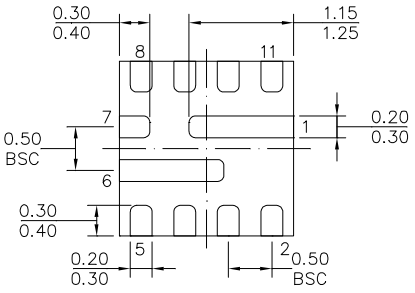
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE INFORMATION

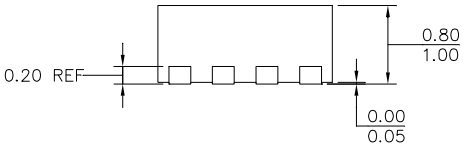
QFN-11 (2mmx2mm)



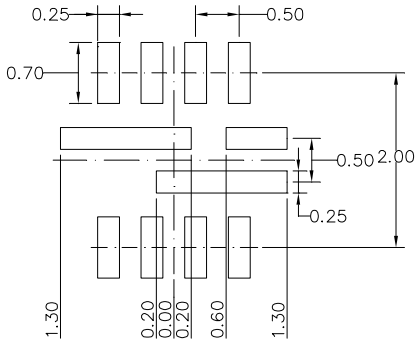
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1 AND PIN6 HAVE THE SAME LENGTH AND WIDTH

2) ALL DIMENSIONS ARE IN MILLIMETERS.

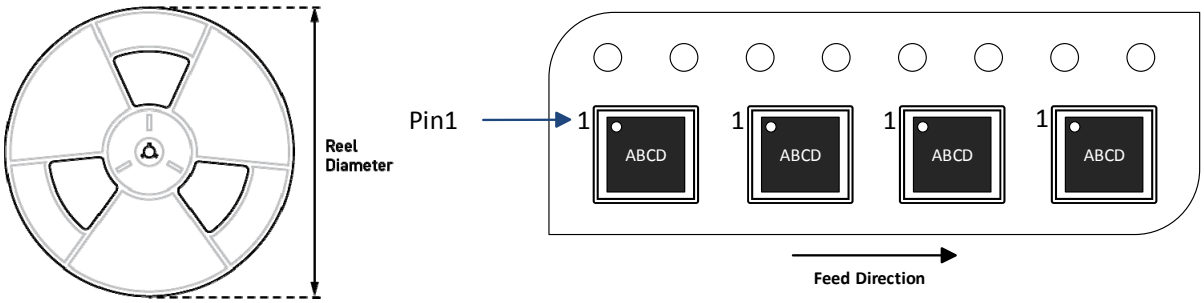
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.

4) JEDEC REFERENCE IS MO-220, VARIATION VCCD.

5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2329GG–Z	QFN-11 (2mmx2mm)	5000	N/A	13in.	12mm	8mm

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.