MP2322

1A, 3-22V, 5µA I_Q, Synchronous, Step-Down Converter in 1.5x2mm QFN

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MP2322A

DESCRIPTION

The MP2322 is a synchronous, rectified, step-down, switch-mode converter with built-in internal power MOSFETs and high light-load efficiency. The MP2322 offers a very compact solution that achieves 1A of continuous output current with excellent load and line regulation over a wide input supply range.

The MP2322 switching edge is optimized for EMI reduction. Constant-on-time (COT) control provides seamless mode transition and a fast load transient response.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), and thermal shutdown.

The MP2322 requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-8 (1.5mmx2mm) package.

FEATURES

- Wide 3V to 22V Operating Input Range
- 5µA Low I_Q
- 1A Load Current
- 260mΩ/120mΩ $R_{DS(ON)}$ Internal Power MOSFETs
- High Efficiency from 100µA to 1A Load during V_{IN} from 4V to 22V
- Power-Save Mode (PSM) in Light-Load Condition
- 1.25MHz Fixed Switching Frequency during CCM
- T_{ON} Extension to Support Large Duty Cycles
- Power Good (PG) Indication
- EN Shutdown Output Discharge
- OCP and OVP and Hiccup
- Output Adjustable from 0.6V
- Available in a QFN-8 (1.5mmx2mm) Package

APPLICATIONS

- IOT
- Home Automation, Home Security
- Single- or Multi-Cell Li-Ion Battery Systems
- Multi-Cell Dry Battery Systems
- 12V Input Power Rails
- White Goods

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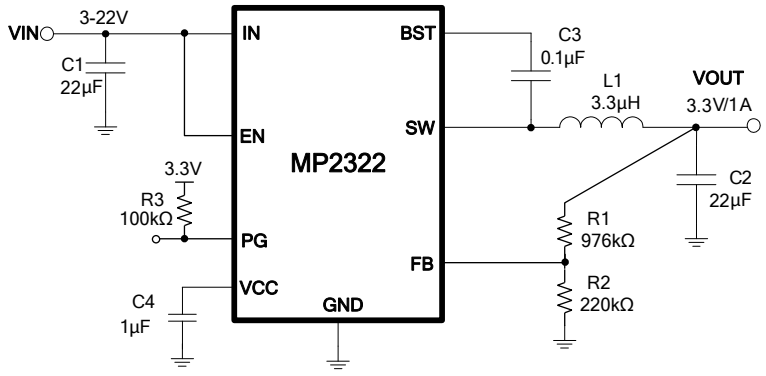
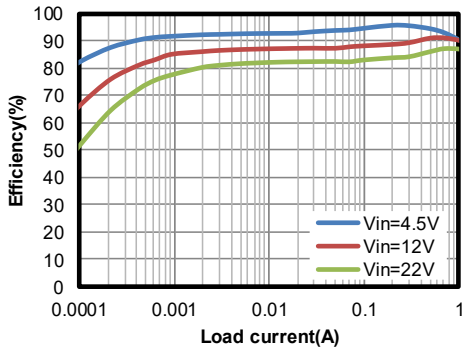
TYPICAL APPLICATION



Efficiency vs. Output Current

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, DCR = 9mΩ



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2322GQH	QFN-8 (1.5mmx2mm)	*See Below*

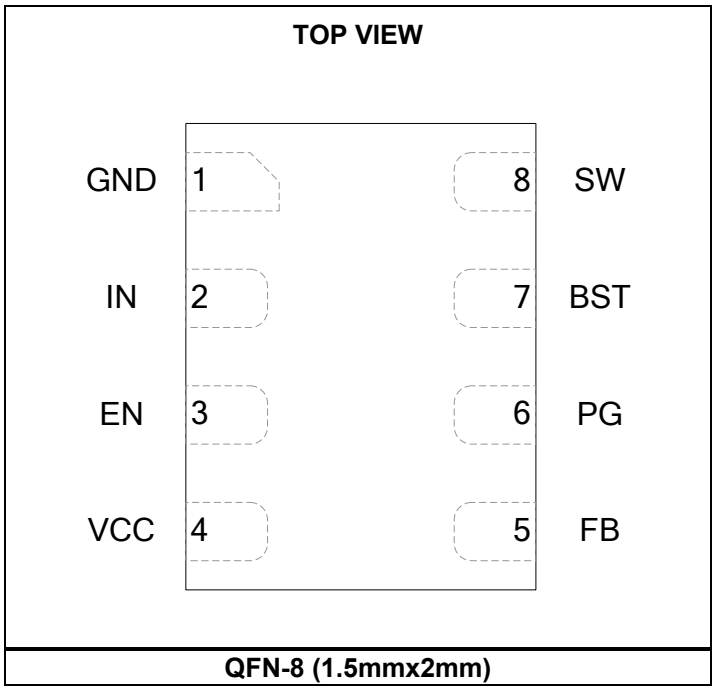
* For Tape & Reel, add suffix –Z (e.g.: MP2322GQH–Z).

TOP MARKING

$\overline{\text{FN}}$
LL

FN: Product code of MP2322GQH
LL: Lot number

PACKAGE REFERENCE



QFN-8 (1.5mmx2mm)

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PIN FUNCTIONS

Package Pin #	Name	Description
1	GND	**System ground.** GND is the reference ground for the regulated output voltage and requires special consideration during the PCB layout.
2	IN	**Supply voltage.** The MP2322 operates from a +3V to +22V input rail. A capacitor (C1) is required to decouple the input rail. Use wide PCB traces or multiple vias to make the connection.
3	EN	**Enable control.** Apply a logic high voltage to EN to enable the IC. Pull EN to logic low to disable the IC. Do not float EN.
4	VCC	**Internal 3.3V LDO output.** VCC powers the driver and control circuits. Decouple VCC with a minimum 1µF ceramic capacitor placed as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
5	FB	**Feedback.** FB sets the output voltage when connected to the tap of an external resistor divider connected between output and GND.
6	PG	**Power good output.** PG is an open drain. PG indicate both output under-voltage (UV) and over-voltage (OV) conditions. PG does not respond to BST low/UV conditions.
7	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
8	SW	**Switch output.** Connect SW using wide PCB traces.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{EN} ..... -0.3V to +24V
V_{SW} ..... -0.3V (-5V < 10ns) to +24V (28V < 10ns)
V_{BST} ..... V_{SW} + 4V
V_{PG} 6.5V
All other pins ..... -0.3V to +4.3V
Continuous power dissipation (T_A = +25°C) (2) 1.14W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3V to 22V
Output Voltage (V_{OUT}) ..... 0.6V to V_{IN}*D_{MAX} or 12V max
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-8 (1.5mmx2mm)	110	55...	°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (5), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN_SD}				2	μA
Supply current (quiescent)	I_Q	V_{FB} = 0.7V		5	9	μA
HS switch on resistance	$HS_{RDS(ON)}$			260	450	mΩ
LS switch on resistance	$LS_{RDS(ON)}$			120	200	mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 22V/0V			1	μA
LS valley current limit	I_{VALLEY}		1.1	1.4	1.7	A
LS sink current limit (6)	I_{LSSINK}	OVP or output discharge		-600		mA
Switching frequency	f_{SW}	V_{OUT} = 3.3V, in CCM	-10%	1250	+10%	kHz
Minimum off time (6)	T_{OFF_MIN}			140		ns
Minimum on time (6)	T_{ON_MIN}			40		ns
Maximum duty cycle	D_{MAX}	V_{FB} = 500mV	96	98		%
Feedback voltage	V_{FBR}	Room temp	594	600	606	mV
	V_{FBF}	Over temp	-1.5%	600	+1.5%	mV
Feedback current	I_{FB}	V_{FB} = 620mV		10	50	nA
Output over-voltage protection rising	V_{OVP_R}		116%	121%	126%	V_{Ref}
Output over-voltage deglitch time (6)	t_{OVP}			8		μs
Output over-voltage protection recovery	V_{OVP_F}		106%	111%	116%	V_{Ref}
V_{IN} under-voltage lockout threshold rising	$INUV_{Vth}$		2.63	2.80	2.97	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			170		mV
Soft-start period	T_{SS}	10% to 90% V_{OUT}	1	1.3	1.6	ms
VCC voltage	V_{CC}	I_{CC} = 2.5mA	3.1	3.3	3.5	V
VCC voltage regulation	V_{CC_RG}	I_{CC} = 0 - 5mA	0.1	0.5	0.9	%
Thermal shutdown (6)	T_{STD}			150		°C
Thermal hysteresis (6)	T_{HYS}			20		°C
EN rising threshold	V_{EN_R}		1.05	1.20	1.35	V
EN hysteresis	V_{EN_F}			150		mV
EN input current	I_{EN}	V_{EN} = 2V			0.1	μA
PG UV rising	$V_{PG_UV_R}$		87%	92%	97%	Vref
PG UV falling	$V_{PG_UV_F}$		82%	87%	92%	Vref
PG OV rising	$V_{PG_OV_R}$		108%	113%	118%	Vref
PG OV falling	$V_{PG_OV_F}$		103%	108%	113%	Vref
PG rise delay	$t_{PG_R_DLY}$			200		μs
PG falling delay	$t_{PG_F_DLY}$			50		μs
PG sink current capability	V_{PG_Sink}	Sink 1mA			0.4	V

NOTES:

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Guaranteed by design and engineering sample characterization.

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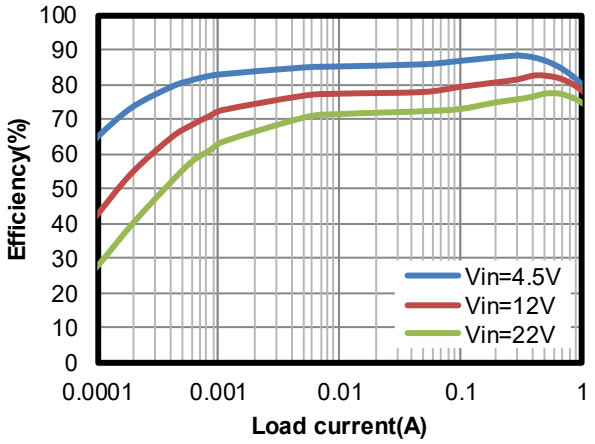
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted

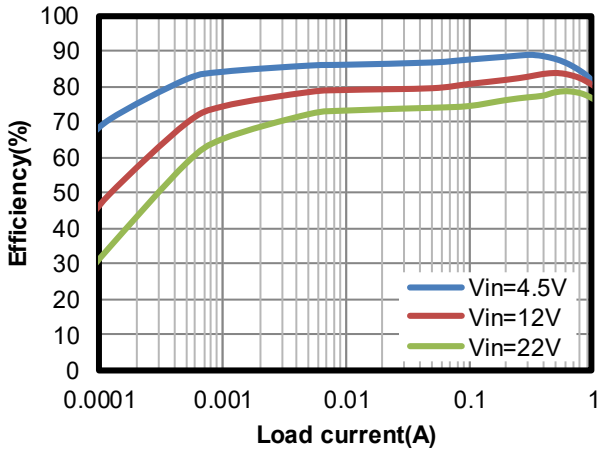
Efficiency vs. Output Current

V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, DCR = 11.4mΩ



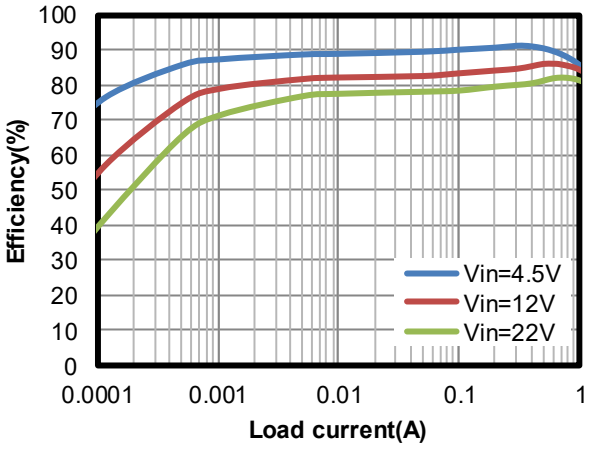
Efficiency vs. Output Current

V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.2µH, DCR = 11.4mΩ



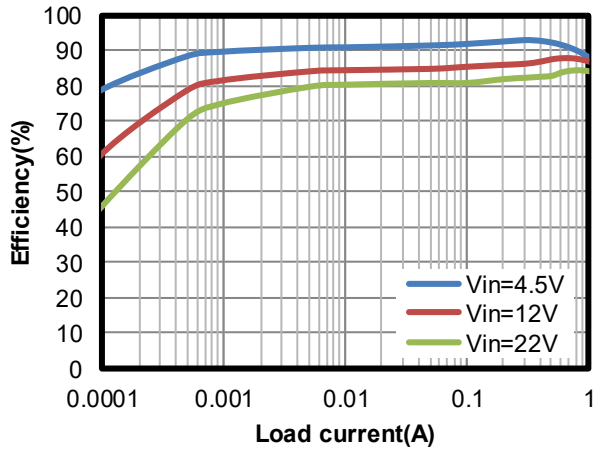
Efficiency vs. Output Current

V_{IN} = 12V, V_{OUT} = 1.8V, L = 3.3µH, DCR = 9mΩ



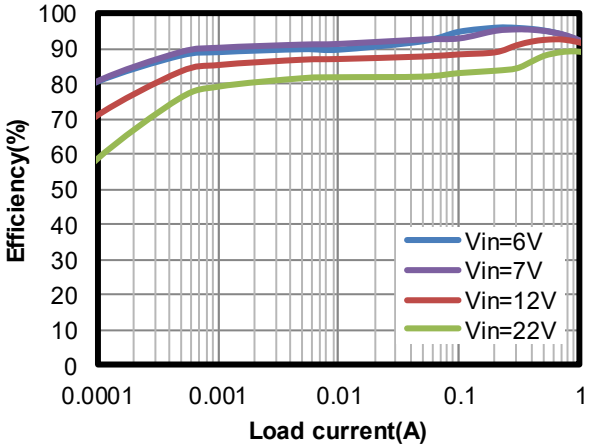
Efficiency vs. Output Current

V_{IN} = 12V, V_{OUT} = 2.5V, L = 3.3µH, DCR = 9mΩ



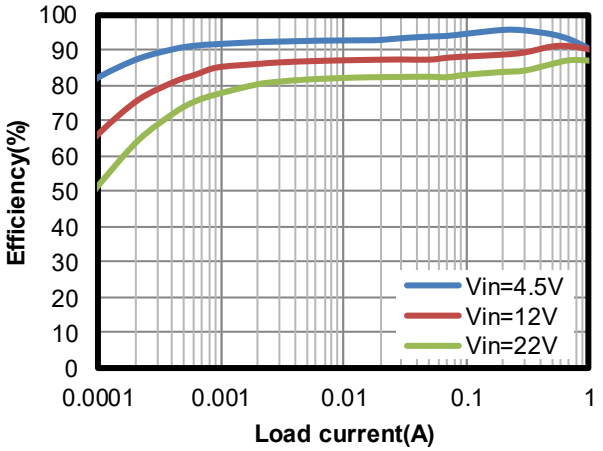
Efficiency vs. Output Current

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, DCR = 24.5mΩ



Efficiency vs. Output Current

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, DCR = 9mΩ



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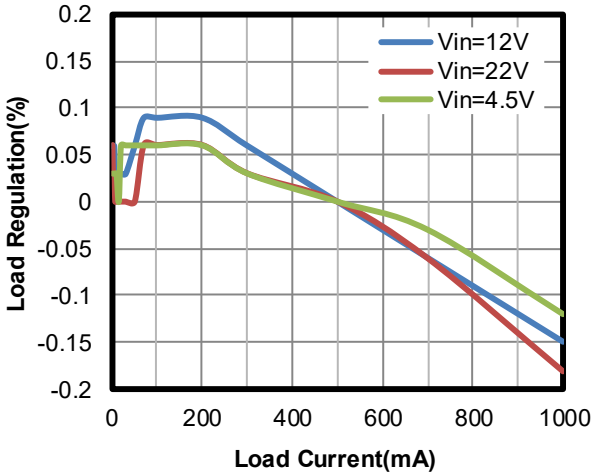
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted

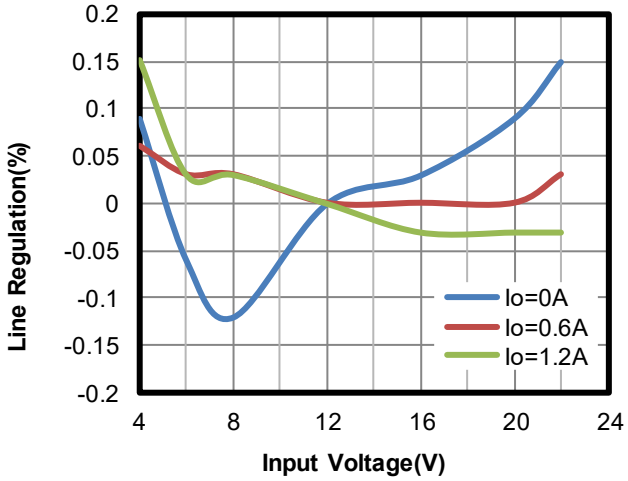
Load Regulation

V_{IN} = 4.5 - 22V



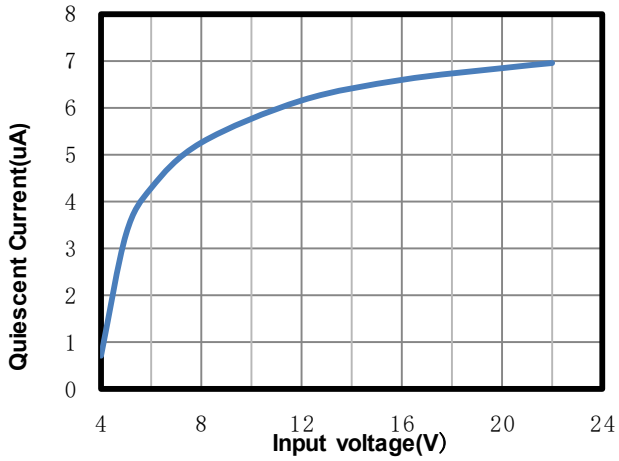
Line Regulation

V_{IN} = 4.5 - 22V



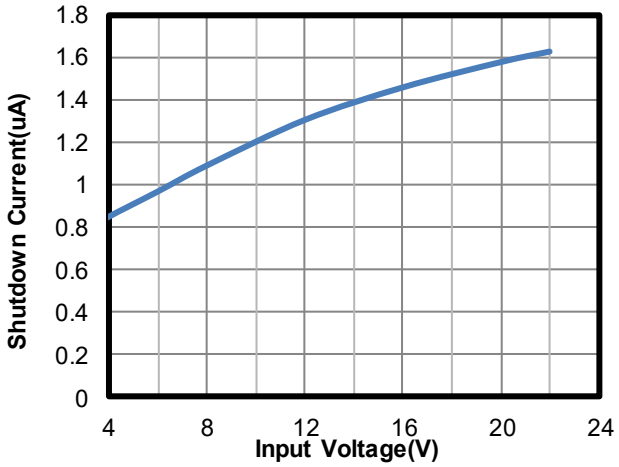
Quiescent Current vs. Input Voltage

V_{EN} = 5V, V_{FB} = 0.64V

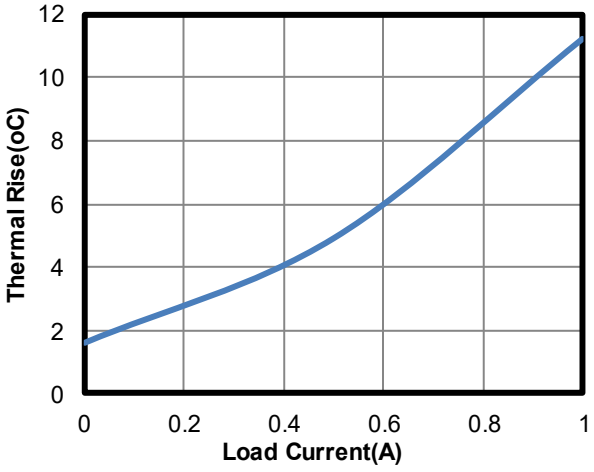


Shutdown Current vs. Input Voltage

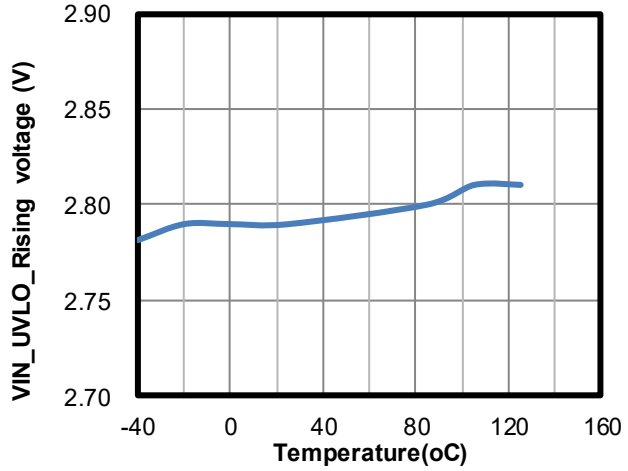
V_{EN} = 0V



Case Temperature Rise vs. Output Current



V_{IN} UVLO vs. Temperature



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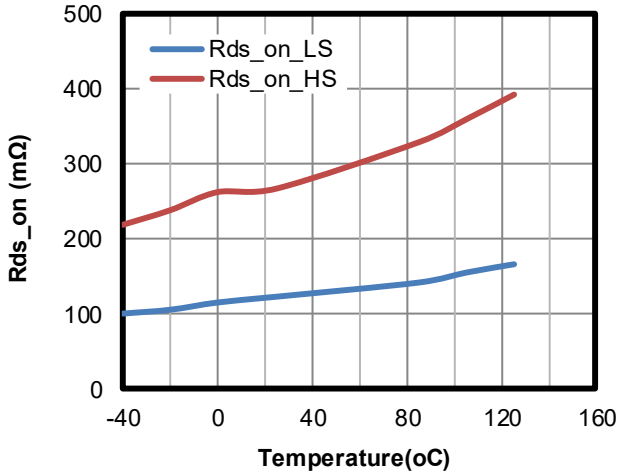
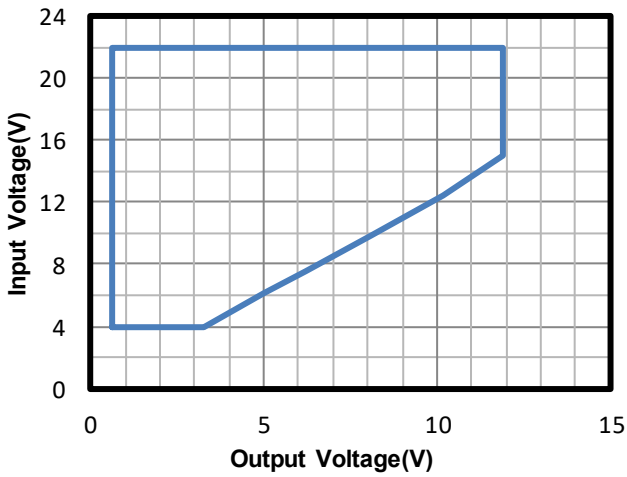
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted

$R_{DS(ON)}$ vs. Temperature



Operation Range of V_{IN} and V_{OUT} for High Light-Load Efficiency
(Area inside blue line indicates recommended values)



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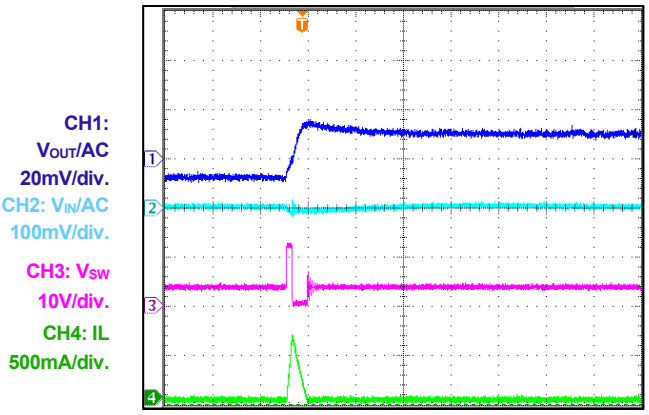
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

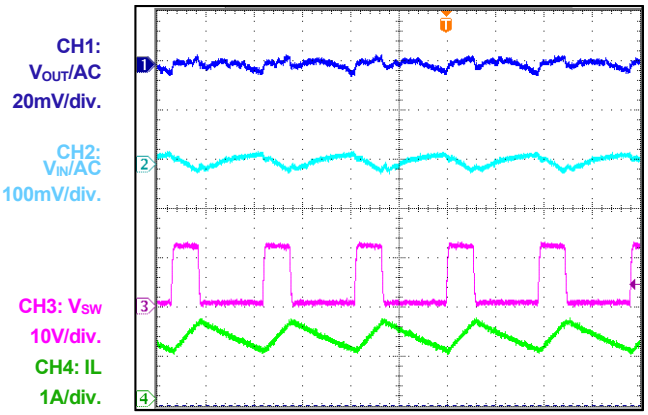
Input/Output Ripple

I_{OUT} = 0A



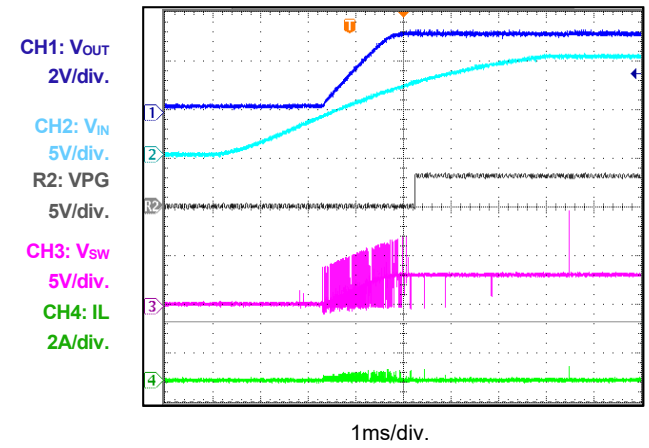
Input/Output Ripple

I_{OUT} = 1A



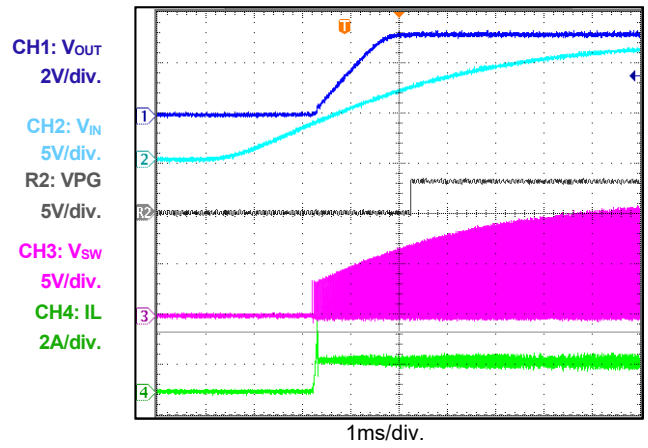
Start-Up through Input Voltage

I_{OUT} = 0A



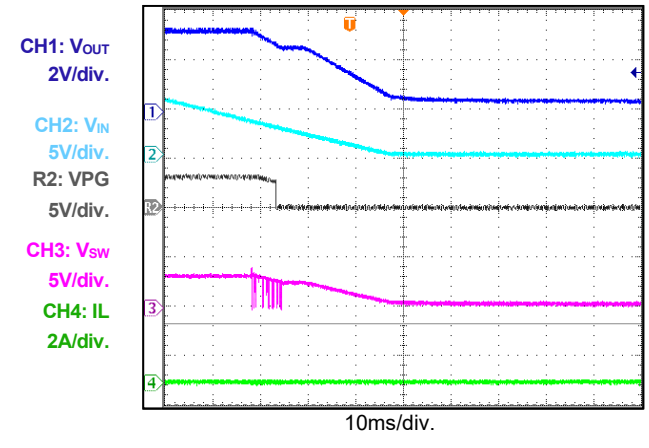
Start-Up through Input Voltage

I_{OUT} = 1A



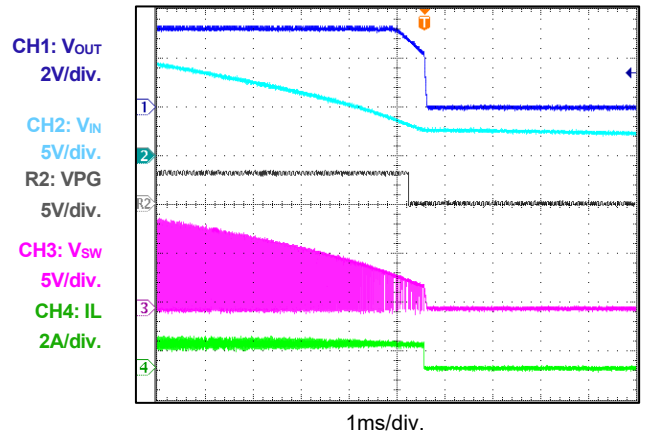
Shutdown through Input Voltage

I_{OUT} = 0A



Shutdown through Input Voltage

I_{OUT} = 1A



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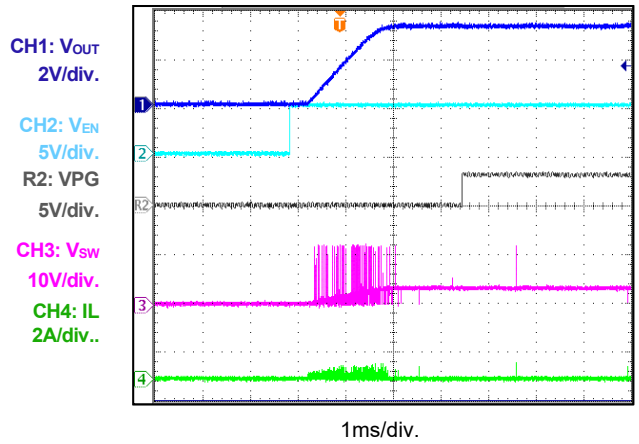
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

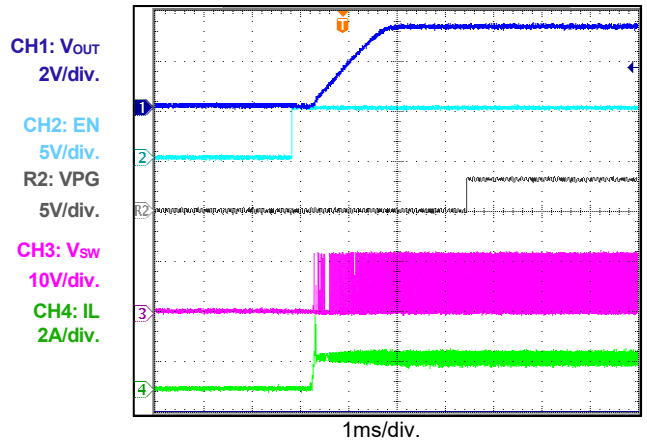
Start-Up through EN

I_{OUT} = 0A



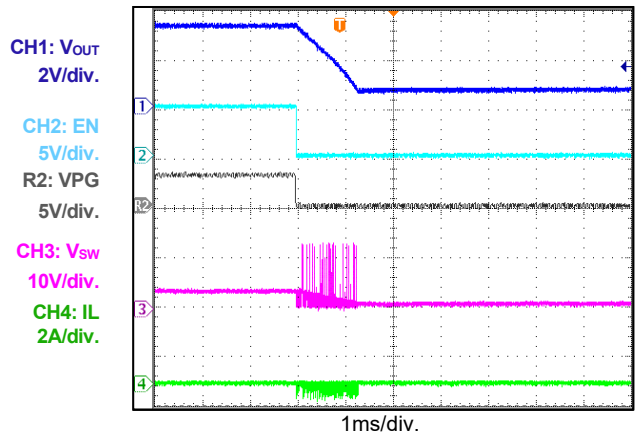
Start-Up through EN

I_{OUT} = 1A



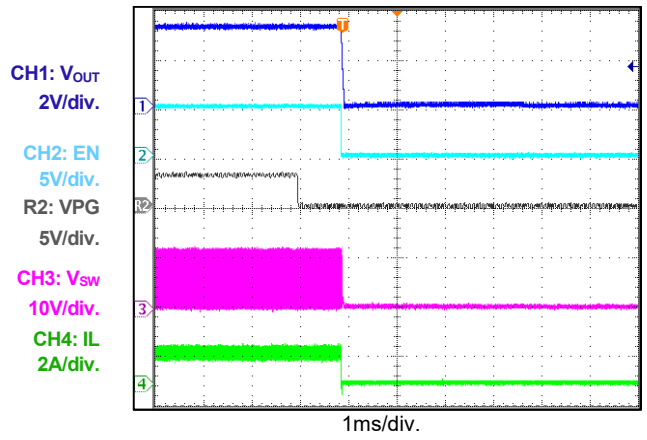
Shutdown through EN

I_{OUT} = 0A

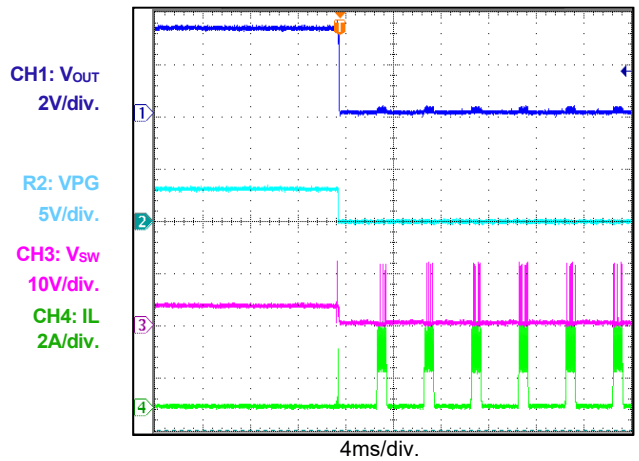


Shutdown through EN

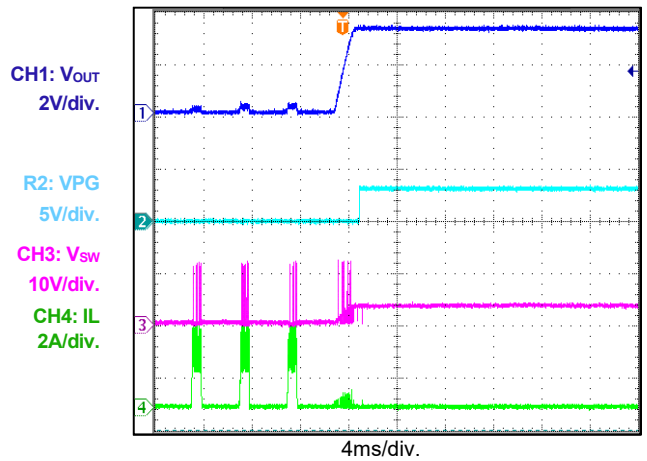
I_{OUT} = 1A



Short-Circuit Protection Entry



Short-Circuit Protection Recovery



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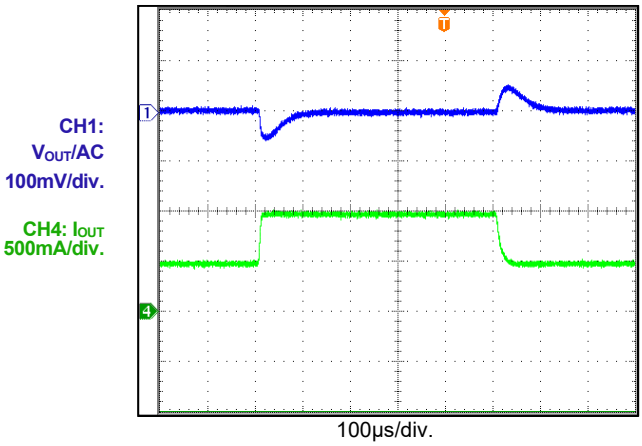
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

Load Transient Response

I_{OUT} = 0.5 - 1A, 2.5A/µs



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BLOCK DIAGRAM

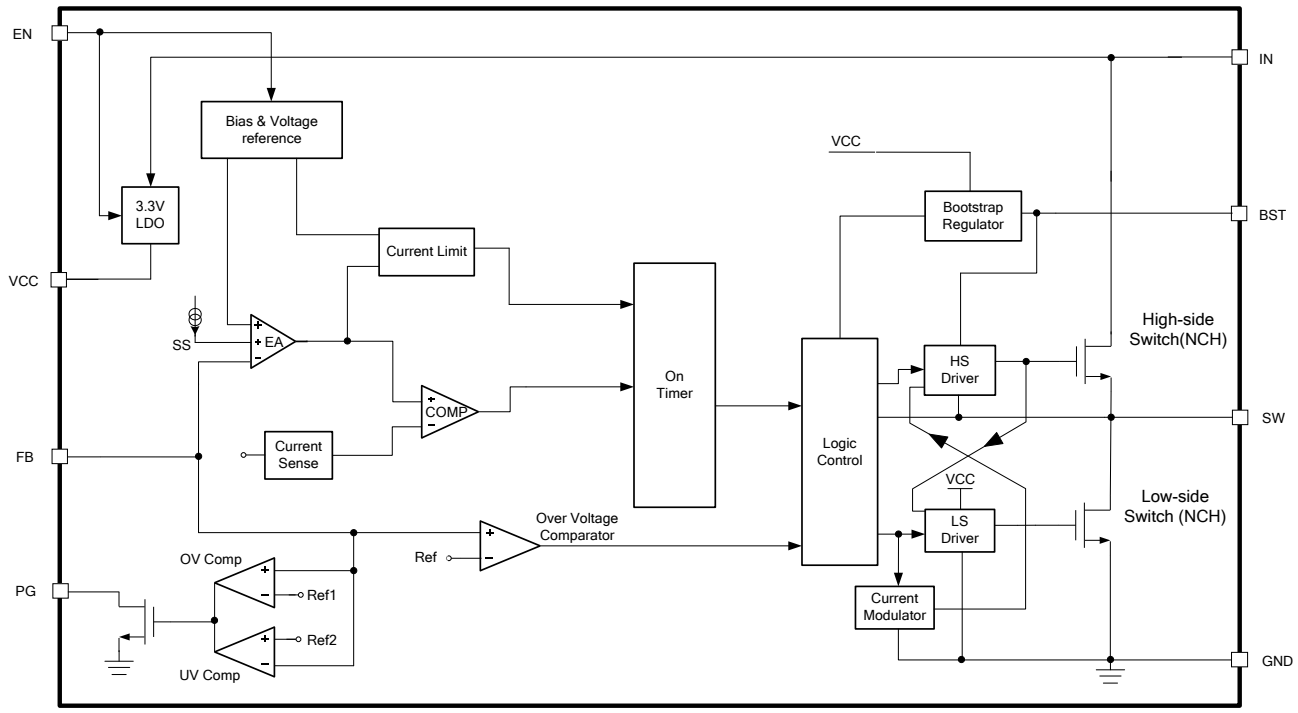

Figure 1: Functional Block Diagram

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OPERATION

The MP2322 is a low quiescent current, fully integrated, synchronous, rectified, step-down switch converter. The MP2322 offers a very compact solution that achieves 1A of output current with excellent efficiency over a wide input supply range.

Pulse-Width Modulation (PWM) Operation

The MP2322 uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. Figure 2 shows the simplified ramp compensation block. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ISENSE ramp voltage (V_{ISENSE}) is lower than the error amplifier output voltage (V_{EAO}), which indicates an insufficient output voltage.

After the on period elapses, the HS-FET enters the off state. By cycling the HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize the conduction loss.

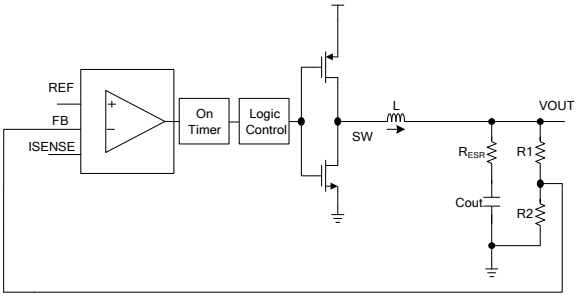

Figure 2: Simplified Control Block

Shoot-through occurs when the HS-FET and LS-FET are both turned on at the same time, causing a dead short between the input and GND. Shoot-through reduces efficiency dramatically. To prevent this, the MP2322 generates a dead time (DT) internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period. The device enters either heavy-load or light-load operation depending on the amplitude of the output current.

Light-Load Operation

When working in light-load condition, the MP2322 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z). The current modulator controls the LS-FET and limits the inductor current to about 0A (see Figure 4). The output capacitors discharge slowly to GND through the LS-FET and feedback resistors (R1, R2). This operation improves device efficiency greatly when the output current is low.

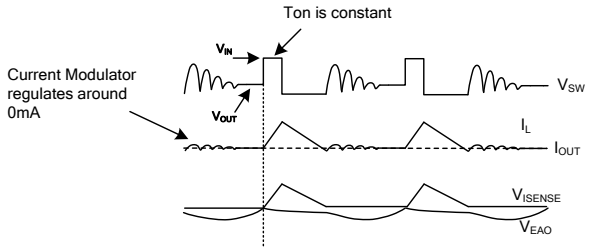

Figure 4: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The HS-FET turn-on frequency is a function of the output current. As the output current increases, the current modulator regulation time period becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (0)$$

The device reverts to pulse-width modulation (PWM) mode once the output current exceeds the critical level. Afterward, the switching frequency remains constant over the output current range.

VCC Regulator

A 3.3V internal regulator powers most of the internal circuitries. Decouple VCC with a minimum 1µF ceramic capacitor as close to VCC as possible. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 3.3V, the output of the regulator is in full regulation. When V_{IN} is lower than 3.3V, the output voltage decreases and follows the input voltage.

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Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own under-voltage lockout (UVLO) protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VCC through M1, C4, L1, and C2 (see Figure 5). The BST capacitor (C4) voltage is charged up quickly by VCC through M1.

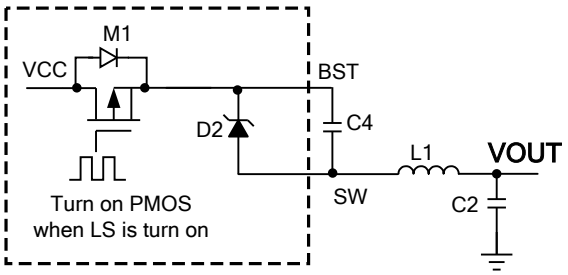

Figure 5: Bootstrap Charging Circuit

Soft Start (SS)

The MP2322 employs a soft start (SS) mechanism to ensure a smooth output during power-up. When the part is enabled and the BST voltage reaches its rising threshold, an internal current source starts to charge up the internal SS capacitor. The SS capacitor voltage takes over the REF voltage (V_{REF}) to the PWM comparator. The output voltage ramps up smoothly with the SS voltage (V_{SS}). Once V_{SS} rises above V_{REF}, it continues ramping up while the PWM comparator only compares V_{REF} and V_{FB}. At this point, the soft start finishes, and the MP2322 enters steady-state operation.

The internal soft-start time is set at fixed 1.3ms (V_{OUT} from 10 - 90%). The output capacitance value should be no larger than 470μF to avoid triggering the current limit during start-up.

Pre-Bias Start-Up

The MP2322 is designed for monotonic start-up into pre-biased V_{OUT} loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the internal soft-start capacitor is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor voltage exceeds the sensed output voltage at FB, the MP2322 begins to switch.

Power Good (PG)

The MP2322 uses a power good (PG) output to indicate whether the output voltage is ready or not. PG is an open-drain output. Connect PG to VCC or another voltage source through a pull-up resistor (e.g.: 100kΩ). When the input voltage is applied, PG is pulled down to GND before the internal V_{SS} becomes greater than 1V. After V_{SS} > 1V and V_{FB} is above 92% of V_{REF}, PG is pulled high after a 200μs delay time. During normal operation, PG is pulled low when V_{FB} drops below 87% of V_{REF} after a 50μs delay.

If EN becomes low, over-temperature protection (OTP) occurs or input voltage UVLO occurs, PG is pulled low immediately. In an over-current (OC) condition, PG is pulled low when V_{FB} drops below 87% of V_{REF} after a 50μs delay.

PG also indicates the output over-voltage condition with a 113% V_{REF} rising threshold, 108% V_{REF} falling threshold, and 200μs/50μs deglitch timer. Note that this threshold is lower than the over-voltage protection (OVP) discharge threshold.

Low Dropout Operation

To reduce the V_{IN}-to-V_{OUT} dropout voltage, the MP2322 is designed to extend the on time when the minimum off time is triggered. The HS-FET on time is extended, and the frequency drops. The typical minimum frequency is 240kHz. When the frequency drops to 240kHz, the duty cycle reaches the maximum duty cycle (D_{MAX}) when the on time is at its maximum value. If the input voltage continues to drop, the MP2322 works at 240kHz, and the output voltage drops.

The typical D_{MAX} is calculated with Equation (2):

$$D_{MAX} = 1 - T_{off_min} \times f_{sw_min} \quad (2)$$

Where T_{off_min} = 140ns, and f_{sw_min} = 240kHz.

Output Over-Voltage Protection (OVP)

The MP2322 monitors the output voltage and enters OVP discharge mode once the output voltage is higher than 120% of the regulation voltage for more than 8μs. In OVP discharge mode, the LS-FET turns on until the low-side current drops to the negative current limit. This discharges the output and keeps the output voltage within the normal range. If the output

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voltage over-voltage (OV) condition still remains, the LS-FET turns on again after a fixed delay to repeat the discharge behavior.

The MP2322 exits this discharge mode when V_{FB} is decreased below 110% of V_{REF}.

If the MP2322 input voltage during OVP discharge mode exceeds 24V of the input OVP, the MP2322 shuts down until the input voltage drops below 22V. Then, the MP2322 restarts. This input OVP function is only active during the output OV condition.

Output Discharge

The MP2322 involves a discharge function that provides an active discharge path for the external output capacitor. The function is active when the MP2322 is in EN disable mode. When EN is disabled, the HS-FET turns off, and the LS-FET turns on to discharge V_{OUT}. When the low-side current reaches the negative current limit, the LS-FET turns off. After a fixed delay time, the LS-FET turns on again. This behavior repeats until FB drops low.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP2322 has a valley current-limit control. The inductor current is monitored during the LS-FET turn-on state. When the sensed inductor current is higher than the valley current-limit threshold, the device enters over-current protection (OCP) mode, the HS-FET is not allowed to turn on until the valley current limit is removed. Meanwhile, the output voltage drops until it is below the under-voltage (UV) threshold (typically 60% below the reference).

Once UV and OC are both triggered, the MP2322 enters hiccup mode to restart the part periodically. The hiccup duty cycle is very small to reduce power dissipation during short-circuit conditions. During OCP, the device attempts to recover from the over-current fault with hiccup mode. This means that the chip disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the over-current condition still remains when the soft start elapses, the device repeats this operation. OCP is a non-latch protection.

Enable (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN cannot be floated. EN can operate with a 22V input voltage, which allows for EN to be connected to V_{IN} directly for automatic start-up.

Under-Voltage Lockout (UVLO) Protection

The MP2322 has a UVLO protection. When the input voltage is higher than the UVLO rising threshold voltage, the MP2322 powers up. The MP2322 shuts down when the input voltage is lower than the UVLO falling threshold voltage.

Thermal Shutdown

The MP2322 employs thermal shutdown by monitoring the junction temperature of the IC internally. If the junction temperature exceeds the 150°C threshold, the converter shuts off. This is a non-latch protection. There is a hysteresis of about 20°C. Once the junction temperature drops to about 130°C, a soft start is initiated.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably since a small R2 leads to considerable quiescent current loss but a large R2 makes FB noise-sensitive. R2 is recommended to be between 100 - 500kΩ. Typically, a 1 - 5μA current through R2 provides a good balance between system stability and no-load loss. Then R1 can be determined with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

A feedforward capacitor is required in the layout. C5 is parallel with R1 for an additional zero-pole pair. The feedback circuit is shown in Figure 6.

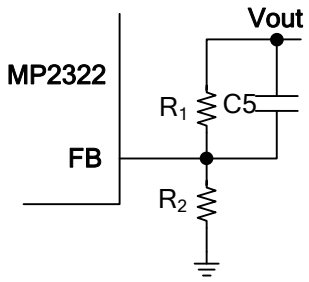

Figure 6: Feedback Network

Table 1 lists recommended resistor and capacitor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C5 (pF)
1.0	147	220	2.2	22
1.2	220	220	2.2	22
1.8	440	220	3.3	22
2.5	697	220	3.3	22
3.3	976	220	3.3	22
5	1613	220	4.7	22

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage but also has a larger physical footprint, higher series resistance, and lower saturation current. For low output current buck applications, a proper discontinuous conduction mode (DCM) threshold should be considered. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be twice the DCM current threshold (10 ~ 25% of the maximum output current). The inductor current should be in the range of 20 ~ 50% of the maximum output current. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance and should be placed as close to V_{IN} as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

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The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (9)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The output voltage ripple caused by the ESR is very small. In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency.

A larger output capacitor can achieve a better load transient response, but the output ripple and maximum output capacitor limitation must be considered in the design application. If the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft-start time and will fail to regulate.

The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (11):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (11)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{ss} is the soft-start time.

PCB Layout Guidelines [7]

Efficient layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 7 and follow the guidelines below.

1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Add more vias on the GND plane.
3. Place the input capacitor as close to IN and GND as possible.
4. Place the feedback resistors (R1 and R2) close to IC.
5. Connect a VCC capacitor close to VCC with a short, direct GND trace.

NOTE:

7) The recommended layout is based on the Typical Application Circuit shown in Figure 8.

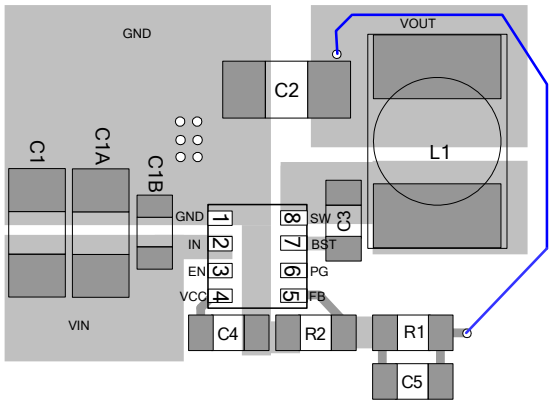

Figure 7: Recommended Layout

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Design Example

Table 2 shows a design example when ceramic capacitors are applied.

Table 2: Design Example

V_{OUT} (V)	3.3
C_{OUT} (µF)	22
L (µH)	3.3
R1 (kΩ)	976
R2 (kΩ)	220

The detailed application schematic is shown in Figure 8. The typical performance and waveforms are shown in the Typical Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUIT

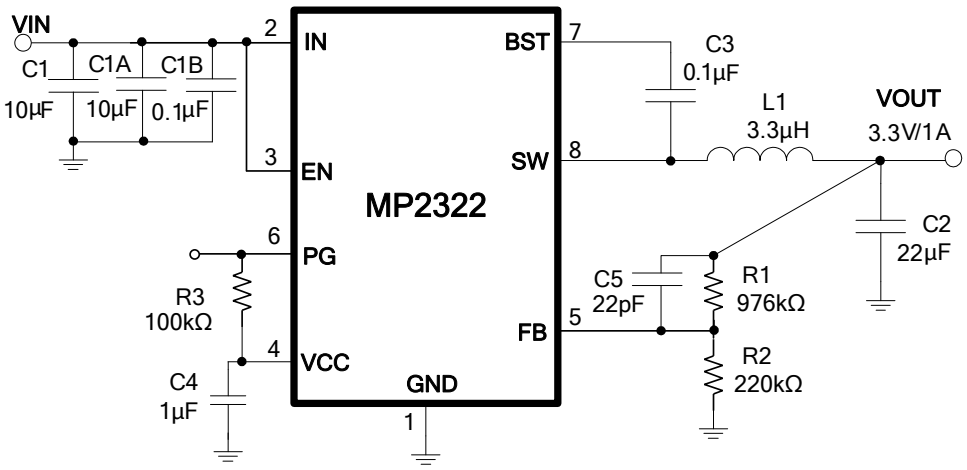

Figure 8: V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A

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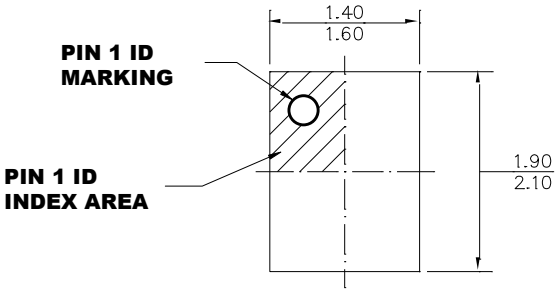
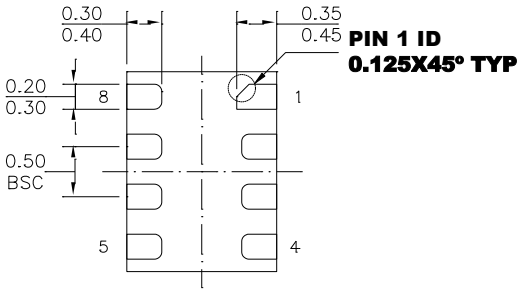
PACKAGE INFORMATION

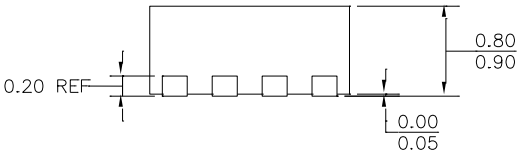
QFN-8 (1.5mmx2mm)



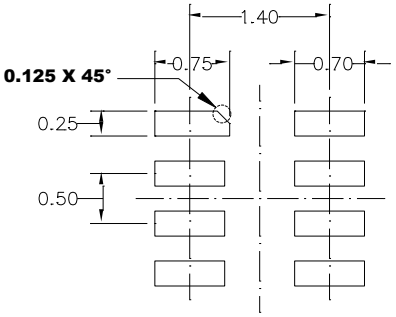
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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