DESCRIPTION

The MP2319 is a fully-integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP2319 offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input range. The MP2319 has synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time control operation provides a very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), over-voltage protection (OVP), and thermal shutdown.

The MP2319 requires a minimal number of readily available, standard, external components and is available in a space-saving, 8-pin, TSOT23 package.

FEATURES

- Wide 4.5V to 18V Operating Input Range
- 3A Output Current
- 105mΩ/57mΩ Low \( R_{DS(ON)} \) Internal Power MOSFETs
- Output Adjustable from 0.8V
- EN Shutdown Output Discharge
- Internal Soft Start
- High-Efficiency Synchronous Mode Operation
- Fixed 650kHz Switching Frequency
- EN and Power Good for Power Sequencing
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Auto-Retry Over-Voltage Protection (OVP)
- Available in a TSOT23-8 Package

APPLICATIONS

- Security Cameras
- Portable Devices, xDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purposes

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TYPICAL APPLICATION
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP2319GJ</td>
<td>TSOT23-8</td>
<td>See Below</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP2319GJ–Z)

TOP MARKING

| APVY |

APV: Product code of MP2319GJ
Y: Year code

PACKAGE REFERENCE

TOP VIEW

PG 1 8 FB
IN 2 7 VCC
SW 3 6 EN
GND 4 5 BST

TSOT23-8
ABSOLUTE MAXIMUM RATINGS (1)
V_{IN} ............................................. -0.3V to +22V
V_{SW} .... -0.6V (-5V < 10ns) to +22V (23V < 10ns)
V_{BST} ........................................... V_{SW} + 5.5V
V_{EN} ................................................................ V_{IN}
All other pins ......................... -0.3V to +5.5V
Continuous power dissipation (T_A = +25°C) (2)
................................................................. 1.25W
Junction temperature ................... 150°C
Lead temperature ......................... 260°C
Storage temperature ................. -65°C to 150°C

Recommended Operating Conditions (3)
Supply voltage (V_{IN}) ................. 4.5V to 18V
Output voltage (V_{OUT}) .............. 0.8V to 12V
Operating junction temp ............ -40°C to +125°C

Thermal Resistance (4) $\theta_{JA}$ $\theta_{JC}$
TSOT23-8 .................................. 100......55 ....°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the
   maximum junction temperature $T_J$ (MAX), the junction-to-
   ambient thermal resistance $\theta_{JA}$, and the ambient temperature
   $T_A$. The maximum allowable continuous power dissipation at
   any ambient temperature is calculated by $P_D$ (MAX) = $(T_J$
   (MAX) - $T_A)/\theta_{JA}$. Exceeding the maximum allowable power
   dissipation produces an excessive die temperature, causing
   the regulator to go into thermal shutdown. Internal thermal
   shutdown circuitry protects the device from permanent
   damage.
3) The device is not guaranteed to function outside of its
   operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
ELECTRICAL CHARACTERISTICS

\( V_{\text{IN}} = 12\,V, \, T_J = -40^\circ\text{C} \) to \(+125^\circ\text{C}\)\(^{(5)}\), unless otherwise noted. Typical value is based on the average value when \( T_J = 25^\circ\text{C}\).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current</td>
<td>( I_{\text{IN}} )</td>
<td>( V_{\text{EN}} = 0,\text{V} )</td>
<td>1.2</td>
<td>5</td>
<td>( \mu\text{A} )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{\text{q}} )</td>
<td>( V_{\text{EN}} = 2,\text{V}, , V_{\text{FB}} = 0.9,\text{V} )</td>
<td>270</td>
<td>350</td>
<td>( \mu\text{A} )</td>
<td></td>
</tr>
<tr>
<td>MOSFET</td>
<td>( \text{HS switch on resistance} )</td>
<td>( \text{HS}_{\text{RDS(on)}} )</td>
<td>( V_{\text{BST-SW}} = 5,\text{V} )</td>
<td>105</td>
<td>( \text{m}\Omega )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( \text{LS switch on resistance} )</td>
<td>( \text{LS}_{\text{RDS(on)}} )</td>
<td>( V_{\text{CC}} = 5,\text{V} )</td>
<td>57</td>
<td>( \text{m}\Omega )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( \text{Switch leakage} )</td>
<td>( \text{SW}_{\text{LKG}} )</td>
<td>( V_{\text{EN}} = 0,\text{V}, , V_{\text{SW}} = 12,\text{V/0V} )</td>
<td>1</td>
<td>( \mu\text{A} )</td>
<td></td>
</tr>
<tr>
<td>Current Limit and ZCD</td>
<td>( I_{\text{LIMIT-VY}} )</td>
<td>Duty = 40%</td>
<td>2.8</td>
<td>3.5</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>( I_{\text{ZCD}} )</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td>( \text{mA} )</td>
</tr>
<tr>
<td>Switching Frequency and Minimum On/Off Timer</td>
<td>( F_s )</td>
<td></td>
<td>510</td>
<td>650</td>
<td>790</td>
<td>( \text{kHz} )</td>
</tr>
<tr>
<td></td>
<td>( T_{\text{On-MIN}} ) ((^{(b)}))</td>
<td></td>
<td></td>
<td>55</td>
<td></td>
<td>( \text{ns} )</td>
</tr>
<tr>
<td></td>
<td>( T_{\text{Off-MIN}} ) ((^{(b)}))</td>
<td></td>
<td></td>
<td>90</td>
<td></td>
<td>( \text{ns} )</td>
</tr>
<tr>
<td>Reference and Soft Start</td>
<td>( V_{\text{FB}} )</td>
<td>( T_J = 25^\circ\text{C} )</td>
<td>792</td>
<td>800</td>
<td>808</td>
<td>( \text{mV} )</td>
</tr>
<tr>
<td></td>
<td>( V_{\text{FB}} )</td>
<td>( T_J = -40^\circ\text{C} ) to (+125^\circ\text{C})(^{(5)})</td>
<td>788</td>
<td>800</td>
<td>812</td>
<td>( \text{mV} )</td>
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<tr>
<td></td>
<td>( I_{\text{FB}} )</td>
<td>( V_{\text{FB}} = 820,\text{mV} )</td>
<td>10</td>
<td>50</td>
<td></td>
<td>( \text{nA} )</td>
</tr>
<tr>
<td></td>
<td>( t_{\text{SS}} )</td>
<td>( V_{\text{OUT}} = 10% ) to (90%)</td>
<td>0.8</td>
<td></td>
<td></td>
<td>( \text{ms} )</td>
</tr>
<tr>
<td>Enable (EN) and UVLO</td>
<td>( V_{\text{EN-RISING}} )</td>
<td></td>
<td>1.22</td>
<td>1.285</td>
<td>1.35</td>
<td>( \text{V} )</td>
</tr>
<tr>
<td></td>
<td>( V_{\text{EN-HYS}} )</td>
<td></td>
<td></td>
<td>140</td>
<td></td>
<td>( \text{mV} )</td>
</tr>
<tr>
<td></td>
<td>( R_{\text{EN-PD}} )</td>
<td></td>
<td></td>
<td>1.1</td>
<td></td>
<td>( \text{M}\Omega )</td>
</tr>
<tr>
<td></td>
<td>( V_{\text{IN}} ) under-voltage lockout threshold rising</td>
<td>( \text{INU}_{\text{Vih}} )</td>
<td></td>
<td>3.4</td>
<td>3.85</td>
<td>4.3</td>
</tr>
<tr>
<td></td>
<td>( V_{\text{IN}} ) under-voltage lockout threshold hysteresis</td>
<td>( \text{INU}_{\text{HY}} )</td>
<td></td>
<td>670</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>( V_{\text{CC}} )</td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>( \text{V} )</td>
</tr>
<tr>
<td></td>
<td>( I_{\text{CC}} )</td>
<td>( I_{\text{CC}} = 5,\text{mA} )</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>OVP</td>
<td>( V_{\text{OVP-RISE}} )</td>
<td></td>
<td>1.18</td>
<td>1.22</td>
<td>1.26</td>
<td>( V_{\text{REF}} )</td>
</tr>
<tr>
<td></td>
<td>( V_{\text{OVP-FALL}} )</td>
<td></td>
<td>1.025</td>
<td>1.065</td>
<td>1.105</td>
<td>( V_{\text{REF}} )</td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN} = 12V$, $T_J = -40°C$ to $+125°C^{(5)}$, unless otherwise noted. Typical value is based on the average value when $T_J = 25°C$.

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<thead>
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<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Good UV rising threshold</td>
<td>$PG_{vth_Hi}$</td>
<td></td>
<td>0.875</td>
<td>0.915</td>
<td>0.955</td>
<td>$V_{FB}$</td>
</tr>
<tr>
<td>Power Good UV falling threshold</td>
<td>$PG_{vth_Lo}$</td>
<td></td>
<td>0.77</td>
<td>0.81</td>
<td>0.85</td>
<td>$V_{FB}$</td>
</tr>
<tr>
<td>Power Good OV rising threshold</td>
<td>$PG_{vth_Hi_OV}$</td>
<td></td>
<td>1.025</td>
<td>1.065</td>
<td>1.105</td>
<td>$V_{FB}$</td>
</tr>
<tr>
<td>Power Good OV falling threshold</td>
<td>$PG_{vth_Lo_OV}$</td>
<td></td>
<td>1.18</td>
<td>1.22</td>
<td>1.26</td>
<td>$V_{FB}$</td>
</tr>
<tr>
<td>Power good low to high delay</td>
<td>$PG_{Td}$</td>
<td></td>
<td>56</td>
<td></td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>Power good high to low delay</td>
<td>$PG_{Td}$</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>Power good sink current capability</td>
<td>$V_{PG}$</td>
<td>Sink 4mA</td>
<td></td>
<td></td>
<td></td>
<td>$V$</td>
</tr>
<tr>
<td>Power good leakage current</td>
<td>$I_{PG_LEAK}$</td>
<td>$V_{PG} = 5V$</td>
<td></td>
<td></td>
<td></td>
<td>$2.5$</td>
</tr>
</tbody>
</table>

**Thermal Protection**

| Thermal shutdown | $T_{SD}$ | | 150 | | | $°C$ |
| Thermal hysteresis | $T_{SD\_HYS}$ | | 20 | | | $°C$ |

**NOTES:**

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Guaranteed by design and characterization test.
TYPICAL PERFORMANCE CHARACTERISTICS

$$V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2\mu H, T_A = 25^\circ C,$$ unless otherwise noted.

- **Enable Supply Current vs. Input Voltage**
- **Disabled Supply Current vs. Input Voltage**
- **VIN UVLO Rising Threshold vs. Temperature**
- **EN Rising Threshold vs. Temperature**
- **Inductor Valley Current Limit vs. Duty Cycle**
- **Reference Voltage vs. Temperature**
- **Inductor Valley Current Limit vs. Temperature**
- **Efficiency vs. Output Current**
  - $V_{OUT} = 3.3V$
  - $V_{OUT} = 5V$

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12\text{V},\ V_{OUT} = 3.3\text{V},\ L = 2.2\mu\text{H},\ T_A = 25^\circ\text{C},$ unless otherwise noted.

- **Efficiency vs. Output Current**
  - $V_{IN} = 6\text{V}$
  - $V_{IN} = 12\text{V}$
  - $V_{IN} = 18\text{V}$

- **Efficiency vs. Output Current**
  - $V_{OUT} = 3.2\text{V}$
  - $V_{OUT} = 1.8\text{V}$
  - $V_{OUT} = 1.5\text{V}$

- **Case Temperature Rise vs. Output Current**
  - $V_{OUT} = 5\text{V}$
  - $V_{OUT} = 3.3\text{V}$

- **Load Regulation**
  - $V_{OUT} = 3.3\text{V}$

- **Line Regulation**
  - $V_{IN} = 6\text{V}$ to 18V

- **Bode Plot**
  - $I_{OUT} = 3\text{A}$

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

- **Start-Up through Input Voltage ($I_{OUT}=0A$)**
  - $V_{OUT}$
  - $V_{PG}$
  - $V_{SW}$
  - $I_L$

- **Shutdown through Input Voltage ($I_{OUT}=0A$)**
  - $V_{OUT}$
  - $V_{PG}$
  - $V_{SW}$
  - $I_L$

- **Start-Up through Enable ($I_{OUT}=0A$)**
  - $V_{OUT}$
  - $V_{PG}$
  - $V_{EN}$
  - $V_{SW}$
  - $I_L$

- **Shutdown through Enable ($I_{OUT}=0A$)**
  - $V_{OUT}$
  - $V_{PG}$
  - $V_{EN}$
  - $V_{SW}$
  - $I_L$

- **Input/Output Ripple ($I_{OUT}=0A$)**
  - $V_{OUT/AC}$
  - $V_{PG/AC}$
  - $V_{SW}$
  - $I_L$
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

\( V_{\text{IN}} = 12\,\text{V}, \quad V_{\text{OUT}} = 3.3\,\text{V}, \quad L = 2.2\,\mu\text{H}, \quad T_A = 25^\circ\text{C}, \) unless otherwise noted.

**Input/Output Ripple**

\( I_{\text{OUT}} = 3\,\text{A} \)

- \( V_{\text{OUT}} \) (AC, 10mV/div.)
- \( V_{\text{IN}} \) (AC, 200mV/div.)
- \( V_{\text{SW}} \) (10V/div.)
- \( I_L \) (5A/div.)

1µs/div.

**SCP Entry**

\( I_{\text{OUT}} = 0\,\text{A} \)

- \( V_{\text{OUT}} \) (2V/div.)
- \( V_{\text{PG}} \) (5V/div.)
- \( V_{\text{SW}} \) (10V/div.)
- \( I_L \) (5A/div.)

2ms/div.

**SCP Recovery**

\( I_{\text{OUT}} = 0\,\text{A} \)

- \( V_{\text{OUT}} \) (2V/div.)
- \( V_{\text{PG}} \) (5V/div.)
- \( V_{\text{SW}} \) (10V/div.)
- \( I_L \) (5A/div.)

2ms/div.

**Load Transient Response**

\( I_{\text{OUT}} = 1.5\,\text{A} \) to \( 3\,\text{A} \)

- \( V_{\text{OUT}} \) (AC, 20mV/div.)
- \( I_L \) (1A/div.)

100µs/div.
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Package Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PG</td>
<td><strong>Power good output.</strong> The output of PG is an open drain that goes high if the output voltage is within a nominal output window.</td>
</tr>
<tr>
<td>2</td>
<td>IN</td>
<td><strong>Supply voltage.</strong> The MP2319 operates from a 4.5V to 18V input rail. C1 is needed to decouple the input rail. Connect IN using wide PCB traces.</td>
</tr>
<tr>
<td>3</td>
<td>SW</td>
<td><strong>Switch output.</strong> Connect SW using wide PCB traces.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td><strong>System ground.</strong> GND is the reference ground of the regulated output voltage. GND requires careful consideration during PCB layout. Connect GND with copper traces and vias.</td>
</tr>
<tr>
<td>5</td>
<td>BST</td>
<td><strong>Bootstrap.</strong> Connect a capacitor between SW and BS to form a floating supply across the high-side switch driver. Place a 10Ω resistor between the SW and BST cap to reduce SW voltage spikes.</td>
</tr>
<tr>
<td>6</td>
<td>EN</td>
<td><strong>Enable.</strong> Set EN = 1 to enable the MP2319. When floating, EN is pulled down to GND by an internal 1.1MΩ resistor, and the MP2319 is disabled.</td>
</tr>
<tr>
<td>7</td>
<td>VCC</td>
<td><strong>Internal bias supply.</strong> Decouple VCC with a 0.1µF to 0.22µF capacitor. The capacitor should not exceed 0.22µF. The VCC capacitor should be placed close to VCC and GND.</td>
</tr>
<tr>
<td>8</td>
<td>FB</td>
<td><strong>Feedback.</strong> FB sets the output voltage when connected to the tap of an external resistor divider that is connected between the output and GND.</td>
</tr>
</tbody>
</table>
Figure 1: Functional Block Diagram
OPERATION
The MP2319 is fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide a fast transient response and ease loop stabilization. Figure 2 shows the simplified ramp compensation block in the MP2319.

At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off or enters an off state. It is turned on again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called a shoot-through. To prevent a shoot-through, a dead time (DT) is generated internally between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation
Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 3). When V_{FB} is below V_{EAO}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period.

Light-Load Operation
In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

Figure 2: Simplified Ramp Compensation Block

Figure 3: Heavy-Load Operation

Figure 4: Light-Load Operation
Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does in heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero, and can be determined with Equation (1):

\[ I_{\text{out}} = \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{2 \times L \times F_{\text{SW}} \times V_{\text{IN}}} \]  

The device reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

**Enable (EN)**

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. When floating, EN is pulled down to GND by an internal 1.1MΩ resistor. EN can be connected directly to VᵢᵣᵢBegan. EN supports an 18V input range.

**Under-Voltage Lockout (UVLO)**

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2319 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.85V, while its falling threshold is 3.18V consistently.

**Internal Soft Start (SS)**

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 0.8ms internally.

**Power Good (PG) Indicator**

The MP2319 uses a power good (PG) output to indicate whether the output voltage of the module is ready or not. PG is an open-drain output. Connect PG to VCC or another voltage source through a pull-up resistor (e.g., 100kΩ). When input voltage is applied, PG is pulled down to GND before the internal V瘐 > 1V. After V瘐 > 1V, when Vᵦᵡ is above 91.5% of Vᵦᵨᵨ, PG is pulled high after a 56µs delay. During normal operation, PG is pulled low when Vᵦᵡ drops below 81% of Vᵦᵨᵨ after a 40μs delay.

When UVLO or OTP occurs, PG is pulled low immediately. When over-current (OC) occurs, PG is pulled low when Vᵦᵡ drops below 81% of Vᵦᵨᵨ after a 40µs delay. PG is pulled low to indicate output over-voltage when Vᵦᵡ rises above 122% of Vᵦᵨᵨ after a 40µs delay. If Vᵦᵡ falls below 105% after over-voltage protection (OVP), PG is pulled high after a 56µs delay.

**Over-Current Protection (OCP) and Short-Circuit Protection (SCP)**

The MP2319 has a valley limit control. During the LS-FET on state, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the inductor current is monitored. When the MP2319 enters over-current protection (OCP) mode. The HS-FET waits until the inductor current falls below the valley current limit before turning on again. Meanwhile, the output voltage drops until Vᵦᵡ is below the under-voltage (UV) threshold, typically 50% below the reference. Once UV is triggered, the MP2319 enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. The MP2319 disables the output power stage, discharges the soft-start cap, and then tries to soft-start automatically. If the over-current condition still remains after the soft-start ends, the MP2319 repeats this operation cycle until the over-current condition is removed, and then the output rises back to regulation levels. OCP is a non-latch protection.
Over-Voltage Protection (OVP)
The MP2319 monitors the resistor-divided feedback voltage to detect over-voltage (OV). When the feedback voltage rises higher than 122% of the target voltage, the controller enters a dynamic regulation period. During this period, the LS-FET is on until the LS current drops to -2.5A. This discharges the output to keep it within the normal range. If the OV still remains, the LS-FET turns on again after a 400ns delay. The MP2319 exits this regulation period when the feedback voltage is decreased below 106.5% of the reference voltage.

Under-Voltage Lockout (UVLO)
The MP2319 has under-voltage lockout protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MP2319 powers up. The MP2319 shuts off when the input voltage is lower than the UVLO falling threshold voltage. UVLO is a non-latch protection.

Pre-Bias Start-Up
The MP2319 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start capacitor voltage exceeds the sensed output voltage at FB, the part begins working normally.

Output Discharge
The MP2319 has a discharge function that provides an active discharge path for the external output capacitor. The function is active when the part is in the EN off state. When EN is off, the HS-FET turns off, and the LS-FET turns on to discharge VOUT. When the LS-FET current reaches -1A, the LS-FET turns off. After a 400ns delay, the LS-FET turns on again. This behavior repeats until FB low occurs.

Thermal Shutdown
Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging
An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. VIN regulates the bootstrap capacitor voltage through D1, M1, R4, C4, L1, and C2 internally (see Figure 5). If VIN - VSW exceeds 5V, U2 regulates M1 to maintain a 5V BST voltage across C4.

Figure 5: Internal Bootstrap Charger Start-Up and Shutdown Circuit
If both VIN and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path initially to avoid any fault triggering. The COMP voltage (VCOMP) and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.
APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the Typical Application on page 1). Refer to Table 1 to choose R1. R2 can then be calculated with Equation (2):

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{0.8V} - 1}$$  (2)

The feedback circuit is shown in Figure 6.

![Figure 6: Feedback Network](image)

Table 1 lists the recommended resistor values for common output voltages.

<table>
<thead>
<tr>
<th>V_{OUT} (V)</th>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>R3 (kΩ)</th>
<th>C6 (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>30</td>
<td>120</td>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>1.2</td>
<td>30</td>
<td>60.4</td>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>1.8</td>
<td>30</td>
<td>24</td>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>2.5</td>
<td>30</td>
<td>14</td>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>3.3</td>
<td>30</td>
<td>9.53</td>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>5</td>
<td>30</td>
<td>5.76</td>
<td>1</td>
<td>100</td>
</tr>
</tbody>
</table>

Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. An inductor with a larger value results in less ripple current and a lower output ripple voltage. However, the larger-value inductor also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current. The peak inductor current should be below the maximum switch current limit.

The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta L \times V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$  (3)

Where $\Delta L$ is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, which can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$  (4)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to $V_{IN}$ as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$  (5)

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2}$$  (6)

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.
The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$  \hspace{1cm} (7)

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}}$$  \hspace{1cm} (8)

**Selecting the Output Capacitor**

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}})$$  \hspace{1cm} (9)

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$  \hspace{1cm} (10)

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR}$$  \hspace{1cm} (11)

Besides the output ripple, a larger output capacitor can also achieve a better load transient response. Maximum output capacitor limitations should be considered in design applications, also. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and fails to regulate. The maximum output capacitor value ($C_{O,max}$) can be limited approximately with Equation (20):

$$C_{O,max} = \left( I_{IM,AVG} - I_{OUT} \right) \times T_{SS} / V_{OUT}$$  \hspace{1cm} (20)

Where $I_{IM,AVG}$ is the average start-up current during the soft-start period, and $T_{SS}$ is the soft-start time.

**PCB Layout Guidelines**

Efficient layout of the switching power supplies is critical for proper function and stable operation. Poor layout design can result in poor line or load regulation and stability issues. To achieve better performances, it is recommended to use two-layer boards. Figure 7 shows the top and bottom layers. For best results, refer to Figure 7 and follow the guidelines below.

1) Place the high current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.

2) Keep the input capacitor as close to IN and GND as possible.

3) Place the external feedback resistors next to FB.

4) Keep the switching node (SW) short and away from the feedback network.
Design Example
Table 2 shows a design example when ceramic capacitors are applied.

<table>
<thead>
<tr>
<th>V&lt;sub&gt;IN&lt;/sub&gt;</th>
<th>12V</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>3.3V</td>
</tr>
<tr>
<td>I&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>3A</td>
</tr>
</tbody>
</table>

The detailed application schematics are shown in Figure 8 through Figure 13. The typical performance and waveforms are shown in the Typical Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.
TYPICAL APPLICATION CIRCUITS

Figure 8: Typical Application Circuit $12V_{\text{IN}}, 5V_{\text{OUT}}/3A$

Figure 9: Typical Application Circuit $12V_{\text{IN}}, 3.3V_{\text{OUT}}/3A$

Figure 10: Typical Application Circuit $12V_{\text{IN}}, 2.5V_{\text{OUT}}/3A$
TYPICAL APPLICATION CIRCUITS (continued)

Figure 11: Typical Application Circuit 12V_{IN}, 1.8V_{OUT}/3A

Figure 12: Typical Application Circuit 12V_{IN}, 1.2V_{OUT}/3A

Figure 13: Typical Application Circuit 12V_{IN}, 1V_{OUT}/3A
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