# MP2227

## 24V, 3A, 1.3MHz Synchronous Step-Down Converter

The Future of Analog IC Technology

## DESCRIPTION

The MP2227 is an internally compensated 1.3MHz fixed frequency PWM synchronous step-down regulator. MP2227 operates from a 3V to 24V input and generates an adjustable output voltage from 0.8V to 0.9x$V_{IN}$ at up to 3A load current.

The MP2227 integrates a 160mΩ high-side switch and an 80mΩ synchronous rectifier for high efficiency without an external Schottky diode. With peak current mode control and internal compensation, it is stable with an output ceramic capacitor and a small inductor. Fault protection includes hiccup short-circuit protection, cycle-by-cycle current limiting and thermal shutdown. Other features include frequency synchronization and soft-start.

The MP2227 is available in a small 3mm x 3mm 10-lead QFN package.

## FEATURES

- 3A Output Current
- Input Supply Range: 3V to 24V
- 160mΩ high-side, 80mΩ low-side Internal Power MOSFET Switches
- All Ceramic Output Capacitor Design
- Up to 95% Efficiency
- 1.3MHz Fixed Switching Frequency
- Adjustable Output from 0.8V to 0.9x$V_{IN}$
- Internal LDO for $V_{CC}$ supply
- 1MHz to 2MHz Frequency Synchronization
- POK
- Thermal Shutdown
- Cycle-by-Cycle Current Limiting
- Hiccup Short Circuit Protection
- 10-lead, 3mm x 3mm QFN Package

## APPLICATIONS

- µP/ASIC/DSP/FPGA Core and I/O Supplies
- Printers and LCD TVs
- Network and Telecom Equipment
- Point of Load Regulators

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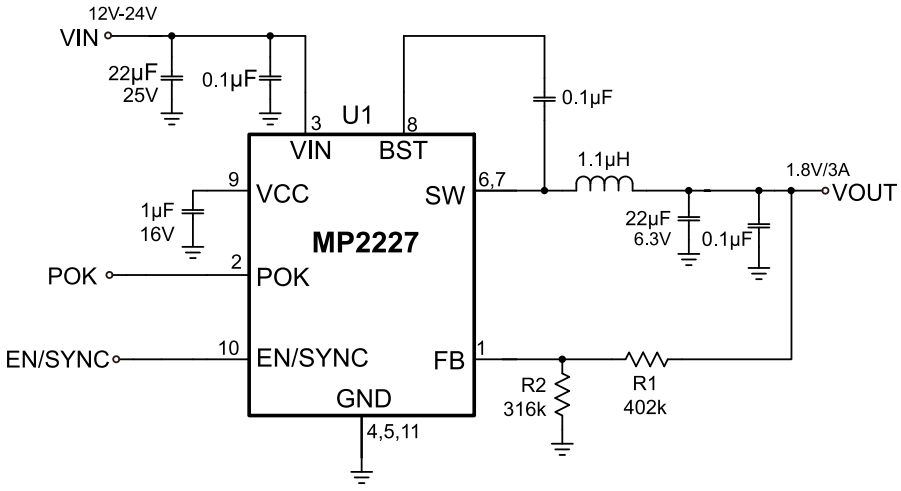
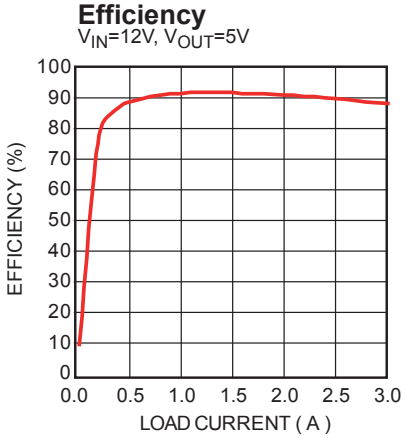
## TYPICAL APPLICATION





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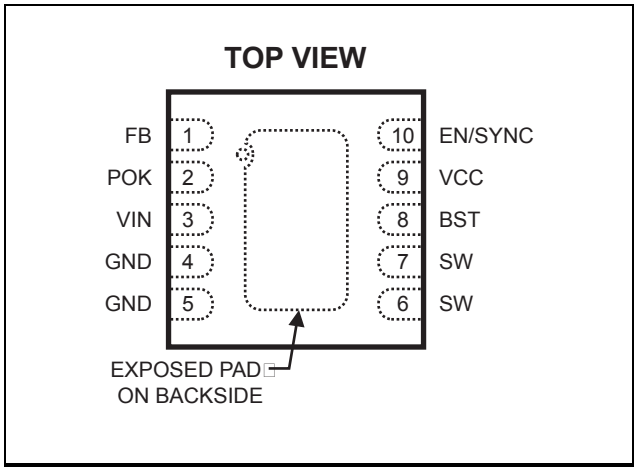
## ORDERING INFORMATION

| Part Number* | Package | Top Marking | Free Air Temperature ($T_A$) |
|---|---|---|---|
| MP2227DQ | QFN10(3mm x 3mm) | 7U | -40°C to +85°C |

* For Tape & Reel, add suffix –Z (e.g. MP2227DQ–Z).
For RoHS Compliant packaging, add suffix –LF (e.g. MP2227DQ–LF–Z)

## PACKAGE REFERENCE




## ABSOLUTE MAXIMUM RATINGS (1)

VIN to GND .....-0.3V to +28V
SW to GND .....-0.3V to $V_{IN}$ + 0.3V
.....-2.5V to $V_{IN}$ + 2.5V for < 50ns
FB, EN/SYNC, VCC to GND.....-0.3V to +6.5V
POK, SYNC_OUT to GND .....-0.3V to +6.5V
BS to SW .....-0.3V to +6.5V
Continuous Power Dissipation ($T_A$ = +25°C) (2)
.....2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

### *Recommended Operating Conditions* (3)

Supply Voltage $V_{IN}$ .....3V to 24V
Output Voltage $V_{OUT}$.....0.8V to 0.9 x $V_{IN}$
Max Operating Junct. Temp ($T_J$).....+125°C

### *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

QFN10 (3mm x 3mm) .....50 ..... 12 ... °C/W

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.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## ELECTRICAL CHARACTERISTICS (5)

**$V_{IN}$=12V, $T_A$ = +25°C, unless otherwise noted.**

| Parameters | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Quiescent Supply Current | $V_{EN}$ = HIGH<br>$V_{FB}$ = 0.85V, not switching | | 1 | | mA |
| Shutdown Current | $V_{EN}$ = 0V | | 1 | | μA |
| $V_{CC}$ Under Voltage Lockout Threshold | Rising Edge | | 2.7 | 2.95 | V |
| $V_{CC}$ Under Voltage Lockout Hysteresis | | | 300 | | mV |
| IN Under Voltage Lockout Threshold, Rising Edge | | | 2.85 | 2.95 | V |
| IN Under Voltage Lockout Hysteresis | | | 300 | | mV |
| Regulated FB Voltage | $T_A$ = +25°C | 0.784 | 0.800 | 0.816 | V |
| | -40°C ≤ $T_A$ ≤ +85°C | 0.780 | | 0.820 | V |
| FB Input Current | $V_{FB}$ = 0.85V | -50 | | 50 | nA |
| EN High Threshold | -40°C ≤ $T_A$ ≤ +85°C | 1.6 | | | V |
| EN Low Threshold | -40°C ≤ $T_A$ ≤ +85°C | | | 0.4 | V |
| High-Side Switch On-Resistance | $I_{SW}$ = 300mA | | 160 | | mΩ |
| Low-Side Switch On-Resistance | $I_{SW}$ = –300mA | | 80 | | mΩ |
| SW Leakage Current | $V_{EN}$ = 0V; $V_{IN}$ = 12V<br>$V_{SW}$ = 0V or 12V | -1 | | 1 | μA |
| BS Under Voltage Lockout Threshold | | | 1.8 | | V |
| High-Side Switch Current Limit | Sourcing | | 4.5 | | A |
| Low-Side Switch Current Limit | Sinking | | 2.5 | | A |
| Oscillator Frequency | | 1 | 1.3 | 1.6 | MHz |
| Maximum Synch Frequency | | | 2 | | MHz |
| Minimum Synch Frequency | | | 1 | | MHz |
| Minimum On Time | | | 50 | | ns |
| Maximum Duty Cycle | | | 90 | | % |
| POK Upper Trip Threshold | FB respect to the nominal value | | 10 | | % |
| POK Lower Trip Threshold | FB respect to the nominal value | | -10 | | % |
| POK Output Voltage Low | $I_{SINK}$ = 5mA | | | 0.4 | V |
| POK Deglitch Timer | | | 40 | | μs |
| SYNC_Input High Level | $V_{CC}$ = 5V, Source 5mA | 4.6 | | | V |
| SYNC_Input Low Level | $V_{CC}$ = 5V, Sink 5mA | | | 0.4 | V |
| Thermal Shutdown Threshold | Hysteresis = 20°C | | 150 | | °C |

**Note:**

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.


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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | FB | Feedback. This is the input to the error amplifier. An external resistive divider connected between the output and GND is compared to the internal 0.8V reference to set the regulation voltage. |
| 2 | POK | Open Drain Power Good Output. “HIGH” output indicates VOUT is within ±10% window. “LOW” output indicates VOUT is out of ±10% window. POK is pulled down in shutdown. |
| 3 | IN | Input Supply. This supplies power to the high side switch. A decoupling capacitor to ground is required close to this pin to reduce switching spikes. |
| 4, 5 | GND | Ground. Connect these pins with larger copper areas to the negative terminals of the input and output capacitors. |
| 6,7 | SW | Switch Node Connection to the Inductor. These pins connect to the internal high and low-side power MOSFET switches. All SW pins must be connected together externally. |
| 8 | BST | Bootstrap. A capacitor between this pin and SW provides a floating supply for the high-side gate driver. |
| 9 | VCC | Bias Supply. Provide 5V to this pin when the input voltage is less than 5V. Otherwise it does not need external supply. This supplies power to both the internal control circuit and the gate drivers. A decoupling capacitor to ground is required close to this pin. |
| 10 | EN/SYNC | Enable and Frequency Synchronization Input Pin. Forcing this pin below 0.4V shuts down the part. Forcing this pin above 1.6V turns on the part. Applying a 1MHz to 2MHz clock signal to this pin synchronizes the internal oscillator frequency to the external source. To enable the device, connect this pin to $V_{IN}$ through a 100kΩ resistor. When $V_{IN}$ is less than 5V and $V_{CC}$ is externally biased, this pin can also be connected to $V_{CC}$ through a 100kΩ resistor. |


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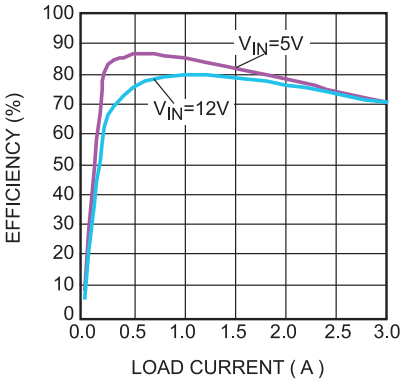
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 1.8V, $C_{1A}$ = 22µF, $C_{2A}$ = $C_{2B}$ = 22µF, L = 1.5µH, $T_A$ = +25ºC, unless otherwise noted.**

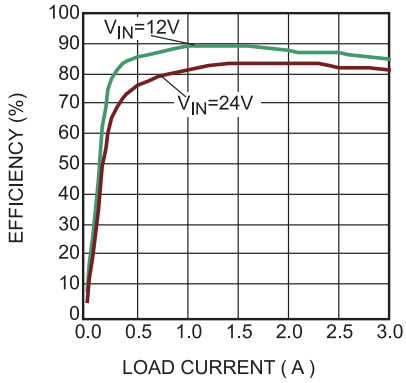
**Efficiency vs. Load Current**

$V_{OUT}$=1.2V



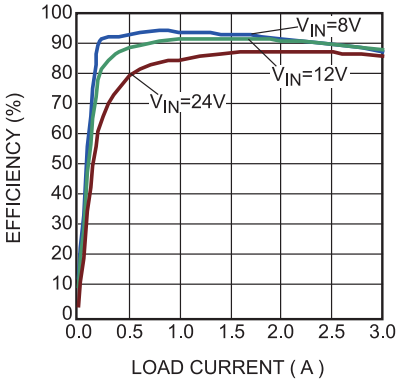

**Efficiency vs. Load Current**

$V_{OUT}$=3.3V

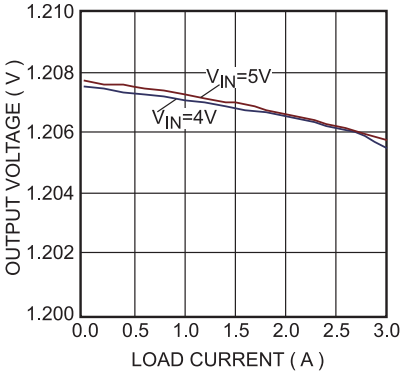



**Efficiency vs. Load Current**

$V_{OUT}$=5V




**Load Regulation**

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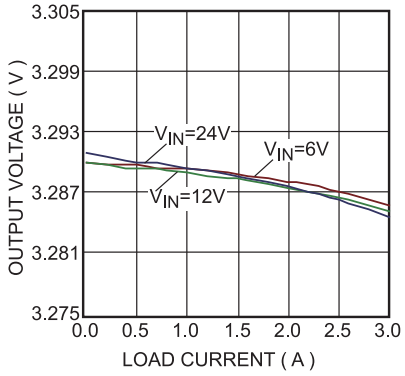
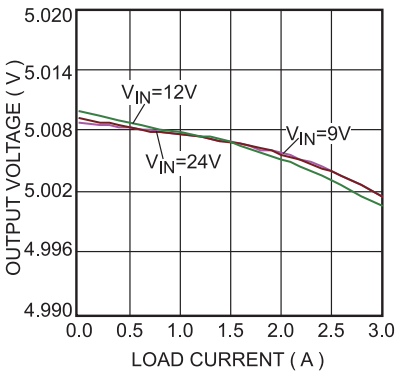
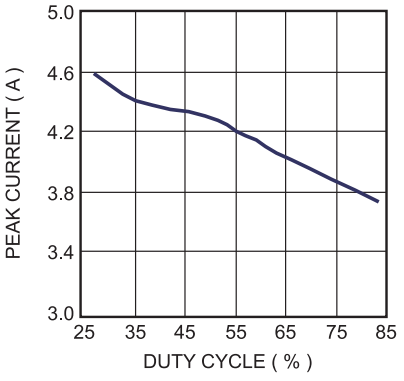



**Load Regulation**

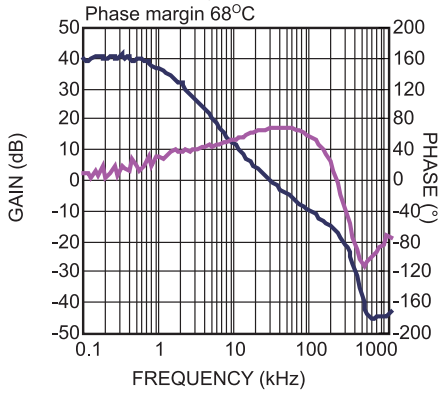



**Peak Current vs. Duty Cycle**

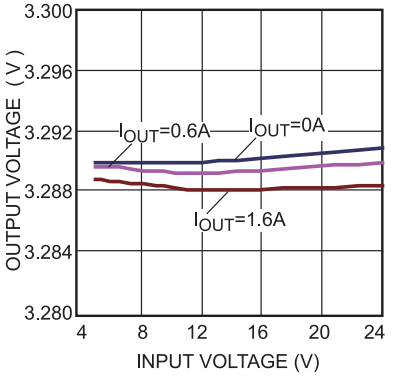



**Loop Gain with Phase Margin**

$V_{IN}$=5V, $V_{OUT}$=1.2V, $I_{OUT}$=3A
0dB Frequency 31kHz
Phase margin 68°C




**Line Regulation**





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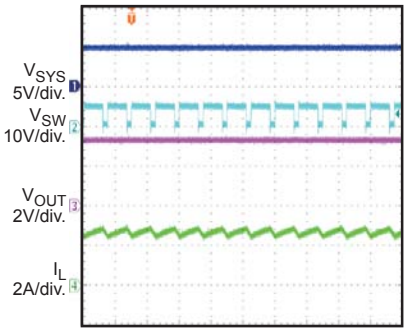
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 1.8V, $C_{1A}$ = 22µF, $C_{2A}$ = $C_{2B}$ = 22µF, L = 1.5µH, $T_A$ = +25ºC, unless otherwise noted.**

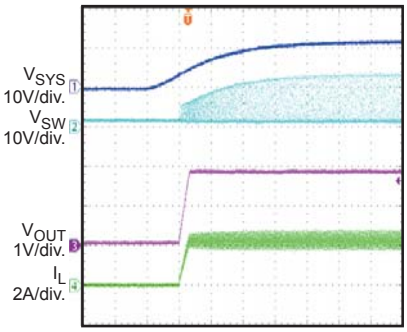
### Steady State

$V_{SYS}$ = 5V, $V_{EN}$ put to $V_{IN}$, $V_{OUT}$= 3.3V, $I_{OUT}$ = 3A



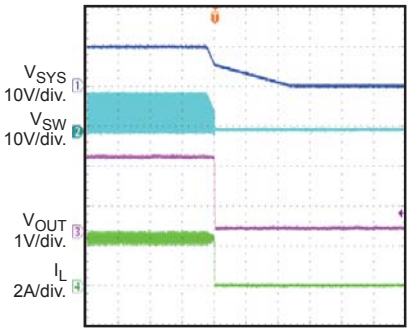

### Power Ramp Up

$V_{IN}$ = 12V, $V_{EN}$ put to $V_{IN}$, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A



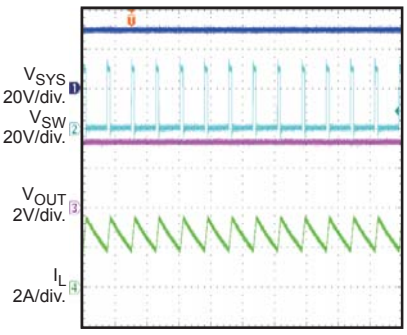

### Power Ramp Down

$V_{IN}$ = 12V, $V_{EN}$ put to $V_{IN}$, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A



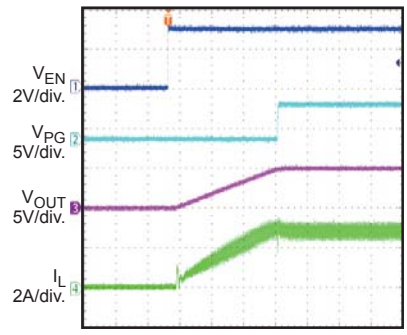

### Steady State

$V_{IN}$ = 26V, $V_{EN}$ put to $V_{IN}$, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 3A



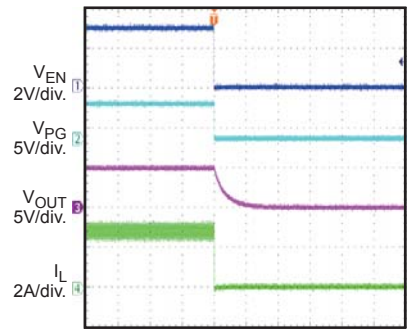

### Enable Up

$V_{IN}$ = 12V, $V_{EN}$ = 0-3V, $V_{OUT}$ = 5V, $I_{OUT}$ = 3A, Resistor Load



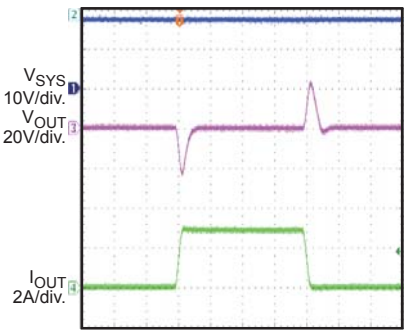

### Enable Down

$V_{IN}$ = 12V, $V_{EN}$ = 3-0V, $V_{OUT}$ = 5V, $I_{OUT}$ = 3A, Resistor Load



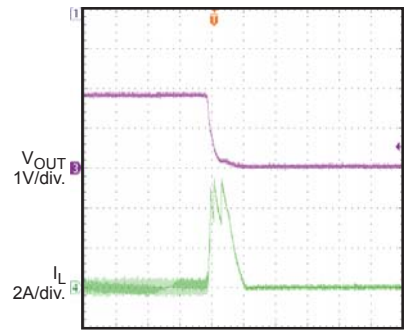

### Transient Response

$V_{IN}$ = 18V, $V_{IN}$,$V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A



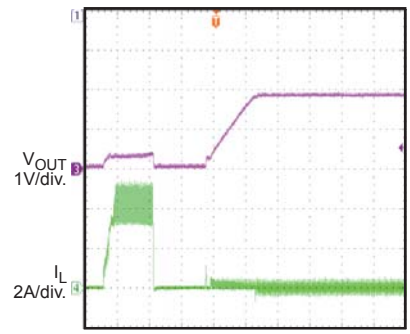

### Short Circuit

$V_{IN}$ = 18V, $V_{EN}$ put to $V_{IN}$, $V_{OUT}$ = 1.8V




### Short Circuit Recovery

$V_{IN}$ = 18V, $V_{EN}$ put to $V_{IN}$, $V_{OUT}$ = 1.8V





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# FUNCTIONAL BLOCK DIAGRAM

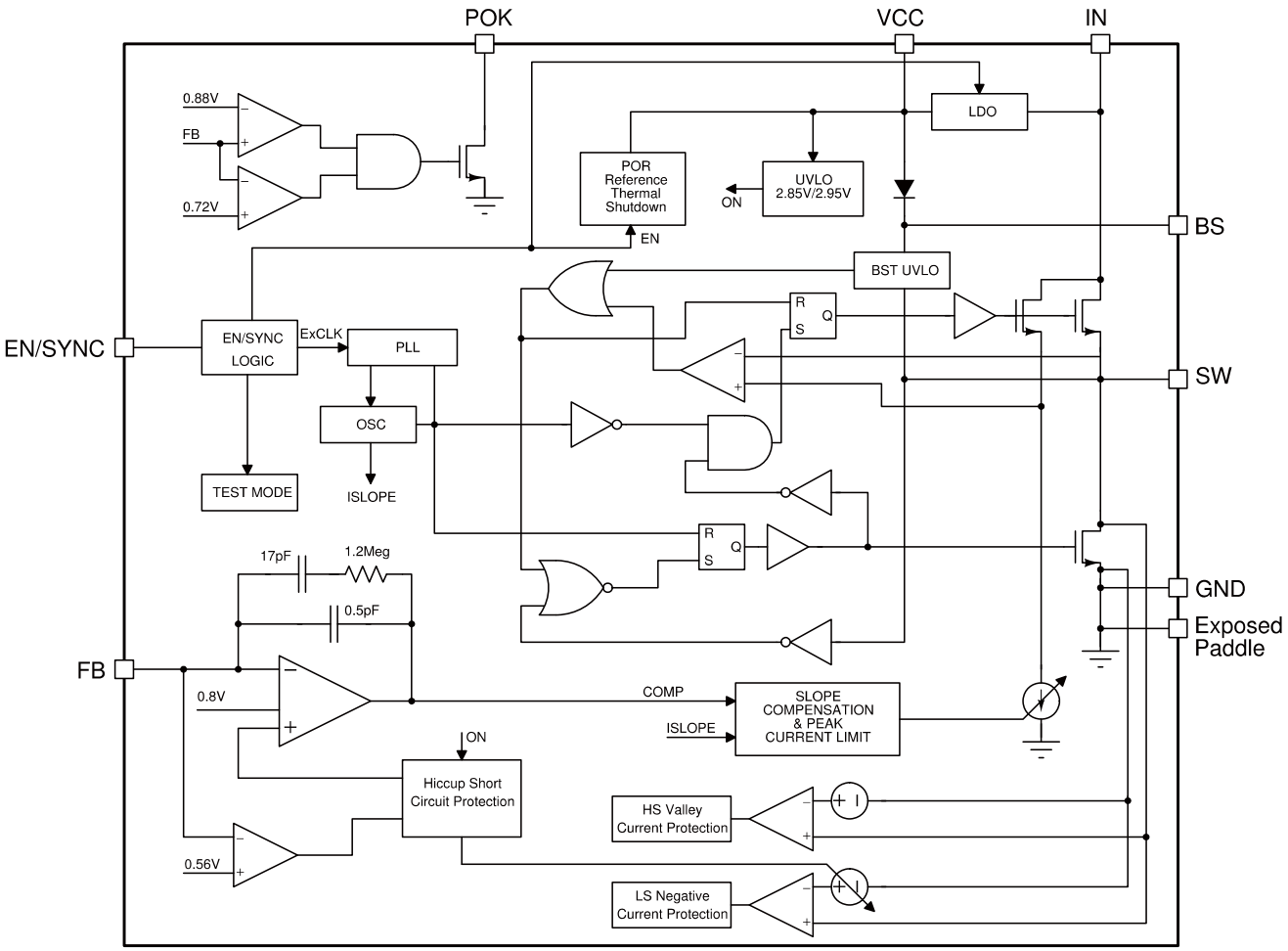


**Figure 1—Functional Block Diagram**


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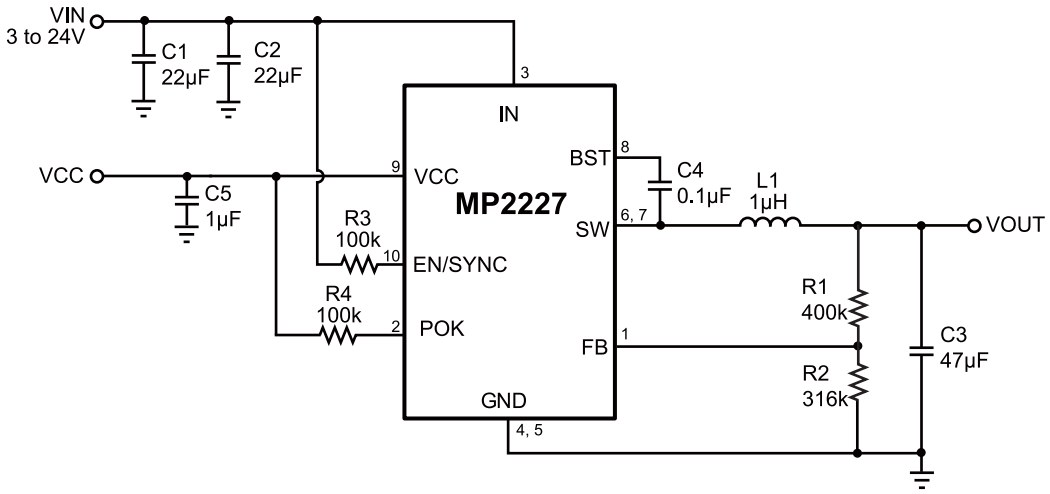
## TYPICAL APPLICATION





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# FUNCTIONAL DESCRIPTION

### PWM Control

The MP2227 is a constant frequency peak-current-mode control PWM switching regulator. Refer to the functional block diagram. The high side N-Channel DMOS power switch turns on at the beginning of each clock cycle. The current in the inductor increases until the PWM current comparator trips to turn off the high side DMOS switch. The peak inductor current at which the current comparator shuts off the high side power switch is controlled by the COMP voltage at the output of feedback error amplifier. The transconductance from the COMP voltage to the output current is set at 11.25A/V.

This current-mode control greatly simplifies the feedback compensation design by approximating the switching converter as a single-pole system. Only Type II compensation network is needed, which is integrated into the MP2227. The loop bandwidth is adjusted by changing the upper resistor value of the resistor divider at the FB pin. The internal compensation in the MP2227 simplifies the compensation design, minimizes external component counts, and keeps the flexibility of external compensation for optimal stability and transient response.

### Enable and Frequency Synchronization (EN/SYNC PIN)

This is a dual function input pin. Forcing this pin below 0.4V for longer than 4us shuts down the part; forcing this pin above 1.6V for longer than 4μs turns on the part. Applying a 1MHz to 2MHz clock signal to this pin also synchronizes the internal oscillator frequency to the external clock. When the external clock is used, the part turns on after detecting the first few clocks regardless of duty cycles. If any ON or OFF period of the clock is longer than 4μs, the signal will be intercepted as an enable input and disables the synchronization.

### Soft-Start and Output Pre-Bias Startup

When the soft-start period starts, an internal current source begins charging an internal soft-start capacitor. During soft-start, the voltage on the soft-start capacitor is connected to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.8V. At this point the reference voltage takes over at the non-inverting error amplifier input. The soft-start time is internally set at 120μs. If the output of the MP2227 is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

### Over Current Protection

The MP2227 offers cycle-to-cycle current limiting for both high-side and low-side switches. The high-side current limit is relatively constant regardless of duty cycles. When the output is shorted to ground, causing the output voltage to drop below 70% of its nominal output, the IC is shut down momentarily and begins discharging the soft start capacitor. It will restart with a full soft-start when the soft- start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

### Bootstrap (BST PIN)

The gate driver for the high-side N-channel DMOS power switch is supplied by a bootstrap capacitor connected between the BS and SW pins. When the low-side switch is on, the capacitor is charged through an internal boost diode. When the Low-side switch is off and the high-side switch turns on, the voltage on the bootstrap capacitor is boosted above the input voltage and the internal bootstrap diode prevents the capacitor from discharging.

No external bootstrap diode is required for typical applications. For applications with low input VCC voltage or where output voltage is very close to input voltage, an external Schottky diode may be connected from the VCC to BS pins to charge the bootstrapped capacitor more strongly for increased gate drive voltage. When using the external bootstrap diode, a resistor at the regulator output or a minimal load current may be required as the bootstrapped capacitor


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always see the supply voltage even when the part is disabled.

**Input UVLO**

Both VCC and IN pins have input UVLO detection. Until both VCC and IN voltage under voltage lockout threshold, the parts remain in shutdown condition. There are also under voltage lockout hysesteres at both VCC and IN pins.


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# APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application Schematic). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). The relation between R1 and feedback loop bandwidth ($f_C$), output capacitance ($C_O$) is as follows:

$$R1(K\Omega) = \frac{1.24 \times 10^6}{f_C(kHz) \times C_O(\mu F)}.$$

The feedback loop bandwidth ($f_C$) is no higher than 1/10$^{th}$ of switching frequency of MP2227. In the case of ceramic capacitor as $C_O$, it's usually set to be in the range of 50kHz and 150kHz for optimal transient performance and good phase margin. If electrolytic capacitor is used, the loop bandwidth is no higher than 1/4$^{th}$ of the ESR zero frequency ($f_{ESR}$). $f_{ESR}$ is given by:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_O}$$

For example, choose $f_C$=70kHz with ceramic capacitor, $C_O$=47uF, R1 is estimated to be 400KΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

**Table 1—Resistor Selection vs. Output Voltage Setting**

| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) | L (μH) | $C_{OUT}$ (ceramic) |
|---|---|---|---|---|
| 1.2 | 400 | 806 | 0.47μH-1μH | 47μF |
| 1.5 | 400 | 453 | 0.47μH-1μH | 47μF |
| 1.8 | 400 | 316 | 0.47μH-1μH | 47μF |
| 2.5 | 400 | 187 | 0.47μH-1μH | 47μF |
| 3.3 | 400 | 127 | 0.47μH-1μH | 47μF |

### Selecting the Inductor

A 0.47μH to 1μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <10mΩ. See Table 2 for recommended inductors and manufacturers. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} x (V_{IN} - V_{OUT})}{V_{IN} x \Delta I_L x f_{OSC}}$$

Where ΔIL is Inductor Ripple Current. Choose inductor ripple current approximately 30% of the maximum load current, 3A.The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions, larger inductance is recommended for improved efficiency

### Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 47μF capacitor is sufficient.


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**Table 2—Suggested Surface Mount Inductors**

| Manufacturer | Part Number | Inductance (µH) | Max DCR (mΩ) | Current Rating (A) | Dimensions L x W x H ($mm^3$) |
|---|---|---|---|---|---|
| Wurth Electronics | | | | | |
| | 744310055 | 0.55 | 4.5 | 14 | 7×6.9×3 |
| | 744310095 | 0.95 | 7.4 | 11 | 7×6.9×3 |
| TOKO | | | | | |
| | B1015AS-1R0N | 1 | 11 | 6.9 | 8.4×8.3×4 |

### Output Capacitor Selection

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. If electrolytic capacitor is used, pay attention to output ripple voltage, extra heating, and the selection of feedback resistor R1 (refer to "Output Voltage Setting" section) due to large ESR of electrolytic capacitor. The output ripple $\Delta V_{OUT}$ is approximately:

$$\Delta V_{OUT} \leq \frac{V_{OUT} x (V_{IN} - V_{OUT})}{V_{IN} x f_{OSC} x L} x (ESR + \frac{1}{8 x f_{OSC} x C3})$$

### PC Board Layout

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. A 0.1µF-1µF ceramic is recommended for VCC supply. C5 must be placed as close as possible to "VCC" pin and "GND" pin. The external feedback resistors shall be placed next to the FB pin. Keep the switching node SW short and away from the feedback network. Please see EV2227EQ datasheet for detailed info.


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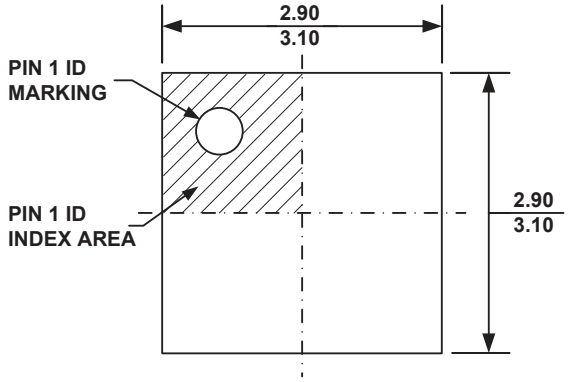
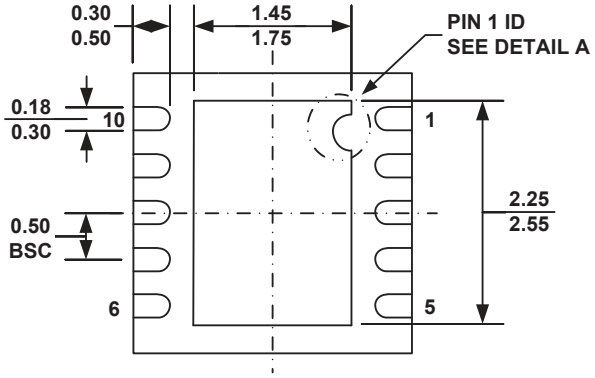
# PACKAGE INFORMATION

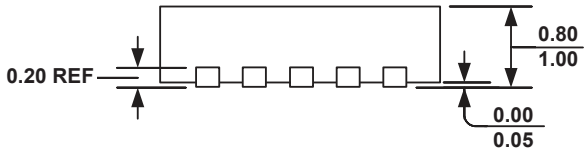
## QFN10 (3mm x 3mm)



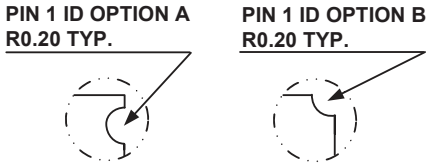

TOP VIEW



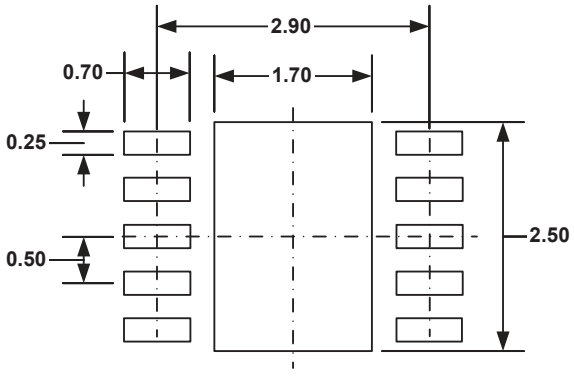

BOTTOM VIEW




SIDE VIEW




DETAIL A




RECOMMENDED LAND PATTERN

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

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