



# MP2183C

2.5V to 5.5V, 3A, Synchronous,  
Step-Down Converter with SS, PG,  
and Forced PWM in SOT583 Package

## DESCRIPTION

The MP2183C is a monolithic, step-down, switch-mode converter with built-in internal power MOSFETs. It achieves 3A of continuous output current from a 2.5V to 5.5V input voltage range, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

A constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2183C is ideal for a wide range of applications including high-performance DSPs, wireless power, portable and mobile devices, and other low-power systems.

The device requires a minimal number of readily available, standard external components. It is available in an ultra-small SOT583 package.

## FEATURES

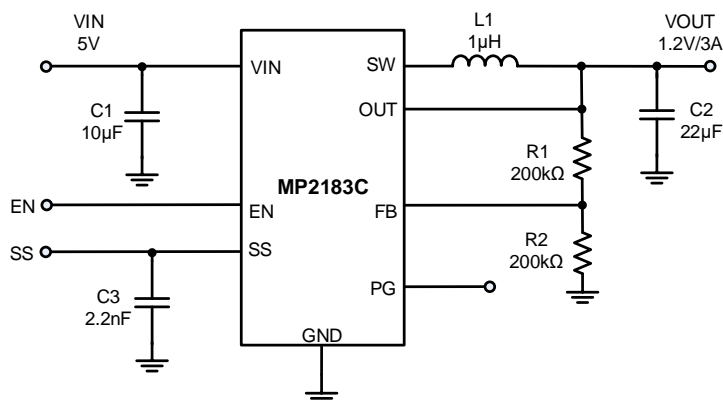
- Forced PWM Mode Operation
- 1.2MHz Switching Frequency
- EN for Power Sequencing
- 1% FB Accuracy
- Wide 2.5V to 5.5V Operating Input Range
- Output Adjustable from 0.6V
- Up to 3A Output Current
- 65mΩ and 35mΩ Internal Power MOSFET Switches
- 100% Duty On
- Output Discharge
- V<sub>O</sub> OVP
- External Soft Start Control
- Short-Circuit Protection with Hiccup Mode
- Power Good
- Available in a SOT583 Package

## APPLICATIONS

- Wireless/Networking Cards
- Portable Instruments
- Low-Voltage I/O System Power
- Multi-Function Printers

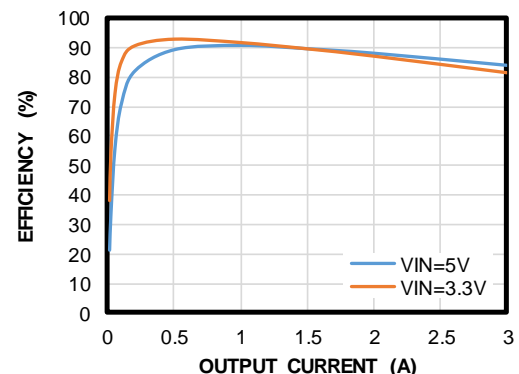
All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

## TYPICAL APPLICATION



### Efficiency vs. Output Current

V<sub>OUT</sub> = 1.2V, L = 1µH (DCR = 27mΩ)



### ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2183CGTL	SOT583	See Below	1

\* For Tape & Reel, add suffix -Z (e.g. MP2183CGTL-Z).

### TOP MARKING

**BMCY**

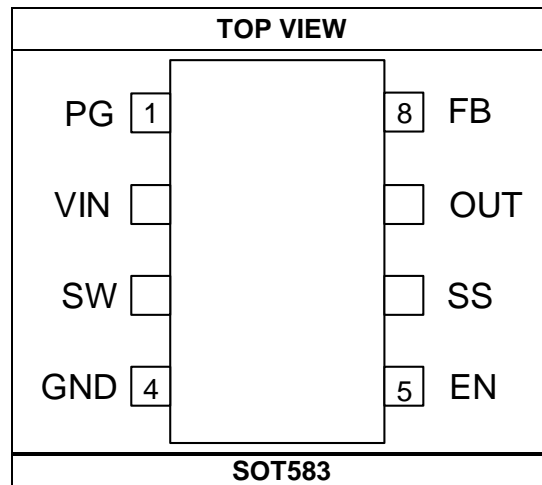
**LLL**

BMC: Product code of MP2183CGTL

Y: Year code

LLL: Lot number

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	PG	<b>Power good indicator.</b> The output of this pin is an open drain.
2	VIN	<b>Supply voltage.</b> The MP2183C operates from a 2.5V to 5.5V unregulated input. A decoupling capacitor is required to prevent large voltage spikes from appearing at the input.
3	SW	<b>Output switching node.</b> SW is the drain of the internal, high-side, P-channel MOSFET. Connect the inductor to SW to complete the converter.
4	GND	<b>Ground.</b>
5	EN	<b>On/off control.</b>
6	SS	<b>Soft start.</b> Connect a capacitor across SS and GND to set the soft-start time to avoid start-up inrush current.
7	OUT	<b>Output voltage power rail and input sense pin for output voltage.</b> Connect the load to this pin. Use an output capacitor to decrease the output voltage ripple.
8	FB	<b>Feedback pin.</b> An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.

### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply voltage ( $V_{IN}$ )	6.5V
$V_{SW}$	-0.3V (-5V for <10ns) to 6.5V (8V for <10ns)
All other pins	-0.3V to +6.5V
Junction temperature	150°C
Lead temperature	260°C
Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2) (4)</sup>	2.3W
Storage temperature	-65°C to +150°C

### ESD Rating

Human-body model (HBM)	2000V
Charged-device model (CDM)	1250V

### Recommended Operating Conditions <sup>(3)</sup>

Supply voltage ( $V_{IN}$ )	2.5V to 5.5V
Operating junction temp ( $T_J$ )	-40°C to +125°C

Thermal Resistance	$\theta_{JA}$	$\theta_{JC}$
SOT583		
EV2183C-TL-00A <sup>(4)</sup>	58	13
JESD51-7 <sup>(5)</sup>	120	55

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on EV2183C-TL-00A, 2-layer PCB.
- Measured on JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(6)</sup>, typical value is tested at  $T_J = 25^{\circ}C$ . The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
$V_{IN}$ range			2.5		5.5	V
Under-voltage lockout rising threshold				2.3	2.45	V
Under-voltage lockout hysteresis threshold				350		mV
Supply current (shutdown)		$V_{EN} = 0V$ , $T_J = 25^{\circ}C$		0	1	$\mu A$
Supply current (quiescent)		$V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 3.6V$ , $T_J = 25^{\circ}C$		450		$\mu A$
Feedback voltage	$V_{FB}$	$T_J = 25^{\circ}C$	594	600	606	mV
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	591	600	609	
Feedback current	$I_{FB}$	$V_{FB} = 0.63V$		50	100	nA
PFET switch on resistance	$R_{DSON\_P}$	$V_{IN} = 5V$		65		m $\Omega$
NFET switch on resistance	$R_{DSON\_N}$	$V_{IN} = 5V$		35		m $\Omega$
Switch leakage		$V_{EN} = 0V$ , $V_{IN} = 6V$ $V_{SW} = 0V$ or $6V$ , $T_J = 25^{\circ}C$		0	1	$\mu A$
Switching frequency	$f_{SW}$	$V_{IN} = 5V$ , $V_{OUT} = 1.2V$ , operating under CCM		1200		kHz
Minimum on time <sup>(7)</sup>	$t_{MIN-ON}$	$V_{IN} = 3.6V$		70		ns
		$V_{IN} = 2.5V$		80		ns
Minimum off time <sup>(7)</sup>	$t_{MIN-OFF}$	$V_{IN} = 3.6V$		80		ns
		$V_{IN} = 2.5V$		90		ns
PFET peak current limit				5		A
NFET valley current limit				3		A
Soft-start current	$I_{SS\_ON}$		1.5	3	4.5	$\mu A$
Maximum duty cycle			100			%
Power good rising threshold UV		FB rising edge	87	90	93	%
Power good falling threshold UV		FB falling edge	82	85	88	%
Power good delay	$PG_D$	PG rising/falling edge		80		$\mu s$
Power good sink current capability	$V_{PG-L}$	Sink 1mA			0.4	V
Power good logic high voltage	$V_{PG-H}$	$V_{IN} = 5V$ , $V_{FB} = 0.6V$	4.9			V
Self-bias PG		When $V_{IN}$ & $EN$ are not available, PG pull-up voltage = 3.6V, pull-up resistor = 300k $\Omega$			0.7	V

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(6)</sup>, typical value is tested at  $T_J = 25^{\circ}C$ . The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good leakage current/logic high		5V logic high			100	nA
EN turn-on delay		EN on to SW active		100		$\mu s$
EN turn-off delay		EN off to stop switching		30		$\mu s$
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
EN pull down resistor				2		M $\Omega$
Output discharge resistor	R <sub>DIS</sub>	$V_{EN} = 0V$ , $V_{OUT} = 1.2V$		150		$\Omega$
EN input current		$V_{EN} = 2V$		1		$\mu A$
		$V_{EN} = 0V$		0		$\mu A$
Output over-voltage threshold	V <sub>OVP</sub>		110%	115%	120%	V <sub>FB</sub>
V <sub>O</sub> OVP hysteresis	V <sub>OVP_HYS</sub>			10%		V <sub>FB</sub>
OVP delay				6		$\mu s$
Low-side current limit		Current flow from SW to GND		1.5		A
Absolute VIN OVP		After V <sub>O</sub> OVP enable		6.1		V
Absolute VIN OVP hysteresis				160		mV
Thermal shutdown <sup>(7)</sup>				160		$^{\circ}C$
Thermal hysteresis <sup>(7)</sup>				30		$^{\circ}C$

**Notes:**

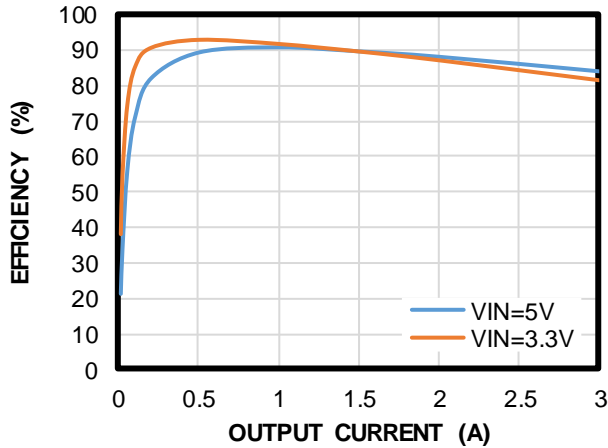
- 6) Not tested in production. Guaranteed by over-temperature correlation.  
 7) Guaranteed by engineering sample characterization.

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 3.6V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C_{OUT} = 44\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

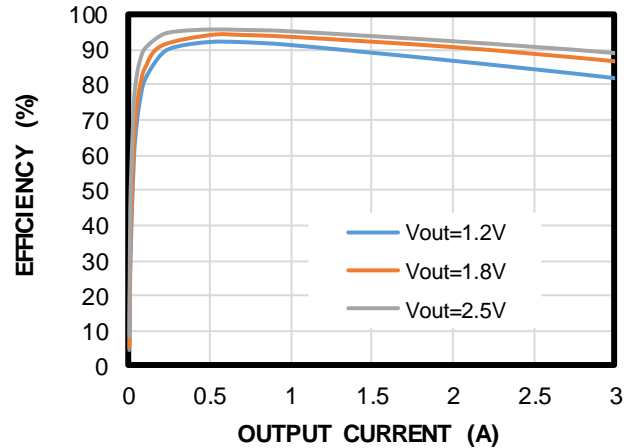
**Efficiency vs. Output Current**

$V_{OUT} = 1.2V$ ,  $L = 1\mu H$  (DCR = 27m $\Omega$ )



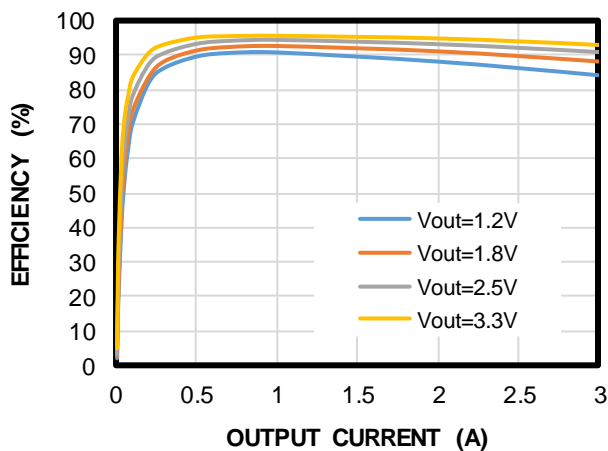
**Efficiency vs. Output Current**

$V_{IN} = 3.6V$ ,  $L = 1\mu H$  (DCR = 27m $\Omega$ )



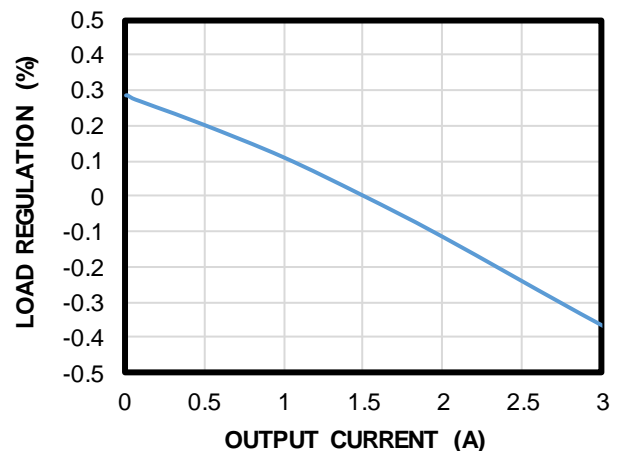
**Efficiency vs. Output Current**

$V_{IN} = 5V$ ,  $L = 1\mu H$  (DCR = 27m $\Omega$ )



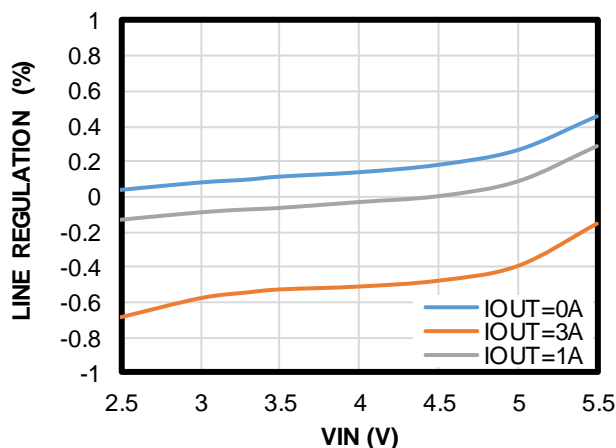
**Load Regulation**

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$

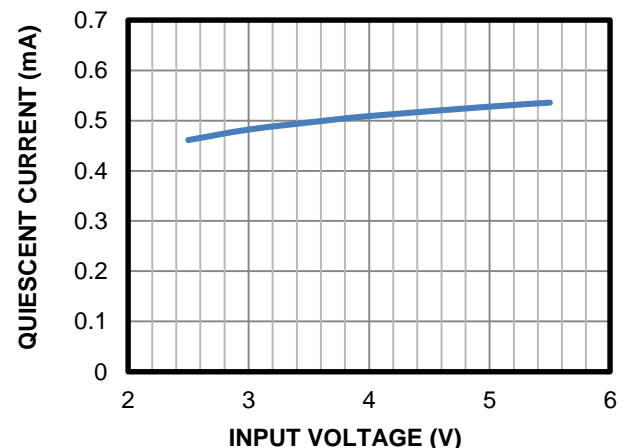


**Line Regulation**

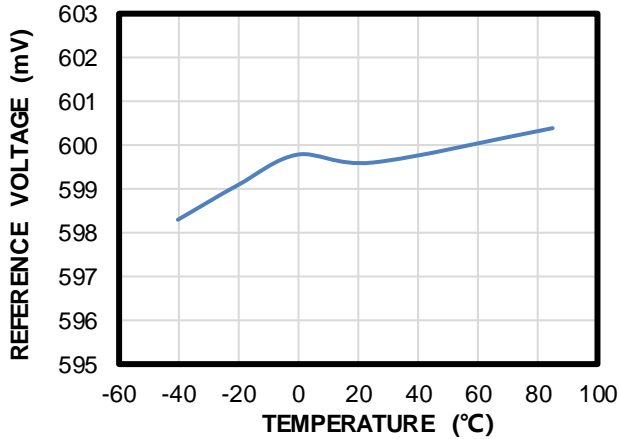
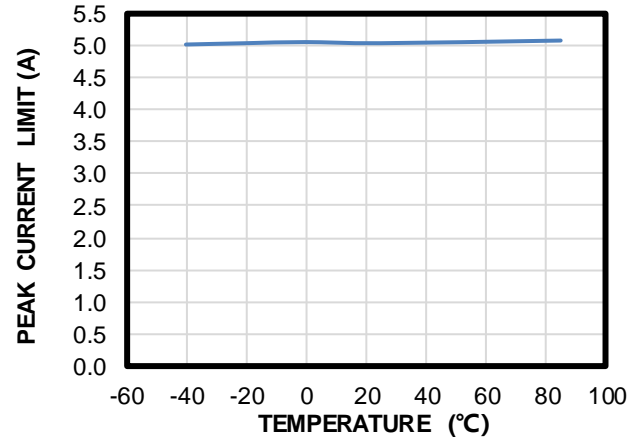
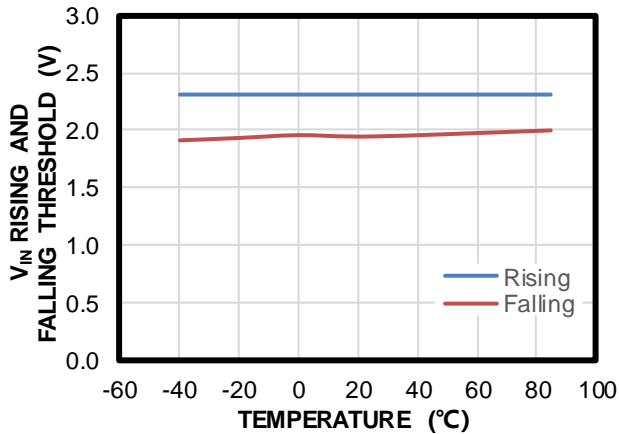
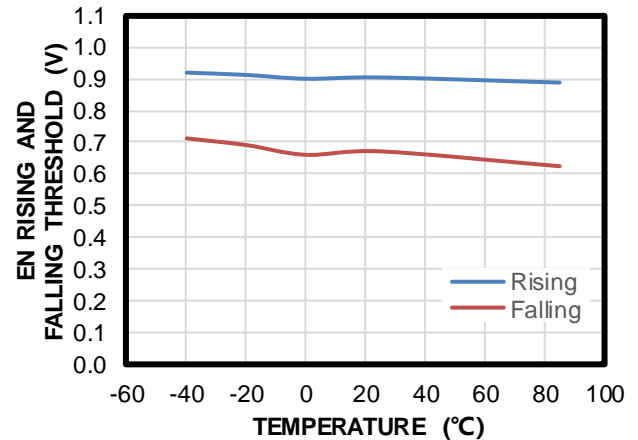
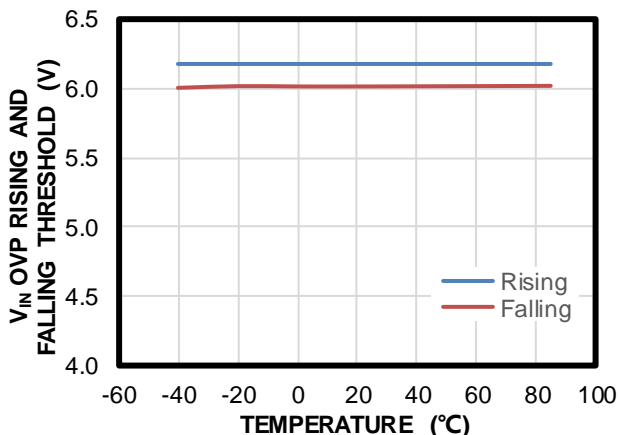
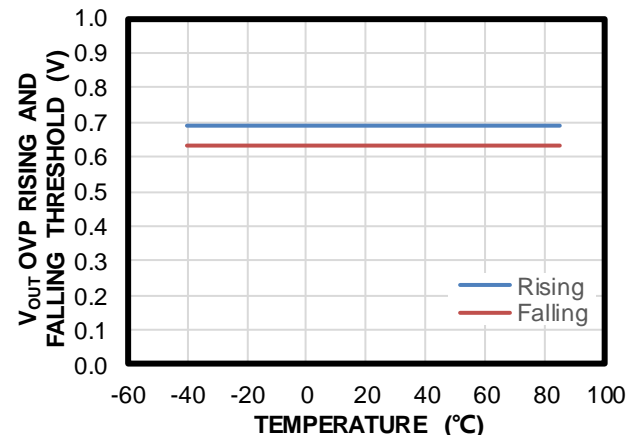
$V_{OUT} = 1.2V$



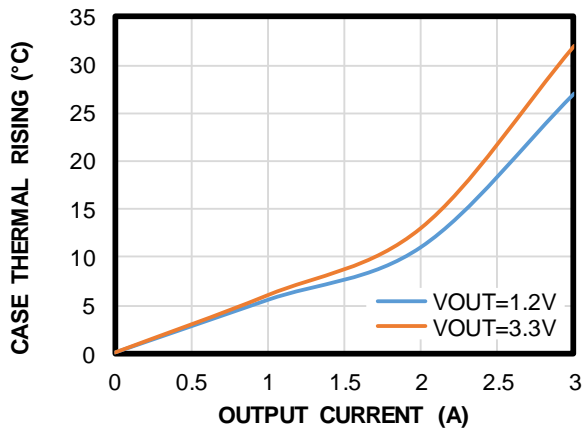
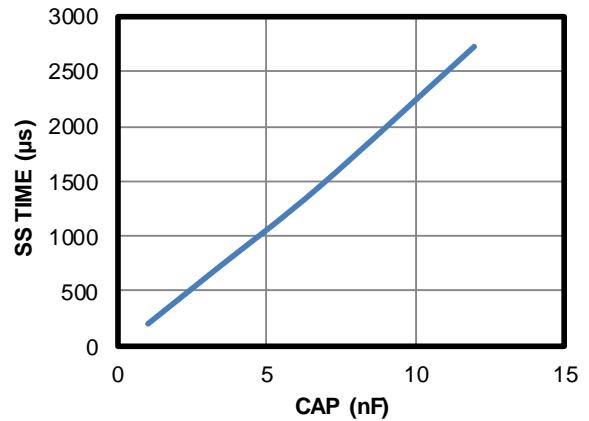
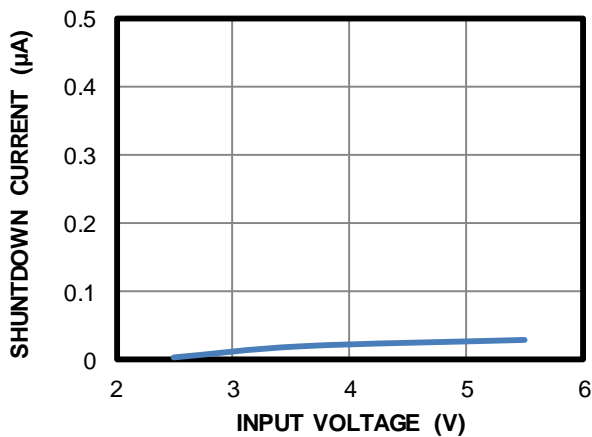
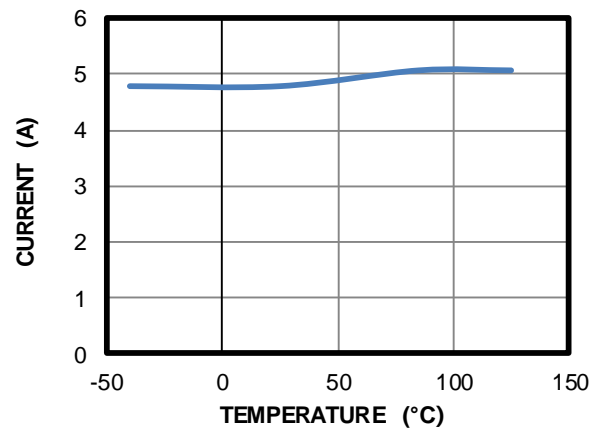
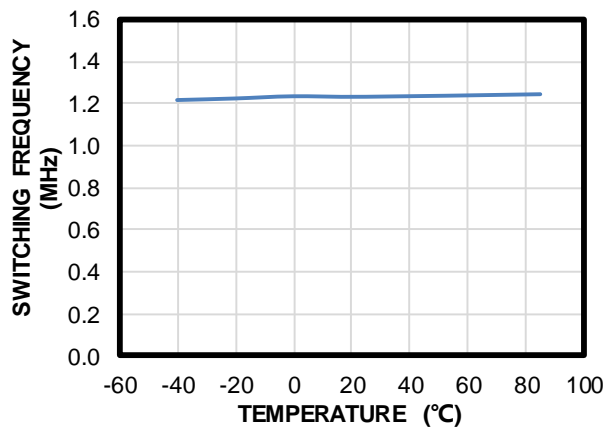
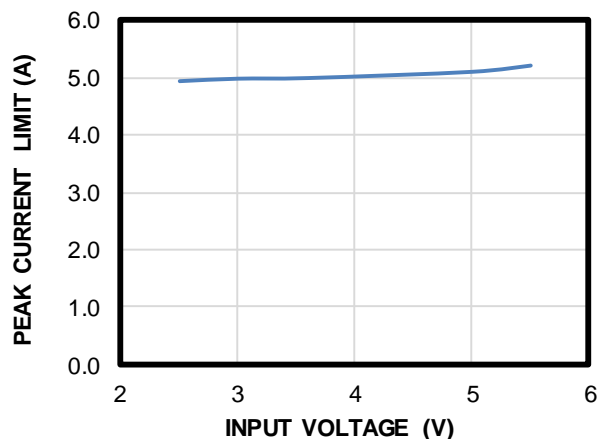
**Quiescent Current vs. Input Voltage**



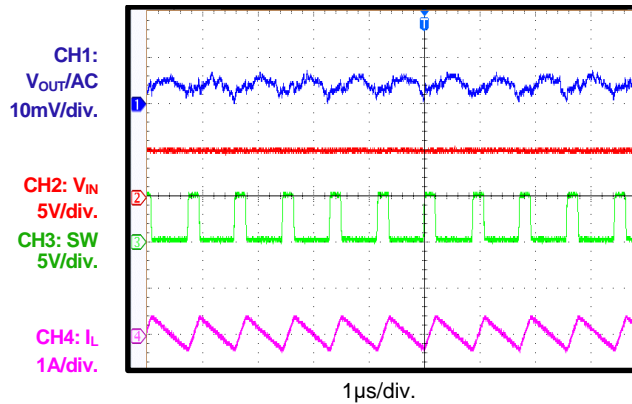
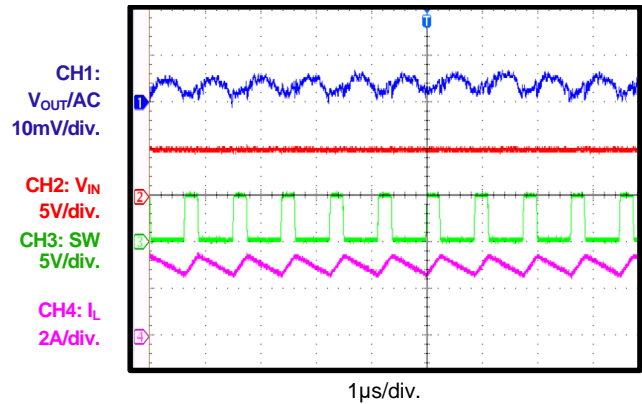
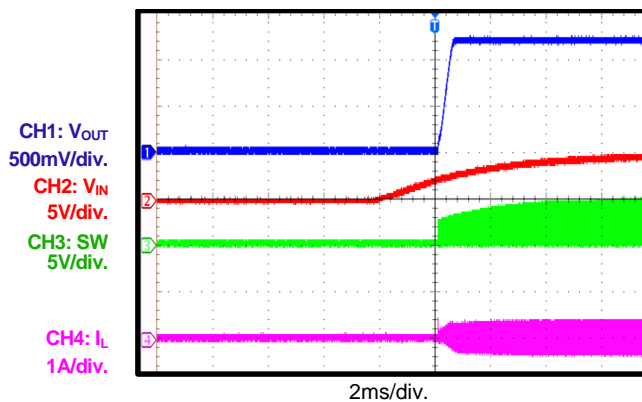
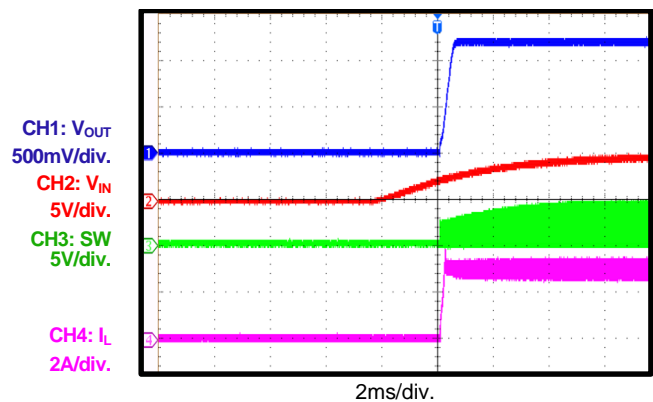
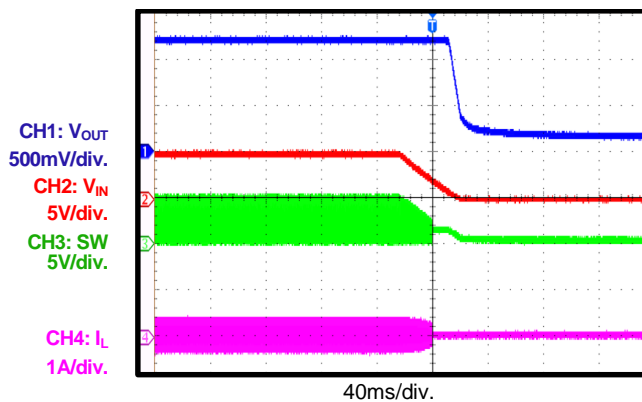
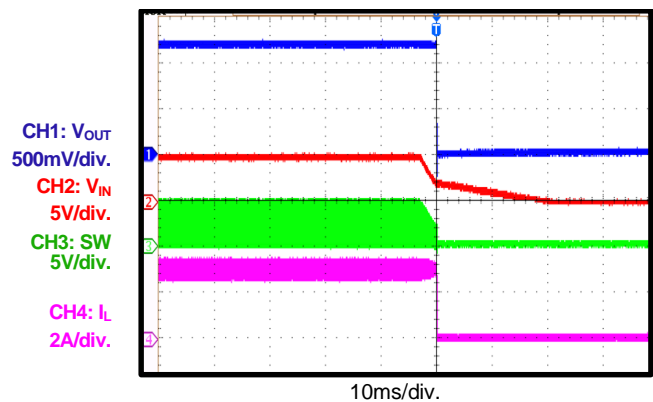
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 3.6V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C_{OUT} = 44\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

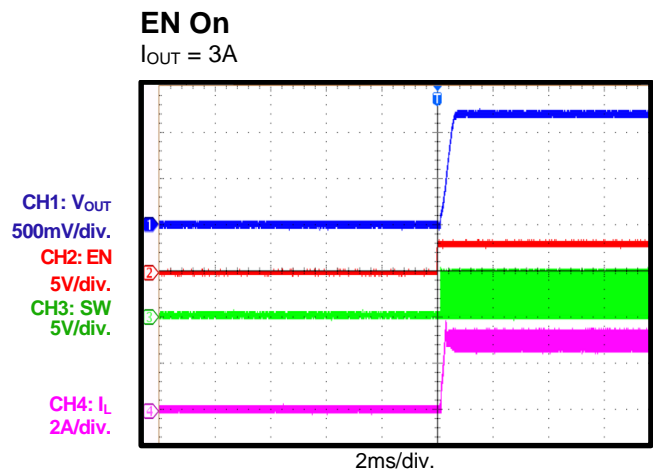
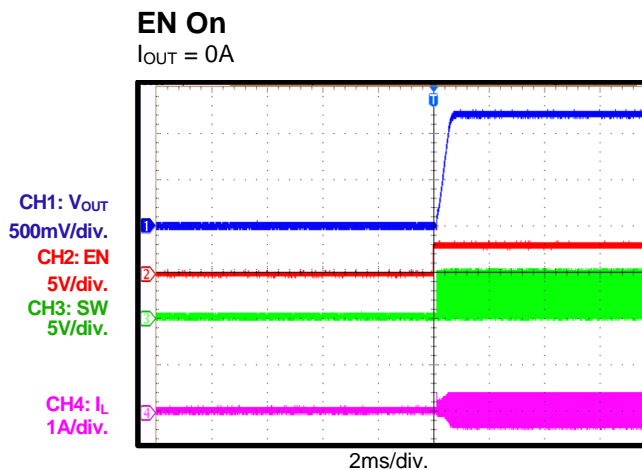
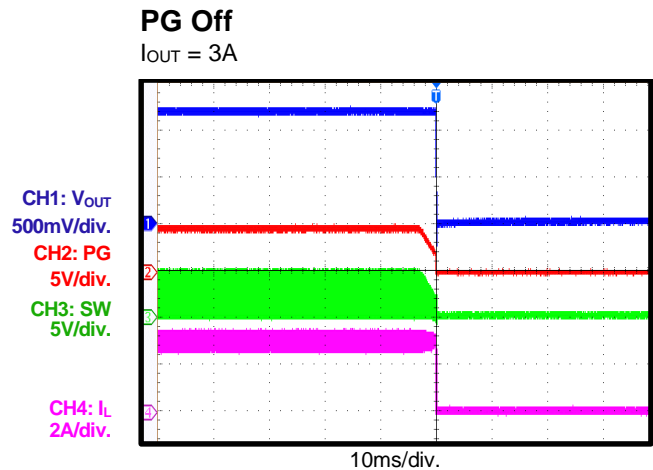
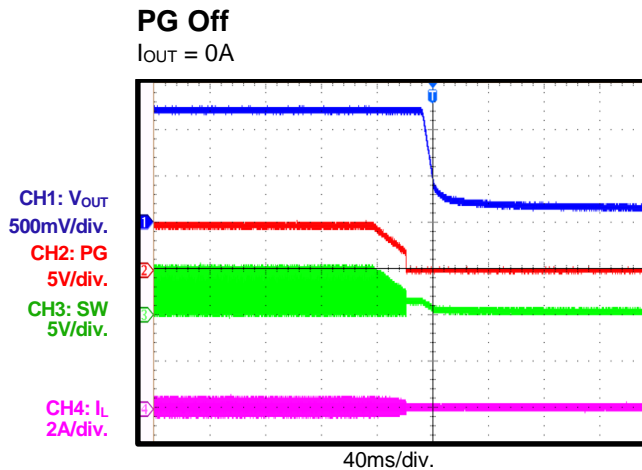
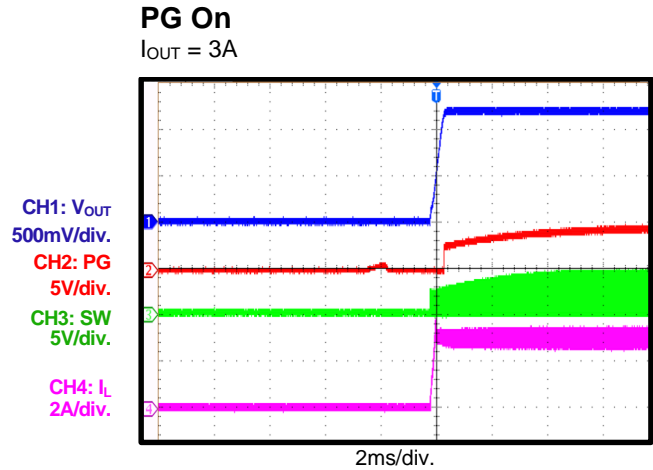
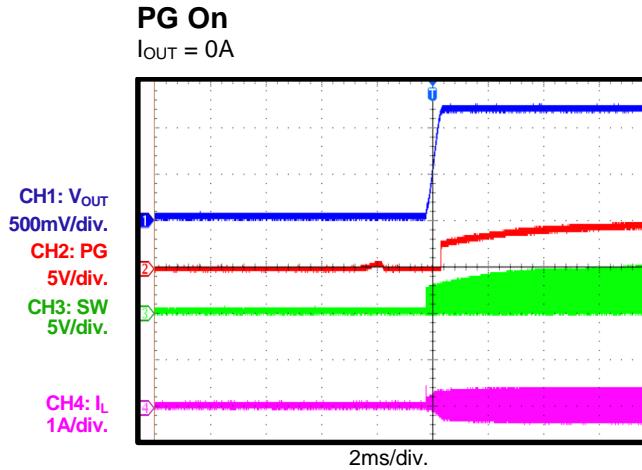
**Reference Voltage vs. Temperature**

**Peak Current Limit vs. Temperature**

 **$V_{IN}$  Rising and Falling Threshold vs. Temperature**

**EN Rising and Falling Threshold vs. Temperature**

 **$V_{IN}$  OVP Rising and Falling Threshold vs. Temperature**

 **$V_{OUT}$  OVP Rising and Falling Threshold vs. Temperature**


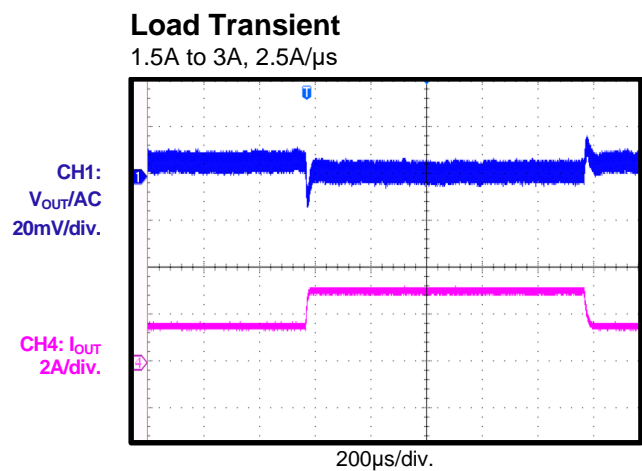
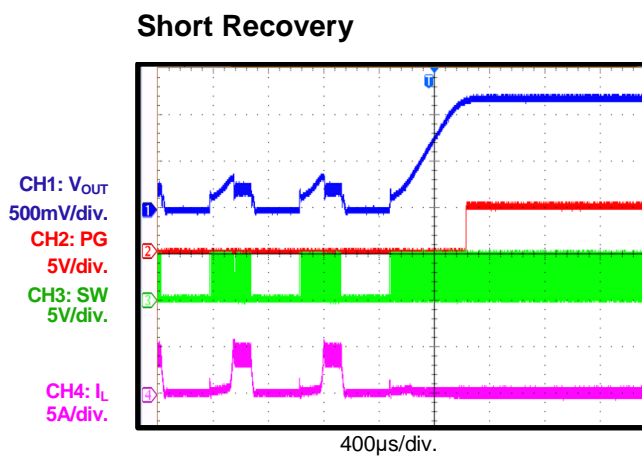
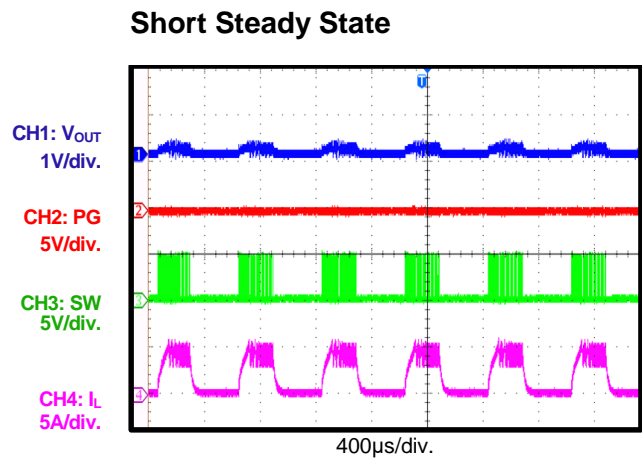
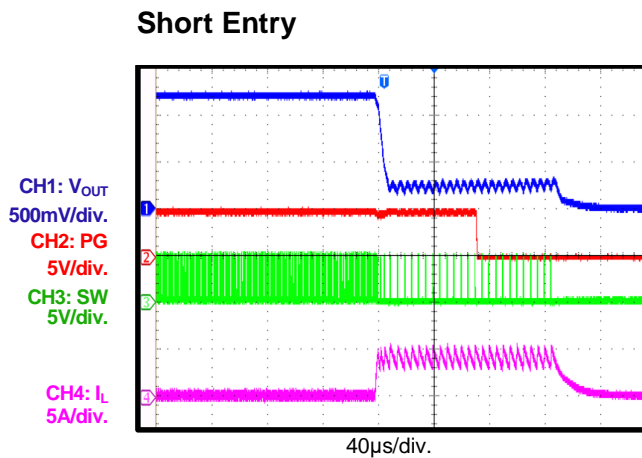
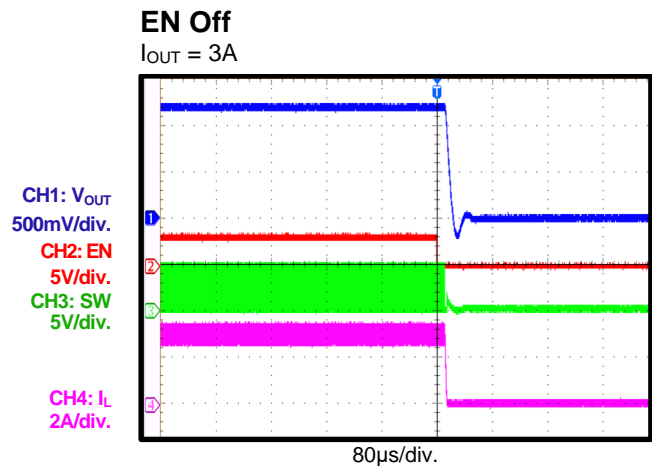
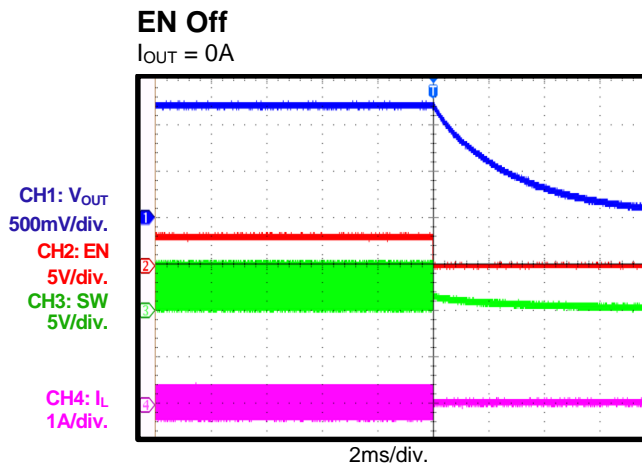
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 3.6V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C_{OUT} = 44\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Case Thermal Rising vs. Output Current**
 $V_{IN} = 5V$ 

**Soft-Start Time vs. Soft-Start Capacitance**

**Shutdown Current vs. Input Voltage**

**Peak Current Limit vs. Temperature**
 $V_{IN} = 5V$ 

**Switching Frequency vs. Temperature**

**Peak Current Limit vs. Input Voltage**


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C_{OUT} = 44\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

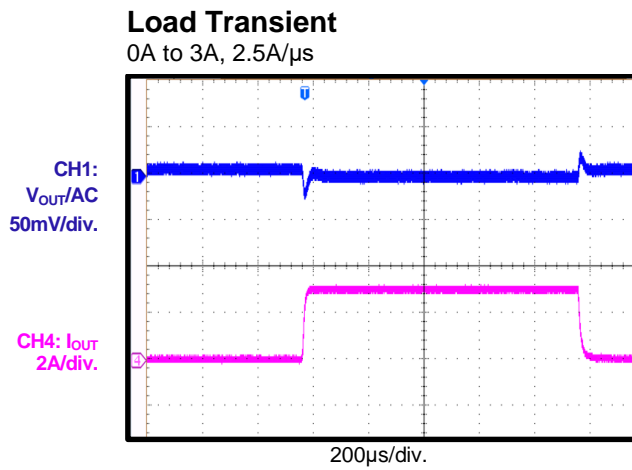
**Ripple**  
 $I_{OUT} = 0A$ 

**Ripple**  
 $I_{OUT} = 3A$ 

**VIN Start-Up**  
 $I_{OUT} = 0A$ 

**VIN Start-Up**  
 $I_{OUT} = 3A$ 

**VIN Shutdown**  
 $I_{OUT} = 0A$ 

**VIN Shutdown**  
 $I_{OUT} = 3A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C_{OUT} = 44\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
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### TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C_{OUT} = 44\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



### FUNCTIONAL BLOCK DIAGRAM

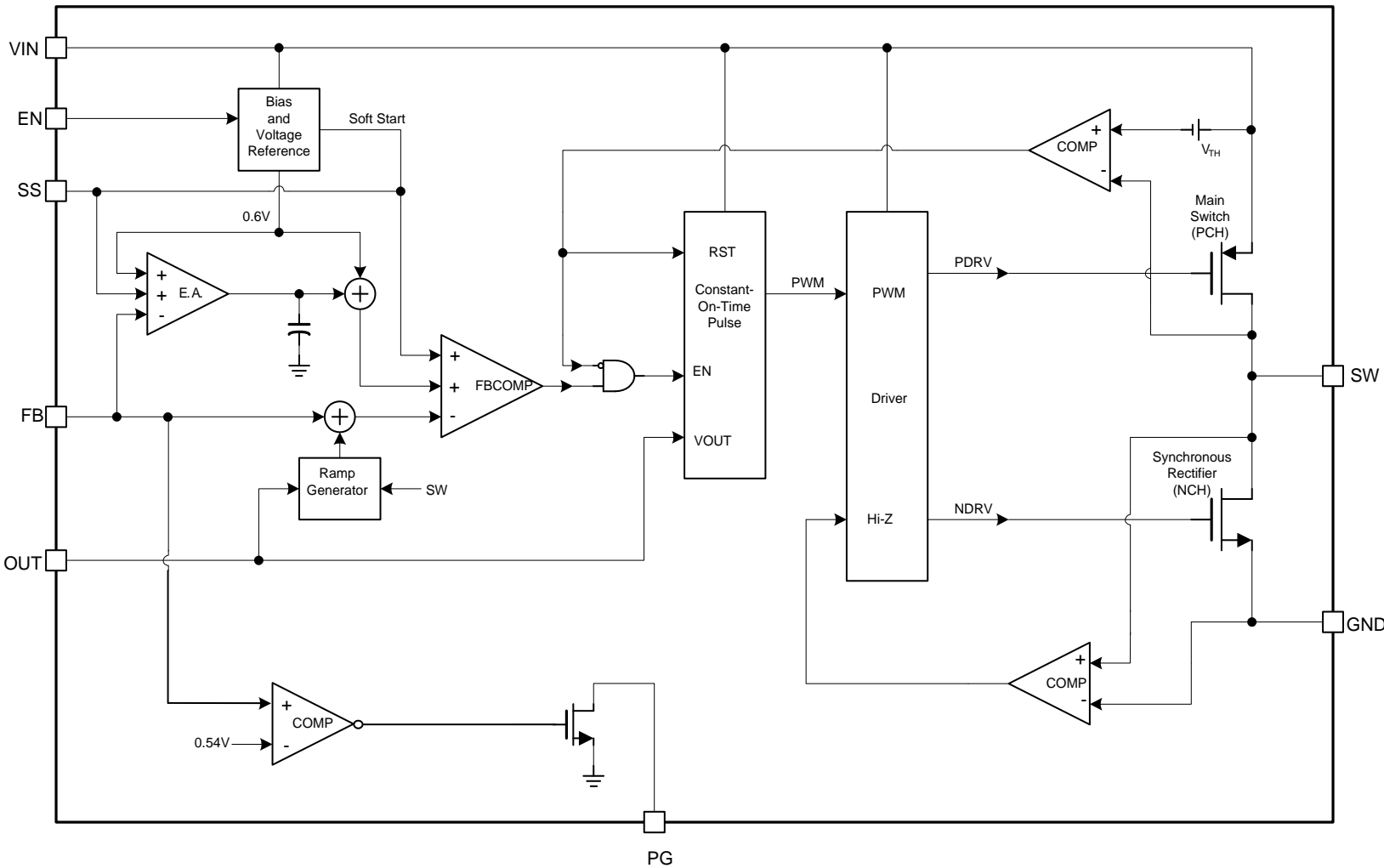


Figure 1: Functional Block Diagram

## OPERATION

The MP2183C uses constant-on-time control with input voltage feed forward to stabilize the switching frequency over the full input range. It achieves 2A of continuous output current from a 2.5V to 5.5V input voltage range, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

### Constant-On-Time (COT) Control

Compared to fixed-frequency PWM control, COT control offers a simpler control loop and a faster transient response. By using input voltage feed forward, the MP2183C maintains a nearly constant switching frequency across the input and output voltage ranges. Estimate the switching pulse on time with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.83\mu\text{s} \quad (1)$$

To prevent inductor current runaway during load transient, the MP2183C has a fixed minimum off time of 90ns.

### Enable (EN)

When the input voltage exceeds the under-voltage lockout threshold (UVLO), typically 2V, the device is enabled by pulling the EN pin above 1.2V. Leave the EN pin floating or pull it down to ground to disable the MP2183C. There is an internal 2M $\Omega$  resistor from EN to ground.

When the device is disabled, the part goes into output discharge mode automatically, and its internal discharge MOSFET provides a resistive discharge path for the output capacitor.

### Soft Start (SS)

The MP2183C has an external SS pin that ramps up the output voltage at a controlled slew rate to avoid overshoot during start-up. The SS pin charge current is about 3 $\mu$ A. The soft-start time is determined by the SS capacitor, and can be estimated with Equation (2):

$$T_{SS}(\text{ms}) = \frac{0.8 \cdot C_{SS}(\text{nF}) \cdot V_{REF}}{I_{SS}(\mu\text{A})} + 0.06 \cdot C_{SS}(\text{nF}) \quad (2)$$

Where  $t_{SS}$  is the soft-start time from 10% to 90% of  $V_{OUT}$ ,  $C_{SS}$  is the SS capacitor,  $I_{SS}$  is the SS pin's charge current (typically 3 $\mu$ A), and  $V_{REF}$  is the reference voltage (typically 0.6V).

### Current Limit

The MP2183C typically has a 5A high-side switch current limit. When the high-side switch reaches its current limit, the MP2183C remains in hiccup mode until the current drops. This prevents the inductor current from continuing to rise and damaging components.

### Short Circuit and Recovery

The MP2183C enters short-circuit protection mode when it reaches the current limit, and tries to recover with hiccup mode. The MP2183C disables the output power stage, discharges the soft-start capacitor, then automatically retries soft start. If the short-circuit condition remains after soft start ends, the MP2183C repeats this cycle until the short circuit disappears and the output returns to its regulation level.

### Over-Voltage Protection ( $V_O$ OVP)

The MP2183C monitors a resistor-divided feedback voltage to detect an over-voltage condition. When the feedback voltage ( $V_{FB}$ ) exceeds 115% of the target voltage, the controller enters a dynamic regulation period (DRP). During this period, the LS-FET is on until the LS-FET current drops to -1.5A. The output discharges to maintain the normal range.

If the over-voltage condition still exists, the LS-FET turns on again after an 800ns time delay. The part exits this regulation period when  $V_{FB}$  drops below 105% of the reference voltage. If the dynamic regulation cannot limit  $V_{OUT}$  and the input detects the 6.1V input, OVP occurs. The MP2183C stops switching and does not operate until the input voltage drops below 6V.

### Power Good Indicator

The MP2183 has an open-drain output and requires an external pull-up resistor (100k $\Omega$  to 500k $\Omega$ ) for the power good indicator. When  $V_{FB}$  exceeds 90% of the regulation voltage,  $V_{PG}$  is pulled up to  $V_{OUT}/V_{IN}$  by the external resistor. If  $V_{FB}$  exceeds this window, the internal MOSFET pulls PG to ground. The MOSFET has a maximum  $R_{DS(ON)}$  below 400 $\Omega$ . When the VIN and EN pins are not available and PG has an external power supply pulled up, the PG self-bias voltage is below 0.7V.

## APPLICATION INFORMATION

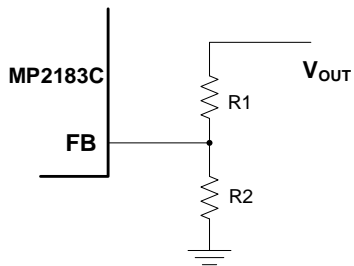
### COMPONENT SELECTION

#### Setting the Output Voltage

The external resistor divider sets the output voltage (see the Functional Block Diagram on page 13). Select a feedback resistor (R1) that reduces the  $V_{OUT}$  leakage current, typically between 100k $\Omega$  and 200k $\Omega$ . There is no strict requirement on the feedback resistor. Ensure that R1 is greater than 10k $\Omega$ . Calculate R2 with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (3)$$

Figure 2 shows the feedback circuit.



**Figure 2: Feedback Network**

Table 1 lists the recommended resistor values for common output voltages.

**Table 1: Resistor Values for Common Output Voltages**

$V_{OUT}$ (V)	R1 (k $\Omega$ )	R2 (k $\Omega$ )
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

#### Selecting the Inductor

Most applications work best with a 0.47 $\mu$ H to 4.7 $\mu$ H inductor. Select an inductor with a DC resistance below 25m $\Omega$  to optimize efficiency.

A high-frequency, switch-mode power supply with a magnetic device has strong electromagnetic interference (EMI). Any unshielded power inductors should be avoided. Metal alloy or multilayer chip power inductors are ideal shielded inductors since they can

decrease the influence effectively. Table 2 lists the recommended inductor.

**Table 2: Recommended Inductor List**

Manufacturer P/N	Inductance ( $\mu$ H)	Manufacturer
74437324010	1.0	Würth
MPL-AL4020-1R0	1.0	MPS

For most designs, the inductance value can be calculated with Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (4)$$

Where  $\Delta I_L$  is the inductor ripple current.

Choose an inductor current that is about 30% of the maximum load current. The maximum inductor peak current can be estimated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

#### Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22 $\mu$ F capacitor is sufficient. Higher output voltages may require a 44 $\mu$ F capacitor to improve system stability.

The input capacitor requires an adequate ripple current rating because it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case occurs when  $V_{IN} = 2V_{OUT}$ , calculated with Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic 0.1µF capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

### Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Ceramic capacitors are recommended. Low-ESR capacitors are recommended to limit the output voltage ripple. The output voltage ripple can be calculated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right) \quad (9)$$

Where  $L_1$  is the inductor value, and  $R_{ESR}$  is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (11):

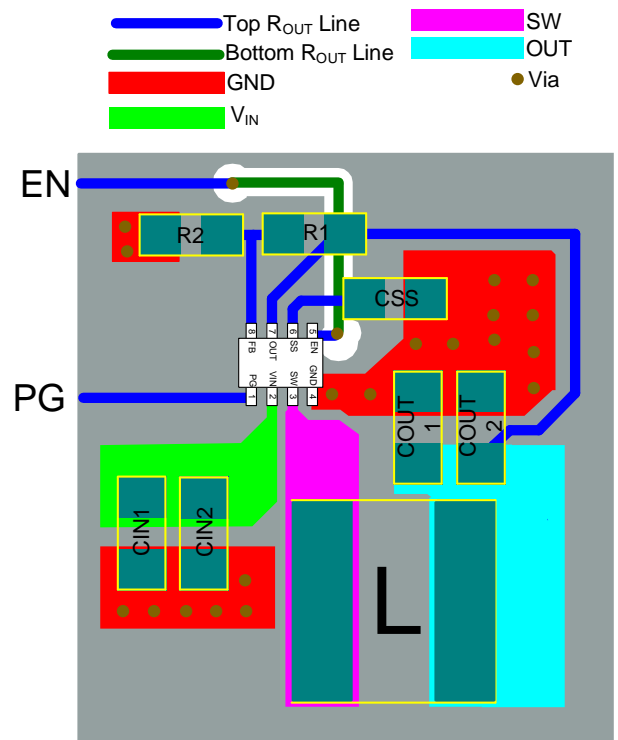
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

### PCB Layout Guidelines

Proper layout of the switching power supplies is very important for proper function. Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 3 and follow the guidelines below:

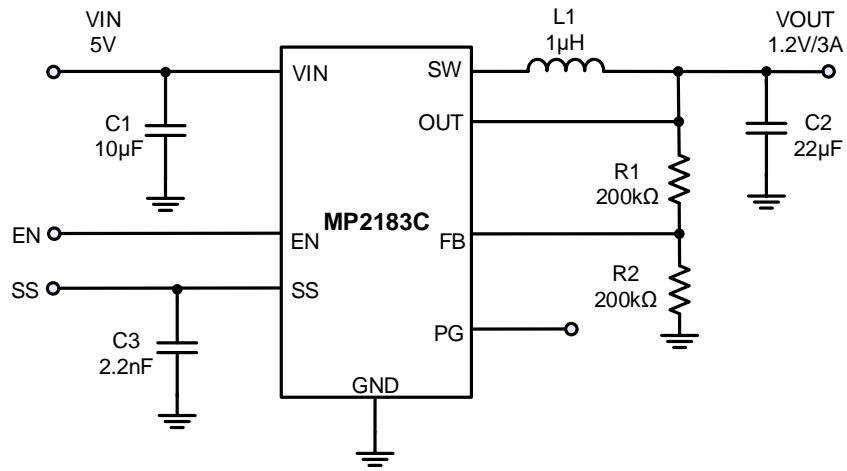
1. Place the high-current paths (GND, IN, and SW) as close as possible to the device with short, direct, and wide traces.
2. Place the input capacitor as close as possible to the IN and GND pins.
3. Place GND's output capacitor as close as possible to the GND pins.
4. Place the external feedback resistors next to the FB pin.
5. Keep SW short and route it away from the feedback network.
6. Keep the  $V_{OUT}$  sense line as short as possible, and route it away from the power inductor and surrounding inductors.



**Figure 3: Recommended PCB Layout**

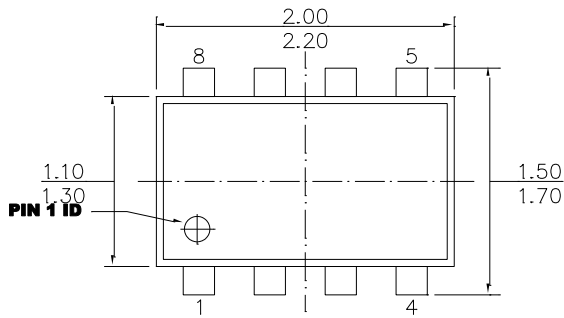
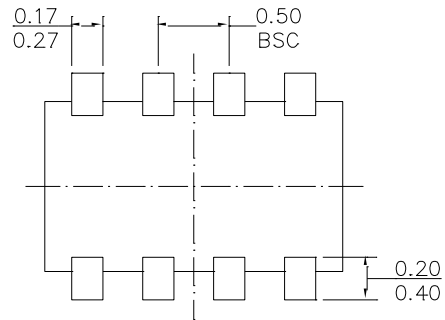
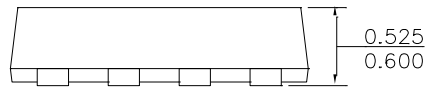
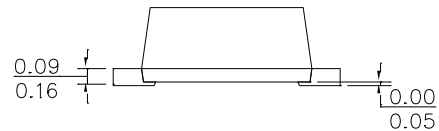
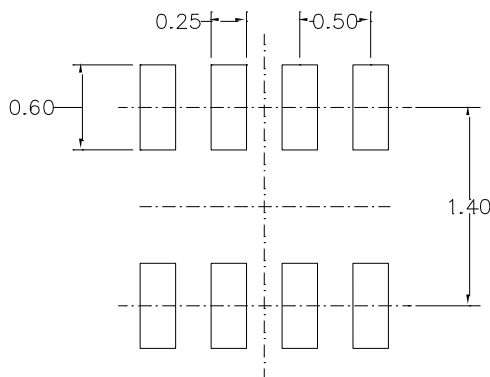


### TYPICAL APPLICATION CIRCUIT



**Figure 4: Typical Application Circuit for the MP2183C**

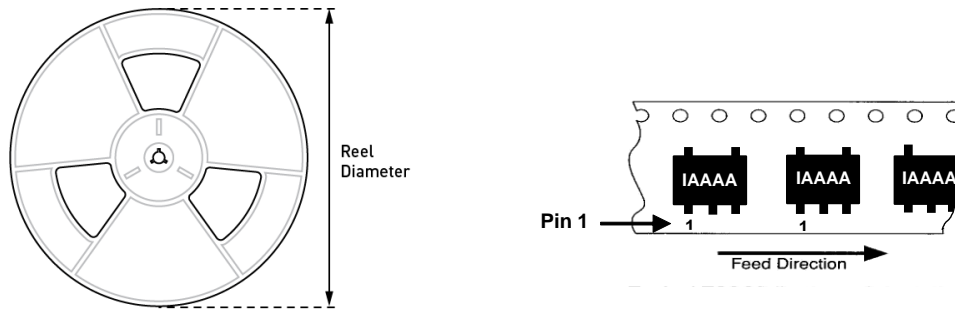
**Note:** If  $V_{IN} < 3.3V$ , it is recommended to use more input capacitors.

**PACKAGE INFORMATION**
**SOT583**

**TOP VIEW**

**BOTTOM VIEW**

**FRONT VIEW**

**SIDE VIEW**

**RECOMMENDED LAND PATTERN**
**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 4) DRAWING IS NOT TO SCALE.

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## CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2183C-GTL-Z	SOT583	5000	N/A	7 in.	8mm	4mm

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