MP2164

2.5 - 5.5V, 3A, 2.3MHz, High Efficiency, Synchronous Step-Down Converter with MODE Pin in Small 2x2mm QFN Package

DESCRIPTION

The MP2164 is a monolithic, step-down, switch-mode converter with built-in, internal power MOSFETs that can achieve 3A of continuous output current from a 2.5V to 5.5V input voltage rangewith excellent load and line regulation. The output voltage can be regulated as low as 0.6V. The MP2164 is ideal for powering portable equipment that run on a single-cell Lithium-ion (Li+) battery.

The constant-on-time (COT) control scheme provides fast transient response, high light-load efficiency, and easy loop stabilization.

Full protection features include output over-voltage protection (OVP), cycle-by-cycle current limiting, and thermal shutdown.

The MP2164 is available in a QFN-12 (2mmx2mm) package.

FEATURES

- More than 80% Light-Load Efficiency
- Forced PWM and Auto PFM Option
- Wide 2.5V to 5.5V Operating Input Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- 3A Output Current
- 32mΩ and 20mΩ Internal Power MOSFET
- 2.3MHz Frequency
- Internal Soft Start (SS)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Thermal Shutdown
- Stable with Low ESR Output Ceramic Capacitors
- Available in a QFN-12 (2mmx2mm) Package

APPLICATIONS

- Wireless Cards
- Smartphones
- Low-Voltage I/O System Power

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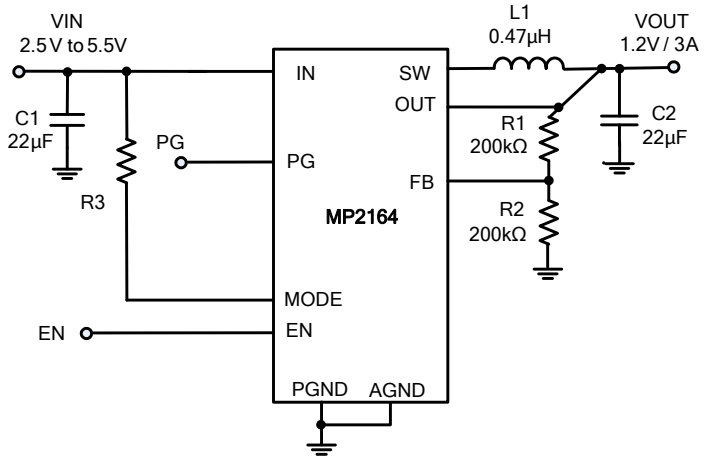
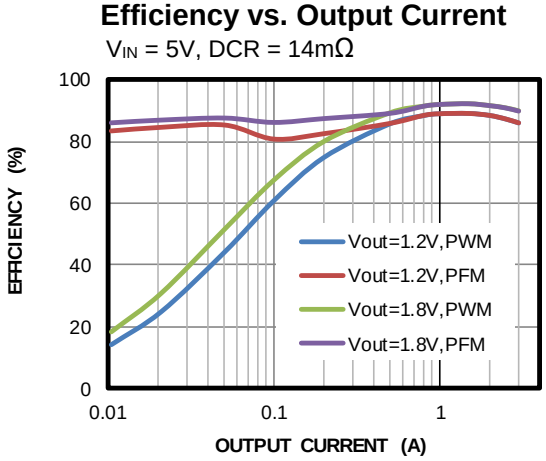
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2164GG	QFN-12 (2mmx2mm)	*See Below*

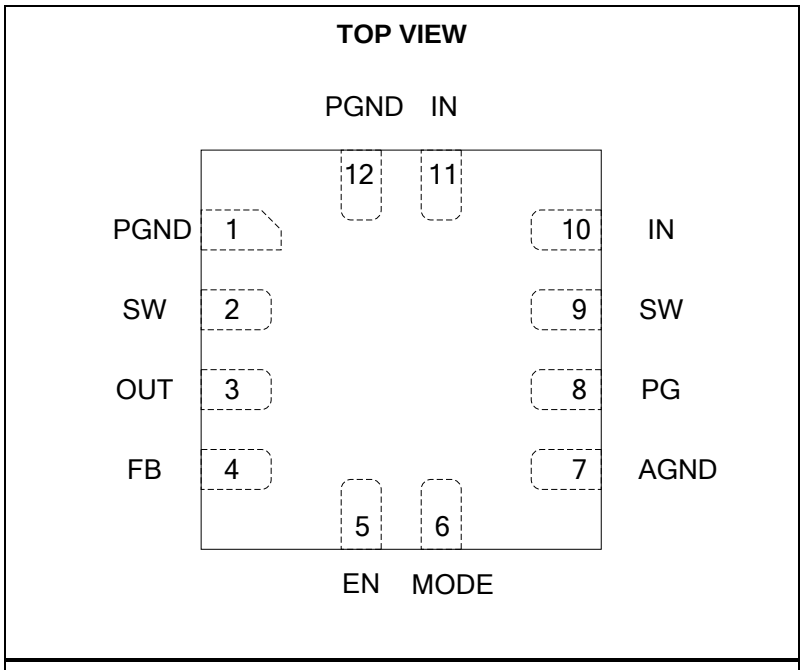
* For Tape & Reel, add suffix –Z (e.g.: MP2164GG–Z).

TOP MARKING

DGY
LLL

DG: Product code of MP2164GG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-12 (2mmx2mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} ..... -0.3V (-4V for <10ns) to 6.5V (8V for <10ns)
All other pins ..... -0.3V to 6.5V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = +25°C) (2)(4) 2.7W
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.5V to 5.5V
Output voltage (V_{OUT}) ... 0.6V (>15% x V_{IN}) to V_{IN}
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
EV2164-G-00A (4)	45	10	°C/W
QFN-12 (2mmx2mm)	80	16	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV2164-G-00A, 2-layer PCB.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C [6], typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Internal feedback voltage	V_{FB}	2.5V ≤ V_{IN} ≤ 5.5V, T_J = +25°C	594	600	606	mV
		2.5V ≤ V_{IN} ≤ 5.5V	591	600	609	mV
Switch leakage current	LSW	V_{EN} = 0V, V_{IN} = 5.5V, V_{SW} = 5.5V, T_J = +25°C		0	1	μA
Minimum on time [7]	T_{MIN-On}			60		ns
Minimum off time [7]	$T_{MIN-OFF}$			100		ns
EN turn on delay	$T_{Delay-ON}$	EN on to SW active		400		μs
Soft-start time		V_{OUT} rises from 10% to 90%		1.2		ms
Power Good (PG)						
PG UV threshold rising	PGUVTH_Hi		85%	90%	95%	VFB
PG UV threshold hysteresis	PGUVTH_Lo			5%		VFB
PG OV threshold rising	PGOVTH_Hi		110%	115%	120%	VFB
Power good hysteresis	PGOVTH_Lo			5%		VFB
Power good deglitch time		Rising		100		μs
Power good sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
Power good logic high voltage	V_{PG_HI}	V_{IN} = 5V	4.9			V
Module Parameters						
Under-voltage lockout threshold rising			2.15	2.3	2.45	V
Under-voltage lockout threshold hysteresis				240		mV
EN wake-up voltage				0.7	0.95	V
EN input logic high voltage			1.15	1.19	1.23	V
EN hysteresis				120		mV
EN input current		V_{EN} = 3V		3		μA
		V_{EN} = 0V		0		μA
Supply current (shutdown)		V_{EN} = 0V, T_J = +25°C		0	1	μA
Supply current (quiescent)		V_{EN} = 2V, V_{IN} = 3.6V, no switching, T_J = +25°C		50	60	μA
P-FET peak current limit		T_J = +25°C	4.4	5		A
P-FET switch on resistance	R_{DSON_P}	V_{IN} = 5V		32		mΩ
N-FET switch on resistance	R_{DSON_N}	V_{IN} = 5V		20		mΩ
Output discharge resistance	RDISR	VEN = 0		45		Ω
Switching frequency	f_s	V_{OUT} = 1.2V		2300		kHz
Thermal shutdown [7]				150		°C
Thermal hysteresis [7]				30		°C

NOTES:

6) Guaranteed by over-temperature correlation, not tested in production.

7) Guaranteed by sample characterization, not production tested.

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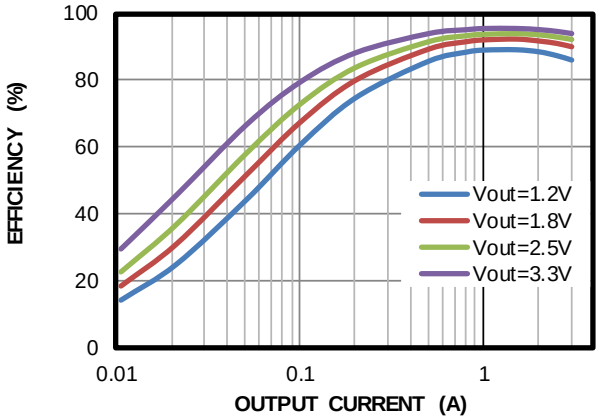
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 0.47µH, Co = 22µF, T_A = +25°C, unless otherwise noted.

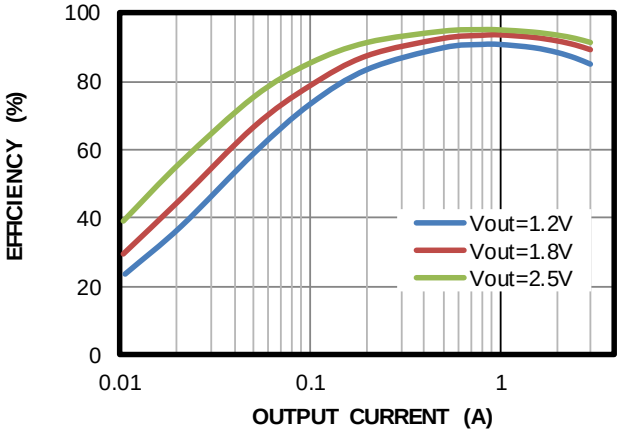
Efficiency vs. Output Current

V_{IN} = 5V, DCR = 14mΩ, PWM



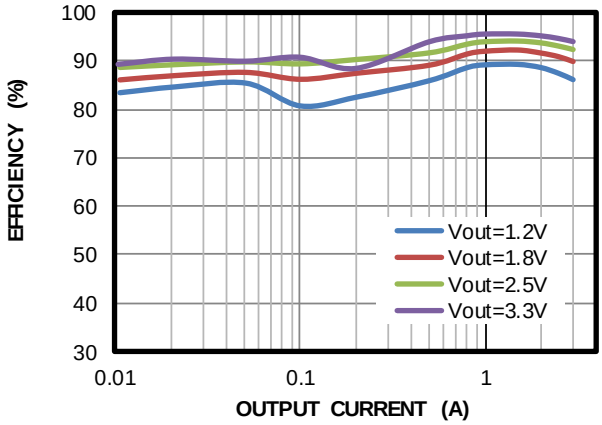
Efficiency vs. Output Current

V_{IN} = 3.6V, DCR = 14mΩ, PWM



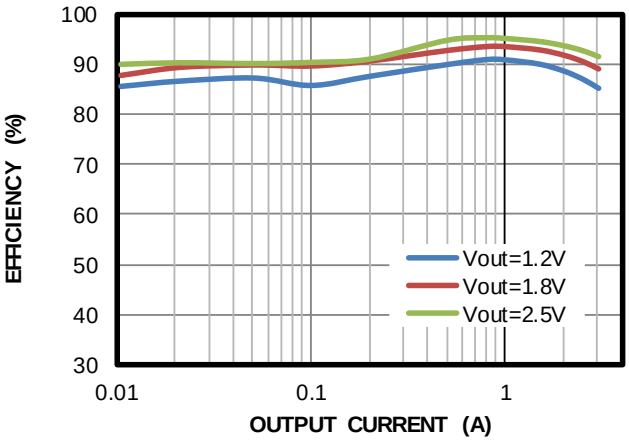
Efficiency vs. Output Current

V_{IN} = 5V, DCR = 14mΩ, PFM



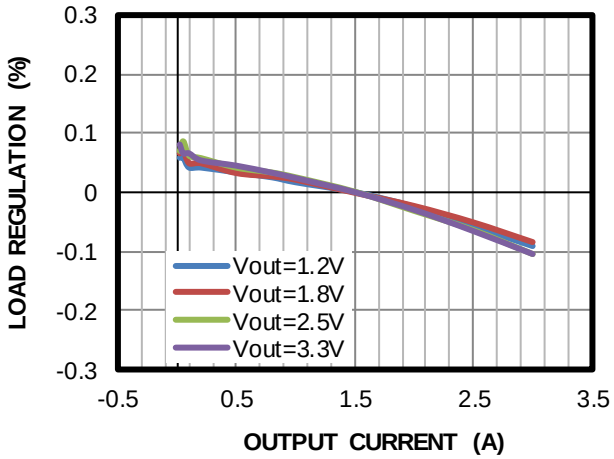
Efficiency vs. Output Current

V_{IN} = 3.6V, DCR = 14mΩ, PFM



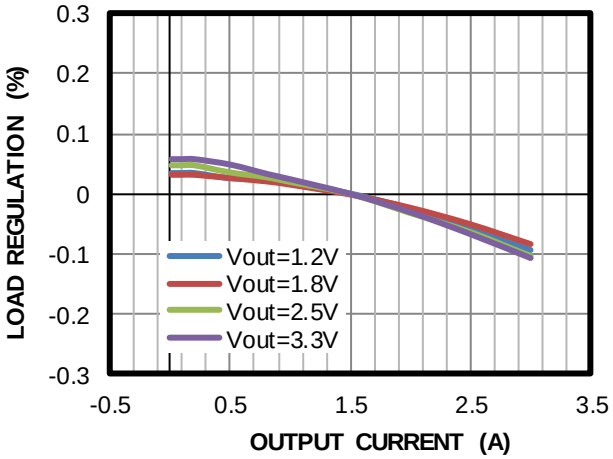
Load Regulation vs. Output Current

V_{IN} = 5V, PFM



Load Regulation vs. Output Current

V_{IN} = 5V, PWM



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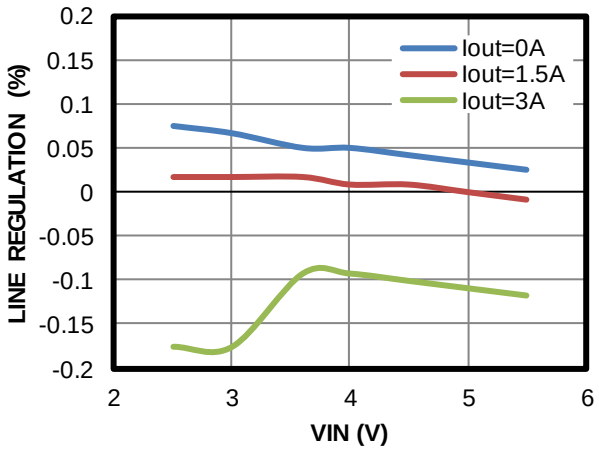
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

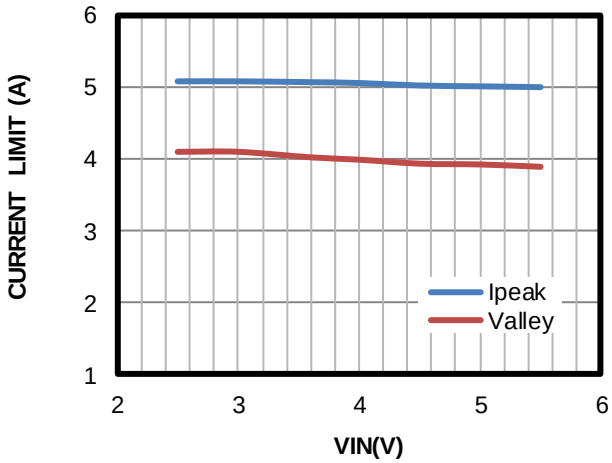
V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 0.47µH, Co = 22µF, T_A = +25°C, unless otherwise noted.

Line Regulation vs. V_{IN}

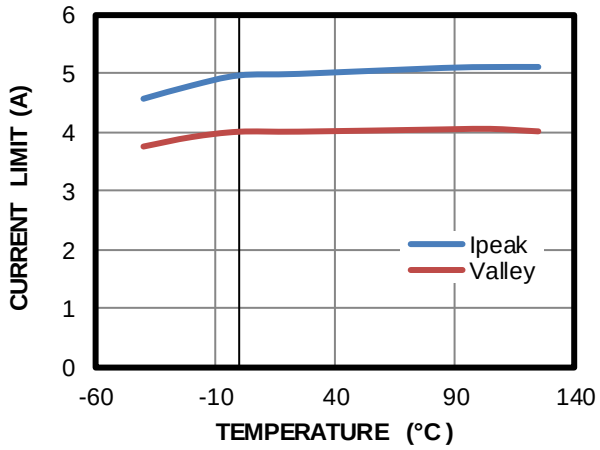
PWM



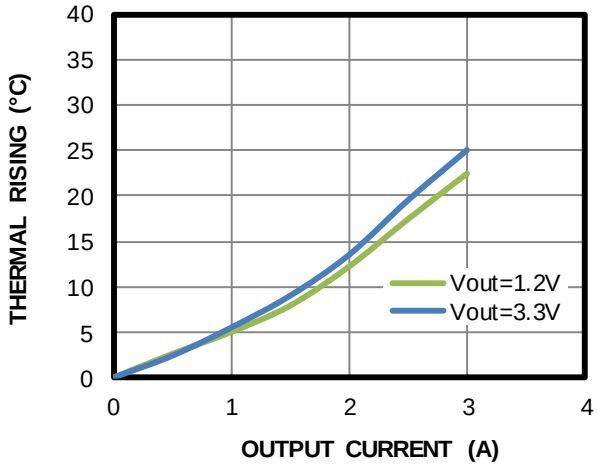
Current Limit vs. V_{IN}



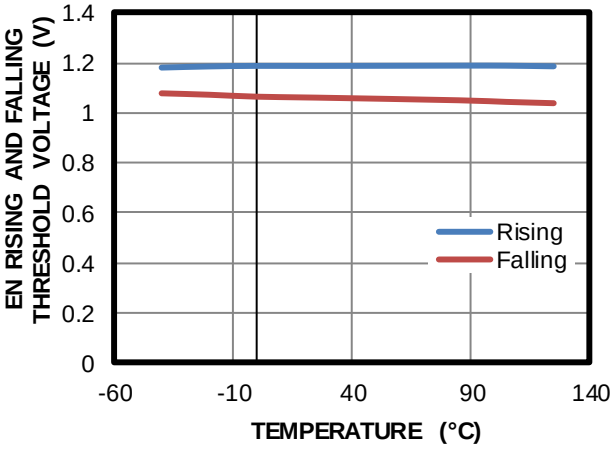
Current Limit vs. Temperature



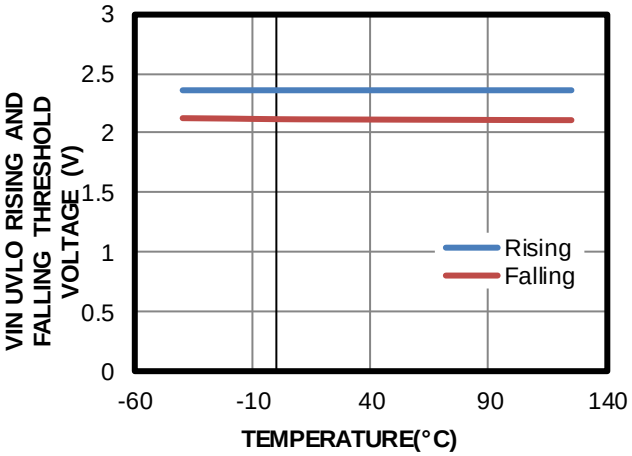
Thermal Rising vs. Output Current



EN Rising and Falling Threshold vs. Temperature



V_{IN} UVLO Rising and Falling Threshold vs. Temperature



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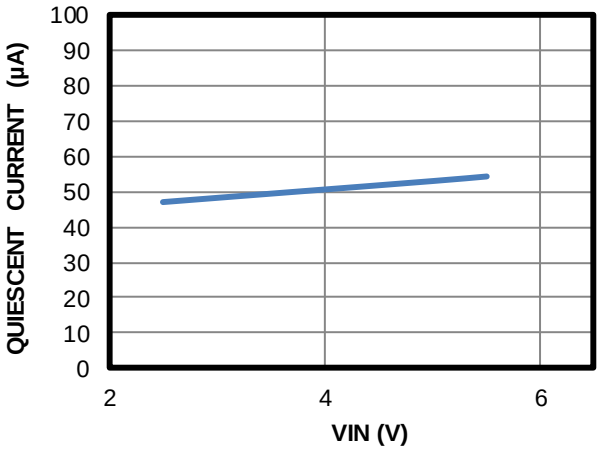
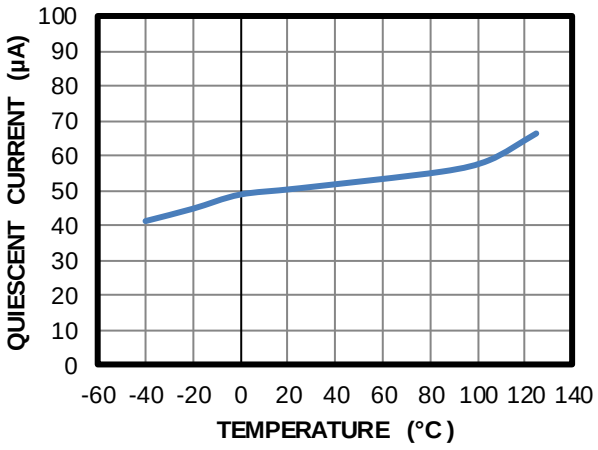
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 0.47µH, Co = 22µF, T_A = +25°C, unless otherwise noted.

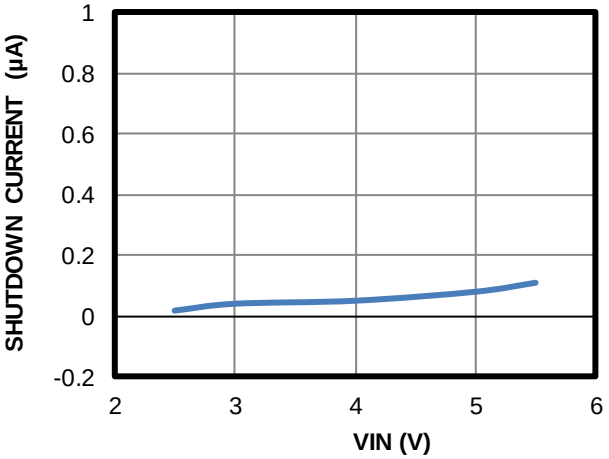
Quiescent Current vs. V_{IN}



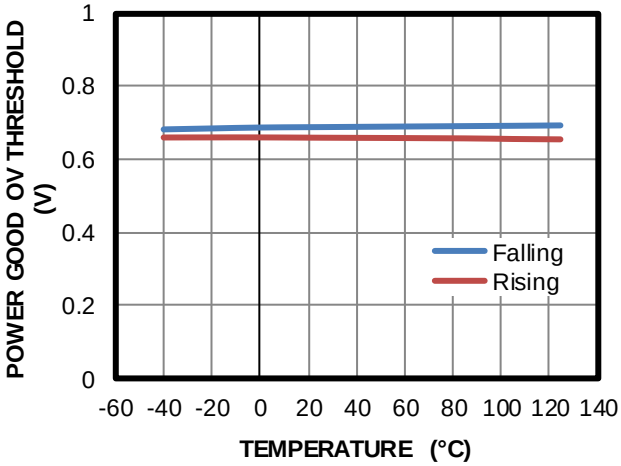
Quiescent Current vs. Temperature



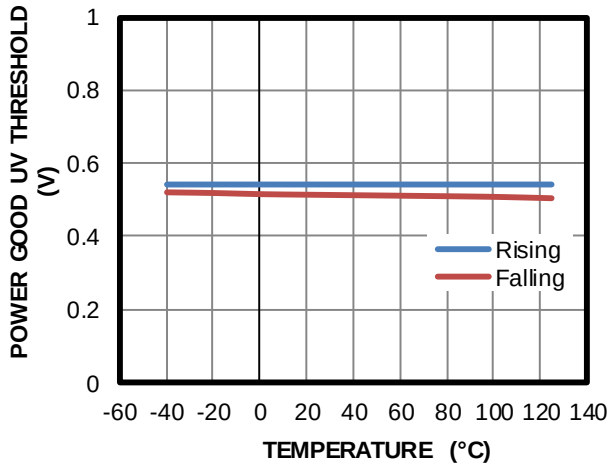
Shutdown Current vs. V_{IN}



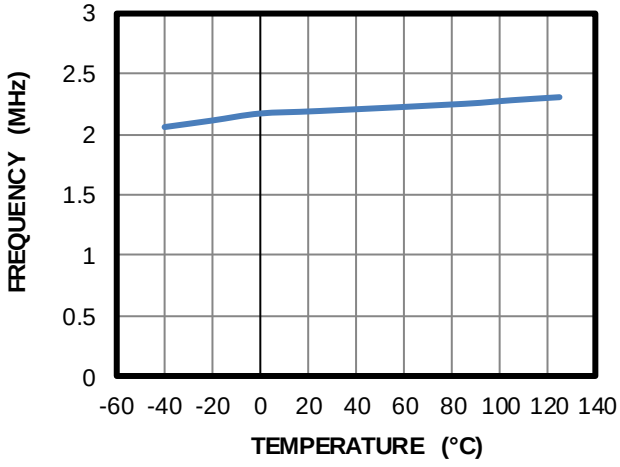
Power Good OV Threshold vs. Temperature



Power Good UV Threshold vs. Temperature



Frequency vs. Temperature



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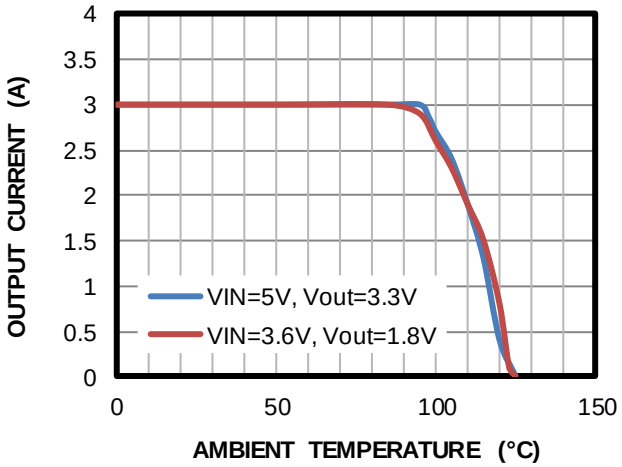
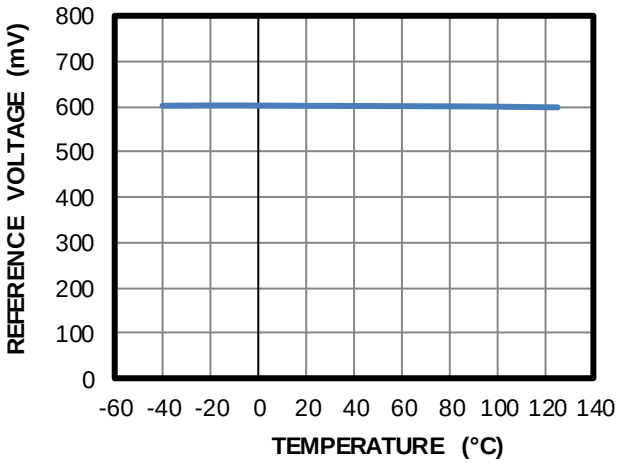
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 0.47µH, Co = 22µF, T_A = +25°C, unless otherwise noted.

Output Current vs. Ambient Temperature



Reference vs. Temperature



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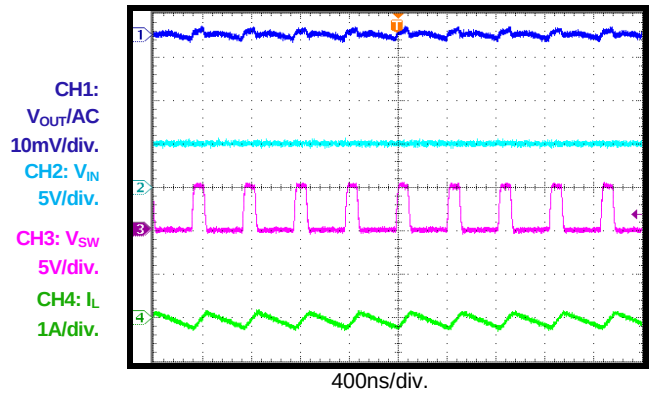
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, Co = 22µF, T_A = +25°C, unless otherwise noted.

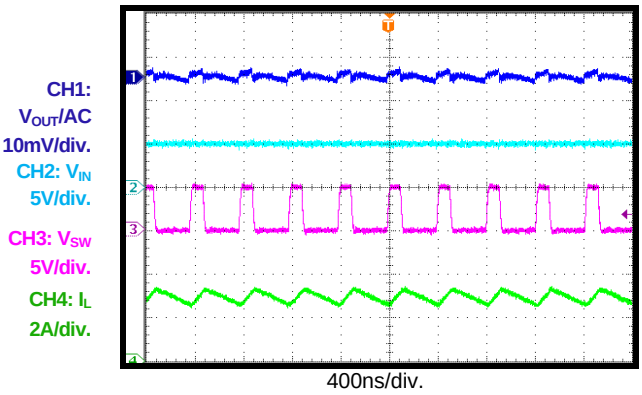
Steady State

I_{OUT} = 0A, PWM



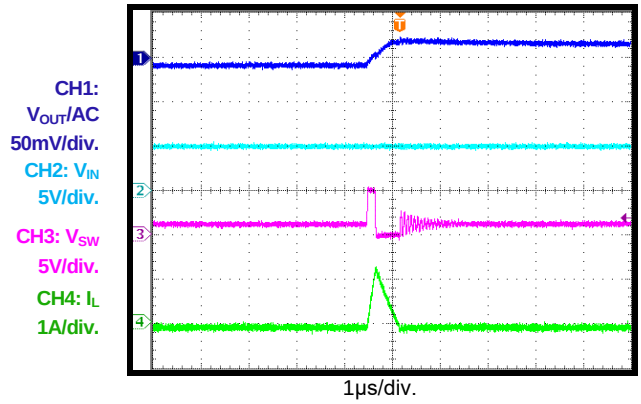
Steady State

I_{OUT} = 3A, PWM



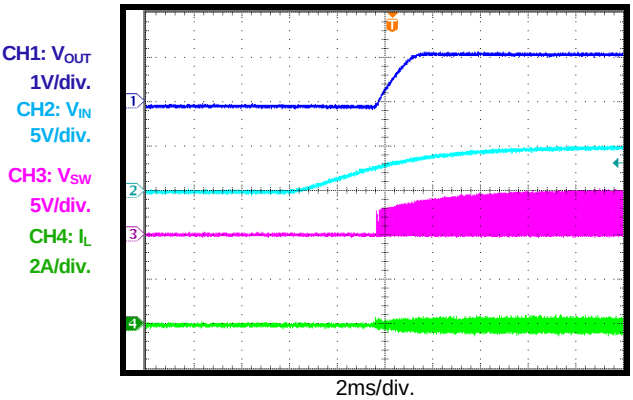
Steady State

I_{OUT} = 0A, PFM



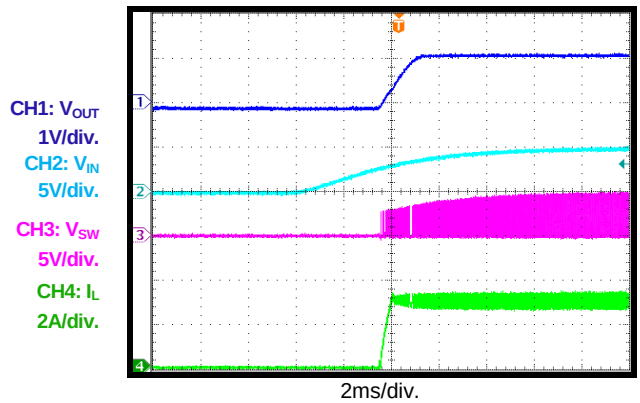
V_{IN} Power-Up

I_{OUT} = 0A, PWM



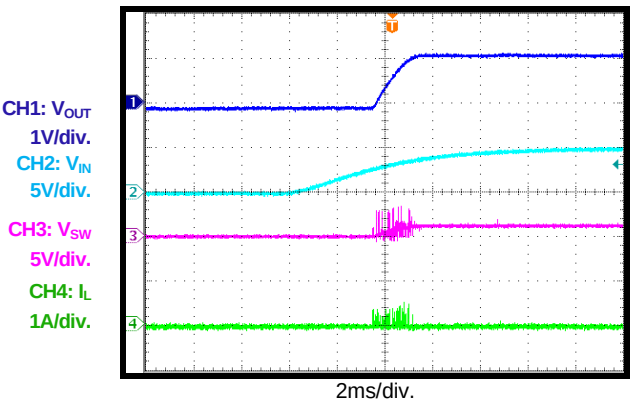
V_{IN} Power-Up

I_{OUT} = 3A, PWM



V_{IN} Power-Up

I_{OUT} = 0A, PFM



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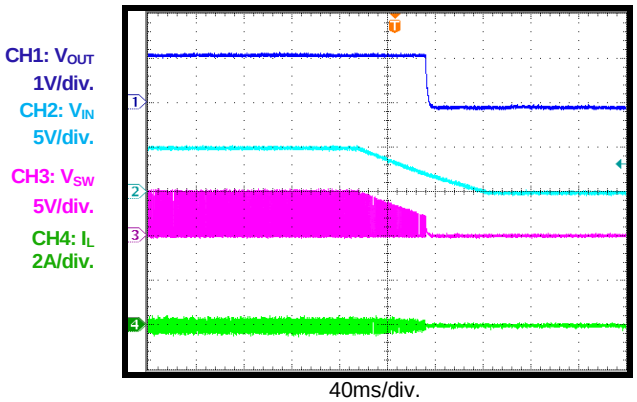
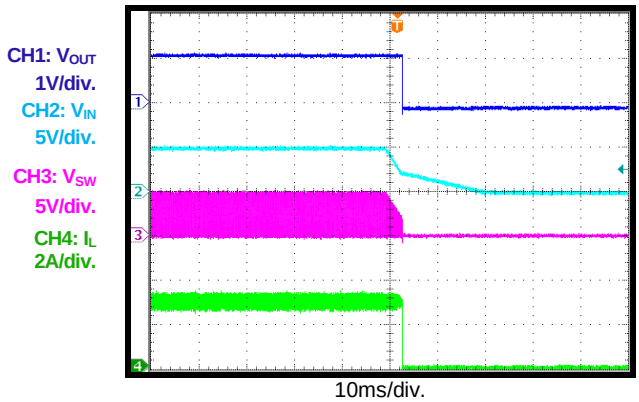
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, Co = 22µF, T_A = +25°C, unless otherwise noted.

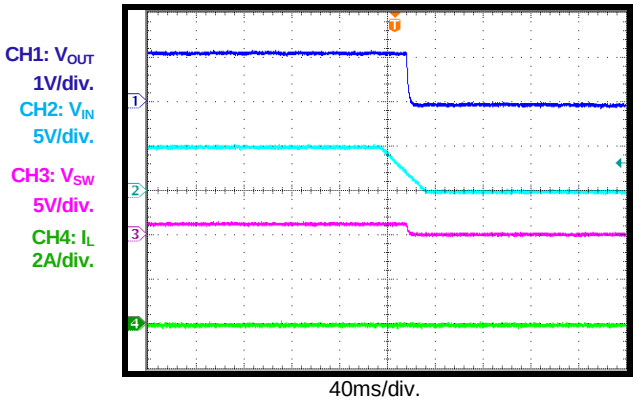
V_{IN} Shutdown
I_{OUT} = 0A, PWM



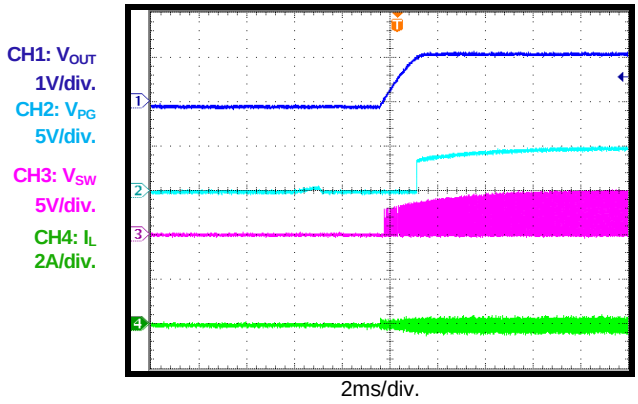
V_{IN} Shutdown
I_{OUT} = 3A, PWM



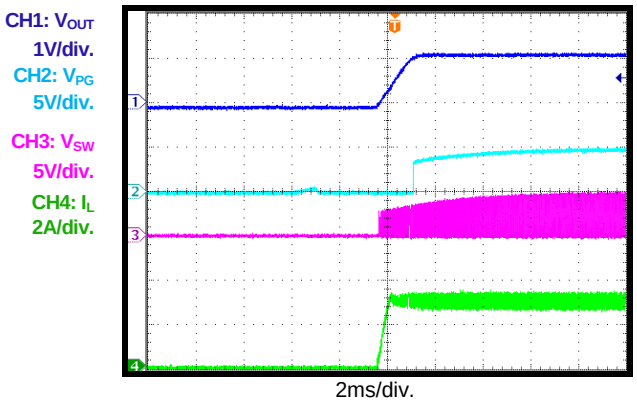
V_{IN} Shutdown
I_{OUT} = 0A, PFM



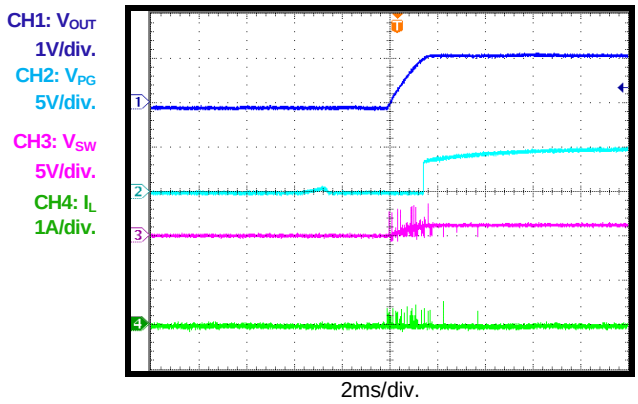
PG On
I_{OUT} = 0A, PWM



PG On
I_{OUT} = 3A, PWM



PG On
I_{OUT} = 0A, PFM



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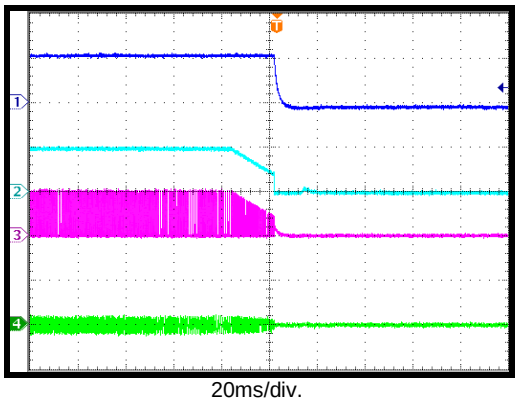
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, Co = 22µF, T_A = +25°C, unless otherwise noted.

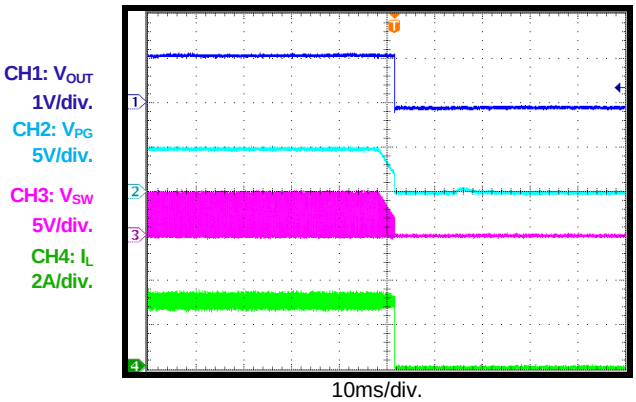
PG Off

I_{OUT} = 0A, PWM



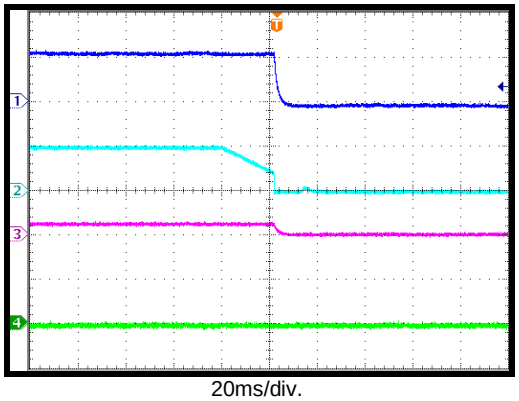
PG Off

I_{OUT} = 3A, PWM



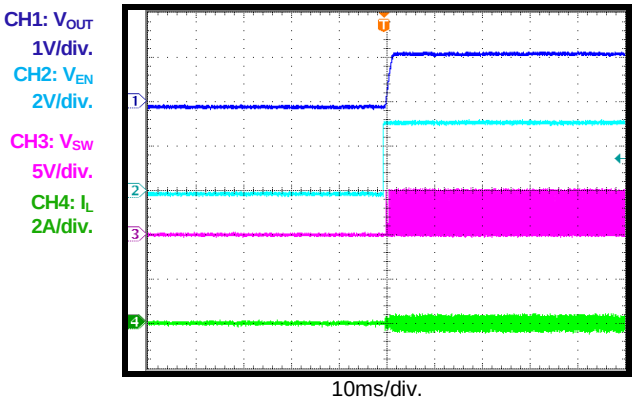
PG Off

I_{OUT} = 0A, PFM



EN On

I_{OUT} = 0A, PWM



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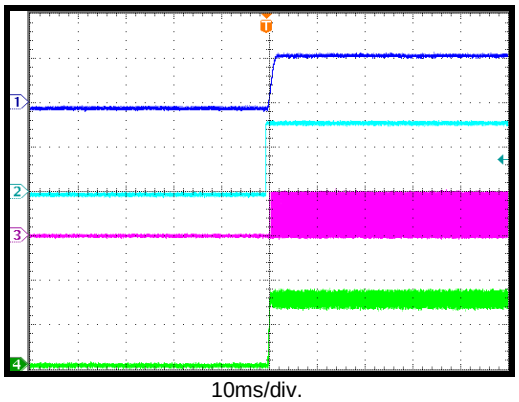
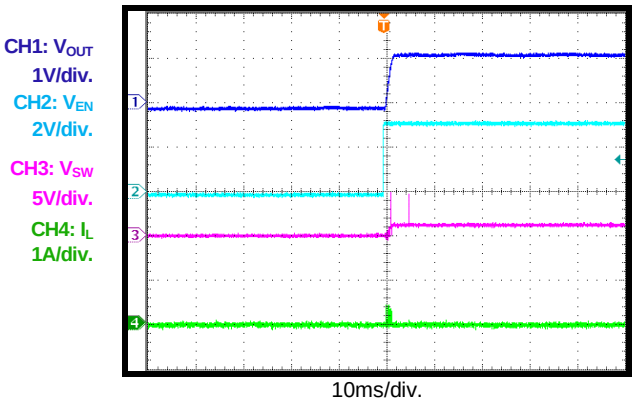
I_{OUT} = 3A, PWM



EN On

I_{OUT} = 0A, PFM



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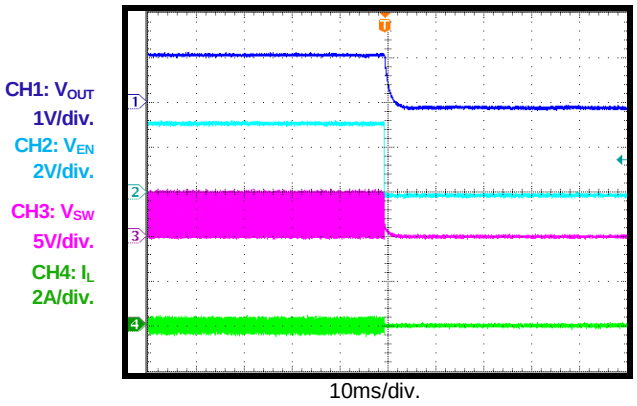
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, Co = 22µF, T_A = +25°C, unless otherwise noted.

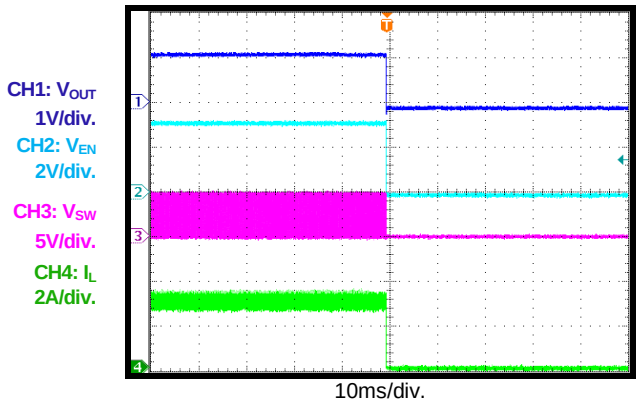
EN Off

I_{OUT} = 0A, PWM



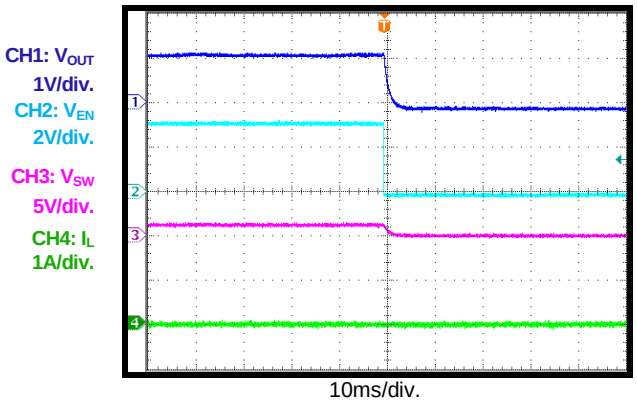
EN Off

I_{OUT} = 3A, PWM



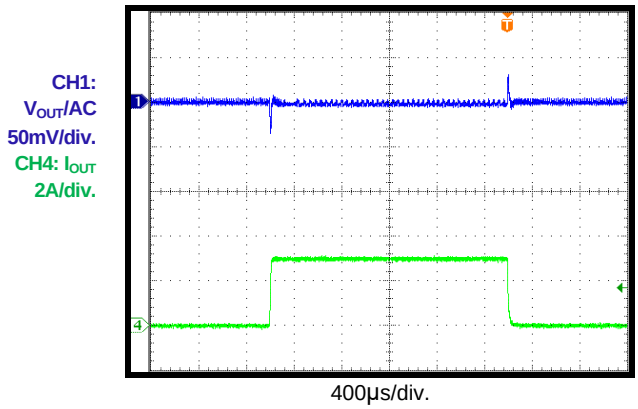
EN Off

I_{OUT} = 0A, PFM



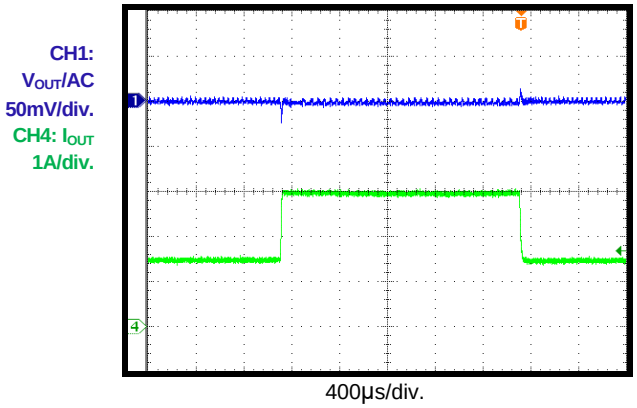
Load Transient

I_{OUT} = 0 - 3A, 2.5A/µs, PWM



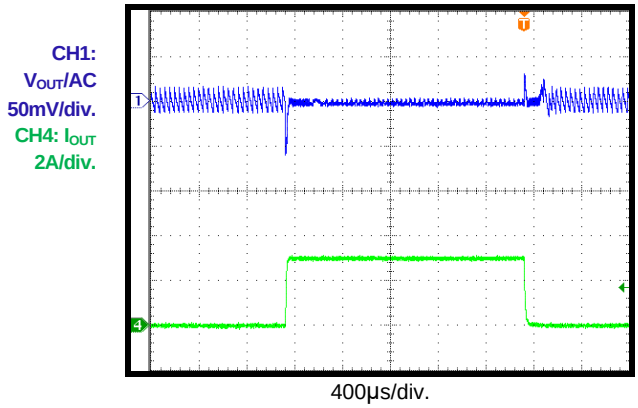
Load Transient

I_{OUT} = 1.5 - 3A, 2.5A/µs, PWM



Load Transient

I_{OUT} = 0 - 3A, 2.5A/µs, PFM



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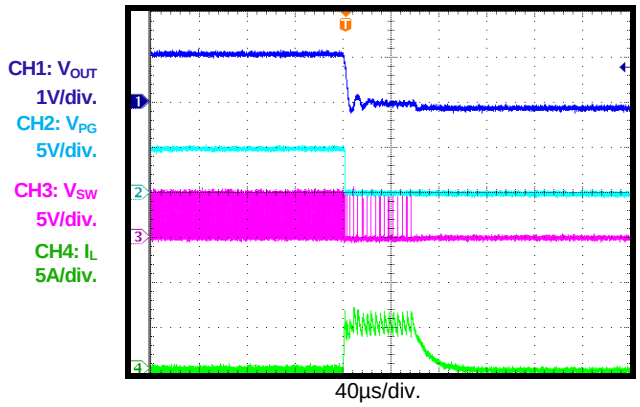
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

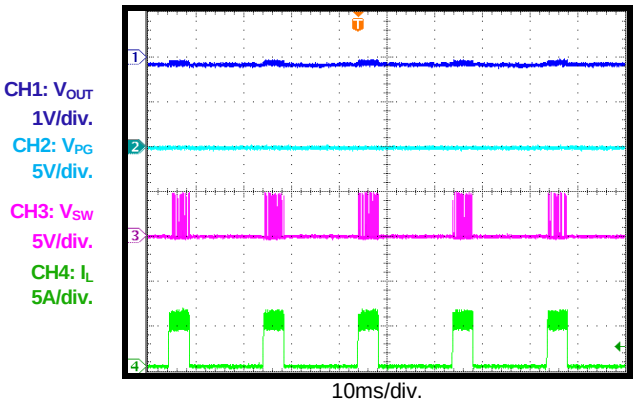
V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, Co = 22µF, T_A = +25°C, unless otherwise noted.

Short-Circuit Entry
PWM



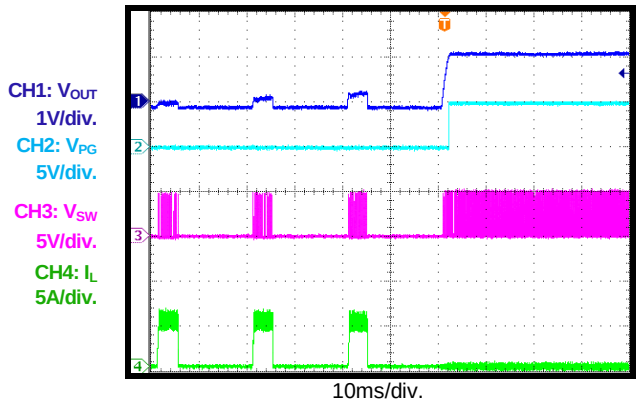
40µs/div.

Short-Circuit Steady State



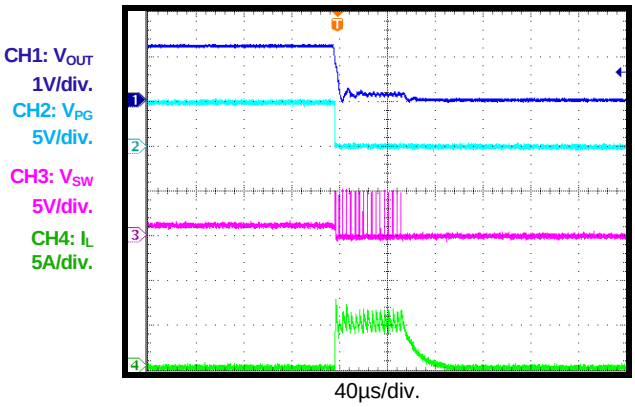
10ms/div.

Short-Circuit Recovery
PWM



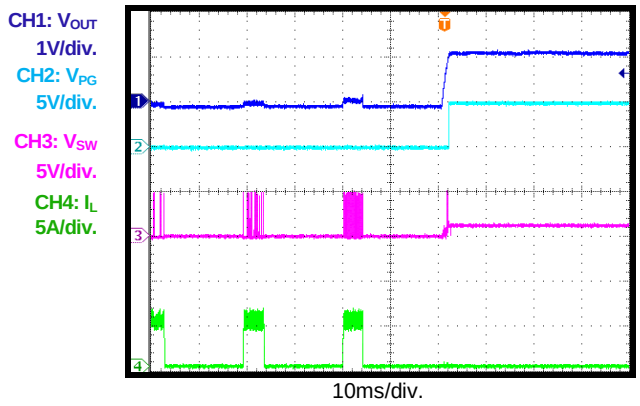
10ms/div.

Short-Circuit Entry
PFM



40µs/div.

Short-Circuit Recovery
PFM



10ms/div.

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PIN FUNCTIONS

Pin #	Name	Description
1, 12	PGND	**Power ground.** Both PGND pins (pin 1, 12) can be connected together.
2, 9	SW	**Switch output.**
3	OUT	**Power output sense pin.**
4	FB	**Feedback.** Connect an external resistor divider from the output to GND tapped to FB to set the output voltage.
5	EN	**On/off control.**
6	MODE	**Mode.** When the MODE voltage is high, the IC works in forced PWM mode. When the MODE voltage is low, the IC works in auto-PFM mode.
7	AGND	**Quiet ground for the controller circuits.**
8	PG	**Power good indicator.** The output of PG is an open-drain structure.
10, 11	IN	**Supply voltage to the internal control circuitry.**

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BLOCK DIAGRAM

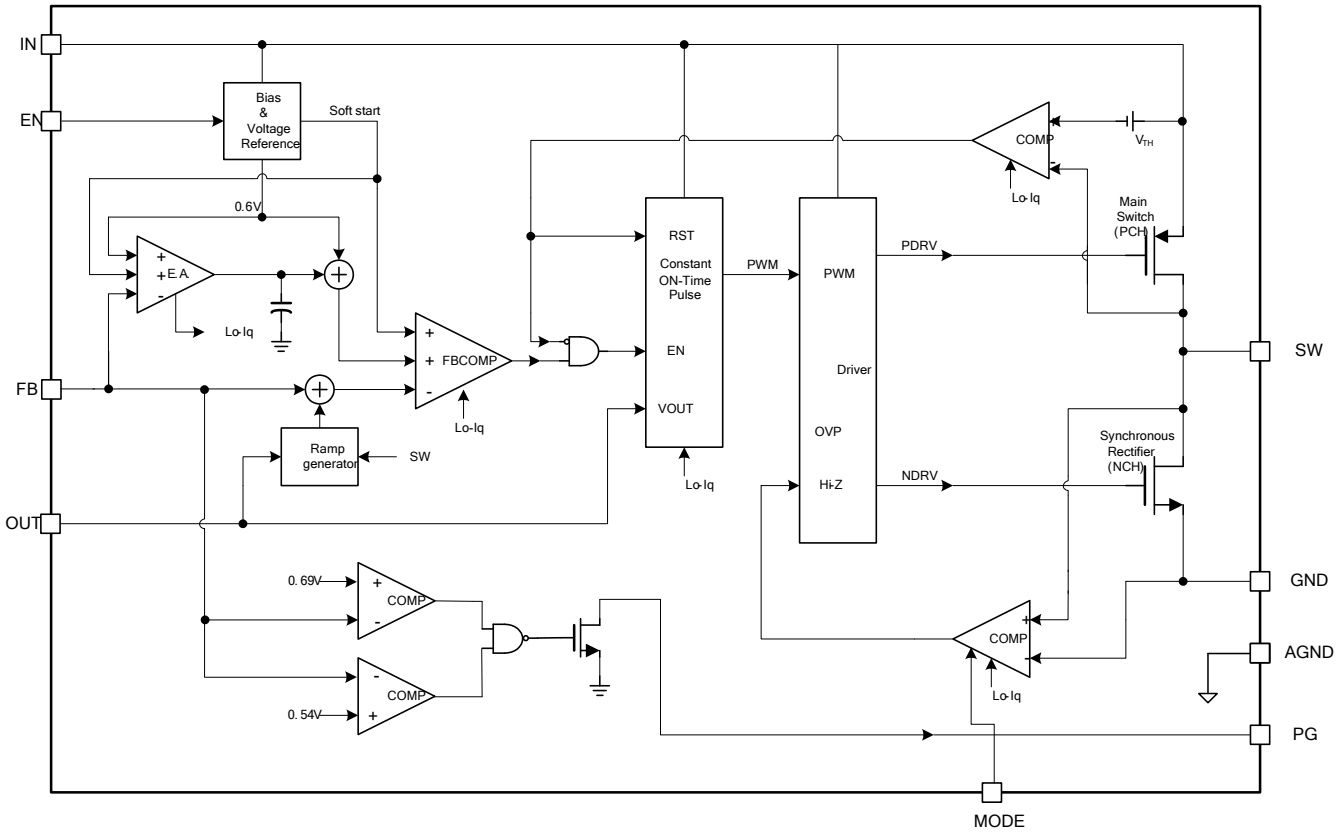

Figure 1: Functional Block Diagram

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OPERATION

The MP2164 comes in a small, surface-mounted QFN (2mmx2mm) package. The synchronous converter make the schematic and layout design very simple. The MP2164 uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency over the entire input range.

Constant-On-Time (COT) Control

Compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers the advantage of a simpler control loop and faster transient response. By using input voltage feed-forward, the MP2164 maintains a nearly constant switching frequency across the input and output voltage ranges. The on-time of the switching pulse can be estimated with Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.434us \quad (1)$$

To prevent inductor current runaway during the load transient, the MP2164 fixes the minimum off time at 100ns. This minimum off time limit does not affect operation of the MP2164 in steady state in any way.

PWM/PFM Mode Selection

The MP2164 has a programmable PWM and pulse-frequency modulation (PFM) work mode. When MODE is higher than 1.2V, the MP2164 enters PWM mode. When MODE is lower than 0.4V or floating, the MP2164 enters PFM mode.

Sleep Mode Operation

The MP2164 features sleep mode to achieve high efficiency at extremely light loads. In sleep mode, most of the circuit blocks are turned off except for the error amplifier (EA) and PWM comparator. This reduces the operation current to a minimal value (see Figure 2).

When the load becomes lighter, the ripple of the output voltage becomes larger and drives the error amplifier output (EAO) lower. When the EAO reaches an internal low threshold, it is clamped at that level, and the MP2164 enters sleep mode. During sleep mode, the valley of the FB voltage is regulated to the internal reference voltage, making the average output voltage slightly higher than the output voltage at discontinuous conduction mode (DCM) or continuous conduction mode (CCM). The on-time pulse at sleep mode is around 40% larger than that in DCM or CCM. Figure 3 shows the average FB voltage relationship with the internal reference at sleep mode.

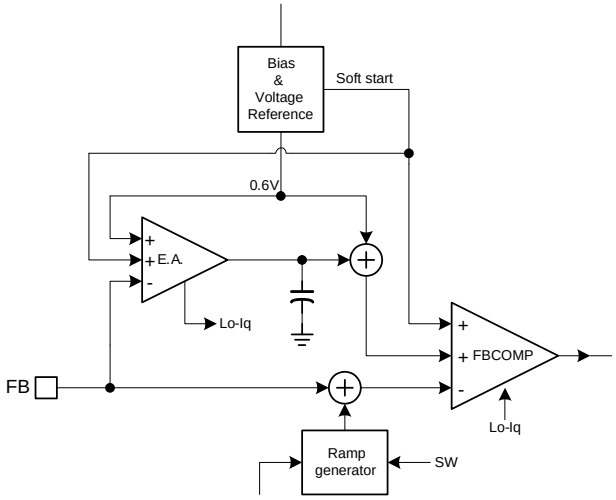

Figure 2: Operation Blocks at Sleep Mode

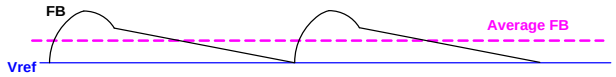

Figure 3: FB Average Voltage at Sleep Mode

When MP2164 is in sleep mode, the average output voltage is higher than the internal reference voltage. The EAO is kept low and clamped in sleep mode. When the load increases, the PWM switching period decreases to keep the output voltage regulated, and the output voltage ripple decreases relatively. Once the EAO is above the internal low threshold, the MP2164 exits sleep mode and enters either DCM or CCM depending on the load. In DCM or CCM, the EA regulates the average output voltage to the internal reference (see Figure 4).

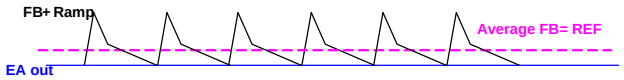

Figure 4: DCM Control

There is always a loading hysteresis when entering and exiting sleep mode due to the error amplifier clamping response time.

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Light-Load Operation

During light loads, the MP2164 uses a proprietary control scheme to save power and improve efficiency. There is a zero-current cross detection (ZCD) circuit to detect when the inductor current starts to reverse. The low-side MOSFET (LS-FET) turns off immediately when the inductor current starts to reverse and triggers the ZCD in DCM operation.

Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.3V), the MP2164 can be enabled by pulling EN above 1.15V. Leaving EN floating or pulling EN down to ground disables the MP2164. There is an internal 1MΩ resistor from EN to ground.

Soft Start (SS)

The MP2164 has a built-in soft start that ramps up the output voltage at a controlled slew rate to prevent an overshoot at start-up. The soft start time is about 1.2ms, typically. When disabled, the MP2164 ramps down the internal reference, allowing the load to discharge the output linearly.

Power Good (PG) Indicator

The MP2164 has an open drain with an external pull-up resistor (100 ~ 500kΩ) pin for power good indication (PG). When FB is within the regulation voltage (i.e.: 0.6V), PG is pulled up to IN by the internal resistor. If the FB voltage is out of regulation, PG is pulled down to ground by an internal MOSFET.

The MOSFET has a maximum $R_{DS(ON)}$ of less than 100Ω.

When IN and EN are not available and PG is pulled up by external power supply, PG uses a self-bias voltage (less than 0.7V).

Current Limit

The MP2164 has a typical 5A current limit for the high-side switch. When the high-side switch reaches the current limit, the MP2164 triggers the hiccup threshold until the current drops. This prevents the inductor current from continuing to build up and damaging the components.

Short Circuit and Recovery

The MP2164 enters short-circuit protection (SCP) mode when the inductor current reaches the current limit and attempts to recover from the short circuit with hiccup mode. In SCP, the MP2164 disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the short-circuit condition still remains after the soft start ends, the MP2164 repeats this operation cycle until the short circuit is removed and the output rises back to the regulation level.

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APPLICATION INFORMATION

Setting the Output Voltage

An external resistor divider is used to set the output voltage. The feedback resistor (R1) cannot be too large or too small considering the trade-off for stability and dynamic. There is no strict requirement on the feedback resistor. R1 is recommended to be greater than 10kΩ for some applications. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \quad (2)$$

The feedback circuit is shown in Figure 5.

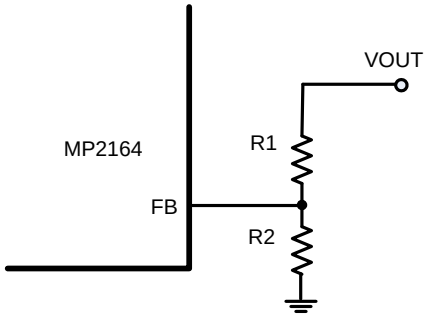

Figure 5: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Inductor

To achieve high efficiency at light load, a low-value inductor (i.e.: 0.47µH) is recommended for most applications. For the highest efficiency, a lower DCR is best. The inductance value can be derived from Equation (3):

$$I_{C1} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{osc}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. For higher output voltage, a 22µF capacitor may be needed for a more stable system.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e.: 0.1µF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

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Selecting the Output Capacitor

An output capacitor (C2) is required to maintain the DC output voltage.

Low ESR ceramic capacitors can be used with the MP2164 to keep the output ripple low. Generally, a 22μF output ceramic capacitor is sufficient for most cases. In higher output voltage conditions, a 47μF capacitor may be needed for a stable system.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

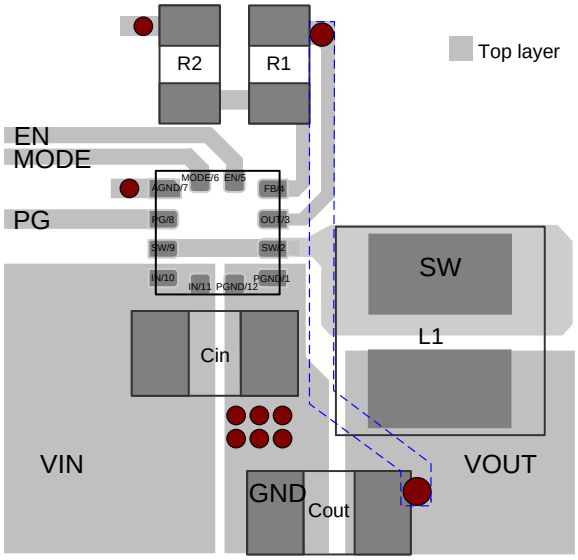
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

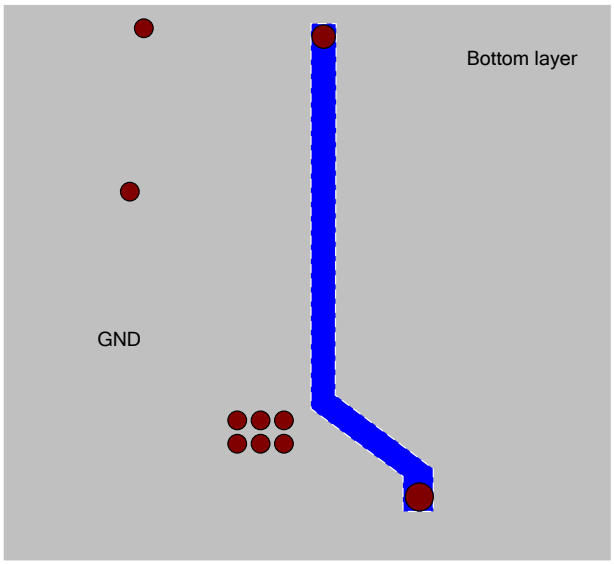
PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. If the layout is not carefully done, the regulator could show poor line or load regulation and stability issues. This is particularly true for the high-switching converter. For best results, refer to Figure 6 and follow the guidelines below. The top layer in Figure 6 shows a 0805 size ceramic capacitor used.

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct and wide traces.
2. Place the input capacitor as close to the IN and GND pins as possible.
3. Place the external feedback resistor next to FB.



Top Layer



Bottom Layer

Figure 7: Recommended Layout

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TYPICAL APPLICATION CIRCUIT

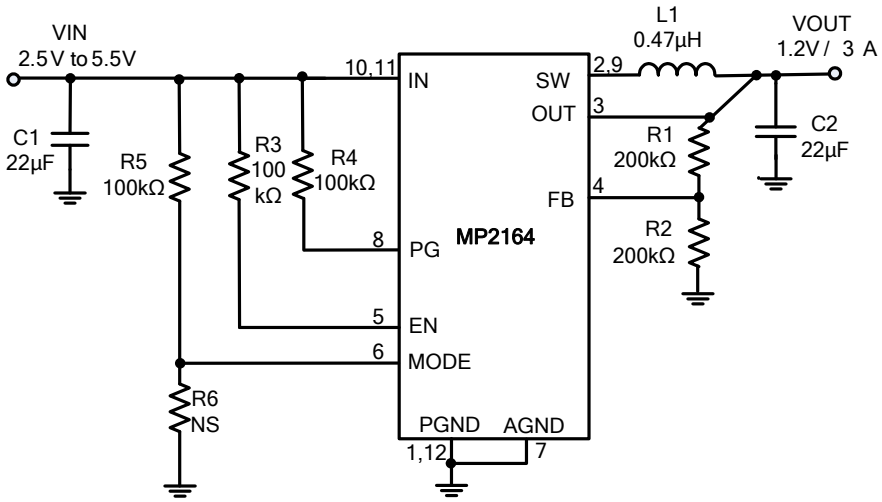

Figure 8: Typical Application Circuits for MP2164

NotE: VIN < 3.3V APPLICATIONS MAY REQUIRE MORE INPUT CAPACITORS.

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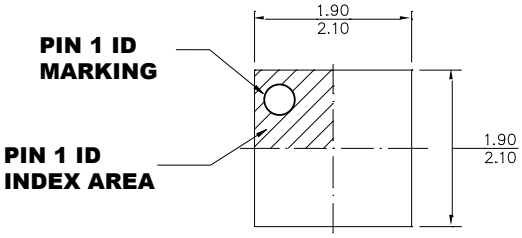
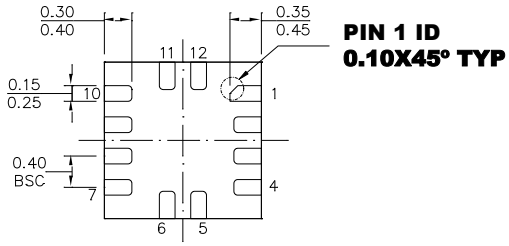
PACKAGE INFORMATION

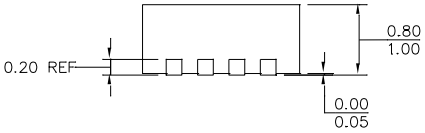
QFN-12 (2mmx2mm)



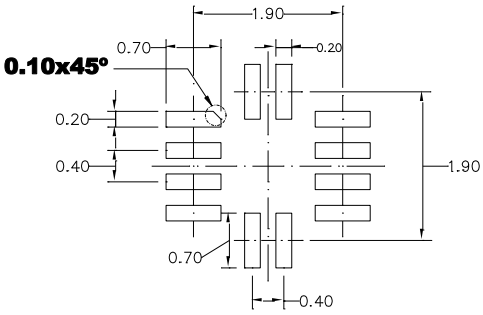
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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