MP2162

2A, 6V, 1.5MHz, 17μA I_Q, COT Synchronous Step Dwon Switcher In Ultra-small 2x1.5mm QFN

The Future of Analog IC Technology

DESCRIPTION

The MP2162 is a monolithic step-down switch mode converter with built-in internal power MOSFETs. It achieves 2A continuous output current from a 2.5V to 6V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

The Constant-On-Time control scheme provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2162 is available in the small QFN8 2.0x1.5mm package and requires a minimum number of readily available standard external components.

The MP2162 is ideal for a wide range of applications including High Performance DSPs, FPGAs, PDAs, and portable instruments.

FEATURES

- Very Low I_Q: 17μA
- Default 1.5MHz Switching Frequency
- EN and Power Good for Power Sequencing
- Ultra-small 2x1.5mm QFN8 Package
- Wide 2.5V to 6V Operating Input Range Output Adjustable from 0.6V
- Up to 2A Output Current
- 100% Duty Cycle in Dropout
- 100mΩ and 60mΩ Internal Power MOSFET Switches
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protect with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors

APPLICATIONS

- Wireless/Networking Cards
- Portable Instruments
- Battery Powered Devices
- Low Voltage I/O Systems Power

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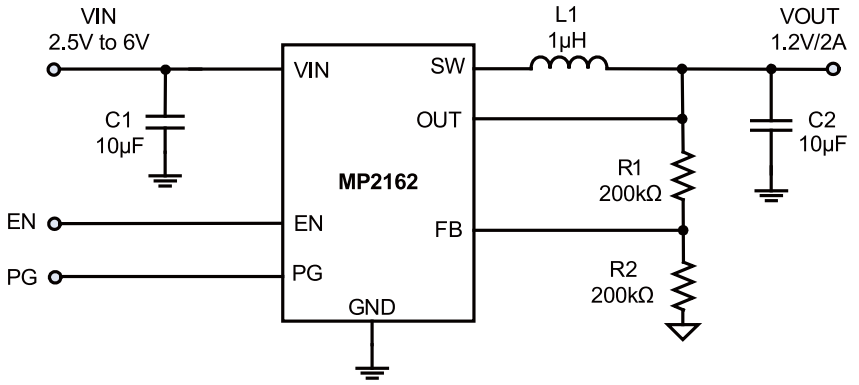
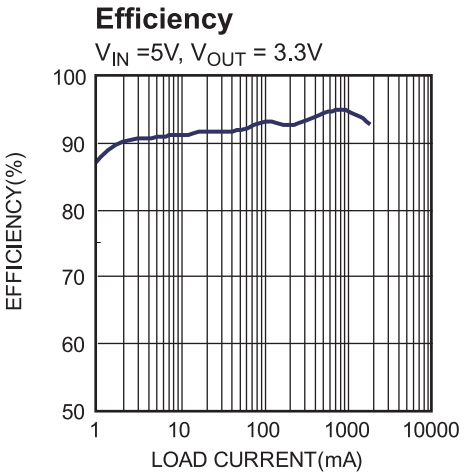
TYPICAL APPLICATION





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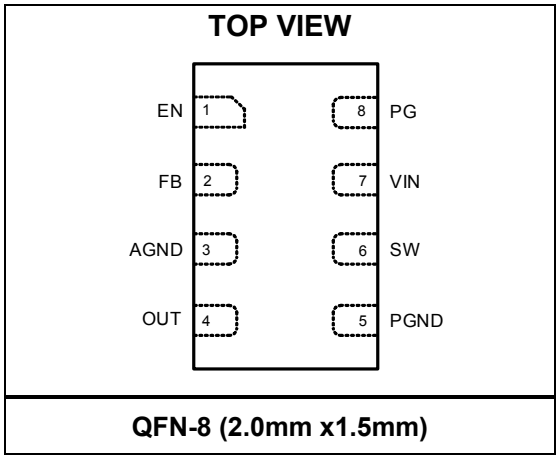
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2162GQH	QFN-8 (2.0mm x1.5mm)	AZ

* For Tape & Reel, add suffix –Z (e.g. MP2162GQH–Z);

PACKAGE REFERENCE



QFN-8 (2.0mm x1.5mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 6.5V
V_{SW} .....
-0.3V (-5V for <10ns) to 6.5V (10V for <10ns)
All Other Pins .....-0.3V to 6.5 V
Junction Temperature .....150°C
Lead Temperature .....260°C
Continuous Power Dissipation (T_A = +25°C) (2)
…….. ..... 1.14W
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....2.5V to 6V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-8 (2.0mm x1.5mm)	110	55	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	2.5V ≤ V_{IN} ≤ 6V	-3%	0.600	+3%	V/%
		T_A=-40°C to +85°C (6)	-3.5%		+3.5%	
Feedback Current	I_{FB}	V_{FB} = 0.6V		10	50	nA
PFET Switch On Resistance	$R_{DSON\ P}$			100		mΩ
NFET Switch On Resistance	$R_{DSON\ N}$			60		mΩ
Switch Leakage		V_{EN} = 0V, V_{IN} = 6V V_{SW} = 0V and 6V		0	1	µA
PFET Current Limit			2.7	3.2	4.0	A
ON Time	T_{ON}	V_{IN}=5V, V_{OUT}=1.2V		185		ns
		V_{IN}=3.6V, V_{OUT}=1.2V		245		
Switching frequency	F_s	V_{OUT}=1.2V	-20%	1500	+20%	kHz/%
		T_A=-40°C to +85°C(6)	-25%	1500	+25%	kHz/%
Minimum Off Time	$T_{MIN-OFF}$			60		ns
Soft-Start Time	T_{SS-ON}			1.5		ms
Power Good Upper Trip Threshold	PG_H	FB voltage respect to the regulation		+10		%
Power Good Lower Trip Threshold	PG_L			-10		%
Power Good Delay	PG_D			50		µs
Power Good Sink Current Capability	V_{PG-L}	Sink 1mA			0.4	V
Power Good Logic High Voltage	V_{PG-H}	V_{IN}=5V, V_{FB}=0.6V	4.9			V
Power Good Internal Pull Up Resistor	R_{PG}			550		kΩ
Under Voltage Lockout Threshold Rising			2.15	2.3	2.45	V
Under Voltage Lockout Threshold Hysteresis				260		mV
EN Input Logic Low Voltage					0.4	V
EN Input Logic High Voltage			1.2			V
EN Input Current		V_{EN}=2V		1.5		µA
		V_{EN}=0V		0		µA
Supply Current (Shutdown)		V_{EN}=0V		0	1	µA
Supply Current (Quiescent)		V_{EN}=2V, V_{FB}=0.63V, V_{IN}=5V		17	20	µA
Thermal Shutdown(5)				150		°C
Thermal Hysteresis(5)				30		°C

Notes:

5) Guaranteed by design.

6) Guaranteed by characterization test.

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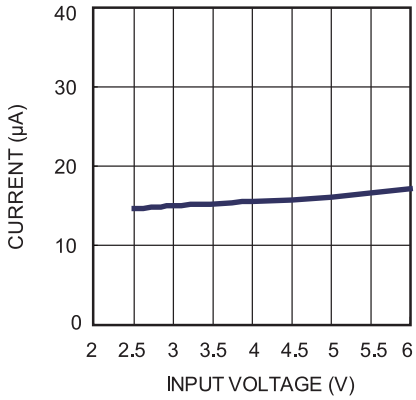
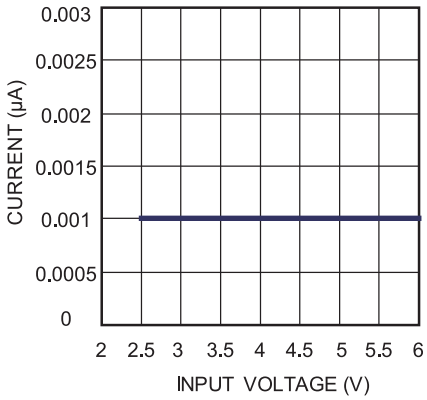
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25ºC, unless otherwise noted.

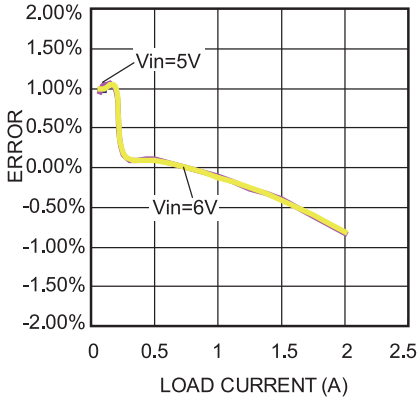
Quiescent Current vs. Input Voltage



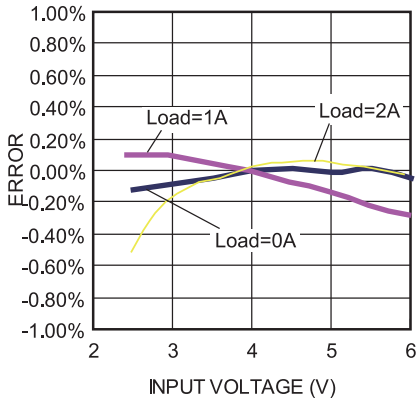
Shutdown Current vs. Input Voltage



Load Regulation

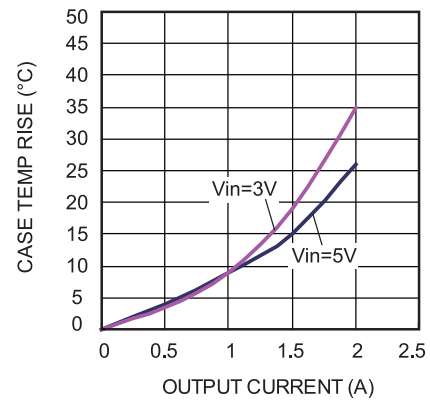


Line Regulation



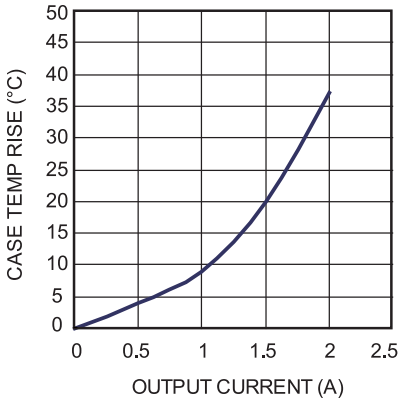
Case Temp Rise

Vin=3/5V, Vo=1.2V

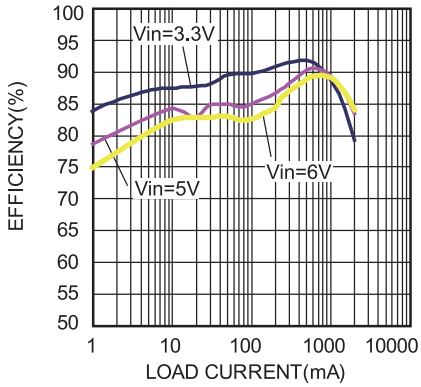


Case Temp Rise

Vin=5V, Vo=3.3V

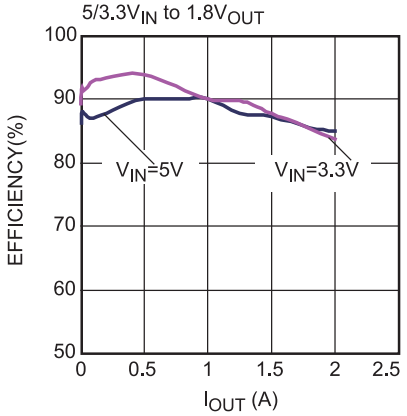


Efficiency



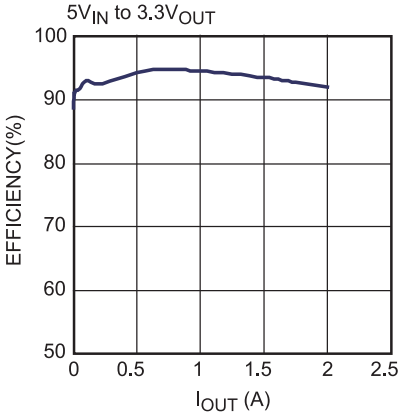
Efficiency

$5/3.3V_{IN}$ to $1.8V_{OUT}$



Efficiency

$5V_{IN}$ to $3.3V_{OUT}$



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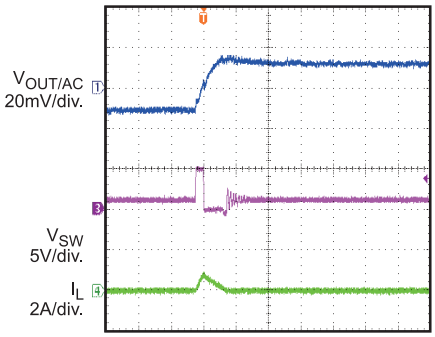
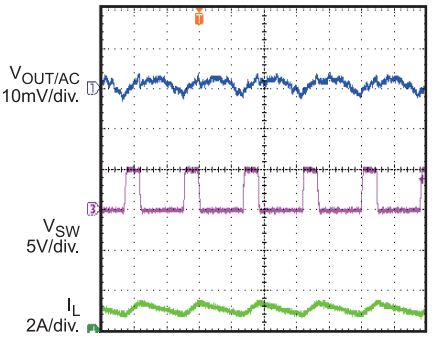
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25ºC, unless otherwise noted.

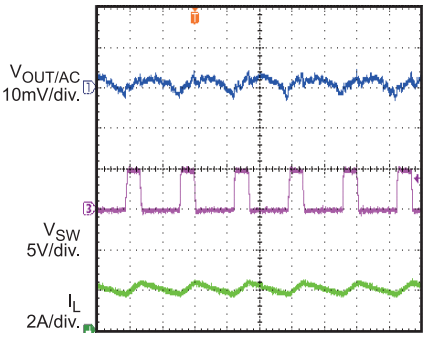
Output Ripple
I_{OUT}=0A



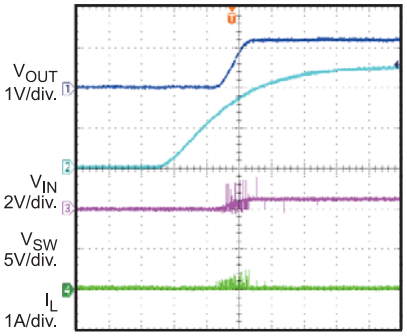
Output Ripple
I_{OUT}=1A



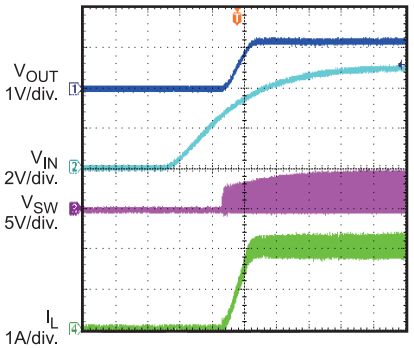
Output Ripple
I_{OUT}=2A



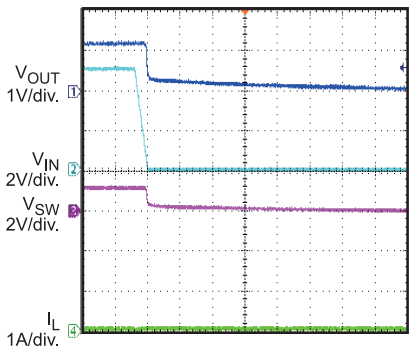
VIN Power Up without Load



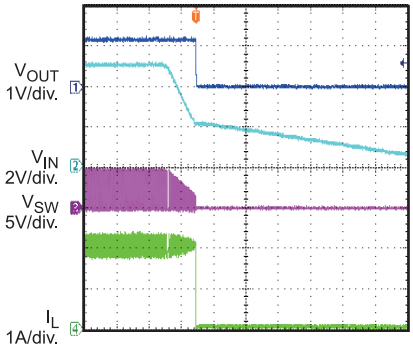
VIN Power Up with 2A Load



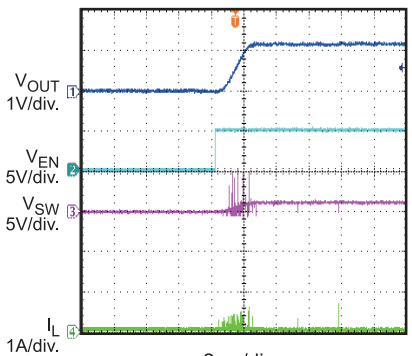
VIN Shut Down without Load



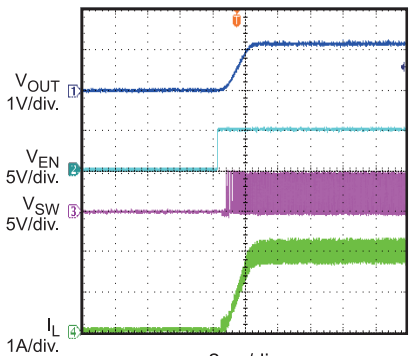
VIN Shut Down with 2A Load



EN Start Up without Load



EN Start Up with 2A Load



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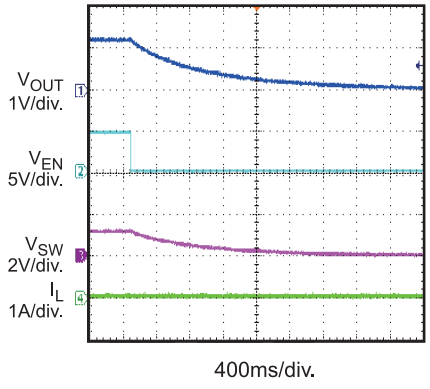
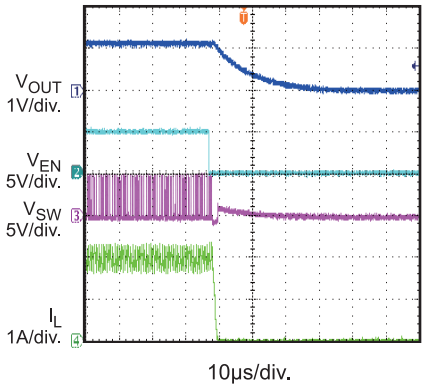
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25ºC, unless otherwise noted

EN Shut Down without Load



EN Shut Down with 2A Load



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PIN FUNCTIONS

Pin #	Name	Description
8	PG	Power Good Indicator. The output of this pin is an open drain with internal pull up resistor to VIN. PGOOD is pulled up to VIN when the FB voltage is within 10% of the regulation level, if FB voltage is out of that regulation range, it is LOW.
7	VIN	Supply Voltage. The MP2162 operates from a +2.5V to +6V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
6	SW	Switch Output
5	PGND	Power ground
4	OUT	Input sense pin for output voltage
3	AGND	Analogy ground for internal control circuit
2	FB	Feedback pin. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
1	EN	On/Off Control

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BLOCK DIAGRAM

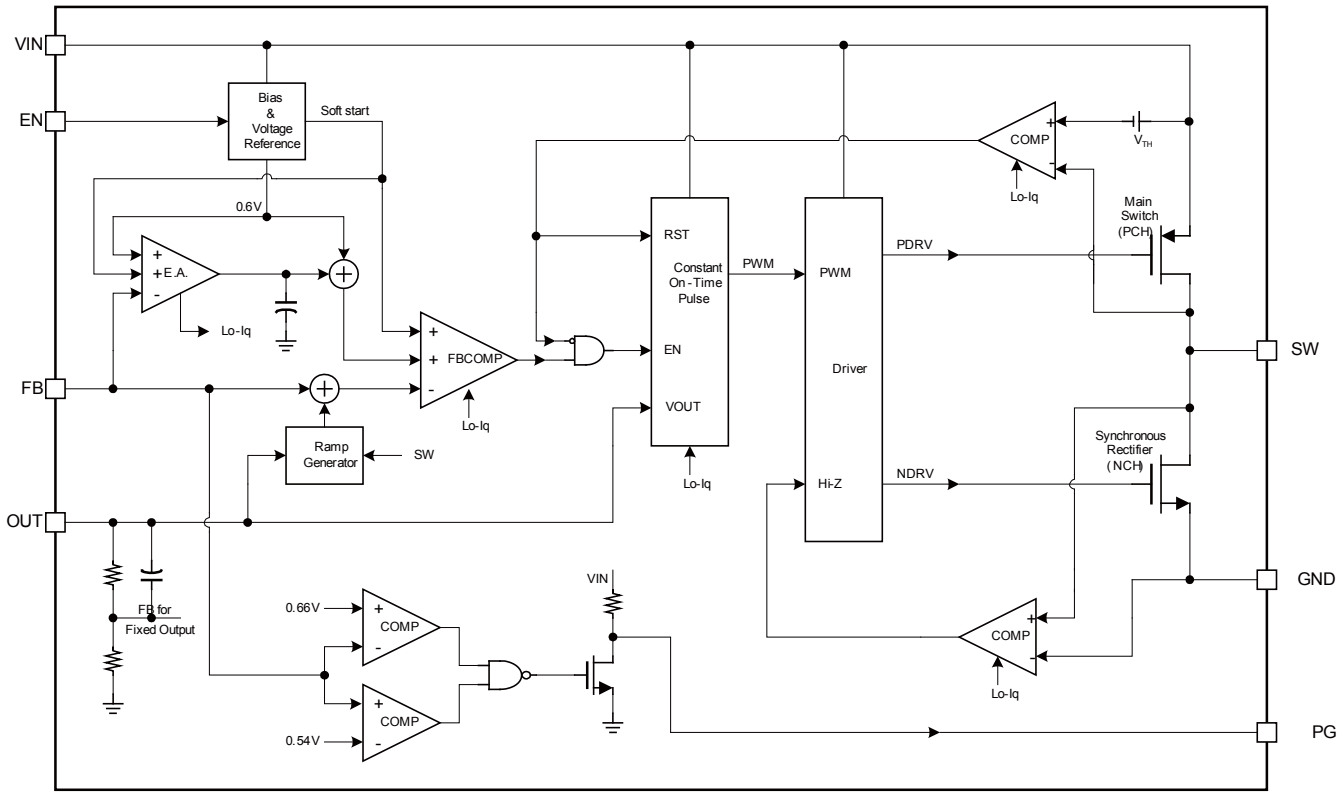

Figure 1: MP2162 Block Diagram

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OPERATION

MP2162 uses constant on-time control with input voltage feed forward to stabilize the switching frequency over full input range. At light load, MP2162 employs a proprietary control of low side switch and inductor current to eliminate ringing on switching node and improve efficiency.

Constant On-time Control

Compare to fixed frequency PWM control, constant on-time control offers the advantage of simpler control loop and faster transient response. By using input voltage feed forward, MP2162 maintains a nearly constant switching frequency across input and output voltage range. The on-time of the switching pulse can be estimated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.667\mu s$$

To prevent inductor current run away during load transient, MP2162 fixes the minimum off time to be 60ns. However, this minimum off time limit will not affect operation of MP2162 in steady state in any way.

Light Load Operation

In light load condition, MP2162 uses a proprietary control scheme to save power and improve efficiency. The MP2162 will turn off the low side switch when inductor current starts to reverse. Then MP2162 works in discontinuous conduction mode (DCM) operation.

The DCM mode happens only after low side switch turned off by ZCD circuit. Considering the ZCD circuit propagation time, the typical delay is 30ns. It means the inductor current still fall after the ZCD is trigger during this delay. If the inductor current falling slew rate is fast (Vo voltage is high or close to Vin), the low side MOSFET is turned off at the moment inductor current may be negative. This phenomena will cause MP2162 can not enter DCM operation. If the DCM mode is required, the off time of low side MOSFET in CCM should be longer than 60ns. It means the maximum duty is 90% to guarantee DCM mode at light load.

For example, V_{IN} is 3.4V and V_{OUT} is 3.3V, the off time in CCM is 20ns. It is difficult to enter DCM at light load. And using smaller inductor can improve it and make it enter DCM easily.

Enable

When input voltage is greater than the under-voltage lockout threshold (UVLO), typically 2.3V, MP2162 can be enabled by pulling EN pin to higher than 1.2V. Leaving EN pin float or pull down to ground will disable MP2162. There is an internal 1Meg Ohm resistor from EN pin to ground.

Soft Start

MP2162 has built-in soft start that ramps up the output voltage in a controlled slew rate, avoiding overshoot at startup. The soft start time is about 1.5ms typical.

Power GOOD Indictor

MP2162 has an open drain with 550kΩ pull-up resistor pin for power good indicator PGOOD. When FB pin is within +/-10% of regulation voltage, i.e. 0.6V, PGOOD pin is pulled up to VIN by the internal resistor. If FB pin voltage is out of the +/-10% window, PGOOD pin is pulled down to ground by an internal MOS FET. The MOS FET has a maximum R_{dson} of less than 100 Ohm.

Current limit

MP2162 has a typical 3.2A current limit for the high side switch. When the high side switch hits current limit, MP2162 will touch the hiccup threshold until the current lower down. This will prevent inductor current from continuing to build up which will result in damage of the components.

Short Circuit and Recovery

MP2162 enters short circuit protection mode also when the current limit is hit, and tries to recover from short circuit with hiccup mode. In short circuit protection, MP2162 will disable output power stage, discharge soft-start cap and then automatically try to soft-start again. If the short circuit condition still holds after soft-start ends, MP2162 repeats this operation cycle till short circuit disappears and output rises back to regulation level.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 can not be too large neither too small considering the trade-off for stability and dynamic. Choose R1 to be around 120kΩ to 200kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1}$$

The feedback circuit is shown as Figure 2.

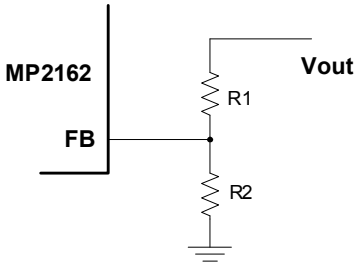

Figure 2: Feedback Network

Table 1 lists the recommended resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

Selecting the Inductor

A 0.68μH to 2.2μH inductor is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. For higher output voltage, 47uF may be needed for more stable system.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small and high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

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Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout

Proper layout of the switching power supplies is very important, and sometimes critical for proper function. For the high-frequency switching converter, poor layout design can result in poor line or load regulation and stability issues.

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

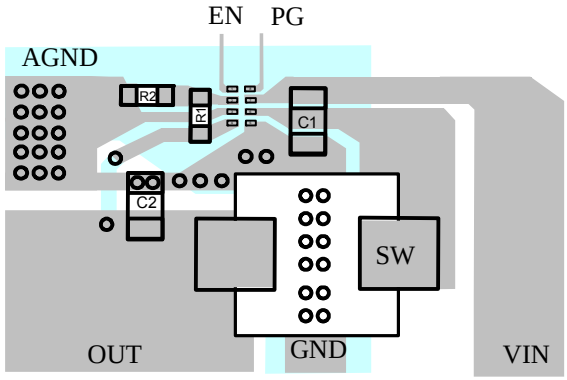

Figure 3: PCB Layout Recommendation

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	5V
V_{OUT}	1.2V
f_{SW}	1500kHz

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

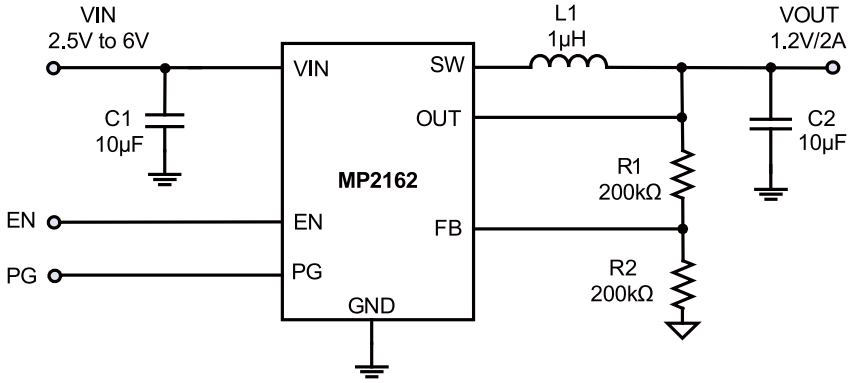

Figure 4: Typical Application Circuit

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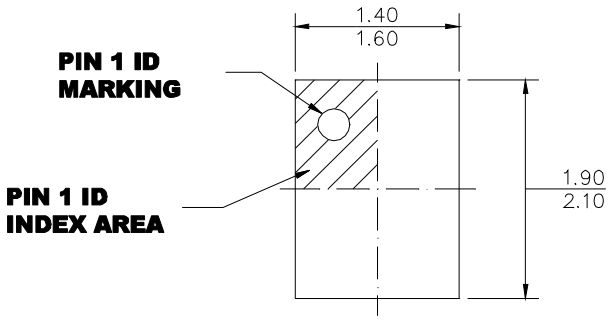
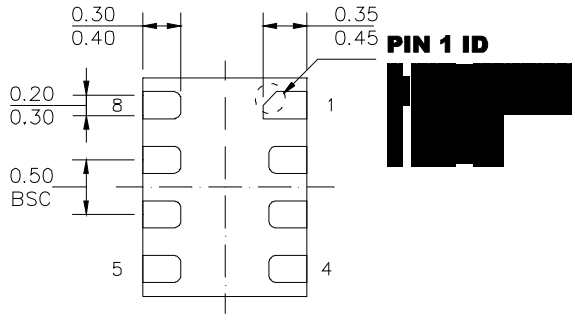
PACKAGE INFORMATION

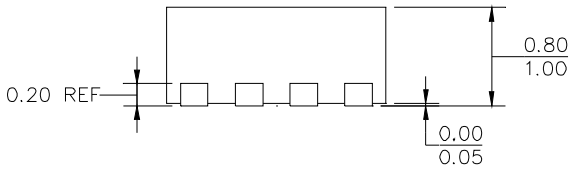
QFN-8 (2.0mm X1.5mm)



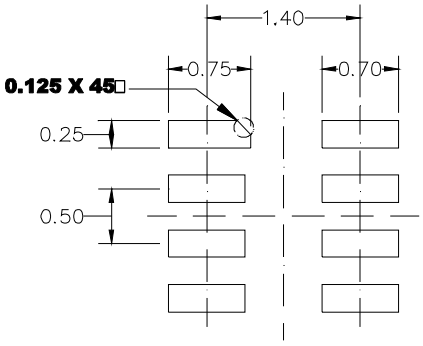
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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