DESCRIPTION

The MP2153 is a monolithic, step-down, switch-mode converter with built-in, internal power MOSFETs. The MP2153 achieves 3A of continuous output current from a 2.5V to 5.5V input voltage range with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2153 is ideal for a wide range of applications, including solid-state drives, portable devices, and other low-power, low-voltage systems.

The MP2153 requires a minimal number of readily available, standard, external components and is available in ultra-small SOT563 (1.6mmx1.6mm) or UTQFN-6 (1.2mmx1.6mm) packages.

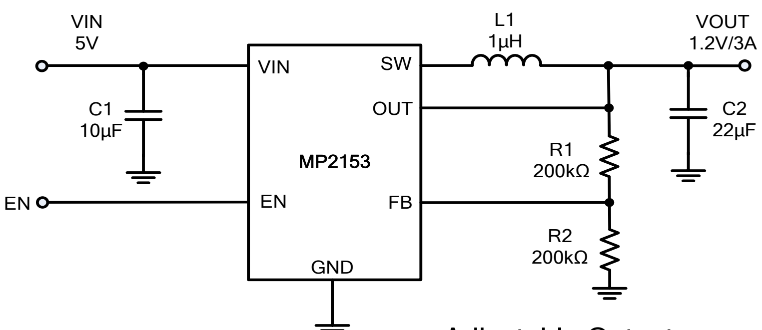
FEATURES

- Low I_Q: 25μA
- 1.1MHz Switching Frequency
- EN for Power Sequencing
- 1% FB Accuracy
- Wide 2.5V to 5.5V Operating Input Range
- Output Adjustable from 0.6V
- Up to 3A Output Current
- 65mΩ and 35mΩ Internal Power MOSFET Switches
- 100% Duty On
- Output Discharge
- V_{OUT} Over-Voltage Protection (OVP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Power Good (for Fixed Output Version Only)
- Available in SOT563 (1.6mmx1.6mm) or UTQFN-6 (1.2mmx1.6mm) Packages

APPLICATIONS

- Solid-State Drives (SSD)
- Portable Instruments
- Battery-Powered Devices
- Multi-Function Printers

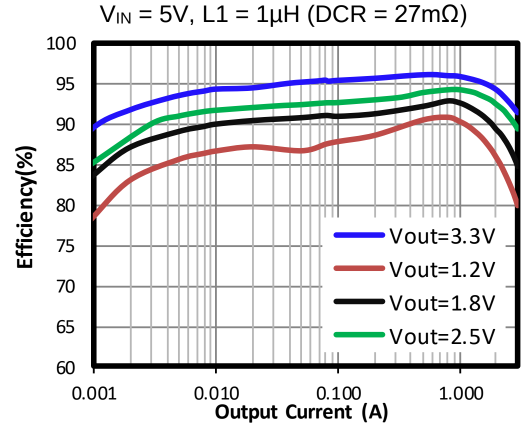
TYPICAL APPLICATION



Adjustable Output

Efficiency vs. Output Current

V_{IN} = 5V, L1 = 1μH (DCR = 27mΩ)



ORDERING INFORMATION

Part Number*	Package	Top Marking	V_{OUT} Range
MP2153GQFU	UTQFN-6 (1.2mmx1.6mm)	See Below	Adjustable
MP2153GQFU-12		See Below	*Fixed 1.2V*
MP2153GQFU-15		See Below	*Fixed 1.5V*
MP2153GQFU-18		See Below	*Fixed 1.8V*
MP2153GQFU-25		See Below	*Fixed 2.5V*
MP2153GQFU-33		See Below	*Fixed 3.3V*

* For Tape & Reel, add suffix –Z (e.g. MP2153GQFU–Z).

TOP MARKING (MP2153GQFU)

FU
LL

FU: Product code of MP2153GQFU
LL: Lot number

TOP MARKING (MP2153GQFU-12)

GP
LL

GP: Product code of MP2153GQFU-12
LL: Lot number

TOP MARKING (MP2153GQFU-15)

GQ
LL

GQ: Product code of MP2153GQFU-15
LL: Lot number

TOP MARKING (MP2153GQFU-18)

GR
LL

GR: Product code of MP2153GQFU-18
LL: Lot number

TOP MARKING (MP2153GQFU-25)

GT
LL

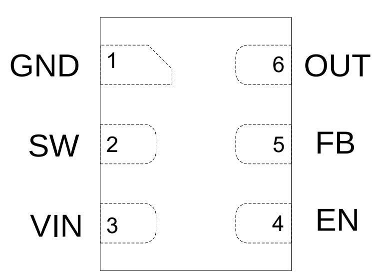
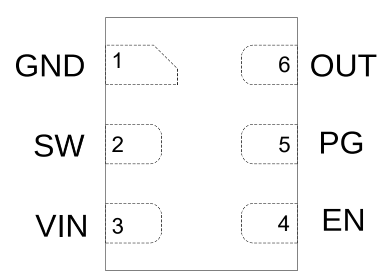
GT: Product code of MP2153GQFU-25
LL: Lot number

TOP MARKING (MP2153GQFU-33)

GU
LL

GU: Product code of MP2153GQFU-33
LL: Lot number

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
UTQFN-6 (1.2mmx1.6mm)	**UTQFN-6 (1.2mmx1.6mm)**
Adjustable Version MP2153GQFU	**Fixed Vo Version MP2153GQFU-12, MP2153GQFU-15, MP2153GQFU-18, MP2153GQFU-25, MP2153GQFU-33**

ORDERING INFORMATION

Part Number*	Package	Top Marking	V_{OUT} Range
MP2153GTF	SOT563 (1.6mmx1.6mm)	*See Below*	*Adjustable*
MP2153GTF-12		*See Below*	*Fixed 1.2V*
MP2153GTF-15		*See Below*	*Fixed 1. 5V*
MP2153GTF-18		*See Below*	*Fixed 1.8V*
MP2153GTF-25		*See Below*	*Fixed 2.5V*
MP2153GTF-33		*See Below*	*Fixed 3.3V*

* For Tape & Reel, add suffix –Z (e.g. MP2153GTF–Z).

TOP MARKING (MP2153GTF)

AYTY
LLL

AYT: Product code of MP2153GTF
Y: Year code
LLL: Lot number

TOP MARKING (MP2153GTF-12)

BBPY
LLL

BBP: Product code of MP2153GTF-12
Y: Year code
LLL: Lot number

TOP MARKING (MP2153GTF-15)

BBQY
LLL

BBQ: Product code of MP2153GTF-15
Y: Year code
LLL: Lot number

TOP MARKING (MP2153GTF-18)

BBRY
LLL

BBR: Product code of MP2153GTF-18
Y: Year code
LLL: Lot number

TOP MARKING (MP2153GTF-25)

BBTY
LLL

BBT: Product code of MP2153GTF-25
Y: Year code
LLL: Lot number

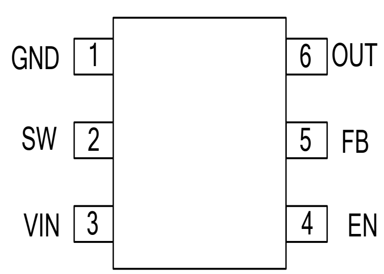
TOP MARKING (MP2153GTF-33)

BBUY
LLL

BBU: Product code of MP2153GTF-33
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

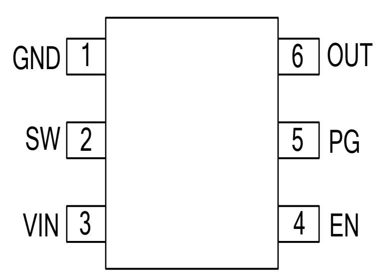
TOP VIEW



SOT563 (1.6mmx1.6mm)

Adjustable Version
MP2153GTF

TOP VIEW



SOT563 (1.6mmx1.6mm)

Fixed Vo Version
MP2153GTF-12,MP2153GTF-15, MP2153GTF-18, MP2153GTF-25, MP2153GTF-33

PIN FUNCTIONS

Pin #	Name (SOT563 and UTQFN) Adj version	Name (SOT563 and UTQFN) Fixed version	Description
1	GND	GND	**Power ground.**
2	SW	SW	**Output switching node.** SW is the drain of the internal, high-side, P-channel MOSFET. Connect the inductor to SW to complete the converter.
3	VIN	VIN	**Supply voltage.** The MP2153 operates from a +2.5V to +5.5V unregulated input. Use a decoupling capacitor to prevent large voltage spikes from appearing at the input.
4	EN	EN	**On/off control.**
5	FB	-	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage.
5	-	PG	**Power good indicator.** The output of PG is an open drain with an external pull-up resistor to VIN.
6	OUT	OUT	**Output sense.** OUT is the voltage power rail and input sense pin for the output voltage. An output capacitor is needed to decrease the output voltage ripple.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} .... -0.3V (-5V for <10ns) to 6.5V (10V for <10ns)
All other pins ....-0.3V to 6.5V
Junction temperature ....150°C
Lead temperature ....260°C
Continuous power dissipation (T_A = +25°C) (2)(4)
SOT563 .... 1.5W
UTQFN .... 2W (2)(5)
Storage temperature .... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....2.5V to 5.5V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOT563 (1.6mmx1.6mm)
EV2153-TF-00A (4) .... 80......50 .... °C/W
JESD51-7 (6)......................... 130.....60 .... °C/W

UTQFN-6 (1.2mmx1.6mm)
EV2153-QFU-00A (5)............. 65......30 .... °C/W
JESD51-7 (6)......................... 173....127 ... °C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV2153-TF-00A, 2-layer PCB, 63mmx63mm.
5) Measured on EV2153-QFU-00A, 2-layer PCB, 63mmx63mm.
6) Measured on JESD51-7, 4-layer PCB.
The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C (7), typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} range	V_{IN}		2.5		5.5	V
Under-voltage lockout threshold rising	$UVLO_R$			2.3	2.45	V
Under-voltage lockout threshold hysteresis	$UVLO_H$			200		mV
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
OUT voltage (MP2153XX-12)	V_O	T_J = 25°C	1188	1200	1212	mV
		T_J = -40°C to +125°C	1182	1200	1218	mV
OUT voltage (MP2153XX-15)	V_O	T_J = 25°C	1485	1500	1515	mV
		T_J = -40°C to +125°C	1478	1500	1522	mV
OUT voltage (MP2153XX-18)	V_O	T_J = 25°C	1782	1800	1818	mV
		T_J = -40°C to +125°C	1773	1800	1827	mV
OUT voltage (MP2153XX-25)	V_O	T_J = 25°C	2475	2500	2525	mV
		T_J = -40°C to +125°C	2463	2500	2537	mV
OUT voltage (MP2153XX-33)	V_O	T_J = 25°C	3267	3300	3333	mV
		T_J = -40°C to +125°C	3251	3300	3349	mV
Feedback current	I_{FB}	V_{FB} = 0.63V		50	100	nA
P-FET switch on resistance	R_{DSON_P}	V_{IN} = 5V		65		mΩ
N-FET switch on resistance	R_{DSON_N}	V_{IN} = 5V		35		mΩ
Switch leakage	I_{SW}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = +25°C		0	1	µA
P-FET peak current limit	I_{HSP}		4		6	A
N-FET valley current limit	I_{HSL}			3.5		A
ZCD				50		mA
On time	T_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V	180	220	260	ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V	240	300	360	
Switching frequency	F_{SW}	V_{OUT} = 1.2V		1100		kHz
Minimum off time	$T_{MIN-OFF}$			100		ns
Minimum on time (7)	T_{MIN-ON}			60		ns
Soft-start time	T_{SS-ON}	V_{OUT} rises from 10% to 90%		0.5		ms
Maximum duty cycle			100			%
Power good rising threshold UV	PG_{UVR}	Fixed V_{OUT} version, V_{OUT} rising edge		90		%
Power good falling threshold UV	PG_{UVF}	Fixed V_{OUT} version, V_{OUT} falling edge		85		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C (7), typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good rising threshold OV	PG_{OVR}	Fixed V_{OUT} version, V_{OUT} rising edge		115		%
Power good falling threshold OV	PG_{OVF}	Fixed V_{OUT} version, V_{OUT} falling edge		105		%
Power good delay	PG_D	Fixed V_{OUT} version, PG rising/falling edge		150		μs
Power good sink current capability	V_{PG-L}	Fixed V_{OUT} version, sink 1mA			0.4	V
Power good logic high voltage	V_{PG-H}	Fixed V_{OUT} version, V_{IN} = 5V, V_{FB} = 0.6V	4.9			V
EN turn-on delay	T_{DEN}	EN on to SW active		150		μs
EN input logic low voltage	V_{EN-L}				0.4	V
EN input logic high voltage	V_{EN-H}		1.2			V
Output discharge resistor	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		200		Ω
EN input current	I_{EN}	V_{EN} = 2V		1.2		μA
		V_{EN} = 0V		0		μA
Supply current (shutdown)	I_{SD}	V_{EN} = 0V, T_J = +25°C		0	1	μA
Supply current (quiescent) (MP2153XX, adjustable)	I_Q	V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 5V, T_J = +25°C		25	30	μA
Supply current (quiescent) (MP2153XX-XX, fixed V_{OUT})		V_{EN} = 2V, no switching, V_{IN} = 5V, T_J = +25°C		30	35	μA
Output over-voltage threshold	V_{OVP}		110%	115%	120%	V_{FB}
V_{OUT} OVP hysteresis	V_{OVP_HYS}			10%		V_{FB}
OVP delay	T_{DOVP}			12		μs
Low-side current	I_{LSN}	Current flow from SW to GND		1.5		A
Absolute V_{IN} OVP	OVP	After V_{OUT} OVP enable		6.1		V
Absolute V_{IN} OVP hysteresis	OVP_H			400		mV
Thermal shutdown (8)	OT			160		°C
Thermal hysteresis (8)	OT_H			30		°C

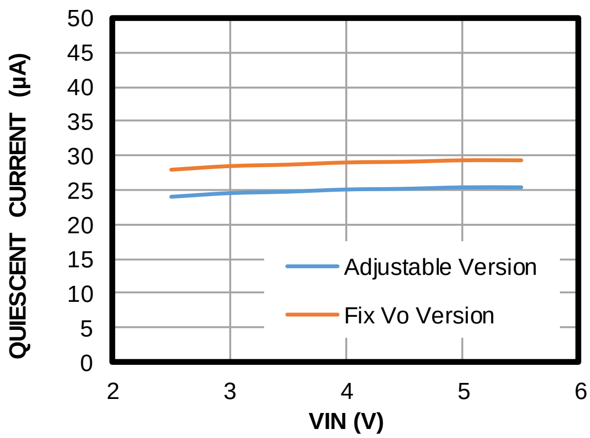
NOTES:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

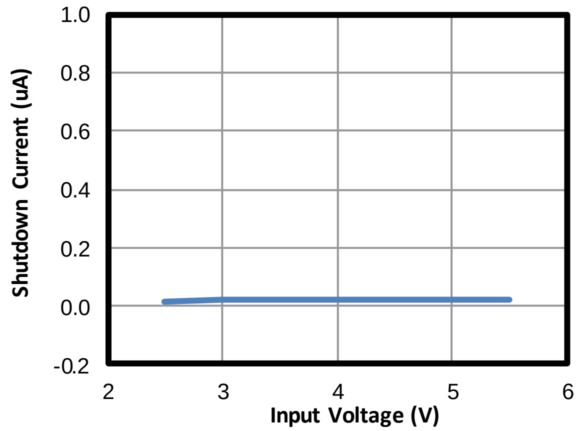
V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

Quiescent Current vs. VIN

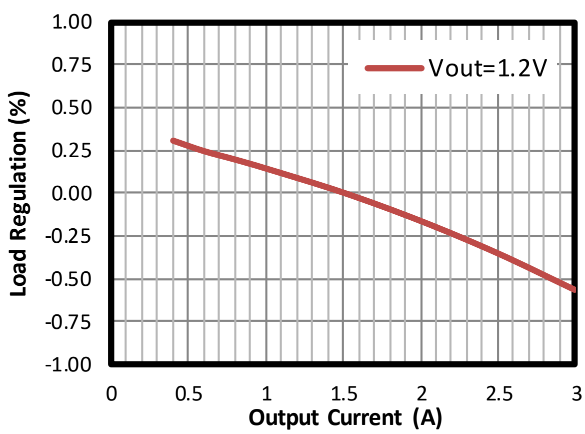


Shutdown Current vs. Input Voltage

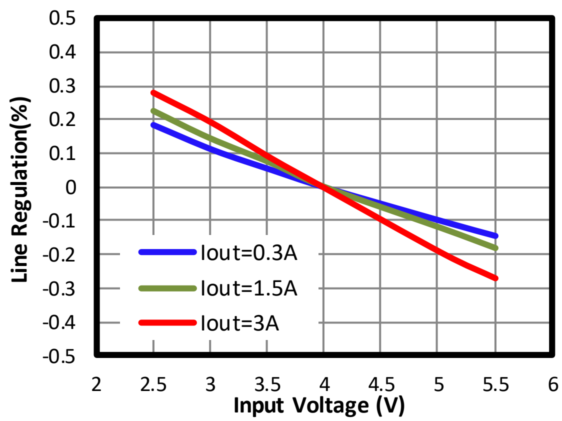
V_{EN} = 0V



Load Regulation

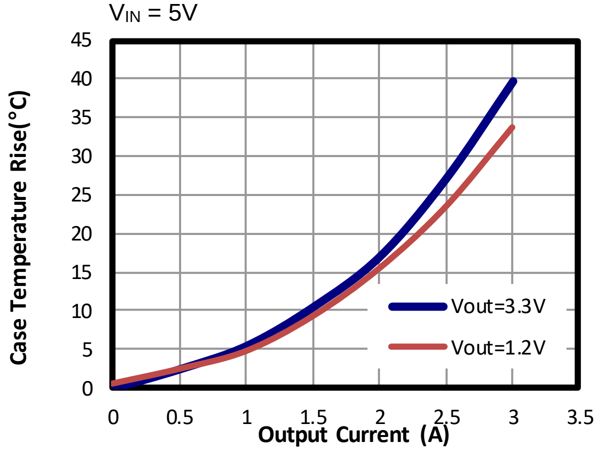


Line Regulation



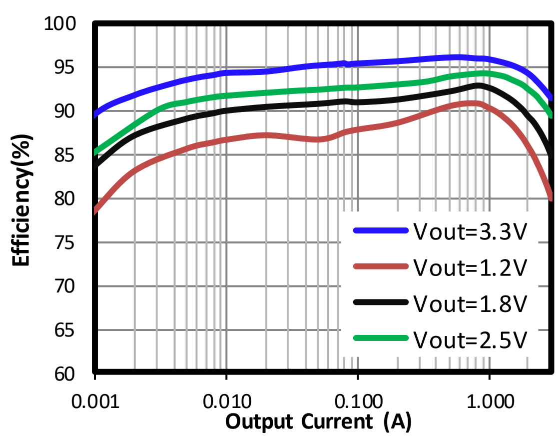
Case Temperature Rising vs. Output Current

V_{IN} = 5V



Efficiency vs. Output Current

V_{IN} = 5V

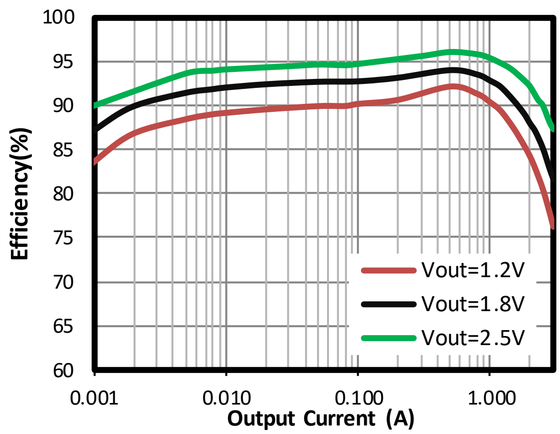


TYPICAL CHARACTERISTICS *(continued)*

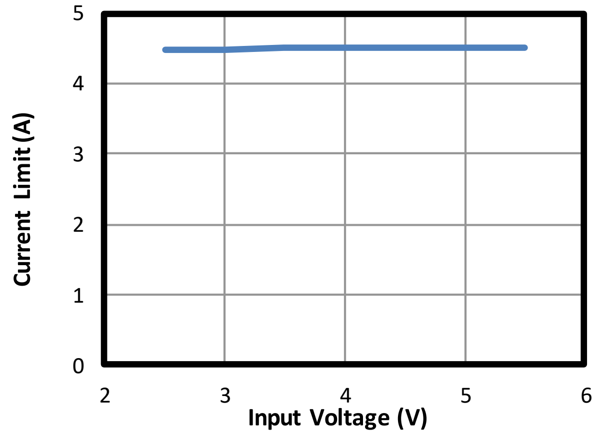
V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

Efficiency vs. Output Current

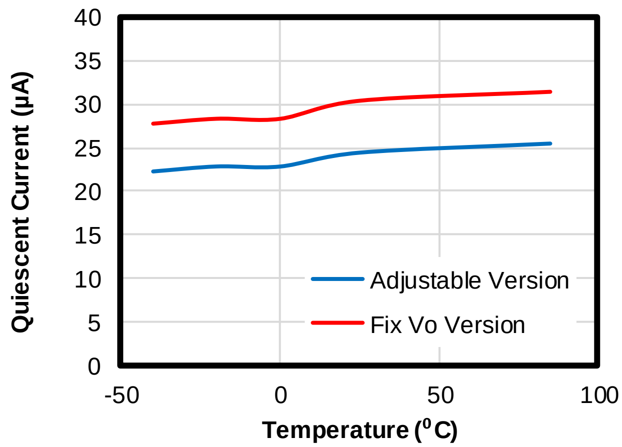
V_{IN} = 3.6V



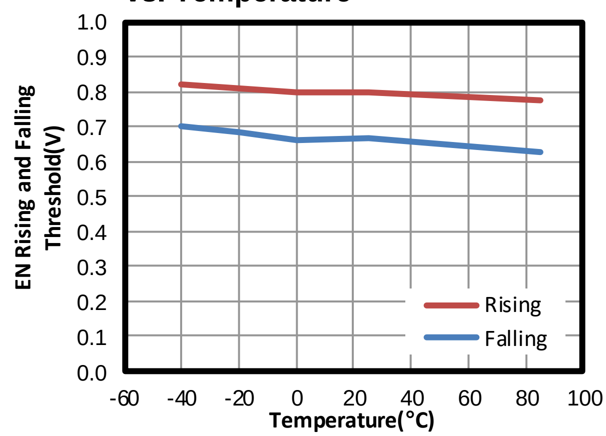
Peak Current Limit vs. V_{IN}



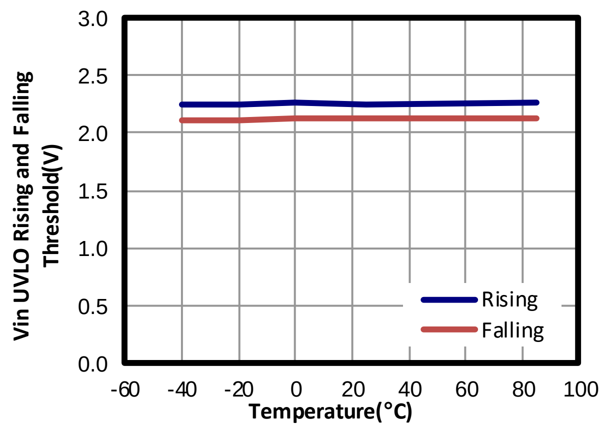
Quiescent Current vs. Temperature



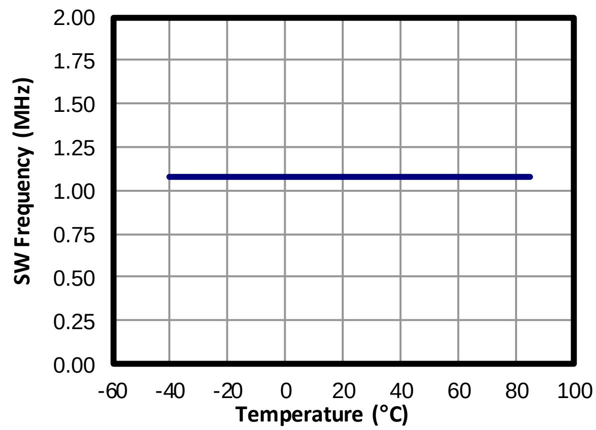
EN Rising and Falling Threshold vs. Temperature



V_{IN} Rising and Falling Threshold vs. Temperature



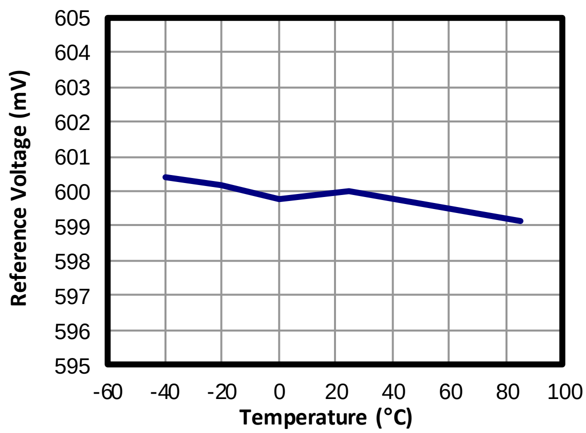
Switch Frequency vs. Temperature



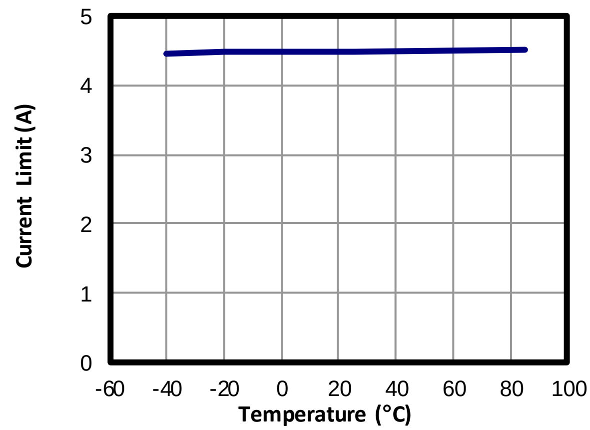
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

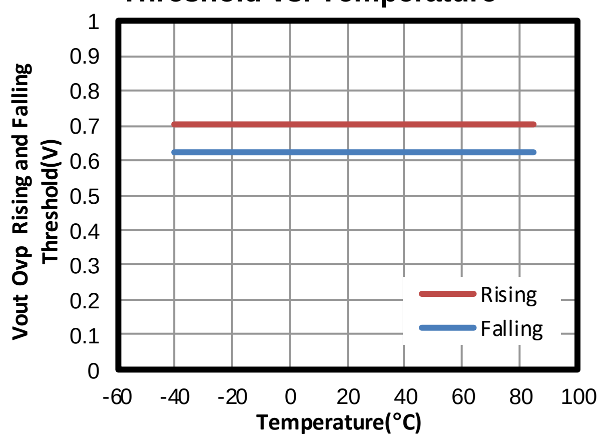
Reference Voltage vs. Temperature



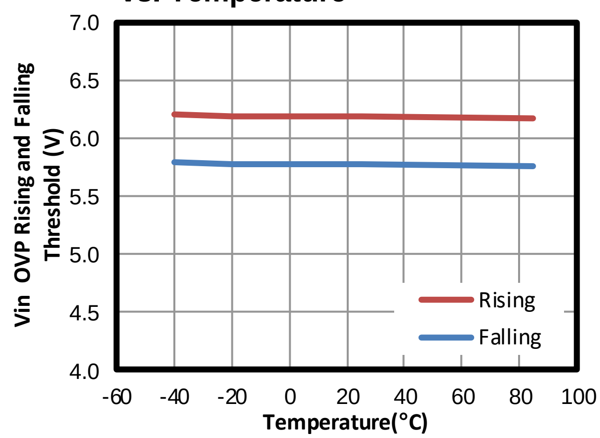
Peak Current Limit vs. Temperature



V_{OUT} OVP Rising and Falling Threshold vs. Temperature

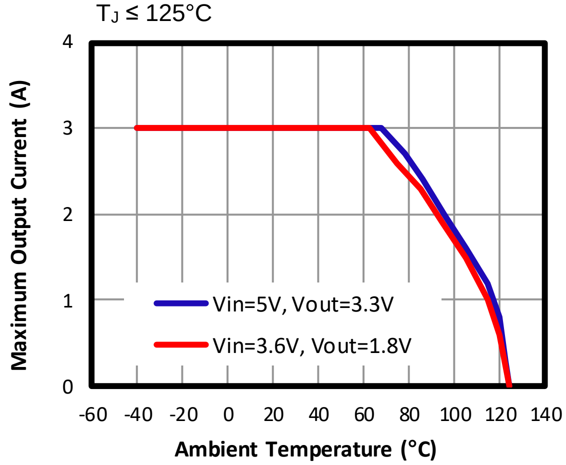


V_{IN} OVP Rising and Falling Threshold vs. Temperature



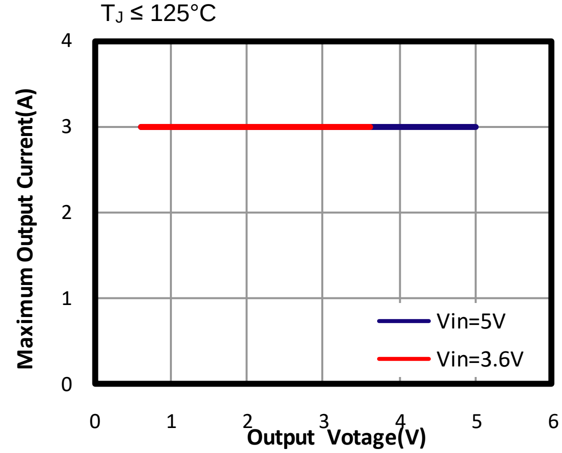
Output Current Derating vs. Ambient Temperature

T_J ≤ 125°C



Output Current Derating vs. Output Voltage

T_J ≤ 125°C



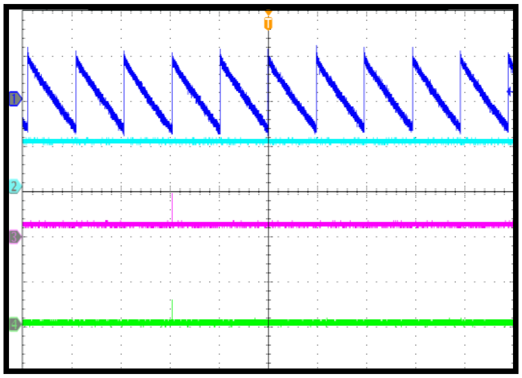
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 22μF, T_A = +25°C, unless otherwise noted.

Steady State

I_{OUT} = 0A

CH1: V_{OUT}/AC 20mV/div.
CH2: V_{IN} 5V/div.
CH3: V_{SW} 5V/div.
CH4: I_L 500mA/div.

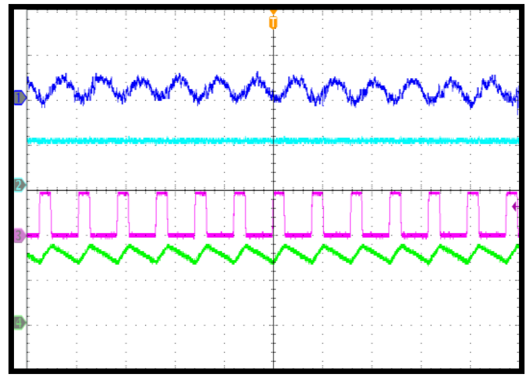


40ms/div.

Steady State

I_{OUT} = 3A

CH1: V_{OUT}/AC 10mV/div.
CH2: V_{IN} 5V/div.
CH3: V_{SW} 5V/div.
CH4: I_L 2A/div.

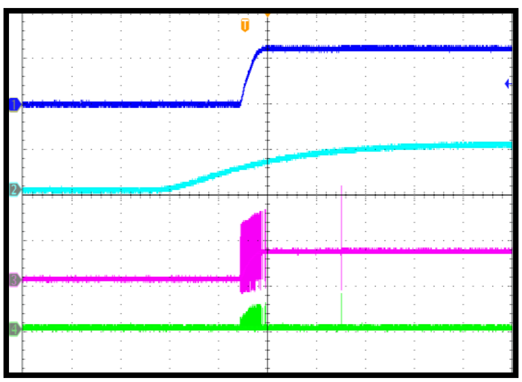


1μs/div.

V_{IN} Power-Up

I_{OUT} = 0A

CH1: V_{OUT} 1V/div.
CH2: V_{IN} 5V/div.
CH3: V_{SW} 2V/div.
CH4: I_L 1A/div.

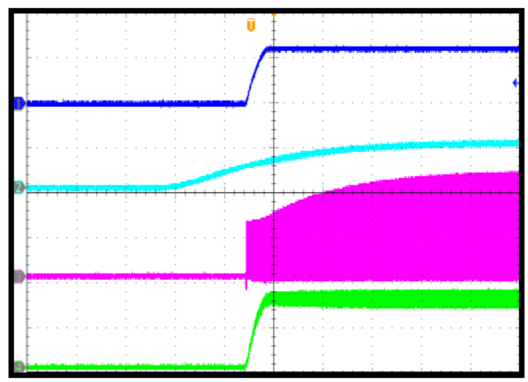


2ms/div.

V_{IN} Power-Up

I_{OUT} = 3A

CH1: V_{OUT} 1V/div.
CH2: V_{IN} 5V/div.
CH3: V_{SW} 2V/div.
CH4: I_L 2A/div.

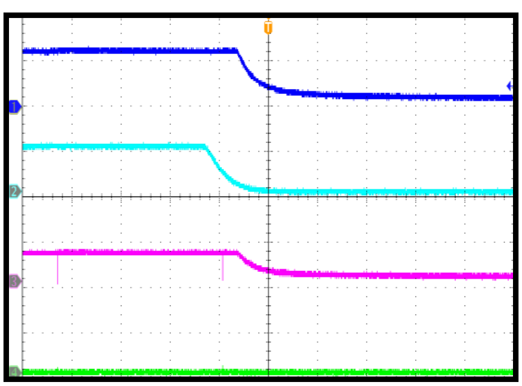


2ms/div.

V_{IN} Shutdown

I_{OUT} = 0A

CH1: V_{OUT} 1V/div.
CH2: V_{IN} 5V/div.
CH3: V_{SW} 2V/div.
CH4: I_L 2A/div.

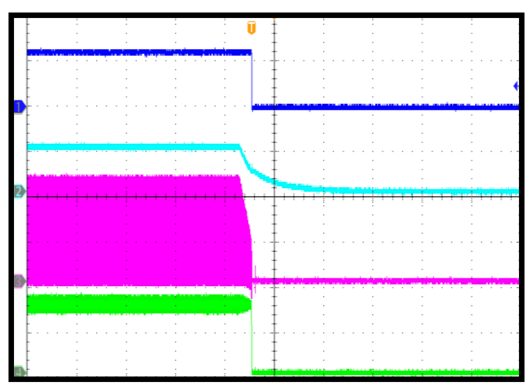


10ms/div.

V_{IN} Shutdown

I_{OUT} = 3A

CH1: V_{OUT} 1V/div.
CH2: V_{IN} 5V/div.
CH3: V_{SW} 2V/div.
CH4: I_L 2A/div.



2ms/div.

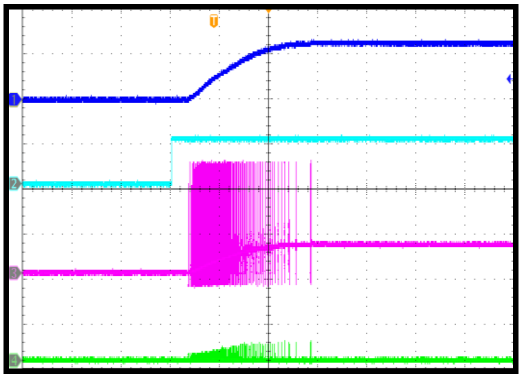
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

EN Power-Up

I_{OUT} = 0A

CH1: V_{OUT} 1V/div.
CH2: V_{EN} 5V/div.
CH3: V_{SW} 2V/div.
CH4: I_L 2A/div.

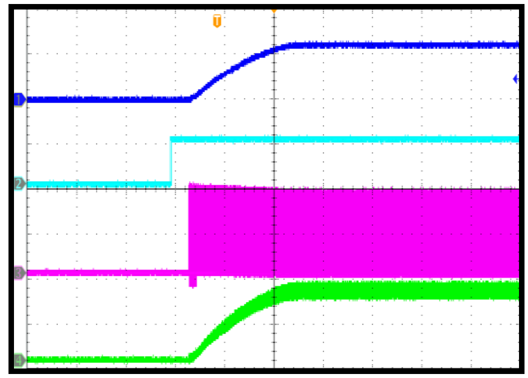


400µs/div.

EN Power-Up

I_{OUT} = 3A

CH1: V_{OUT} 1V/div.
CH2: V_{EN} 5V/div.
CH3: V_{SW} 2V/div.
CH4: I_L 2A/div.

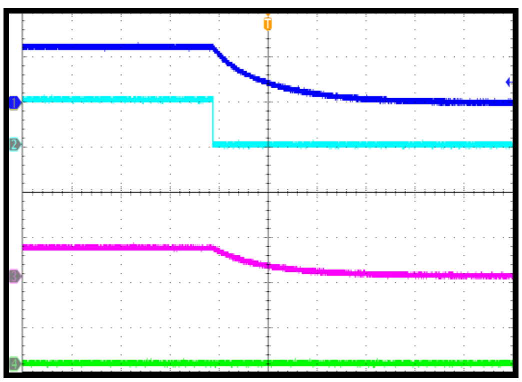


400µs/div.

EN Shutdown

I_{OUT} = 0A

CH1: V_{OUT} 1V/div.
CH2: V_{EN} 5V/div.
CH3: V_{SW} 2V/div.
CH4: I_L 2A/div.

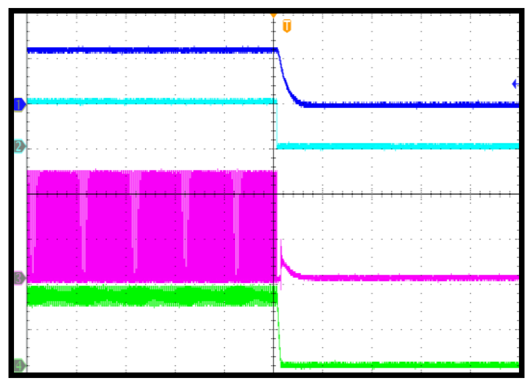


4ms/div.

EN Shutdown

I_{OUT} = 3A

CH1: V_{OUT} 1V/div.
CH2: V_{EN} 5V/div.
CH3: V_{SW} 2V/div.
CH4: I_L 2A/div.

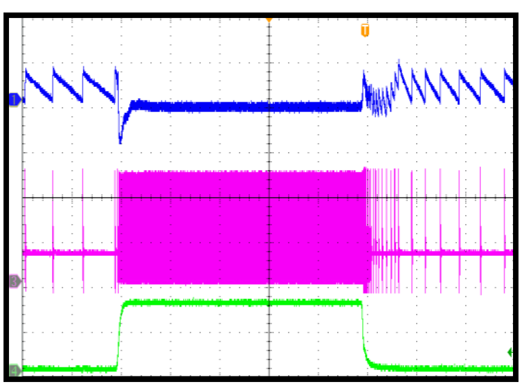


40µs/div.

Load Transient

I_{OUT} = 0 - 1.5A, 1A/µs

CH1: V_{OUT}/AC 50mV/div.
CH3: V_{SW} 2V/div.
CH4: I_{OUT} 1A/div.

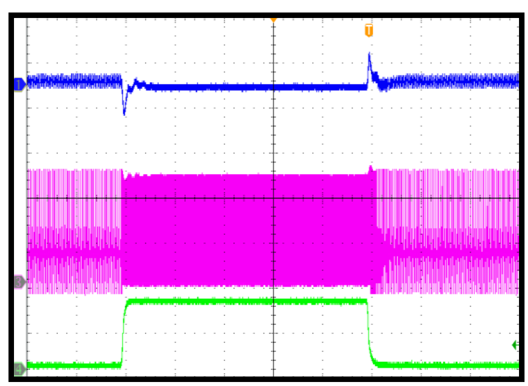


100µs/div.

Load Transient

I_{OUT} = 0.1 - 3A, 1A/µs

CH1: V_{OUT}/AC 100mV/div.
CH3: V_{SW} 2V/div.
CH4: I_{OUT} 2A/div.

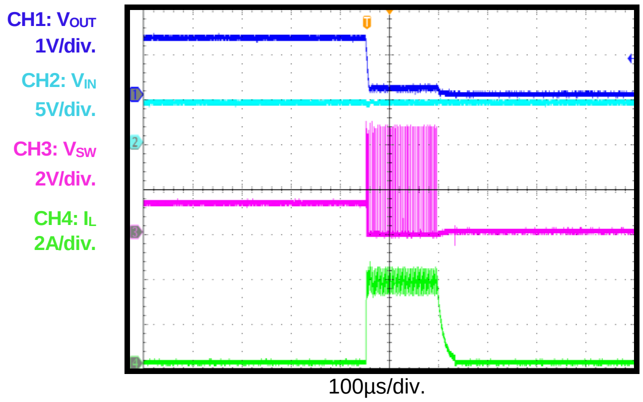


100µs/div.

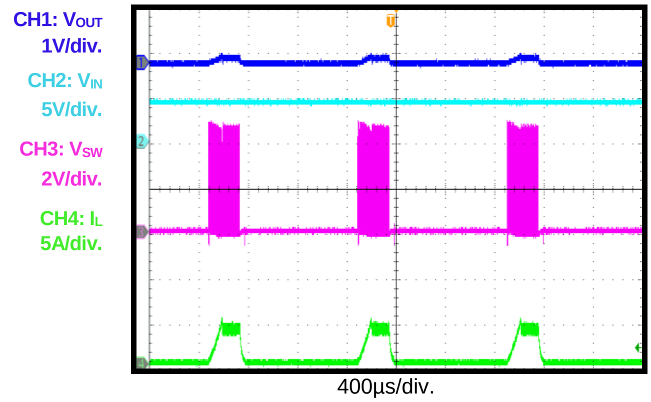
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

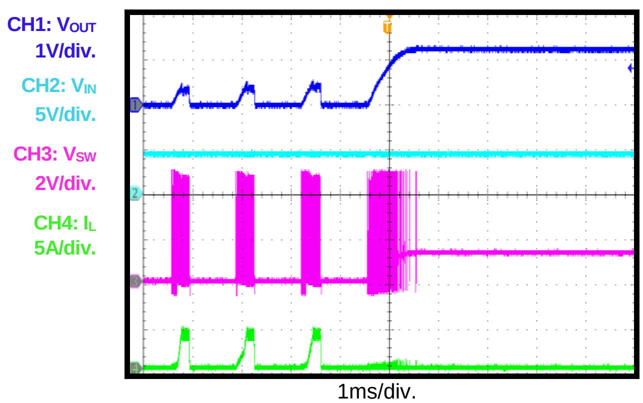
Short-Circuit Entry



Short-Circuit State



Short-Circuit Recovery



BLOCK DIAGRAM

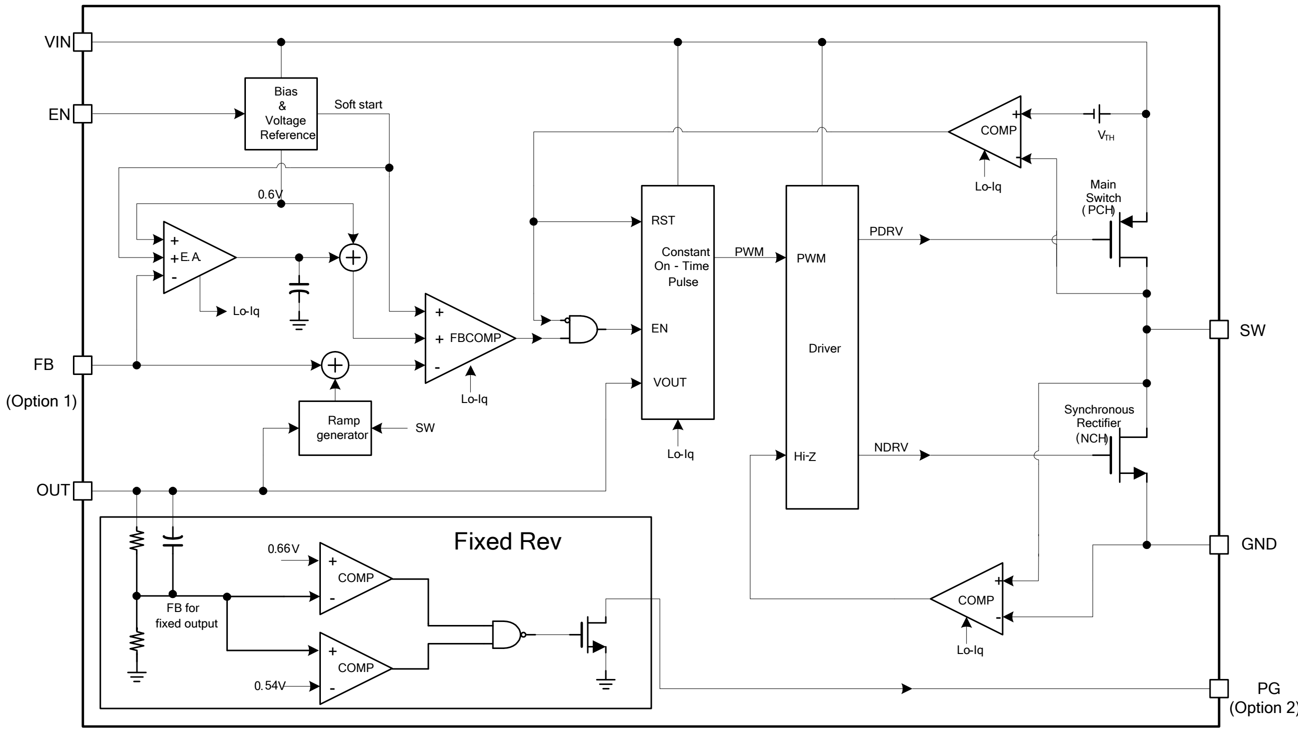


Figure 1: Functional Block Diagram

Option 1: FB pin is only for MP2153XXX

Option 2: PG pin is only for MP2153XXX-XX

OPERATION

The MP2153 uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency over the entire input range. The MP2153 achieves 3A of continuous output current from a 2.5V to 5.5V input voltage range with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

Constant-On-Time (COT) Control

Compared to fixed frequency pulse-width modulation (PWM) control, COT control offers a simpler control loop and faster transient response. By using input voltage feed-forward, the MP2153 maintains a fairly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.91us \qquad (1)$$

To prevent inductor current runaway during the load transient, the MP2153 has a fixed minimum off time of 100ns.

Sleep Mode Operation

The MP2153 features sleep mode to achieve high efficiency at extremely light loads. In sleep mode, all of the circuit blocks, except the error amplifier and PWM comparator, are turned off. Therefore, the operation current is reduced to a minimal value (see Figure 2).

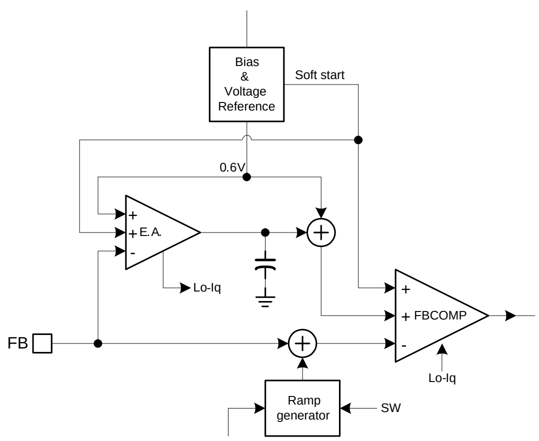


Figure 2: Operation Blocks at Sleep Mode

When the load becomes lighter, the ripple of the output voltage increases and drives the error amplifier output (EAO) lower. When the EAO reaches an internal low threshold, it is clamped at that level, and the MP2153 enters sleep mode. During sleep mode, the valley of the FB voltage (V_{FB}) is regulated to the internal reference voltage (V_{REF}). Therefore, the average output voltage is slightly higher than the output voltage at discontinuous conduction mode (DCM) or continuous conduction mode (CCM). The on-time pulse at sleep mode is slightly larger than that in DCM or CCM. Figure 3 shows the average V_{FB} relationship with the internal reference at sleep mode.

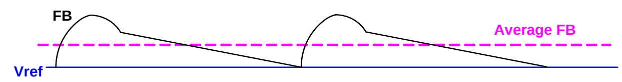


Figure 3: FB Average Voltage at Sleep Mode

When the MP2153 is in sleep mode, the average output voltage is higher than the internal reference voltage. The EAO is kept low and clamped in sleep mode. When the load increases, the PWM switching period decreases to keep the output voltage regulated, and the output voltage ripple decreases relatively. Once the EAO is higher than the internal low threshold, the MP2153 exits sleep mode and enters either DCM or CCM, depending on the load. In DCM or CCM, the EA regulates the average output voltage to the internal reference (see Figure 4).

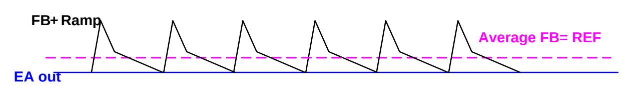


Figure 4: DCM Control

There is always a loading hysteresis when entering and exiting sleep mode due to the error amplifier clamping response time.

AAM Operation at Light-Load Operation

The MP2153 enters advanced asynchronous modulation (AAM) power-save mode when the zero-current cross detection (ZCD) is triggered during light-load condition (see Figure 5).

The AAM current (I_{AAM}) is set internally. The SW on pulse time is decided by either the on-time generator or AAM comparator. The on time is determined by the longer value between the two. If the AAM comparator pulse is longer than the on-time generator, the on time is determined by the AAM comparator (see Figure 6).

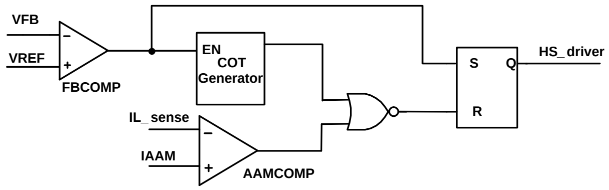


Figure 5: Simplified AAM Control Logic

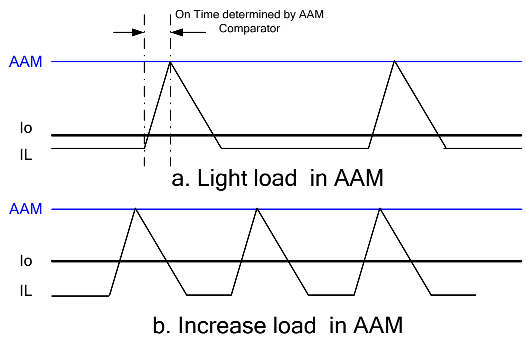


Figure 6: AAM Comparator Control T_{ON}

If the AAM comparator pulse is shorter than the on-time generator, the operation mode is as shown in Figure 7.

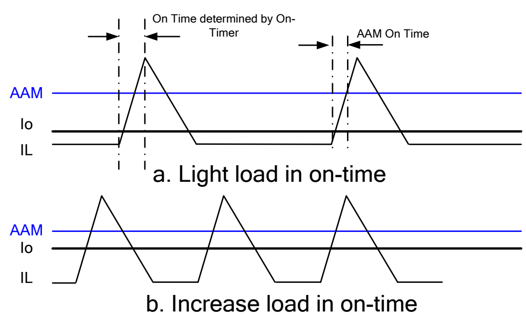


Figure 7: On-Time Control T_{ON}

Figure 8 shows the AAM threshold decreasing as T_{ON} increases gradually. The load current needs more than half of the AAM threshold to enter CCM.

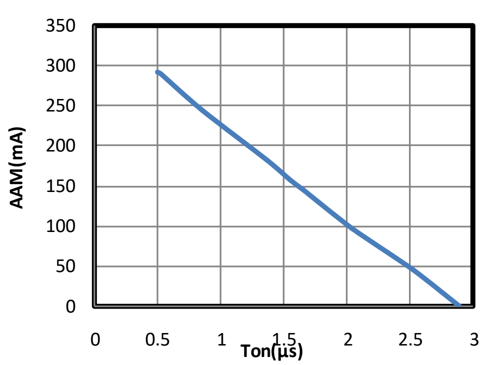


Figure 8: AAM Threshold Decreasing as T_{ON} Increases

It is recommended to design the inductor peak-to-peak current to be higher than the AAM threshold. The MP2153 has a ZCD to determine when the inductor current begins to reverse. When the inductor current reaches the ZCD threshold, the low-side switch turns off.

AAM mode and the ZCD circuit together make the MP2153 work in DCM continuously, even for large duty cycle applications.

Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.3V), the MP2153 can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to ground to disable the MP2153. There is an internal 1MΩ resistor from EN to ground.

When the device is disabled, the MP2153 enters output discharge mode automatically. Its internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft Start (SS)

The MP2153 has a built-in soft start that ramps up the output voltage at a controlled slew rate to prevent an overshoot during start-up. The soft-start time is about 0.5ms, typically.

Current Limit

The MP2153 has a minimum 4A high-side switch current limit. When the high-side switch reaches its current limit, the MP2153 remains in hiccup mode until the current drops. This prevents the inductor current from continuing to rise and damaging components.

Short Circuit and Recovery

The MP2153 enters short-circuit protection (SCP) mode when it reaches the current limit and attempts to recover with hiccup mode. The MP2153 disables the output power stage, discharges the internal soft-start capacitor, and then attempts to soft start again automatically. If the short-circuit condition remains after the soft start ends, the MP2153 repeats this cycle until the short circuit disappears and the output rises back to the regulation level.

Over-Voltage Protection (V_{OUT} OVP)

The MP2153 monitors the feedback voltage to detect a possible output over-voltage event. When the V_{FB} rises above 115% of the regulation voltage, the MP2153 enters a dynamic regulation period. During this period, the low-side switch is forced to turn on until the low-side current drops to -1.5A. The current discharges the output voltage and attempts to pull it down to the normal regulation range.

If the over-voltage condition persists, the low-side switch turns on again after a 1µs delay. The MP2153 exits this mode when the V_{FB} drops below 105% of the V_{REF}. If the dynamic regulation cannot reduce the over-voltage condition, and the input rises above the 6.1V input over-voltage protection (OVP) threshold at the same time, the MP2153 stops switching until the input voltage drops below 5.7V. The MP2153 then resumes operation.

Power Good Indicator (only for MP2153XXX-XX)

The MP2153XXX-XX has an open-drain output and requires an external pull-up resistor (100 ~ 500kΩ) for power good (PG) indication. When the V_{FB} is within -10% / +15% of the regulation voltage, the PG voltage (V_{PG}) is pulled up to V_{OUT}/V_{IN} by the external resistor. If the V_{FB} exceeds this window, the internal MOSFET pulls PG to ground. The MOSFET has a maximum $R_{DS(ON)}$ of less than 400Ω.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application Circuit shown in Figure 11). Select a feedback resistor (R1) that will reduce the V_{OUT} leakage current (typically between 100 - 200kΩ). There is no strict requirement on the feedback resistor. An R1 value higher than 10kΩ is reasonable for most applications. Then determine R2 with Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \tag{2}$$

Figure 9 shows the feedback circuit.

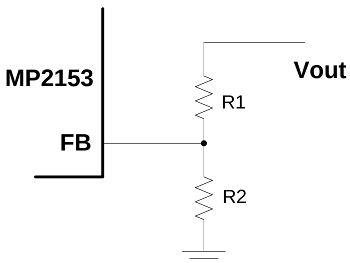


Figure 9: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Inductor

Most applications work best with a 1 - 2.2µH inductor. Select an inductor with a DC resistance less than 50mΩ to optimize efficiency.

High-frequency, switch-mode power supplies with a magnetic device have strong, electronic, magnetic system inference. Unshielded power inductors are not recommended due to poor magnetic shielding. Shield inductors, such as
For simplification, choose an input capacitor with an RMS current rating greater than half of

metal alloy or multiplayer chip power, are recommended for applications since they can decrease influence effectively. Table 2 lists some recommended inductors.

Table 2: Recommended Inductor List

Manufacturer P/N	Inductance (µH)	Manufacturer
PIFE25201B-1R0MS	1.0	CYNTEC CO. LTD.
74437324010	1.0	Wurth

For most designs, estimate the inductance value with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \tag{3}$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current that is approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \tag{4}$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Low ESR ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient. Higher output voltages may require a 44µF capacitor to increase system stability.

The input capacitor absorbs the input switching current and requires an adequate ripple current rating. Estimate the RMS current in the input capacitor with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{5}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \tag{6}$$

the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1μF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{7}$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Low ESR ceramic capacitors are recommended for limiting the output voltage ripple. Estimate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \tag{8}$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\,2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{9}$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with (Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \tag{10}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high-frequency switching converter, a poor layout design could result in poor line or load regulation and stability issues. For best results, refer to Figure 10 and follow the guidelines below.

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to the VIN and GND pins as possible.
3. Place the external feedback resistors next to the FB pin.
4. Keep the switching node (SW) short and away from the feedback network.
5. Keep the VOUT sense line as short as possible or away from the power inductor, especially the surrounding inductor.

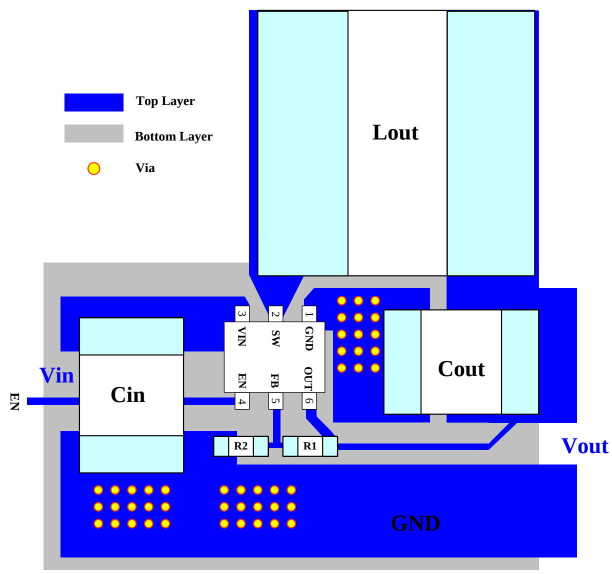


Figure 10: Recommended Layout for MP2153GTF

TYPICAL APPLICATION CIRCUITS

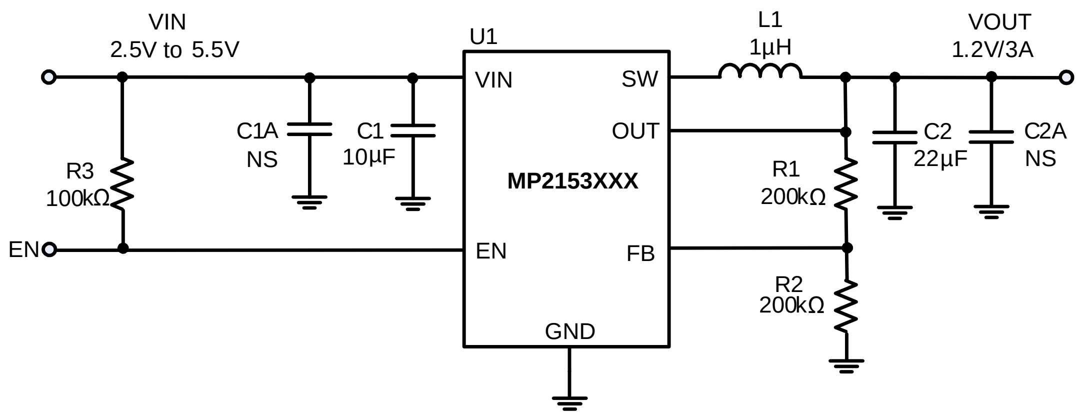


Figure 11: Typical Application Circuit for MP2153XXX
NOTE: VIN < 3.3V applications may require more input capacitors.

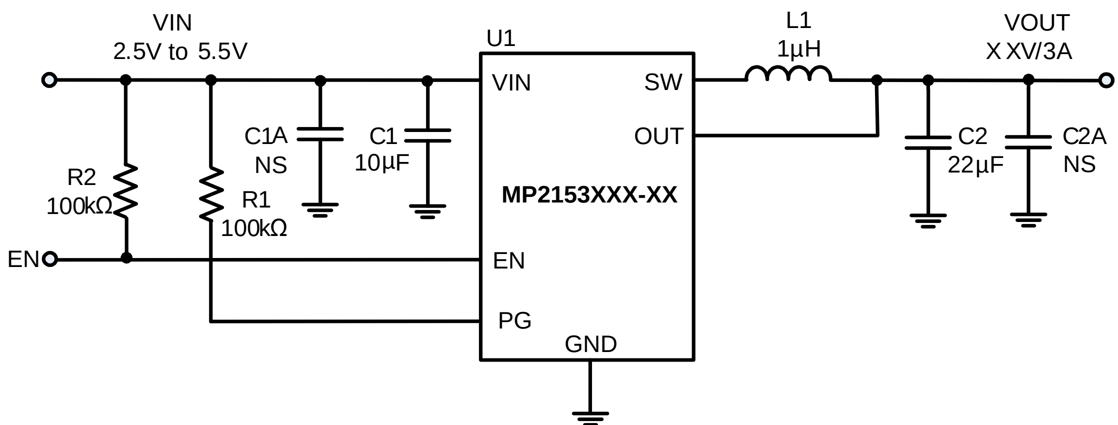
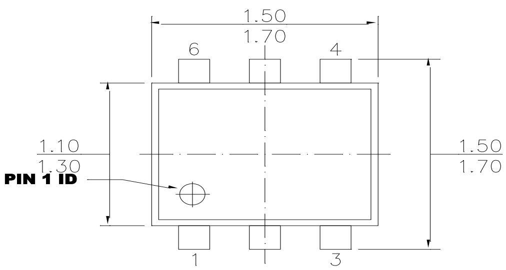


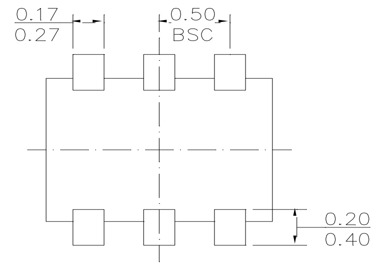
Figure 12: Typical Application Circuit for MP2153XXX-XX
NOTE: VIN < 3.3V applications may require more input capacitors.

PACKAGE INFORMATION

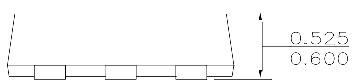
SOT563 (1.6mmx1.6mm)



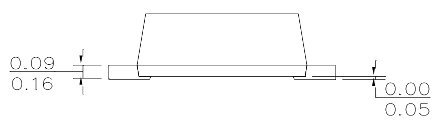
TOP VIEW



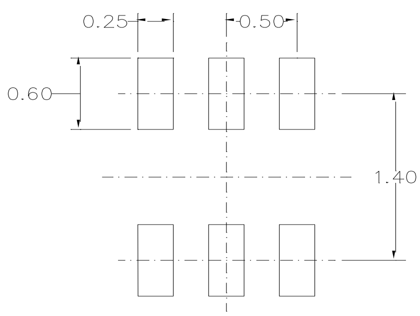
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



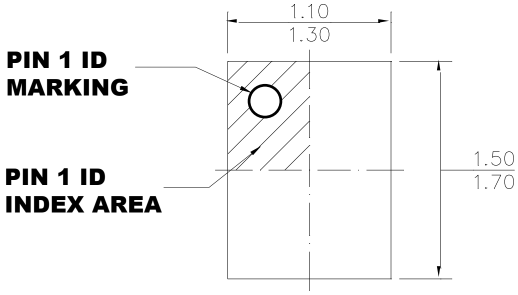
RECOMMENDED LAND PATTERN

NOTE:

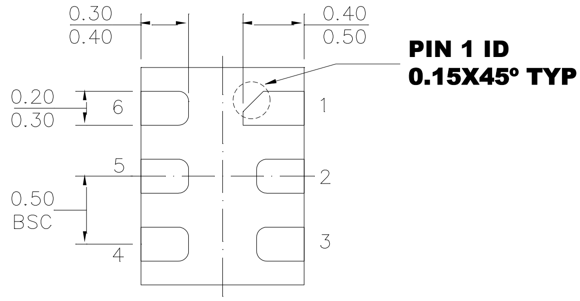
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

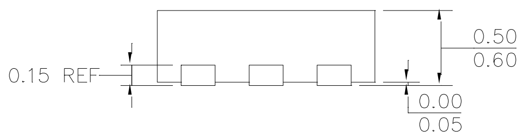
UTQFN-6 (1.2mmx1.6mm)



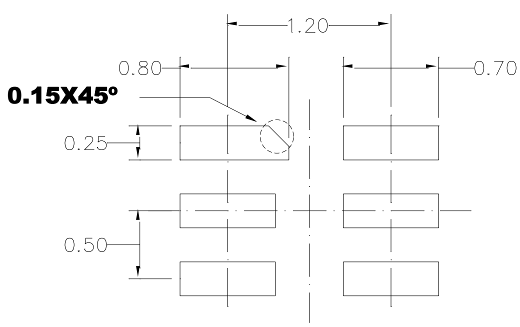
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.