# MP2040

## Fast Transient Response, 3A Dual Supply Very Low Dropout Linear Regulator

## DESCRIPTION

The MP2040 is a very low dropout, dual supply linear regulator. The use of two supplies allows the BIAS to control an NMOS device. The NMOS device supplies power to the load via the IN. In this way the input supply can be just above the desired output, yet still provide very good regulation performance due to the higher bias supply. The BIAS operates from a 3.3V to 5.5V input and regulates the output voltage to as low as 0.9V, and as high as 3.3V.

The MP2040 can supply up to 3A of load current with a typical dropout voltage of 150mV. The BIAS runs the internal reference and drive circuitry, while the output current comes directly from the IN for high efficiency regulation.

Other features of MP2040 include thermal overload and current limit protection, power good indicator, stability with ultra low ESR ceramic capacitors as low as 1uF, and fast transient response. The MP2040 is available in 10-pin QFN (3mm x 3mm), and in QFN (5mm x 5mm) packages.

## FEATURES

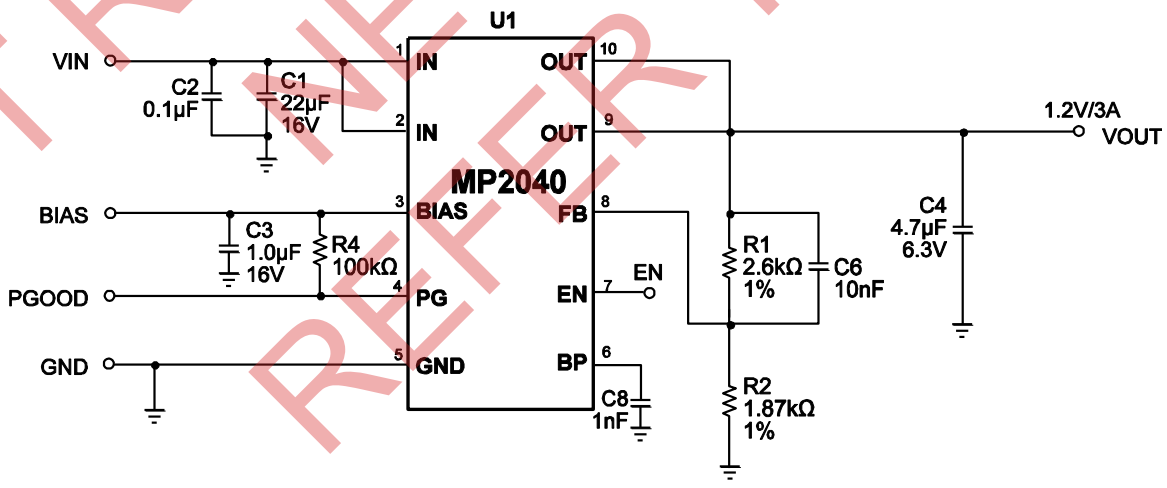
- Wide 1.1V to 5V Input Voltage Range
- Stable with Very Small Ceramic Capacitors
- 150mV Dropout at 3A Output
- 2% Accurate Output Voltage
- Adjustable Output Range of 0.9V to 3.3V
- Low Noise: 80$\mu V_{RMS}$ (10Hz to 100kHz)
- Very fast transient response
- PSRR
  - 40dB at 100kHz
- Better Than 0.001%/mA Load Regulation
- Stable With Low-ESR Output Capacitors
- Internal Thermal Protection
- Current Limit Protection
- 0.1µA Typical Quiescent Current at Shutdown
- Power Good Indicator

## APPLICATIONS

- Industrial Process & Control Equipment
- Telecom Equipment
- PAID Storage
- DSP/ASIC/µC Post Regulation for Switching Power Supplies



## TYPICAL APPLICATION

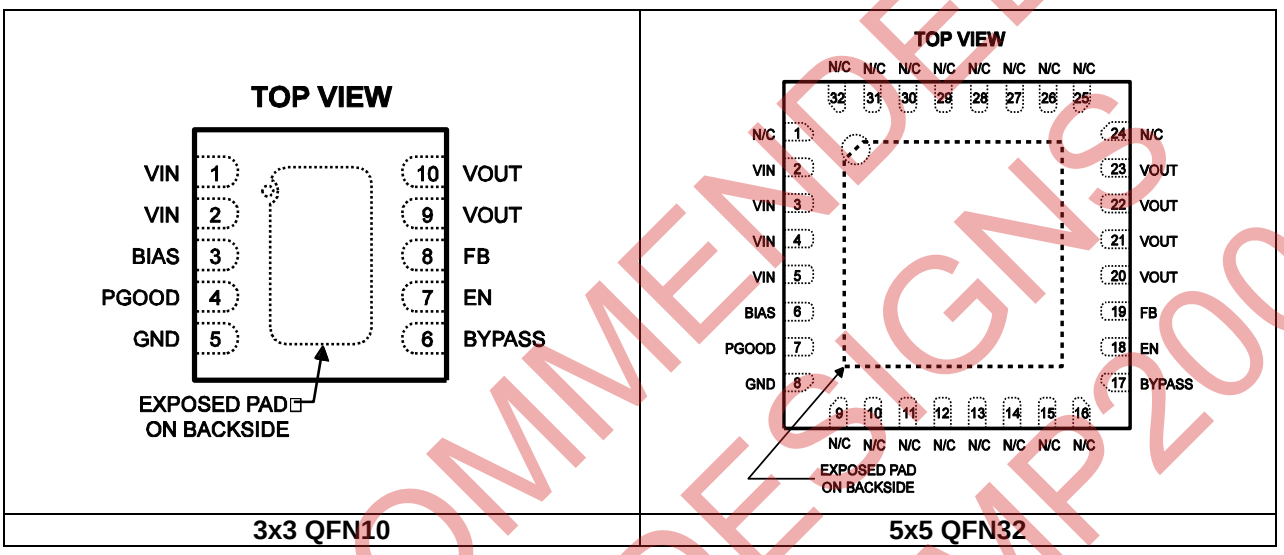


## ORDERING INFORMATION

| Part Number | Package | Top Marking | Free Air Temperature ($T_A$) |
|---|---|---|---|
| MP2040DQ* | 3x3 QFN10 | 8H | -40°C to +85°C |
| MP2040DU** | 5x5 QFN32 | MP2040DU | -40°C to +85°C |

* For Tape & Reel, add suffix –Z (e.g. MP2040DQ–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP2040DQ–LF–Z)
** For Tape & Reel, add suffix –Z (e.g. MP2040DU–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP2040DU–LF–Z)

## PACKAGE REFERENCE




3x3 QFN10 | 5x5 QFN32

## ABSOLUTE MAXIMUM RATINGS (1)

$V_{BIAS}$, $V_{IN}$ to GND ..... -0.3V to +6V
FB, EN, to GND ..... -0.3V to 6V
$V_{OUT}$ ..... -0.3V to $V_{IN}$ + 0.3 or 6V
PGOOD ..... -0.3V to $V_{BIAS}$ + 0.3 or 6V
BYPASS ..... -0.3V to $V_{BIAS}$ +0.3 or 6V
Continuous Power Dissipation ($T_A$ = +25°C) (2)
QFN10 3X3 ..... 2.5W
QFN32 5X5 ..... 3.47W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

## *Recommended Operating Conditions* (3)

Input Voltage $V_{IN}$ ..... 1.1V to 5.5V
Input Voltage $V_{BIAS}$ ..... 3.3V to 5.5V
Output Voltage ..... 0.9V to 3.3V
Load Current ..... 3.0A Maximum
Operating Junct. Temp ($T_J$) ..... -40°C to +125°C

## *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

QFN10 3X3 ..... 50 ..... 12 °C/W
QFN32 5X5 ..... 36 ..... 8 °C/W

**Notes:**
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 1.5V, $V_{BIAS}$ = 3.6V, $V_{OUT}$ = 1.2V, $C_{OUT}$ = 1µF, $C_{IN}$ = 0.1µF, $T_A$ = +25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ Operating Voltage | | | 1.1 | | 5.5 | V |
| $V_{BIAS}$ Operating Voltage | | $I_{OUT}$ = 2A | 3.3 | | 5.5 | V |
| $V_{BIAS}$ Operating Current | | | | 3.5 | | mA |
| FB Regulation Voltage | | | 0.5 | 0.51 | 0.52 | V |
| | | -40°C ≤ $T_A$ ≤ +85°C | 0.495 | 0.51 | 0.525 | |
| Dropout Voltage | | $I_{OUT}$ = 3A, $V_{BIAS}$ = 3.6V | | 150 | | mV |
| $V_{IN}$ Line Regulation | | $I_{OUT}$ = 1mA,<br>$V_{IN}$ = 1.5 to 5V<br>$V_{BIAS}$ = 5V $V_{OUT}$ = 1.2V | | 1 | | mV |
| $V_{BIAS}$ Line Regulation | | $I_{OUT}$ = 1mA,<br>$V_{BIAS}$ = 3.6V to 5.5V $V_{OUT}$ = 1.2V<br>$V_{IN}$ = 1.5V | | 2 | | mV |
| Load Regulation | | $I_{OUT}$ = 1mA to 1A | | 0.001 | | %/mA |
| PSRR ($V_{IN}$) | | $V_{IN}$ > $V_{OUT}$ + 0.5V, $C_{OUT}$ = 4.7µF,<br>$V_{IN}$(AC) = 100mV, f = 100kHz<br>$V_B$=5V | | 40 | | dB |
| Power Good Threshold | | | | 440 | | mV |
| Power Good Delay | | | | 80 | | µs |
| Current Limit (5) | | | | 3.6 | | A |
| Soft Start | | BYPASS=open | | 280 | | µs |
| Power Good Voltage | | $I_{sink}$=230µA | | 0.39 | | V |
| EN Input High Voltage | | | 1.5 | | | V |
| EN Input Low Voltage | | | | | 0.8 | V |
| EN Input Bias Current | | $V_{EN}$ = 1.2V | –1 | | +1 | µA |
| Thermal Protection | | | | 135 | | °C |
| Thermal Protection Hysteresis | | | | 15 | | °C |

**Notes:**

5) Guaranteed by Designer.

## PIN FUNCTIONS

### QFN3X3 10pins

| Pin # | Name | Description |
|---|---|---|
| 9, 10 | VOUT | Regulator Output. OUT is the output of the linear regulator, By pass OUT to GND with a 4.7μF or greater capacitor. |
| 3 | BIAS | Bias Voltage. Bypass to ground with a 1μF or greater capacitor, VB>=VIN. |
| 8 | FB | Feedback Input. Connect a resistive voltage divider from OUT to FB to set the output voltage. OUT feedback threshold is 0.51V. |
| 7 | EN | Enable Input. Drive EN high to turn on the MP2040, drive EN low to turn it off. For automatic startup, connect EN to IN. |
| 5 | GND | Ground, exposed pad. |
| 1, 2 | VIN | Power Source Input. IN supplies power to the load at the output (through the power transistor). Bypass IN to GND with a 1μF or greater capacitor. |
| 4 | PGOOD | Open drain output. High indicated $V_{OUT}$> **90%** final value. |
| 6 | BYPASS | Connect a 1nF to this pin. Do not load this pin resistively. |

### QFN5x5 32pins

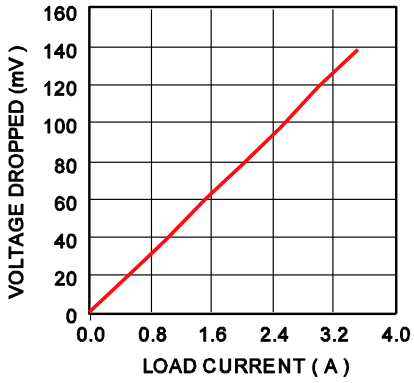
| Pin # | Name | Description |
|---|---|---|
| 20, 21,22, 23 | VOUT | Regulator Output. OUT is the output of the linear regulator, By pass OUT to GND with a 4.7μF or greater capacitor. |
| 6 | BIAS | Bias Voltage. Bypass to ground with a 1μF or greater capacitor, VB>=VIN. |
| 19 | FB | Feedback Input. Connect a resistive voltage divider from OUT to FB to set the output voltage. OUT feedback threshold is 0.51V. |
| 18 | EN | Enable Input. Drive EN high to turn on the MP2040, drive EN low to turn it off. For automatic startup, connect EN to IN. |
| 8 | GND | Ground, exposed pad. |
| 2, 3, 4, 5 | VIN | Power Source Input. IN supplies power to the load at the output (through the power transistor). Bypass IN to GND with a 1μF or greater capacitor. |
| 7 | PGOOD | Open drain output. High indicated $V_{OUT}$> **90%** final value. |
| 17 | BYPASS | Connect a 1nF to this pin. Do not load this pin resistively. |
| 1, 9, 10, 11, 12, 13, 14, 15, 16, 24, 25, 26, 27, 28, 29, 30, 31, 32 | NC | These are no connection pins. |

## TYPICAL PERFORMANCE CHARACTERISTICS

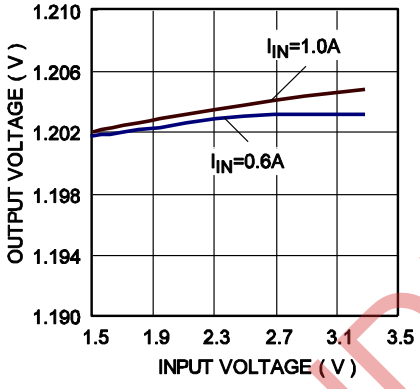
**C1=22µF, C2=0.1µF, C3=1.0µF, C4=4.7µF, C6=22nF, $V_B$=5V, $T_A$=25ºC, unless otherwise noted**

**Voltage Dropout**

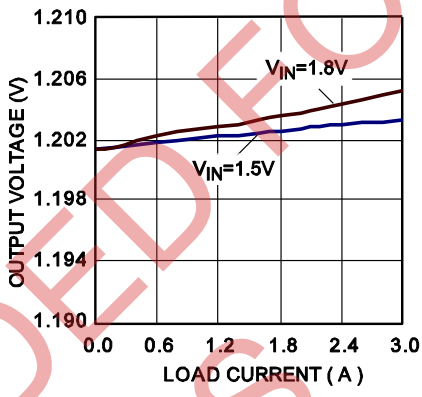
$V_{OUT}$=1.2V




**Line Regulation**

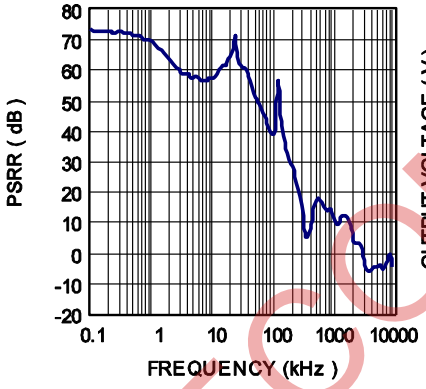



**Load Regulation**




**PSRR vs. Frequency**

$V_{IN}$=1.5V,$V_{OUT}$=1.2V

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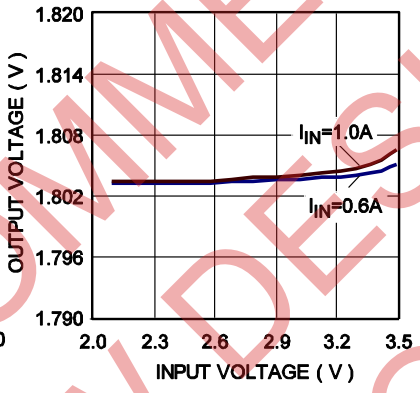
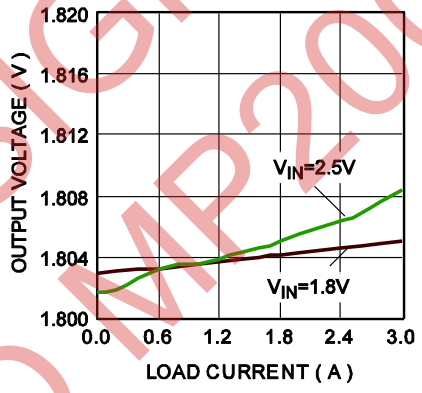
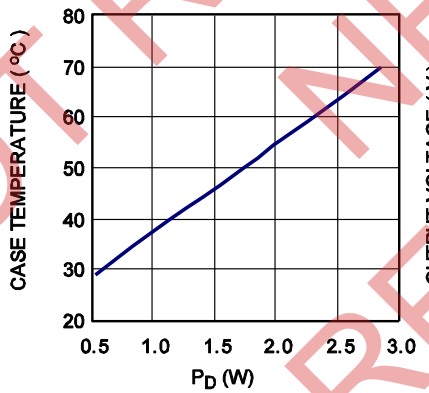



**Load Regulation**

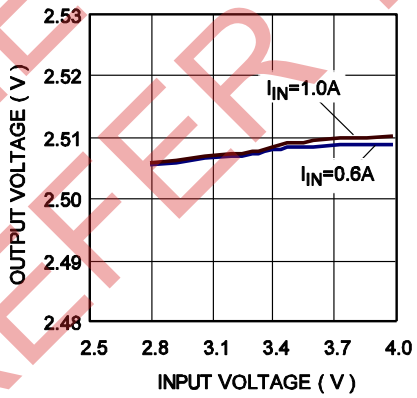



**MP2040DU Case Temperature vs. $P_D$**

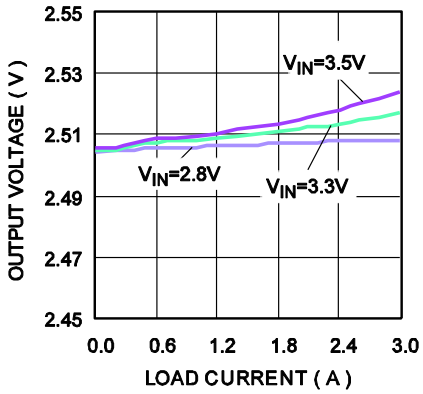
$V_B$=5V,$V_{OUT}$=1.2V




**Line Regulation**




**Load Regulation**

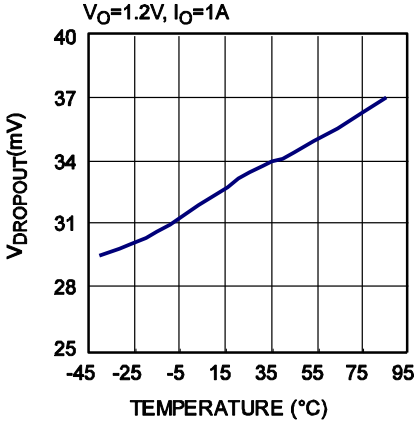


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**C1=22µF, C2=0.1µF, C3=1.0µF, C4=4.7µF, C6=22nF, $V_B$=5V, $T_A$=25ºC, unless otherwise noted**

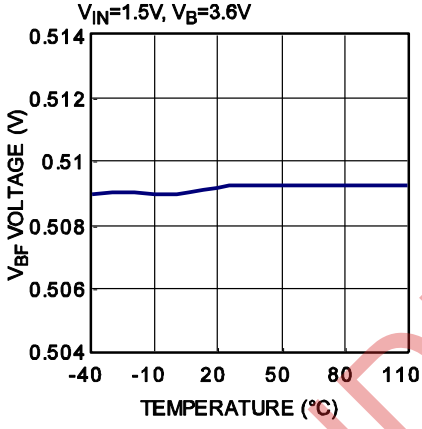
**$V_{DROPOUT}$ vs. Temperature**

$V_O$=1.2V, $I_O$=1A



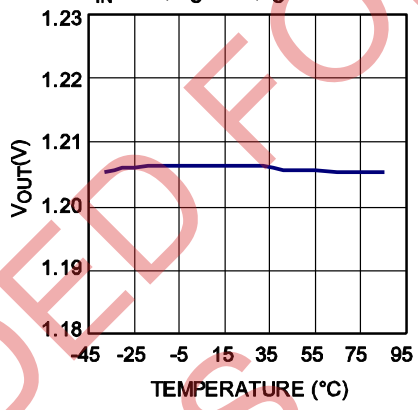

**$V_{BF}$ vs. Temperature**

$V_{IN}$=1.5V, $V_B$=3.6V



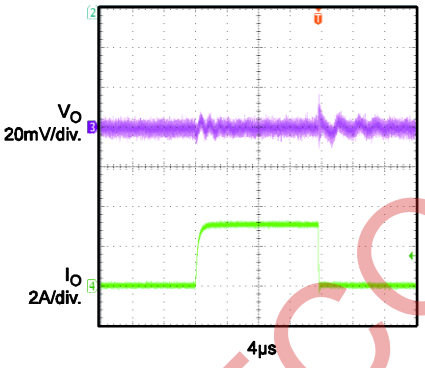

**$V_{OUT}$ vs. Temperature**

$V_{IN}$=1.5V, $V_O$=1.5V, $I_O$=1mA



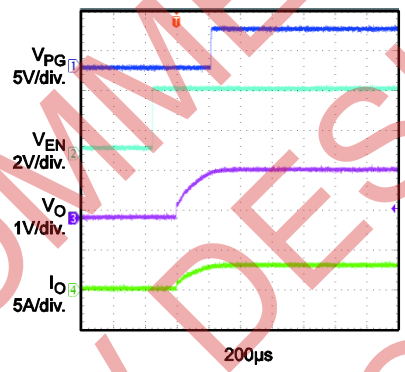

**Load Transient**

$V_{IN}$=1.9V, $V_O$=1.2V, $I_O$=0 to 3A



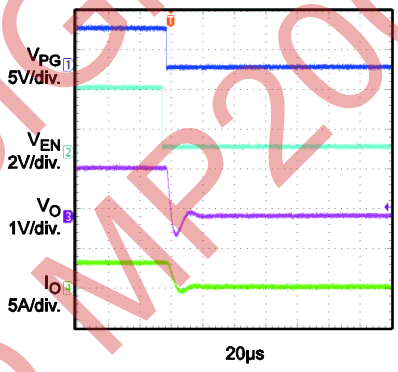

**Enable Turn ON**

$V_{IN}$=1.6V, $V_O$=1.2V,
$V_{EN}$=0V to 3V, $I_O$=3A



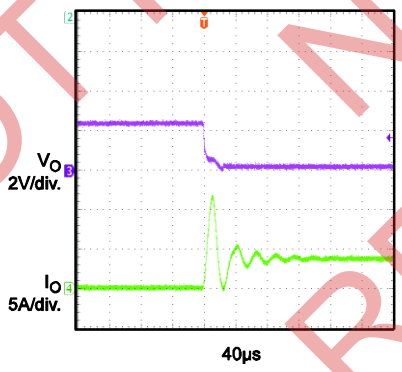

**Enable Turn Off**

$V_{IN}$=1.6V, $V_O$=1.2V,
$V_{EN}$=3V to 0V, $I_O$=3A



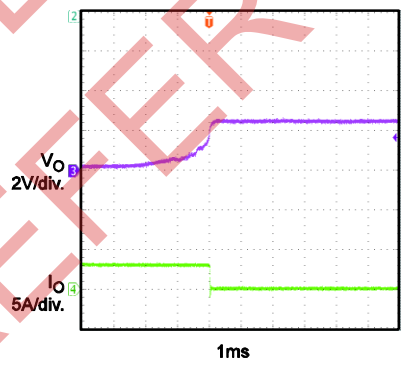

**Short Circuit**

$V_{IN}$=2.1V, $V_O$=1.2V



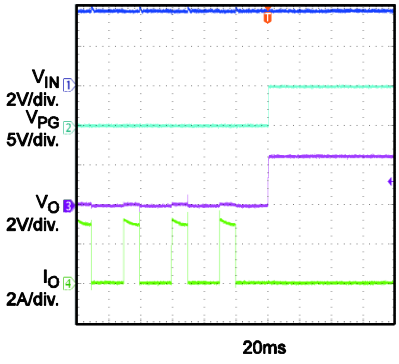

**Short Circuit Recovery**

$V_{IN}$=2.1V, $V_O$=1.2V




**Thermal Protection**

$V_{IN}$=3.8V, $V_O$=2.5V, $I_O$=3.6A

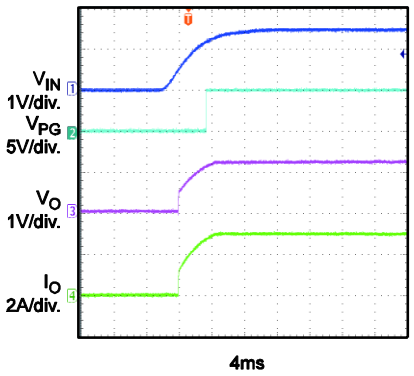


## TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

**C1=22µF, C2=0.1µF, C3=1.0µF, C4=4.7µF, C6=22nF, $V_B$=5V, $T_A$=25ºC, unless otherwise noted**

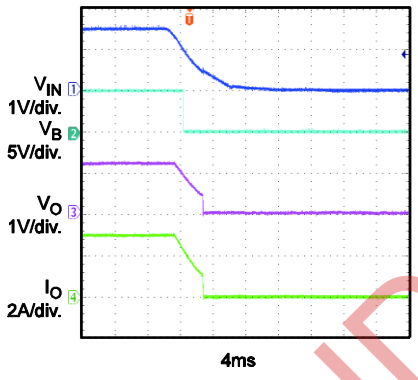
**Power Ramp Up**

$V_{IN}$=1.5V, $V_O$=1.2V, $I_O$=3A
with Resistor load



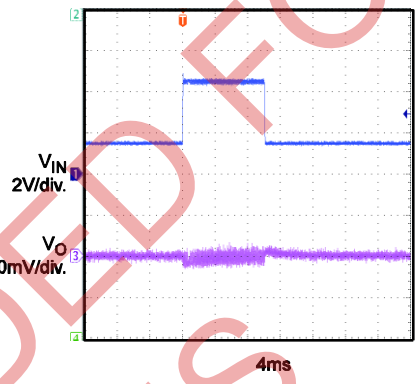

**Power Ramp Down**

$V_{IN}$=1.5V, $V_O$=1.2V, $I_O$=3A
with Resistor load




**Line Transient**

$V_{IN}$=1.5V to 4.5V, $V_O$=1.2V, $I_O$=0.4A



## BLOCK DIAGRAM

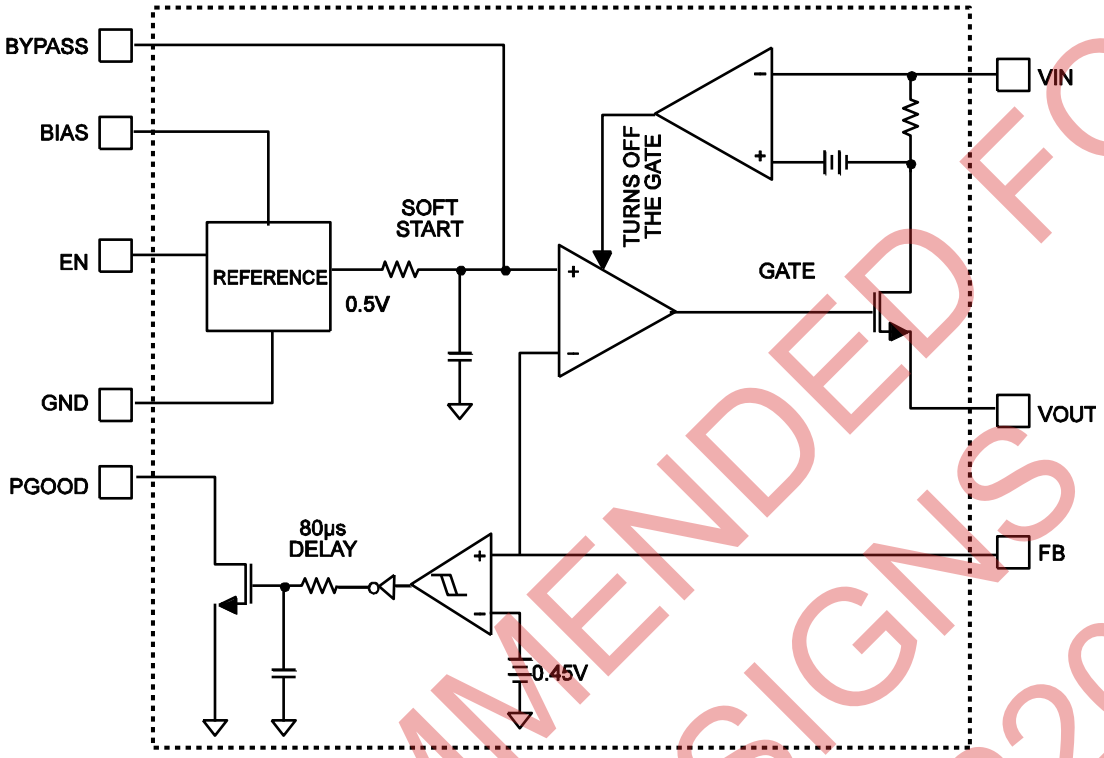



**Figure 1—Block Diagram of Low Dropout Regulator**

## OPERATION

### MP2040 Theory of Operation

The MP2040 linear dropout regulator provides adjustable output voltages from 0.9V to 3.3V at currents up to 3A. This LDO is protected against short circuits, and it has thermal shut down protection with 15°C hystheresis.

### Utilizing Two Power Supplies

In order to maximize the efficiency MP2040 uses two power supplies. One power supply is connected to the BIAS pin and it is used to power up the internal circuitries including band gap reference and the rest of control circuitries. The other power supply is connected to the VIN pins which are the drain of pass device. This power supply can be set close to output voltage of LDO. The output pins are the source of the pass device. The smaller voltage drop across the pass device translates to the smaller power loss in pass device. Thus, the part operates with higher efficiency.

### Internal Current Limit

The MP2040 has an internal current limit set at almost 3.8A. Internal current limit is very well controlled over process variations and ambient temperature.

### Enable

The enable (EN) pin is active high. The enable pin has a built-in hystheresis. If this pin is held below 0.8V then part shuts down and draws less than 1uA from $V_{BIAS}$ supply.

If not used then connect this pin to $V_{BIAS}$.

### Under Voltage Lockout

The Bias voltage is monitored by a circuit that prevents the LDO start up when the bias voltage is below 2.35V. This circuitry has an approximate hystheresis of 90mV.

**Soft Start**

MP2040 incorporates internal soft start function. This internal function reduces the start up current surge into the output capacitor. This allows the gradual built up of output voltage to its final set value. The internal soft start cap is held to ground if there is a fault condition. The fault conditions are UVLO, Thermal shut down, and disable. The internal soft start time is almost 280µ

**Power Good**

The Power Good pin is an open drain output and can be connected to Bias voltage via a pull up resistor. Open drain transistor turns off and PG pin voltage value becomes $V_{BIAS}$ when $V_{FB}$ exceeds 450mV. Also PG pin can sink at least 230µA while being low.

**Setting the Output Voltage**

The MP2040 has an adjustable output voltage, set by using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \times R_2/ (R_1+R_2)$$

Where $V_{FB}$ is the feedback threshold voltage ($V_{FB}$=0.5V), and $V_{OUT}$ is the output voltage. $R_1$ connects between $V_{OUT}$ and $V_{FB}$, and $R_2$ connects between $V_{FB}$ and ground.

Thus the output voltage is:

$$V_{OUT} = 0.5 \times (R_1+R_2)/R_2$$

$R_2$ can be as high as 100kΩ, but a typical value is 10kΩ. Using that value, $R_1$ is determined by:

$$R_1=R_2 \times (V_{OUT}-V_{FB})/V_{FB}$$

For example, for a 1.8V output voltage, $R_2$ is 10kΩ, and $R_1$ is 26kΩ. You can select 26kΩ (1%) resistor for $R_1$.

**Power Dissipation**

Most of the power dissipation is due to power dissipation in PASS device. For example, assume $V_{BIAS}$=5.0V, $V_{IN}$=2.0V, $V_{OUT}$=1.8V, and $I_{OUT}$=3A:

$$P_D\ (_{PASS}) = (V_{IN}-V_{OUT}) \times I_{OUT}$$

$$P_D\ (_{PASS}) = (2.0V-1.8V) \times 3A=0.6W$$

$P_{BIAS} = V_{BIAS} \times I_{GND}$= 5V x (220µA) = 1.25mW. This is negligible compared to $P_D\ (_{PASS})$ =0.6W

For QFN 3X3 $\theta_{JA}$ is 50°C/W.

0.6W power is dissipated when 3A output current goes through PASS device with $V_{IN}$=2.0V, and $V_{OUT}$=1.8V.

This gives a rise in die temperature for 0.6 x 50°C/W=30°CThis is a safe operating point assuming a junction temperature of 135°C at an 85°C ambient temperature.

A heat sink needs to be utilized for a better temperature performance.

## APPLICATION INFORMATION

### PG

The power good pin is an open drain output a pull up resistor (100kΩ recommended). The pull up resistor can be tied to a supply within the voltage range of the pin (0 to 5.5V). For example, the pull up resistor can be tied to the input voltage that is monitored by an IC powered from this input voltage. If the output voltage is 10% below its regulation point, the PG pin becomes low.

### Bypass Capacitors

For lower noise, the reference voltage can be bypassed by an external capacitor. A low ESR capacitor, such as the ceramic type, will provide the best performance.

It also can function as an external soft start, the soft start time;

$$Tss=1000 \times C_{BP}$$

### Performance Transient Response

For a 3A transient response, suggests increasing the input capacitance should be increased to 22µF or higher to get better performance. This will also avoid glitches on the PG pin due to excessive undershoot. Also increase the input voltage 0.4V above the $V_{OUT}$, to improve the load transient response.

### Maximum Output Voltage and Load Current

If the $V_{OUT}$ is set to 3.3V then the maximum output current will be decreased to 2.5A. The maximum bias voltage limits the $V_{OUT}$. $V_{OUT}$ must be at least 2.5V less than $V_B$;

$$V_{OUT}=V_B -2.5V$$

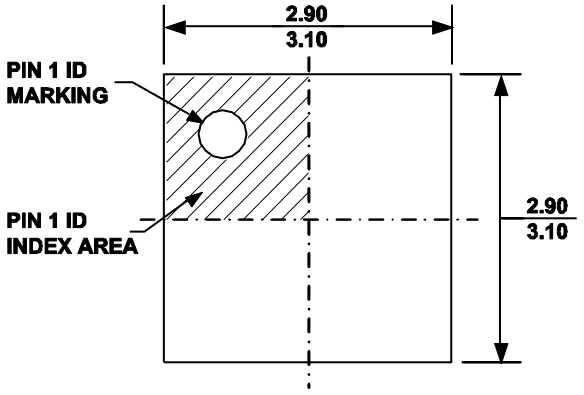
### Bias Input Voltage

The bias input is designed for low drop application. The bias pin must be at least 3.3V,

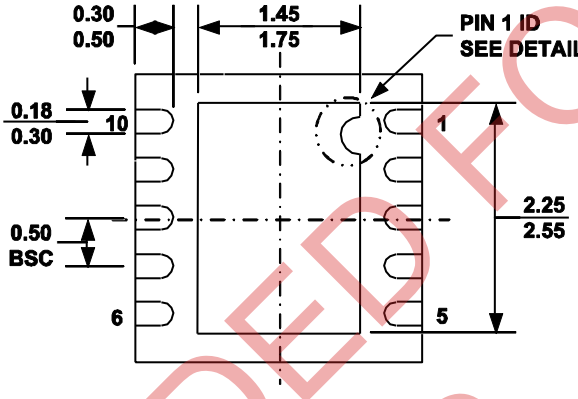
and at least 2.5V higher than the output voltage. If the $V_{IN}$ supply voltage meets these requirements, the bias pin can be tied to $V_{IN}$.

## PACKAGE INFORMATION

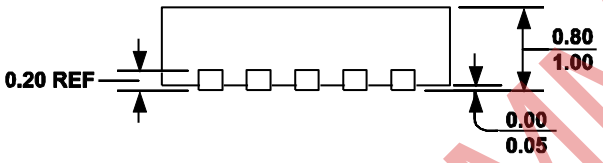
### QFN10 (3mm x 3mm)



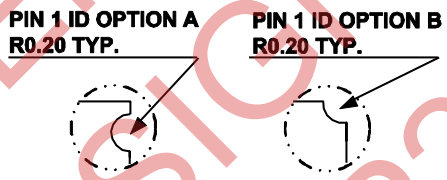

TOP VIEW



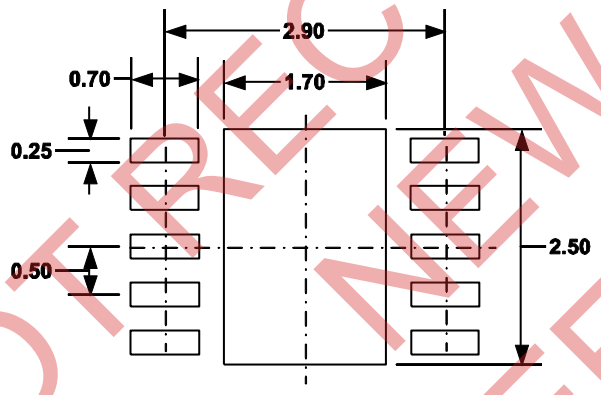

BOTTOM VIEW




SIDE VIEW




DETAIL A

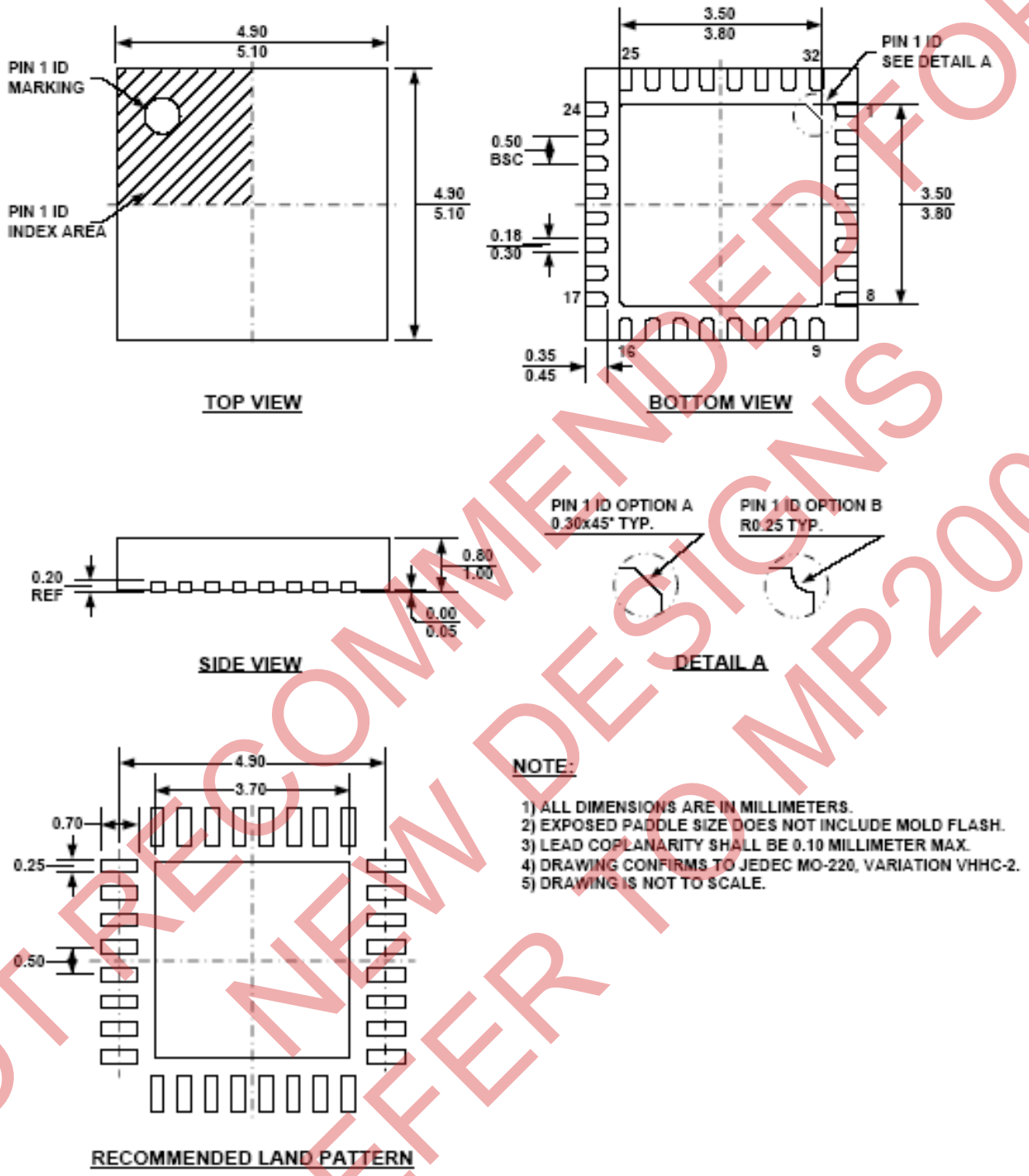



RECOMMENDED LAND PATTERN

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

## QFN32 (5mm x 5mm)




NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHC-2.
5) DRAWING IS NOT TO SCALE.