MP20249

Dual, Ultra-Low Noise, High PSRR 200mA Linear Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP20249 is a dual-channel, ultra-low noise, low dropout and high PSRR linear regulator. Fixed output voltage options are available between 1.2V to 3.3V with 1% accuracy by operating from a +2.3V to +6.0V input. It is designed to deliver up to 200mA of load current at each channel. Dropout voltage is only 75mV at full load. The MP20249 uses internal PMOSFETS as pass elements, which consume 125µA supply current (both LDOs on) at no load condition. With new innovative design techniques, the MP20249 can achieve an output voltage noise as low as 16µVRMS without using a bypass capacitor at each channel. The MP20249 is designed and optimized to work with small-value, low-cost ceramic capacitors, making it ideal for applications with space-constraints. It typically requires only 1µF of output capacitance for stability with any load at each channel.

The EN1 and EN2 pins control each output respectively. When both channels shutdown simultaneously, the chip is turned off and consumes nearly zero operation current, which is suitable for battery-power devices. The MP20249 features current limit and over-temperature protection.

The MP20249 also has an output discharge function that controls the quick discharging of the output capacitor.
It is available in a miniature 6-ball WLCSP package.

FEATURES

- Input Voltage Range: 2.3V to 6.0V
- Two LDOs in a 1.0x1.5mm WLCSP Package
- Up to 200mA Output Current (Per Channel)
- Dual Enable Pins Control Each Output
- 16µVRMS Output Noise (100Hz-1kHz) Bandwidth with No Bypass Capacitor required
- High PSRR: 65dB @ 1kHz
- Low dropout: 60mV @ 150mA Load
- Stable with 1µF Ceramic Capacitor for Any Load (Per Channel)
- Very Fast Line and Load Transient Response
- Output Discharge Function
- Current Limit and Thermal Protection

APPLICATIONS

- Cellular Mobile Phones
- Digital Cameras
- Handheld and Battery-powered Equipment
- Wireless LAN
- Post DC-to-DC Regulation

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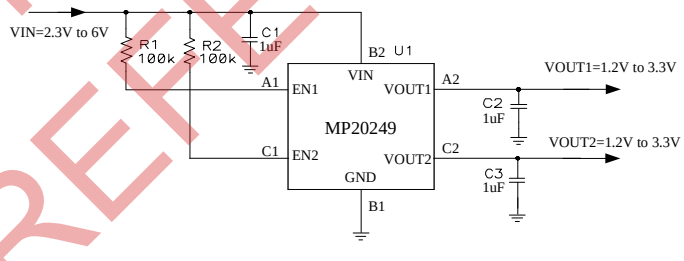
TYPICAL APPLICATION



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ORDERING INFORMATION*

Part Number*	V_{OUT1}	V_{OUT2}	Package	Top Marking	Free Air Temperature Range (T_A)
MP20249DC-MC-LF-Z	2.8V	1.2V	WLCSP (1.0X1.5mm)	9WY	-40°C to +85°C

* Contact factory for other fixed output options

ORDERING GUIDE**

MP20249XX-XX-LF-Z
- VOUT2
- VOUT1
- Package Type
- Operation Temperature

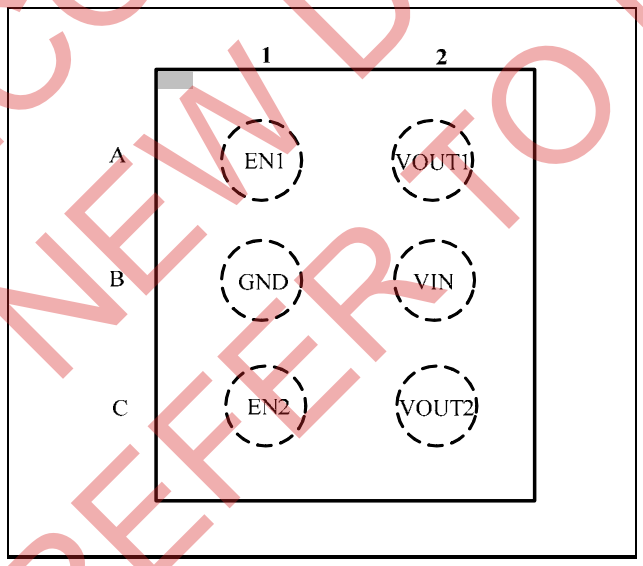
** For RoHS Compliant Packaging, add suffix - LF (e.g. MP20249DC-☐☐-LF); For Tape and Reel, add suffix -Z (e.g. MP20249DC-☐☐-LF-Z)

OUTPUT VOLTAGE SELECTOR GUIDE***

Code	V_{OUT}	Code	V_{OUT}
C	1.2	T	2.65
B	1.3	L	2.7
F	1.5	M	2.8
W	1.6	N	2.85
G	1.8	V	2.9
D	1.85	P	3.0
Y	1.9	Q	3.1
H	2.0	X	3.15
E	2.1	R	3.2
J	2.5	S	3.3
K	2.6		

*** Code in **Bold** are standard versions. For other output voltages between 1.2V and 3.3V contact factory for availability. Minimum order quantity on non-standard versions is 25,000 units.

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

Supply Input Voltage 6.5V
Continuous Power Dissipation (T_A = +25°C)(2)
WLCSP……..…….0.5W
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10sec) ....300°C

ESD SUSCEPTIBILITY(3)

HBM (Human Body Mode) 2kV
MM (Machine Mode) 200V

Recommended Operating Conditions (4)

Supply Input Voltage .....2.3V to 6.0V
Enable Input Voltage .....0V to 5.5V
Operating Junct. Temp (T_J)..... -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}
WLCSP	250	n/a .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD sensitive. Handling precaution recommended.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = (V_{OUT} + 0.5 V) or 2.3V (whichever is greater), EN = V_{IN}, I_{OUT} = 10mA, C_{IN} = $C_{OUT1,2}$ = 1µF, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		2.3		6.0	V
Maximum Output Current	I_{MAX}	Continuous	200			mA
Output Voltage Accuracy	ΔV_{OUT}	I_{LOAD} = 10mA	-1		+1	%
Current Limit	I_{LIM}	R_{Load}=1Ω	220	270	440	mA
Ground Current	I_Q	No Load		125		µA
Dropout Voltage (6)	V_{DROP}	V_{OUT} =1.8V, I_{OUT} = 150mA, T_J=-40°C to +125°C		60		mV
		V_{OUT} =1.8V, I_{OUT} = 200mA T_J=-40°C to +125°C		75		mV
Line regulation(7)	V_{LNR}	V_{IN}=2.3v to 6v I_{OUT}=0.1mA	-0.03		0.03	%/V
Load regulation(8)	V_{LDR}	I_{OUT}=1mA to 200mA		0.001		%/mA
EN Input High Threshold	V_{IH}	V_{IN} = 2.3V to 5.5V	1.2			V
EN Input Low Threshold	V_{IL}	V_{IN} = 2.3V to 5.5V			0.4	V
EN Input Bias Current	I_{SD}	EN = V_{IN}=5.5V		100	300	nA
Shutdown Supply Current	I_{GSD}	EN1 = EN2 = GND		0.12	1	µA
Under-voltage Lockout	$UVLO_{RISE}$				2.25	V
Under-voltage Lockout Hysteresis	$UVLO_{HYS}$			160		mV
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	ΔT_{SD}			15		°C
Output Voltage Noise		100Hz to 1kHz, $C_{OUT1,2}$=4.7µF, V_{OUT}=1.2V I_{LOAD}=10mA		16		μV_{RMS}
Output Voltage AC PSRR		1kHz, $C_{OUT1,2}$ = 2.2µF, I_{LOAD} = 10mA		65		dB
		10kHz, $C_{OUT1,2}$ = 2.2µF, I_{LOAD} = 10mA		65		dB
		100kHz , $C_{OUT1,2}$ = 2.2µF, I_{LOAD} = 10mA		55		dB
Active Pull-Down Resistance	$R_{Shutdown}$	No Load, $C_{OUT1,2}$=1µF		80		Ω

Notes:

6) Load Regulation= $\frac{\left|V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}\right|}{V_{OUT(NOM)}} \times (\%)$

7) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

8) Line Regulation= $\frac{\left|V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}\right|}{\left[V_{IN(MAX)} - V_{IN(MIN)}\right] \times V_{OUT(NOM)}} \times (\% / V)$

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PIN FUNCTIONS

Package Pin #	Name	Description
A1	EN1	Enable Input for Regulator 1. Drive EN1 high to turn on Regulator 1; drive it low to turn off Regulator 1. For automatic startup, connect EN1 to VIN.
B1	GND	Ground Pin.
C1	EN2	Enable Input for Regulator 2. Drive EN2 high to turn on Regulator 2; drive it low to turn off Regulator 2. For automatic startup, connect EN2 to VIN.
A2	VOUT1	Regulated Output Voltage 1. Connect a 1µF or greater output capacitor between VOUT1 and GND.
B2	VIN	Regulator Input Supply. Bypass VIN to GND with a 1µF or greater capacitor.
C2	VOUT2	Regulated Output Voltage 2. Connect a 1µF or greater output capacitor between VOUT2 and GND.

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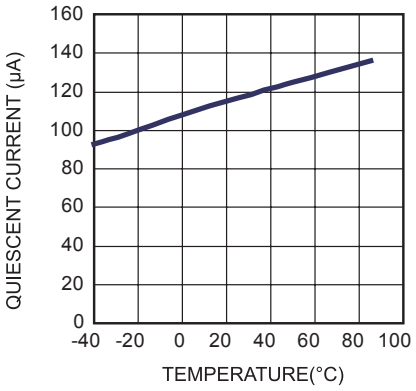
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = (V_{OUT} + 0.5 V) or 2.3V (whichever is greater), EN = V_{IN}, I_{OUT} = 10mA, V_{OUT1}=2.8V, V_{OUT2}=1.2V, C_{IN} = $C_{OUT1,2}$ = 1µF, T_A = 25°C, unless otherwise noted.

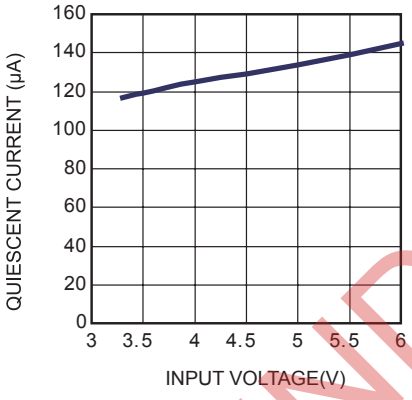
Quiescent Current vs. Temperature

Only one channel is enabled



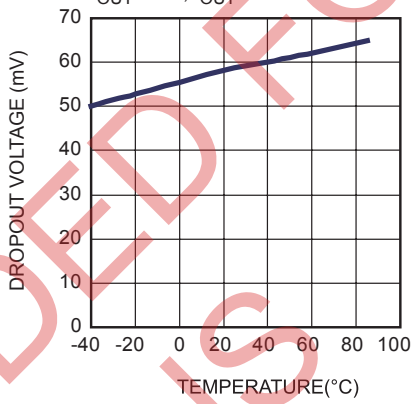
Quiescent Current vs. Input Voltage

Only one channel is enabled



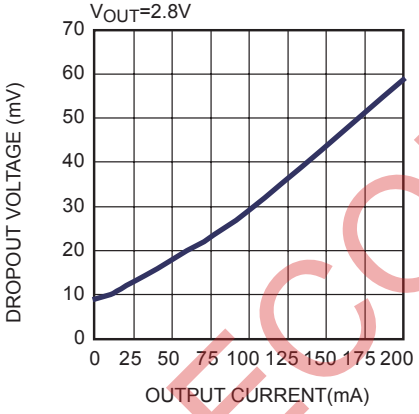
Dropout Voltage vs. Temperature

V_{OUT}=2.8V, I_{OUT}=200mA

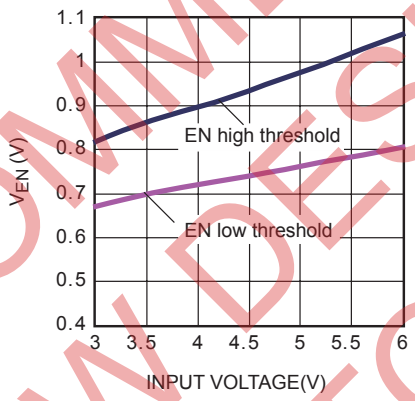


Dropout Voltage vs. Output Current

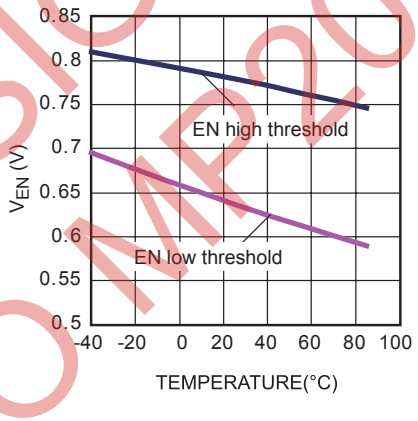
V_{OUT}=2.8V



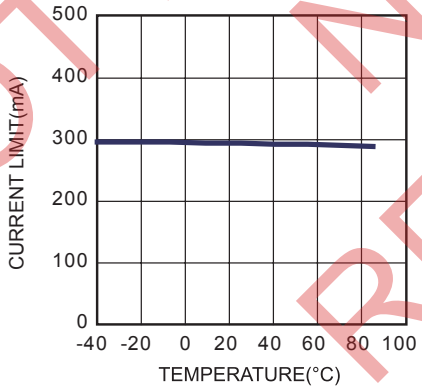
EN threshold vs. Input Voltage



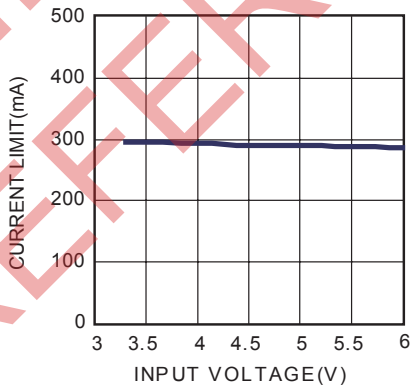
EN threshold vs. Temperature



Current Limit vs. Temperature

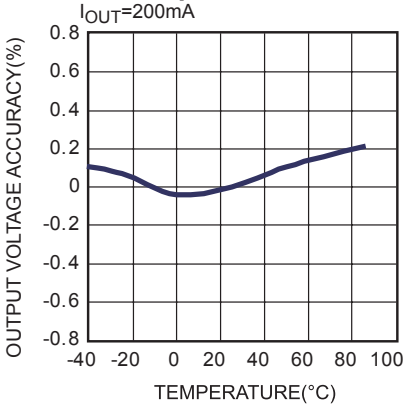


Current Limit vs. Input Voltage



Output Voltage Accuracy vs. Temperature

I_{OUT}=200mA



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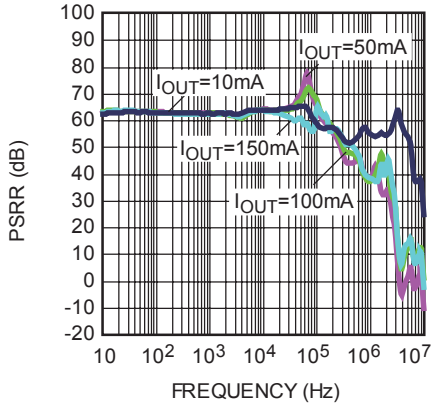
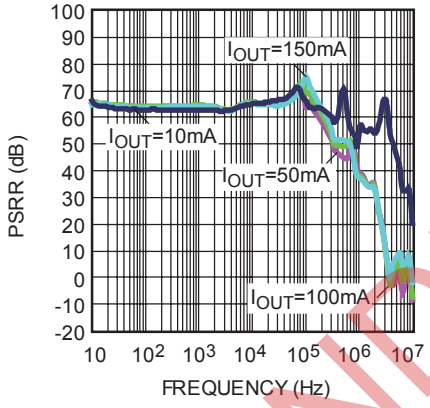
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = (V_{OUT} + 0.5 V) or 2.3V (whichever is greater), EN = V_{IN}, I_{OUT} = 10mA, V_{OUT1}=2.8V, V_{OUT2}=1.2V, C_{IN} = $C_{OUT1,2}$ = 1µF, T_A = 25°C, unless otherwise noted.

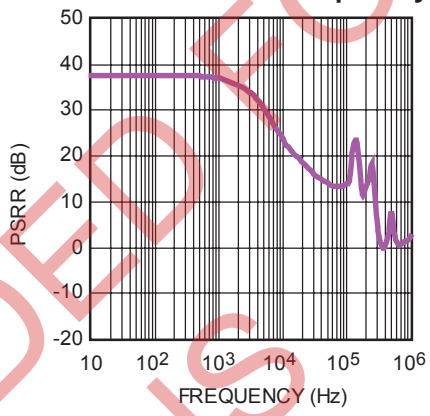
PSRR vs. Frenquency
V_{OUT}=2.8V



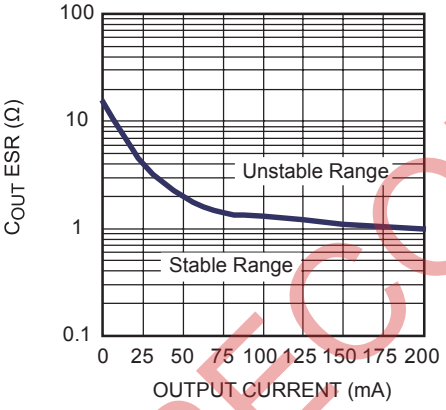
PSRR vs. Frenquency
V_{OUT}=1.2V



Channel to Channel Isolation vs. Frenquency



Region of Stable C_{OUT} ESR vs. Output Current



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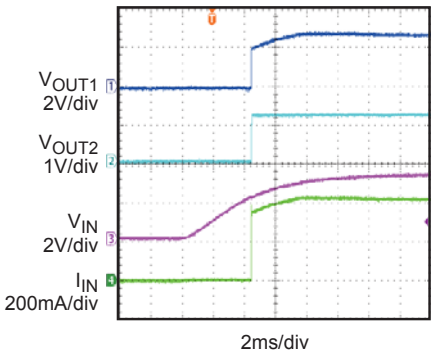
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = (V_{OUT} + 0.5 V) or 2.3V (whichever is greater), EN = V_{IN}, I_{OUT} = 10mA, V_{OUT1}=2.8V, V_{OUT2}=1.2V, C_{IN} = $C_{OUT1,2}$ = 1µF, T_A = 25°C, unless otherwise noted.

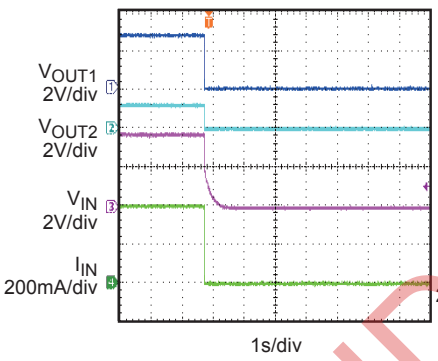
Input Power Start Up

I_{OUT1}=I_{OUT2}=200mA



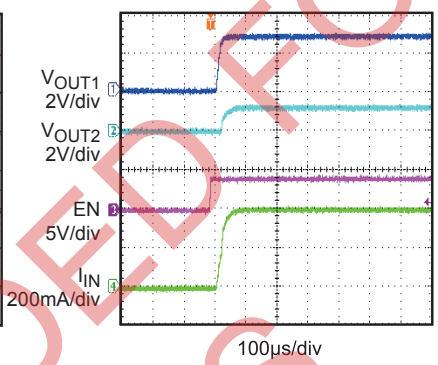
Input Power Shut Down

I_{OUT1}=I_{OUT2}=200mA



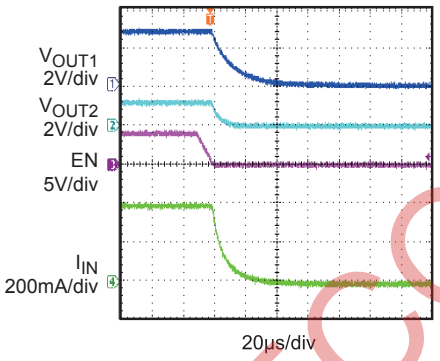
EN Start Up

I_{OUT1}=I_{OUT2}=200mA



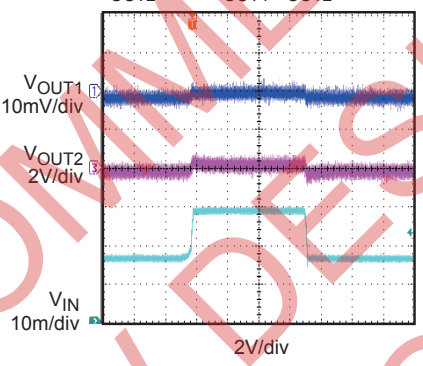
EN Shut Down

I_{OUT1}=I_{OUT2}=200mA



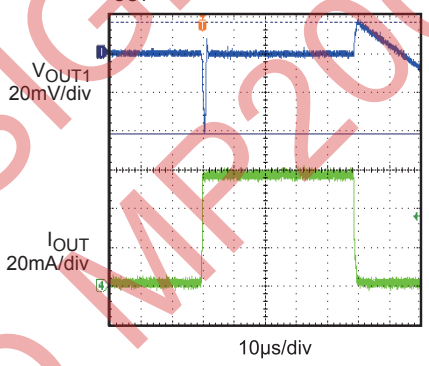
Line Transient

V_{IN}=3V to 6V, V_{OUT1}=2.8V
V_{OUT2}=1.2V, I_{OUT1}=I_{OUT2}=200mA



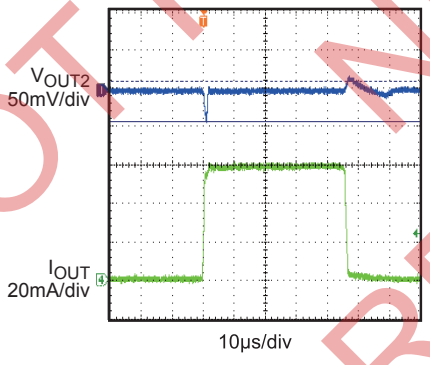
Load Transient

V_{IN}=3.3V, V_{OUT1}=2.8V
I_{OUT}=1mA to 60mA, with Resistor Load



Load Transient

V_{IN}=3.3V, V_{OUT2}=1.2V
I_{OUT}=1mA to 60mA, with Resistor Load



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BLOCK DIAGRAM

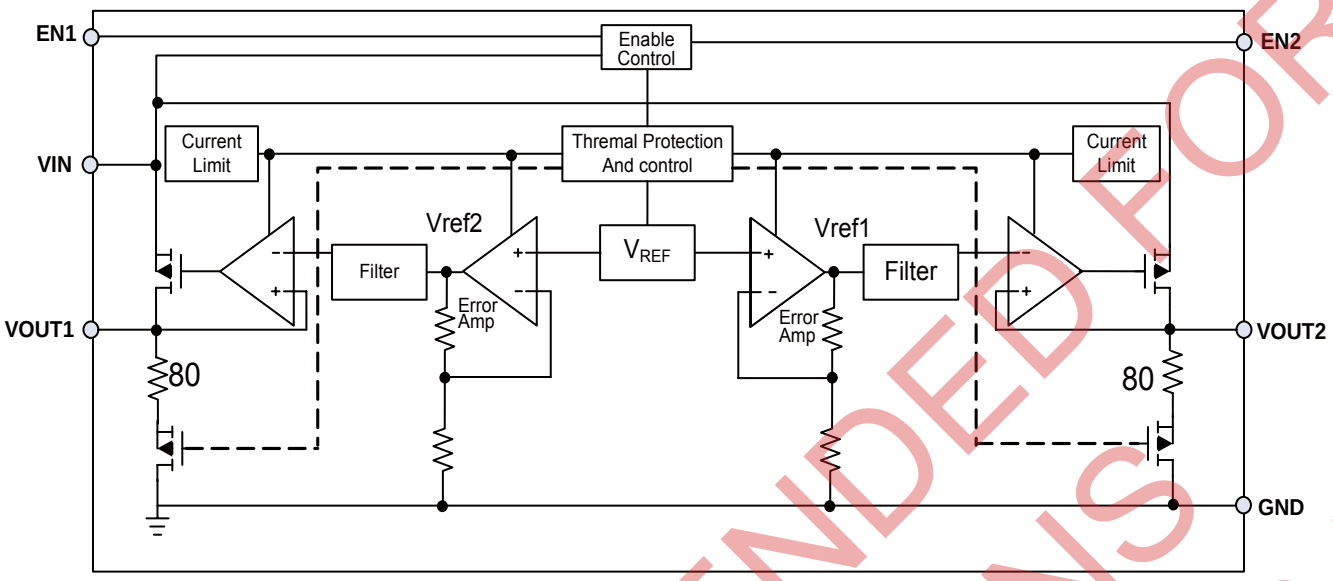

Figure 1—Function Block Diagram

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OPERATION

The MP20249 integrates two ultra low noise, low dropout, low quiescent current and high PSRR linear regulators for space-restricted applications. It is intended for use in devices that require very low voltage, and ultra-small footprint, such as mobile phones and MP3 players.

The MP20249 uses internal P-channel MOSFETs as the pass elements and features internal thermal shutdown and internal current limit circuits.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. It determines the available end-of-life battery voltage in battery-powered systems. For the P-channel MOSFET pass element, the dropout voltage is a function of drain to source on resistance. Because the P-channel MOSFET pass element behaves as a low-value resistor, the dropout voltage of MP20249 is very low.

Under Voltage Lockout

The MP20249 has an internal under-voltage lockout circuit that disables the device when the input voltage is less than approximately 2.1V. This ensures that the input and the output of the MP20249 behave in a predictable manner during input power-up.

EN On / Off

The MP20249 can be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin will turn the device on. When the EN pin is low, the regulator output is off. The EN pin should be tied to VIN to keep the regulator output always on if the application does not require the shutdown feature.
Do not float the EN pin.

Output Discharge Function

When either channel is disabled, it goes into output discharge mode automatically and its internal discharge MOSFET provides a resistive discharge path for the output capacitor. This function is only suitable for discharge output capacitor in the limited time.

Current Limit and Thermal Protection

The MP20249 includes two independent current limit structures which monitor and control each P-channel MOSFET's gate voltage to limit the guaranteed maximum output current to 200mA.

Thermal protection turns off the P-channel MOSFETs when the junction temperature exceeds +150ºC, allowing the IC to cool. When the IC's junction temperature drops by 15ºC, the P-channel MOS will be turned on again. Thermal protection limits total power dissipation in the MP20249. For reliable operation, junction temperature should be limited to 125ºC maximum.

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APPLICATION INFORMATION

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature difference between the junction and ambient air, and the rate of airflow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where ($T_{Junction}$ - $T_{Ambient}$) is the temperature difference between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connecting the GND pin of MP20249 to ground with a large ground plane will help the channel heat away.

Input Capacitor Selection

Using a capacitor whose value is >1μF on the MP20249 input and the amount of capacitance can be increased without limit. Larger values will help to improve line transient response with the drawback of increased size. Ceramic capacitors are preferred, but tantalum capacitors may also suffice.

Output Capacitor Selection

The MP20249 is designed specifically to work with very low ESR ceramic output capacitor and benefit applications with space limitation. Output capacitor of larger values will help to improve load transient response and reduce noise with the drawback of increased size. For the application circuit, the MP20249 requires a minimum capacitance of 0.7uF with an ESR of 1Ω or less.

Output Noise and PSRR

In the MP20249 device, each channel has an internal 50pF bypass capacitor with new innovative structure that reduces output noises greatly. Therefore, space-limited applications do not need to use external bypass capacitors. The power supply rejection is 65dB at 10kHz and 55dB at 100kHz.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP20241

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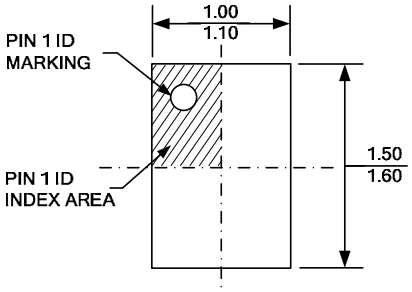
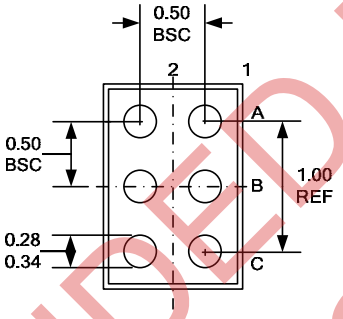
PACKAGE INFORMATION

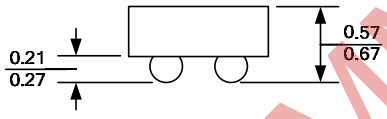
PACKAGE OUTLINE DRAWING FOR 6L WLCSP (1.0x1.5mm)
MF-PO-D-0088 preliminary



TOP VIEW



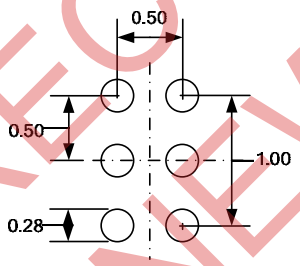
BOTTOM VIEW



SIDE VIEW

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211, VARIATION BB.
4) DRAWING IS NOT TO SCALE.



RECOMMENDED LAND PATTERN

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP2041

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