MP20046

Fast Transient Response, 2A Low Dropout Voltage Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP20046 is a low dropout linear regulator supplying up to 2A current with 210mV dropout voltage. The output voltage is preset internally which ranges from 1.5V to 3.3V.

An internal PMOS pass element is used to allow a low 75μA ground current at full load and drops down to 1uA when the device is disabled, making the MP20046 suitable for battery-power devices. Integrated power good (PG) function resets microcomputer and microprocessor systems in the event of an under voltage condition. MP20046 are designed to have fast response for larger load and line transient response. Other features include current limit and thermal protection.

The MP20046 is available in thermally enhanced SOIC8 package and 10-pin QFN package.

FEATURES

- Up to 2A Output Current
- Low 210mV Dropout at 2A
- Fast Transient Response
- Open Drain Power-Good(PG) Status Output
- High 70dB at100Hz PSRR
- Low 17μV_{RMS} Output Noise
- Current Limit and Thermal Protection
- Available in SOIC8 with Exposed Pad and 10-pin QFN Packages

APPLICATIONS

- Telecom
- Servers
- DSP, FPGA Supplies

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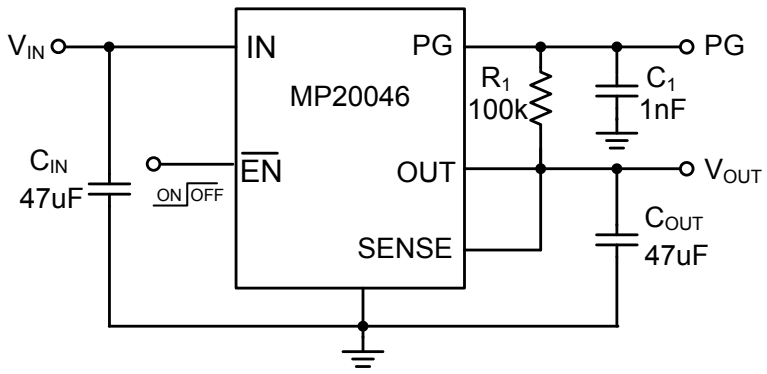
TYPICAL APPLICATION



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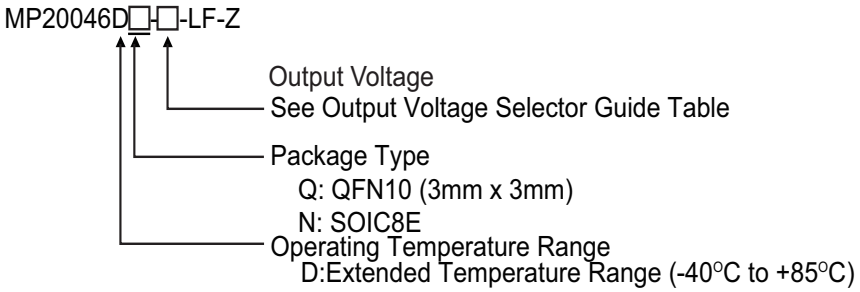
ORDERING INFORMATION

Part Number*	Output Voltage	Package	Top Marking	Junction Air Temperature (T_J)
MP20046DN-F**	1.5V	SOIC8E	M20046F	-40°C to +85°C
MP20046DQ-S**	3.3V	QFN10 (3x3)	9N	

*Other output voltage versions between 1.5V and 3.3V, contact factory for availability.

ORDERING GUIDE**



** For RoHS Compliant Packaging, add suffix - LF (e.g. MP20046D□-□-LF);
For Tape and Reel, add suffix -Z (e.g. MP20046D□-□-LF-Z).

OUTPUT VOLTAGE SELECTOR GUIDE

Code	V_{OUT}	Code	V_{OUT}
F	1.5	L	2.7
W	1.6	M	2.8
G	1.8	N	2.85
D	1.85	V	2.9
Y	1.9	P	3.0
H	2.0	Q	3.1
E	2.1	X	3.15
J	2.5	R	3.2
K	2.6	S	3.3
T	2.65		

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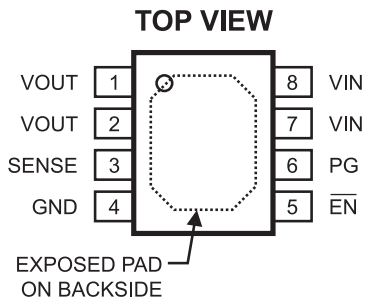
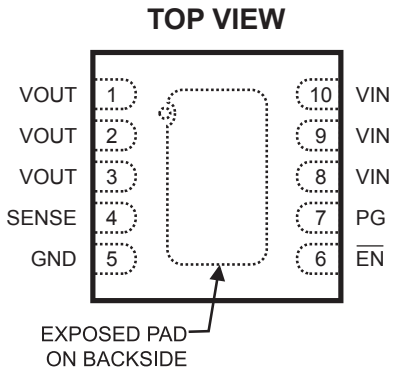
PACKAGE REFERENCE

SOIC8E	QFN10(3x3)
	

ABSOLUTE MAXIMUM RATINGS (1)

Supply Input Voltage 6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8E 2.0W
QFN10 (3x3) 1.67W
Junction Operation Temperature Range
..... -40°C to 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 260°C

Recommended Operating Conditions (3)

Supply Input Voltage ..... 2.7V to 5.5V
Enable Input Voltage ..... 0V to 5.5V
Operating Junct. Temp (T_J) ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
SOIC8E	50	10	°C/W
QFN10 (3x3)	60	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{IN}=($V_{OUT\ (TYP)}$ +1V) or +2.7V, I_{OUT}=1mA, V_{EN}=0V, C_{OUT}=47µF, T_J =-40°C to +125°C, unless otherwise noted. Typical values are at T_A =+25°C.

Parameter		Symbol	Condition	Min	Typ	Max	Units
Output Voltage	1.5V	V_{OUT}	2.7V < V_{IN} < 5.5V	1.485	1.5	1.515	V
	2.5V		3.5V < V_{IN} < 5.5V	2.475	2.5	2.525	
	3.3V		4.3V < V_{IN} < 5.5V	3.267	3.3	3.333	
Ground Pin Current		I_{GND}	I_{OUT} = 1mA to 2A		75	300	µA
Line Regulation(5)		ΔV_{OUT}%/ V_{OUT}	V_{OUT} + 1V < V_{IN} ≤ 5.5V		0.01	0.1	%/V
Load Regulation(6)		ΔV_{OUT}	I_{OUT} = 1mA to 2A		4		mV
Output Voltage Noise			10Hz to 30kHz, V_{OUT}=3.3V, C_{OUT}=100µF		17		μV_{RMS}
Dropout Voltage(7)		V_{DO}	I_{OUT}=2A,,V_{OUT}= 1.4V		300	470	mV
			I_{OUT}=2A, V_{OUT}= 1.7V		300	470	
			I_{OUT}=2A, V_{OUT}= 2.4V		280	420	
			I_{OUT}=2A,,V_{OUT}= 3.2V		210	400	
Current Limit		I_{LIM}	V_{OUT}=0V		3.3	4.5	A
Standby Current		I_{STBY}	$\overline{EN}$=V_{IN}		1	10	µA
$\overline{EN}$ Input High Threshold		V_{IH}		1.5			V
$\overline{EN}$ Input Low Threshold		V_{IL}				0.4	V
Thermal Shutdown Temperature		T_{SD}			+150		°C
Output Voltage AC PSRR		PSRR	F=100Hz, C_{OUT}=100µF, I_{OUT}=2A		70		dB
PG	Minimum Input Voltage for Valid PG		$I_{OUT(PG)}$=300µA, $V_{(PG)}$ ≤ 0.8 V			1.6	V
	Trip Threshold Voltage		V_{OUT} decreasing	78		86	$\%V_{OUT}$
	Hysteresis Voltage		Measured at V_{OUT}		1.15		$\%V_{OUT}$
	Output Low Voltage		$I_{OUT(PG)}$=1mA		0.15	0.4	V
	Leakage Current		$V_{(PG)}$ = 5.5V			1	µA
$\overline{EN}$ Input Current			$\overline{EN}$=V_{IN}	-1		1	µA
			$\overline{EN}$=0V	-1	0	1	µA

Notes:

5) Line Regulation= $\frac{\left|V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}\right|}{\left[V_{IN(MAX)} - V_{IN(MIN)}\right] \times V_{OUT(NOM)}} \times 100(\%/V)$

6) Load Regulation= $\left|V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}\right|$

7) Ramp down input voltage till output voltage equals $V_{OUT(NOM)}$ – 0.1V

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PIN FUNCTIONS

SOIC8E Pin #	QFN10 (3mm×3mm) Pin #	Name	Description
1, 2	1, 2, 3	VOUT	Regulated output voltage
3	4	SENSE	Output sense
4	5	GND/ Exposed Pad	Ground. Connect exposed pad to GND plane for optimal thermal performance
5	6	$\overline{EN}$	Negative polarity enable ($\overline{EN}$) input
6	7	PG	Open-drain power-good (PG) output
7, 8	8, 9, 10	VIN	Input voltage

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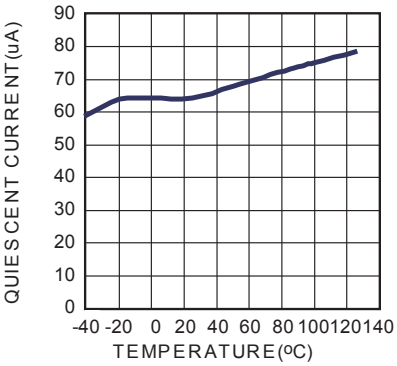
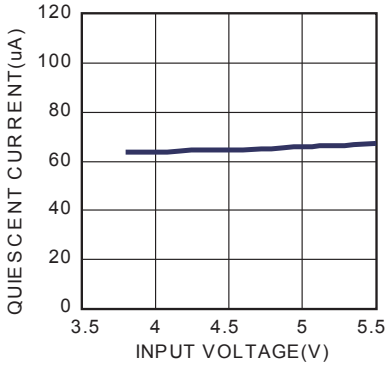
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=3.8V, V_{OUT} =3.3V, C_{IN}=C_{OUT} =47µF, T_A=25°C, unless otherwise noted.

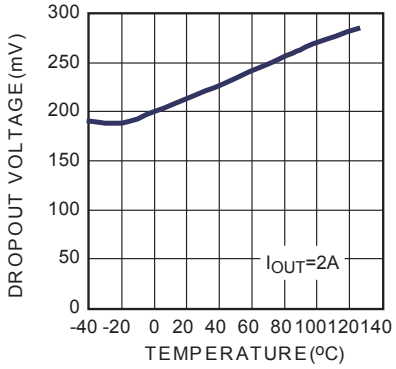
Quiescent Current vs. Temperature



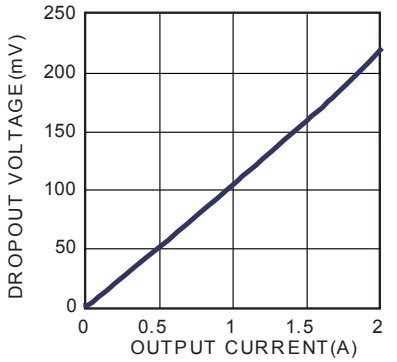
Quiescent Current vs. Input Voltage



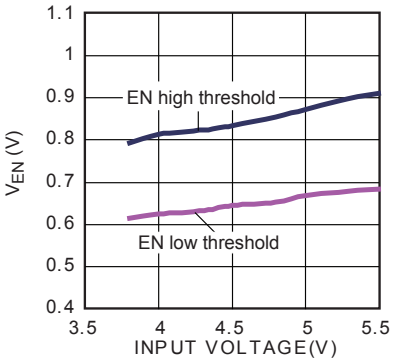
Dropout Voltage vs. Temperature



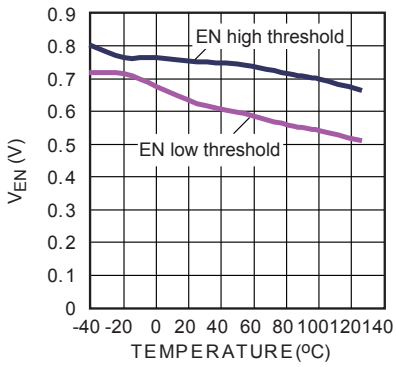
Dropout Voltage vs. Output Current



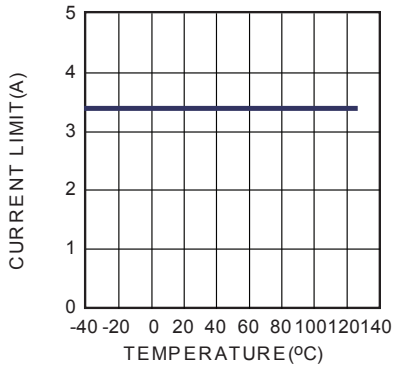
EN threshold vs. Input Voltage



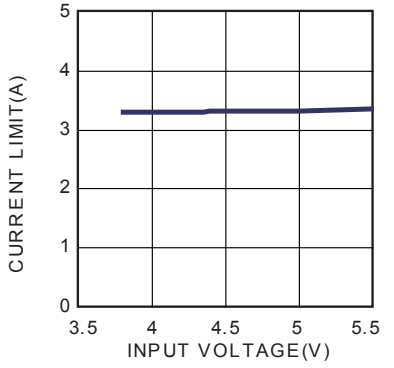
EN threshold vs. Temperature



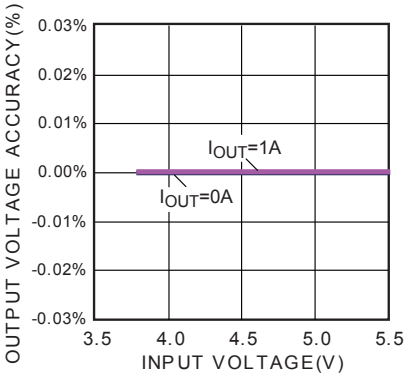
Current Limit vs. Temperature



Current Limit vs. Input Voltage



Line Regulation



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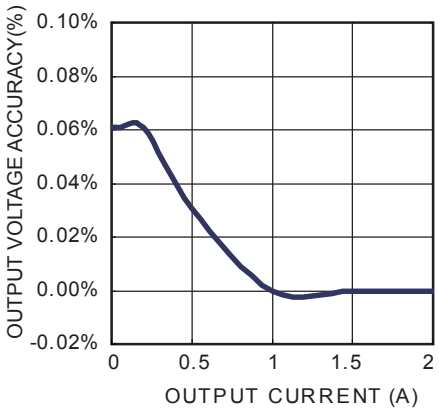
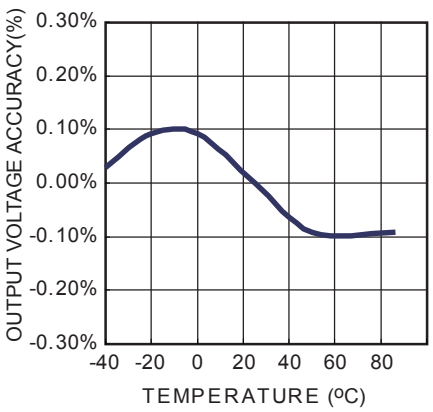
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=3.8V, V_{OUT}=3.3V, C_{IN}=C_{OUT} =47µF, T_A=25°C, unless otherwise noted.

Load Regulation



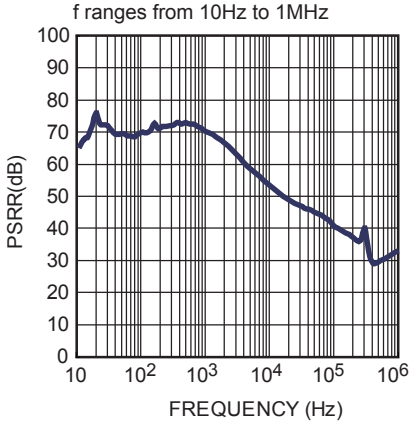
Output Voltage Accuracy vs. Temperature



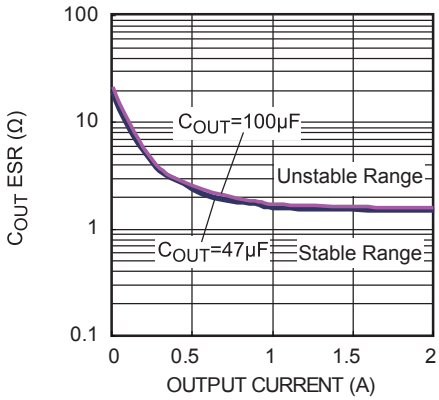
PSRR

I_{OUT}=2A

f ranges from 10Hz to 1MHz



Region of Stable C_{OUT} ESR vs. Output Current



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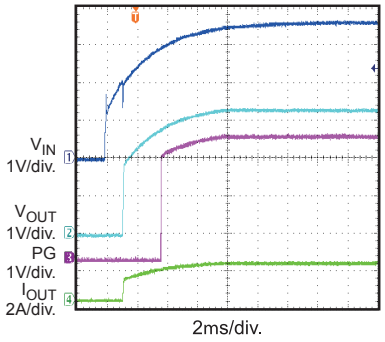
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=3.8V, V_{OUT}=3.3V, C_{IN}=C_{OUT} =47µF, T_A=25°C, unless otherwise noted.

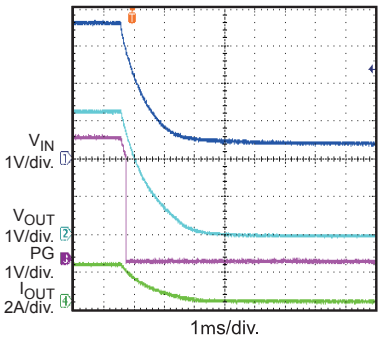
Input Power Start Up

V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 2A
with Resistiver Load



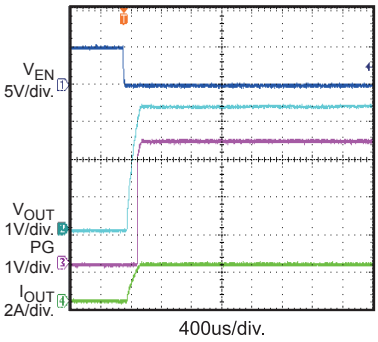
Input Power Shutdown

V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 2A
with Resistive Load



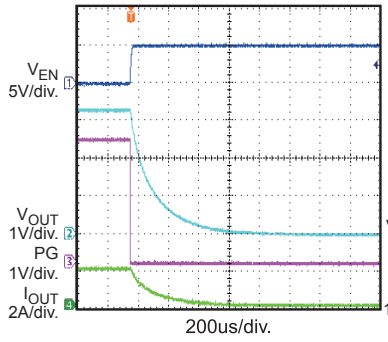
EN Start Up

V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 2A
with Resistive Load



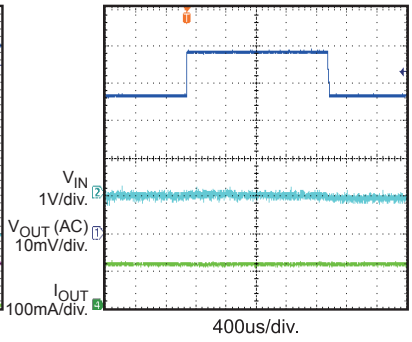
EN Shutdown

V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 2A
with Resistive Load



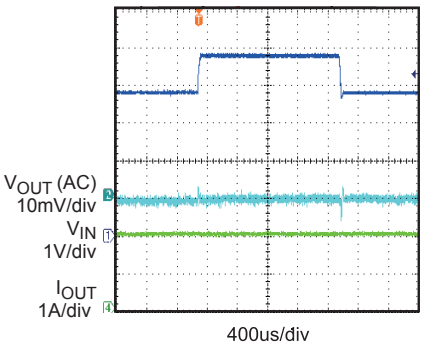
Line Transient

V_{IN} = 3.8V to 4.8V, V_{OUT} = 3.3V
I_{OUT} = 100mA,
with Resistive Load



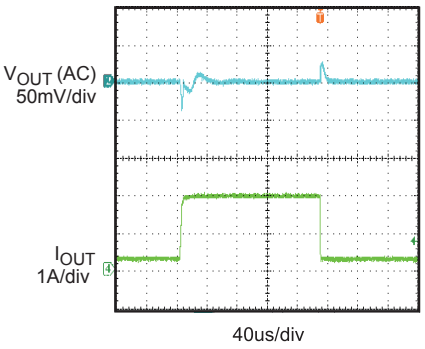
Line Transient

V_{IN}=3.8V to 4.8V, V_{OUT}=3.3V, I_{OUT}=2A
with Resistive Load



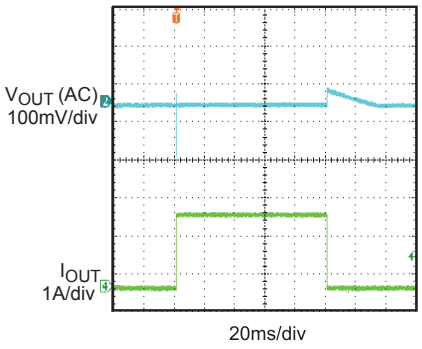
Load Transient

V_{IN}=3.8V, V_{OUT}=3.3V, I_{OUT}=200mA to 2A
with Resistive Load



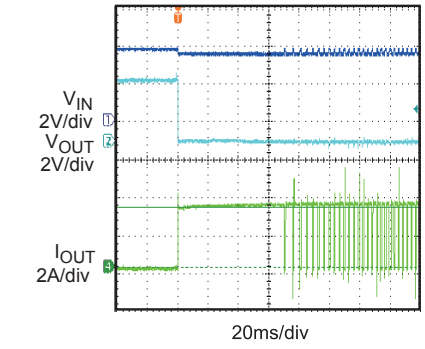
Load Transient

V_{IN}=3.8V, V_{OUT}=3.3V, I_{OUT}=0mA to 2A
with Resistive Load



Short Protection Entry

V_{IN}=3.8V, V_{OUT}=3.3V
Short Out to GND



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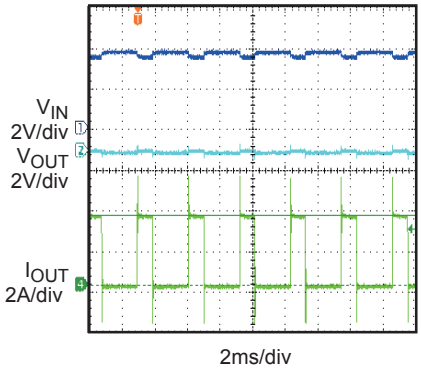
TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

V_{IN}=3.8V, V_{OUT}=3.3V, C_{IN}=C_{OUT} =47µF, T_A=25°C, unless otherwise noted.

Short Protection Steady State

V_{IN}=3.8V, V_{OUT}=3.3V

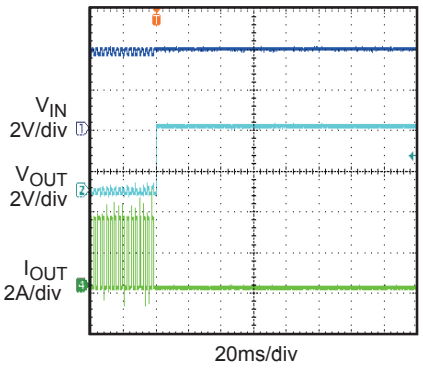
Short Out to GND



Short Protection Recovery

V_{IN}=3.8V, V_{OUT}=3.3V

Short Out to GND



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FUNCTION BLOCK DIAGRAM

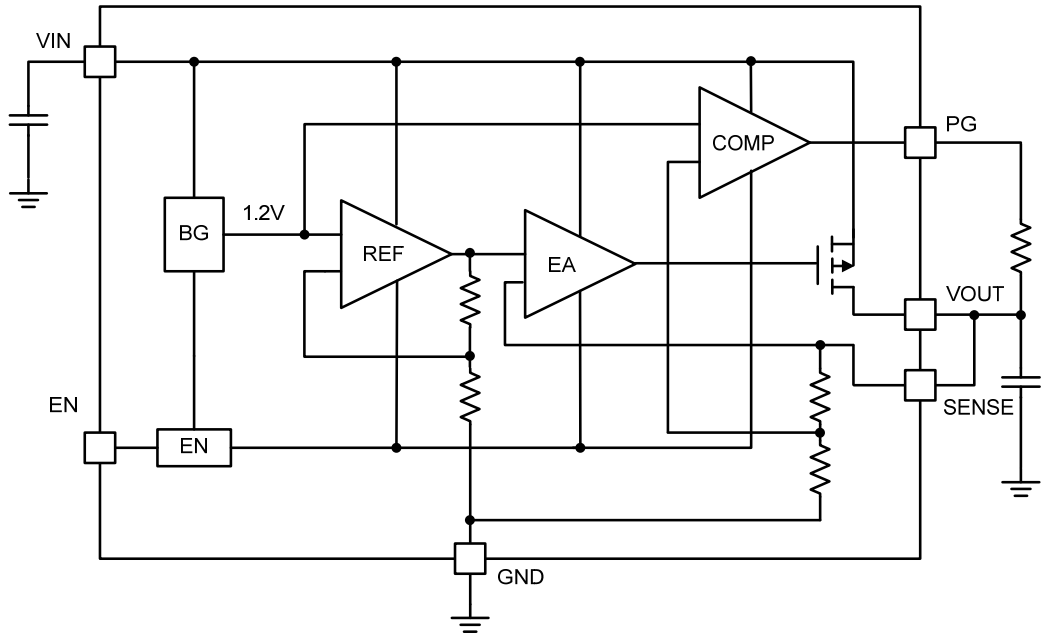

Figure 1—Block Diagram of Low Dropout Regulation

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OPERATION

The MP20046 is a low dropout linear regulator supplying up to 2A current. It is intended for use in devices that require very low dropout voltage, low quiescent, low noise and high PSRR such as wireless LAN, battery powered equipment and hand-held equipment.

The MP20046 uses an internal PMOS as the pass element and features internal thermal shutdown and internal current limit circuit.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage of MP20046 is very low.

Shutdown

The MP20046 can be switched ON or OFF by a logic input at the $\overline{EN}$ pin. A high voltage at this pin will turn the device off. When the $\overline{EN}$ pin is low, the regulator output is on. The $\overline{EN}$ pin should be tied to GND to keep the regulator output always on if the application does not require the shutdown feature. Do not float the $\overline{EN}$ pin.

Current Limit

The MP20046 includes a current limit structure which monitors and controls PMOS's gate voltage to limit the guaranteed maximum output current to 3.3A.

Power Good

The power good pin is an open collector output connected to OUT with a pull up resistor. It monitors the output voltage, and if the output voltage deceases below 83% of its regulation point, the PG pin becomes low. Enlarging pull up resistor or bypass capacitor will extend the set up time of PG output.

Thermal Protection

Thermal protection turns off the PMOS when the junction temperature exceeds +150ºC, allowing the IC to cool. When the IC's junction temperature drops by 20ºC, the PMOS will be turned on again. Thermal protection limits total power dissipation in the MP20046. For reliable operation, junction temperature should be limited to 125 ºC maximum.

Load-Transient Considerations

The output response of load-transient consists of a DC shift and transient response. Because of the excellent load regulation of MP20046, the DC shift is very small. For external circuit, the output voltage transient depends on the output capacitor's value and the ESR. Increasing the capacitance and decreasing the ESR will improve the transient response.

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APPLICATION INFORMATION

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature difference between the junction and ambient air, and the rate of air flow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where ($T_{Junction}$ − $T_{Ambient}$) is the temperature difference between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connecting the GND pin of MP20046 to ground using a large pad or ground plane helps to channel heat away.

Output Noise

Output noise voltage is the RMS output noise voltage over a given range of frequencies (10Hz to 30kHz) under the conditions of a constant output current and a ripple-free input voltage. Most of noise is caused by the internal voltage reference. A precision bandgap reference of MP20046 is used to generate the internal reference voltage. And a low pass filter is also used to reduce the output noise. These make the output noise of MP20046 low to $17uV_{RMS}$ over the range of the full load.

Power Supply Rejection Ratio (PSRR)

Power supply rejection ratio (PSRR), also known as ripple rejection, measures the LDO regulator's ability to prevent the regulated output voltage fluctuating caused by input voltage variations.

The ripple rejection is defined by

$$PSRR = \frac{V_{IN},ripple}{V_{OUT},ripple} \text{ at all frequencies}$$

The control loop tends to be the dominant contributor of supply rejection. The output capacitor of large value and low ESR, and adding by-pass capacitors will improve the PSRR performance.

Input Capacitor Selection

For a typical application, an input bypass capacitor is recommended for device stability. This capacitor should be as close to the input pins as possible. For fast transient conditions where droop at the input of the LDO may occur because of high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor depends on the output current and response time of the main power supply, as well as the distance to the load (LDO).

Output Capacitor Selection

The MP20046 is designed specifically to work with very low ESR ceramic output capacitor in space-saving and performance consideration. A 47μF ceramic capacitor with ESR lower than 1.5Ω is suitable for the MP20046 application circuit. Output capacitor of larger values will help to improve load transient response and reduce noise with the drawback of increased size.

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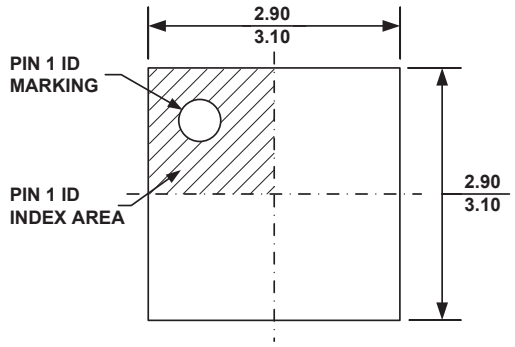
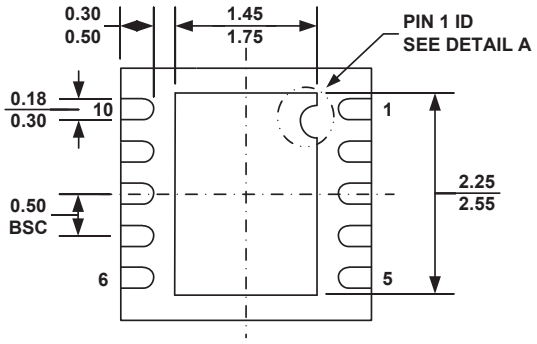
PACKAGE INFORMATION

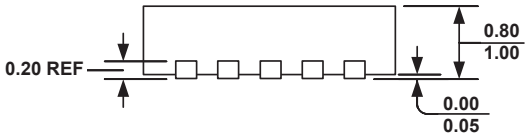
3mm×3mm QFN10



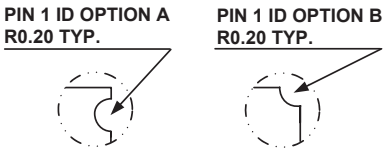
TOP VIEW



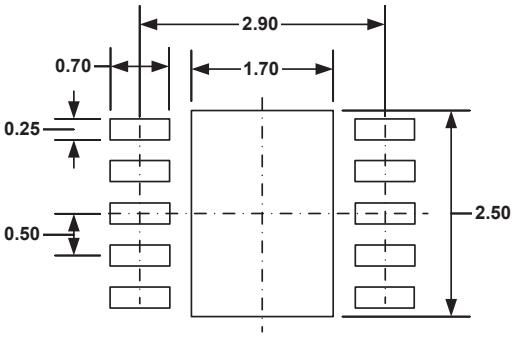
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

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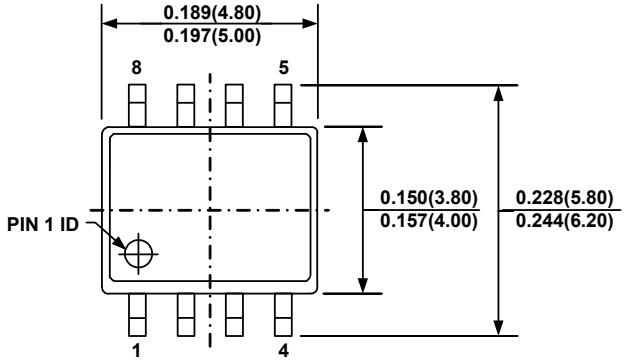
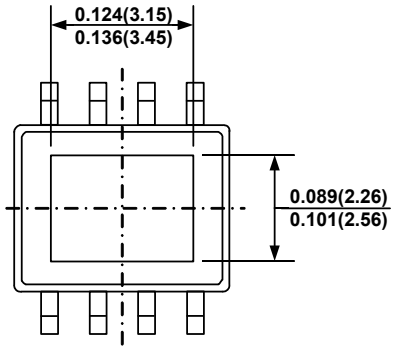
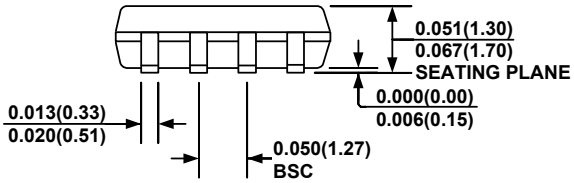


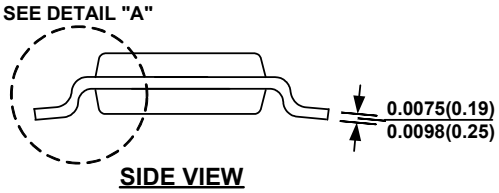
TOP VIEW



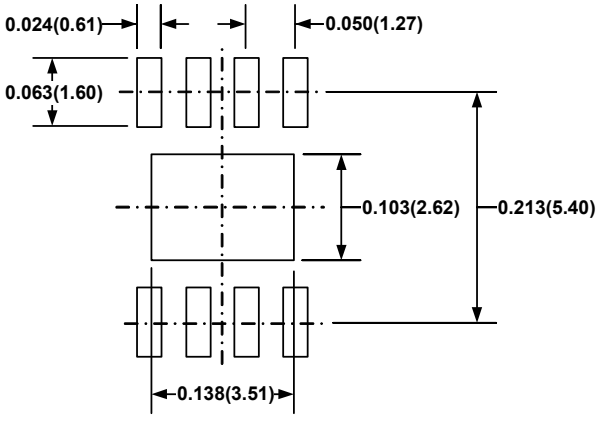
BOTTOM VIEW



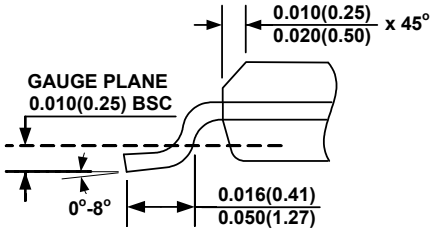
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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