MP20041

Dual, Ultra Low Noise, High PSRR 300mA Linear Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP20041 is a dual-channel, micropower, ultra low noise, low dropout and high PSRR linear regulator. The output voltage of MP20041 ranges from 1.2V to 3.6V in 100mV increments and 1% accuracy by operating from a +2.5V to +6.0V input. The MP20041 can supply up to 300mA of load current at each channel.

The MP20041 uses an internal PMOS as the pass element, which consumes 114μA supply current (both LDOs on) at no load condition. The EN1 and EN2 pins control each output respectively. When both channels shutdown simultaneously, the chip will be turned off and consume nearly zero operation current which is suitable for battery-power devices. The MP20041 features current limit and over temperature protection.

It is available in a 2mm x 2mm TQFN8 package.

FEATURES

- Wide Operating Voltage Ranges: 2.5V to 6V
- Two LDOs in a 2mmx2mm TQFN8 Package
- Up to 300mA Output Current (Per Channel)
- Dual Enable Pins Control Each Output
- 72dB PSRR at 10kHz
- $11\mu V_{RMS}$ Ultra Low Noise Output with No Noise Bypass Capacitor Required
- 73mV Dropout at 100mA Load
- Very Fast Line/Load Transient Responses with Small Input/Output Capacitor
- Current Limit and Thermal Protection

APPLICATIONS

- Cellular Phones
- Battery-powered Equipment
- Laptop, Notebook, and Palmtop Computers
- Hand-held Equipment
- Wireless LAN

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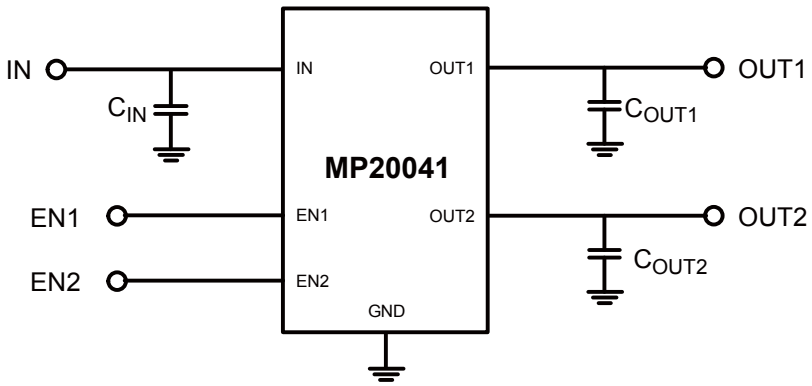
TYPICAL APPLICATION



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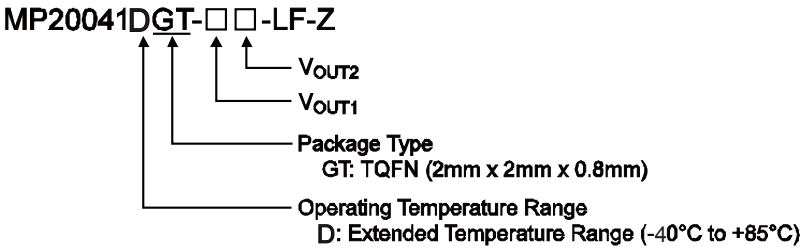
ORDERING INFORMATION*

Part Number	V_{OUT1}	V_{OUT2}	Package	Free Air Temperature (T_A)	Top Marking
MP20041DGT-GJ-LF-Z	1.8V	2.5V	TQFN8 (2mmx2mm)	-40°C to +85°C	5H
MP20041DGT-MG-LF-Z	2.8V	1.8V			7K
MP20041DGT-SS-LF-Z	3.3V	3.3V			9P
MP20041DGT-PP-LF-Z	3.0V	3.0V			6P

* Other output voltage versions between 1.2V and 3.3V are available in 100mV increments. Contact factory for availability.

ORDERING GUIDE**



** For RoHS Compliant Packaging, add suffix - LF (e.g. MP20041DGT-□□-LF); For Tape and Reel, add suffix -Z (e.g. MP20041DGT-□□-LF-Z).

OUTPUT VOLTAGE SELECTOR GUIDE***

Code	V_{OUT}	Code	V_{OUT}
C	1.2	T	2.65
B	1.3	L	2.7
F	1.5	**M**	**2.8**
W	1.6	**N**	**2.85**
G	**1.8**	V	2.9
D	**1.85**	**P**	**3.0**
Y	1.9	Q	3.1
H	2.0	X	3.15
E	2.1	R	3.2
J	**2.5**	**S**	**3.3**
K	2.6	Z	5.0

*** Code in **Bold** are standard versions. For other output voltages between 1.2V and 5.0V contact factory for availability. Minimum order quantity on non-standard versions is 25,000 units.

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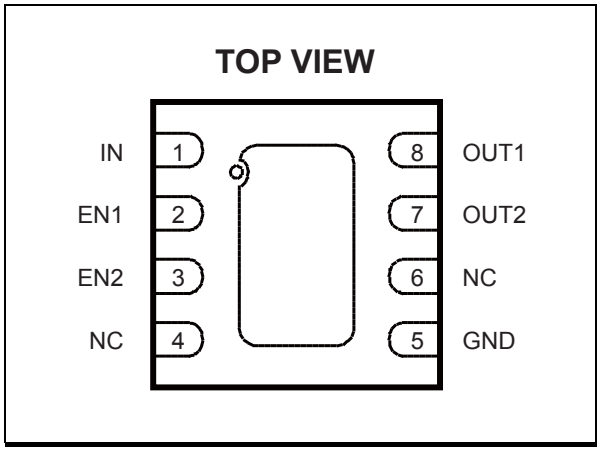
PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Input Voltage 6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 1.25W
Operation Temperature Range .... -40°C to 85°C
Storage Temperature Range..... -65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 260°C

Recommended Operating Conditions (3)

Supply Input Voltage..... 2.5V to 6.0V
Enable Input Voltage ..... 0V to 6.0V
Operating Junct. Temp (T_J) .....–40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

2mmx2mm TQFN8	80	16	°C/W

Notes:

1) Exceeding these ratings may cause permanent damage to the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside its operating conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{IN}=3.5V, V_{OUT1}=1.8V, V_{OUT2}=2.5V, C_{IN}=C_{OUT1}=C_{OUT2}=1µF, EN1=EN2=V_{IN}, Typical Value at T_A=25°C for each LDO unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Input Voltage	V_{IN}	V_{IN}=2.5V to 6.0V		2.5		6	V
Output Voltage Range	V_{OUT}			1.2		3.6	V
Load regulation(5)	ΔV_{OUT}	I_{LOAD} = 1mA to 300mA		-35	-10	5	mV
Line Regulation(6)	ΔV_{LINE}	V_{IN} =(V_{OUT}+0.3V or 2.5V) to 6V, I_{OUT}=1mA				0.05	%/V
Maximum Output Current	I_{MAX}	Continuous		300			mA
Current Limit	I_{LIM}	Short circuit current limit			525		mA
Quiescent Current	I_G	No Load			114		uA
Dropout Voltage (7)	V_{DROP1}	V_{OUT1}=1.8V, I_{OUT1} = 100mA			75		mV
		V_{OUT1}=1.8V, I_{OUT1} = 300mA			220		mV
	V_{DROP2}	V_{OUT2}=2.5V, I_{OUT2} = 100mA			60		mV
		V_{OUT2}=2.5V, I_{OUT2} = 300mA			180		mV
EN Input High Threshold	V_{IH}	V_{IN} = 2.5V to 6.0V		1.6			V
EN Input Low Threshold	V_{IL}	V_{IN} = 2.5V to 6.0V				0.45	V
EN Input Bias Current	I_{SD}	EN = GND or V_{IN}				300	nA
Shutdown Supply Current	I_{GSD}	EN1 = EN2 = GND			0.03	1	uA
Thermal Shutdown Temperature	T_{SD}				140		°C
Thermal Shutdown Hysteresis	ΔT_{SD}				10		°C
Output Voltage Noise		100Hz to 100kHz, C_{OUT}=1µF, I_{LOAD}=10mA			11		μV_{RMS}
		100Hz to 100kHz, C_{OUT}=1µF, I_{LOAD}=100mA			11		μV_{RMS}
Output Voltage AC PSRR	PSRR	I_{Load}=10mA	f=100Hz		68		dB
			f=1kHz		66		dB
			f=10kHz		65		dB
		I_{Load}=150mA	f=100Hz		69		dB
			f=1kHz		65		dB
			f=10kHz		72		dB

Notes:

5) Load Regulation= $\frac{\left|V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}\right|}{V_{OUT(NOM)}} \times 100(\%)$

6) Line Regulation= $\frac{\left|V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}\right|}{\left[V_{IN(MAX)} - V_{IN(MIN)}\right] \times V_{OUT(NOM)}} \times 100(\%/V)$

7) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

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PIN FUNCTIONS

Pin #	Name	Description
1	IN	Supply Input Pin.
2	EN1	Channel 1 Enable (Active High). Do Not Float This Pin.
3	EN2	Channel 2 Enable (Active High). Do Not Float This Pin.
4, 6	NC	
5	GND	Common Ground.
7	OUT2	Channel 2 Output Voltage.
8	OUT1	Channel 1 Output Voltage.

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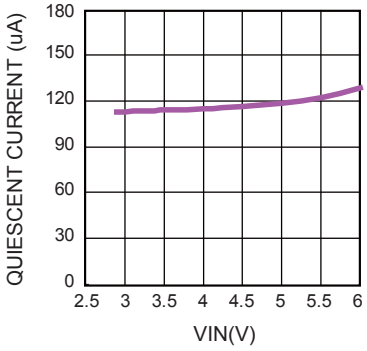
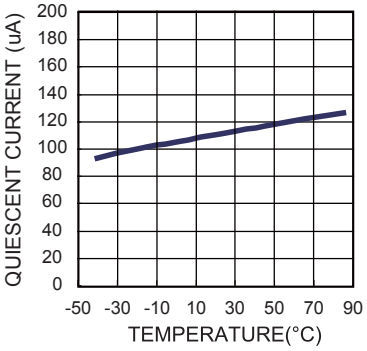
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=3.5V, V_{OUT1}=1.8V, V_{OUT2}=2.5V, I_{OUT1}=I_{OUT2}=0mA, C_{IN}=C_{OUT1}=C_{OUT2}=1μF, EN1=EN2=V_{IN}, Typical Value at T_A = 25°C for Both Channel Enabled.

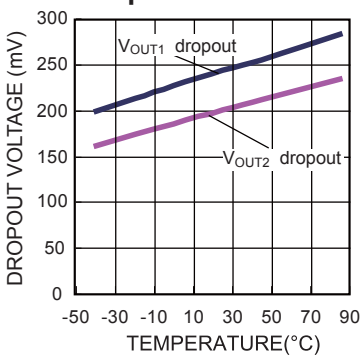
Quiescent Current vs. Supply Voltage



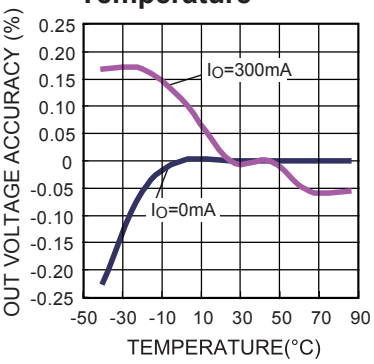
Quiescent Current vs. Temperature



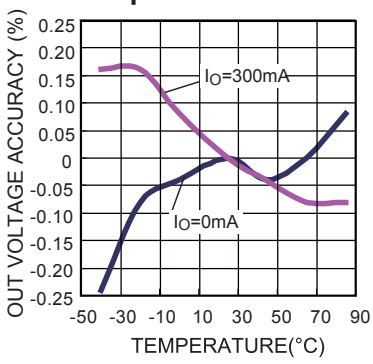
Dropout Voltage vs. Temperature



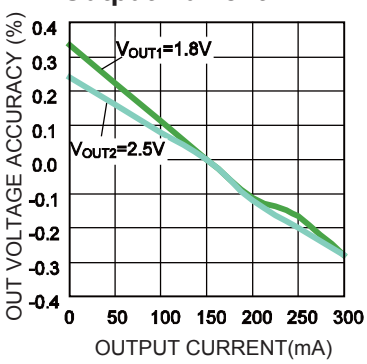
Out1 Voltage Accuracy vs. Temperature



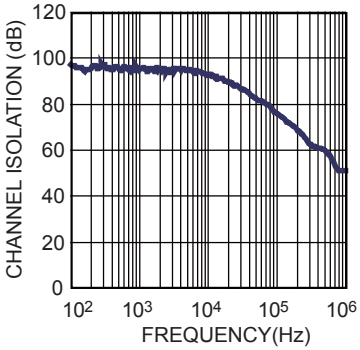
Out2 Voltage Accuracy vs. Temperature



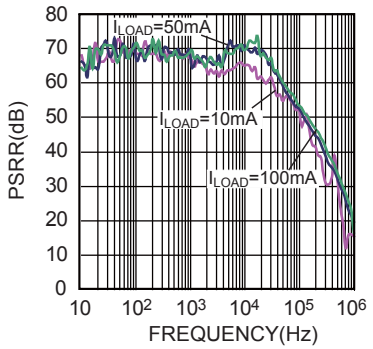
Out Voltage Accuracy vs. Output Current



Channel-to-Channel Isolation vs. Frequency

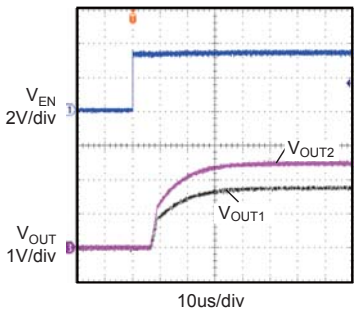


Power Supply Rejection Ratio vs. Frequency



EN Start Up Waveform

V_{IN}=3.5V, I_{OUT1}=I_{OUT2}=50mA



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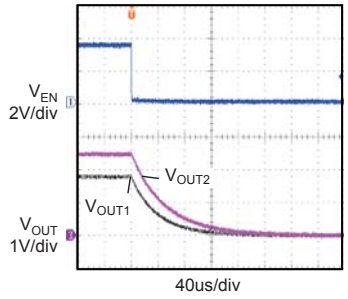
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=3.5V, V_{OUT1}=1.8V, V_{OUT2}=2.5V, I_{OUT1}=I_{OUT2}=0mA, C_{IN}=C_{OUT1}=C_{OUT2}=1μF, EN1=EN2=V_{IN}, Typical Value at T_A = 25°C for Both Channel Enabled.

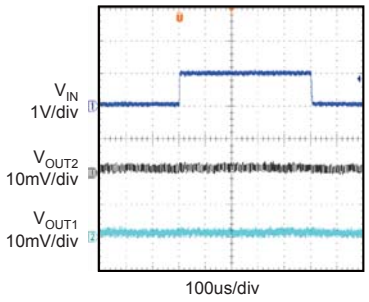
EN Shut Down Waveform

V_{IN}=3.5V, I_{OUT1}=I_{OUT2}=50mA



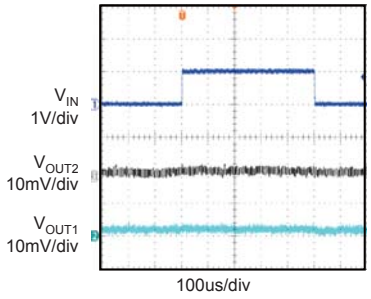
Line Transient Response

V_{IN}=3V to 4V, I_{LOAD}=1mA



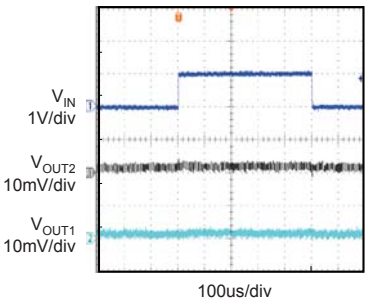
Line Transient Response

V_{IN}=3V to 4V, I_{LOAD}=10mA



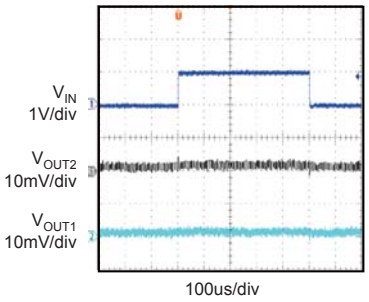
Line Transient Response

V_{IN}=3V to 4V, I_{LOAD}=50mA



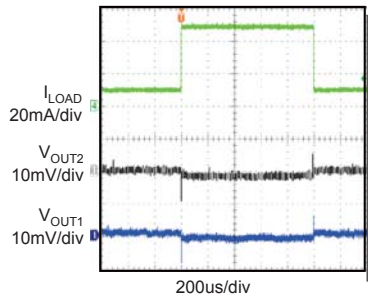
Line Transient Response

V_{IN}=3V to 4V, I_{LOAD}=100mA



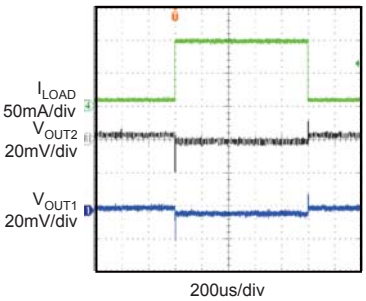
Load Transient Response

I_{LOAD}=10 to 50mA, with Resistor Load



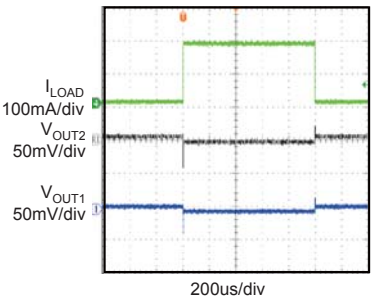
Load Transient Response

I_{LOAD}=10 to 100mA, with Resistor Load



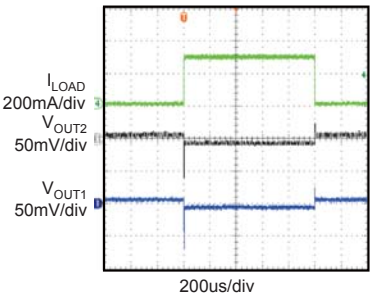
Load Transient Response

I_{LOAD}=10 to 200mA, with Resistor Load



Load Transient Response

I_{LOAD}=10 to 300mA, with Resistor Load



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BLOCK DIAGRAM

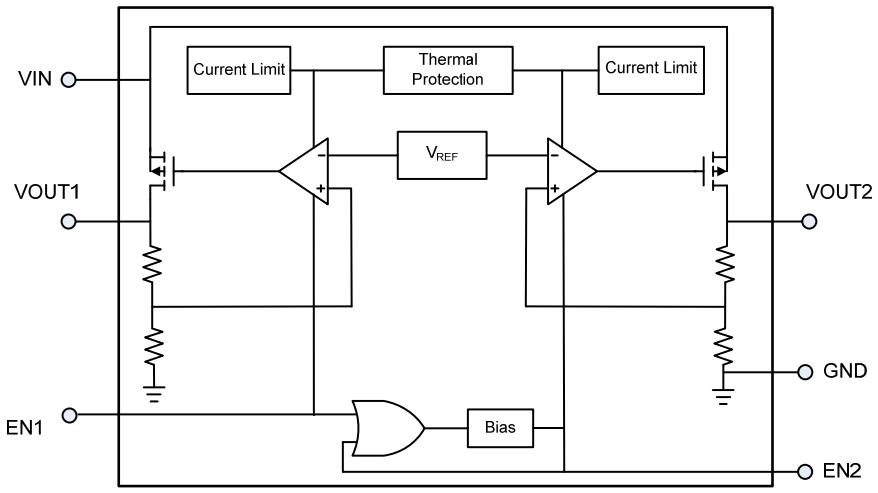

Figure1—Function Block Diagram

OPERATION

The MP20041 integrates two low noise, low dropout, low quiescent current and high PSRR linear regulators. It is intended for use in devices that require very low voltage, low quiescent current power such as wireless LAN, battery-powered equipment and hand-held equipment. The MP20041 uses internal PMOSs as the pass elements and features internal thermal shutdown and internal current limit circuits.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage of MP20041 is very low.

Shutdown

The MP20041 can be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin will turn the device on. When the EN pin is low, the regulator output is off. The EN pin should be tied to VIN to keep the regulator output always on if the application does not require the shutdown feature. Do not float the EN pin.

Current Limit

The MP20041 includes two independent current limit structures which monitor and control each PMOS's gate voltage limiting the guaranteed maximum output current to 300mA.

Thermal Protection

Thermal protection turns off the PMOS when the junction temperature exceeds +140ºC, allowing the IC to cool. When the IC's junction temperature drops by 10ºC, the PMOS will be turned on again. Thermal protection limits total power dissipation in the MP20041. For reliable operation, junction temperature should be limited to 125 ºC maximum.

Load-Transient Considerations

The output response of load-transient consists of a DC shift and transient response. Because of the excellent load regulation of MP20041, the DC shift is very small. The output voltage transient depends on the output capacitor's value and the ESR. Increasing the capacitance and decreasing the ESR will improve the transient response. Typical output voltage transient spike of MP20041 for a step change in the load current from 10mA to 100mA is tens mV.

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APPLICATION INFORMATION

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature difference between the junction and ambient air, and the rate of airflow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where ($T_{Junction}$ - $T_{Ambient}$) is the temperature difference between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connect the GND pin of MP20041 to ground using a large pad or ground plane helps to channel heat away.

Input Capacitor Selection

Using a capacitor whose value is >0.47μF on the MP20041 input and the amount of capacitance can be increased without limit. Larger values will help improve line transient response with the drawback of increased size. Ceramic capacitors are preferred, but tantalum capacitors may also suffice.

Output Capacitor Selection

The MP20041 is designed specifically to work with very low ESR ceramic output capacitor in space-saving and performance consideration. A ceramic capacitor in the range of 0.47μF and 10μF, and with ESR lower than 1.2Ω is suitable for the MP20041 application circuit. Output capacitor of larger values will help to improve load transient response and reduce noise with the drawback of increased size.

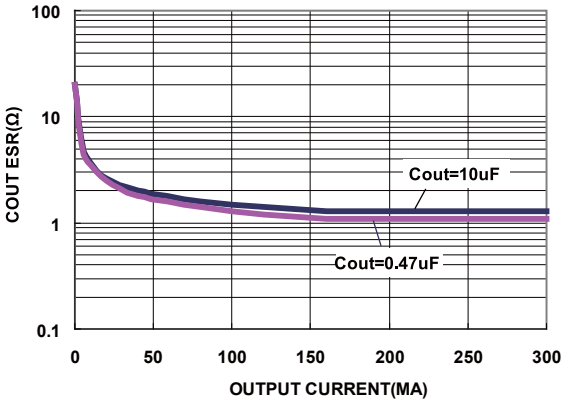

Figure 2—Relationship between ESR and LDO Stability

Reverse Current Path

The PMOS used in the MP20041 has an inherent diode connected between input and output (see Figure3). If V_{OUT} - V_{IN} is more than a diode-drop, this diode gets forward biased and starts to conduct. To avoid misoperation, an external Schottky connected in parallel with the internal parasitic diode prevents it from being turned on by limiting the voltage drop across it to about 0.3V (see Figure 4).

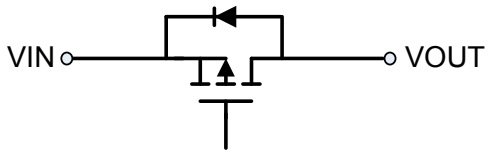

Figure 3—Inherent Diode Connected between Each Regulator Input and Output

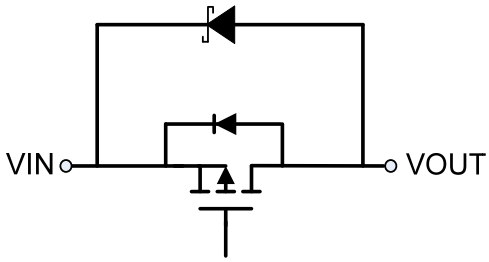

Figure 4—External Schottky Diode Connected in Parallel with the Internal Parasitic Diode

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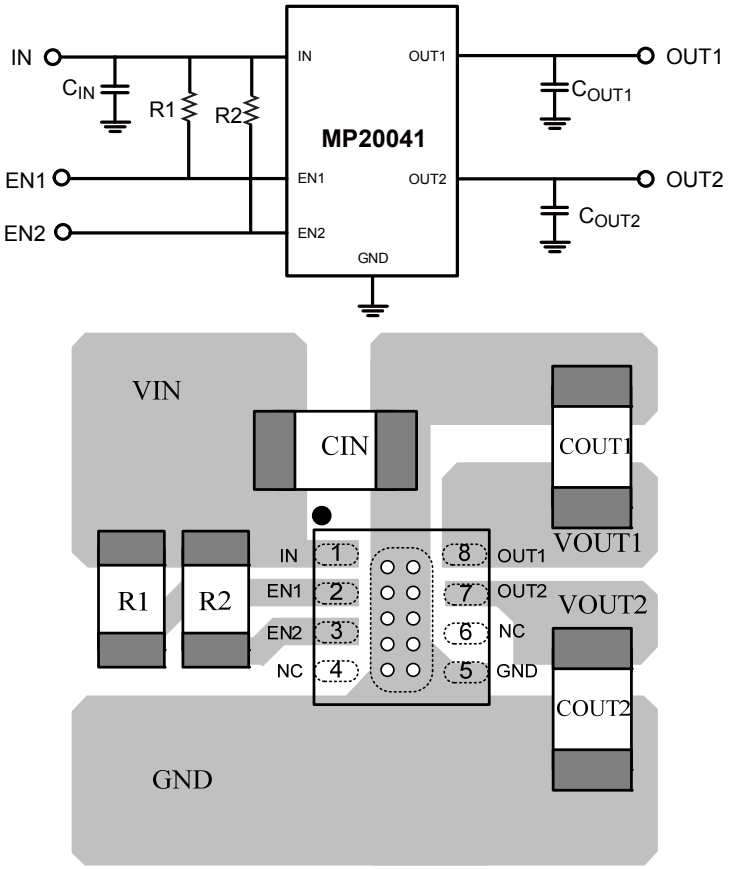
PCB layout guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take figure 5 for reference.

1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
3) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



Top Layer

Figure 5—PCB Layout

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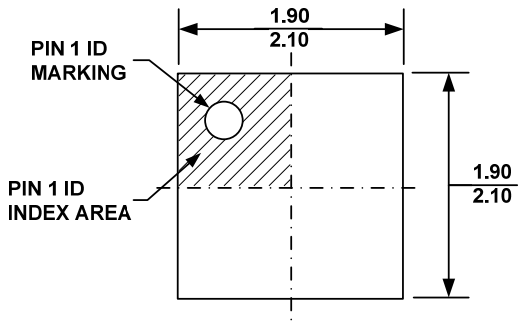
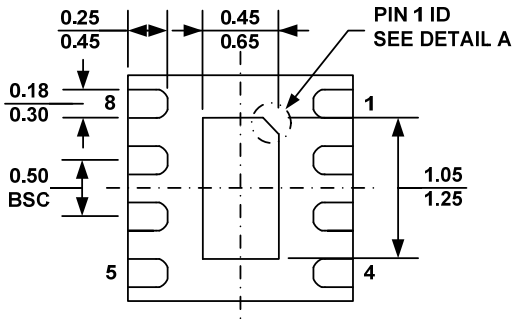
PACKAGE INFORMATION

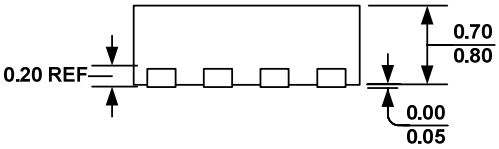
2mm x 2mm TQFN8



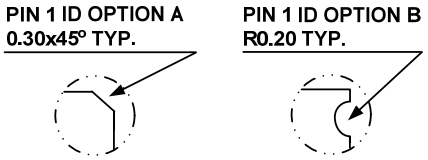
TOP VIEW



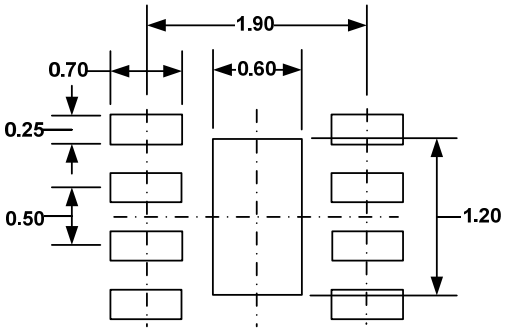
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCCD-3.
5) DRAWING IS NOT TO SCALE.

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