

### DESCRIPTION

The MP1925 is a high-frequency, half-bridge, N-channel power MOSFET driver. Its low-side and high-side driver channels are controlled independently and matched with less than 5ns of time delay. Under-voltage lockout (UVLO) on both the high-side and low-side supplies forces the outputs low in the event that the supply is insufficient. The integrated bootstrap diode reduces the external component count.

The MP1925 is available in a QFN-8 (4mmx4mm) package.

### FEATURES

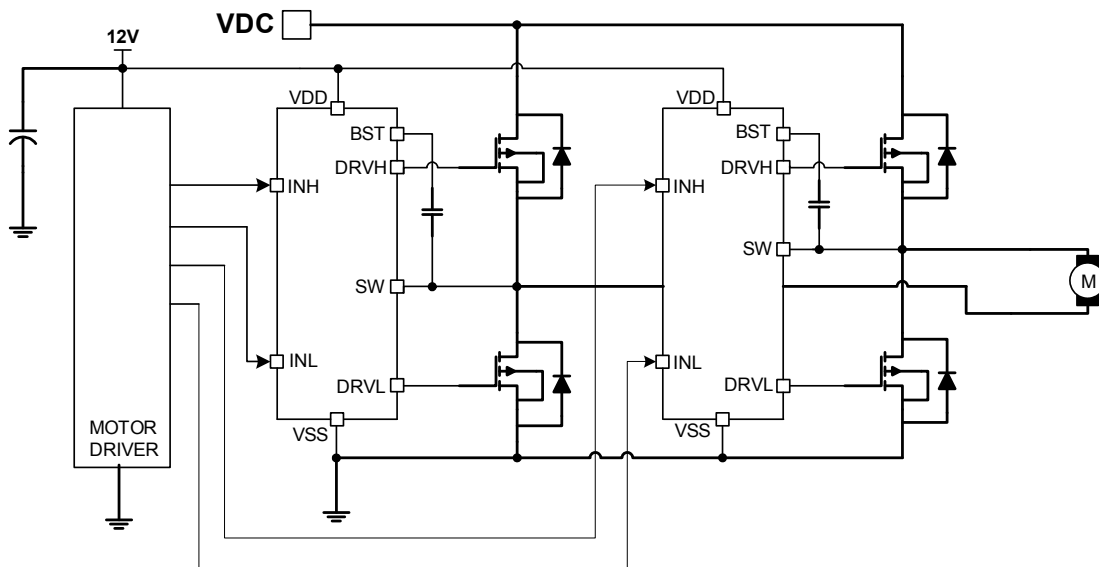
- Drives an N-Channel MOSFET Half-Bridge
- 115V Bootstrap Voltage Range
- On-Chip Bootstrap Diode
- Typical Propagation Delay of 20ns
- Gate Driver Matching of Less than 5ns
- Drives a 2.2nF Load with 15ns of Rise Time and 10ns of Fall Time at 12V VDD
- TTL-Compatible Input
- Quiescent Current of Less than 150µA
- UVLO for Both High-Side and Low-Side Gate Drivers
- Available in a QFN-8 (4mmx4mm) Package

### APPLICATIONS

- Motor Drivers
- Telecom Half-Bridge Power Supplies
- Avionics DC/DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

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### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1925HR	QFN-8 (4mmx4mm)	See Below

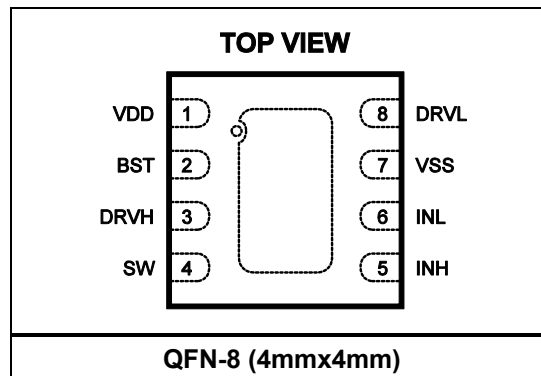
\* For Tape & Reel, add suffix -Z (e.g. MP1925HR-Z)  
 For RoHS compliant packaging, add suffix -LF (e.g. MP1925HR-LF-Z)

### TOP MARKING

**MPSYWW**  
**MP1925**  
**LLLLLL**

MPS: MPS prefix  
 Y: Year code  
 WW: Week code  
 MP1925: Part number  
 LLLLLL: Lot number

### PACKAGE REFERENCE



### PIN FUNCTIONS

Pin #	Name	Description
1	VDD	<b>Supply input.</b> VDD supplies power to the internal circuitry. Place a decoupling capacitor to ground close to VDD to ensure a stable and clean supply.
2	BST	<b>Bootstrap.</b> BST is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
3	DRVH	<b>Floating driver output.</b>
4	SW	<b>Switching node.</b>
5	INH	<b>Control signal input for the floating driver.</b>
6	INL	<b>Control signal input for the low-side driver.</b>
7	VSS, exposed pad	<b>Chip ground.</b> Connect the exposed pad to VSS for proper thermal operation.
8	DRVL	<b>Low-side driver output.</b>

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

Supply voltage ( $V_{DD}$ )	-0.3V to +18V
SW voltage ( $V_{SW}$ )	-5.0V to +105V
BST voltage ( $V_{BST}$ )	-0.3V to +115V
BST to SW	-0.3V to +18V
DRVH to SW	-0.3V to (BST - SW) + 0.3V
DRVL to VSS	-0.3V to ( $V_{DD}$ + 0.3V)
All other pins	-0.3V to ( $V_{DD}$ + 0.3V)
Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup>	
QFN-8 (4mmx4mm)	2.66W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

**Recommended Operating Conditions** <sup>(3)</sup>

Supply voltage ( $V_{DD}$ )	8.0V to 15.0V
SW voltage ( $V_{SW}$ )	-1.0V to +100V
SW slew rate	<50V/ns
Operating junction temp ( $T_J = T_A$ )	
	-40°C to +125°C

<b>Thermal Resistance</b> <sup>(4)</sup>	$\theta_{JA}$	$\theta_{JC}$
QFN-8 (4mmx4mm)	47	7
	°C/W	

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{BST} - V_{SW} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ , no load at DRVH and DRVL,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Supply Currents</b>						
VDD quiescent current	$I_{DDQ}$	INL = INH = 0		110	150	$\mu A$
VDD operating current	$I_{DDO}$	$f_{SW} = 500kHz$		9		mA
Floating driver quiescent current	$I_{BSTQ}$	INL = INH = 0		60	90	$\mu A$
Floating driver operating current	$I_{BSTO}$	$f_{SW} = 500kHz$		8		mA
Leakage current	$I_{LK}$	BST = SW = 100V		0.05	1	$\mu A$
<b>Inputs</b>						
INL/INH high				2	2.4	V
INL/INH low			1	1.4		V
INL/INH internal pull-down resistance	$R_{IN}$			185		k $\Omega$
<b>Under-Voltage Protection</b>						
VDD rising threshold	$V_{DDR}$		6	6.8	7.2	V
VDD hysteresis	$V_{DDH}$			0.4		V
BST-SW rising threshold	$V_{BSTR}$		5.8	6.5	6.9	V
BST-SW hysteresis	$V_{BSTH}$			0.4		V
<b>Bootstrap Diode</b>						
Bootstrap diode VF at 100 $\mu A$	$V_{F1}$			0.5		V
Bootstrap diode VF at 100mA	$V_{F2}$			0.95		V
Bootstrap diode dynamic R	$R_D$	At 100mA		2.5		$\Omega$
<b>Low-Side Gate Driver</b>						
Low-level output voltage	$V_{OLL}$	$I_o = 100mA$		0.1		V
High-level output voltage to rail	$V_{OHL}$	$I_o = -100mA$		0.19		V
Source current <sup>(5)</sup>	$I_{OHL}$	$V_{DRVL} = 0V, V_{DD} = 12V$		3		A
		$V_{DRVL} = 0V, V_{DD} = 16V$		4.7		A
Sink current <sup>(5)</sup>	$I_{OLL}$	$V_{DRVL} = V_{DD} = 12V$		4.5		A
		$V_{DRVL} = V_{DD} = 16V$		6		A
<b>Floating Gate Driver</b>						
Low-level output voltage	$V_{OLH}$	$I_o = 100mA$		0.1		V
High-level output voltage to rail	$V_{OHH}$	$I_o = -100mA$		0.19		V
Source current <sup>(5)</sup>	$I_{OHH}$	$V_{DRVH} = 0V, V_{DD} = 12V$		2.6		A
		$V_{DRVH} = 0V, V_{DD} = 16V$		4		A
Sink current <sup>(5)</sup>	$I_{OLH}$	$V_{DRVH} = V_{DD} = 12V$		4.5		A
		$V_{DRVH} = V_{DD} = 16V$		5.9		A

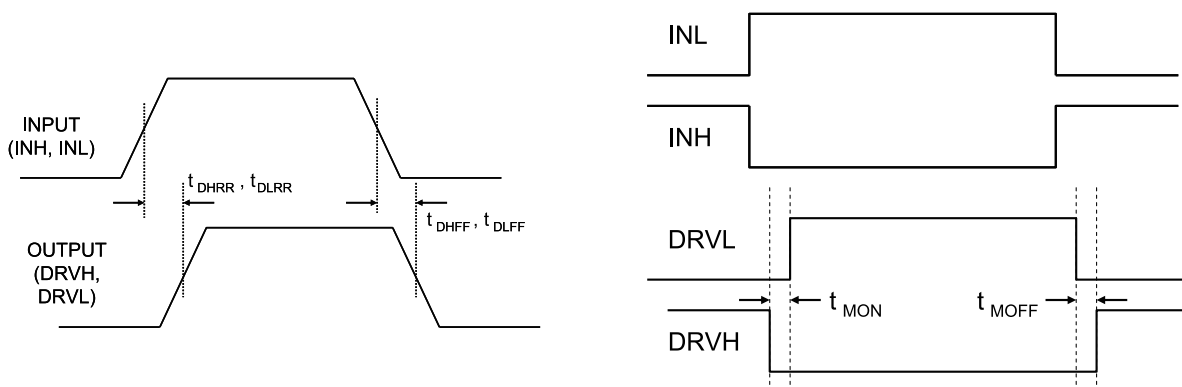
**ELECTRICAL CHARACTERISTICS (continued)**

$V_{DD} = V_{BST} - V_{SW} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ , no load at DRVH and DRVL,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Switching Specification – Low-Side Gate Driver</b>						
Turn-off propagation delay INL falling to DRVL falling	$t_{DLFF}$			20		ns
Turn-on propagation delay INL rising to DRVL rising	$t_{DLRR}$			20		
DRVL rise time		$C_L = 2.2nF$		15		ns
DRVL fall time		$C_L = 2.2nF$		10		ns
<b>Switching Specification – Floating Gate Driver</b>						
Turn-off propagation delay INH falling to DRVH falling	$t_{DHFF}$			20		ns
Turn-on propagation delay INH rising to DRVH rising	$t_{DHRR}$			20		ns
DRVH rise time		$C_L = 2.2nF$		15		ns
DRVH fall time		$C_L = 2.2nF$		10		ns
<b>Switching Specification – Matching</b>						
Floating driver turn-off to low-side driver turn-on <sup>(5)</sup>	$t_{MON}$			1	5	ns
Low-side driver turn-off to floating driver turn-on <sup>(5)</sup>	$t_{MOFF}$			1	5	ns
Minimum input pulse width that changes the output <sup>(5)</sup>	$t_{PW}$				50	ns
Bootstrap diode turn-on or turn- off time <sup>(5)</sup>	$t_{BS}$			10		ns
Thermal shutdown				150		$^{\circ}C$
Thermal shutdown hysteresis				25		$^{\circ}C$

**Note:**

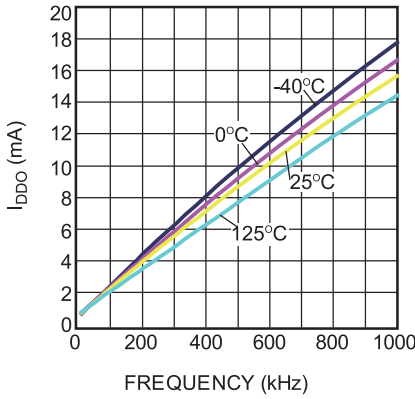
5) Guaranteed by design.

**TIMING DIAGRAM**

**Figure 1: Timing Diagram**

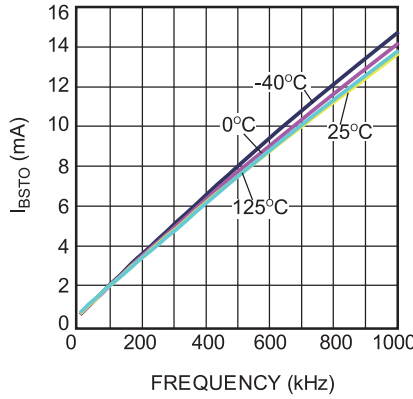
## TYPICAL CHARACTERISTICS

$V_{DD} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

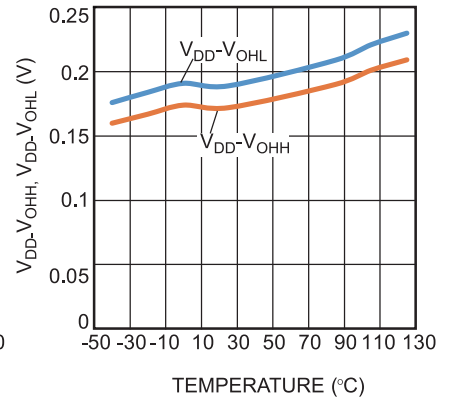
**$I_{DDO}$  Operation Current vs. Frequency**



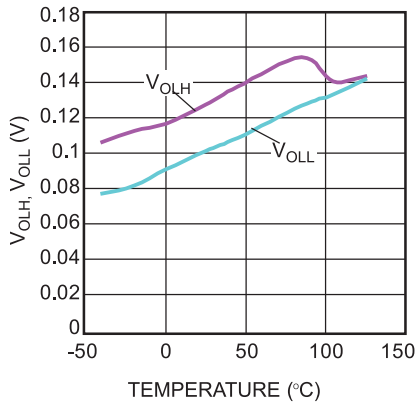
**$I_{BSTO}$  Operation Current vs. Frequency**



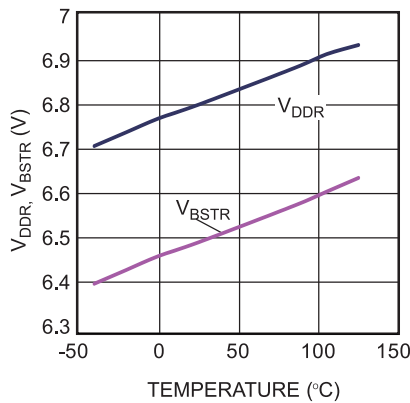
**High-Level Output Voltage vs. Temperature**



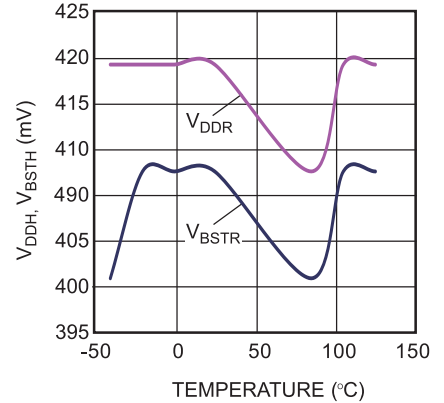
**Low-Level Output Voltage vs. Temperature**



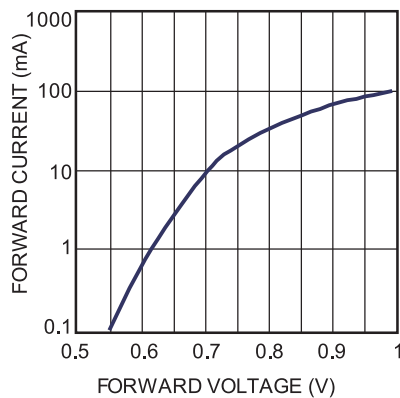
**Under-Voltage Lockout Threshold vs. Temperature**



**Under-Voltage Lockout Hysteresis vs. Temperature**

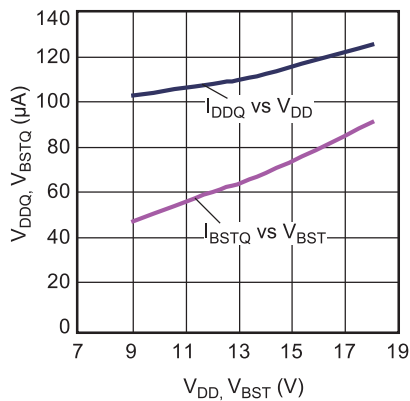


**Bootstrap Diode I-V Characteristic**

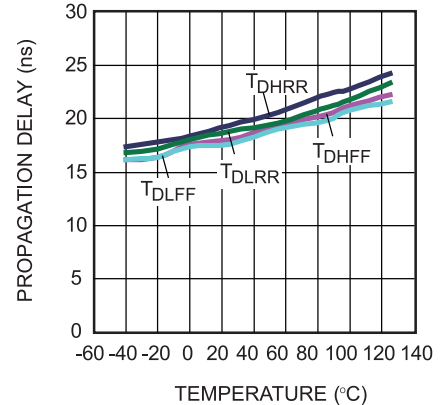


**Quiescent Current vs. Voltage**

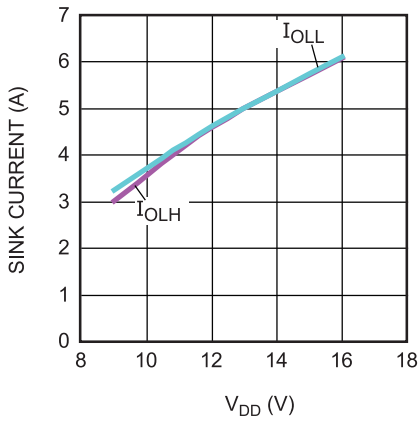
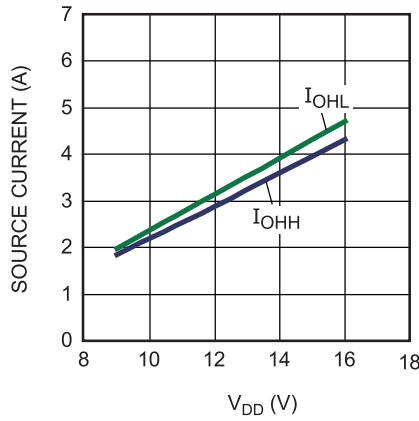
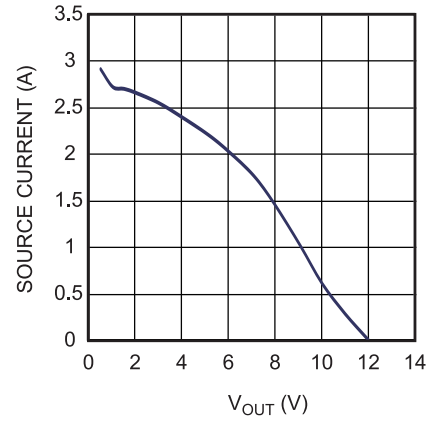
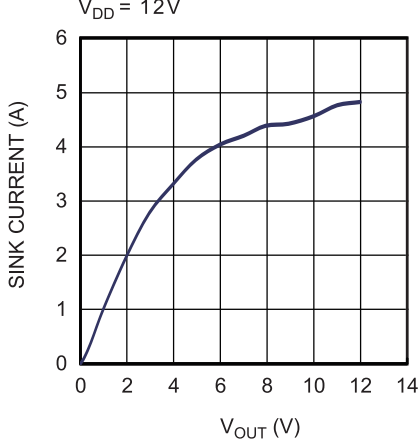
$INH = INL = 0V$



**Propagation Delay vs. Temperature**



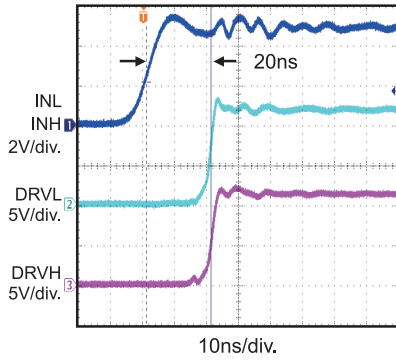
**TYPICAL CHARACTERISTICS (continued)**
 $V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25^\circ C$ , unless otherwise noted.

**Sink Current vs.  $V_{DD}$  Voltage**

**Source Current vs.  $V_{DD}$  Voltage**

**Source Current vs. Output Voltage**  
 $V_{DD} = 12V$ 

**Sink Current vs. Output Voltage**  
 $V_{DD} = 12V$ 


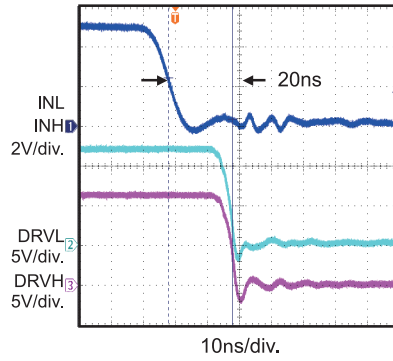
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

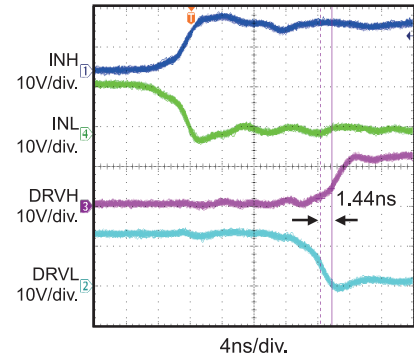
Turn-On Propagation Delay



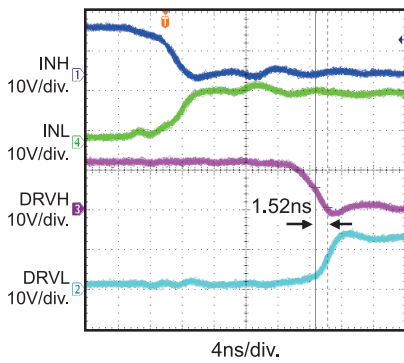
Turn-Off Propagation Delay



Gate Drive Matching  $t_{MOFF}$

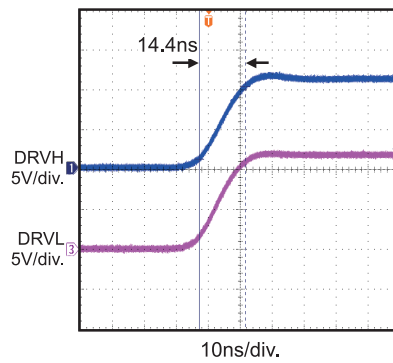


Gate Drive Matching  $t_{MON}$



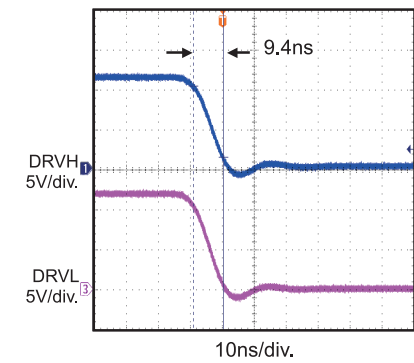
Drive Rise Time

2.2nF load



Drive Fall Time

2.2nF load





### FUNCTIONAL BLOCK DIAGRAM

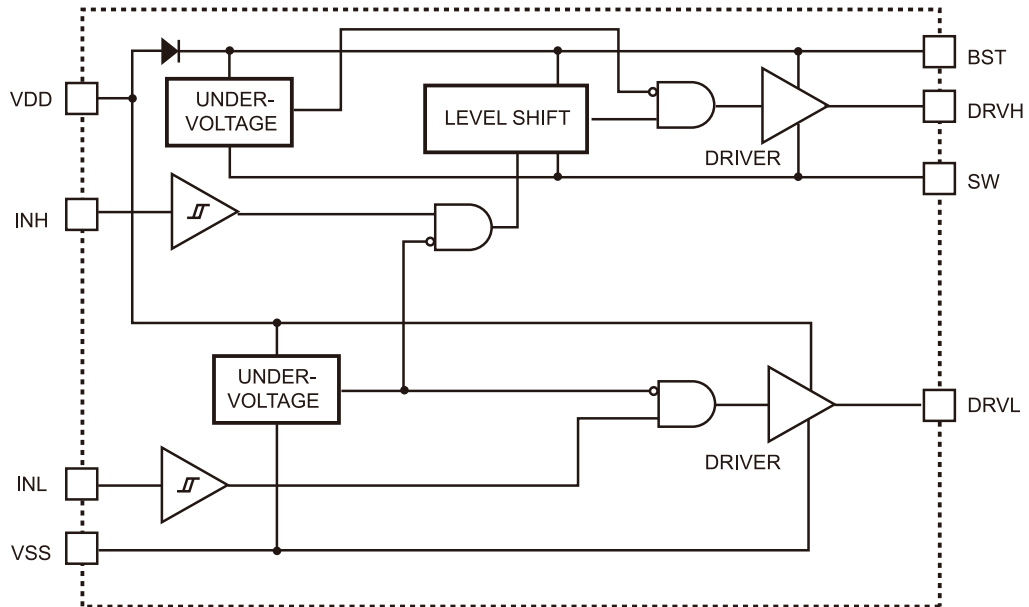
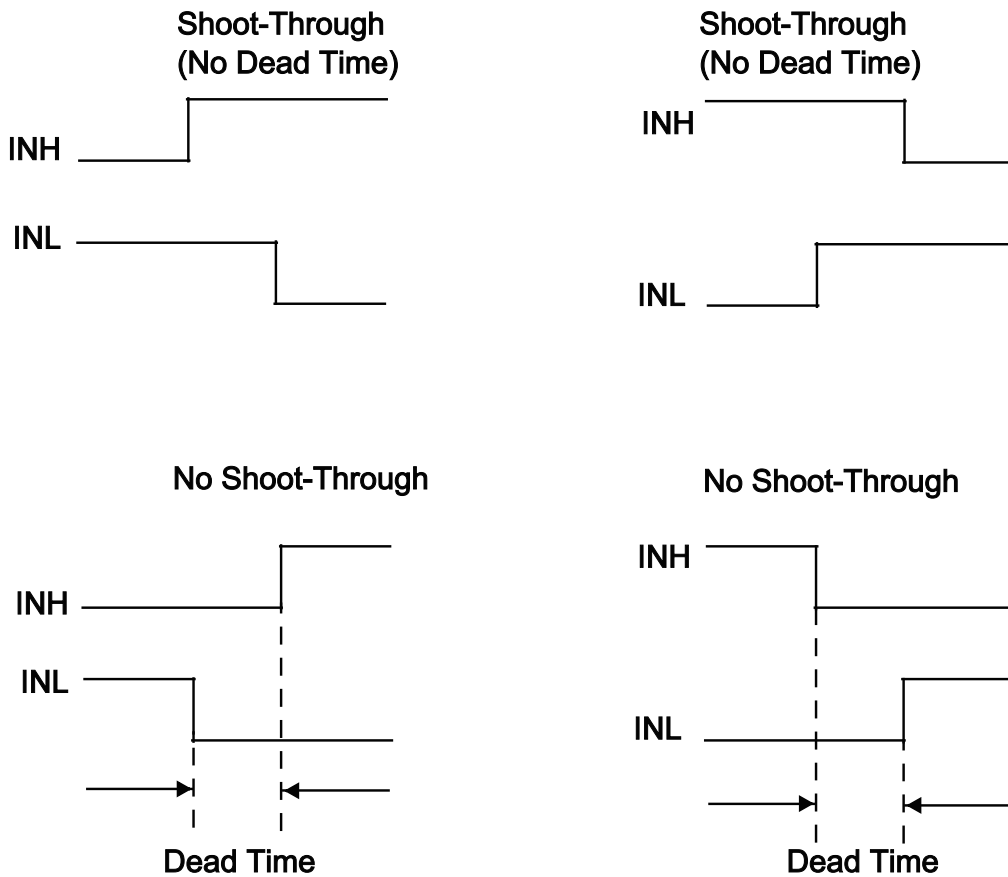


Figure 2: Functional Block Diagram

### APPLICATION INFORMATION

The input signals of INH and INL can be controlled independently. If both INH and INL control the high-side and low-side MOSFETs of the same bridge, set a sufficient dead time

between INH and INL low (and vice versa) to avoid shoot-through (see Figure 3). Dead time is defined as the time interval between INH low and INL low.



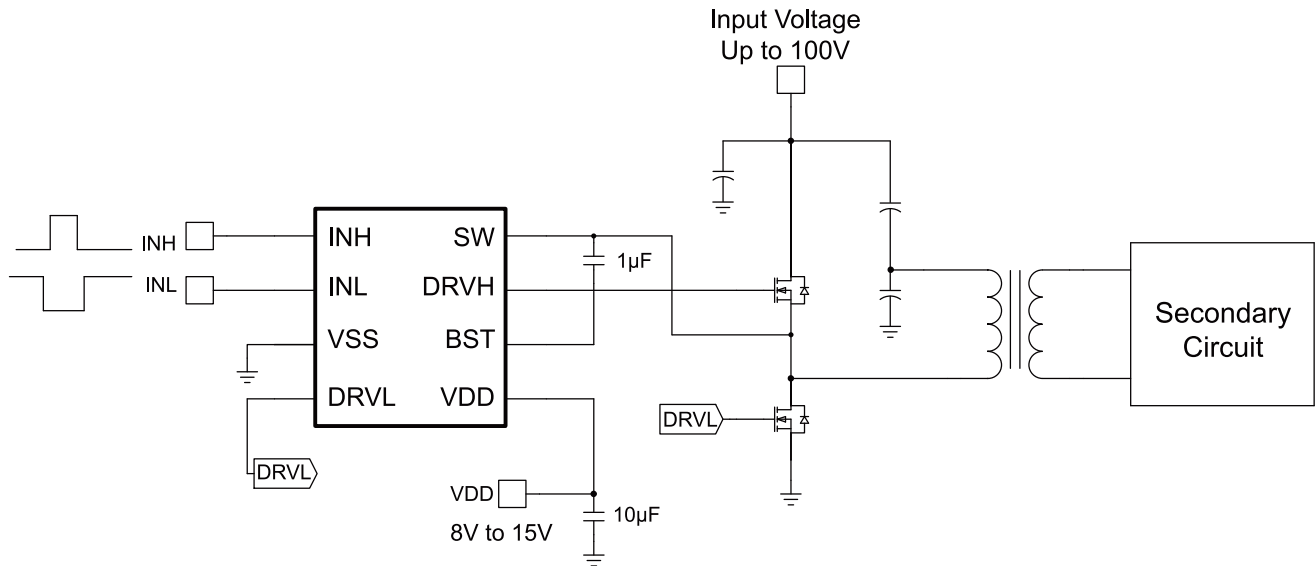
**Figure 3: Shoot-Through Timing Diagram**

## REFERENCE DESIGN CIRCUITS

### Half-Bridge Converter

The MP1925 drives the MOSFETS via alternating signals with dead time in half-bridge converter topology. The input voltage can rise up

to 100V with the alternating signals (INH and INL) coming from the PWM controller (see Figure 4).

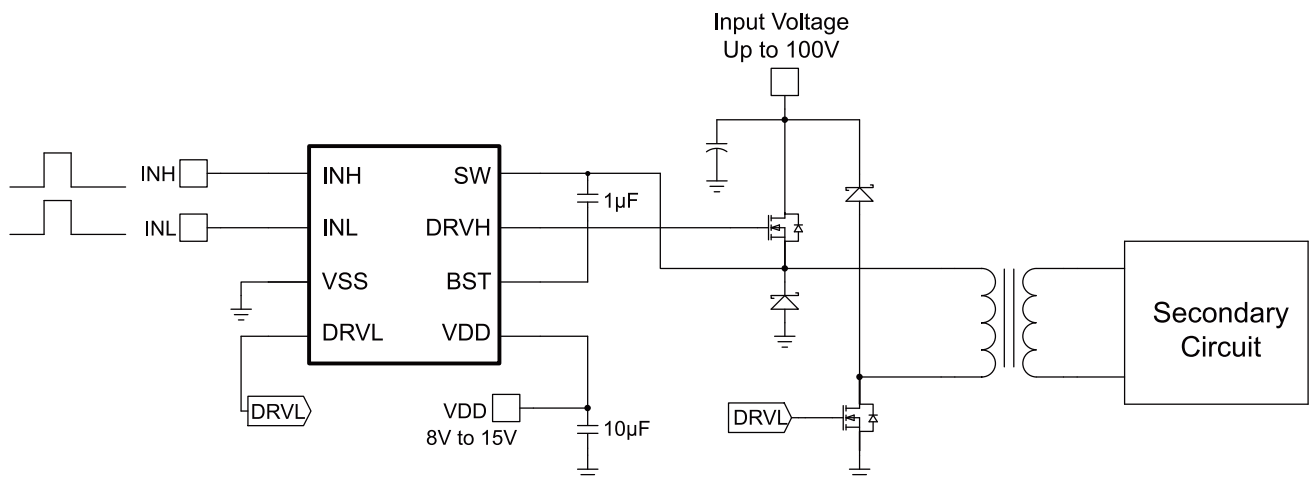


**Figure 4: Half-Bridge Converter**

### Two-Switch Forward Converter

In two-switch forward converter topology, both MOSFETs turn on and off simultaneously. The input signals (INH and INL) come from a PWM controller that senses the output voltage and output current during current mode control.

The Schottky diodes clamp the reverse swing of the power transformer, and must be rated for the input voltage. The input voltage can rise up to 100V (see Figure 5).

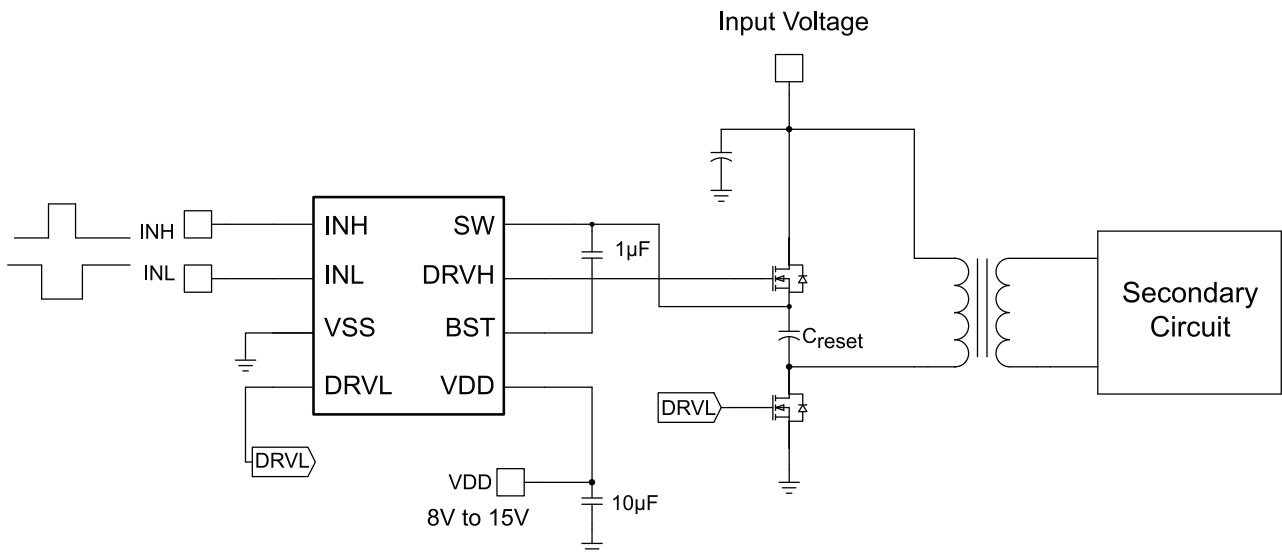


**Figure 5: Two-Switch Forward Converter**

### Active Clamp Forward Converter

In active clamp forward converter topology, the MP1925 drives the MOSFETs with alternating signals. The high-side MOSFET, in conjunction with  $C_{reset}$ , is used to reset the power transformer without loss.

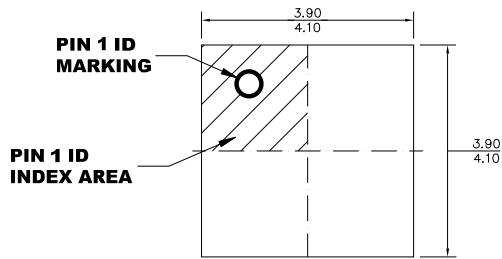
This topology is optimal for running at duty cycles exceeding 50%. The device may not be able to run at 100V in this topology (see Figure 6).



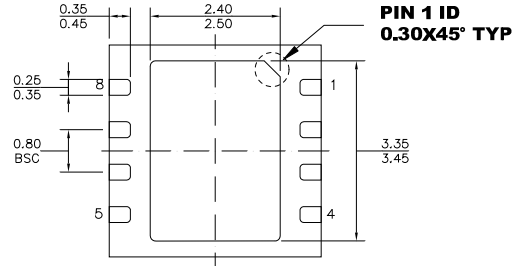
**Figure 6: Active Clamp Forward Converter**

**PACKAGE INFORMATION**

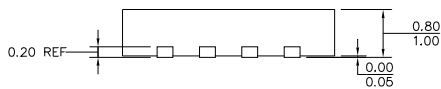
**QFN-8 (4mmx4mm)**



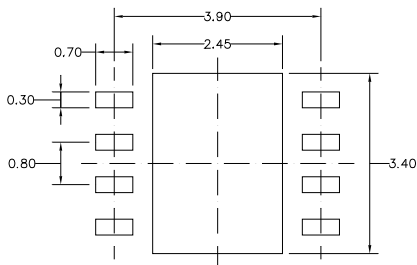
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

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