DESCRIPTION
The MP1924 is a high-frequency, 100V, half-bridge, N-channel, power MOSFET driver. Its low-side and high-side driver channels are independently controlled and matched with less than 5ns in time delay. Under-voltage lockout on both high-side and low-side supplies force their outputs low in case of insufficient supply. The integrated bootstrap diode reduces external component count.

FEATURES
- Drives an N-Channel MOSFET Half Bridge
- 118V \( V_{BST} \) Voltage Range
- On-Chip Bootstrap Diode
- Typical Propagation Delay of 20ns
- Gate Drive Matching of Less than 5ns
- Drives a 2.2nF Load with 15ns Rise Time and 12ns Fall Time at 12V VDD
- TTL-Compatible Input
- Quiescent Current of Less than 150\( \mu \)A
- UVLO for Both High Side and Low Side
- QFN-10 (4mmx4mm) and SOIC-8 Packages

APPLICATIONS
- Motor Drivers
- Telecom Half-Bridge Power Supplies
- Avionics DC-DC Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

“MPS” and “The Future of Analog IC Technology” are Registered Trademarks of Monolithic Power Systems, Inc.
### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP1924HR*</td>
<td>QFN-10 (4x4mm)</td>
<td>See Below</td>
</tr>
<tr>
<td>MP1924HS**</td>
<td>SOIC-8</td>
<td>See Below</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP1924HR–Z)
For RoHS compliant packaging, add suffix –LF (e.g. MP1924HR–LF–Z)

** For Tape & Reel, add suffix –Z (e.g. MP1924HS–Z)
For RoHS compliant packaging, add suffix –LF (e.g. MP1924HS–LF–Z)

### TOP MARKING (MP1924HR)

**MPSYWW**

**MP1924**

**LLLLLL**

MPS: MPS prefix;
Y: year code;
WW: week code;
MP1924: product code of MP1924HR;
LLLLLLL: lot number;

### TOP MARKING (MP1924HS)

**MP1924**

**LLLLLLLL**

**MPSYWW**

MP1924: product code of MP1924HS;
LLLLLLLLL: lot number;
MPS: MPS prefix;
Y: year code;
WW: week code;
**ABSOLUTE MAXIMUM RATINGS**<sup>(1)</sup>

Supply Voltage \(V_{DD}\) ........................................ -0.3V to 18V  
SW Voltage \(V_{SW}\) ........................................ -5.0V to 105V  
BST Voltage \(V_{BST}\) ......................................... -0.3V to 118V  
BST to SW .......................................................... -0.3V to 18V  
DRVH to SW ...................................................... -0.3V to \((\text{BST}_2-\text{SW}) + 0.3V\)  
DRVL to VSS .................................................... -0.3V to \((\text{VDD} + 0.3V)\)  
All Other Pins ................................................因为在-0.3V to \((\text{VDD} + 0.3V)\)

Continuous Power Dissipation \(\text{QFN-10 (4mmx4mm)}\) ......................... 2.66W  
\(\text{SOIC-8} \) ......................................................... 1.3W  

**Junction Temperature** .............................................. 150°C  
**Lead Temperature** .............................................. 260°C  
**Storage Temperature** ........................................... -65°C to 150°C

**Recommended Operating Conditions**<sup>(3)</sup>

- Supply Voltage \(V_{DD}\) ................. 9.0V to 16.0V  
- SW Voltage \(V_{SW}\) ......................... -1.0V to 100V  
- SW Slew Rate .............................................. <50V/\(\text{ns}\)  
- Operating Junction Temp. \(T_J\) ... -40°C to 125°C

**Thermal Resistance**<sup>(4)</sup>  
- \(\theta_{JA}\) \(\quad \theta_{JC}\)  
- \(\text{QFN-10 (4mmx4mm)} \) ....... 47 ...... 7 .... °C/W  
- \(\text{SOIC-8} \) .............................................. 96 ...... 45 ... °C/W

**Notes:**

1) Exceeding these ratings may damage the device.  
2) The maximum allowable power dissipation is a function of the maximum junction temperature \(T_J(\text{MAX})\), the junction-to-ambient thermal resistance \(\theta_{JA}\), and the ambient temperature \(T_A\). The maximum allowable continuous power dissipation at any ambient temperature is calculated by \(P_{D(\text{MAX})} = (T_J(\text{MAX})-T_A)/\theta_{JA}\). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.  
3) The device is not guaranteed to function outside of its operating conditions.  
4) Measured on JESD51-7, 4-layer PCB.
# ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{BST} - V_{SW} = 12V$, $V_{SS} = V_{SW} = 0V$, No load at DRVH and DRVL, $T_A = +25^\circ C$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Supply Currents</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD quiescent current</td>
<td>$I_{DDQ}$</td>
<td>INL = INH = 0</td>
<td>100</td>
<td>150</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>VDD operating current</td>
<td>$I_{DDO}$</td>
<td>fs = 500kHz</td>
<td>9</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Floating driver quiescent current</td>
<td>$I_{BSTQ}$</td>
<td>INL = INH = 0</td>
<td>60</td>
<td>90</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Floating driver operating current</td>
<td>$I_{BSTO}$</td>
<td>fs = 500kHz</td>
<td>7.5</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Leakage current</td>
<td>$I_LK$</td>
<td>BST = SW = 100V</td>
<td>0.05</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td><strong>Inputs</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INL/INH High</td>
<td></td>
<td></td>
<td>2</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>INL/INH Low</td>
<td></td>
<td></td>
<td>1</td>
<td>1.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>INL/INH internal pull-down resistance</td>
<td>$R_{IN}$</td>
<td></td>
<td>185</td>
<td></td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td><strong>Under Voltage Protection</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD rising threshold</td>
<td>$V_{DDR}$</td>
<td></td>
<td>8.1</td>
<td>8.4</td>
<td>8.8</td>
<td>V</td>
</tr>
<tr>
<td>VDD hysteresis</td>
<td>$V_{DDH}$</td>
<td></td>
<td>0.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(BST-SW) rising threshold</td>
<td>$V_{BSTR}$</td>
<td></td>
<td>6.9</td>
<td>7.3</td>
<td>7.7</td>
<td>V</td>
</tr>
<tr>
<td>(BST-SW) hysteresis</td>
<td>$V_{BSTH}$</td>
<td></td>
<td>0.55</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>Bootstrap Diode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bootstrap diode VF @ 100µA</td>
<td>$V_{F1}$</td>
<td></td>
<td>0.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Bootstrap diode VF @ 100mA</td>
<td>$V_{F2}$</td>
<td></td>
<td>0.95</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Bootstrap diode dynamic R</td>
<td>$R_D$</td>
<td>@ 100mA</td>
<td>2</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td><strong>Low Side Gate Driver</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level output voltage</td>
<td>$V_{OLL}$</td>
<td>$I_O = 100mA$</td>
<td>0.08</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High level output voltage to rail</td>
<td>$V_{OHL}$</td>
<td>$I_O = -100mA$</td>
<td>0.23</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Source Current$^{(5)}$</td>
<td>$I_{OHL}$</td>
<td>$V_{DRVL} = 0V$, $V_{DD} = 12V$</td>
<td>3</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DRVL} = 0V$, $V_{DD} = 16V$</td>
<td>4.7</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Sink Current$^{(5)}$</td>
<td>$I_{OLL}$</td>
<td>$V_{DRVL} = V_{DD} = 12V$</td>
<td>4.5</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DRVL} = V_{DD} = 16V$</td>
<td>6</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td><strong>Floating Gate Driver</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level output voltage</td>
<td>$V_{OLH}$</td>
<td>$I_O = 100mA$</td>
<td>0.08</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High level output voltage to rail</td>
<td>$V_{OHH}$</td>
<td>$I_O = -100mA$</td>
<td>0.23</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Source Current$^{(5)}$</td>
<td>$I_{OHH}$</td>
<td>$V_{DRVH} = 0V$, $V_{DD} = 12V$</td>
<td>2.6</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DRVH} = 0V$, $V_{DD} = 16V$</td>
<td>4</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Sink Current$^{(5)}$</td>
<td>$I_{OLH}$</td>
<td>$V_{DRVH} = V_{DD} = 12V$</td>
<td>4.5</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DRVH} = V_{DD} = 16V$</td>
<td>5.9</td>
<td></td>
<td>A</td>
<td></td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS (continued)**

\[ V_{DD} = V_{BST} - V_{SW} = 12V, \ V_{SS} = V_{SW} = 0V, \]  
No load at DRVH and DRVL, \( T_A = +25^\circ C \), unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Switching Spec. --- Low Side Gate Driver</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-off propagation delay</td>
<td>( T_{DLFF} )</td>
<td>INL falling to DRVL falling</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-on propagation delay</td>
<td>( T_{DLRR} )</td>
<td>INL rising to DRVL rising</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRVL rise time</td>
<td></td>
<td>( C_L = 2.2nF )</td>
<td>15</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRVL fall time</td>
<td></td>
<td>( C_L = 2.2nF )</td>
<td>9</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Switching Spec. --- Floating Gate Driver</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-off propagation delay</td>
<td>( T_{DHFF} )</td>
<td>INH falling to DRVH falling</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-on propagation delay</td>
<td>( T_{DHRR} )</td>
<td>INH rising to DRVH rising</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRVH rise time</td>
<td></td>
<td>( C_L = 2.2nF )</td>
<td>15</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRVH fall time</td>
<td></td>
<td>( C_L = 2.2nF )</td>
<td>12</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Switching Spec. --- Matching</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Floating driver turn-off to low side drive turn-on</td>
<td>( T_{MON} )</td>
<td></td>
<td>1</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Low side driver turn-off to floating driver turn-on</td>
<td>( T_{MOFF} )</td>
<td></td>
<td>1</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Minimum input pulse width that changes the output</td>
<td>( T_{PW} )</td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Bootstrap diode turn-on or turn-off time</td>
<td>( T_{BS} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>Thermal shutdown</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal shutdown hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:**

5) Guaranteed by design.

---

**Figure 1: Timing Diagram**

![Timing Diagram](image)
### PIN FUNCTIONS

<table>
<thead>
<tr>
<th>QFN4x4-10 Pin #</th>
<th>SOIC-8 Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>VDD</td>
<td>Supply input. This pin supplies power to all the internal circuitry. Place a decoupling capacitor to ground close to this pin to ensure stable and clean supply.</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>BST</td>
<td>Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>DRVH</td>
<td>Floating driver output.</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>SW</td>
<td>Switching node.</td>
</tr>
<tr>
<td>5, 6</td>
<td></td>
<td>NC</td>
<td>No connection.</td>
</tr>
<tr>
<td>7</td>
<td>5</td>
<td>INH</td>
<td>Control signal input for the floating driver.</td>
</tr>
<tr>
<td>8</td>
<td>6</td>
<td>INL</td>
<td>Control signal input for the low side driver.</td>
</tr>
<tr>
<td>9</td>
<td>7</td>
<td>VSS, exposed pad</td>
<td>Chip ground. Connect exposed pad to VSS for proper thermal operation.</td>
</tr>
<tr>
<td>10</td>
<td>8</td>
<td>DRVL</td>
<td>Low side driver output.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

- **IBSTO Operation Current vs. Frequency**
- **IGDO Operation Current vs. Frequency**
- **High Level Output Voltage vs. Temperature**
- **Undervoltage Lockout Threshold vs. Temperature**
- **Undervoltage Lockout Hysteresis vs. Temperature**
- **Low Level Output Voltage vs. Temperature**
- **Bootstrap Diode I-V Characteristic**
- **Quiescent Current vs. Voltage**
- **Propagation Delay vs. Temperature**
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

Sink Current vs. $V_{DD}$ Voltage

Source Current vs. $V_{DD}$ Voltage

Source Current vs. Output Voltage

Sink Current vs. Output Voltage

$V_{DD} = 12V$
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

Turn-on Propagation Delay

Turn-off Propagation Delay

Gate Drive Matching $T_{MOFF}$

Gate Drive Matching $T_{MON}$

Drive Rise Time

Drive Fall Time

2.2nF Load

10ns/div.

4ns/div.

10ns/div.

10ns/div.
Figure 2: Function Block Diagram
APPLICATION

The input signals of INH and INL can be controlled independently. If both INH and INL control the high-side MOSFET and low-side MOSFET of the same bridge, then users must avoid shoot through by setting sufficient dead time between INH and INL low, and vice versa. See Figure 3 below. Dead time is defined as the time interval between INH low and INL low.

Shoot through
(No dead time)

INH

INL

No Shoot through

Dead time

INH

INL

INH

INL

INH

INL

Figure 3: Shoot-Through Timing Diagram
REFERENCE DESIGN CIRCUITS

Half Bridge Converter

The MP1924 drives the MOSFETs with alternating signals (with dead time) in half-bridge converter topology. Therefore, from the PWM controller drives INH and INL with alternating signals the input voltage can go up to 100V.

![Figure 4: Half Bridge Converter](image)

Two-Switch Forward Converter

In two-switch forward converter topology, both MOSFETs are turned on and off simultaneously. The input signal (INH and INL) comes from a PWM controller that senses the output voltage (and output current during current-mode control). The Schottky diodes clamp the reverse swing of the power transformer and must be rated for the input voltage. The input voltage can go up to 100V.

![Figure 5: Two-Switch Forward Converter](image)
Active-Clamp Forward Converter

In active-clamp forward converter topology, the MP1924 drives the MOSFETs with alternating signals. The high-side MOSFET, in conjunction with $C_{\text{reset}}$, is used to reset the power transformer in a lossless manner.

This topology lends itself well to run at duty cycles exceeding 50%. The device may not be able to run at 100V under this topology.

![Active-Clamp Forward Converter Diagram](image-url)

**Figure 6 Active-Clamp Forward Converter**
PACKAGE INFORMATION

QFN-10 (4mm×4mm)

NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

RECOMMENDED LAND PATTERN
MP1924—100V, 4A HIGH FREQUENCY HALF-BRIDGE GATE DRIVER

SOIC-8

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.