DESCRIPTION
The MP1906 is a high-performance, 80V, gate driver that can drive two external N-MOSFETs in a half-bridge configuration with a 12V gate supply. It accepts independent gate input signals and provides shoot-through prevention. During under-voltage lockout, the output of the high- and low-side drivers goes low to prevent erratic operation under low supply conditions.

The high-current driving capability and short dead time make it suitable for high-power and high-efficiency power applications, such as telecom DC-DC converters. The compact 8-pin SOIC package minimizes the component count and the board space.

FEATURES
- Drives Two Low-Cost, High-Efficiency N-MOSFETs
- 10V-16V Gate Drive Supply
- 3.3V, 5V Logic Compatibility
- 80ns Propagation Delay
- Less than 90μA Quiescent Current
- Under-Voltage Lockout for Both Channels
- Input-Signal-Overlap Protection
- Internal 150ns Dead Time
- Available in a Compact 8-pin SOIC Package

APPLICATIONS
- Motor Drivers
- Half-Bridge Power Supplies
- Avionics DC-DC Converters
- Active-Clamp Forward Converters

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ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP1906DS</td>
<td>SOIC8</td>
<td>MP1906</td>
</tr>
</tbody>
</table>

*For Tape & Reel, add suffix –Z (e.g. MP1906DS–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP1906DS–LF–Z)

PACKAGE REFERENCE

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage $V_{CC}$ ......................... -0.3V to +18V
Voltage on SW $V_{SW}$ ................................. -0.3V (-5V < 10ns) to +100V
Voltage on BT $V_{BT}$ ........................... $V_{SW}$ +18V
Logic Inputs ...........................................-0.3 to $(V_{CC}+6.5V)$, or 18.5V for $V_{CC}$ ≥ 12V
Continuous Power Dissipation $(T_{A} = 25^\circ C)$ (2) ................................. 1.4W
Junction Temperature ............... -40°C to +150°C
Lead Temperature (Solder 10sec).............260°C
Storage Temperature...............-55°C to +150°C

Recommended Operating Conditions (3)

Input Voltage $V_{CC}$ ......................... 10V to 16V
Maximum Voltage on SW $V_{SW}$ .............. 80V
Logic Inputs ...........................................0V to $V_{CC}$
Voltage slew rate on SW ...................... < 50V/ns
PWM frequency ................................. < 300kHz
Operating Junction Temp. $(T_{J})$ ........................ -40°C to 125°C

Thermal Resistance (4) $\theta_{JA}$  $\theta_{JC}$
SOIC8................................. 90...... 45... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J}$(MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_{A}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D}$(MAX) = ($T_{J}$(MAX) - $T_{A}$)$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
## ELECTRICAL CHARACTERISTICS

*V_{CC} = 12V, V_{SW}=0V, no load on TG or BG, T_A = 25^\circ C, unless otherwise noted.*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Supply Current</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{CC} quiescent current</td>
<td>I_{CCQ}</td>
<td>V_{LPWM}=5V, V_{HPWM}= 0V</td>
<td>70</td>
<td>90</td>
<td>110</td>
<td>μA</td>
</tr>
<tr>
<td>V\textsubscript{CC} operation current</td>
<td>I_{CC}</td>
<td>f=50kHz, C_{LOAD BG}=1nF</td>
<td>0.9</td>
<td>1.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Bootstrap quiescent current</td>
<td>I_{BTQ}</td>
<td>V_{LPWM}=5V, V_{HPWM}= 0V</td>
<td>30</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Bootstrap operation current</td>
<td>I_{BT}</td>
<td>f=50kHz, C_{LOAD TG}=1nF</td>
<td>0.7</td>
<td>1</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>SW BT leakage current</td>
<td>I_{LK}</td>
<td>V_{SW}=V_{BT}=80V</td>
<td>0.1</td>
<td>0.5</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td><strong>Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LPWM falling threshold</td>
<td>V_{LPWMF}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>LPWM rising threshold</td>
<td>V_{LPWMR}</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>HPWM falling threshold</td>
<td>V_{HPWMF}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>HPWM rising threshold</td>
<td>V_{HPWMR}</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>Under-Voltage Protection (UVLO)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{CC} rising threshold</td>
<td>V_{CCHR}</td>
<td></td>
<td>8.2</td>
<td>8.8</td>
<td>9.4</td>
<td>V</td>
</tr>
<tr>
<td>V\textsubscript{CC} threshold hysteresis</td>
<td>V_{CCHH}</td>
<td></td>
<td></td>
<td></td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>Bootstrap rising threshold</td>
<td>V_{BTCHR}</td>
<td></td>
<td>4.5</td>
<td>5.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>Bootstrap threshold hysteresis</td>
<td>V_{BTCHH}</td>
<td></td>
<td></td>
<td></td>
<td>0.65</td>
<td>V</td>
</tr>
<tr>
<td><strong>Gate Driver Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-side gate pull-up peak current(^{(5)})</td>
<td>I_{BGU}</td>
<td>V_{BG}=0V</td>
<td>350</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Low-side gate pull-down peak current(^{(5)})</td>
<td>I_{BGD}</td>
<td>V_{BG}=12V</td>
<td>1</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>High-side gate pull-up peak current(^{(6)})</td>
<td>I_{TGU}</td>
<td>V_{TG}=0V</td>
<td>350</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>High-side gate pull-down peak current(^{(6)})</td>
<td>I_{TGD}</td>
<td>V_{TG}=12V</td>
<td>1</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td><strong>Propagation Delays, Dead Times and Output Rising and Falling Times (C_{Load}=1nF cap) (please see timing diagram)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-on propagation delay (TG)</td>
<td>τ\textsubscript{ON} \textsubscript{TG}</td>
<td>V_{SW}=0V</td>
<td>80</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-off propagation delay (TG)</td>
<td>τ\textsubscript{OFF} \textsubscript{TG}</td>
<td>V_{SW}=0V</td>
<td>80</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-on rise time (TG)</td>
<td>τ\textsubscript{RISE} \textsubscript{TG}</td>
<td></td>
<td>50</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-off fall time (TG)</td>
<td>τ\textsubscript{FALL} \textsubscript{TG}</td>
<td></td>
<td>30</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-on propagation delay (BG)</td>
<td>τ\textsubscript{ON} \textsubscript{BG}</td>
<td></td>
<td>80</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-off propagation delay (BG)</td>
<td>τ\textsubscript{OFF} \textsubscript{BG}</td>
<td></td>
<td>80</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-on rise time (BG)</td>
<td>τ\textsubscript{RISE} \textsubscript{BG}</td>
<td></td>
<td>50</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-off fall time (BG)</td>
<td>τ\textsubscript{FALL} \textsubscript{BG}</td>
<td></td>
<td>30</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Deadtime, LS turn-off to HS turn-on &amp; HS turn-on to LS turn-off</td>
<td>τ\textsubscript{DT}</td>
<td></td>
<td>150</td>
<td>250</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{CC} = 12V, V_{SW}=0V, \text{ no load on TG or BG, } T_A = 25^\circ C, \text{ unless otherwise noted.}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPWM source current</td>
<td>$I_{LPWM}$</td>
<td>$I_{LPWM}=5V$</td>
<td>-8</td>
<td>-3</td>
<td>-1</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>HPWM sink current</td>
<td>$I_{HPWM}$</td>
<td>$I_{HPWM}=5V$</td>
<td>1</td>
<td>3</td>
<td>8</td>
<td>$\mu A$</td>
</tr>
</tbody>
</table>

Floating Gate Driver

- BG-output-low to GND  
  $V_{BGL} \quad I_{BG}=100mA \quad 0.4 \quad 0.7 \quad V$
- BG-output-high to rail  
  $V_{BGH} \quad I_{BG}=-100mA, V_{BGH}=V_{CC}-V_{BG} \quad 1.5 \quad 1.7 \quad V$
- TG-output-low to SW  
  $V_{TGL} \quad I_{TG}=100mA \quad 0.4 \quad 0.7 \quad V$
- TG-output-high to rail  
  $V_{TGH} \quad I_{TG}=-100mA, V_{TGH}=V_{CC}-V_{TG} \quad 1.5 \quad 1.7 \quad V$

Switching Specifications

- Minimum input pulse width to change the output\(^5\)  
  $\tau_{PWM_{min}} \quad 50 \quad ns$

Notes:

5) Guaranteed by design

![Gate Driver Timing Diagram](image)

Figure 1: Gate Driver Timing Diagram
TYPICAL CHARACTERISTICS

$V_{DD}=12\,\text{V}$, $V_{SW}=0\,\text{V}$, $T_A=+25\,\text{°C}$, unless otherwise noted.

### High Level Output Voltage vs. Temperature

- $V_{TGH}$
- $V_{BGH}$

### Low Level Output Voltage vs. Temperature

- $V_{TGL}$
- $V_{BGL}$

### Undervoltage Lockout Threshold vs. Temperature (Rising)

- $V_{CCTHR}$
- $V_{BTTHR}$

### Undervoltage Lockout Hysteresis vs. Temperature (Falling)

- $V_{CCTHF}$
- $V_{BTTHF}$

### Propagation Delay vs. Temperature

- $T_{ON\_TG}$
- $T_{OFF\_TG}$
- $T_{ON\_BG}$
- $T_{OFF\_BG}$

### Quiescent Current vs. Temperature

- $I_{CCQ}$
- $I_{BTQ}$
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 12V, V_{SW}=0V, 1\text{nF load on TG and BG, } T_A = 25^\circ\text{C, unless otherwise noted.}$

### Turn-on Propagation Delay

![Turn-on Propagation Delay](image)

### Turn-off Propagation Delay

![Turn-off Propagation Delay](image)

### Drive Rise Time (1\text{nF Load})

![Drive Rise Time (1\text{nF Load})](image)

### Drive Fall Time (1\text{nF Load})

![Drive Fall Time (1\text{nF Load})](image)

### Input Signal Overlap Protection

![Input Signal Overlap Protection](image)
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>Supply Input. Supplies power to all internal circuitry. Requires a decoupling capacitor to ground placed close to this pin to ensure a stable and clean supply.</td>
</tr>
<tr>
<td>2</td>
<td>HPWM</td>
<td>Logic input for high-side gate driver output.</td>
</tr>
<tr>
<td>3</td>
<td>LPWM</td>
<td>Logic input for low-side gate driver output. Active low.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground.</td>
</tr>
<tr>
<td>5</td>
<td>BG</td>
<td>Gate Driver Output for low-side MOSFET.</td>
</tr>
<tr>
<td>6</td>
<td>SW</td>
<td>Source Return for high-side MOSFET.</td>
</tr>
<tr>
<td>7</td>
<td>TG</td>
<td>Gate Driver Output for high-side MOSFET.</td>
</tr>
<tr>
<td>8</td>
<td>BT</td>
<td>Bootstrap. Internal power supply pin for high-side floating driver. Add a 1µF ceramic bootstrap capacitor from BT to SW pin.</td>
</tr>
</tbody>
</table>
Figure 2: Functional Block Diagram
OPERATION

Switch Shoot-through Protection
The input signals of HPWM and LPWM are independently controlled. Input shoot-through protection circuitry prevents shoot-through between the TG and BG outputs. Only one of the FET drivers can be on at one time. If HPWM is high and LPWM is low, both TG and BG are OFF.

Under Voltage Lockout
When $V_{CC}$ or $V_{BT}$ goes below their respective UVLO threshold, both BG and TG outputs will go low to both FETS. Once $V_{CC}$ and $V_{BT}$ rises above the UVLO threshold, both TG and BG will stay low until there is a rising edge on either HPWM or LPWM.

Figure 3 shows the operation of the TG and BG under different HPWM and LPWM and UVLO conditions.

![Figure 3: Input/Output Timing Diagram](image-url)
APPLICATION INFORMATION

Reference Design Circuits
Half Bridge Motor Driver

In a half-bridge converter topology, the MOSFET-driving signals have a dead time: HPWM and LPWM driven with alternating signals from the PWM controller. The input voltage can be up to 80V in this application.

![Figure 4: Half-Bridge Motor Driver](image)

Active-Clamp-Forward Converter

An active-clamp-forward-converter topology alternately drives the MOSFETs. The high-side MOSFET and the capacitor, $C_{\text{RESET}}$, reset the power transformer in a lossless manner. This topology runs well at duty cycles exceeding 50%. However, the input voltage may not run at 80V.

![Figure 5: Active-Clamp Forward Converter](image)
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NOTE:
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.