



# MP18811

## Isolated Single-Channel Gate Driver with Split Outputs

### DESCRIPTION

The MP18811 is an isolated, single-channel gate driver solution with up to 4A of source and sink peak current capability. The gate driver is designed to drive power switching devices with a short propagation delay and minimal pulse-width distortion. By utilizing MPS's proprietary capacitive-based isolation technology, the driver can provide up to 3kV<sub>RMS</sub> withstand voltage (per UL 1577). It can also provide a common-mode transient immunity (CMTI) rating above 100kV/μs between the input side and output driver. These advanced features enable high efficiency, high power density, and robustness in a wide variety of power applications.

The MP18811 provides primary on/off control and split outputs that can control source and sink driving capability individually. A wide primary-side VDDI supply voltage (V<sub>DDI</sub>) range makes the driver suitable to be interfaced with 3.3V and 5V digital controllers. The secondary-side driver can accept up to a 30V supply. All of the supply voltage pins feature multiple under-voltage lockout (UVLO) protection options.

The MP18811 is available in an SOIC-8 NB (narrow-body) package.

### FEATURES

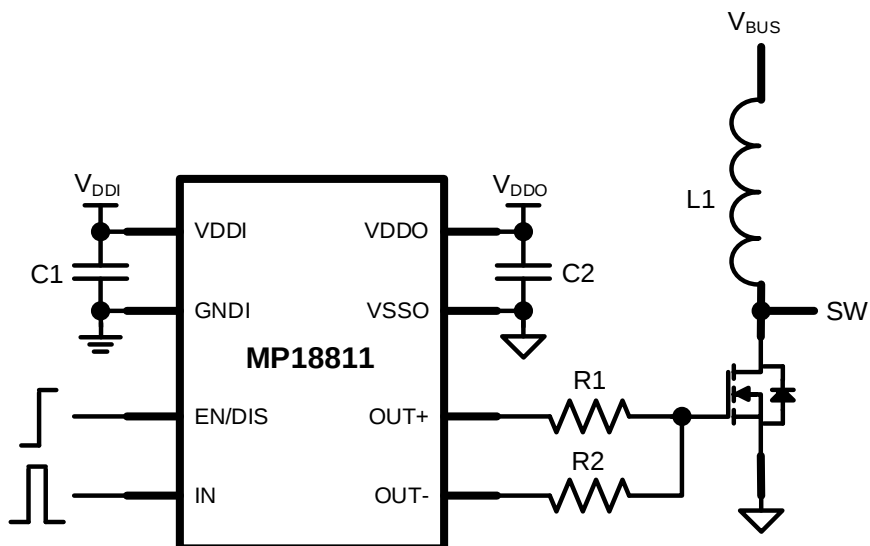
- Single-Channel Gate Driver
- Up to 3kV<sub>RMS</sub> Input to Output Isolation
- Common-Mode Transient Immunity (CMTI) >100kV/μs
- 2.8V to 5.5V Input VDDI Voltage (V<sub>DDI</sub>) Range to Interface with TTL and CMOS-Compatible Inputs
- Up to 30V Output Drive Supply with Several Under-Voltage Lockout (UVLO) Options
- 4A Source, 4A Sink Peak Current Output
- Primary On/Off Control
- Split Source and Sink Outputs
- 50ns Typical Propagation Delay
- -40°C to +125°C Operating Temperature Range
- UL 1577 Certified:
  - SOIC-8 NB: 3kV<sub>RMS</sub> Isolation for 60s
- DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 Certified
- TUV SUD Certification per IEC/EN/UL/CSA 62368-1, 60950-1, 61010-1
- CQC Certification per GB4943.1-2022

### APPLICATIONS

- Half/Full-Bridge Converters
- Isolated DC/DC Converters
- Offline Isolated AC/DC Converters
- DC/AC Inverters

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## TYPICAL APPLICATION



## SELECTION GUIDE

| Part Number | Peak Output Current (A) | Output UVLO (V) | On/Off Logic | Input Logic | Configuration | Package Type |
|-------------|-------------------------|-----------------|--------------|-------------|---------------|--------------|
| MP18811-4A  | 4                       | 3               | EN           | IN          | Single        | SOIC-8 NB    |
| MP18811-4B  |                         | 5               |              |             |               |              |
| MP18811-4C  |                         | 8               |              |             |               |              |
| MP18811-4D  |                         | 10              |              |             |               |              |
| MP18811-4E  |                         | 12              |              |             |               |              |
| MP18811-A4A | 4                       | 3               | DIS          | IN          | Single        | SOIC-8 NB    |
| MP18811-A4B |                         | 5               |              |             |               |              |
| MP18811-A4C |                         | 8               |              |             |               |              |
| MP18811-A4D |                         | 10              |              |             |               |              |
| MP18811-A4E |                         | 12              |              |             |               |              |

## ORDERING INFORMATION <sup>(1)</sup>

| Part Number*  | Package   | Top Marking      | MSL Rating |
|---------------|-----------|------------------|------------|
| MP18811-4AGS  | SOIC-8 NB | <i>See Below</i> | 2          |
| MP18811-4BGS  |           |                  |            |
| MP18811-4CGS  |           |                  |            |
| MP18811-4DGS  |           |                  |            |
| MP18811-4EGS  |           |                  |            |
| MP18811-A4AGS | SOIC-8 NB |                  |            |
| MP18811-A4BGS |           |                  |            |
| MP18811-A4CGS |           |                  |            |
| MP18811-A4DGS |           |                  |            |
| MP18811-A4EGS |           |                  |            |

\* For Tape & Reel, add suffix -Z (e.g. MP18811-4AGS-Z).

### Note:

1) Contact MPS sales or our distributors to check the latest availability status for the ordering part numbers.

## TOP MARKING (MP18811-4x)

**18811-4X**

**LLLLLLLL**

**MPSYWW**

18811-4X: Part number

X: UVLO level code, where X = A, B, C, D, or E

LLLLLLLL: Lot number

MPS: MPS prefix

Y: Year code

WW: Week code

## TOP MARKING (MP18811-A4x)

**18811A4X**

**LLLLLLLL**

**MPSYWW**

18811A4X: Part number

X: UVLO level code, where X = A, B, C, D, or E

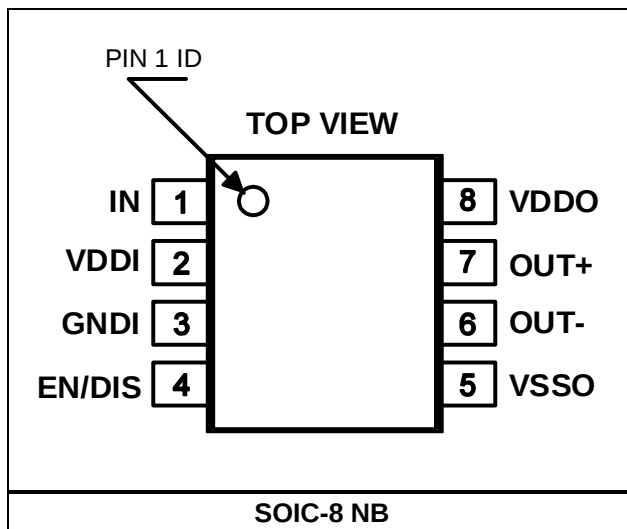
LLLLLLLL: Lot number

MPS: MPS prefix

Y: Year code

WW: Week code

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | IN     | <b>Non-inverting logic control signal input.</b> The IN pin can accept a TTL/CMOS level compatible input logic. This pin is pulled down internally to GNDI. A logic high signal on IN forces OUT+ to go high and OUT- into a high-impedance (Hi-Z) state. A logic low signal on IN or leaving the pin open forces OUT- low and OUT+ into a Hi-Z state.                                                                                                                                                                                                          |
| 2     | VDDI   | <b>Input-side power supply input.</b> The VDDI pin supplies power to the primary-side control circuitry. This pin is locally decoupled to GNDI using a low-ESR/ESL bypass capacitor. Place the capacitor as close to the chip as possible.                                                                                                                                                                                                                                                                                                                      |
| 3     | GNDI   | <b>Input-side ground.</b> Reference ground for all input-side signal and internal control blocks.                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 4     | EN/DIS | <b>Enable/disable control input.</b> The EN/DIS pin can be driven by an external TTL/CMOS level compatible input logic signal to enable/disable the chip. EN/DIS can be configured for the EN or DIS function.<br><u>EN:</u> The EN pin is pulled high internally. Pull EN high or leave it open to enable the chip; pull EN low to shut down the driver output and disable the chip.<br><u>DIS:</u> The DIS pin is pulled low internally. Pull DIS low or leave it open to enable the chip; pull DIS high to shut down the driver output and disable the chip. |
| 5     | VSSO   | <b>Output-side ground.</b> Reference ground for the output driver.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 6     | OUT-   | <b>Gate drive pull-down output.</b> Connect the OUT- pin to the gate of the power device. When IN asserts a logic low signal or the pin is left open, OUT- pulls down the gate of the power device to switch it off. Pulling IN high forces OUT- into a Hi-Z state.                                                                                                                                                                                                                                                                                             |
| 7     | OUT+   | <b>Gate drive pull-up output.</b> Connect the OUT+ pin to the gate of the power device. When IN asserts a logic high signal, OUT+ drives the power device to switch it on. Pull IN low or leave the pin open to force OUT+ into a Hi-Z state.                                                                                                                                                                                                                                                                                                                   |
| 8     | VDDO   | <b>Output-side driver power supply input.</b> The VDDO pin supplies power to the secondary-side driver circuitry. It is locally decoupled to VSSO using a low-ESR/ESL bypass capacitor. Place the capacitor as close to the chip as possible.                                                                                                                                                                                                                                                                                                                   |

**ABSOLUTE MAXIMUM RATINGS** <sup>(2)</sup>

|                                                                    |                                                     |
|--------------------------------------------------------------------|-----------------------------------------------------|
| $V_{DDI} - V_{GNDI}$ .....                                         | -0.3V to +6.5V                                      |
| $V_{IN}, V_{EN/DIS}$ .....                                         | ..... ( $V_{GNDI} - 0.3V$ ) to ( $V_{DDI} + 0.3V$ ) |
| $V_{IN}, V_{EN/DIS}$ transient for 50ns .....                      | ..... ( $V_{GNDI} - 5V$ ) to ( $V_{DDI} + 0.3V$ )   |
| $V_{DDO} - V_{SSO}$ .....                                          | -0.3V to +35V                                       |
| $V_{OUT+}, V_{OUT-}$ .....                                         | ( $V_{SSO} - 0.3V$ ) to ( $V_{DDO} + 0.3V$ )        |
| $V_{OUT+}, V_{OUT-}$ transient for 200ns .....                     | ..... ( $V_{SSO} - 2V$ ) to ( $V_{DDO} + 0.3V$ )    |
| Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(3)</sup> |                                                     |
| SOIC-8 NB .....                                                    | 1130mW                                              |
| Junction temperature .....                                         | 150°C                                               |
| Lead temperature .....                                             | 260°C                                               |
| Storage temperature .....                                          | -65°C to +150°C                                     |

**ESD Ratings**

|                                  |       |
|----------------------------------|-------|
| Human body model (HBM) .....     | 4000V |
| Charged-device model (CDM) ..... | 2000V |

**Recommended Operating Conditions** <sup>(4)</sup>

|                                        |                                |
|----------------------------------------|--------------------------------|
| $V_{DDI} - V_{GNDI}$ .....             | 2.8V to 5.5V                   |
| $V_{IN}, V_{EN/DIS}$ .....             | $V_{GNDI}$ to $V_{DDI}$        |
| $V_{DDO} - V_{SSO}$ .....              |                                |
| .....                                  | 4.2V to 30V (3V UVLO option)   |
| .....                                  | 6.5V to 30V (5V UVLO option)   |
| .....                                  | 9.2V to 30V (8V UVLO option)   |
| .....                                  | 12V to 30V (10V UVLO option)   |
| .....                                  | 14.5V to 30V (12V UVLO option) |
| Operating junction temp ( $T_J$ ) .... | -40°C to +125°C                |

| <b>Thermal Resistance</b> <sup>(5)</sup> | $\theta_{JA}$ | $\theta_{JC}$ |
|------------------------------------------|---------------|---------------|
| SOIC-8 NB .....                          | 110 .....     | 45... °C/W    |

**Notes:**

- 2) Exceeding these ratings may damage the device.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on the MP18811 evaluation board, a 2-layer PCB.

## ELECTRICAL CHARACTERISTICS

$2.8V \leq V_{DDI} - V_{GNDI} \leq 5.5V$ ,  $V_{DDO} - V_{SSO} = 5V/12V/15V$  <sup>(6)</sup>,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , all voltages with respect to the corresponding ground(s), unless otherwise noted.

| Parameters                                                                             | Symbol                    | Condition                                                                                                                           | Min                     | Typ                     | Max                     | Units |
|----------------------------------------------------------------------------------------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-------------------------|-------------------------|-------|
| Input-Side Supply Voltage                                                              |                           |                                                                                                                                     |                         |                         |                         |       |
| V <sub>DDI</sub> under-voltage lockout (UVLO) threshold                                | V <sub>DDI_UVLO</sub>     | (V <sub>DDI</sub> - V <sub>GNDI</sub> ) falling                                                                                     | 2.42                    | 2.6                     | 2.78                    | V     |
| V <sub>DDI</sub> UVLO hysteresis                                                       | V <sub>DDI_UVLO_HYS</sub> |                                                                                                                                     | 100                     | 120                     | 140                     | mV    |
| Input-Side Supply Current                                                              |                           |                                                                                                                                     |                         |                         |                         |       |
| VDDI shutdown current                                                                  | I <sub>VDDI_SD</sub>      | V <sub>EN</sub> = V <sub>GNDI</sub> or V <sub>DIS</sub> = V <sub>DDI</sub>                                                          |                         | 1                       | 1.3                     | mA    |
| VDDI quiescent current                                                                 | I <sub>VDDI_Q</sub>       | V <sub>EN</sub> = V <sub>DDI</sub> or V <sub>DIS</sub> = V <sub>GNDI</sub> ,<br>V <sub>IN</sub> = V <sub>GNDI</sub>                 |                         | 1                       | 1.3                     | mA    |
| VDDI operating current                                                                 | I <sub>VDDI</sub>         | f <sub>SW</sub> = 500kHz, 50% duty,<br>C <sub>LOAD</sub> = 100pF                                                                    |                         | 1.3                     | 2                       | mA    |
| Logic Input (IN, EN/DIS)                                                               |                           |                                                                                                                                     |                         |                         |                         |       |
| Logic input high threshold                                                             | V <sub>LI_H</sub>         | (V <sub>LI</sub> - V <sub>GNDI</sub> ) rising                                                                                       |                         | 1.6                     | 1.8                     | V     |
| Logic input low threshold                                                              | V <sub>LI_L</sub>         | (V <sub>LI</sub> - V <sub>GNDI</sub> ) falling                                                                                      | 1                       | 1.2                     |                         | V     |
| Logic input hysteresis voltage                                                         | V <sub>LI_HYS</sub>       |                                                                                                                                     | 360                     | 400                     | 440                     | mV    |
| Internal pull-up resistance                                                            | R <sub>LI_PU</sub>        | EN                                                                                                                                  |                         | 200                     |                         | kΩ    |
| Internal pull-down resistance                                                          | R <sub>LI_PD</sub>        | IN, DIS                                                                                                                             |                         | 200                     |                         | kΩ    |
| Output-Side Supply Voltage                                                             |                           |                                                                                                                                     |                         |                         |                         |       |
| V <sub>DDO</sub> UVLO threshold when (V <sub>DDO</sub> - V <sub>SSO</sub> ) is falling | V <sub>DDO_UVLO</sub>     | -A, 3V threshold                                                                                                                    | 2.7                     | 3.2                     | 3.7                     | V     |
|                                                                                        |                           | -B, 5V threshold                                                                                                                    | 5                       | 5.5                     | 6                       | V     |
|                                                                                        |                           | -C, 8V threshold                                                                                                                    | 7.5                     | 8                       | 8.5                     | V     |
|                                                                                        |                           | -D, 10V threshold                                                                                                                   | 9.3                     | 10                      | 10.7                    | V     |
|                                                                                        |                           | -E, 12V threshold                                                                                                                   | 11                      | 12                      | 13                      | V     |
| VDDO UVLO hysteresis                                                                   | V <sub>DDO_UVLO_HYS</sub> | -A/-B, 3V/5V threshold                                                                                                              | 200                     | 300                     | 400                     | mV    |
|                                                                                        |                           | -C, 8V threshold                                                                                                                    | 420                     | 520                     | 620                     | mV    |
|                                                                                        |                           | -D/-E, 10V/12V threshold                                                                                                            | 0.8                     | 1                       | 1.2                     | V     |
| Output-Side Supply Current                                                             |                           |                                                                                                                                     |                         |                         |                         |       |
| VDDO shutdown current                                                                  | I <sub>VDDO_SD</sub>      | V <sub>EN</sub> = V <sub>GNDI</sub> or V <sub>DIS</sub> = V <sub>DDI</sub>                                                          |                         | 1                       | 1.3                     | mA    |
| VDDO quiescent current                                                                 | I <sub>VDDO_Q</sub>       | V <sub>EN</sub> = V <sub>DDI</sub> or V <sub>DIS</sub> = V <sub>GNDI</sub> ,<br>V <sub>IN</sub> = V <sub>GNDI</sub>                 |                         | 1                       | 1.3                     | mA    |
| VDDO operating current                                                                 | I <sub>VDDO</sub>         | f <sub>SW</sub> = 500kHz, C <sub>LOAD</sub> = 100pF,<br>V <sub>DDO</sub> - V <sub>SSO</sub> = 12V                                   |                         | 2.5                     | 3                       | mA    |
|                                                                                        |                           | f <sub>SW</sub> = 500kHz, C <sub>LOAD</sub> = 100pF,<br>V <sub>DDO</sub> - V <sub>SSO</sub> = 15V                                   |                         | 3                       | 4.6                     | mA    |
| Gate Driver                                                                            |                           |                                                                                                                                     |                         |                         |                         |       |
| Logic high output voltage                                                              | V <sub>OUT+_H</sub>       | I <sub>OUT+</sub> = -10mA                                                                                                           | V <sub>DDO</sub> - 0.03 | V <sub>DDO</sub> - 0.01 |                         | V     |
| Logic low output voltage                                                               | V <sub>OUT-_L</sub>       | I <sub>OUT-</sub> = 10mA                                                                                                            |                         | V <sub>SSO</sub> + 0.01 | V <sub>SSO</sub> + 0.03 | V     |
| Peak output source current <sup>(7)</sup>                                              | I <sub>OUT+_SRC</sub>     | V <sub>DDO</sub> - V <sub>SSO</sub> = 15V,<br>V <sub>OUT+</sub> - V <sub>SSO</sub> = 5V (5V Miller plateau), f <sub>SW</sub> = 1kHz |                         | -4                      |                         | A     |

## ELECTRICAL CHARACTERISTICS (continued)

$2.8V \leq V_{DDI} - V_{GNDI} \leq 5.5V$ ,  $V_{DDO} - V_{SSO} = 5V/12V/15V$  <sup>(6)</sup>,  $T_J = -40^\circ C$  to  $+125^\circ C$ , typical value is tested at  $T_J = 25^\circ C$ , all voltages with respect to the corresponding ground(s), unless otherwise noted.

| Parameters                                                                                    | Symbol          | Condition                                                                                                                                      | Min | Typ | Max | Units       |
|-----------------------------------------------------------------------------------------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-------------|
| Peak output sink current <sup>(7)</sup>                                                       | $I_{OUT\_SNK}$  | $V_{DDO} - V_{SSO} = 15V$ ,<br>$V_{OUT-} - V_{SSO} = 5V$ (5V Miller plateau), $f_{SW} = 1kHz$                                                  |     | 4   |     | A           |
| Output source resistance                                                                      | $R_{OUT+}$      | $I_{OUT+} = -10mA$                                                                                                                             |     | 1.3 | 2.5 | $\Omega$    |
| Output sink resistance                                                                        | $R_{OUT-}$      | $I_{OUT-} = 10mA$                                                                                                                              |     | 1   | 2   | $\Omega$    |
| <b>Switching</b> <sup>(8)</sup>                                                               |                 |                                                                                                                                                |     |     |     |             |
| Output rise time                                                                              | $t_R$           | $(V_{OUT+} - V_{SSO})$ rising,<br>$C_{LOAD} = 1.8nF$                                                                                           |     | 10  | 20  | ns          |
| Output fall time                                                                              | $t_F$           | $(V_{OUT-} - V_{SSO})$ falling<br>$C_{LOAD} = 1.8nF$                                                                                           |     | 10  | 20  | ns          |
| Minimum pulse width                                                                           | $t_{PW\_MIN}$   | Output pulse off if shorter than $t_{PW\_MIN}$ , $C_{LOAD} = 0pF$                                                                              |     | 23  | 35  | ns          |
| Propagation delay from IN high to the output rising edge                                      | $t_{PDLH}$      | $V_{EN} = V_{DDI}$ or $V_{DIS} = V_{GNDI}$ ,<br>$C_{LOAD} = 0pF$                                                                               | 35  | 50  | 65  | ns          |
| Propagation delay from IN low to the output falling edge                                      | $t_{PDHL}$      | $V_{EN} = V_{DDI}$ or $V_{DIS} = V_{GNDI}$ ,<br>$C_{LOAD} = 0pF$                                                                               | 35  | 50  | 65  | ns          |
| Propagation delay from enable true to the output rising edge                                  | $t_{PDEN}$      | $V_{IN} = V_{DDI}$ , $C_{LOAD} = 0pF$                                                                                                          | 35  | 50  | 65  | ns          |
| Propagation delay from disable true to the output falling edge                                | $t_{PDDIS}$     | $V_{IN} = V_{DDI}$ , $C_{LOAD} = 0pF$                                                                                                          | 35  | 50  | 65  | ns          |
| Pulse-width distortion $ t_{PDLH} - t_{PDHL} $                                                | $t_{PWD}$       | $C_{LOAD} = 0pF$                                                                                                                               |     | 1   | 6   | ns          |
| Start-up delay from the input supply exiting UVLO to the output rising edge                   | $t_{STU\_VDDI}$ | $V_{EN} = V_{DDI}$ or $V_{DIS} = V_{GNDI}$ ,<br>$V_{IN} = V_{DDI}$ , $C_{LOAD} = 0pF$                                                          | 15  | 25  | 35  | $\mu s$     |
| Shutdown delay from the input supply entering UVLO to the output falling edge <sup>(7)</sup>  | $t_{SHD\_VDDI}$ | $V_{EN} = V_{DDI}$ or $V_{DIS} = V_{GNDI}$ ,<br>$V_{IN} = V_{DDI}$ , $C_{LOAD} = 0pF$                                                          |     | 500 |     | ns          |
| Start-up delay from the output supply exiting UVLO to the output rising edge                  | $t_{STU\_VDDO}$ | $V_{EN} = V_{DDI}$ or $V_{DIS} = V_{GNDI}$ ,<br>$V_{IN} = V_{DDI}$ , $C_{LOAD} = 0pF$                                                          | 10  | 20  | 30  | $\mu s$     |
| Shutdown delay from the output supply entering UVLO to the output falling edge <sup>(7)</sup> | $t_{SHD\_VDDO}$ | $V_{EN} = V_{DDI}$ or $V_{DIS} = V_{GNDI}$ ,<br>$V_{IN} = V_{DDI}$ , $C_{LOAD} = 0pF$                                                          |     | 500 |     | ns          |
| Static common-mode transient immunity (CMTI) <sup>(7)</sup>                                   | $CMTI_{STC}$    | $V_{EN} = V_{DDI}$ or $V_{DIS} = V_{GNDI}$ ,<br>$V_{IN} = V_{GNDI}$ or $V_{DDI}$ , slew rate of $V_{GNDI}$ vs. $V_{SSO}$ ,<br>$V_{CM} = 1500V$ | 100 |     |     | kV/ $\mu s$ |
| Dynamic CMTI <sup>(7)</sup>                                                                   | $CMTI_{DYN}$    | $V_{EN} = V_{DDI}$ or $V_{DIS} = V_{GNDI}$ ,<br>$f_{SW} = 100kHz$ pulse at IN, slew rate of $V_{GNDI}$ vs. $V_{SSO}$ ,<br>$V_{CM} = 1500V$     | 100 |     |     | kV/ $\mu s$ |

### Notes:

- For the test conditions,  $V_{DDO} - V_{SSO} = 5V$  is used for 3V UVLO devices;  $V_{DDO} - V_{SSO} = 12V$  is used for 5V and 8V UVLO devices; and  $V_{DDO} - V_{SSO} = 15V$  is used for 10V and 12V UVLO devices.
- Guaranteed by characterization. Not tested in production.
- For more details, see Figure 1, Figure 2, and Figure 3 on page 16, as well as Figure 4 on page 17.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

| Parameters                                                                                                                                                  | Symbol             | Condition                                                                                                                                                                                                                 | SOIC-8 NB         | Units            |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------------------|
| External air gap (clearance) <sup>(9)</sup>                                                                                                                 | CLR                | Shortest pin-to-pin distance through the air between the primary and secondary sides                                                                                                                                      | >4                | mm               |
| External tracking (creepage) <sup>(9)</sup>                                                                                                                 | CPG                | Shortest pin-to-pin distance across the package surface between the primary and secondary sides                                                                                                                           | >4                | mm               |
| Distance through insulation                                                                                                                                 | DTI                | Internal clearance                                                                                                                                                                                                        | >20               | μm               |
| Comparative tracking index                                                                                                                                  | CTI                | According to IEC60112                                                                                                                                                                                                     | >600              | V                |
| Material group                                                                                                                                              |                    | According to IEC 60664-1                                                                                                                                                                                                  | I                 |                  |
| Overvoltage category per IEC 60664-1                                                                                                                        |                    | Rated mains voltages ≤ 150V <sub>RMS</sub>                                                                                                                                                                                | I-IV              |                  |
|                                                                                                                                                             |                    | Rated mains voltages ≤ 300V <sub>RMS</sub>                                                                                                                                                                                | I-III             |                  |
|                                                                                                                                                             |                    | Rated mains voltages ≤ 600V <sub>RMS</sub>                                                                                                                                                                                | I-II              |                  |
| UL 1577, 5th Edition                                                                                                                                        |                    |                                                                                                                                                                                                                           |                   |                  |
| Recognized under UL 1577 Component Recognition Program, Single Protection. File number: E322138                                                             |                    |                                                                                                                                                                                                                           |                   |                  |
| Dielectric withstand insulation voltage                                                                                                                     | V <sub>ISO</sub>   | V <sub>TEST</sub> = V <sub>ISO</sub> for t = 60s (qualification),<br>V <sub>TEST</sub> = 1.2 x V <sub>ISO</sub> for t = 1s (100% production)                                                                              | 3000              | V <sub>RMS</sub> |
| DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 <sup>(10)</sup>                                                                                                  |                    |                                                                                                                                                                                                                           |                   |                  |
| Certified according to DIN EN IEC 60747-17 (VDE 0884-17): 2021-10; EN IEC 60747-17:2020+AC: 2021.<br>Certification number: 40055265                         |                    |                                                                                                                                                                                                                           |                   |                  |
| Maximum repetitive peak isolation voltage                                                                                                                   | V <sub>IORM</sub>  | AC voltage (bipolar)                                                                                                                                                                                                      | 630               | V <sub>PK</sub>  |
| Maximum working isolation voltage                                                                                                                           | V <sub>IOWM</sub>  | AC voltage (sine wave), time dependent dielectric breakdown (TDDb) test method                                                                                                                                            | 450               | V <sub>RMS</sub> |
|                                                                                                                                                             |                    | DC voltage                                                                                                                                                                                                                | 630               | V <sub>DC</sub>  |
| Maximum transient isolation voltage                                                                                                                         | V <sub>IOTM</sub>  | V <sub>TEST</sub> = V <sub>IOTM</sub> for t = 60s (qualification),<br>V <sub>TEST</sub> = 1.2 x V <sub>IOTM</sub> for t = 1s (100% production)                                                                            | 4242              | V <sub>PK</sub>  |
| Apparent charge <sup>(11)</sup> measuring voltage                                                                                                           | V <sub>PD(M)</sub> | Method b1, at routine test (100% production),<br>V <sub>PD(INI)</sub> = 1.2 x V <sub>IOTM</sub> , t <sub>INI</sub> = 1s, V <sub>PD(M)</sub> = 1.875 x V <sub>IORM</sub> ,<br>t <sub>M</sub> = 1s, partial discharge < 5pC | 1181              | V <sub>PK</sub>  |
| Maximum surge isolation voltage <sup>(12)</sup>                                                                                                             | V <sub>IOSM</sub>  | Tested per IEC 62368-1 with 1.2/50μs pulse,<br>V <sub>TEST</sub> = 1.3 x V <sub>IOSM</sub> (qualification)                                                                                                                | 4000              | V <sub>PK</sub>  |
| Barrier capacitance <sup>(13)</sup>                                                                                                                         | C <sub>IO</sub>    | f <sub>SW</sub> = 1MHz                                                                                                                                                                                                    | ~1                | pF               |
| Insulation resistance <sup>(13)</sup>                                                                                                                       | R <sub>IO</sub>    | V <sub>IO</sub> = 500V, T <sub>A</sub> = 25°C                                                                                                                                                                             | >10 <sup>12</sup> | Ω                |
|                                                                                                                                                             |                    | V <sub>IO</sub> = 500V, 100°C ≤ T <sub>A</sub> ≤ 125°C                                                                                                                                                                    | >10 <sup>11</sup> | Ω                |
|                                                                                                                                                             |                    | V <sub>IO</sub> = 500V, T <sub>A</sub> = T <sub>S</sub> = 150°C                                                                                                                                                           | >10 <sup>9</sup>  | Ω                |
| Pollution degree                                                                                                                                            |                    | Per DIN VDE 0110 Table 1                                                                                                                                                                                                  | 2                 |                  |
| Climatic category                                                                                                                                           |                    |                                                                                                                                                                                                                           | 40/125/21         |                  |
| IEC/EN/UL/CSA 62368-1, 60950-1, 61010-1                                                                                                                     |                    |                                                                                                                                                                                                                           |                   |                  |
| TUV SUD certification conformity.<br>Certificate number: SG PSB-IV-07941, SG PSB-OF-07050, SG PSB-MS-00361, U10 113824 0011 Rev. 00, B 113824 0010 Rev. 00. |                    |                                                                                                                                                                                                                           |                   |                  |
| Basic insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 660V <sub>P</sub> /630V <sub>RMS</sub> maximum working voltage                       |                    |                                                                                                                                                                                                                           |                   |                  |

## INSULATION AND SAFETY-RELATED SPECIFICATIONS *(continued)*

|                                                                                                                                                                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>GB 4943.1-2022</b>                                                                                                                                                     |
| Certified according to CQC GB 4943.1-2022.<br>File number: CQC23001376765.                                                                                                |
| Basic insulation, altitude $\leq 5000\text{m}$ , $125^{\circ}\text{C}$ thermal cycling test passed, $660\text{V}_\text{P}/630\text{V}_\text{RMS}$ maximum working voltage |

### Notes:

- 9) See the Package Information on page 26 for detailed dimensions. As an isolated solution, the recommended land pattern is helpful to ensure adequate safety creepage and clearance distances on a PCB.
- 10) This coupler is suitable for “basic electrical insulation” only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- 11) Electrical discharge caused by a partial discharge in the coupler.
- 12) The surge test is carried out in oil.
- 13) The barrier’s primary-side and secondary-side terminals are connected, forming a two-terminal device.  $C_{\text{IO}}$  and  $R_{\text{IO}}$  are measured between the two terminals of the coupler.

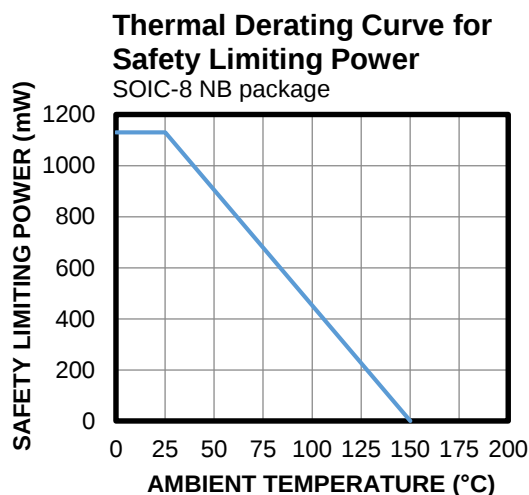
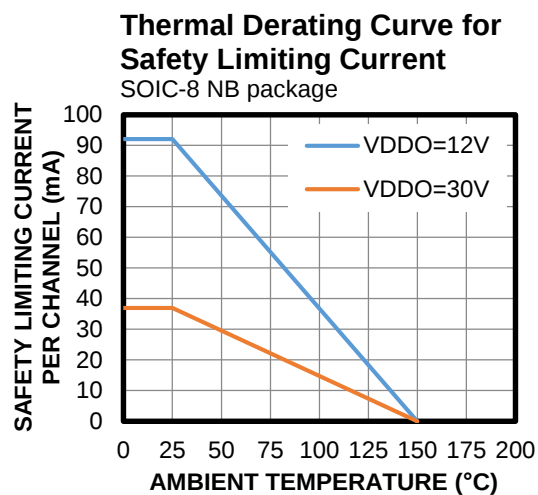
## SAFETY LIMITING VALUES <sup>(14)</sup>

| Parameters                                 | Symbol     | Condition                                                                                                        | SOIC-8 NB | Units              |
|--------------------------------------------|------------|------------------------------------------------------------------------------------------------------------------|-----------|--------------------|
| Maximum safety temperature <sup>(15)</sup> | $T_S$      |                                                                                                                  | 150       | $^{\circ}\text{C}$ |
| Maximum output safety current              | $I_{S\_O}$ | $V_{\text{DDO}} - V_{\text{SSO}} = 12\text{V}^{(16)}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$ | 92        | mA                 |
|                                            |            | $V_{\text{DDO}} - V_{\text{SSO}} = 30\text{V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$        | 37        | mA                 |
| Safety power dissipation <sup>(17)</sup>   | $P_S$      | Input side                                                                                                       | 15        | mW                 |
|                                            |            | Output side                                                                                                      | 1115      | mW                 |
|                                            |            | Total                                                                                                            | 1130      | mW                 |

### Notes:

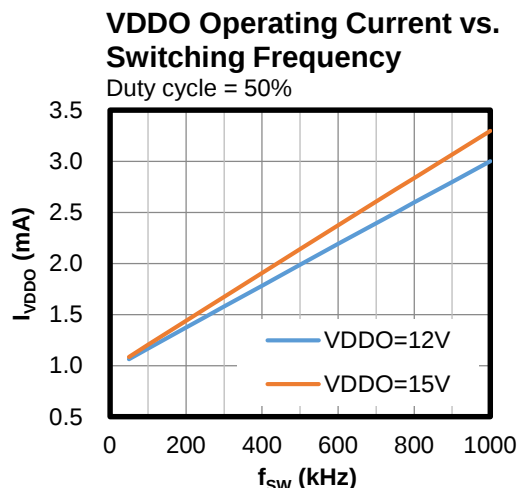
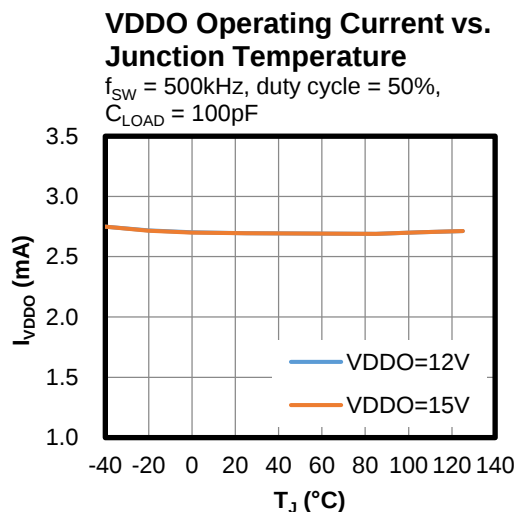
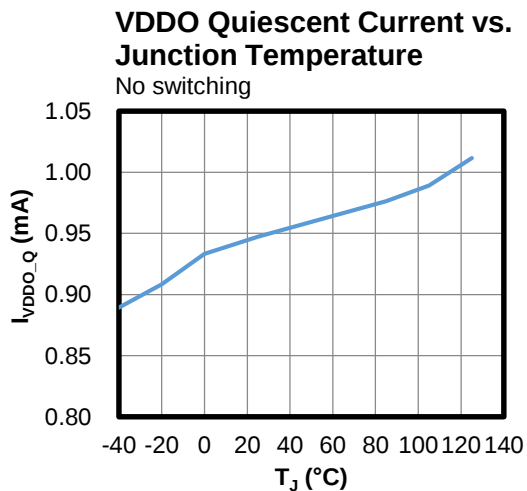
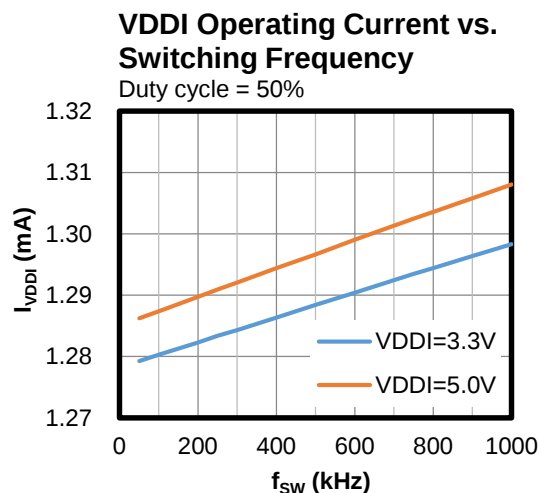
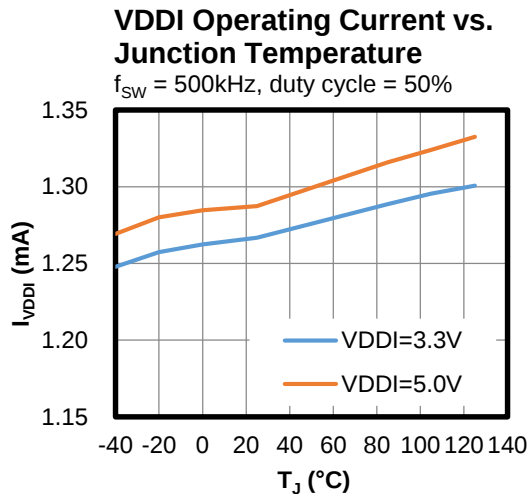
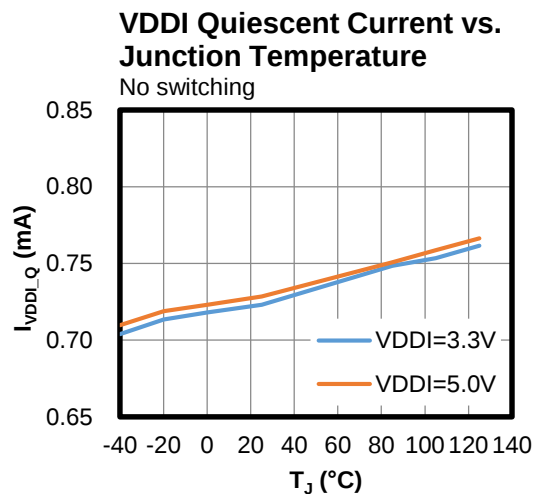
- 14) Maximum value allowed in the event of a failure.
- 15) The maximum safety temperature ( $T_S$ ) has the same value as the maximum junction temperature ( $T_J$  (MAX)) specified in the Absolute Maximum Ratings on page 6.
- 16) Tested for 5V and 8V UVLO devices.
- 17) Test conditions:  $V_{\text{DDI}} - V_{\text{GNDI}} = 5.5\text{V}$ ,  $V_{\text{DDO}} - V_{\text{SSO}} = 30\text{V}$ ,  $T_J = 150^{\circ}\text{C}$ ,  $T_A = 25^{\circ}\text{C}$ . The safety power dissipation is a function of the maximum junction temperature ( $T_J$  (MAX)), the junction-to-ambient thermal resistance ( $\theta_{JA}$ ), and the ambient temperature ( $T_A$ ). This function can be calculated using the following equations:  
 $T_S = T_J (\text{MAX}) = T_A + (\theta_{JA} \times P_S)$   
 $P_S = I_S \times V_I$   
Where  $V_I$  is the input voltage.

## THERMAL DERATING CURVES FOR SAFETY LIMITING VALUES



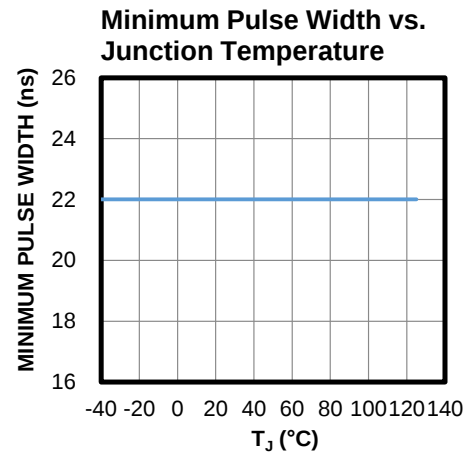
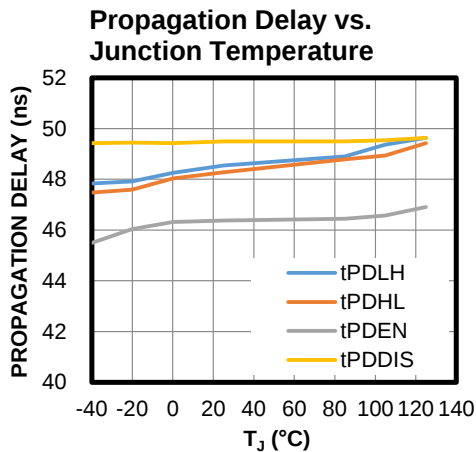
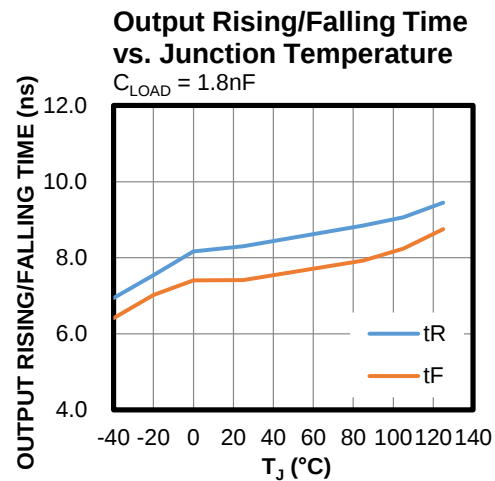
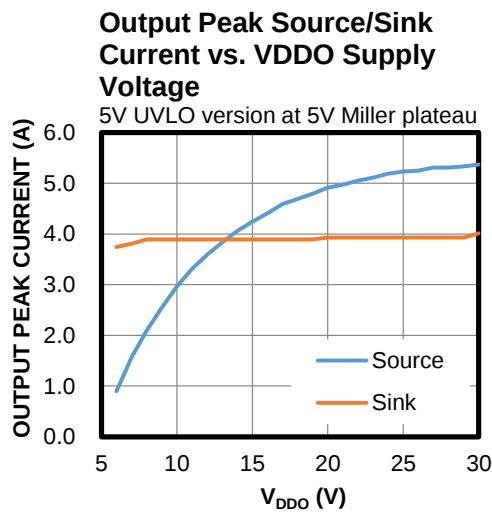
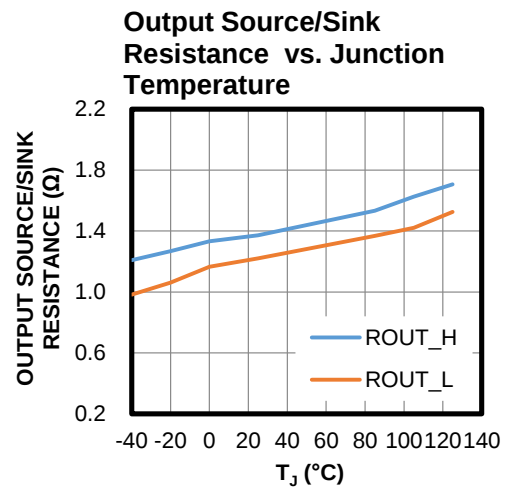
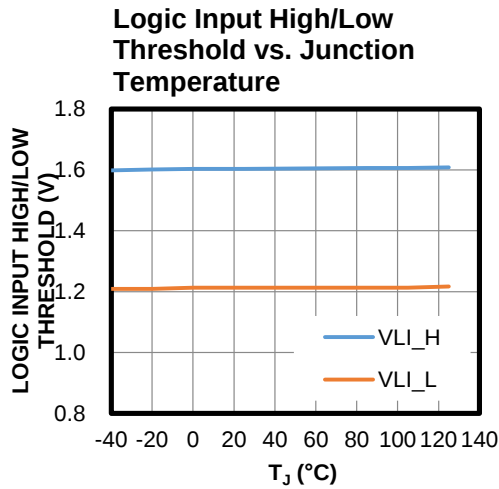
# TYPICAL CHARACTERISTICS

$V_{DDI} - V_{GNDI} = 5V$ ,  $V_{DDO} - V_{SSO} = 12V$ ,  $C_{LOAD} = 0pF$ ,  $T_J = 25^{\circ}C$ , all voltages with respect to the corresponding ground(s), unless otherwise noted.



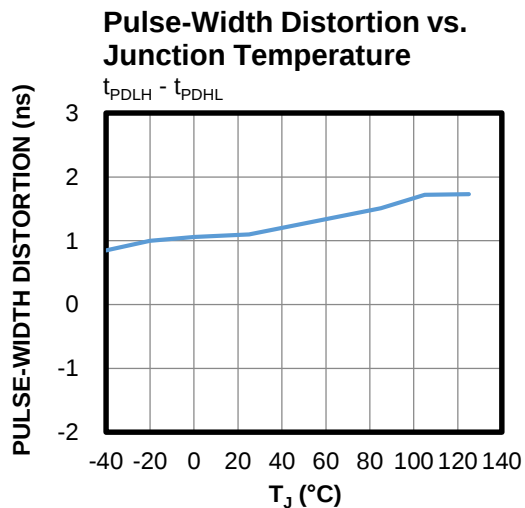
## TYPICAL CHARACTERISTICS (continued)

$V_{DDI} - V_{GNDI} = 5V$ ,  $V_{DDO} - V_{SSO} = 12V$ ,  $C_{LOAD} = 0pF$ ,  $T_J = 25^{\circ}C$ , all voltages with respect to the corresponding ground(s), unless otherwise noted.



## TYPICAL CHARACTERISTICS *(continued)*

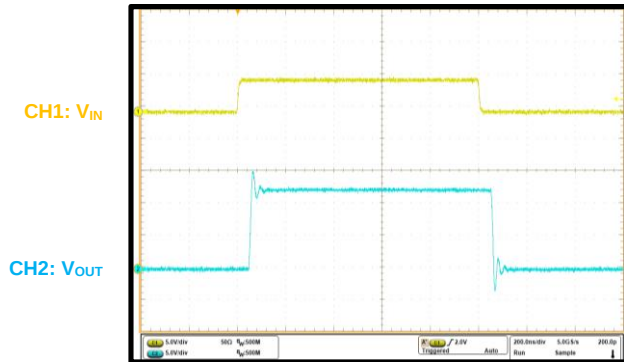
$V_{DDI} - V_{GNDI} = 5V$ ,  $V_{DDO} - V_{SSO} = 12V$ ,  $C_{LOAD} = 0pF$ ,  $T_J = 25^{\circ}C$ , all voltages with respect to the corresponding ground(s), unless otherwise noted.



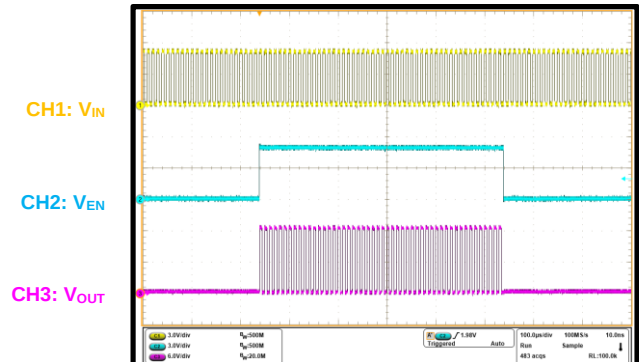
## TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.  $V_{DDI} - V_{GNDI} = 5V$ ,  $V_{DDO} - V_{SSO} = 12V$ ,  $C_{LOAD} = 0pF$ ,  $T_A = 25^{\circ}C$ , all voltages with respect to the corresponding ground(s), unless otherwise noted.

Typical Switching Waveforms



EN Control



DIS Control



# DYNAMIC PARAMETERS DEFINITIONS

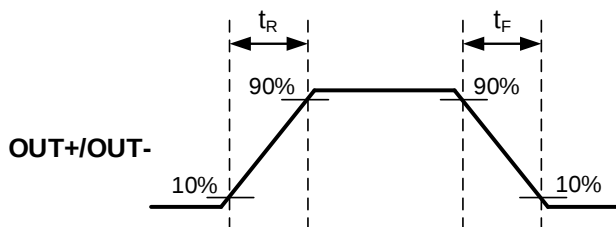


Figure 1: Output Rising and Falling Time

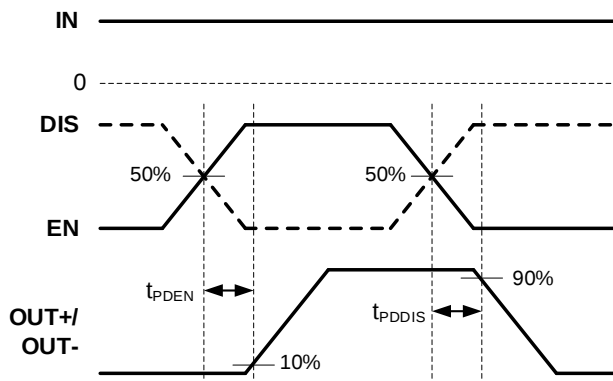


Figure 2: Enable/Disable Response Time

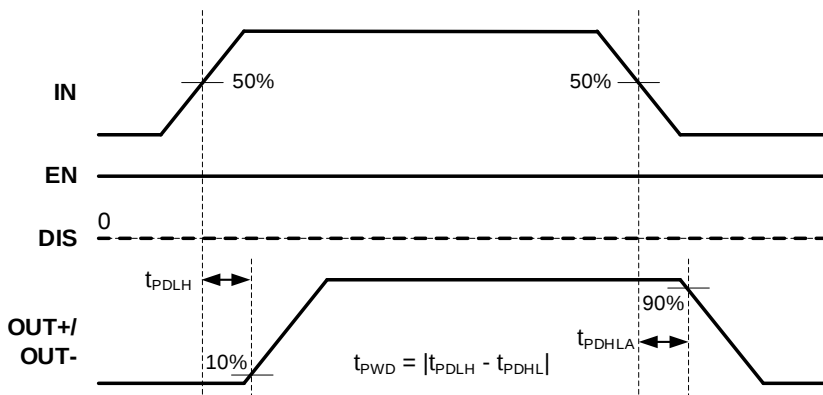
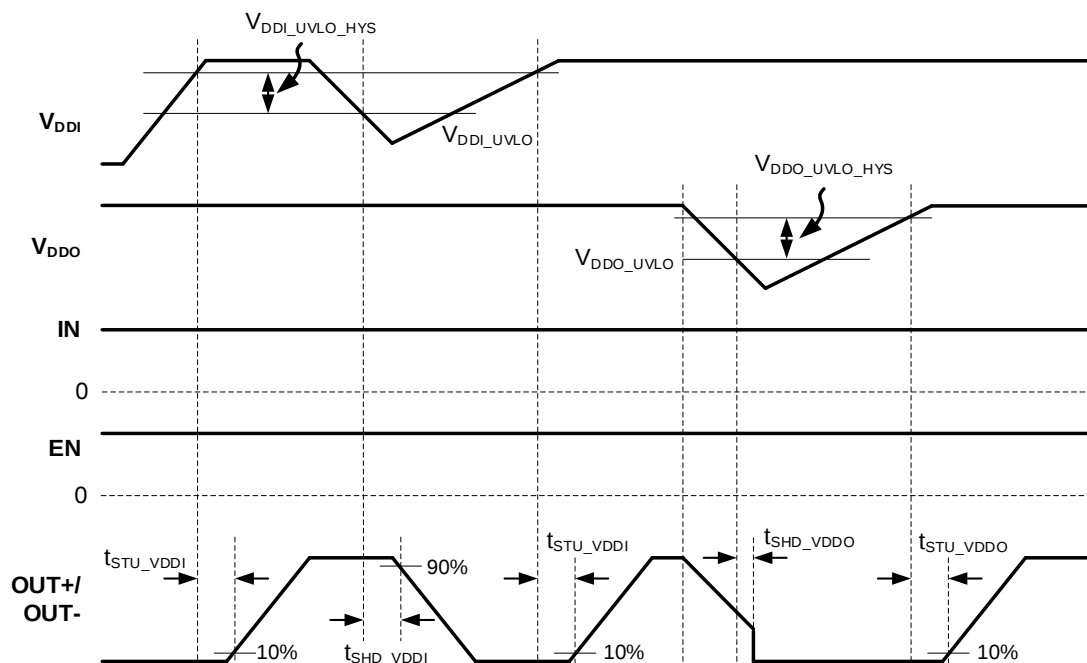


Figure 3: Propagation Delay from Input to Output

# DEFINITIONS OF DYNAMIC PARAMETERS *(continued)*



**Figure 4: V<sub>DDI</sub> and V<sub>DDO</sub> Under-Voltage Lockout (UVLO)**

## DEVICE FUNCTIONAL MODES

Table 1: Logic Truth Table <sup>(18)</sup>

| Inputs |        |        | Power Supply |      | Outputs |      | Notes                |
|--------|--------|--------|--------------|------|---------|------|----------------------|
| IN     | EN     | DIS    | VDDI         | VDDO | OUT+    | OUT- |                      |
| H      | H or O | L or O | P            | P    | H       | Hi-Z | Normal operation     |
| L or O | H or O | L or O | P            | P    | Hi-Z    | L    |                      |
| X      | L      | H      | P            | P    | Hi-Z    | L    | The chip is disabled |
| X      | X      | X      | UP           | X    | Hi-Z    | L    | VDDI is unpowered    |
| X      | X      | X      | P            | UP   | Hi-Z    | L    | VDDO is unpowered    |

**Note:**

18) L: Logic low, H: Logic high; O: Open; X: Not applicable, P: Powered, UP: Unpowered, UVLO condition.

The schematic diagram illustrates a digital isolator circuit. On the left, the input side features an input signal **IN** and a digital input **DIS**. The **IN** signal is connected to a buffer (represented by a triangle with a double slash) and a pull-up resistor to **V<sub>DDI</sub>**. The **DIS** signal is also connected to a buffer and a pull-up resistor to **V<sub>DDI</sub>**. A **UVLO** (Under-Voltage Lockout) block is connected to **V<sub>DDI</sub>** and **GNDI**. The outputs of the **IN** and **DIS** buffers and the **UVLO** block are connected to a 3-input AND gate. The output of this AND gate passes through an **Isolation Barrier**, represented by a thick grey vertical bar. On the right side of the barrier, the signal is connected to another 3-input AND gate, which also has inputs from **V<sub>DDO</sub>** and **V<sub>SSO</sub>**. The output of this second AND gate is connected to a buffer. The output of the buffer is connected to a pull-up resistor to **V<sub>DDO</sub>** and a pull-down resistor to **V<sub>SSO</sub>**. The output signal is labeled **OUT+** and **OUT-**. The **OUT+** signal is connected to a switch **SW** and a pull-up resistor to **V<sub>BUS</sub>**. The **OUT-** signal is connected to a pull-down resistor to **V<sub>SSO</sub>**.

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## OPERATION

The MP18811 is an isolated, single-channel gate driver solution with 4A peak output current capability. This IC is designed to drive power switching devices with a short propagation delay and minimal pulse-width distortion. These advanced features enable high efficiency, high power density, and robustness in a wide variety of power applications.

See Table 1 on page 18 for device functional modes.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to avoid the chip or certain blocks from operating at an insufficient supply voltage. The MP18811 incorporates internal UVLO comparators for all of the input and output supply circuit blocks to monitor the VDDI and VDDO voltages ( $V_{DDI}$  and  $V_{DDO}$ , respectively). Figure 4 shows the input and output supply UVLO time sequence diagram.

If the input bias voltage ( $V_{DDI}$ ) is unpowered or below the UVLO threshold, the chip is not enabled, and the output stage does not receive the control signals from the input stage. UVLO holds the output low, regardless of the present logic levels of the input signals (including EN/DIS and IN).

If the output stage of the driver is unpowered or below the UVLO threshold, the driver's output is also pulled low. As long as the output is powered normally, the driver can accept the related control signal.

### Input Stage and On/Off Control

All of the control input pins (EN/DIS and IN) accept a TTL/CMOS compatible logic input that is reliably isolated from each output. These control pins can easily be driven with common logic-level signals from a digital controller. However, any input signal applied to these control pins must never exceed the input stage supply ( $V_{DDI}$ ). Therefore, it is recommended to connect VDDI to the same power supply as the control signal sources. The control logic for EN and IN is active high, while the control logic of DIS is active low.

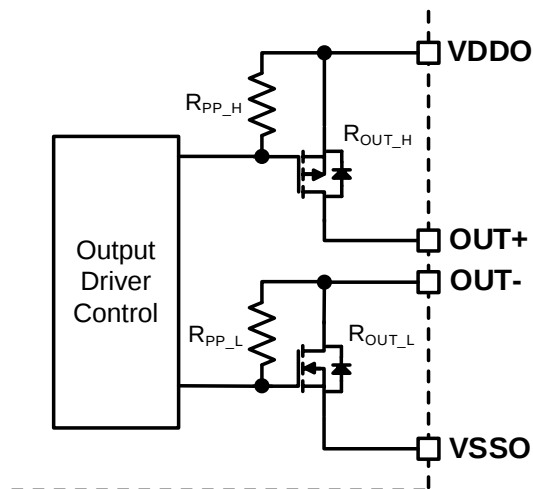
If the IN input is left open, it is forced logic low via the internal pull-down resistor. This

configuration ensures that the output remains low if the control input is not connected. It is recommended to connect the IN input to ground externally for better noise immunity and stable operation.

Similarly, for on/off control, the EN pin is connected to VDDI via the internal pull-up resistor, while the DIS pin is connected to GNDI via the internal pull-down resistor. Although leaving the EN/DIS pin floating allows the chip to operate normally after start-up, it is recommended to provide a stable external signal input for on/off control in real applications.

### Output Stage

The MP18811's output stage is comprised of an upper P-channel MOSFET and a lower N-channel MOSFET (see Figure 7). The effective output pull-up source resistance ( $R_{OUT\_H}$ ) is the on resistance of the upper P-channel MOSFET, which delivers the large peak source current during the external power switch turn-on transition. The pull-down structure is an N-channel MOSFET, for which  $R_{OUT\_L}$  is the output effective pull-down impedance when the device is driven low.



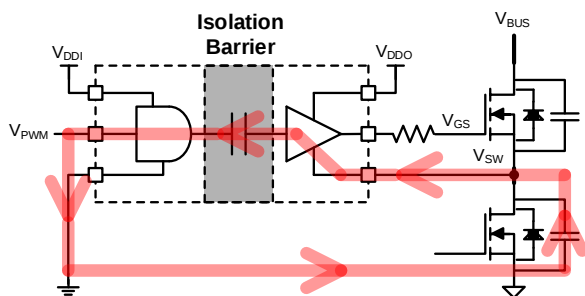
**Figure 7: Output Stage with Active-Low Clamp Circuitry**

The output stage is optimized to provide strong driving capacity to a power device during the Miller plateau interval of the on/off switching procedure.

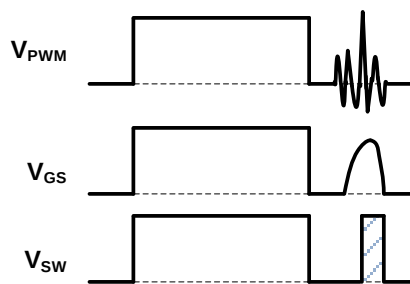
The MP18811 is capable of delivering 4A peak source/sink current pulses. The rail-to-rail output ensures that the voltage switches between  $V_{DDO}$  and  $V_{SSO}$ , respectively.

### Common-Mode Transient Immunity (CMTI)

Common-mode transient immunity (CMTI) is one of the key characteristics that determines an isolator's robustness, and is especially important in high-voltage applications that utilize devices with fast transient response (e.g. SiC/GaN FET). When a power device is switching, the high slew rate ( $dV/dt$  or  $dI/dt$ ) transient noise can corrupt the signal transmission across the isolation barrier (see Figure 8 and Figure 9).



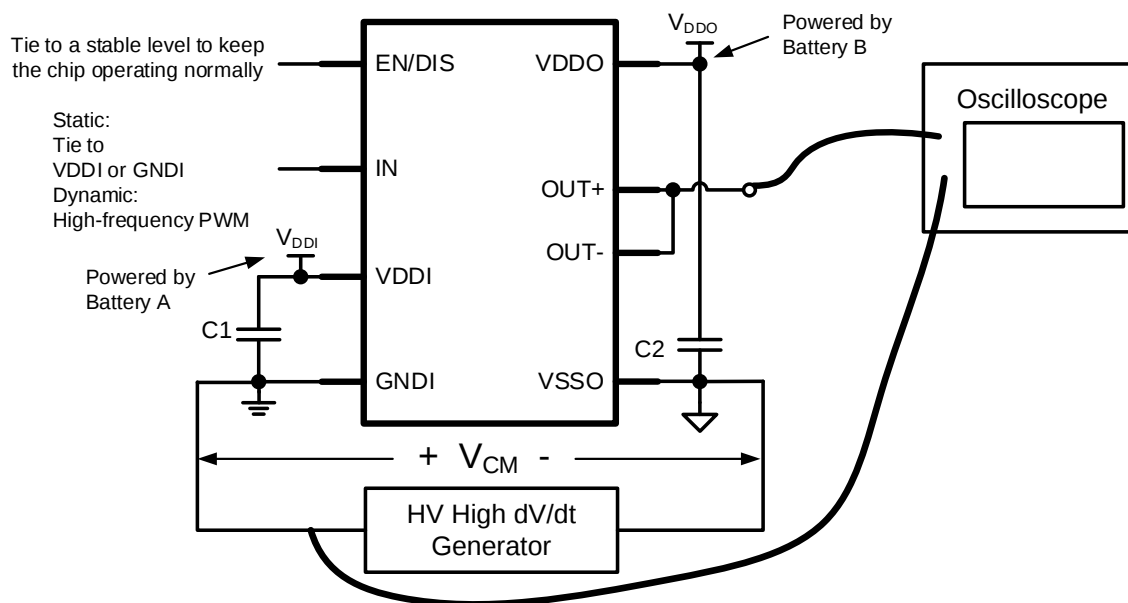
**Figure 8: High Slew Rate Transient Noise Coupling Path**



**Figure 9: Abnormal Pulse Caused by Coupled Noise if  $dV/dt > CMTI$**

CMTI is defined as the maximum tolerable rate-of-rise (or fall) of a common-mode voltage applied between two isolated circuits, given in volts per second (V/ns or kV/ $\mu$ s). Below the maximum slew rate of a common-mode voltage, the isolator's output remains at the specified logic level and timing.

Figure 10 shows the CMTI test set-up to measure the CMTI of a coupler in both static and dynamic operation, under the specified common-mode pulse magnitude ( $V_{CM}$ ), the specified slew rate for the common-mode pulse ( $dV_{CM}/dt$ ), and other specified test or ambient conditions. The isolator's output must remain in the correct state while the pulse magnitude and slew rate meet the CMTI specifications.



**Figure 10: CMTI Test Set-Up**

## APPLICATION INFORMATION

### Selecting the VDDI Capacitor

The VDDI capacitor reduces the surge current drawn from the input supply, and supports current consumption for the primary logic interface and transmitter block. Since the input side's operating current is only a few mA, a 100nF ceramic capacitor with X5R or X7R dielectrics is highly recommended because of its low ESR and small temperature coefficients. For most applications, if the real supply power is far away from the VDDI pin, then it is recommended to add a >1μF bypass capacitor in parallel with this 100nF ceramic capacitor.

### Selecting the VDDO Capacitor

The VDDO capacitor is the bypass capacitor for the output gate driver. It supports current consumption for the driving control block, maintains a stable driving voltage, and supports up to 4A of transient source current.

Given that the allowable  $V_{DDO}$  voltage ripple is  $\Delta V_{DDO}$ , and guarantees that the driver supply voltage cannot drop close to the UVLO threshold, the minimum VDDO capacitance ( $C_{VDDO}$ ) can be calculated with Equation (1):

$$C_{VDDO} = \frac{I_{VDDO} \times \frac{1}{f_{SW}} + Q_G}{\Delta V_{DDO}} \quad (1)$$

Where  $I_{VDDO}$  is the VDDO operating current,  $f_{SW}$  is the switching frequency, and  $Q_G$  is the power device's gate charge.

Keep in mind that the loop resistance, voltage drop, and DC bias voltage ripple impact the supply voltage. A 10μF ceramic capacitor is typically selected. It is also recommended to place a secondary, high-frequency, 100nF bypass capacitor in parallel.

### Selecting the Input Filter for IN

The IN input filter is not necessary in theory because the low-pass filter slows the PWM signal's rising/falling edge and affects the propagation delay. However, if there is significant high-frequency ringing introduced by the PCB traces, it is recommended to add a simple RC filter at the input, close to the IN pin.

To avoid increasing the input resistance, a resistor below 100Ω is typically recommended.

When selecting the filter capacitor, ensure that the filter's cutoff frequency is at least ten times greater than  $f_{SW}$ , where a capacitance of dozens of pF is typically sufficient.

### Selecting the External Driving Resistor

The external driving resistor can be applied to limit the ringing noise on the driving signal and adjust the switching speed to improve EMI performance. However, a higher driving resistance increases the switching losses, reduces system efficiency, and can introduce thermal issues.

The MP18811 provides split outputs that can control source and sink driving capability individually. Connect the source/sink resistor with OUT+ and OUT- ,respectively, and connect the other end of the resistors together using the device's gate.

The peak driving current can be used to evaluate the effect of the driving resistors. Without a driving resistor, the MP18811 can drive up to 4A of peak source and sink currents.

Considering the driving resistor, the peak source driving current for output ( $I_{OUT\_SRC}$ ) can be calculated with Equation (2):

$$I_{OUT\_SRC} = \frac{V_{DDO}}{R_{OUT\_H} + R_{G\_SRC} + R_{G(INT)}} \quad (2)$$

The peak sink driving current for output ( $I_{OUT\_SNK}$ ) can be calculated with Equation (3):

$$I_{OUT\_SNK} = \frac{V_{GS\_ON}}{R_{OUT\_L} + R_{G\_SNK} + R_{G(INT)}} \quad (3)$$

Where  $R_{G\_SRC}$  is the external source resistor,  $R_{G\_SNK}$  is the external sink resistor,  $R_{G(INT)}$  is the power device's internal gate resistance, and  $V_{GS\_ON}$  is the power device's stable gate-source voltage during the turn-on interval.

$V_{GS\_ON}$  should typically be close to  $V_{DDO}$ .

Since the driving current cannot exceed 4A, set the actual peak driving current to be the smaller value between the estimated  $I_{OUT\_SRC}$  or  $I_{OUT\_SNK}$  and 4A.

### Estimated Gate Driver Power Loss

The total gate driver power loss is used to estimate the thermal performance. The MP18811 must operate under the safety limiting values (see the Safety Limiting Values section on page 10 for more details).

To estimate the gate driver power loss, first calculate the chip's operating power consumption ( $P_{OP}$ ) with Equation (4):

$$P_{OP} = V_{DDI} \times I_{VDDI} + V_{DDO} \times I_{VDDO} \quad (4)$$

The gate driver's self-power consumption is related to  $f_{SW}$  and the supply voltage. For the relationship reference between the input and output channel's current consumption vs. the operating frequency, see the Typical Characteristics section on page 12.

Next, consider the gate driver power loss during switching operation. As a conventional totem-pole (TP) gate driver, the MP18811 charges and discharges the power device's gate capacitance once during every switching cycle. During the charging and the discharging period,

the total energy is supplied by  $V_{DDO}$ . If there is no external gate driver resistor, the power dissipation ( $P_{SW}$ ) can be calculated with Equation (5):

$$\begin{aligned} P_{SW} &= V_{DDO} \times \int_0^{t_{ON}} I_G(t) dt \times f_{SW} \\ &= V_{DDO} \times Q_G \times f_{SW} \end{aligned} \quad (5)$$

Where  $t_{ON}$  is the turn-on time, and  $I_G(t)$  is the driving current.

The behavior of the external source/sink resistors adds complexity to the dynamic power dissipation estimation.

If the driving current is not saturated to 4A within one switching cycle with external gate resistors, then  $P_{SW}$  is shared between the gate driver's internal source and sink resistances and the external gate driver resistors, based on the ratio of these series resistances. In this circumstance,  $P_{SW}$  can be calculated with Equation (6):

$$P_{SW} = \frac{V_{DDO} \times Q_G \times f_{SW}}{2} \times \left( \frac{R_{OUT\_H}}{R_{OUT\_H} + R_{G\_SRC} + R_{G(INT)}} + \frac{R_{OUT\_L}}{R_{OUT\_L} + R_{G\_SNK} + R_{G(INT)}} \right) \quad (6)$$

In some conditions, the MP18811 outputs the saturated 4A current at the beginning of the turn-on/off interval. During this saturation time,

the power loss ( $P_{SW\_SAT}$ ) can be calculated with Equation (7):

$$P_{SW\_SAT} = 4A \times \int_0^{t_{ON\_SAT}} (V_{DDO} - V_{GS}(t)) dt + 4A \times \int_0^{t_{OFF\_SAT}} V_{GS}(t) dt \quad (7)$$

Where  $t_{ON\_SAT/OFF\_SAT}$  is the turn-on/off time with a saturated 4A current output, and  $V_{GS}(t)$  is the power device's gate voltage during this saturation time.

The actual power loss is the sum of Equation (4) and Equation (5). Therefore, the total power loss dissipated in the MP18811 ( $P_{LOSS}$ ) can be calculated with Equation (8):

$$P_{LOSS} = P_{OP} + P_{SW} \quad (8)$$

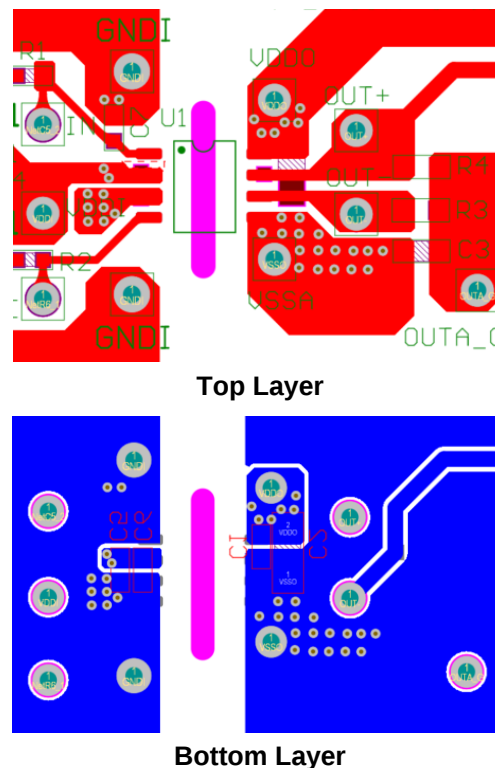
Multiply  $P_{LOSS}$  by the junction-to-ambient thermal resistance ( $\theta_{JA}$ ) to determine the junction temperature rise above the ambient temperature. Ensure that the junction temperature ( $T_J$ ) is below the maximum safety temperature ( $T_S$ ).

## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 11 and follow the guidelines below:

1. Place the bypass/decoupling capacitors as close as possible to the VDDI and VDDO supply pins and the corresponding grounds. For each supply pin, it is recommended to add a low-ESR/ESL, high-frequency, 100nF bypass capacitor.
2. If an input RC filter is used, it is recommended to place this filter close to the corresponding control pin.
3. Place the high-current paths (e.g. the supply path, drive path, and the connection between the external power device source and the VSSO pin) very close to the driver chip with short, direct, and wide traces to minimize the parasitic inductance and avoid large transients and ringing noise.
4. It is strongly recommended to place large power and ground planes (or multiple ground layers) to help dissipate heat from the gate driver chip to the PCB and improve the thermal performance. Be careful when splitting the traces or coppers to allow sufficient insulation distance between the different low-/high-voltage planes.
5. Keep the driving loop from OUT+/OUT- to the power device's gate-to-source to VSSO short and with minimal area. Avoid placing the driving trace across different PCB layers through vias, as it can introduce parasitic inductance. Place the driver IC as close as possible to the power device.

6. Use the recommended land pattern design for each package type to ensure adequate insulation space between the primary and secondary sides. Avoid placing any components, tracks, or copper below the chip's body in any PCB layer.
7. A board cutout under the chip is recommended to extend the creepage distance on the PCB surface.

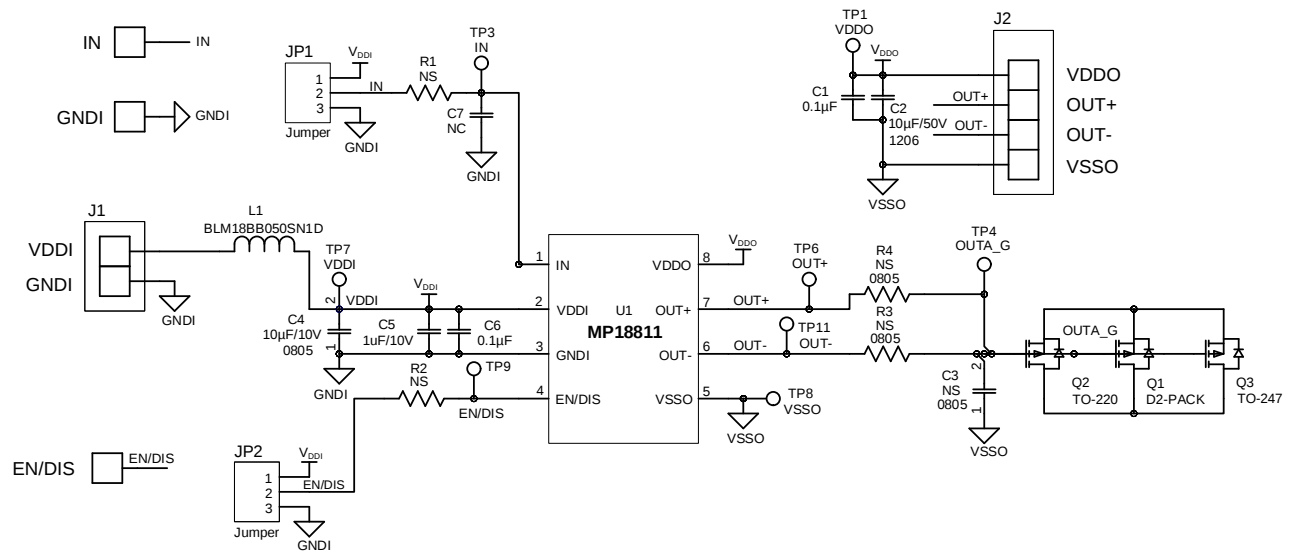


**Figure 11: Recommended PCB Layout** <sup>(19)</sup>

**Note:**

- 19) This example uses a 2-layer PCB layout.

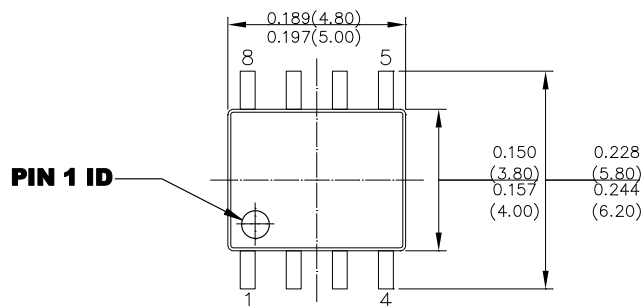
## TYPICAL APPLICATION CIRCUIT



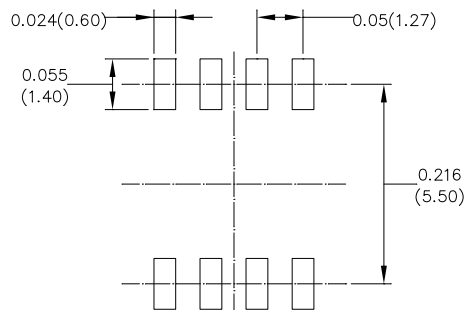
**Figure 12: Typical Application Circuit**

# PACKAGE INFORMATION

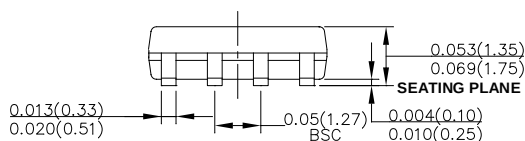
## SOIC-8 NB (HV ISOLATION)



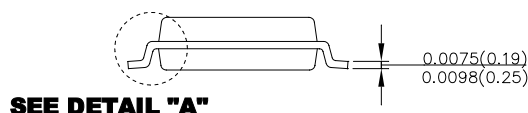
**TOP VIEW**



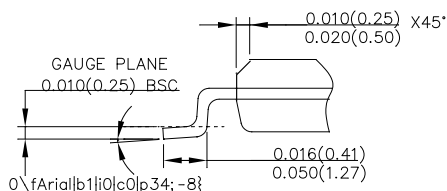
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**

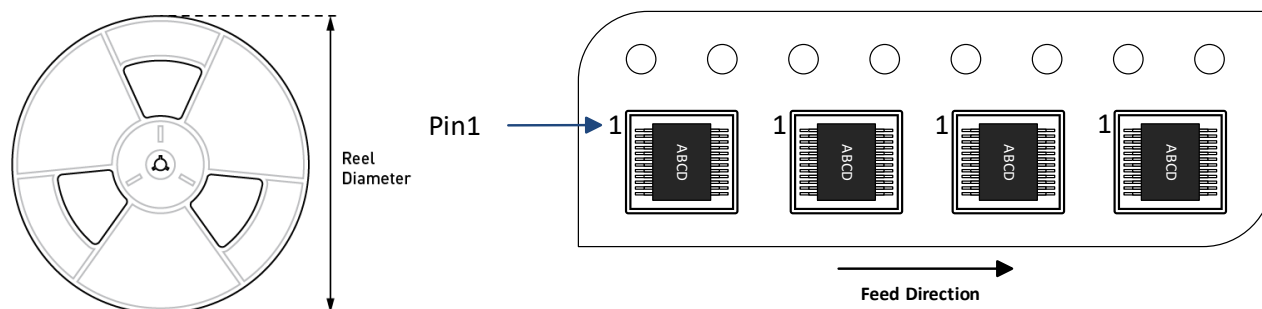


**DETAIL "A"**

### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING REFERENCE TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

# CARRIER INFORMATION



| Part Number   | Package Description | Quantity/ Reel | Quantity/ Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---------------|---------------------|----------------|----------------|---------------|--------------------|--------------------|
| MP18811-4AGS  | SOIC-8 NB           | 2500           | 100            | 13in          | 12mm               | 8mm                |
| MP18811-4BGS  |                     |                |                |               |                    |                    |
| MP18811-4CGS  |                     |                |                |               |                    |                    |
| MP18811-4DGS  |                     |                |                |               |                    |                    |
| MP18811-4EGS  |                     |                |                |               |                    |                    |
| MP18811-A4AGS | SOIC-8 NB           | 2500           | 100            | 13in          | 12mm               | 8mm                |
| MP18811-A4BGS |                     |                |                |               |                    |                    |
| MP18811-A4CGS |                     |                |                |               |                    |                    |
| MP18811-A4DGS |                     |                |                |               |                    |                    |
| MP18811-A4EGS |                     |                |                |               |                    |                    |

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 4/21/2023     | Initial Release | -             |

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