MP183

Non-Isolated, Up to 250mA Output Current, Zero Standby Buck Regulator

DESCRIPTION

The MP183 is a primary-side regulator that provides accurate constant voltage (CV) regulation without an optocoupler. It supports buck, buck-boost, and flyback topologies. The MP183 has an integrated, 700V MOSFET that simplifies structure and reduces costs, which means the MP183 is well-suited for offline, low-power applications.

The MP183 is a green-mode operation regulator. Both the current limit (I_{LIMIT}) and the switching frequency (f_{SW}) decrease as the load decreases, which provides excellent efficiency at light loads, and burst mode prevents audible noise. The MP183 can achieve below 3mW of no-load consumption under $265V_{AC}$, which is ideal for Internet of Things (IoT) applications, such as smart plugs and wall switches.

The MP183 features various protections, including thermal shutdown (TSD), VCC voltage (V_{CC}) under-voltage lockout (UVLO), brown-in (B/I), open-loop detection (OLD), overload protection (OLP), and short-circuit protection (SCP).

The MP183 is available in TSOT23-5 and SOIC-8 packages.

FEATURES

- Constant Voltage (CV) Control Supports Buck, Buck-Boost, and Flyback Topologies
- Integrated 700V, 17.5Ω MOSFET
- Internal High-Voltage (HV) Current Source
- Externally Adjustable, or Internally Fixed 12V Output
- Improved Electromagnetic Interference (EMI) Performance
- <3mW No-Load Consumption at $265V_{AC}$ and 5V Output
- Anti-Audible Operation with Burst Mode
- Frequency Foldback
- Thermal Shutdown (TSD), V_{CC} Under-Voltage Lockout (UVLO), Brown-In (B/I), Open-Loop Detection (OLD), Overload Protection (OLP), and Short-Circuit Protection (SCP)
- Available in TSOT23-5 and SOIC-8 Packages

APPLICATIONS

- Internet of Things (IoT) Power Supplies, Including Non-Neutral Applications
- Non-Isolated Modules
- Ultra-Low Consumption Standby and Auxiliary Supplies

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TYPICAL APPLICATION

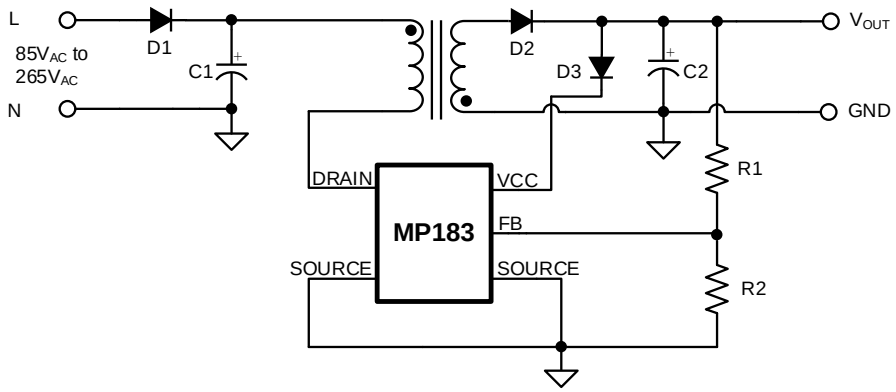

Figure 1: Typical Flyback Converter Application

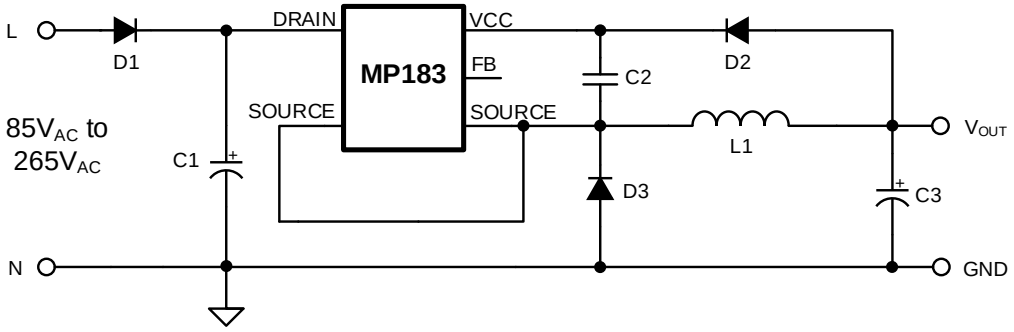

Figure 2: Typical Buck Converter Application

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP183GJ	TSOT23-5	*See Below*	1
MP183GS	SOIC-8	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MP183GJ-Z, MP183GS-Z).

TOP MARKING (MP183GJ-Z)

BZAY

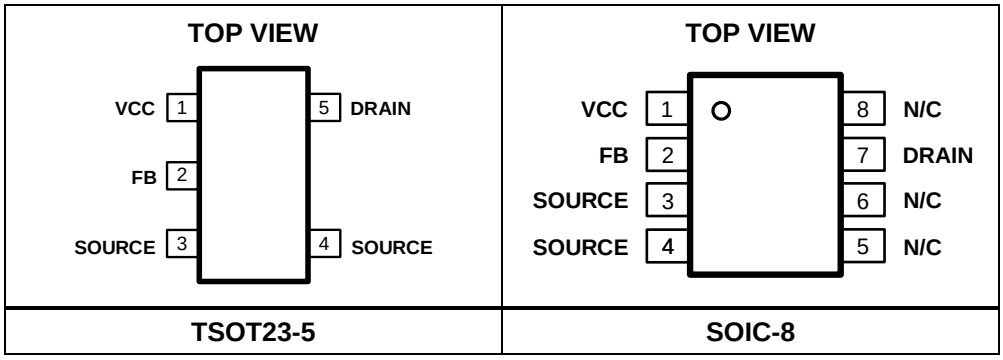
BZA: Product code
Y: Year code

TOP MARKING (MP183GS-Z)

MP183
LLLLLLLL
MPSYWW

MP183: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #		Name	Description
TSOT23-5	SOIC-8		
1	1	VCC	**Control circuit power supply.** The VCC pin is available for internal feedback.
2	2	FB	**Regulator feedback.**
3, 4	3, 4	SOURCE	**Internal power MOSFET source.** The SOURCE pin is the ground reference for the VCC and FB pins.
5	7	DRAIN	**Internal power MOSFET drain.** The DRAIN pin is the high-voltage (HV) current source input.
-	5, 6, 8	N/C	**Not connected.**

ABSOLUTE MAXIMUM RATINGS (1)

Drain-to-source (T_J = 25°C) .....-0.3V to +700V
VCC-to-source .....-0.3V to +30V
All other pins .....-0.3V to +6.5V
Continuous power dissipation .....(T_A = 25°C) (2)
TSOT23-5 ..... 1W
SOIC-8 ..... 1W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -60°C to +150°C

ESD Ratings

Human body model (HBM) 2.0kV
Charged-device model (CDM).....1.5kV

Recommended Operating Conditions (3)

Operating V_{CC} range ..... 4.5 to 26V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-5 ..... 100 ..... 55... °C/W
SOIC-8..... 96 ..... 45... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated with P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown (TSD). Internal TSD circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-up Current Source and Internal MOSFET (Drain Pin)						
Internal regulator supply current	$I_{REGULATOR}$	V_{CC} = V_{CC_OFF} - 0.1V, V_{DRAIN} = 40V, T_J = 25°C	1.9	2.2	2.5	mA
Drain pin leakage current	I_{LEAK}	V_{DRAIN} = 400V, T_J = 25°C			1	μA
Breakdown voltage	$V_{(BR)DSS}$		700			V
On resistance	$R_{DS(ON)}$	T_J = 25°C		17.5	22	Ω
Maximum on time	t_{ON_MAX}		18	24	30	μs
Minimum off time	t_{OFF_MIN}		11	14	17.5	μs
Overload protection (OLP) valid cycles		t_{OFF} = t_{OFF_MIN}		4096		
Brown-in (B/I) threshold	V_{DS_BI}			40		V
Supply Voltage Management (VCC Pin)						
Threshold to stop the internal regulator	V_{CC_OFF}		4.36	4.55	4.75	V
Threshold to start the internal regulator	V_{CC_ON}		3.88	4.1	4.3	V
Under-voltage lockout (UVLO) rising threshold	$V_{CC_UVLO_RISING}$			V_{CC_OFF}		V
UVLO falling threshold	$V_{CC_UVLO_FALLING}$		3.4	3.6	3.75	V
High-voltage (HV) current source turn-on threshold and UVLO falling threshold hysteresis		V_{CC_ON} - $V_{CC_UVLO_FALLING}$	390			mV
Protections reset threshold	V_{CC_PRO}		2.08	2.3	2.5	V
IC consumption	I_{CC}	f_{SW} = 30kHz, V_{CC} = 5.3V			1300	μA
		f_{SW} = 250Hz, V_{CC} = 5.3V			170	μA
Regulating voltage (MOSFET turn-on threshold)	V_{CC_REF}	FB open	11.7	12.2	13.15	V
IC consumption (latch-off phase)	I_{CCL}			9	24	μA
Internal Current Sense (Source Pin)						
Peak current limit	I_{LIMIT_PEAK}	T_J = 25°C	390	440	490	mA
Leading-edge blanking time	t_{LEB1}			330		ns
Short-circuit protection (SCP) threshold	I_{SCP}	T_J = 25°C	450	600		mA
Leading-edge blanking time for SCP (5)	t_{LEB2}			280		ns
Minimum current limit (5)	I_{LIMIT_MIN}			110		mA
Burst I_{LIMIT} (5)	I_{LIMIT_BURST}			160		mA
External Feedback (FB/NC Pin)						
Reference voltage (MOSFET turn-on threshold)	V_{REF}		1.16	1.215	1.265	V
Internal low-side (LS) lower resistance	R_{LOW}			0.52		MΩ

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ELECTRICAL CHARACTERISTICS *(continued)*

T_J = -40-125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Internal high-side (HS) upper resistance	R_{UP}			4.8		MΩ
Open-loop detection (OLD) threshold	V_{OLD}		0.16	0.2	0.24	V
Burst high level	V_{FBH}		1.23	1.27	1.32	V
Burst low level	V_{FBL}		1.12	1.17	1.215	V
Burst fast recovery level	V_{FBL_FAST}		1.04	1.08	1.125	V
Minimum frequency	f_{SW_MIN}	T_J = 25°C		21		kHz
Thermal Shutdown (TSD)						
TSD threshold (5)				150		°C

Note:

5) Guaranteed by design.

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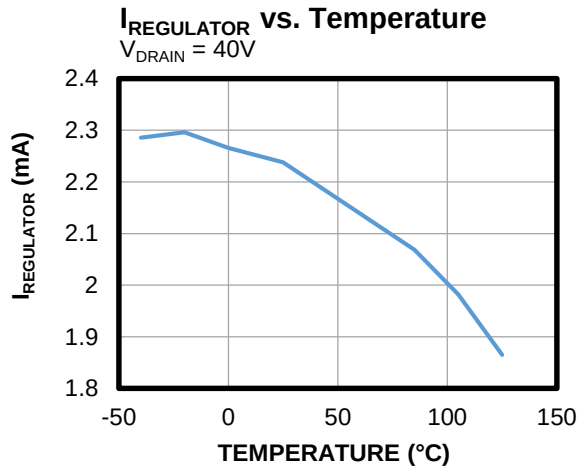

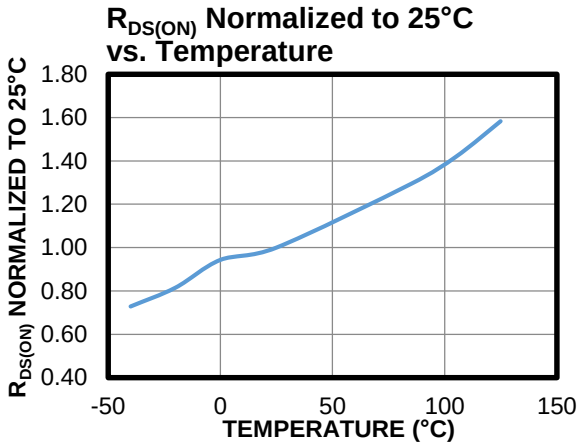

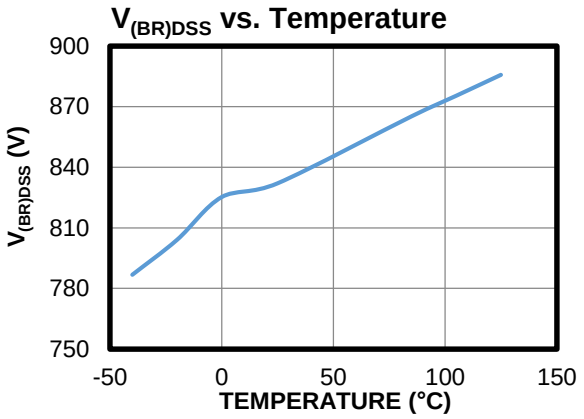

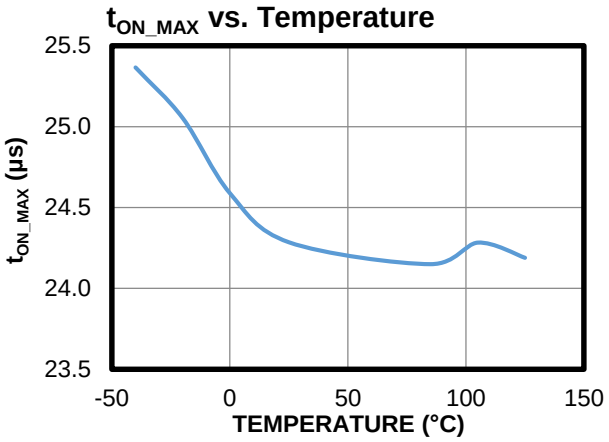

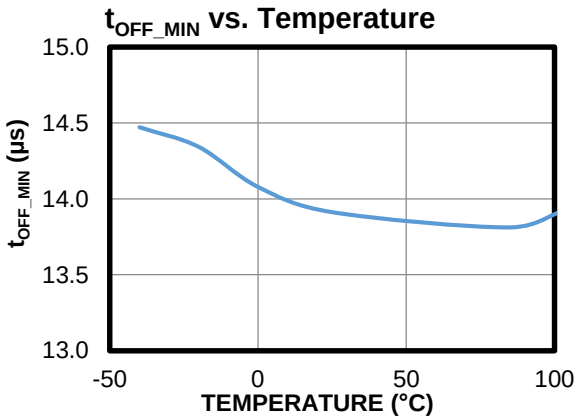

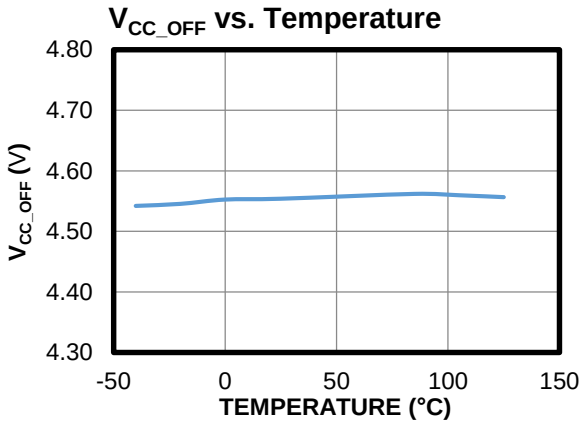

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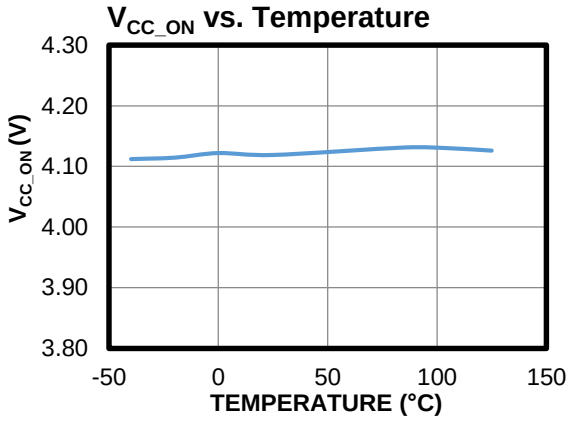

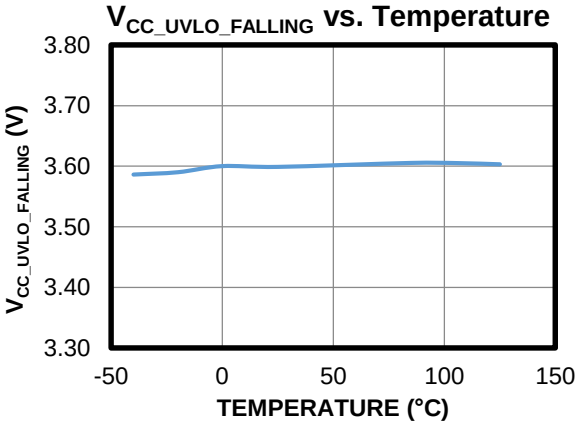

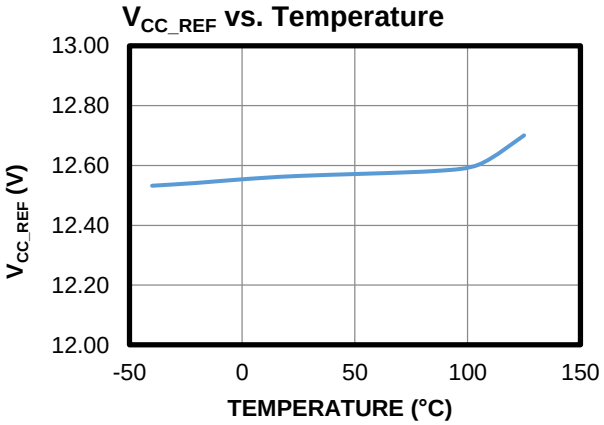

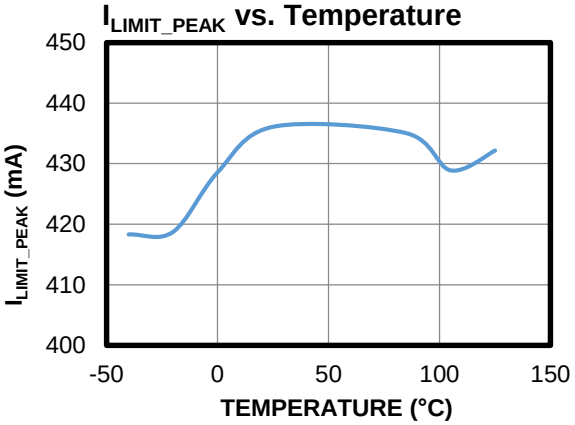

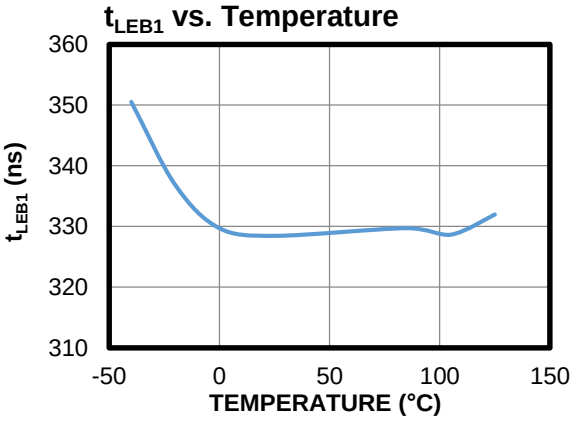

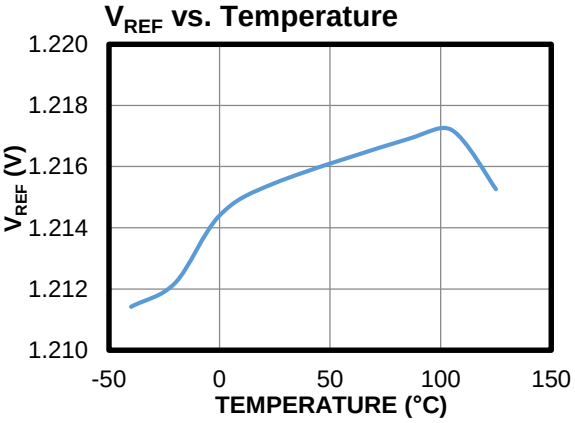

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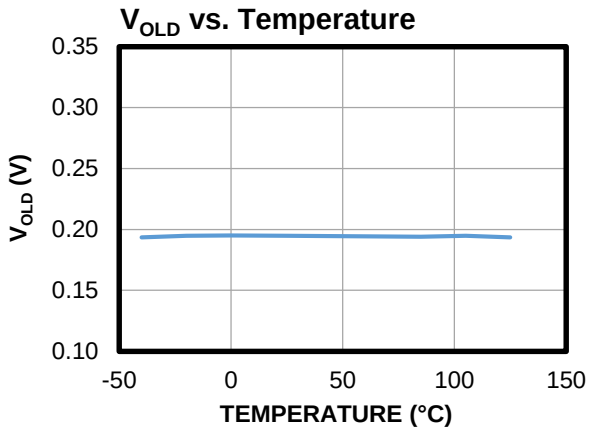

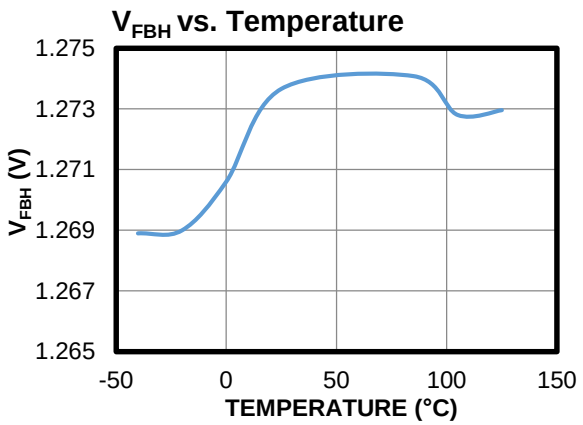

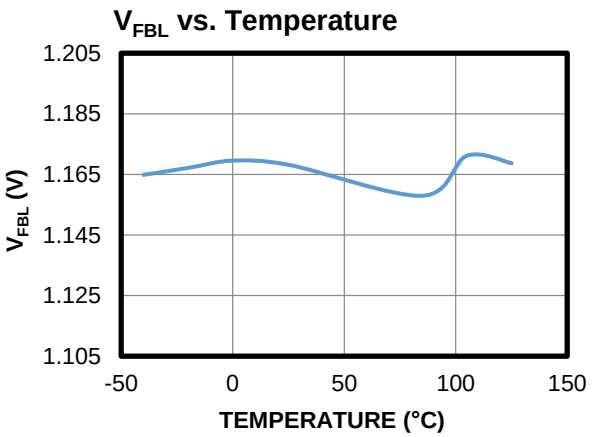

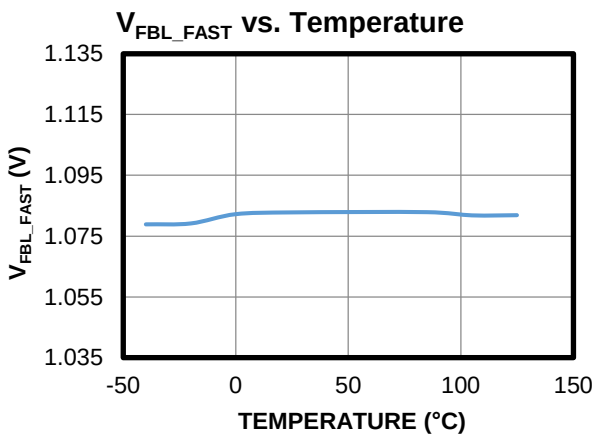

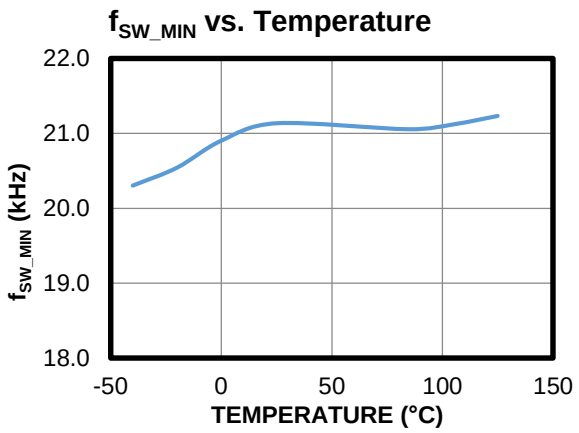

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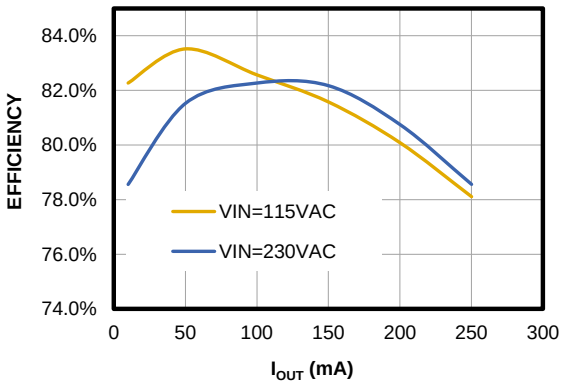
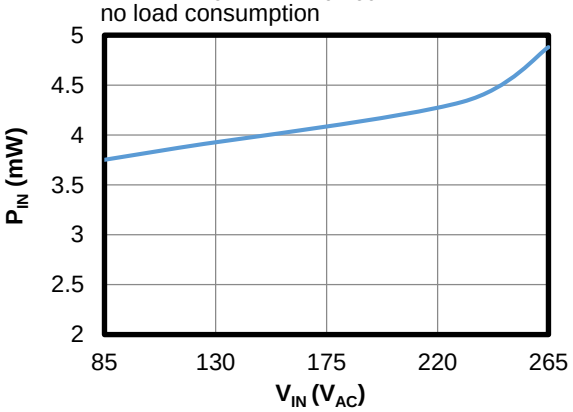
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 230V_{AC}, V_{OUT} = 12V, I_{OUT} = 250mA, L = 1mH, C_{OUT} = 470µF, T_A = 25°C, unless otherwise noted.

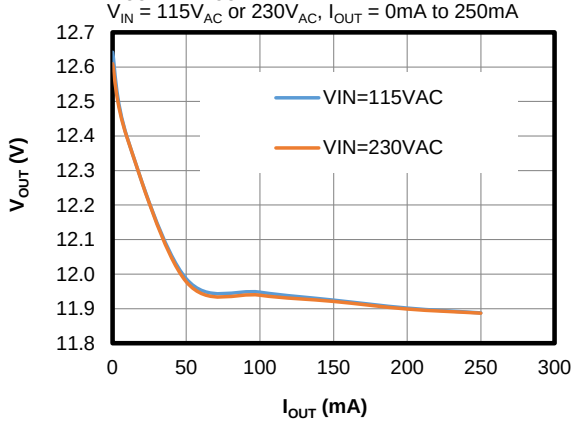
Efficiency vs. I_{OUT}
V_{IN} = 115V_{AC} or 230V_{AC}, I_{OUT} = 0mA to 250mA



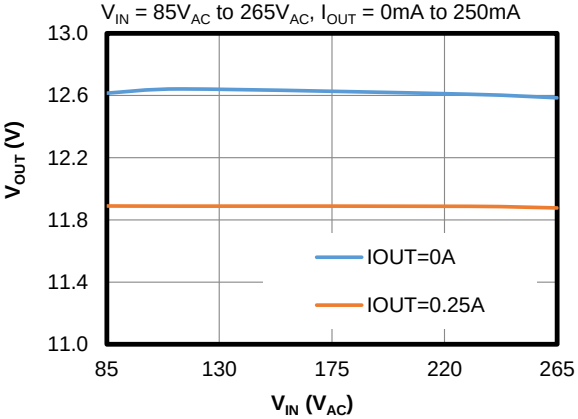
P_{IN} vs. V_{IN}
V_{IN} = 85V_{AC} to 265V_{AC}, I_{OUT} = 0A,
no load consumption



V_{OUT} vs. I_{OUT}
V_{IN} = 115V_{AC} or 230V_{AC}, I_{OUT} = 0mA to 250mA



V_{OUT} vs. V_{IN}
V_{IN} = 85V_{AC} to 265V_{AC}, I_{OUT} = 0mA to 250mA



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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

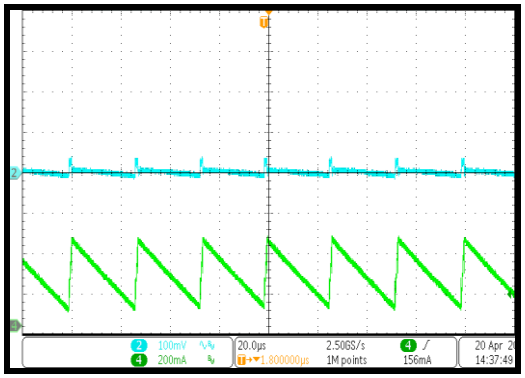
V_{IN} = 230V_{AC}, V_{OUT} = 12V, I_{OUT} = 250mA, L = 1mH, C_{OUT} = 470µF, T_A = 25°C, unless otherwise noted.

Output Voltage Ripple

V_{IN} = 230V_{AC}, I_{OUT} = 250mA

CH2: V_{OUT_AC}

CH4: I_L



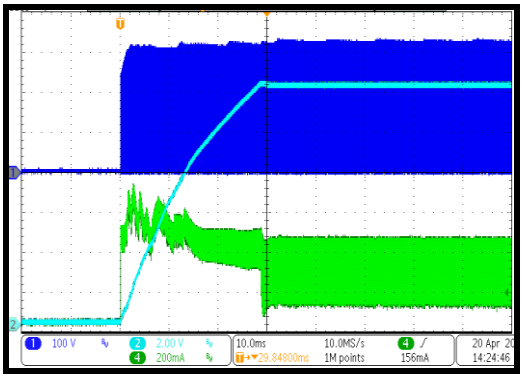
Start-Up

V_{IN} = 230V_{AC}, I_{OUT} = 250mA

CH1: V_S

CH2: V_{OUT}

CH4: I_L



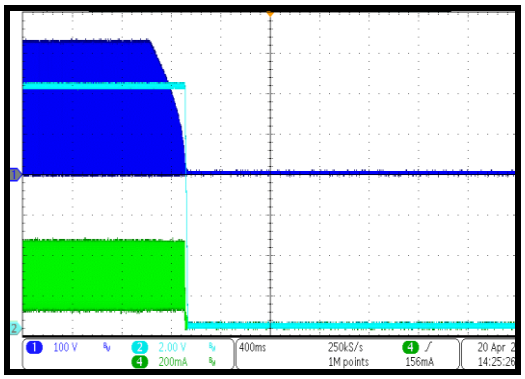
Shutdown

V_{IN} = 230V_{AC}, I_{OUT} = 250mA

CH1: V_S

CH2: V_{OUT}

CH4: I_L



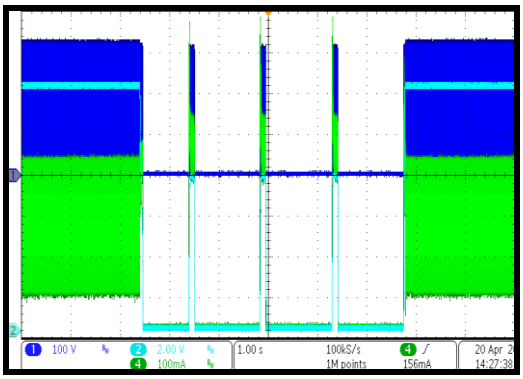
OLP Entry and Recovery

V_{IN} = 230V_{AC}, I_{OUT} = 250mA

CH1: V_S

CH2: V_{OUT}

CH4: I_L



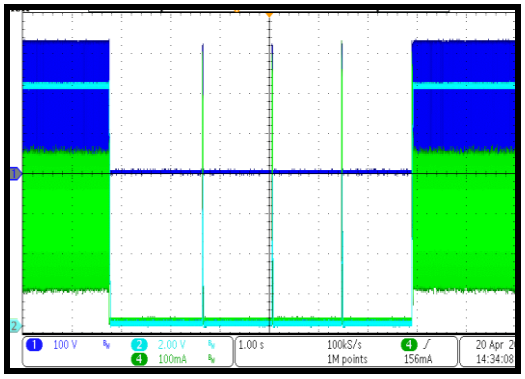
Open Loop Entry and Recovery

V_{IN} = 230V_{AC}, I_{OUT} = 250mA

CH1: V_S

CH2: V_{OUT}

CH4: I_L

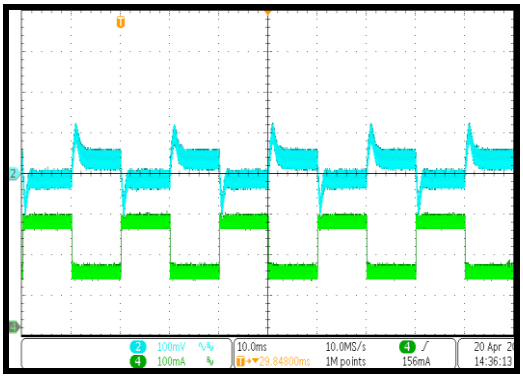


Load Transient

V_{IN} = 230V_{AC}, from half-load to full load

CH2: V_{OUT_AC}

CH4: I_{OUT}



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FUNCTIONAL BLOCK DIAGRAM

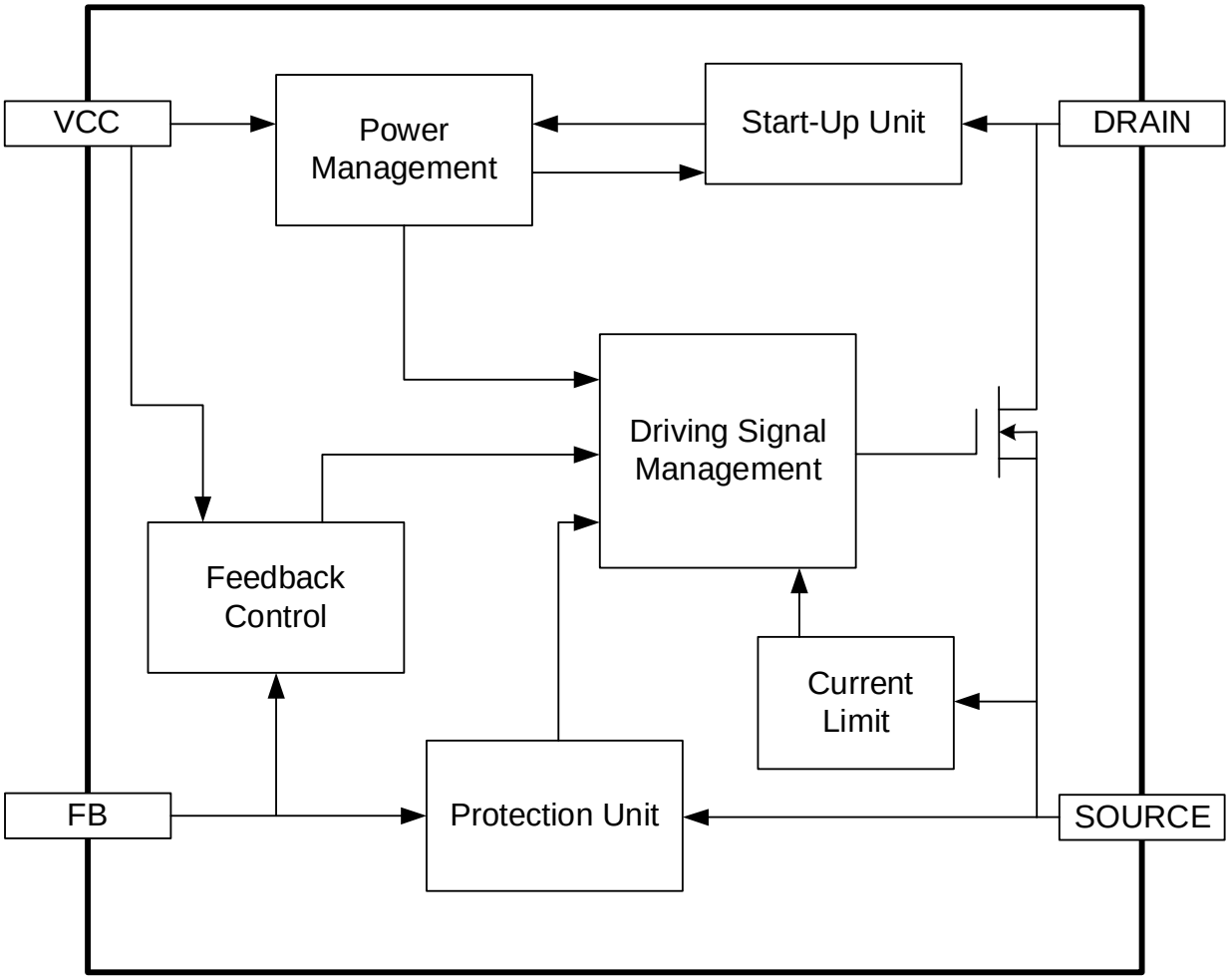

Figure 3: Functional Block Diagram

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OPERATION

The MP183 is a green-mode offline regulator with an integrated, 700V MOSFET. It incorporates multiple features that are described in greater detail below.

Start-Up and Under-Voltage Lockout (UVLO)

The internal high-voltage (HV) regulator supplies the MP183 from the DRAIN pin. When the VCC voltage (V_{CC}) reaches the threshold to stop the internal regulator (V_{CC_OFF}), the internal HV regulator turns off and brown-in (B/I) detection is enabled.

The MP183 starts switching after the drain-to-source voltage (V_{DS}) reaches the B/I threshold (V_{DS_BI}). The internal HV regulator turns on to charge the external VCC capacitor when V_{CC} falls below the threshold to start the internal regulator (V_{CC_ON}). Through this process, the power supply can start up with a very small capacitor (in the low µF range) on VCC.

If V_{CC} falls below the under-voltage lockout (UVLO) lower threshold ($V_{CC_UVLO_FALLING}$), UVLO stops the device's switching to prevent misbehaviors caused by an insufficient supply voltage. The MP183 remains shut down until V_{CC} charges to V_{CC_OFF} again (see Figure 4).

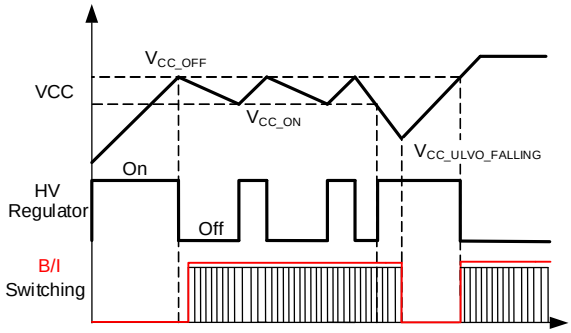

Figure 4: Start-Up and UVLO Operation

Soft Start (SS)

When the chip starts switching, there is a soft-start period, which can effectively prevent the inductor current (I_L) from overshoot.

The MP183 implements soft start (SS) by gradually reducing the minimum off time (t_{MIN_OFF}) in 8 steps. Table 1 shows the sequence pattern during SS.

Table 1: Soft Start Pattern

Step	Min Off Time (µs)	Cycles
#1	48	16
#2	36	16
#3	24	32
#4	20	64
#5	18	128
#6	16	128
#7	14	128
#8	13	128

Constant Voltage (CV) Operation

The MP183 integrates a 700V regulator that regulates the output voltage (V_{OUT}) through feedback on the VCC or FB pin, depending on the external set-up. When the external divider is not connected, the regulator operates at a fixed output via the internal feedback on VCC. The VCC capacitor samples and maintains V_{OUT}, regardless of whether the regulator is set up as a fixed output or adjustable output. In addition, the VCC capacitor supplies power for the MP183 operation.

An internal feedback resistor divider simplifies the external circuit and reduces the cost of additional components. The lower resistor is typically 520kΩ. As a result, when a feedback divider with a lower-value resistance is externally connected to FB, the internal feedback is overridden, which means that the regulator can adjust V_{OUT}.

Figure 5 shows how the internal MOSFET turns on when the feedback voltage (V_{FB}) falls below the reference voltage (V_{REF}), and turns off based on the current limit (I_{LIMIT}).

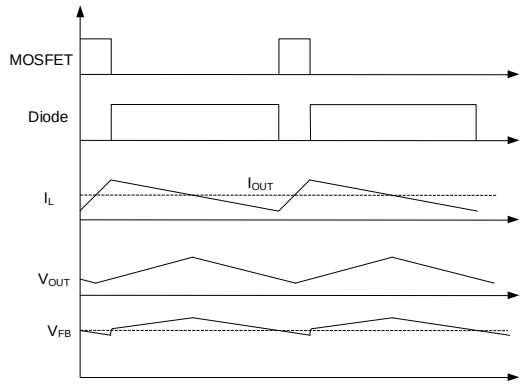

Figure 5: Constant Voltage Regulation in the Buck Converter

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Figure 6 shows how to adjust the output by tuning R_1 and R_2.

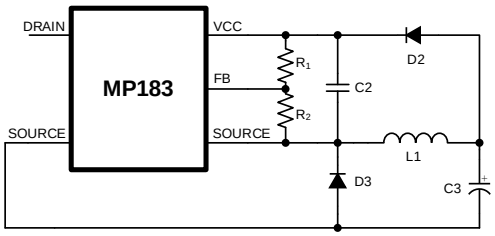

Figure 6: External Divider for Adjustable Output

V_{OUT} for the external feedback can be calculated with Equation (1):

$$V_{OUT} = V_{REF} \times \frac{(R_1 + R_2)}{R_2} - V_{D3} + V_{D2} \quad (1)$$

Frequency and Peak Current Foldback

Due to the MP183's constant voltage (CV) regulation scheme, the HV regulator's switching frequency (f_{SW}) decreases as the load decreases. As a result, the MP183 can achieve excellent efficiency under light-load conditions. f_{SW} in continuous conduction mode (CCM) can be estimated with Equation (2):

$$f_{SW} = \frac{(V_{IN} - V_{OUT})}{2 \times L \times (I_{LIMIT} - I_{OUT})} \times \frac{V_{OUT}}{V_{IN}} \quad (2)$$

f_{SW} in discontinuous conduction mode (DCM) can be estimated with Equation (3):

$$f_{SW} = \frac{2 \times (V_{IN} - V_{OUT})}{L \times I_{LIMIT}^2} \times \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \quad (3)$$

To minimize audible noise issues when the frequency drops to the audible range, I_{LIMIT} falls when f_{SW} falls.

I_{LIMIT} (with a lower limit of I_{LIMIT_MIN}) can be calculated with Equation (4):

$$I_{LIMIT} = I_{LIMIT_PEAK} - 16mA/\mu s \times (t_{OFF} - 22\mu s) \quad (4)$$

Where t_{OFF} is the internal MOSFET's off time.

Burst Mode

The MP183 employs burst mode to further reduce noise. The MP183 has a limited frequency set at f_{SW_MIN}. If f_{SW_MIN} is reached, V_{OUT} increases along with V_{FB}. When V_{FB} reaches the burst high level (V_{FBH}), the MP183 enters burst mode. In burst mode, the MP183 stops transferring energy, and continues switching until V_{FB} drops to the burst low level (V_{FBL}).

During the switching on period, f_{SW} is fixed at f_{SW_MIN}, and I_{LIMIT} is set to the burst current limit (I_{LIMIT_BURST}) from the fourth cycle. I_{LIMIT} for the first three cycles is limited by the minimum current limit (I_{LIMIT_MIN}). The MP183 can recover from burst mode when V_{FB} meets the conditions below:

- V_{FB} is below V_{FBL} for 40 cycles
- V_{FB} is below burst fast recovery level (V_{FBL_FAST})

To prevent the device from entering burst mode due an overshoot under transient conditions, a blanking time is added. The following parameters are blanked under specific conditions:

- Blank f_{SW_MIN} and burst mode for 4096 cycles during start-up.
- Blank f_{SW_MIN}, burst mode, and short-circuit protection (SCP) for 896 cycles after recovering from burst mode.
- Blank f_{SW_MIN} for 64 cycles once the minimum t_{OFF} (t_{OFF_MIN}) is triggered.

Leading-Edge Blanking (LEB)

An internal leading-edge blanking (LEB) unit prevents premature switching pulse termination due to a turn-on spike. The spike is caused mainly by parasitic capacitance and reverse recovery of the freewheeling diode.

Protections

If a protection is triggered, the MP183 stops switching, the internal HV regulator is disabled, and then the VCC capacitor is discharged by IC consumption current in the latch-off phase (I_{CCL}). The internal HV regulator is not enabled again until V_{CC} drops below the protections reset threshold (V_{CC_PRO}).

Overload Protection (OLP)

The switching regulator's maximum output power is limited by t_{OFF_MIN} and I_{LIMIT_PEAK}. If the load exceeds the limit, V_{OUT} cannot stay in regulation. When f_{SW} runs within the t_{OFF_MIN} limitation for 4096 consecutive cycles, overload protection (OLP) is triggered. The validation

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time for OLP can effectively prevent OLP from being tripped during start-up and transient periods.

Short Circuit Protection (SCP)

If the current flowing through the internal MOSFET exceeds the short-circuit protection (SCP) threshold, SCP is triggered immediately. During start-up, SCP is blanked for 4096 cycles.

Thermal Shutdown (TSD)

To prevent damage due to thermal conditions, the MP183 shuts down when the junction temperature (T_J) exceeds the thermal shutdown (TSD) threshold.

Open-Loop Detection (OLD)

If V_{FB} falls below the open-loop detection (OLD) threshold (V_{OLD}), the MP183 stops switching, and a restart cycle begins. During SS, OLD is blanked.

Brown-In (B/I)

The MP183 has a B/I function by sampling V_{DS}. After the MP183 stops switching, it can only start to operate again once V_{DS} exceeds V_{DS_BI}.

B/I prevents switching after the device shuts down.

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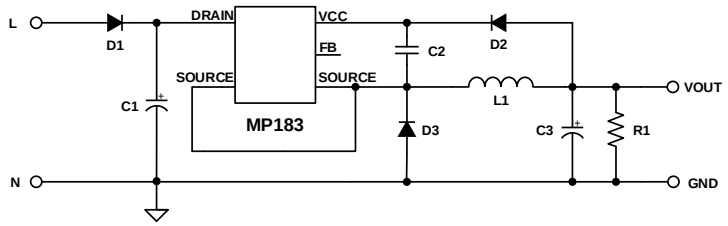
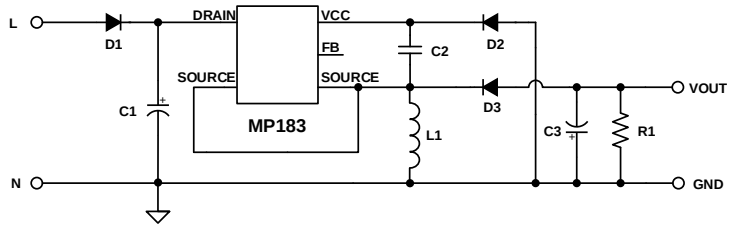
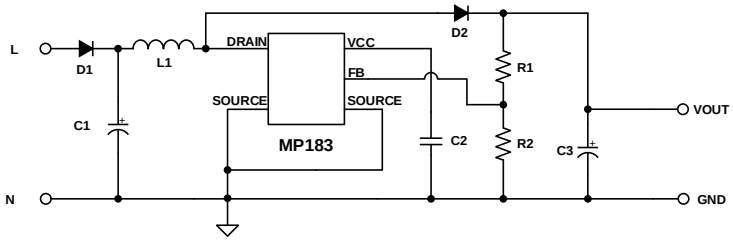
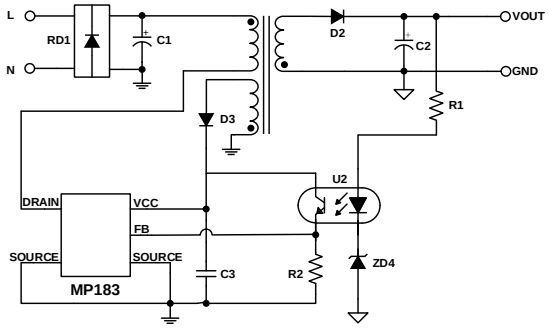
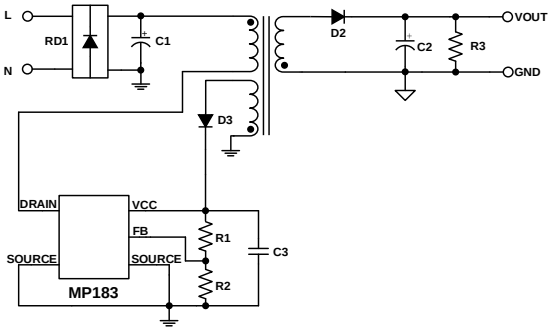
APPLICATION INFORMATION

Table 2 shows common topologies using the MP183.

Table 2: Common Topologies Using the MP183

Topology	Circuit Schematic	Features
High-side (HS) buck		• Non-isolation • Positive output • Low cost • Indirect feedback
HS buck-boost		• Non-isolation • Negative output • Low cost • Indirect feedback
Boost		• Non-isolation • Positive output • Low cost • Direct feedback
Flyback	 	• Isolation • Positive output • Low cost • Indirect feedback

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Topology Options

The MP183 is a green-mode, offline regulator with an integrated, 700V MOSFET. It provides accurate CV regulation without an optocoupler, and it can support buck, buck-boost, boost, and flyback topologies (see Table 2). Figure 2 on page 2 shows a typical application that is based on a typical buck application.

Selecting the Input Capacitor

The input capacitor (C1) supplies the DC input voltage (V_{IN}) for the converter. Figure 7 shows the typical DC bus voltage waveform of a half-wave rectifier.

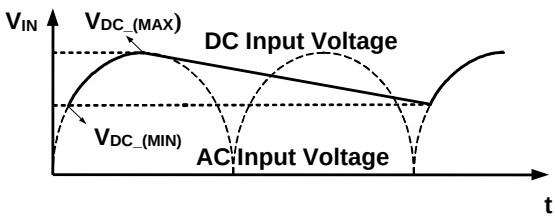

Figure 7: Input Voltage Waveform (Half-Wave Rectifier)

Figure 8 shows the waveform of a full-wave rectifier.

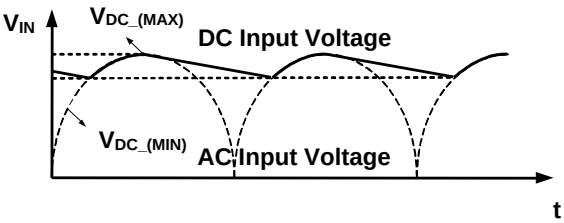

Figure 8: Input Voltage Waveform (Full-Wave Rectifier)

Typically, using a half-wave rectifier requires a C1 rated at 3µF/W for the universal input condition. When using a full-wave rectifier, C1 should be between 1.5µF/W and 2µF/W for the universal input condition. A half-wave rectifier is recommended for <2W output applications. A full-wave rectifier is recommended for >2W output applications.

Avoid using a C1 with an insufficient capacitance, as it may not maintain the DC voltage long enough. A low DC V_{IN} can lead to suboptimal thermal performance.

Selecting the Inductor

The MP183 has t_{OFF_MIN} and I_{LIMIT_PEAK} that determine the maximum output power (P_{OUT_MAX}). A smaller inductance may lead to insufficient P_{OUT}, but a larger inductance results in too high of an OLP threshold. The OLP threshold in CCM (P_{OUT_MAX}) can be estimated with Equation (5):

$$P_{OUT_MAX} = V_{OUT} \times (I_{LIMIT_PEAK} - \frac{V_{OUT} \times t_{OFF_MIN}}{2 \times L}) \quad (5)$$

The OLP threshold in DCM (P_{OUT_MAX}) can be estimated with Equation (6):

$$P_{OUT_MAX} = \frac{1}{2} \times L \times I_{LIMIT_PEAK}^{2} \times \frac{1}{t_{OFF_MIN}} \quad (6)$$

Typically, thermal performance is the final consideration when limiting P_{OUT} in application. For low-line V_{IN}, the internal MOSFET's RMS value decreases as I_{LIMIT} decreases. The RMS value drops slower as I_{LIMIT} drops, but the switching loss increases (especially under high-line V_{IN}).

To optimize thermal performance and ensure normal operation, it is not recommended to use a larger inductance to force the MP183 to operate in deep CCM.

Selecting the Freewheeling Diode

The freewheeling diode's reverse recovery affects the efficiency and circuit operation. Select a diode based on the maximum V_{IN} and maximum I_{LIMIT}. For DCM, it is recommended to select a diode with a <75ns recovery time. For CCM, select an ultrafast diode with a <35ns recovery time.

Selecting the Output Capacitor

The output capacitor (C3) is required to maintain the DC V_{OUT}. The V_{OUT} ripple (V_{OUT_RIPPLE}) during CCM can be calculated with Equation (7):

$$V_{OUT_RIPPLE} = \frac{\Delta i}{8 \times f_{SW} \times C3} + \Delta i \times R_{ESR} \quad (7)$$

V_{OUT_RIPPLE} during DCM can be calculated with Equation (8):

$$V_{OUT_RIPPLE} = \frac{I_{OUT}}{f_{SW} \times C3} \times (\frac{I_{LIMIT} - I_{OUT}}{I_{LIMIT}})^2 + I_{LIMIT} \times R_{ESR} \quad (8)$$

If required, it is recommended to use low-ESR electrolytic or ceramic capacitors to reduce V_{OUT_RIPPLE}.

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Selecting the External Feedback Resistors

It is recommended to use a <50kΩ resistor to override the internal feedback for configurations with an adjustable V_{OUT}.

For normal start-up, avoid using too low of a resistance when adopting a VCC feedback structure.

Selecting the Feedback Capacitor

The feedback capacitor provides a sample and hold function. For both fixed and adjustable V_{OUT} set-ups, VCC can be used as the feedback capacitor (see Figure 9).

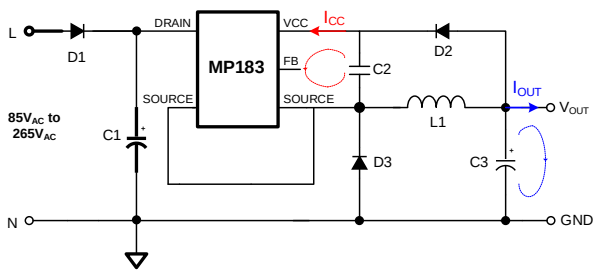

Figure 9: Typical Buck Application Circuit

A higher VCC capacitance is recommended because it results in minimal no-load consumption and excellent light-load regulation. It also helps increase the hiccup duration during protections. However, stability may be affected when the feedback capacitance is too large. The feedback capacitor (C2) should meet the requirements below, which can be estimated with Equation (9):

$$\frac{I_{CC} \times C3}{2 \times I_{OUT}} < C2 < \frac{I_{CC} \times C3}{I_{OUT}} \quad (9)$$

Dummy Load

The MP183's switching under no-load conditions is determined by the feedback RC discharging rate. It delivers a certain amount of power, and a dummy load is required to dissipate this power and regulate V_{OUT}.

A large dummy load current improves regulation, but increases power consumption under no-load conditions. There is a tradeoff between no-load consumption and no-load regulation.

Burst Set-Up

Since burst mode induces a certain ripple, it is important to select external devices that limit the output within an appropriate range. Ensure there is a hysteresis that prevents a repeated burst-in and burst-out condition. Select C2, C3, and the power inductor (L1) following certain guidelines, which are described in greater detail below.

Selecting the Feedback Capacitor (C2)

It is standard to make the switch-off period longer than 2ms to indicate a safe, noiseless state under light-load conditions. C2 can be calculated with Equation (10):

$$C2 \geq \frac{V_{REF} \times I_{CC} \times 2ms}{(V_{FBH} - V_{FBL}) \times V_{OUT}} \quad (10)$$

Typically, it is recommended to use a ≥1μF capacitor.

Selecting the Output Capacitor (C3)

Figure 10 shows how to define the output currents (I_{OUT1}, I_{OUT2}, and I_{OUT3}) for C3 selection. The MP183 limits the frequency at f_{SW_MIN}. Once f_{SW_MIN} is reached, the system enters burst mode by slightly decreasing the load. In this scenario, the system transfers energy with a fixed I_{LIMIT} and fixed frequency during the switch-on period.

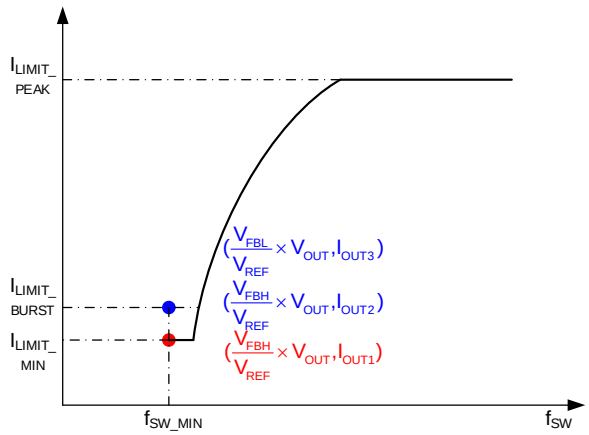

Figure 10: Power Transfer during Burst Mode

When the load drops to I_{OUT1}, the MP183 starts to operate in burst mode. The MP183 recovers from this hiccup operation when V_{FB} drops to V_{FBL_FAST}. The MP183 also recovers if V_{FB} drops below V_{FBL} for 40 continuous cycles, and t_1 reaches about 2ms (t_R) (see Figure 11 on page 19).

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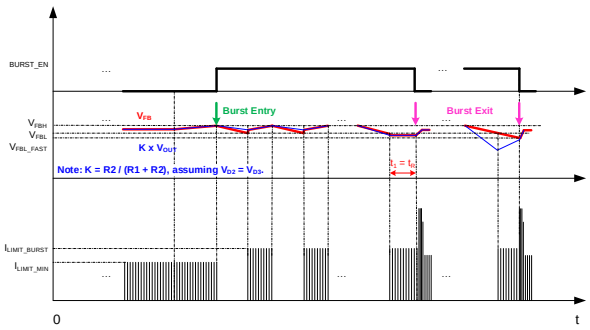

Figure 11: Burst Entry and Exit

Typically, V_{OUT_RIPPLE} is limited within the inherent range of the control scheme. The output circuit's RC discharge rate should not be faster than the feedback rate before the load reaches I_{OUT2}. C3 can be estimated with Equation (11):

$$C3 \geq \frac{C2}{I_{CC}} \times I_{OUT2} \quad (11)$$

In this scenario, the system does not enter burst mode until the load drops to I_{OUT1}. The system stays in burst mode until the load rises to I_{OUT3}. The load hysteresis is (I_{OUT3} - I_{OUT1}), and the worst-case condition for V_{OUT_RIPPLE} occurs at I_{OUT2}. V_{OUT_RIPPLE} can be calculated with Equation (12):

$$V_{OUT_RIPPLE} \leq V_{OUT} \times \left(\frac{V_{FBH} - V_{FBL}}{V_{REF}}\right) \quad (12)$$

Note that if the load exceeds I_{OUT2}, V_{FB} can no longer reach V_{FBH}. This state does not end until the load exceeds I_{OUT3}. At this point, V_{FB} reaches V_{FBL}, and the traditional feedback loop takes control. Although V_{OUT_RIPPLE} is reduced between I_{OUT2} and I_{OUT3} due to the continuous pulses, V_{OUT} is regulated down. The minimum V_{OUT} (V_{OUT_MIN}) occurs at I_{OUT3}, which can be estimated with Equation (13):

$$V_{OUT_MIN} = V_{OUT} \times \left(\frac{V_{FBL}}{V_{REF}}\right) \quad (13)$$

Selecting the Power Inductor (L1)

It is not recommended to use a smaller inductance when considering the LEB limitation. I_{LIMIT} at light loads is determined by t_{LEB1} and the external inductor (rather than the internal reference). In this scenario, the burst behavior and other performances may be affected. L1 can be calculated with Equation (14):

$$L1 \geq \frac{(V_{IN_MAX} - V_{OUT}) \times t_{LEB1}}{I_{LIMIT_MIN}} \quad (14)$$

Surge Performance

The input capacitor and filter can be used for surge suppression. If an ideal input circuit is chosen, the MP183 may pass the low-level surge test without any other surge suppression components.

Figure 12 shows the typical half-wave rectifier used in low-power, offline applications.

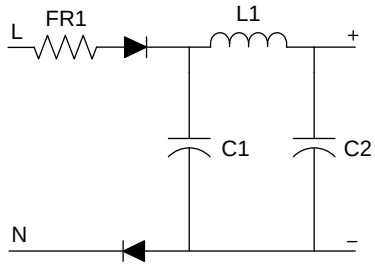

Figure 12: Half-Wave Rectifier

Table 3 shows the capacitance that the MP183 requires under normal conditions for different surge levels. FR1 is a 20Ω/2W fusible resistor, and L1 is 1mH.

Table 3: Recommended Capacitance

Surge Voltage	500V	1000V	2000V
C1	1μF	2.2μF	3.3μF
C2	1μF	2.2μF	3.3μF

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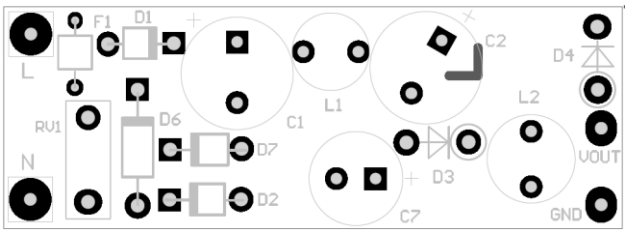
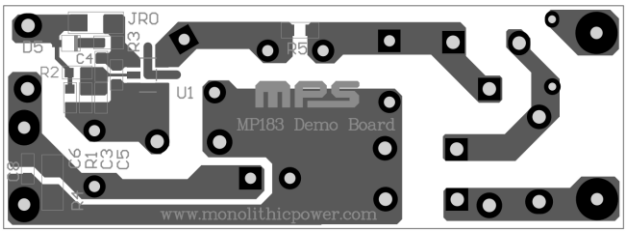
PCB Layout Guidelines

PCB layout is critical for stable operation, as well as excellent EMI and thermal performance. For the best performance, refer to Figure 13 and follow the guidelines below:

1. Minimize the loop area formed by the input capacitor, the MP183's internal MOSFET, the freewheeling diode, the inductor, and the output capacitor.
2. Place the power inductor far away from the input filter while keeping the loop area small.
3. Keep the AC input loop as small as possible to prevent noise coupling.
4. Place a bypass capacitor between the FB and GND pins, and as close to the IC as possible.
5. Connect a large copper area to the DRAIN pin to improve thermal performance.



Top Layer



Bottom Layer

Figure 13: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

Figure 14 shows a typical application example of a 12V, 250mA, non-isolated power supply using the MP183.

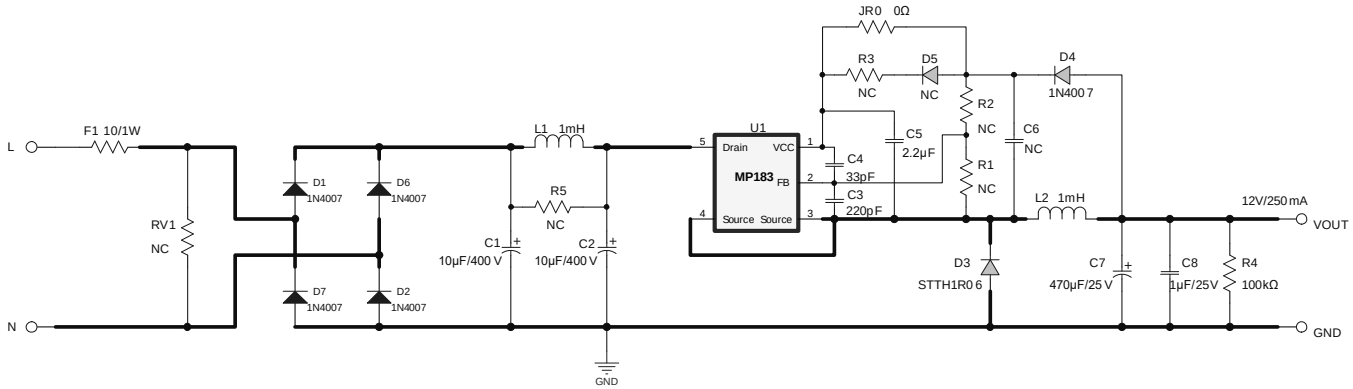

Figure 14: Typical Application Circuit (12V, 250mA)

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PACKAGE INFORMATION

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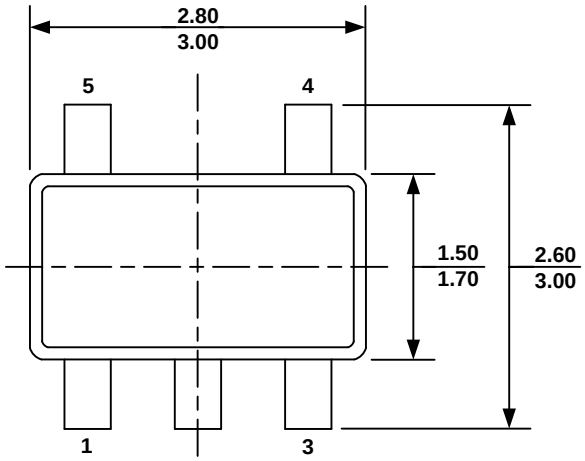
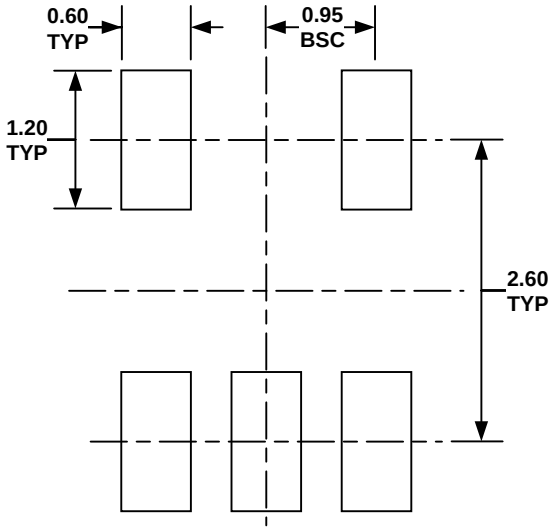
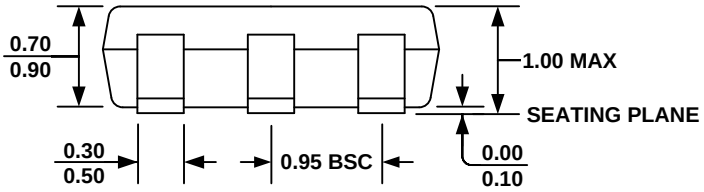


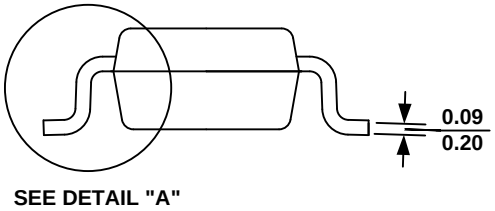
TOP VIEW



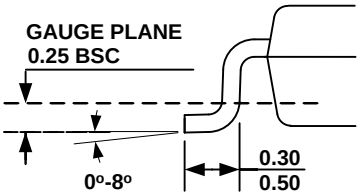
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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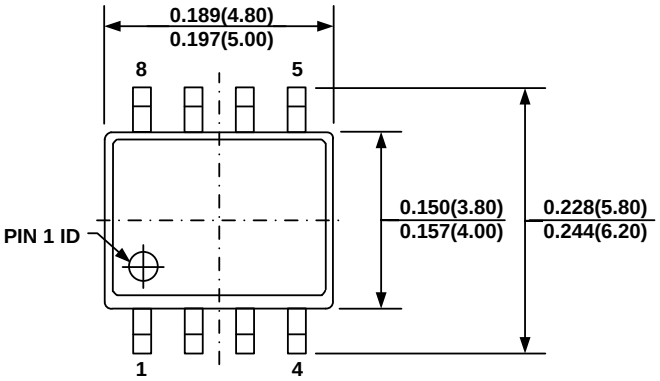
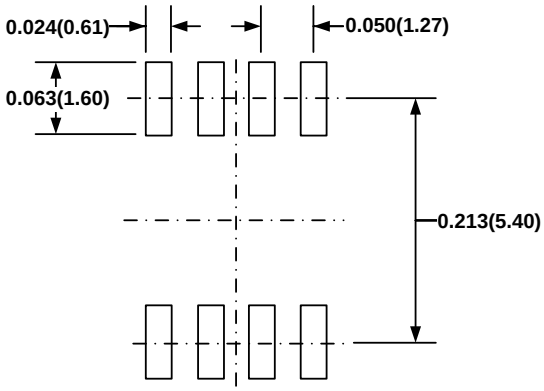
PACKAGE INFORMATION *(continued)*

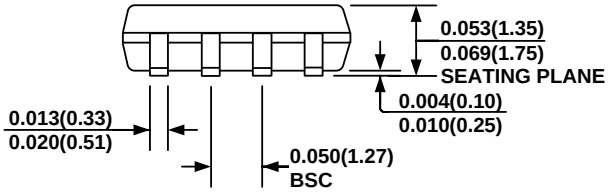
SOIC-8



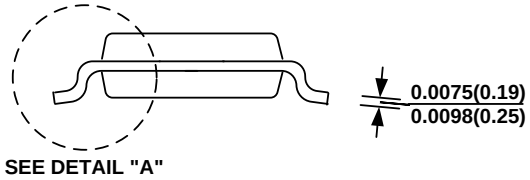
TOP VIEW



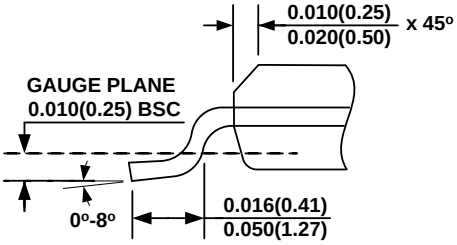
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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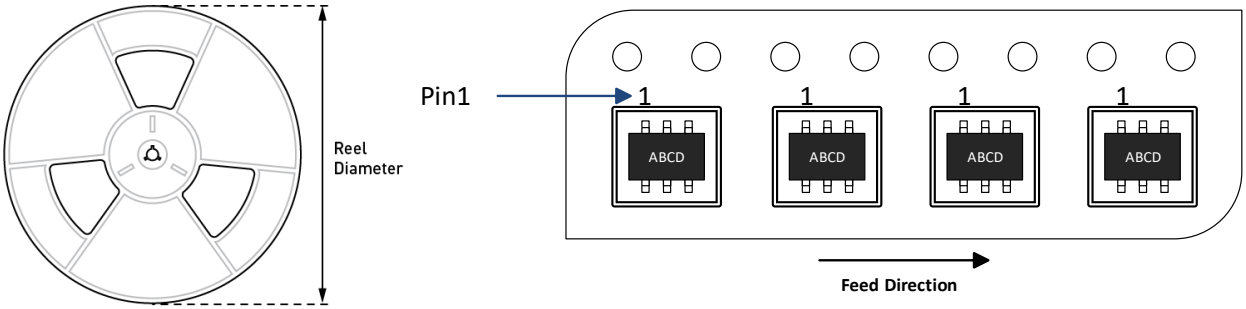
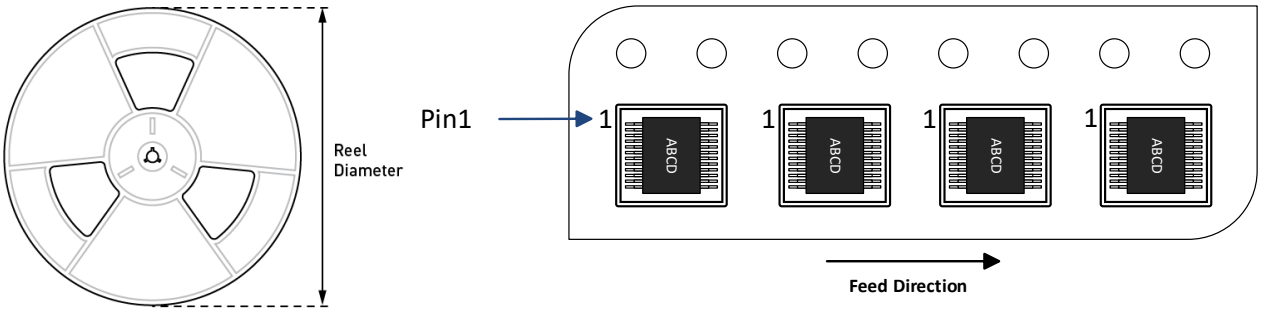
CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP183GJ -Z	TSOT23-5	3000	N/A	N/A	7in	8mm	4mm



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP183GS -Z	SOIC-8	2500	100	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/22/2023	Initial Release	-

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