

## DESCRIPTION

The MP18021 is a high frequency, 100V half bridge N-channel power MOSFET driver. Its low side and high side driver channels are independently controlled and matched with less than 5ns in time delay. Under voltage lock-out on both high side and low side supplies force their outputs low in case of insufficient supply. The integrated bootstrap diode reduces external component count.

## FEATURES

- Drives N-channel MOSFET half bridge
- 100V  $V_{BST}$  voltage range
- On-chip bootstrap diode
- Typical 16ns propagation delay time
- Less than 5ns gate drive matching
- Drive 1nF load with 12ns/9ns rise/fall times with 12V VDD
- TTL compatible input
- Less than 150 $\mu$ A quiescent current
- UVLO for both high side and low side
- In SOIC8 EPAD and 3 $\times$ 3mm QFN8 Packages

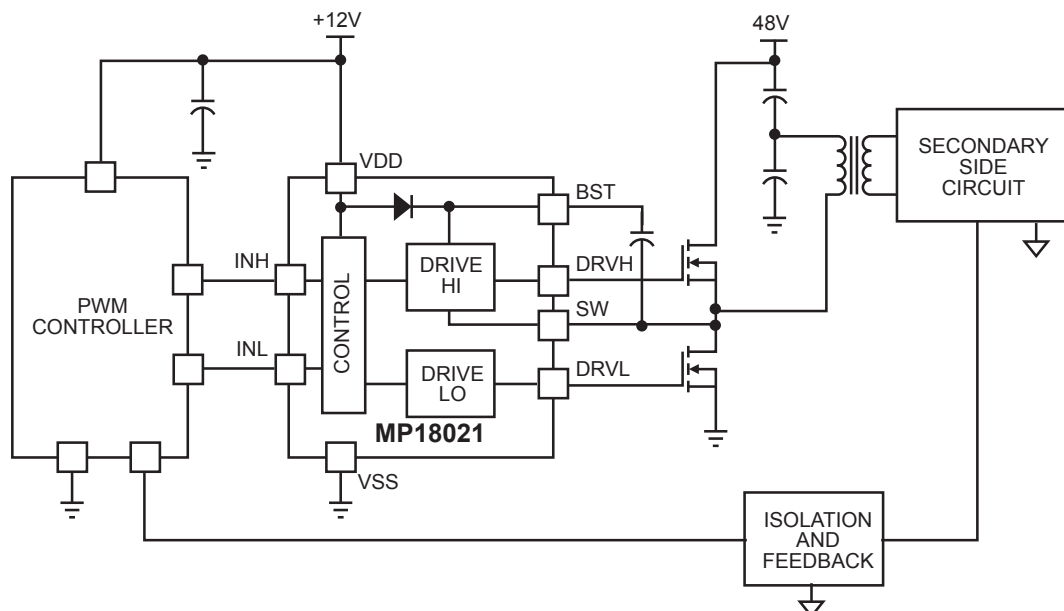
## APPLICATIONS

- Telecom half bridge power supplies
- Avionics DC-DC converters
- Two-switch forward converters
- Active clamp forward converters

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

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## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package       | Top Marking | Free Air Temperature (T <sub>A</sub> ) |
|--------------|---------------|-------------|----------------------------------------|
| MP18021HN    | SOIC8EP       | MP18021HN   | -40°C to +125°C                        |
| MP18021HQ    | QFN8 (3x 3mm) | ABN         | -40°C to +125°C                        |

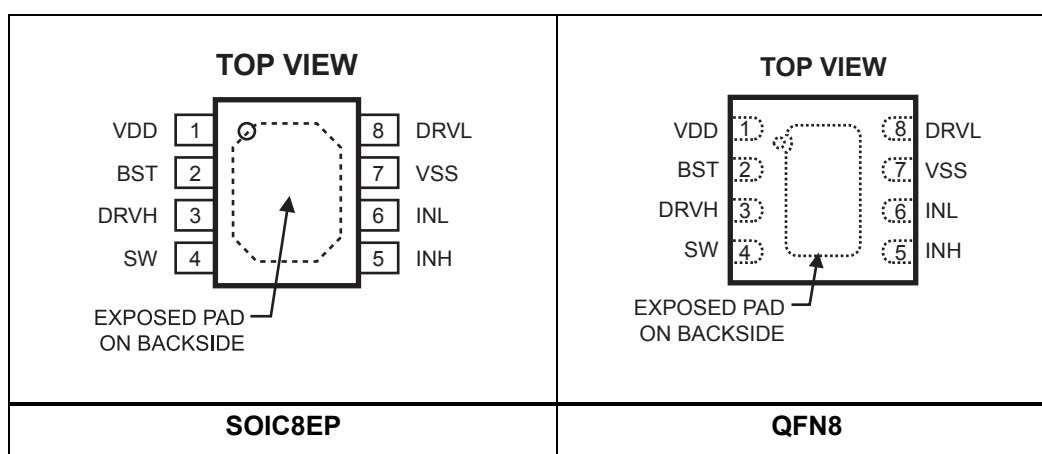
\* For Tape & Reel, add suffix -Z (e.g. MP18021HN-Z);

For RoHS compliant packaging, add suffix -LF; (e.g. MP18021HN-LF-Z)

For Tape & Reel, add suffix -Z (e.g. MP18021HQ-Z);

For RoHS compliant packaging, add suffix -LF; (e.g. MP18021HQ-LF-Z)

## PACKAGE REFERENCE



## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                      |                                  |
|----------------------------------------------------------------------|----------------------------------|
| Supply Voltage (V <sub>DD</sub> )                                    | -0.3V to +18V                    |
| SW Voltage (V <sub>SW</sub> )                                        | -5.0V to 100V                    |
| BST Voltage (V <sub>BST</sub> )                                      | -0.3V to 100V                    |
| BST to SW                                                            | -0.3V to +18V                    |
| DRVH to SW                                                           | -0.3V to +18V                    |
| All Other Pins                                                       | -0.3V to (V <sub>DD</sub> +0.3V) |
| Continuous Power Dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup> |                                  |
| SOIC8 (Exposed Pad)                                                  | 2.6W                             |
| QFN8 (3x3)                                                           | 2.5W                             |
| Junction Temperature                                                 | 150°C                            |
| Lead Temperature                                                     | 260°C                            |
| Storage Temperature                                                  | -65°C to +150°C                  |

## Recommended Operating Conditions <sup>(3)</sup>

|                                         |                               |
|-----------------------------------------|-------------------------------|
| Supply Voltage V <sub>DD</sub>          | +9.0V to 16.0V                |
| SW Voltage (V <sub>SW</sub> )           | -1.0V to 100V-V <sub>DD</sub> |
| SW slew rate                            | <50V/nsec                     |
| Operating Junct. Temp (T <sub>J</sub> ) | -40°C to +125°C               |

## Thermal Resistance <sup>(4)</sup>

|                     | θ <sub>JA</sub> | θ <sub>JC</sub> |
|---------------------|-----------------|-----------------|
| SOIC8 (Exposed Pad) | 48              | 10              |
| QFN8 (3x3)          | 50              | 12              |

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub>(MAX)=(T<sub>J</sub>(MAX)-T<sub>A</sub>)/θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{BST} - V_{SW} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ , No load at DRVH and DRVL,  $T_A = +25^\circ C$ , unless otherwise noted.

| Parameter                             | Symbol            | Condition                                              | Min | Typ  | Max  | Units |
|---------------------------------------|-------------------|--------------------------------------------------------|-----|------|------|-------|
| Supply Currents                       |                   |                                                        |     |      |      |       |
| VDD quiescent current                 | I <sub>DDQ</sub>  | INL=INH=0                                              |     | 100  | 150  | μA    |
| VDD operating current                 | I <sub>DDO</sub>  | fsw=500kHz                                             |     | 2.8  | 3.5  | mA    |
| Floating driver quiescent current     | I <sub>BSTQ</sub> | INL=INH=0                                              |     | 60   | 90   | μA    |
| Floating driver operating current     | I <sub>BSTO</sub> | fsw=500kHz                                             |     | 2.1  | 3    | mA    |
| Leakage Current                       | I <sub>LK</sub>   | BST=SW=100V                                            |     | 0.05 | 1    | μA    |
| Inputs                                |                   |                                                        |     |      |      |       |
| INL/INH High                          |                   |                                                        |     | 2    | 2.4  | V     |
| INL/INH Low                           |                   |                                                        | 1   | 1.4  |      | V     |
| INL/INH internal pull-down resistance | R <sub>IN</sub>   |                                                        |     | 185  |      | kΩ    |
| Under Voltage Protection              |                   |                                                        |     |      |      |       |
| VDD rising threshold                  | V <sub>DDR</sub>  |                                                        | 7.7 | 8.1  | 8.5  | V     |
| VDD hysteresis                        | V <sub>DDH</sub>  |                                                        |     | 0.5  |      | V     |
| (BST-SW) rising threshold             | V <sub>BSTR</sub> |                                                        | 6.7 | 7.1  | 7.5  | V     |
| (BST-SW) hysteresis                   | V <sub>BSTH</sub> |                                                        |     | 0.55 |      | V     |
| Bootstrap Diode                       |                   |                                                        |     |      |      |       |
| Bootstrap diode VF @ 100uA            | V <sub>F1</sub>   |                                                        |     | 0.5  |      | V     |
| Bootstrap diode VF @ 100mA            | V <sub>F2</sub>   |                                                        |     | 0.9  |      | V     |
| Bootstrap diode dynamic R             | R <sub>D</sub>    | @ 100mA                                                |     | 2.5  |      | Ω     |
| Low Side Gate Driver                  |                   |                                                        |     |      |      |       |
| Low level output voltage              | V <sub>OLL</sub>  | I <sub>O</sub> =100mA                                  |     | 0.15 | 0.22 | V     |
| High level output voltage to rail     | V <sub>OHL</sub>  | I <sub>O</sub> =-100mA                                 |     | 0.45 | 0.6  | V     |
| Peak pull-up current                  | I <sub>OHL</sub>  | V <sub>DRV<sub>L</sub></sub> =0V, V <sub>DD</sub> =12V |     | 1.5  |      | A     |
|                                       |                   | V <sub>DRV<sub>L</sub></sub> =0V, V <sub>DD</sub> =16V |     | 2.5  |      | A     |
| Peak pull-down current                | I <sub>OLL</sub>  | V <sub>DRV<sub>L</sub></sub> =V <sub>DD</sub> =12V     |     | 2.5  |      | A     |
|                                       |                   | V <sub>DRV<sub>L</sub></sub> =V <sub>DD</sub> =16V     |     | 3.5  |      | A     |
| Floating Gate Driver                  |                   |                                                        |     |      |      |       |
| Low level output voltage              | V <sub>OLH</sub>  | I <sub>O</sub> =100mA                                  |     | 0.15 | 0.22 | V     |
| High level output voltage to rail     | V <sub>OHH</sub>  | I <sub>O</sub> =-100mA                                 |     | 0.45 | 0.6  | V     |
| Peak pull-up current                  | I <sub>OHH</sub>  | V <sub>DRV<sub>H</sub></sub> =0V, V <sub>DD</sub> =12V |     | 1.5  |      | A     |
|                                       |                   | V <sub>DRV<sub>H</sub></sub> =0V, V <sub>DD</sub> =16V |     | 2.5  |      | A     |
| Peak pull-down current                | I <sub>OLH</sub>  | V <sub>DRV<sub>H</sub></sub> =V <sub>DD</sub> =12V     |     | 2.5  |      | A     |
|                                       |                   | V <sub>DRV<sub>H</sub></sub> =V <sub>DD</sub> =16V     |     | 3.5  |      | A     |

# ELECTRICAL CHARACTERISTICS *(continued)*

$V_{DD} = V_{BST} - V_{SW} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ , No load at DRVH and DRVL,  $T_A = +25^{\circ}C$ , unless otherwise noted.

| Parameter                                                 | Symbol     | Condition   | Min | Typ        | Max        | Units       |
|-----------------------------------------------------------|------------|-------------|-----|------------|------------|-------------|
| <b>Switching Spec. --- Low Side Gate Driver</b>           |            |             |     |            |            |             |
| Turn-off propagation delay<br>INL falling to DRVL falling | $T_{DLFF}$ |             |     | 16         |            | ns          |
| Turn-on propagation delay<br>INL rising to DRVL rising    | $T_{DLRR}$ |             |     | 16         |            |             |
| DRVL rise time                                            |            | $C_L = 1nF$ |     | 12         |            | ns          |
| DRVL fall time                                            |            | $C_L = 1nF$ |     | 9          |            | ns          |
| <b>Switching Spec. --- Floating Gate Driver</b>           |            |             |     |            |            |             |
| Turn-off propagation delay<br>INL falling to DRVH falling | $T_{DHFF}$ |             |     | 16         |            | ns          |
| Turn-on propagation delay<br>INL rising to DRVH rising    | $T_{DHRR}$ |             |     | 16         |            | ns          |
| DRVH rise time                                            |            | $C_L = 1nF$ |     | 12         |            | ns          |
| DRVH fall time                                            |            | $C_L = 1nF$ |     | 9          |            | ns          |
| <b>Switching Spec. --- Matching</b>                       |            |             |     |            |            |             |
| Floating driver turn-off to low<br>side drive turn-on     | $T_{MON}$  |             |     | 1          | 5          | ns          |
| Low side driver turn-off to floating<br>driver turn-on    | $T_{MOFF}$ |             |     | 1          | 5          | ns          |
| Minimum input pulse width that<br>changes the output      | $T_{PW}$   |             |     |            | $50^{(5)}$ | ns          |
| Bootstrap diode turn-on or turn-<br>off time              | $T_{BS}$   |             |     | $10^{(5)}$ |            | ns          |
| <b>Over Temperature Protection<sup>(5)</sup></b>          |            |             |     |            |            |             |
| OTP entry threshold                                       |            |             |     | 160        |            | $^{\circ}C$ |
| OTP recovery threshold                                    |            |             |     | 140        |            |             |
| OTP hysteresis                                            |            |             |     | 20         |            |             |

**Note:**

5) Derived from bench characterization. Not tested in production.

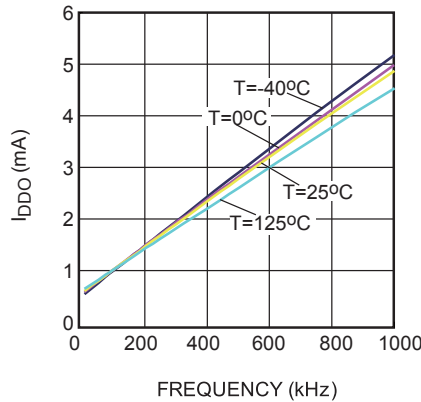
## PIN FUNCTIONS

| Pin # | Name                   | Description                                                                                                                                                               |
|-------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | VDD                    | Supply input. This pin supplies power to all the internal circuitry. A decoupling capacitor to ground must be placed close to this pin to ensure stable and clean supply. |
| 2     | BST                    | Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.                   |
| 3     | DRVH                   | Floating driver output.                                                                                                                                                   |
| 4     | SW                     | Switching node.                                                                                                                                                           |
| 5     | INH                    | Control signal input for the floating driver.                                                                                                                             |
| 6     | INL                    | Control signal input for the low side driver.                                                                                                                             |
| 7     | VSS,<br>Exposed<br>Pad | Chip ground. Connect to Exposed pad to VSS for proper thermal operation.                                                                                                  |
| 8     | DRVL                   | Low side driver output.                                                                                                                                                   |

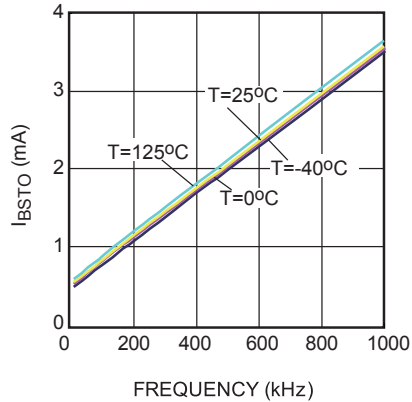
# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

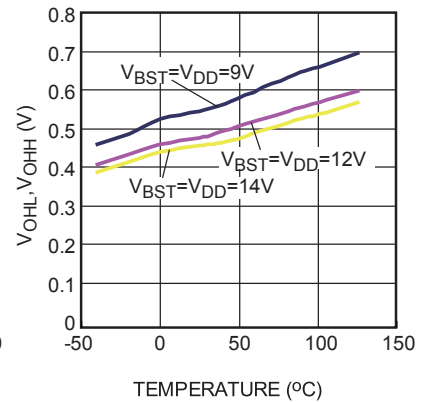
**$I_{DDO}$  Operation Current vs. Frequency**



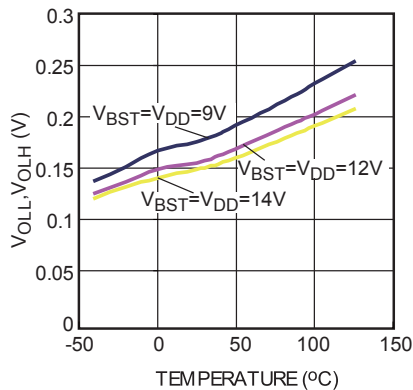
**$I_{BSTO}$  Operation Current vs. Frequency**



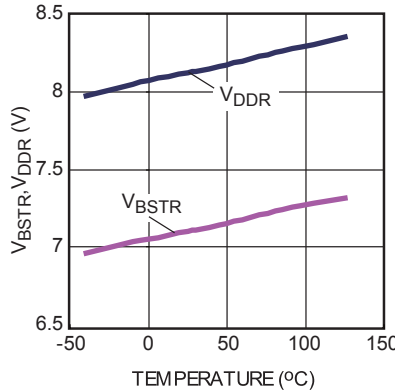
**High Level Output Voltage vs. Temperature**



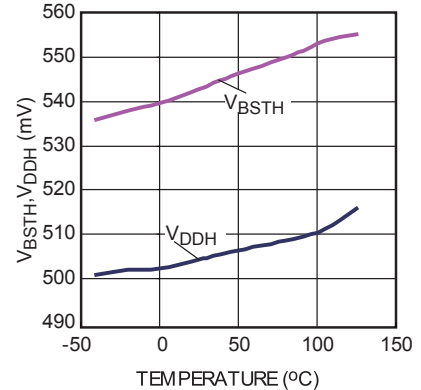
**Low Level Output Voltage vs. Temperature**



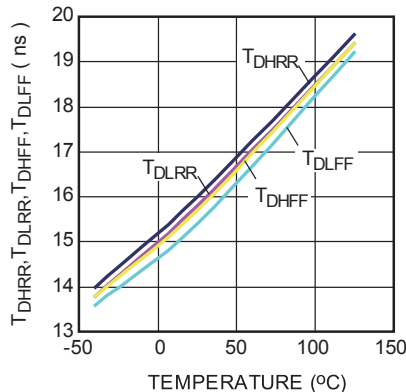
**Undervoltage Lockout Threshold vs. Temperature**



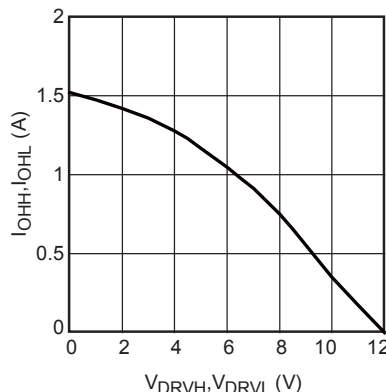
**Undervoltage Lockout Hysteresis vs. Temperature**



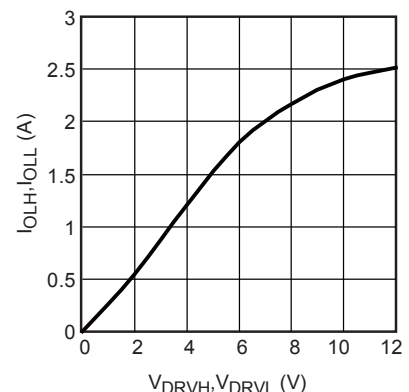
**Propagation Delay vs. Temperature**



**Peak Pull-up Current vs. Output Voltage**



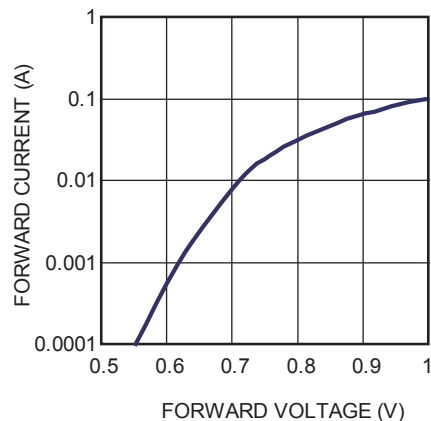
**Peak Pull-down Current vs. Output Voltage**



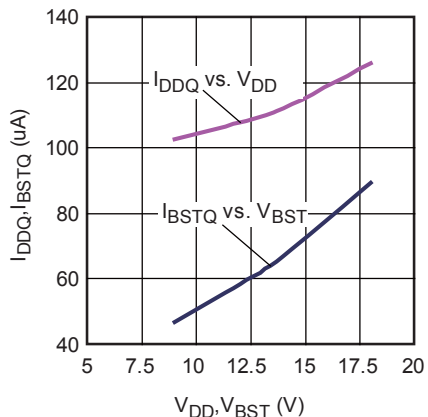
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

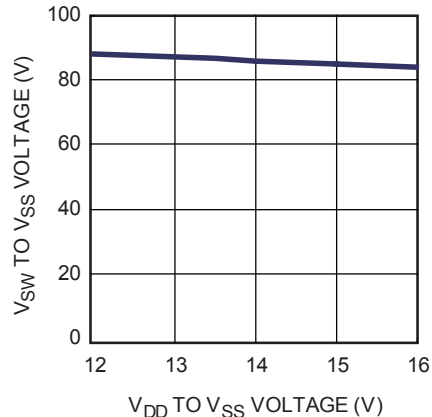
**Bootstrap Diode I-V Characteristics**



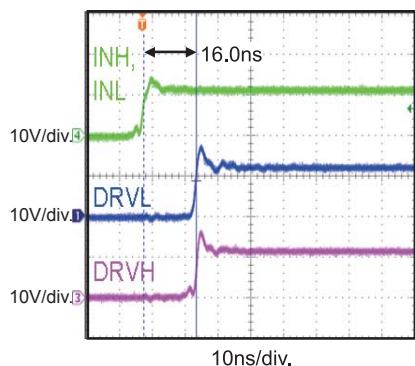
**Quiescent Current vs. Voltage**



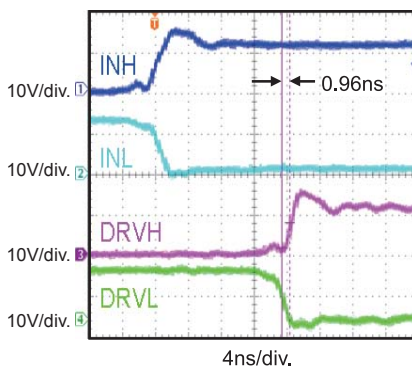
**Maximum  $V_{SW}$  Voltage vs.  $V_{DD}$  Voltage**



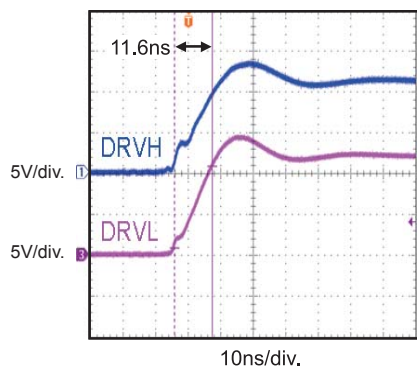
**Turn-on Propagation Delay**



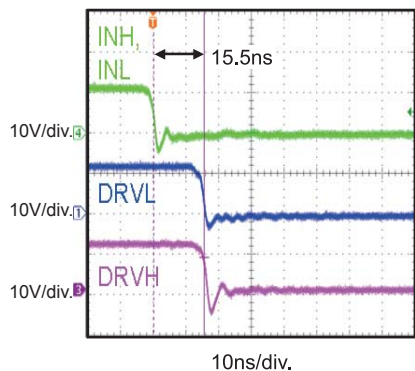
**Gate Drive Matching  $T_{MOFF}$**



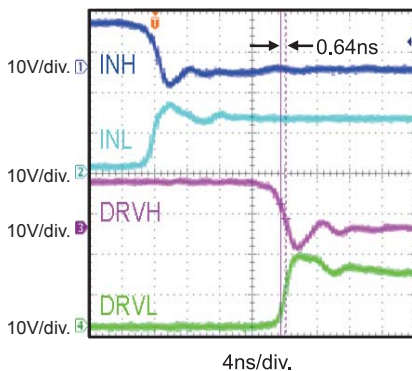
**Drive Rise Time (1nF Load)**



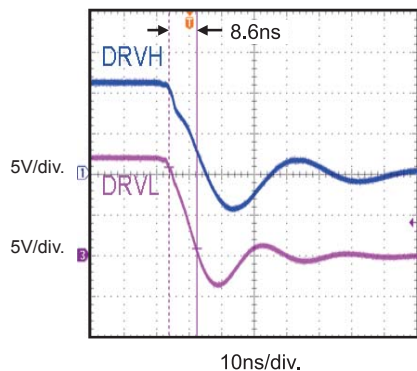
**Turn-off Propagation Delay**



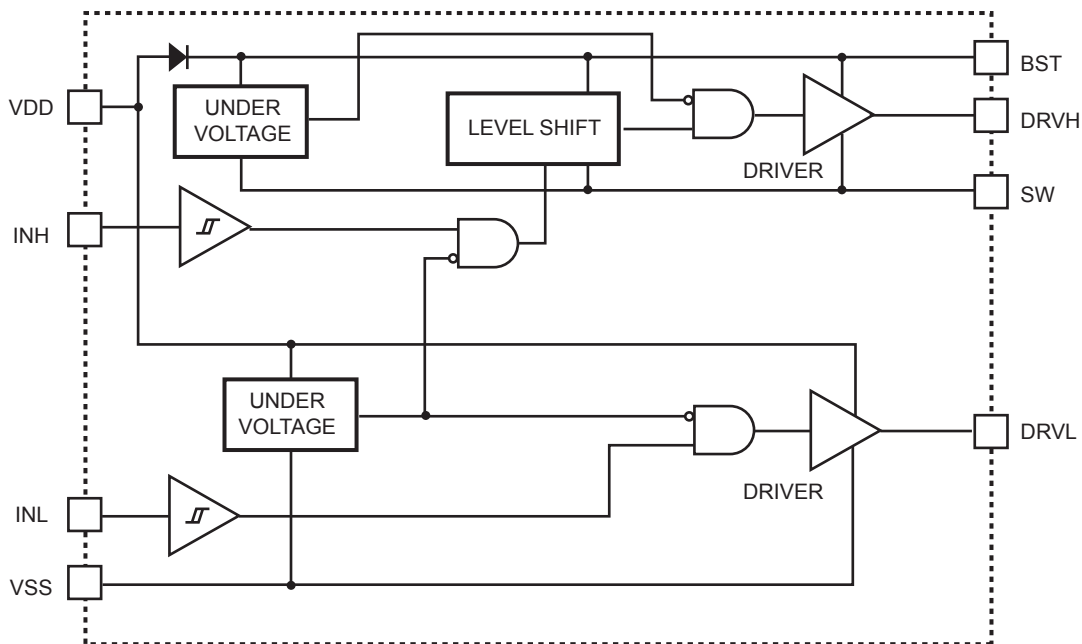
**Gate Drive Matching  $T_{MON}$**



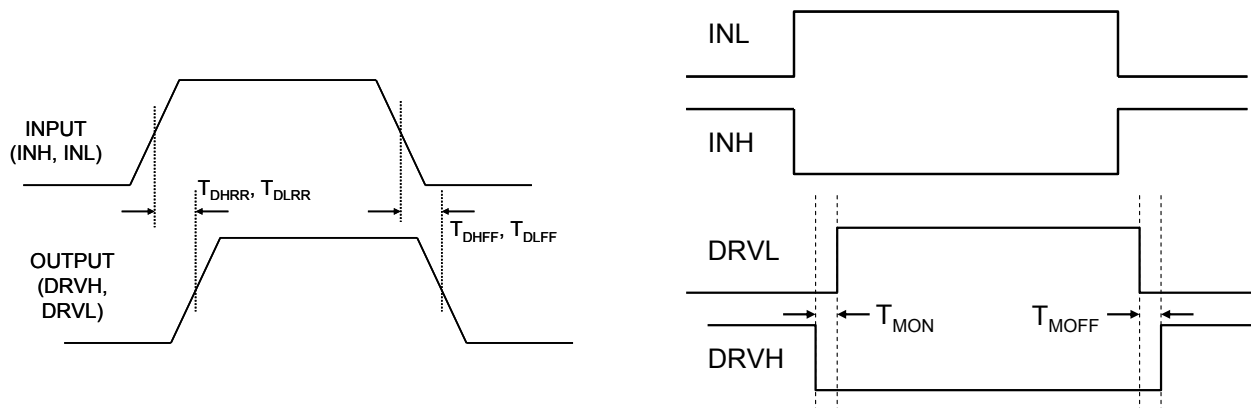
**Drive Fall Time (1nF Load)**



## BLOCK DIAGRAM



**Figure 1—Function Block Diagram**

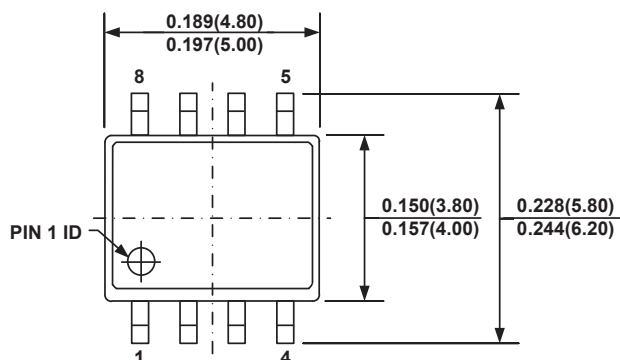


**Figure 2—Timing Diagram**

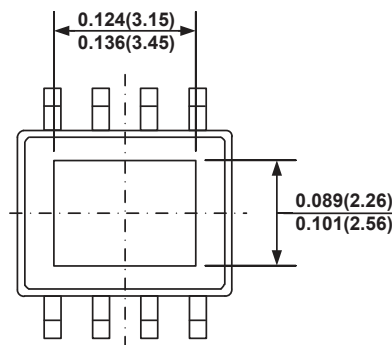


# PACKAGE INFORMATION

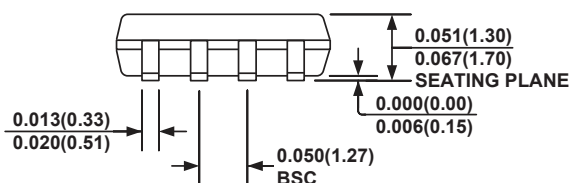
## SOIC8 (EXPOSED PAD)



TOP VIEW

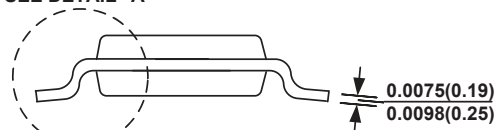


BOTTOM VIEW

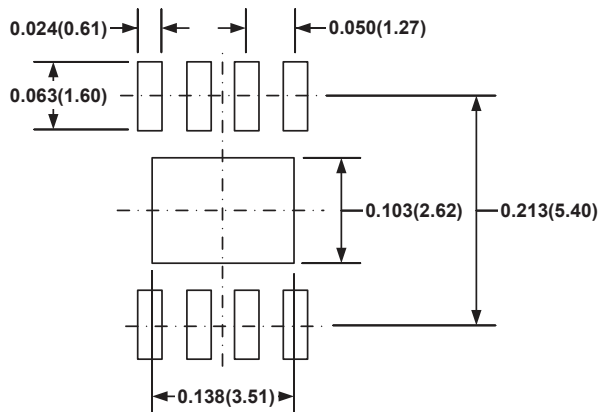


FRONT VIEW

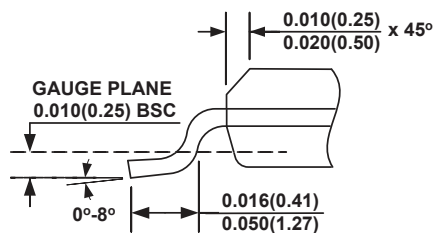
SEE DETAIL "A"



SIDE VIEW



RECOMMENDED LAND PATTERN

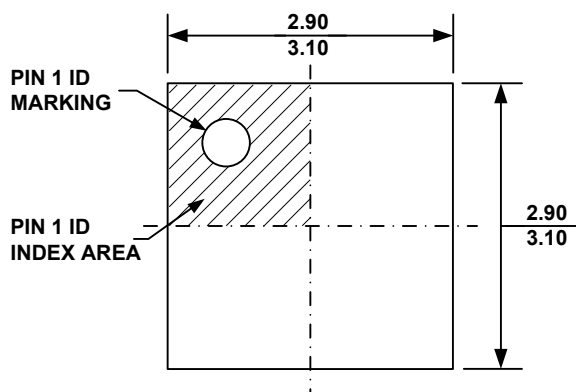


DETAIL "A"

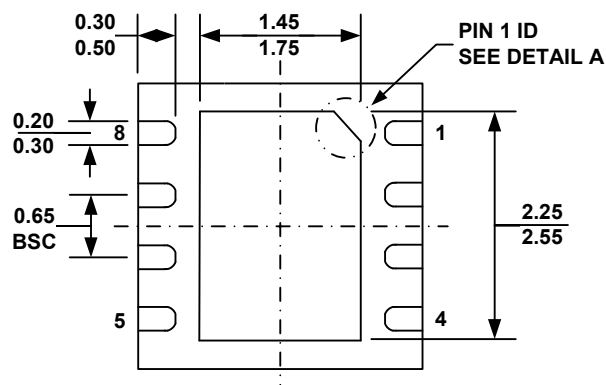
### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

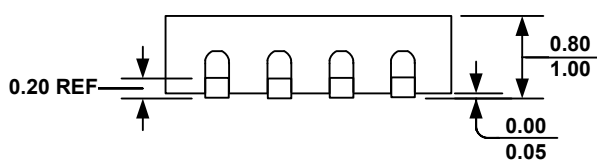
**QFN8 (3mm×3mm)**



**TOP VIEW**

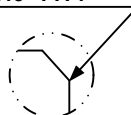


**BOTTOM VIEW**

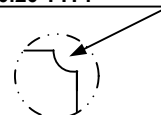


**SIDE VIEW**

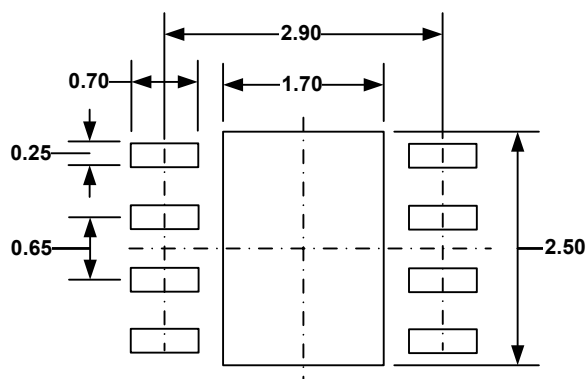
**PIN 1 ID OPTION A**  
0.30x45° TYP.



**PIN 1 ID OPTION B**  
R0.20 TYP.



**DETAIL A**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEEC-2.
- 5) DRAWING IS NOT TO SCALE.

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