MP175L

700V, Non-Isolated, Offline Regulator with Up to 600mA Output Current and Brown-In Protection

DESCRIPTION

The MP175L is a primary-side regulator that provides accurate constant-voltage (CV) regulation without an optocoupler. The MP175L supports buck, buck-boost, boost, and flyback topologies. The MP175L has an integrated 700V MOSFET and high-voltage current source to simplify the structure and reduce costs.

The MP175L is a green-mode operation regulator. Both the peak current limit (I_{LIMIT}) and switching frequency (f_{SW}) decrease with decreasing load. This feature provides excellent efficiency under light-load conditions and improves the overall average efficiency.

The MP175L has multiple protection features, including over-temperature protection (OTP), VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), brown-in protection, and open-loop detection (OLD).

These features make the MP175L an ideal regulator for offline, low-power applications, such as home appliances and standby power.

The MP175L is available in an SOIC-8 package.

FEATURES

- Primary-Side Constant Voltage (CV) Control, Supporting Buck, Buck-Boost, Boost, and Flyback Topologies
- Integrated 700V/4.5Ω MOSFET
- Internal 700V High-Voltage Current Source
- <30mW No-Load Power Consumption
- Up to 9W Output Power (P_{OUT})
- Maximum Continuous Conduction Mode (CCM) with an Output Current (I_{OUT}) Up to 600mA
- Low VCC Operating Current
- Frequency Foldback
- Limited Maximum Frequency
- Peak-Current Compression
- Internally Biased VCC
- Over-Temperature Protection (OTP), Under-Voltage Lockout (UVLO), Overload Protection (OLP), Short-Circuit Protection (SCP), Open-Loop Detection (OLD), and Brown-In Protection
- Available in an SOIC-8 Package

APPLICATIONS

- Home Appliances, White Goods, and Consumer Electronics
- Industrial Controls
- Standby Power

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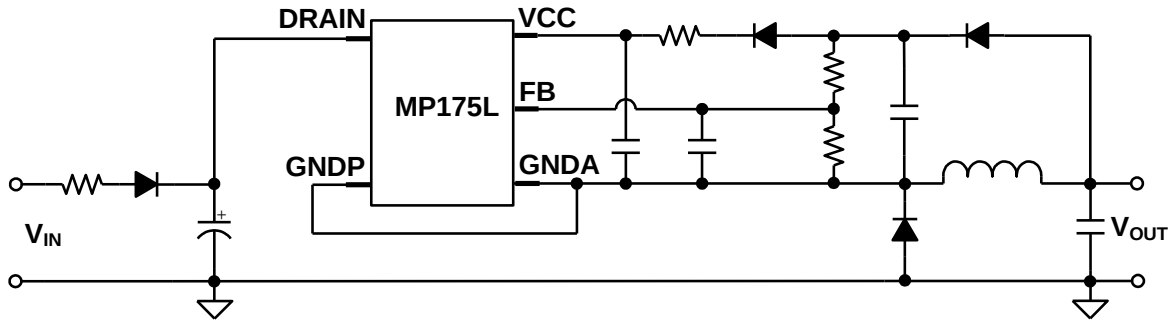
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP175LGS	SOIC-8	*See Below*	2

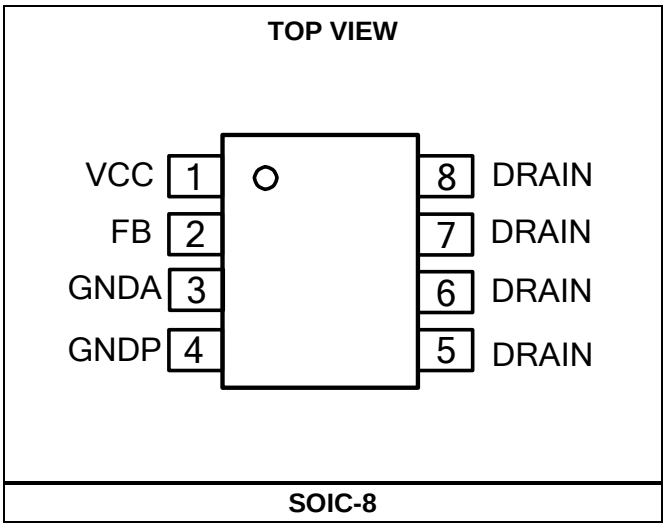
* For Tape & Reel, add suffix -Z (e.g. MP175LGS-Z).

TOP MARKING

MP175L
LLLLLLLL
MPSYWW

MP175L: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**Control circuit power supply.**
2	FB	**Regulator feedback.**
3	GNDA	**Short to GNDP in the application.**
4	GNDP	**IC power ground.**
5, 6, 7, 8	DRAIN	**Internal power MOSFET drain.** DRAIN is the high-voltage current source regulator input.

ABSOLUTE MAXIMUM RATINGS (1)

DRAIN to GND..... -0.3V to +700V
VCC to GND ..... -0.3V to +30V
FB to GND ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8 .....1.64W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-60°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM).....2kV

Recommended Operating Conditions (3)

Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8..... 76.....35..... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 12V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-Voltage Current Source and Internal MOSFET (DRAIN)						
Internal current-source regulator supply current	$I_{REGULATOR}$	V_{CC} = 4V, V_{DRAIN} = 100V	3	4.5	6	mA
DRAIN leakage current	I_{LEAK}	V_{DRAIN} = 400V			40	µA
Breakdown voltage	$V_{(BR)DSS}$	T_J = 25°C	700			V
On resistance	R_{ON}	T_J = 25°C		4.5	6.5	Ω
Brown-in threshold	V_{DS_BI}	T_J = 25°C		40		V
Supply Voltage (V_{CC}) Management						
Increasing V_{CC} level at which the internal regulator turns off	V_{HV_OFF}		8.4	9	9.6	V
Decreasing V_{CC} level at which the internal regulator turns on	V_{HV_ON}		7.9	8.5	9.1	V
HV regulator on and off hysteresis			200			mV
V_{CC} under-voltage lockout (UVLO) threshold	V_{CCL}		7	7.9	8.7	V
Decreasing V_{CC} level at which the protection phase ends	V_{CC_PRO}			3.5	4	V
IC consumption (5)	I_{CC}	f_{SW} = 40kHz, T_J = 25°C		920	1070	µA
		MOSFET on		900	1050	
		MOSFET off	220	310	400	
Internal IC consumption under protection	I_{CC_PRO}			40	65	µA
Internal Current Sense						
Peak current limit	I_{LIMIT}	T_J = 25°C	1.02	1.1	1.18	A
Leading-edge blanking (LEB) time	t_{LEB1}			230		ns
Short-circuit protection (SCP) threshold	I_{SCP}	T_J = 25°C	135%	155%	175%	I_{LIMIT}
LEB for SCP	t_{LEB2}			200		ns
Feedback (FB) Input						
Minimum off time	t_{MINOFF}		19.9	24	28.4	µs
Maximum on time	t_{MAXON}		29.5	34	39.5	µs
MOSFET turn-on threshold	V_{FB}		2.31	2.43	2.53	V
Overload protection (OLP) counter				4096		cycles
Open-loop detection (OLD)	V_{OLD}		0.2	0.3	0.4	V
Thermal Shutdown						
Over-temperature protection (OTP) threshold (5)				150		°C

Note:

5) Guaranteed by design.

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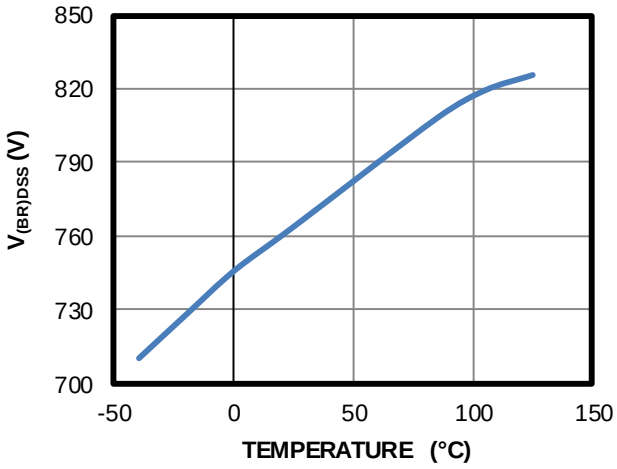
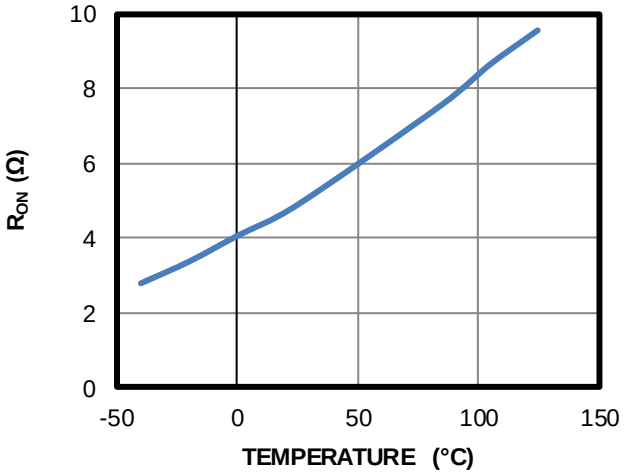
TYPICAL CHARACTERISTICS

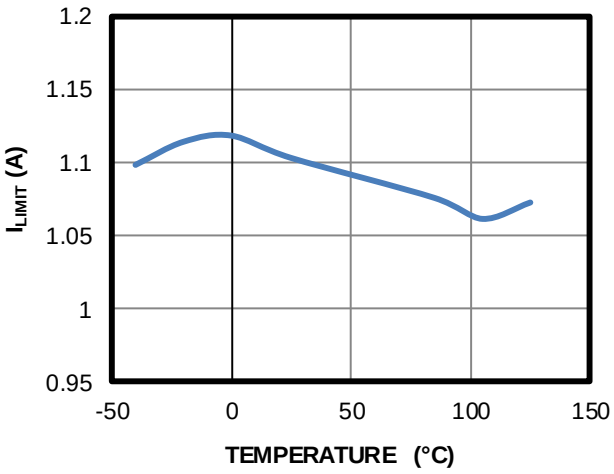
Breakdown Voltage vs. Temperature



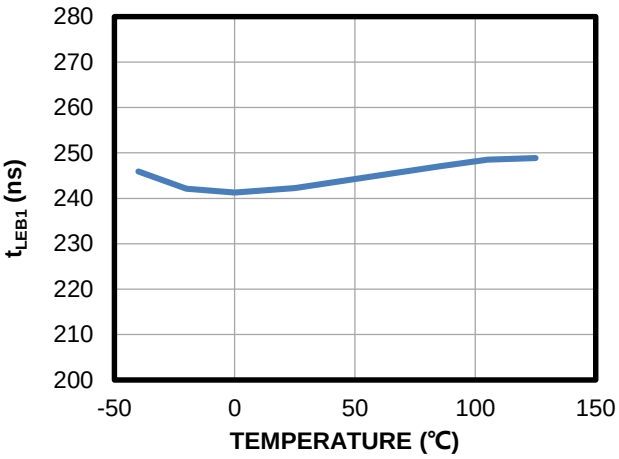
On Resistance vs. Temperature



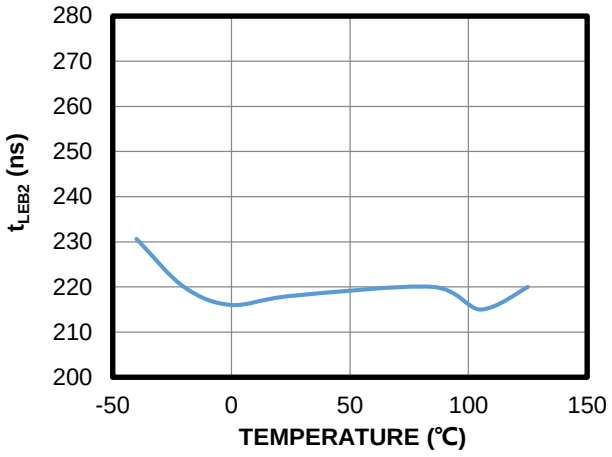
Peak Current Limit vs. Temperature



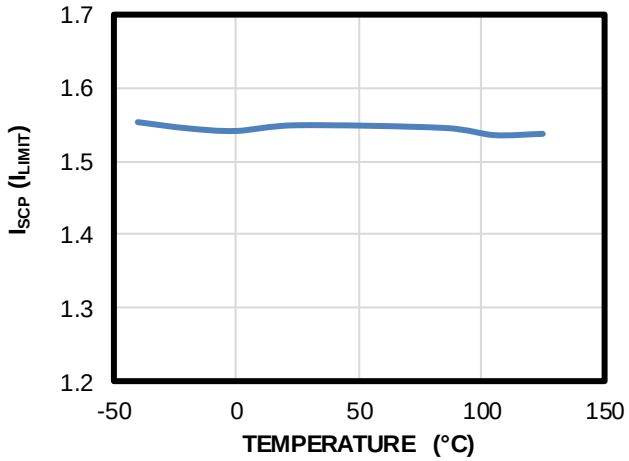
Leading-Edge Blanking Time vs. Temperature



Leading-Edge Blanking Time for SCP vs. Temperature



SCP Threshold vs. Temperature



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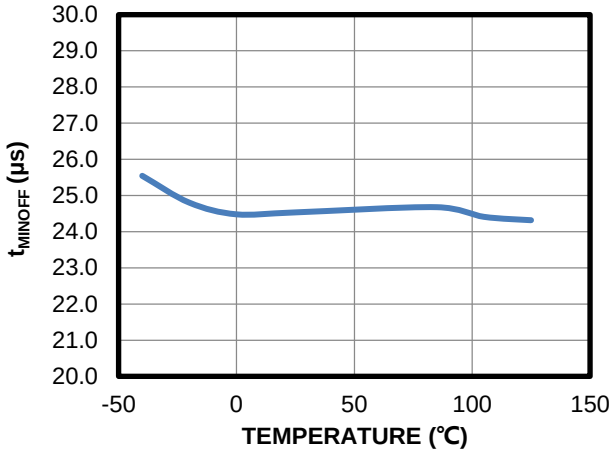
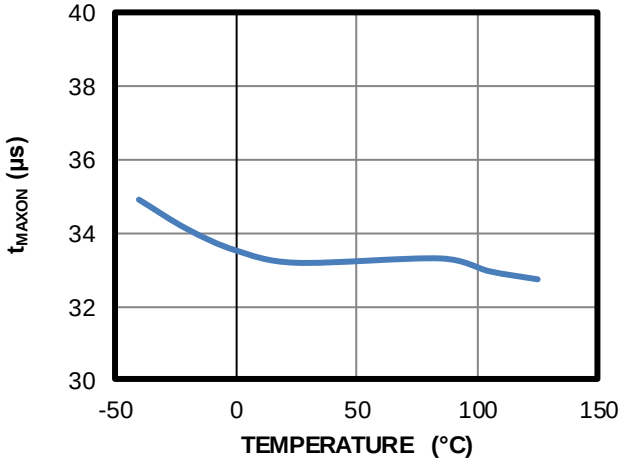
TYPICAL CHARACTERISTICS *(continued)*

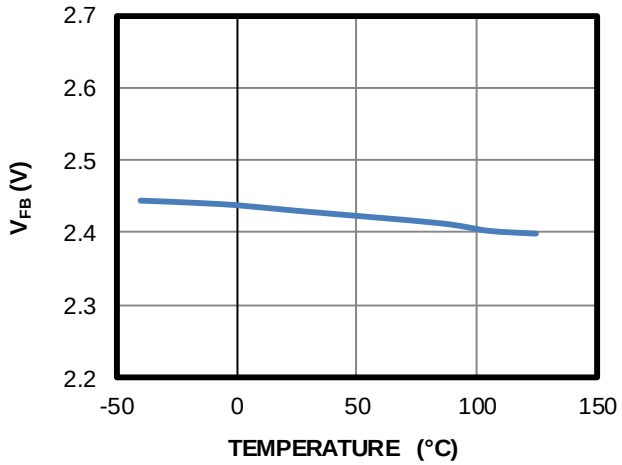
Minimum Off Time vs. Temperature



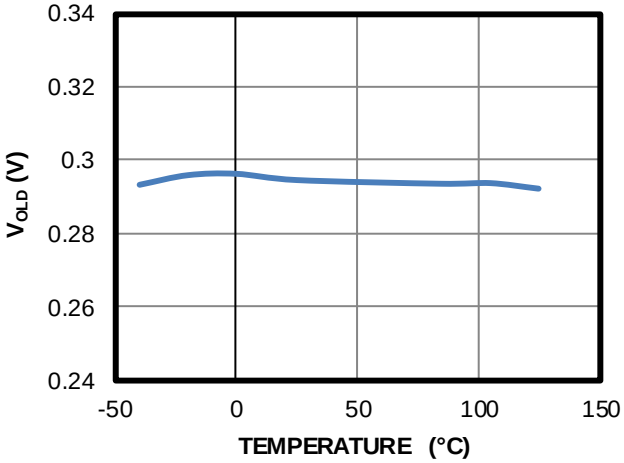
Maximum On Time vs. Temperature



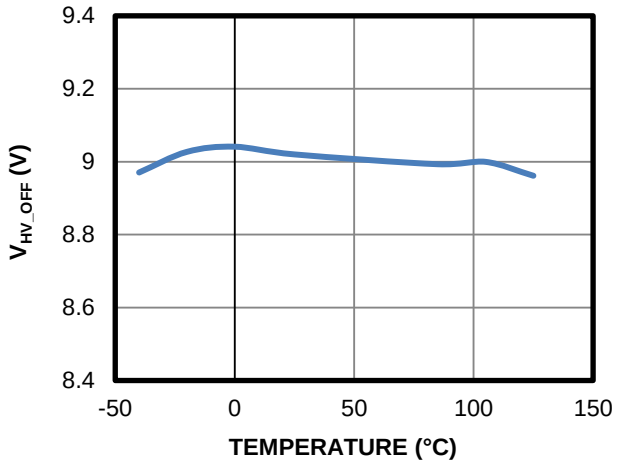
MOSFET Turn-On Threshold vs. Temperature



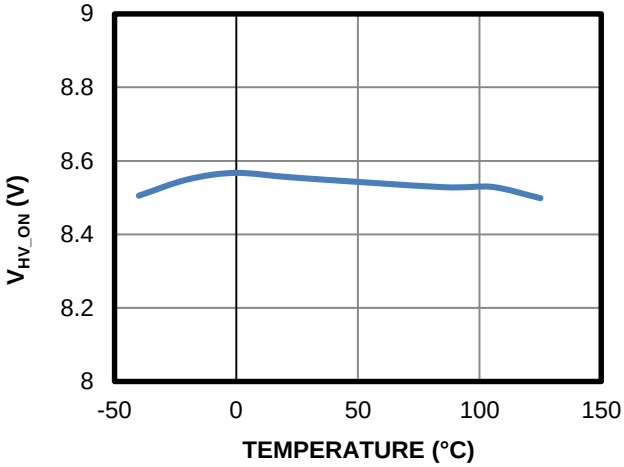
Open-Loop Detection vs. Temperature



Increasing VCC Level at which the Internal Regulator Turns Off vs. Temperature



Decreasing VCC Level at which the Internal Regulator Turns On vs. Temperature



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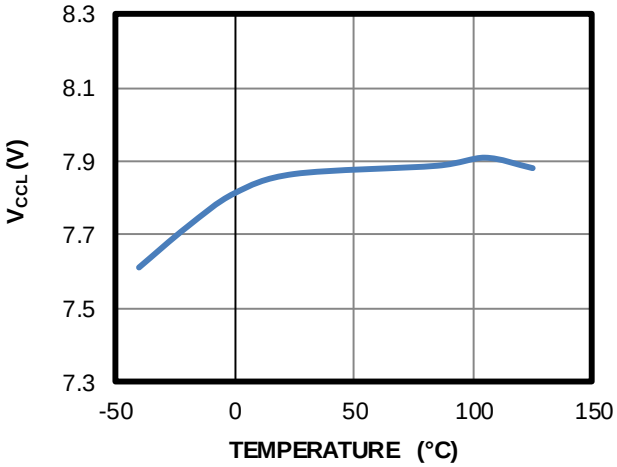
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} Under-Voltage Lockout Threshold vs. Temperature



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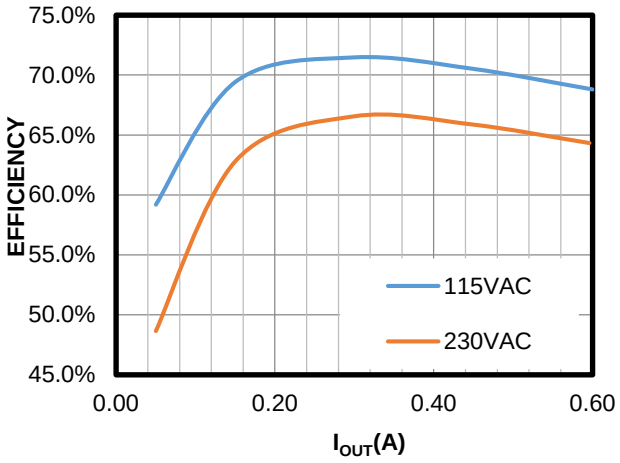
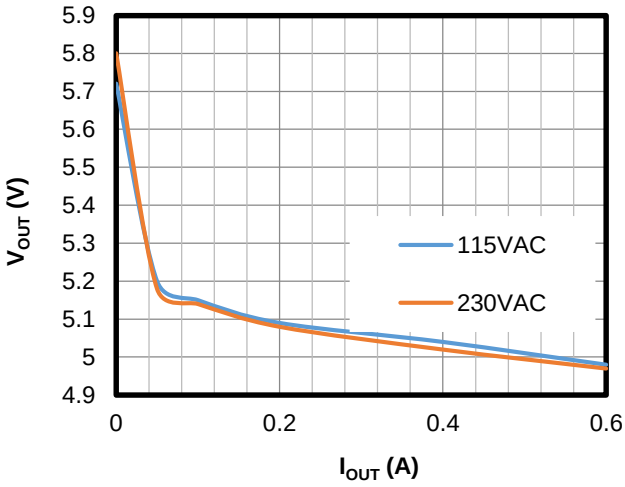
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested with the evaluation board, V_{IN} = 230V_{AC}, V_{OUT} = 5V, I_{OUT} = 600mA, T_A = 25°C, unless otherwise noted.

Efficiency vs. Output Current



Load Regulation



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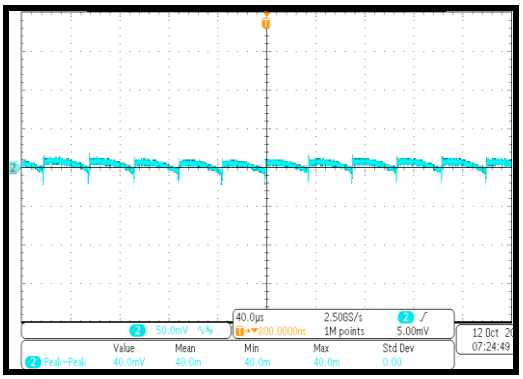
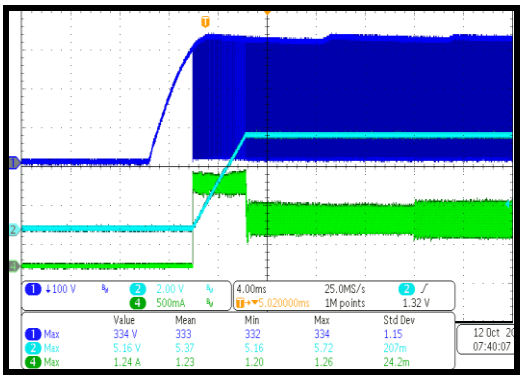
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested with the evaluation board, V_{IN} = 230V_{AC}, V_{OUT} = 5V, I_{OUT} = 600mA, T_A = 25°C, unless otherwise noted.

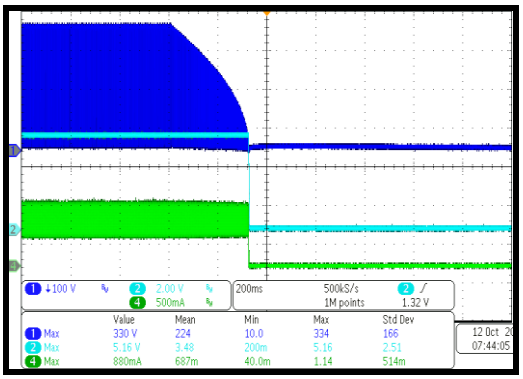
Ripple



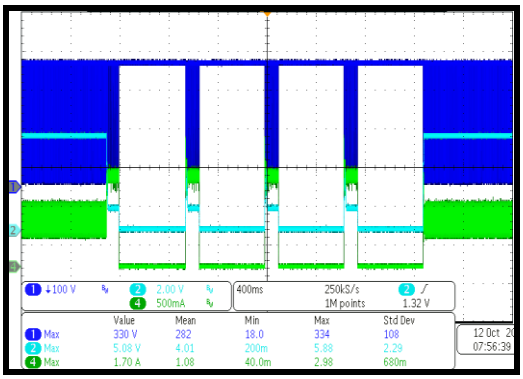
Start-Up



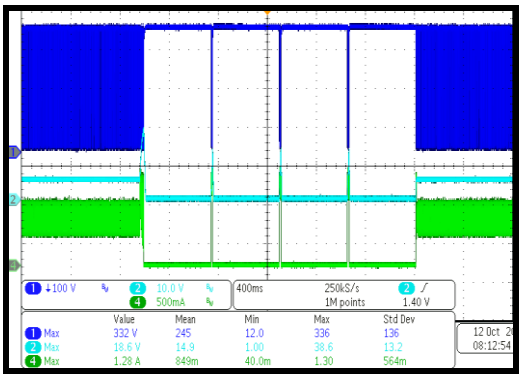
Shutdown



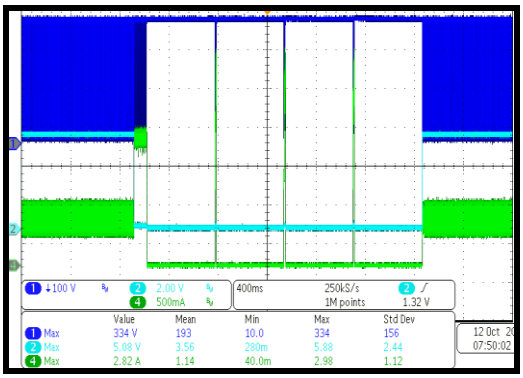
OLP Entry and Recovery



Open Loop Entry and Recovery



SCP Entry and Recovery



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FUNCTIONAL BLOCK DIAGRAM

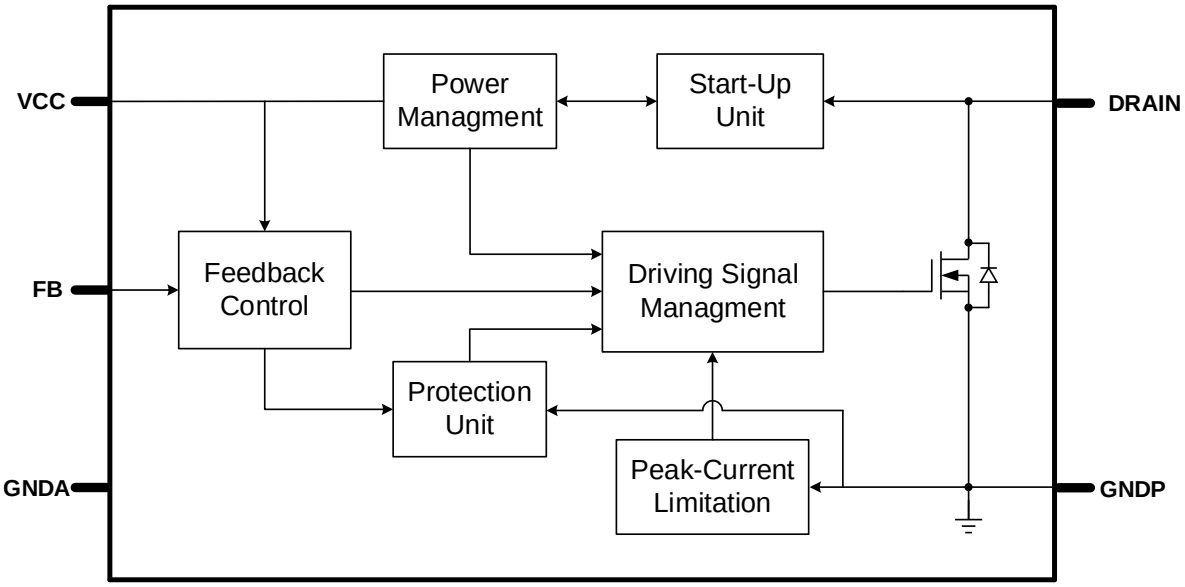

Figure 1: Functional Block Diagram

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OPERATION

The MP175L is a green-mode operation regulator. The peak current limit (I_{LIMIT}) and the switching frequency (f_{SW}) both decrease as the load decreases. As a result, the MP175L offers excellent light-load efficiency and improves average efficiency. The Typical Application diagram on page 1 shows a regular buck configuration.

Start-Up and Under-Voltage Lockout (UVLO)

The internal high-voltage current-source regulator supplies the VCC pin from DRAIN. When VCC is charged to the increasing supply voltage level (V_{HV_OFF}), the internal high-voltage current source turns off. Subsequently, the IC is ready for switching until the drain-to-source voltage reaches the brown-in threshold (V_{DS_BI}) before UVLO occurs. If VCC falls below the decreasing VCC level (V_{HV_ON}), then the internal high-voltage current source turns on to charge the external VCC capacitor. Therefore, the MP175L can work with a small VCC capacitor (in the low µF range).

UVLO makes the IC stop switching when VCC falls below the VCC UVLO threshold (V_{CCL}), preventing errors caused by an insufficient supply voltage. The IC remains off until the supply voltage (V_{CC}) is charged to V_{HV_OFF} again (see Figure 2).

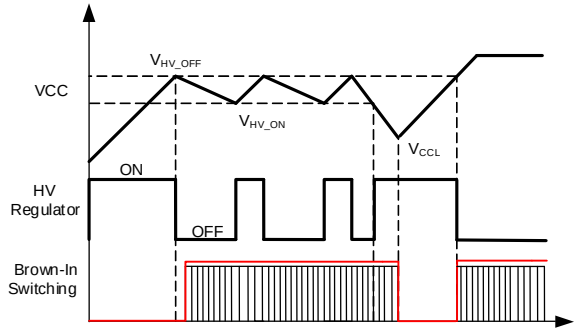

Figure 2: Start-Up and UVLO Operation

Soft Start (SS)

The soft start (SS) period, which occurs whenever the chip begins switching, prevents the inductor current from overshooting.

The MP175L implements SS by gradually decreasing the minimum off time in eight steps. Table 1 shows the sequence pattern for SS.

During SS, short-circuit protection (SCP), overload protection (OLP), and open-loop detection (OLD) are disabled.

Table 1: SS Sequence Pattern

Step	Min Off Time (µs)	Cycles
1	48	16
2	36	16
3	24	32
4	20	64
5	18	128
6	16	128
7	14	128
8	13	128

Constant-Voltage (CV) Operation

The MP175L is a constant-voltage (CV) regulator that regulates the output voltage (V_{OUT}) using the feedback (FB) voltage, depending on the external divider set-up.

Figure 3 shows that the internal MOSFET is turned on when the FB voltage falls below the MOSFET turn-on threshold (V_{FB}), and is turned off based on I_{LIMIT}. V_{FB} is the reference voltage for the FB pin.

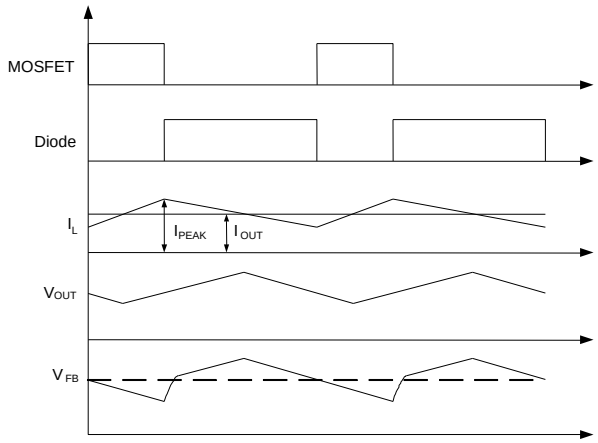

Figure 3: Constant-Voltage Regulation

In this way, the FB voltage is regulated at the reference voltage. V_{OUT} can be calculated using Equation (1):

$$V_{OUT} = V_{FB} \times \frac{R_{UP} + R_{LOW}}{R_{LOW}} \quad (1)$$

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Frequency Foldback and Peak-Current Compression

Due to the MP175L's constant voltage regulation scheme, the high-voltage regulator's switching frequency (f_{SW}) decreases as the load decreases. As a result, the MP175L can achieve excellent efficiency under light-load conditions.

f_{SW} can be estimated using Equation (2) for continuous conduction mode (CCM) and Equation (3) for discontinuous conduction mode (DCM):

$$f_{SW} = \frac{(V_{IN} - V_{OUT})}{2L \times (I_{PEAK} - I_{OUT})} \times \frac{V_{OUT}}{V_{IN}} \quad (2)$$

$$f_{SW} = \frac{2(V_{IN} - V_{OUT})}{L \times I^2_{PEAK}} \times \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \quad (3)$$

As f_{SW} decreases, I_{LIMIT} also decreases to minimize audible noise when the frequency drops down to the audible range. I_{LIMIT} can be estimated using Equation (4):

$$I_{PEAK} = I_{LIMIT} - (40mA/\mu s) \times (t_{OFF} - t_{MINOFF}) \quad (4)$$

The minimum peak current (I_{PEAK}) is limited internally.

Overload Protection (OLP)

The MP175L's maximum output power (P_{OUT}) is limited by t_{MINOFF} and I_{LIMIT}. The MP175L is considered to be in an overload condition when working under a t_{MINOFF}, which indicates a maximum f_{SW}.

When the MP175L works at a t_{MINOFF}, the overload protection (OLP) counter begins counting the switching cycle. If the counter reaches 4096 cycles, OLP is triggered. The OLP counter helps prevent OLP from triggering falsely during start-up or load transition.

The overload state is also affected by external settings, such as V_{IN}, V_{OUT}, and inductor value. OLP helps avoid overstress operation of the system in most cases.

Short-Circuit Protection (SCP)

The MP175L monitors I_{PEAK}, and shuts down if I_{PEAK} exceeds the SCP threshold. Once the fault condition is removed, the power supply resumes normal operation.

Over-Temperature Protection (OTP)

Over-temperature protection (OTP) is triggered when the junction temperature (T_J) exceeds the thermal shutdown threshold to prevent any thermally induced damage to the chip.

Brown-In Protection

The MP175L integrates a brown-in function by sampling the drain-to-source voltage (V_{DS}). After the IC stops switching, V_{DS} must exceed the brown-in threshold (V_{DS_BI}) before the IC can start to work again.

Brown-in protection prevents switching after shutdown.

Open-Loop Detection (OLD)

If V_{FB} is below the OLD threshold (V_{OLD}), the IC stops switching and a restart cycle begins. During SS, OLD is blanked.

To use OLD, the FB capacitor should be separated from the VCC capacitor. For circuit design recommendations, see the FB Set-Up section on page 13.

OLD is disabled when the VCC capacitor functions as an FB capacitor.

Leading-Edge Blanking (LEB)

An internal LEB unit prevents premature switching pulse termination due to a start-up spike. Start-up spikes are caused by parasitic capacitance and reverse recovery of the freewheeling diode. During the blanking time, the current comparator is disabled and cannot turn off the internal MOSFET (see Figure 4).

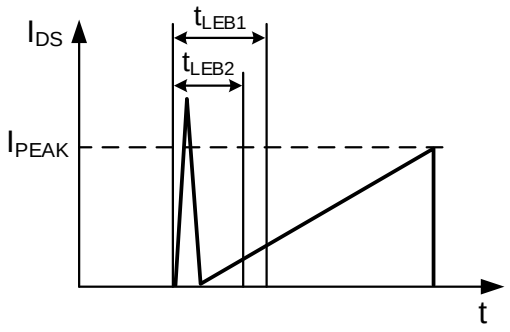

Figure 4: Leading-Edge Blanking Time

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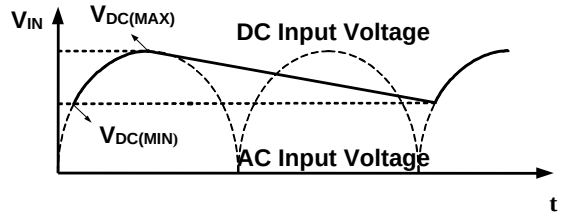
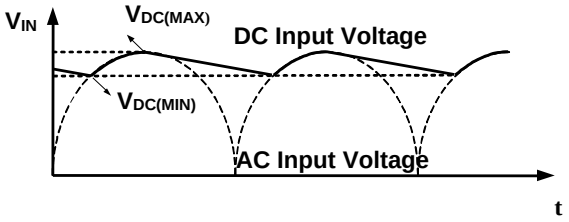
APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor supplies the DC input voltage (V_{IN}) to the converter. Figure 5 shows the typical DC bus voltage waveform of a half-wave rectifier and full-wave rectifier.



(a) V_{IN} of Half-Wave Rectifier



(b) V_{IN} of Full-Wave Rectifier

Figure 5: Input Voltage Waveforms

Typically, a half-wave rectifier requires an input capacitor rated at 3μF/W for the universal input condition. When using a full-wave rectifier, the input capacitor should be between 1.5μF/W and 2μF/W for the universal input condition. A half-wave rectifier is recommended for <2W output applications. A full-wave rectifier is recommended for >2W output applications.

Avoid using an input capacitor that is too small, since it may not hold the DC voltage high for long enough. A low DC V_{IN} can lead to bad thermal performance. If V_{IN} is very low, the MOSFET on time may reach the maximum on time (t_{MAXON}).

Selecting the Inductor

The MP175L has a t_{MINOFF} limit that determines the maximum P_{OUT}. Since I_{LIMIT} is fixed, the maximum power (P_{OMAX}) increases as the inductance increases. Using a small inductance may lead to insufficient output power, but a larger inductance results in an inappropriate OLP point.

It is recommended to select an inductor with the minimum inductance needed to meet the overload requirement. The I_{LIMIT} and t_{MINOFF} tolerances should also be considered for mass production. The OLP point can be estimated using Equation (5) for CCM or Equation (6) for DCM:

$$P_{OMAX} = V_{OUT} \times (I_{LIMIT} - \frac{V_{OUT} \times t_{MINOFF}}{2L}) \quad (5)$$

$$P_{OMAX} = \frac{1}{2} L \times I_{LIMIT}^2 \times \frac{1}{t_{MINOFF}} \quad (6)$$

To reduce costs, use a standard, off-the-shelf inductor with at least the calculated value.

Freewheeling Diode

The diode should be selected based on the maximum V_{IN} and I_{PEAK}.

Since the freewheeling diode's reverse recovery can affect efficiency and circuit operation in CCM, it is recommended to use an ultra-fast reverse recovery diode, such as the STTH2R06.

Selecting the Output Capacitor

The output capacitor (C_{OUT}) is required to maintain the DC V_{OUT}. The V_{OUT} ripple can be estimated using Equation (7) for CCM or Equation (8) for DCM:

$$V_{OUT_RIPPLE} = \frac{\Delta I}{8 f_{SW} \times C_{OUT}} + \Delta I \times R_{ESR} \quad (7)$$

$$V_{OUT_RIPPLE} = \frac{I_{OUT}}{f_{SW} \times C_{OUT}} \left(\frac{I_{PEAK} - I_{OUT}}{I_{PEAK}} \right)^2 + I_{PEAK} \times R_{ESR} \quad (8)$$

It is recommended to use low-ESR electrolytic or ceramic capacitors to reduce the V_{OUT} ripple.

FB Set-Up

Two kinds of FB set-ups are recommended for the MP175L (see Figure 6 and Figure 7 on page 14). The FB set-up can be selected according to cost and performance requirements.

Figure 6 on page 14 shows the typical external FB circuit with the OLD function enabled. C1 is a dedicated FB capacitor, isolated from VCC via D2. This prevents V_{CC} from interfering with the FB pin's operation. Both the VCC capacitor and FB loop can be adjusted. The set-up shown in Figure 6 is recommended for most

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applications due to its high reliability and good performance.

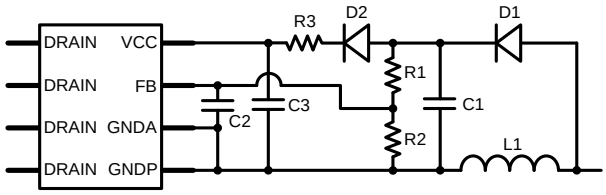

Figure 6: External FB Circuit with Dedicated FB Circuit

Figure 7 shows a typical external FB circuit using the VCC capacitor for V_{OUT} sampling. R1 and R2 form a resistor divider for adjustable V_{OUT}.

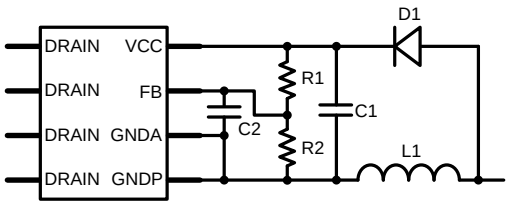

Figure 7: External FB Circuit

OLD is disabled in the set-ups shown in Figure 7. After start-up, V_{CC} is always above V_{CCL}. V_{FB} is proportional to V_{CC} due to the presence of the FB resistor divider, and V_{FB} cannot drop to V_{OLD}. However, the MP175L hiccups when the FB circuit is open because OLP is triggered.

External FB Resistors

The resistor divider determines V_{OUT}. Choose appropriate R1 and R2 values to maintain the FB voltage = 2.43V. R2 should typically be between 5kΩ and 20kΩ. It is recommended to avoid a large R2 value.

FB Capacitor

The FB capacitor provides a sample-and-hold function for V_{OUT} regulation. In Figure 6, C1 is the dedicated FB capacitor. In Figure 7, the VCC capacitor is used as the FB capacitor.

A large FB capacitor (a few μF in value) is typically preferred because it helps reduce no-load consumption and achieves good light-load regulation. However, stability may be affected if the FB capacitor is too large.

A large VCC capacitor can help increase the hiccup interval during protections, which reduces the input power during SCP and reduces V_{OUT} under open-loop conditions.

Control Loop Robustness Optimization

The MP175L requires a small capacitor connected between FB and GND to achieve stable operation (about 1nF, which may vary in different applications). This small capacitor bypasses the noises that interfere with FB sampling.

Dummy Load

The MP175L switches at a minimum f_{SW} and delivers a certain amount of power under no-load conditions. This minimum f_{SW} is determined by the feedback discharging rate. A dummy load is required to dissipate this power and keep V_{OUT} regulated.

A large dummy load current leads to better regulation but larger no-load consumption. A tradeoff must be made between small no-load consumption and good no-load regulation for the intended application.

Surge Performance

The input capacitor and filter can also be used for surge suppression. If an appropriate input circuit is chosen, the MP175L may pass the low-level surge test without any other surge suppression components. Figure 8 shows the typical half-wave rectifier used in low-power offline applications.

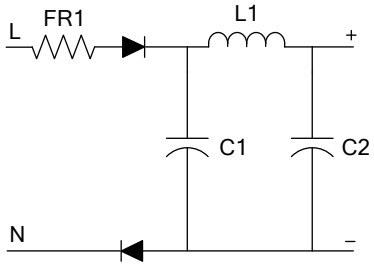

Figure 8: Half-Wave Rectifier

Table 2 shows the capacitance required by the MP175L under normal conditions for different surge levels. FR1 is a 20Ω/2W fused resistor, and L1 is 1mH for this recommendation.

Table 2: Recommended Capacitance

Surge Voltage	C1	C2
500V	1μF	1μF
1000V	2.2μF	2.2μF
2000V	3.3μF	3.3μF

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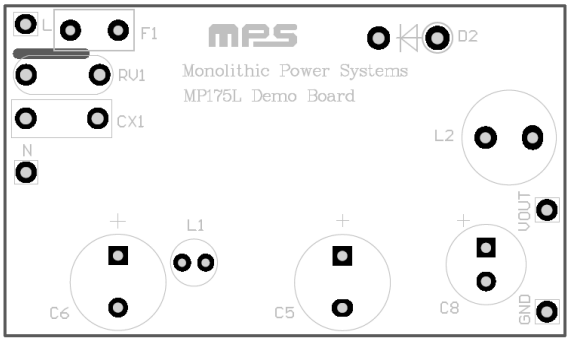
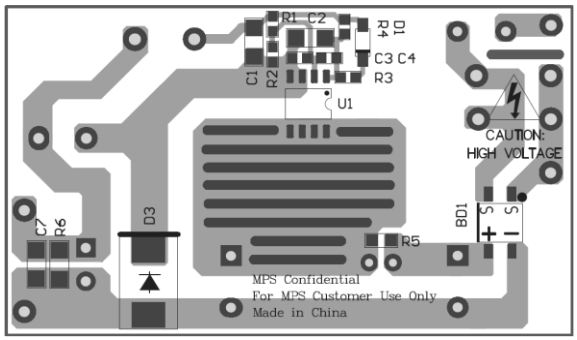
PCB Layout Guidelines

PCB layout is critical for reliable operation, as well as good EMI and thermal performance. For the best performance, refer to Figure 9 and follow the guidelines below:

1. Minimize the loop area formed by the input capacitor, the MP175L's internal MOSFET, the freewheeling diode, the inductor, and the output capacitor.
2. Place the power inductor far away from the input filter while minimizing the loop area.
3. Keep the AC input loop as small as possible to prevent noise coupling.
4. Place a bypass capacitor (about 1nF) between FB and GND, as close to the IC as possible.
5. Connect a large copper area to DRAIN for better thermal performance.



Top Layer



Bottom Layer

Figure 9: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

Figure 10 shows a typical application example of an 5V/600mA, non-isolated power supply using the MP175L.

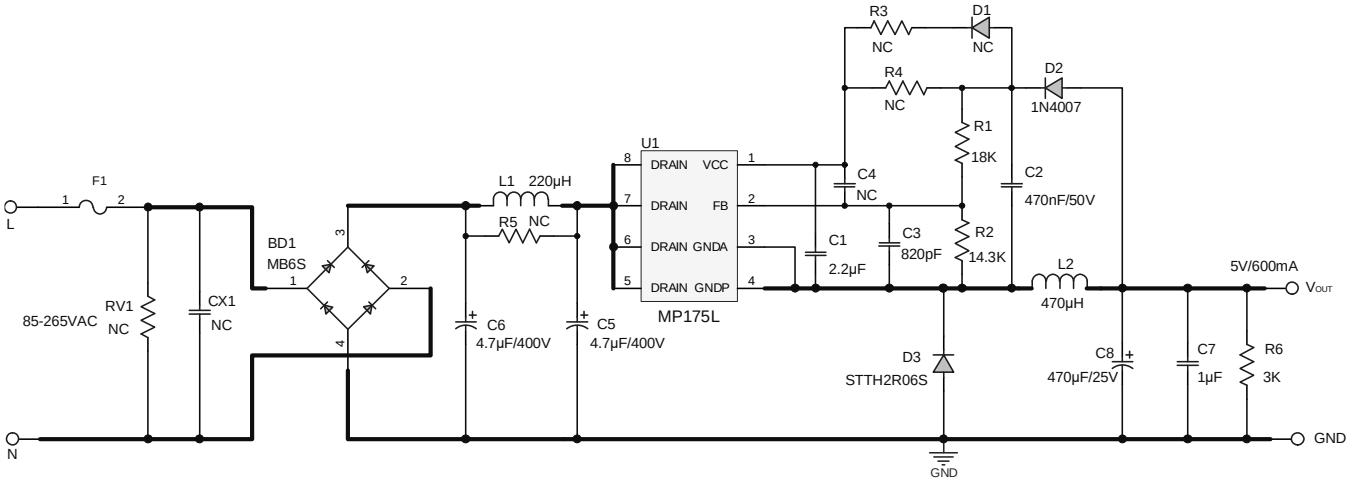

Figure 10: Typical Application with Universal Input and 5V/600mA Output

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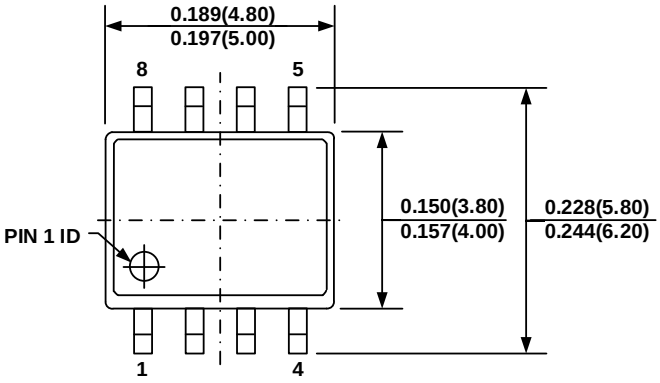
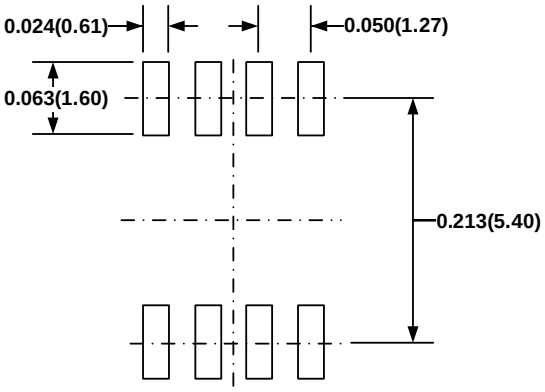
PACKAGE INFORMATION

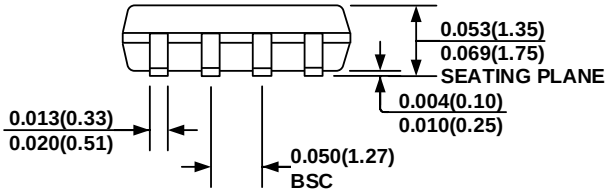
SOIC-8



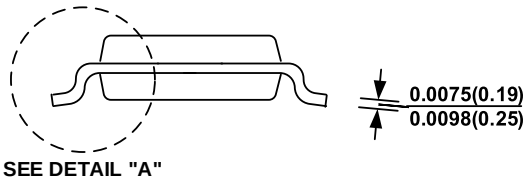
TOP VIEW



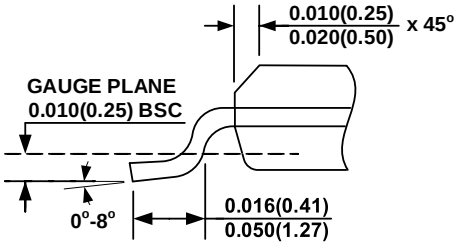
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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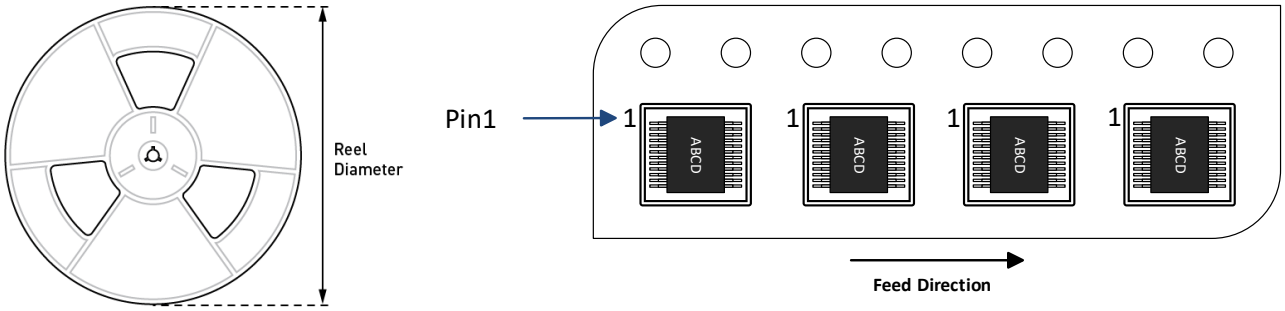
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP175LGS-Z	SOIC-8	2500	100	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/06/2021	Initial Release	-

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