MP171A

700V, Non-Isolated, Offline Regulator, Up to 60mA Output Current with Improved EMI Performance

DESCRIPTION

The MP171A is a primary-side regulator that provides accurate constant voltage (CV) regulation without an optocoupler. It supports buck, boost, buck-boost, and flyback topologies.

The device's integrated 700V MOSFET simplifies the structure and reduces cost. This feature optimizes the device for offline, low-power applications such as home appliances and standby power.

The MP171A is a green-mode operation regulator. Both the peak current and switching frequency lower as the load decreases. This feature provides excellent efficiency at light load, and improves the overall efficiency.

Protection features include thermal shutdown (TSD), VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), and open-loop detection.

The MP171A is available in TSOT23-5 and SOIC-8 packages.

FEATURES

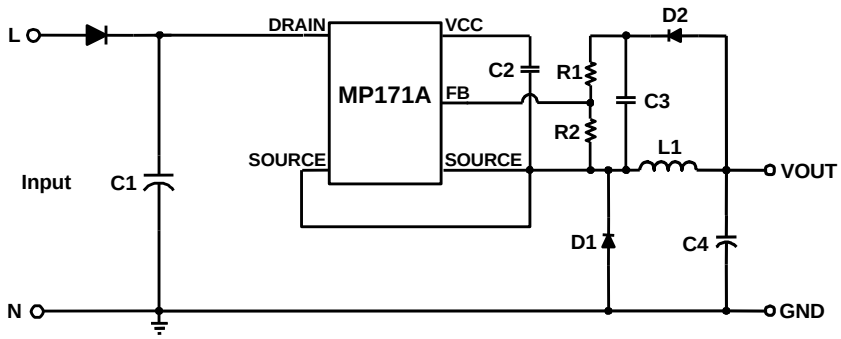
- Primary-Side CV Control
- Supports Buck, Boost, Buck-Boost, and Flyback Topologies
- Integrated 700V MOSFET and Current Source
- Under 30mW No-Load Power Consumption
- Up to 2W Output Power
- Maximum DCM Output Current below 40mA
- Maximum CCM Output Current below 60mA
- Low VCC Operating Current
- Frequency Foldback
- Limited Maximum Frequency
- Peak Current Compression
- Internally Biased VCC
- TSD, UVLO, OLP, SCP, Open-Loop Detection
- Available in TSOT23-5 and SOIC-8 Packages

APPLICATIONS

- Home Appliances, White Goods, and Consumer Electronics
- Industrial Controls
- Standby Power

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are registered trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP171AGJ*	TSOT23-5	*See Below*	1
MP171AGS**	SOIC-8	*See Below*	2

* For Tape & Reel, add suffix –Z (e.g. MP171AGJ–Z).

** For Tape & Reel, add suffix –Z (e.g. MP171AGS–Z).

TOP MARKING (MP171AGJ)

BMXY

BMX: Product code of MP171AGJ
Y: Year code

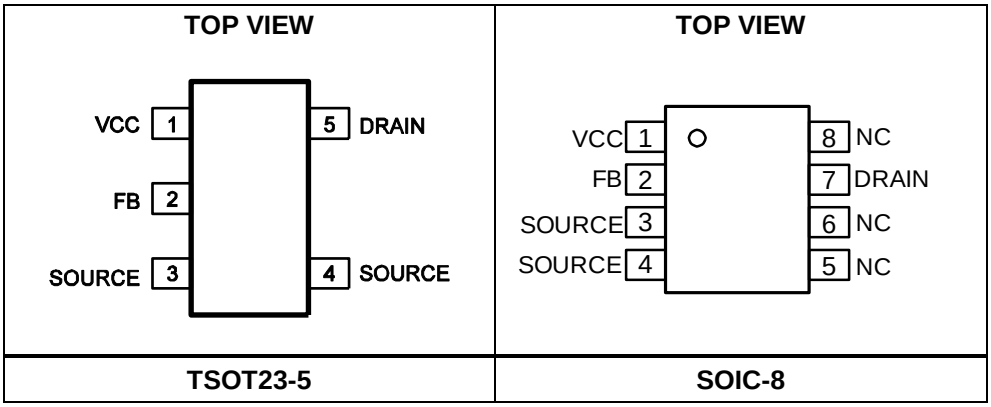
TOP MARKING (MP171AGS)

MP171A
LLLLLLLL
MPSYWW

MP171A: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE REFERENCE



TSOT23-5	SOIC-8

PIN FUNCTIONS

Pin # TSOT23-5	Pin # SOIC-8	Name	Description
1	1	VCC	**Control circuit power supply.**
2	2	FB	**Regulator feedback.**
3, 4	3, 4	SOURCE	**Internal power MOSFET source.** Ground reference for the VCC and FB pins.
5	7	DRAIN	**Internal power MOSFET drain.** High-voltage current source input.
	5, 6, 8	N/C	**Not connected.**

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Drain to source (T_J = 25°C)..... -0.3V to +700V
All other pins..... -0.3V to +6.5V
Continuous power dissipation ..... (T_A = 25°C) (2)
TSOT23-5.....1W
SOIC-8 .....1W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -60°C to +150°C

ESD Rating

Human body model (HBM) 2.0kV
Charged device model (CDM)
TSOT23-5.....1.2kV
SOIC-8…….....1.5kV

Recommended Operating Conditions (3)

Operating junction temp (T_J) .... -40°C to +125°C
Operating VCC range ..... 5.5V to 5.7V

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-5 ..... 100 ..... 55 ... °C/W
SOIC-8..... 96 ..... 45 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowance continuous power dissipation at any ambient temperature is calculated with P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowance power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

VCC = 5.5V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-Up Current Source and Internal MOSFET (DRAIN)						
Internal regulator supply current	$I_{REGULATOR}$	VCC = 4V, V_{DRAIN} = 100V	2.2	4.1	6	mA
DRAIN leakage current	I_{LEAK}	VCC = 5.8V, V_{DRAIN} = 400V		10	17	µA
Breakdown voltage	$V_{(BR)DSS}$	T_J = 25°C	700			V
On resistance	R_{ON}	T_J = 25°C		20	25	Ω
Supply Voltage Management (VCC)						
VCC increasing level where the internal regulator stops	VCC_{OFF}		5.4	5.7	6	V
VCC decreasing level where the internal regulator turns on	VCC_{ON}		5.1	5.5	5.8	V
VCC regulator on and off hysteresis			130	250		mV
VCC decreasing level where the IC stops	VCC_{STOP}		3	3.4	3.6	V
VCC decreasing level where the protection phase ends	VCC_{PRO}		2	2.5	2.8	V
Internal IC consumption	I_{CC}	f_{SW} = 36kHz, D = 64%			720	µA
Internal IC consumption (no switching)					200	µA
Internal IC consumption (latch-off phase)	$I_{CCLATCH}$	VCC = 5.3V		16	24	µA
Internal Current Sense						
Peak current limit	I_{LIMIT}	T_J = 25°C	85	105	125	mA
Leading-edge blanking	t_{LEB1}			350		ns
SCP threshold	I_{SCP}	T_J = 25°C	220	300	400	mA
Leading-edge blanking for SCP (1)	t_{LEB2}			180		ns
Feedback Input (FB)						
Minimum off time	t_{MINOFF}		7.5	10	12.5	µs
Maximum on time	t_{MAXON}		13	18	23	µs
Primary MOSFET feedback turn-on threshold	V_{FB}		2.45	2.55	2.65	V
OLP feedback trigger threshold	V_{FB_OLP}		1.64	1.74	1.84	V
OLP delay time	t_{OLP}	f_{SW} = 36 kHz		175		ms
Open-loop detection	V_{OLD}		0.4	0.5	0.6	V
Thermal Shutdown						
Thermal shutdown threshold (5)				150		°C
Thermal shutdown recovery hysteresis (5)				30		°C

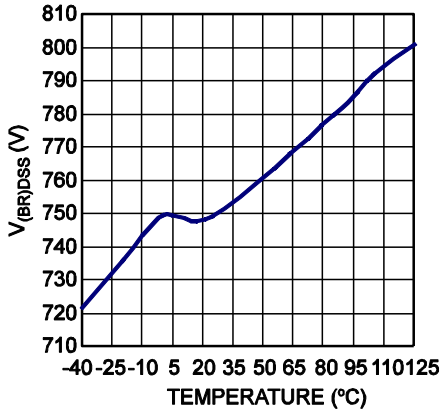
Note:

5) This parameter is guaranteed by design.

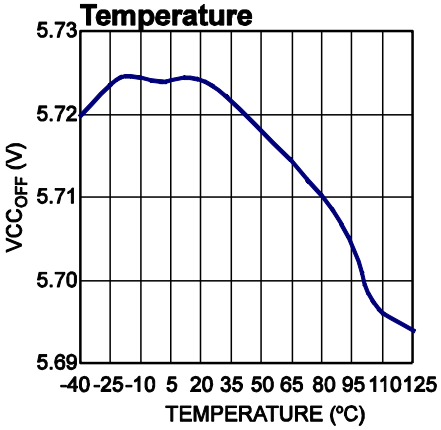
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

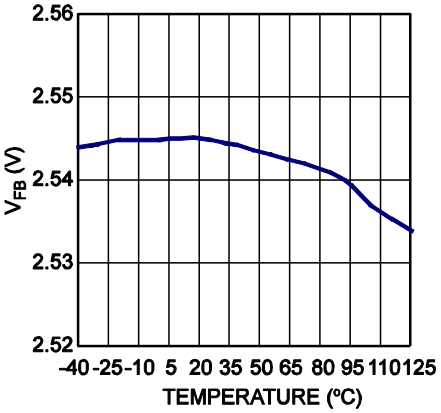
Breakdown Voltage vs. Temperature



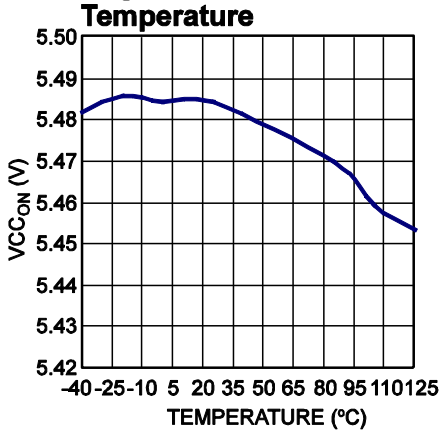
VCC Increasing Level at which the Internal Regulator Stops vs. Temperature



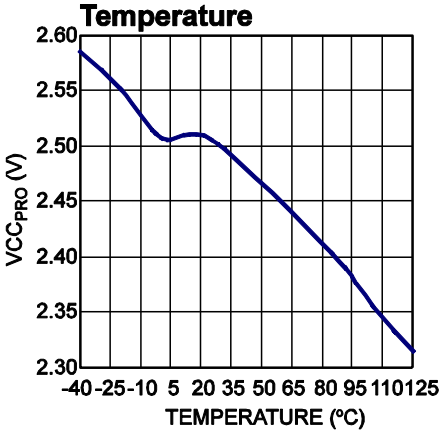
Feedback Voltage vs. Temperature



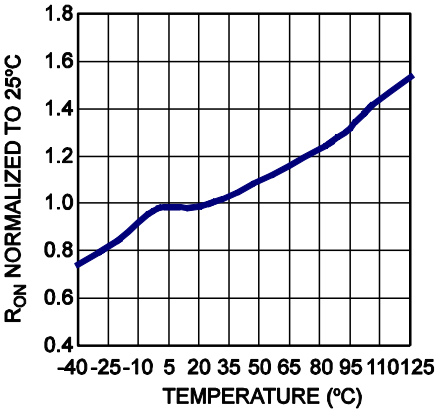
VCC Decreasing Level at which the Internal Regulator Turns On vs. Temperature



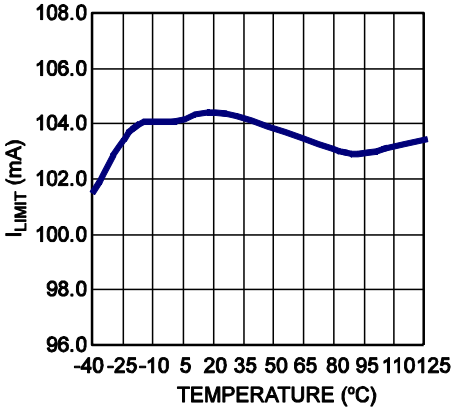
VCC Decreasing Level at which the Protection Phase Ends vs. Temperature



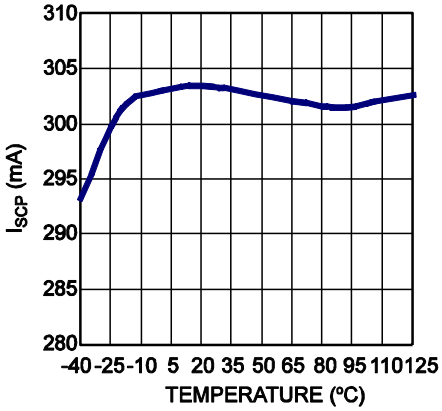
On-State Resistance vs. Temperature



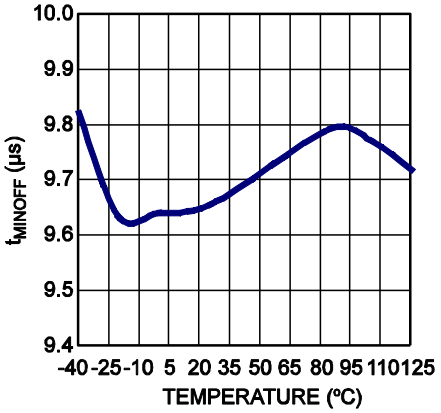
Peak Current Limit vs. Temperature



SCP Point vs. Temperature



Minimum Off Time vs. Temperature

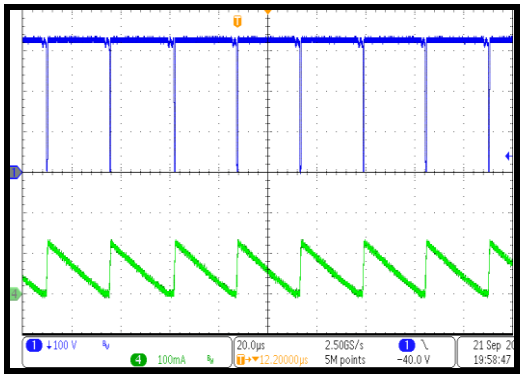


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

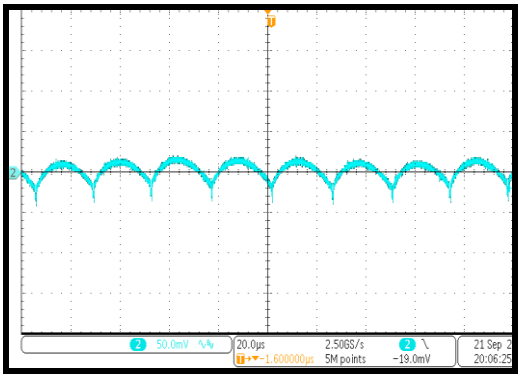
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 230VAC, V_{OUT} = 5V, I_{OUT} = 50mA, L = 1mH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

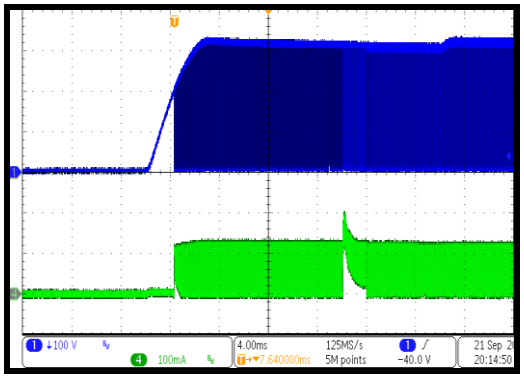
Steady State



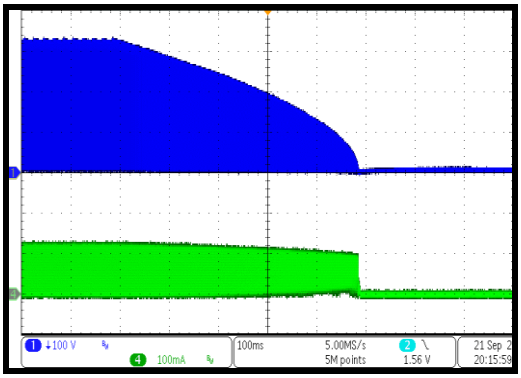
Output Ripple



Start-Up

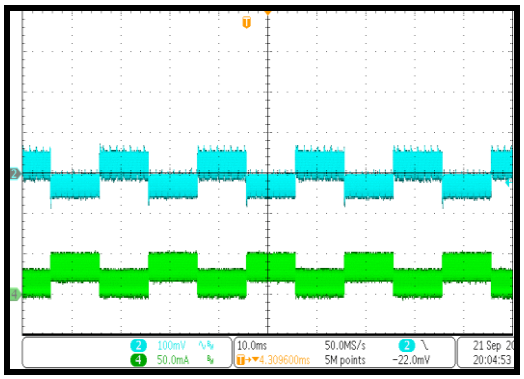


Shutdown

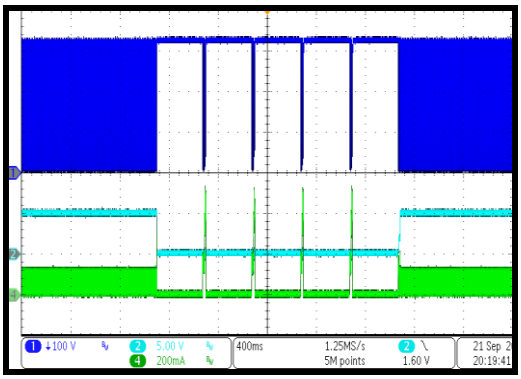


Load Transient

Half-load to full load



SCP Entry and Recovery

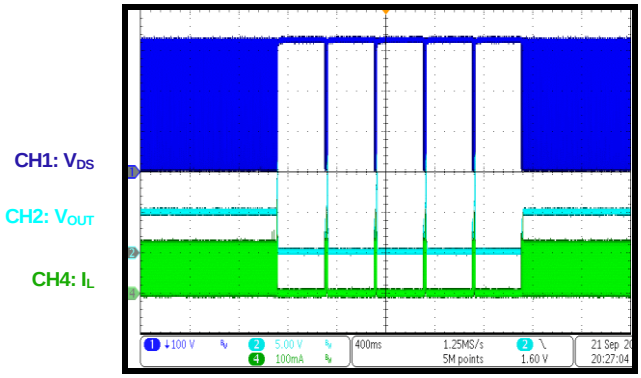


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 230VAC, V_{OUT} = 5V, I_{OUT} = 50mA, L = 1mH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Open-Loop Entry and Recovery



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

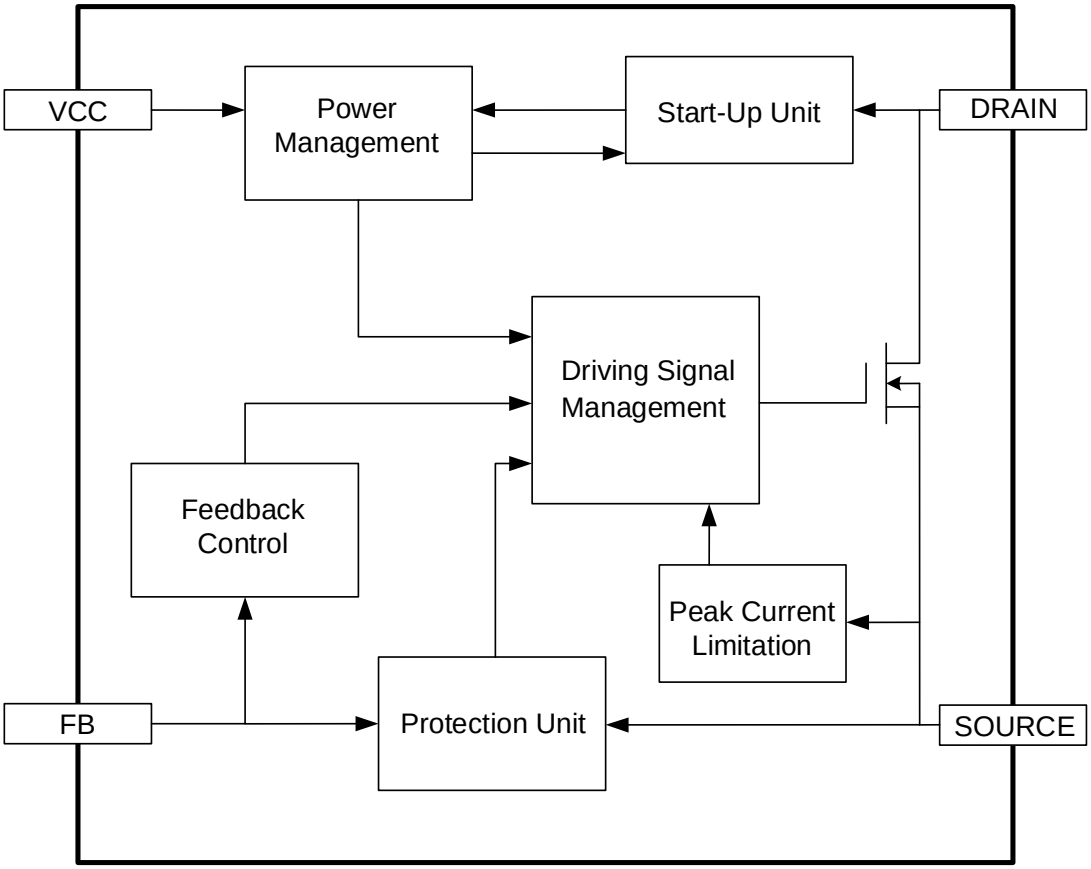


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

OPERATION

The MP171A is a green-mode operation regulator. The peak current and switching frequency both drop with a decreasing load. As a result, the device offers excellent light-load efficiency and improves overall efficiency. The regulator incorporates multiple features and operates with a minimal number of external components.

The device acts as a fully integrated regulator when used in buck topology (see the Typical Application on page 1).

Start-Up and Under-Voltage Lockout (UVLO)

The internal high-voltage regulator self-supplies the IC from DRAIN. When the VCC voltage reaches VCC_{OFF}, the IC switches and the internal high-voltage regulator turns off. The internal high-voltage regulator turns on to charge the external VCC capacitor when the VCC voltage falls below VCC_{ON}. A capacitor with a low µF value is recommended to maintain the VCC voltage, and lower the capacitor cost.

The IC stops switching when the VCC voltage drops below VCC_{STOP}.

Under fault conditions, such as overload protection (OLP), short-circuit protection (SCP), and thermal shutdown (TSD), the IC stops switching. The internal current source $I_{CCLATCH}$ (about 16µA) discharges the VCC capacitor. The internal high-voltage regulator does not charge the VCC capacitor until the VCC voltage drops below VCC_{PRO}. The restart time can be estimated with Equation (1):

$$t_{RESTART} = C_{VCC} \times \left(\frac{VCC - VCC_{PRO}}{I_{CCLATCH}} + \frac{VCC_{OFF} - VCC_{PRO}}{I_{REGULATOR}} \right) \quad (1)$$

Soft Start (SS)

The MP171A stops operation when the VCC voltage drops below VCC_{STOP}. Operation resumes when VCC charges to VCC_{OFF}. When the IC initiates operation, there is always a soft-start period. The soft start limits the minimum off time to prevent the inductor current from overshooting.

The MP171A adopts a two-phase minimum off time limit soft start. Each phase retains 256 switching cycles. During a soft start, the off time limit gradually shortens from 48µs to 18µs until it reaches the standard off time limit (see Figure 2).

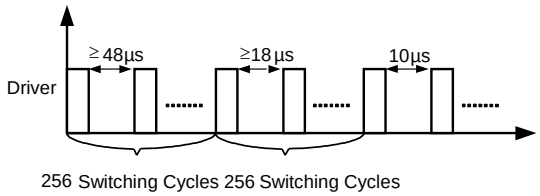


Figure 2: t_{MINOFF} at Start-Up

Constant Voltage Operation

Take Typical Application on page 1 for reference, the MP171A regulates the output voltage by monitoring the sampling capacitor (C3).

At the beginning of each cycle, the integrated MOSFET turns on when the feedback voltage drops below the 2.55V reference voltage (V_{FB}) and indicates insufficient output. The peak current limitation determines the on period. After the on period, the integrated MOSFET turns off.

The sampling capacitor (C3) voltage charges to the output voltage when the freewheeling diode (D1) turns on. The sampling capacitor (C3) samples and holds the output voltage for output regulation. The sampling capacitor's (C3) voltage drops when the L1 inductor current falls below the output current. When the feedback voltage drops below the 2.55V reference voltage, a new switching cycle begins. Figure 3 shows this operation in continuous conduction mode (CCM).

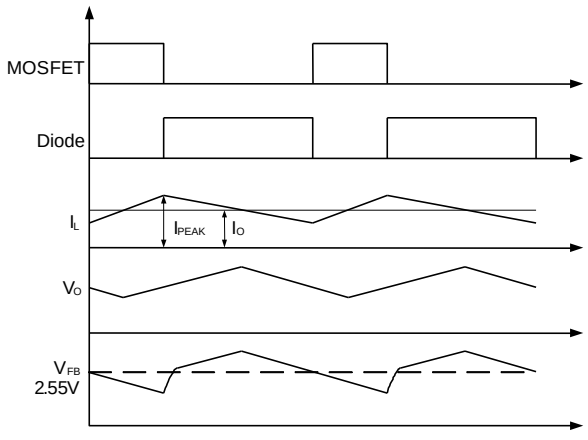


Figure 3: V_{FB} vs. V_O

The output voltage (V_O) can be estimated with Equation (2):

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

$$V_{OUT} = 2.55V \times \frac{R1+R2}{R2} \quad (2)$$

Frequency Foldback and Peak Current Compression

The MP171A automatically reduces the switching frequency to maintain high efficiency during light-load conditions. Under light-load or no-load conditions, the output voltage drops slowly to increase the MOSFET off time. The frequency drops as the load drops.

The switching frequency can be calculated with Equation (3) and Equation (4) for CCM and DCM, respectively:

$$f_{SW} = \frac{(V_{IN} - V_{OUT})}{2L \times (I_{PEAK} - I_{OUT})} \times \frac{V_{OUT}}{V_{IN}} \quad (3)$$

$$f_{SW} = \frac{2(V_{IN} - V_{OUT})}{L \times I^2_{PEAK}} \times \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \quad (4)$$

As the peak current limit drops from I_{LIMIT}, the off time increases. In standby mode, the frequency and the peak current are both minimized to allow for a smaller dummy load. As a result, peak current compression reduces no-load consumption. The peak current limit can be estimated with Equation (5):

$$I_{PEAK} = 105mA - (0.4mA/\mu s) \times (t_{OFF} - 10\mu s) \quad (5)$$

Where t_{OFF} is the off time of the power module.

EA Compensation

The MP171A has an internal error amplifier (EA) compensation loop (see Figure 4). It samples the feedback voltage 6µs after the MOSFET turns off, and regulates the output based on the 2.55V reference voltage.

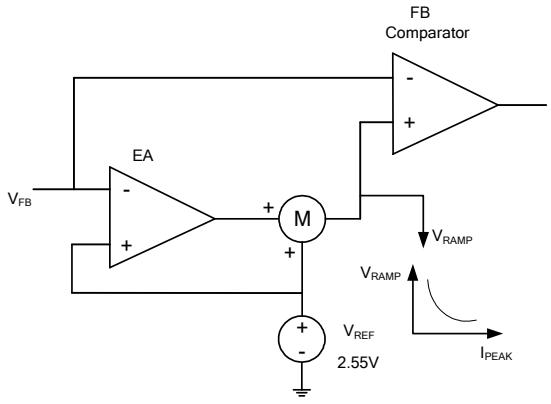


Figure 4: EA and Ramp Compensation

Ramp Compensation

An internal ramp compensation circuit improves the load regulation. An exponential voltage signal is added to pull down the feedback comparator's reference voltage (see Figure 4). The ramp compensation is a function of the load conditions; the compensation is about 1mV/µs under full-load conditions. The compensation increases exponentially as the peak current decreases.

Overload Protection (OLP)

The MP171A's maximum output power is limited by the minimum off time and peak current limit. If the load is too large, the output voltage drops with the feedback voltage.

An error occurs when V_{FB} drops below V_{FB_OLP}, and the timer starts. If the timer reaches 170ms (f_{SW} = 36kHz), overload protection (OLP) occurs. This timer duration avoids triggering OLP when the power supply starts up or the load transitions. The power supply should start up in less than 170ms (f_{SW} = 36kHz). The OLP delay time is calculated with Equation (6):

$$t_{DELAY} \approx 170ms \times \frac{36kHz}{f_{SW}} \quad (6)$$

Short-Circuit Protection (SCP)

The MP171A monitors the peak current, and shuts down when the peak current exceeds the short-circuit protection (SCP) threshold. The power supply resumes operation once the fault is removed. During soft start and the following 512 cycles, SCP is blanked to guarantee a successful start-up with a large output capacitor.

Thermal Shutdown (TSD)

To prevent thermal damage, the MP171A stops switching when the junction temperature exceeds 150°C. During thermal shutdown (TSD), the VCC capacitor is discharged to VCC_{PRO}, and the internal high-voltage regulator recharges. The device recovers when the junction temperature falls below 120°C.

Open-Loop Detection

If V_{FB} drops below V_{OLD}, the IC stops switching and initiates a restart period. During soft start and the following 512 cycles, open-loop detection is

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

blanked. This guarantees successful start-up with a large output capacitor.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Leading-Edge Blanking (LEB)

An internal leading-edge blanking (LEB) unit avoids premature switching pulse termination due to a turn-on spike. Turn-on spikes are caused by parasitic capacitance and reverse recovery of the freewheeling diode. During the blanking time, the current comparator is disabled and cannot turn off the external MOSFET. Figure 5 shows leading-edge blanking.

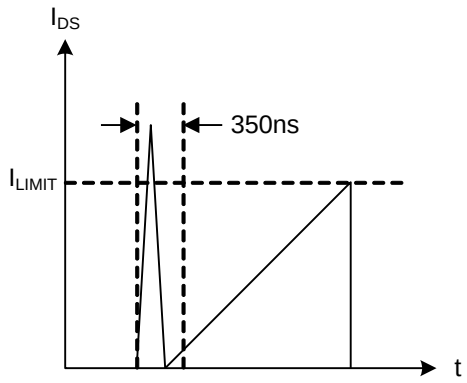
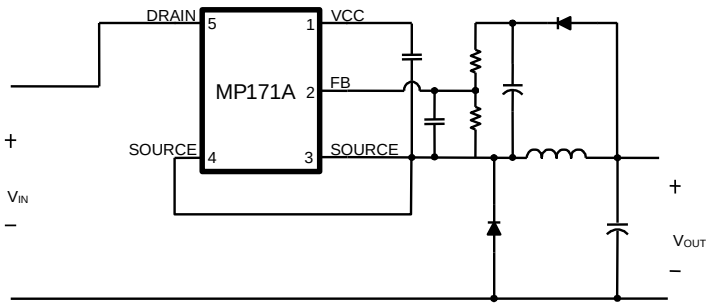
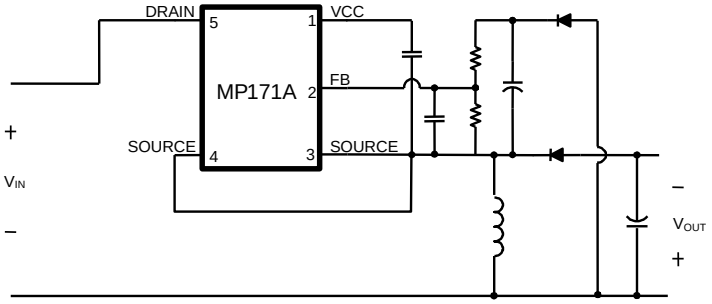
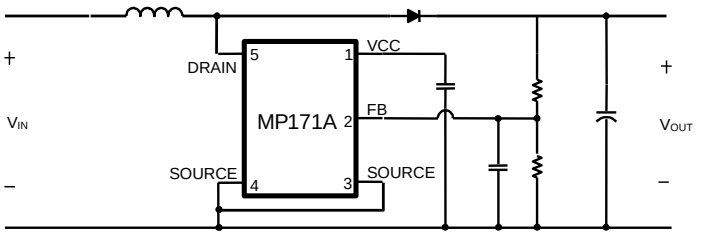
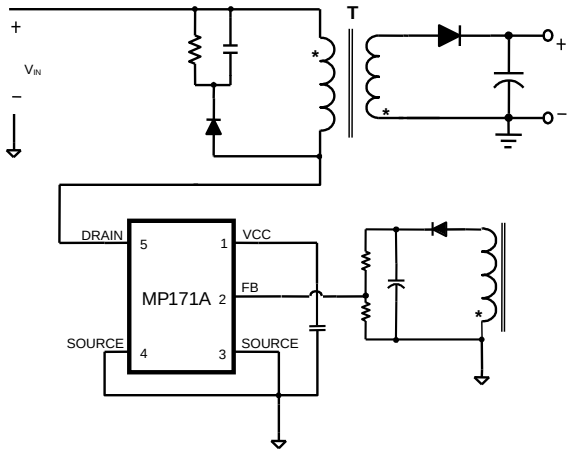


Figure 5: Leading-Edge Blanking

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

APPLICATION INFORMATION

Table 1: Common Topologies for the MP171A

Topology	Circuit Schematic	Features
High-side buck		• No isolation • Positive output • Low cost • Direct feedback
High-side buck boost		• No isolation • Negative output • Low cost • Direct feedback
Boost		• No isolation • Positive output • Low cost • Direct feedback
Flyback		• Isolation • Positive output • Low cost • Indirect feedback

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Topology Options

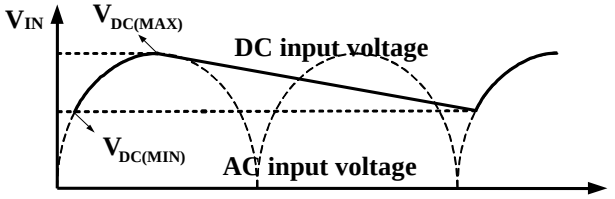
The MP171A can be used in common topologies, such as buck, boost, buck-boost, and flyback (see Table 1 on page 13).

The component selections below are based on the MP171A's typical application (see page 1).

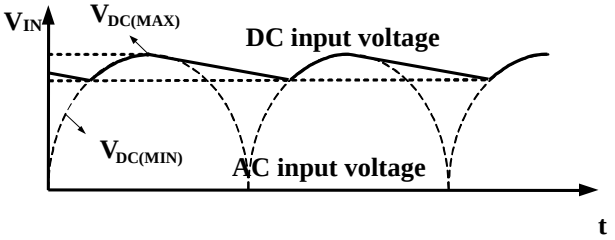
Component Selection

Input Capacitor

The input capacitor supplies the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of a half-wave rectifier and a full-wave rectifier.



Half-wave rectifier



Full-wave rectifier

Figure 6: Input Voltage Waveform

A half-wave rectifier typically requires an input capacitor (about 3μF/W) for the universal input condition. When using the full-wave rectifier, the input capacitor should be between 1.5μF/W and 2μF/W for the universal input condition.

Avoid a minimum DC voltage below 70V. A low DC input voltage can cause thermal instability. A half-wave rectifier is recommended for output applications that do not require more than 2W; otherwise, a full-wave rectifier is recommended for output applications that require more than 2W.

Inductor

The MP171A has a minimum off time limit that determines the maximum power output. The maximum power increases as the inductance increases. A small inductor may cause a failure at full load, but a larger inductor means a higher overload protection (OLP) load. It is recommended to select an inductor with the lowest value possible to supply the rated power.

The maximum power (P_{OMAX}) can be estimated with Equation (7) and Equation (8) for CCM and DCM, respectively:

$$P_{OMAX} = V_{OUT} \times (I_{PEAK} - \frac{V_{OUT} \times t_{MINOFF}}{2L}) \quad (7)$$

$$P_{OMAX} = \frac{1}{2} L \times I_{PEAK}^2 \times \frac{1}{t_{MINOFF}} \quad (8)$$

For mass production, consider tolerance on the parameters (e.g. peak current limitation and minimum off time).

Freewheeling Diode

The diode should be selected based on the maximum input voltage and peak current.

The freewheeling diode's reverse recovery can affect efficiency and circuit operation for CCM conditions. A diode such as the EGC10JH is recommended.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. The output voltage ripple can be calculated with Equation (9) and Equation (10) for CCM and DCM, respectively:

$$V_{CCM_RIPPLE} = \frac{\Delta I}{8 f_{SW} \times C_O} + \Delta I \times R_{ESR} \quad (9)$$

$$V_{DCM_RIPPLE} = \frac{I_O}{f_{SW} \times C_O} \times \left(\frac{I_{PEAK} - I_O}{I_{PEAK}} \right)^2 + I_{PEAK} \times R_{ESR} \quad (10)$$

To reduce the output voltage ripple, use ceramic, tantalum, or low-ESR electrolytic capacitors. A maximum 470μF capacitance is recommended in typical applications to avoid triggering SCP during start-up.

Feedback Resistors

The resistor divider determines the output voltage. Choose appropriate R1 and R2 values to maintain the feedback voltage at 2.55V. R2 should typically be between 5kΩ and 10kΩ. Avoid a large R2 value.

Feedback Capacitor

The feedback capacitor provides a sample and hold function. Small capacitors result in poor

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

regulation at light loads, and large capacitors affect the circuit operation. The optimal capacitor value can be estimated with Equation (11):

$$\frac{1}{2}\times\frac{V_{OUT}}{R1+R2}\times\frac{C_O}{I_{OUT}}\le C_{FB}\le\frac{V_{OUT}}{R1+R2}\times\frac{C_O}{I_{OUT}} \quad (11)$$

Dummy Load

A dummy load is required to maintain the load regulation. This ensures there is sufficient inductor energy to charge the sample and hold the capacitor to detect the output voltage. A 3mA dummy load is required; it can be adjusted according to the regulated voltage.

For applications that require a 30mW no-load consumption, there is a tradeoff between small no-load consumption and optimal no-load regulation. Use a Zener diode to reduce no-load consumption if no-load regulation is not vital for the application.

Auxiliary VCC Supply

For an application where V_O exceeds 7V, the MP171A can meet a 30mW no-load power requirement. To do this, the IC requires an external VCC supply to reduce overall power consumption (see Figure 7).

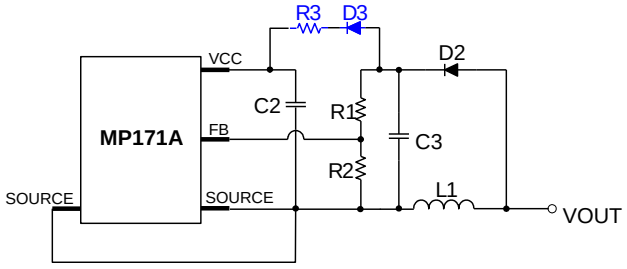


Figure 7: Auxiliary VCC Supply Circuit

This auxiliary VCC supply is derived from the resistor connected between C2 and C3. C3 should be greater than the recommendation (see the Feedback Capacitor section on page 14). D3 is used in case VCC interferes with FB. R3 is calculated using Equation (12):

$$R3\approx\frac{V_{OUT}-V_{FW}-5.8V}{I_S} \quad (12)$$

Where I_S is the VCC consumption under a no-load condition, and V_{FW} is the forward voltage drop of D3. R3 should be adjusted to meet the actual I_S, because it varies in different applications. In a particular configuration, I_S is measured at about 200μA.

Surge Performance

Choose an appropriate input capacitor value to obtain an efficient surge performance. Figure 8 shows the half-wave rectifier.

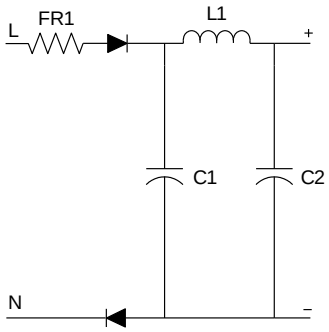


Figure 8: Half-Wave Rectifier

Table 2 shows the capacitance required under normal conditions for different surge voltages. In this example, FR1 is a 20Ω/2W fused resistor and L1 is 1mH.

Table 2: Recommended Capacitance

Surge Voltage	500V	1000V	2000V
C1	1μF	2.2μF	3.3μF
C2	1μF	2.2μF	3.3μF

Design Example

Table 3 shows a design example for the following application guideline specifications:

Table 3: Design Example

V_{IN}	85VAC to 265VAC
V_{OUT}	5V
I_{OUT}	50mA

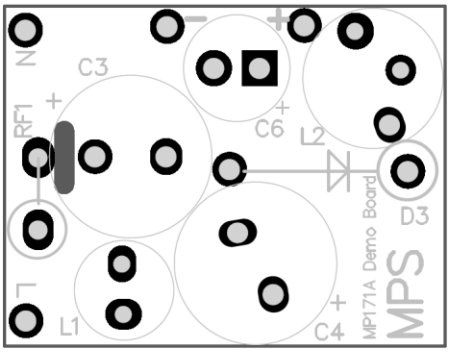
Figure 10 on page 17 shows a detailed application schematic. For the typical performance and circuit waveforms of the device, see the Typical Performance Characteristics section on page 7. Refer to the related evaluation board datasheets for additional information.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

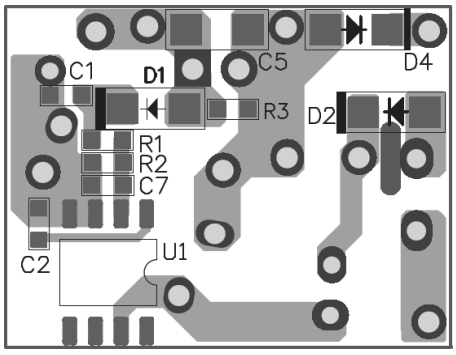
PCB Layout Guidelines

PCB layout is vital for stable operation, good EMI, and thermal performance. For the best results, refer to Figure 9 and follow the guidelines below:

1. Minimize the loop area formed by the input capacitor, IC, freewheeling diode, inductor, and output capacitor.
2. Place the power inductor away from the input filter.
3. Minimize the loop area to the inductor (see Figure 9).
4. Place a capacitor valued at several hundred pF between FB and SOURCE, as close to the IC as possible.
5. Connect the exposed pads or large copper area to DRAIN to improve thermal performance.



Top Layer



Bottom Layer

Figure 9: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

Figure 10 shows a typical application example of a 5V, 50mA, non-isolated power supply using the MP171A.

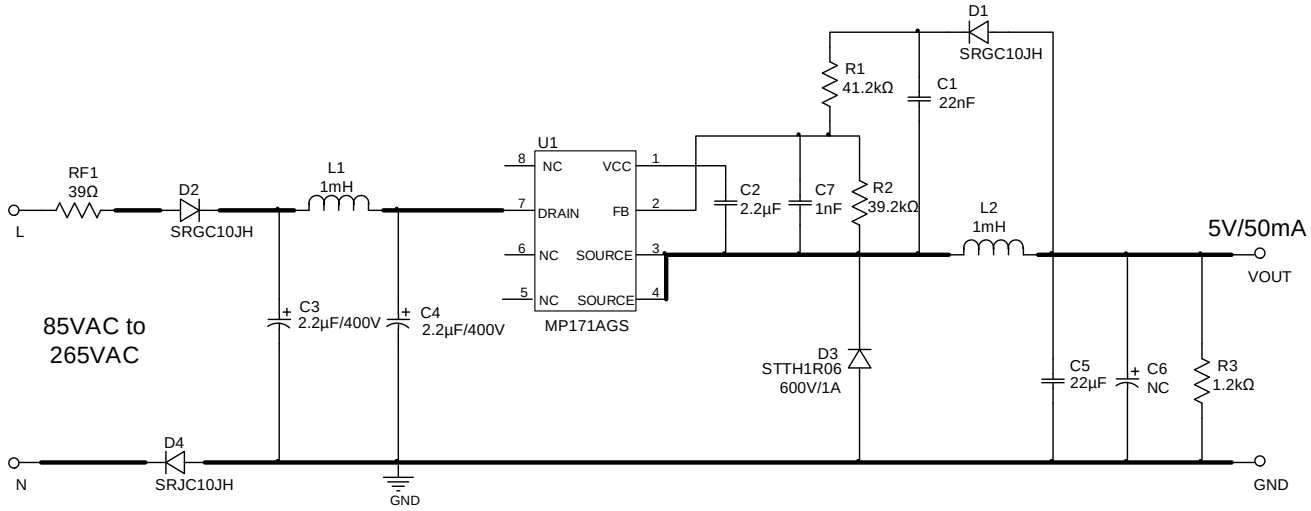
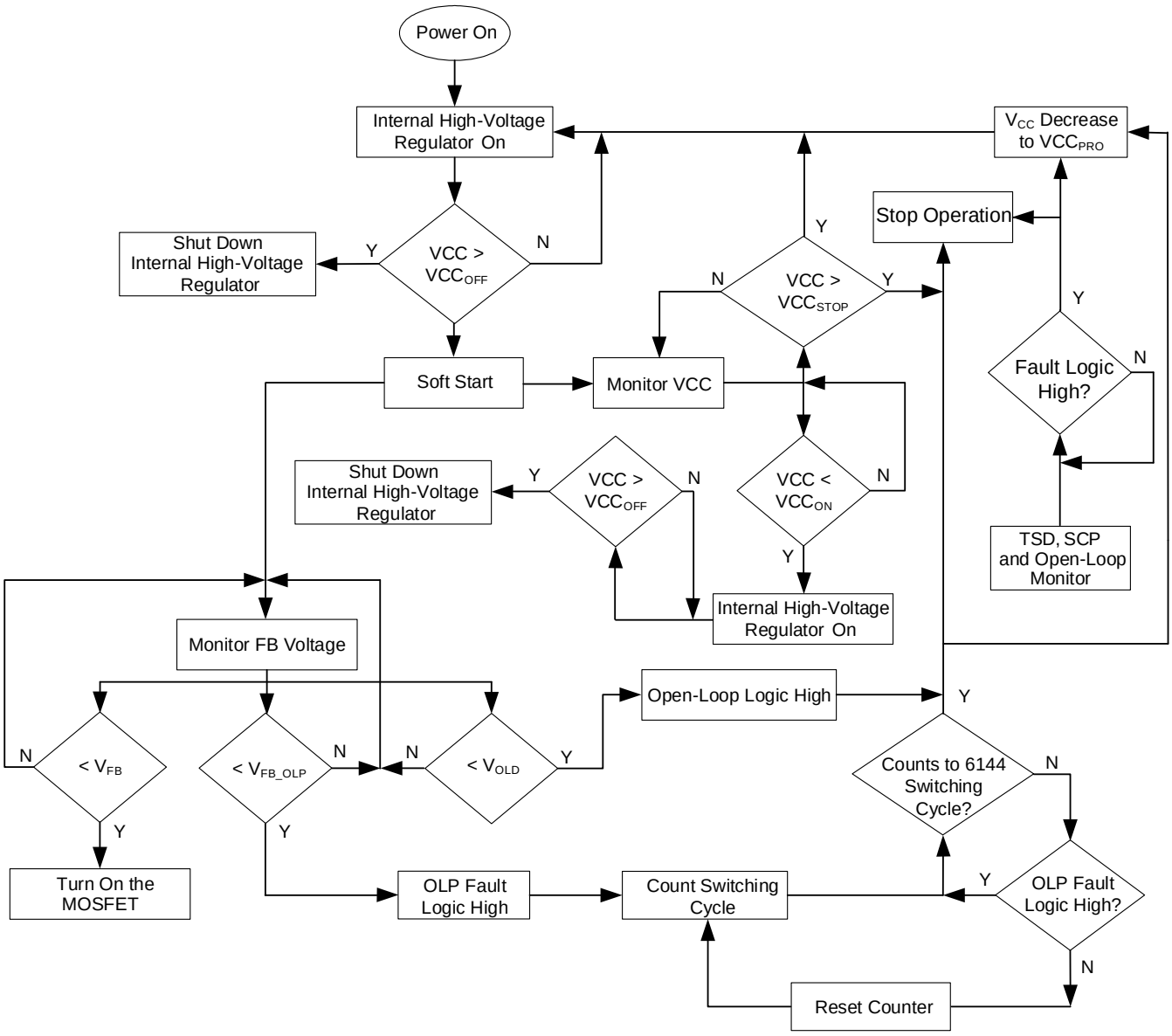


Figure 10: Typical Application at 5V, 50mA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

FLOWCHART



UVLO, SCP, OLP, OTP, and open-loop protections are auto-restart.

Figure 11: Control Flowchart

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

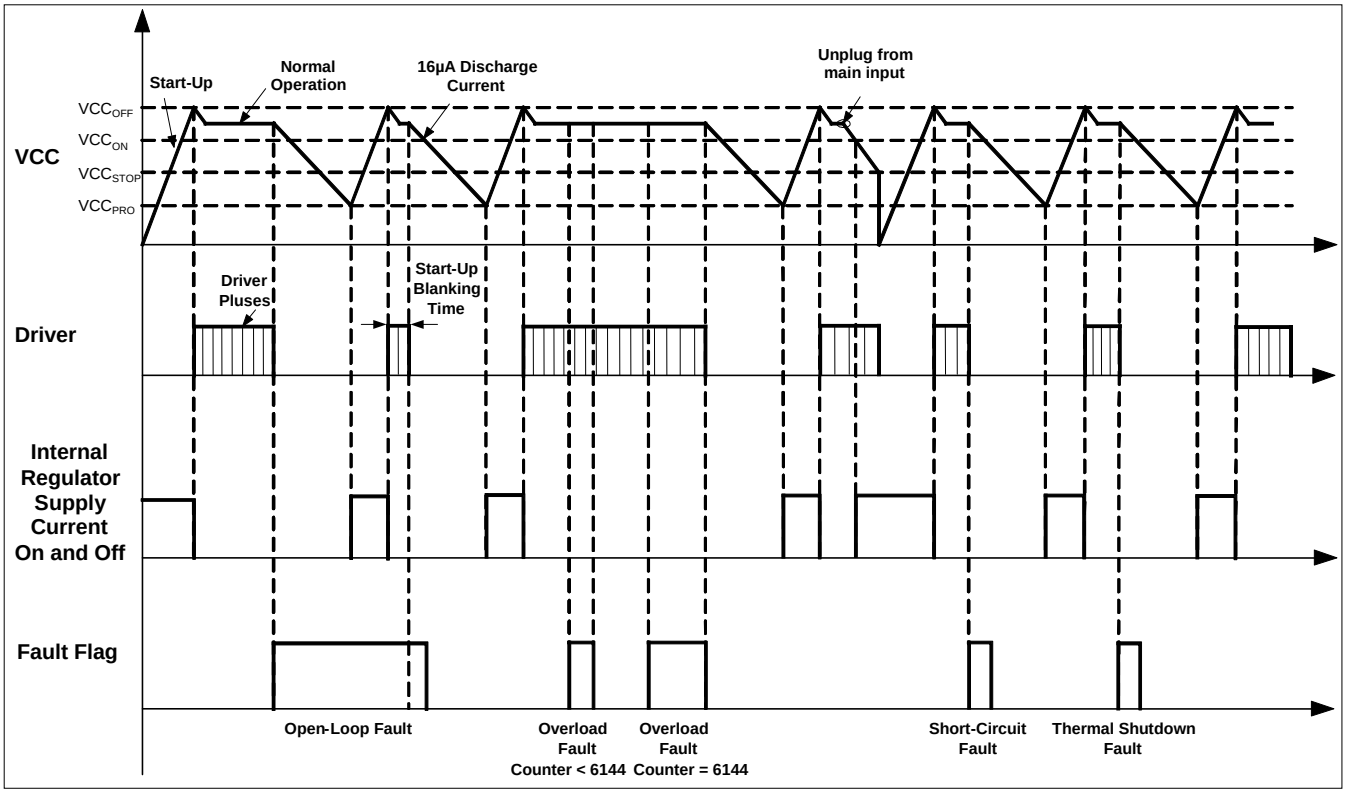
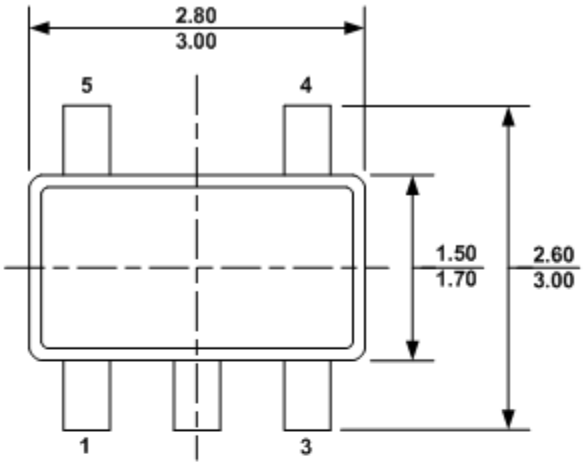


Figure 12: Signal Evolution in the Presence of a Fault

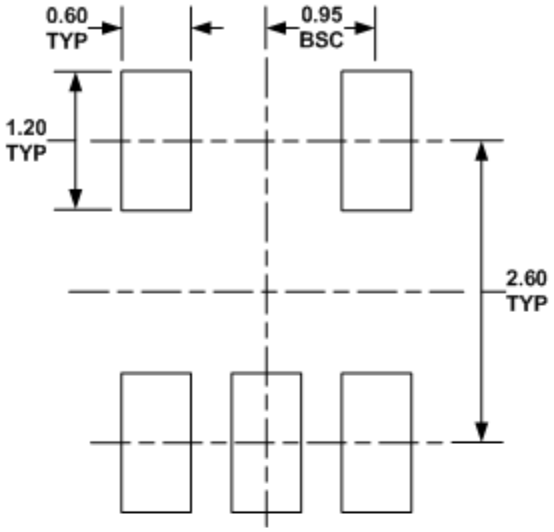
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE INFORMATION

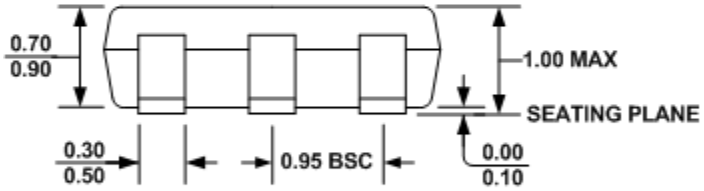
TSOT23-5



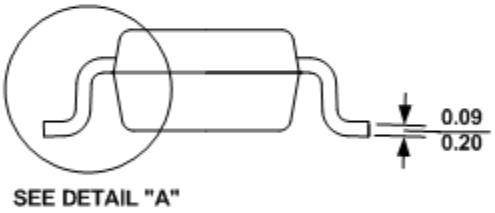
TOP VIEW



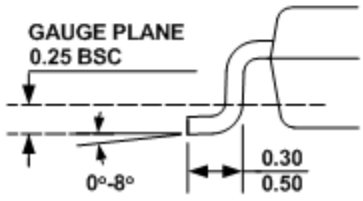
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

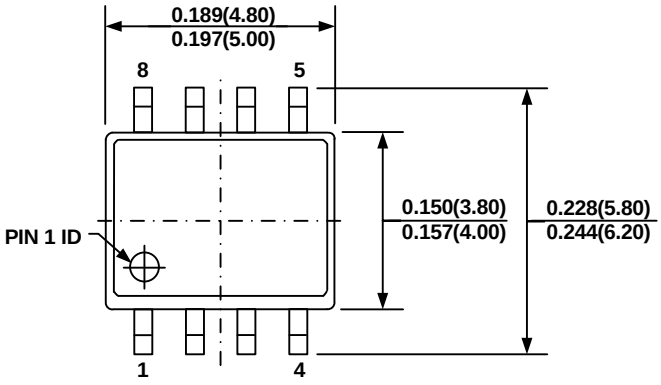
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

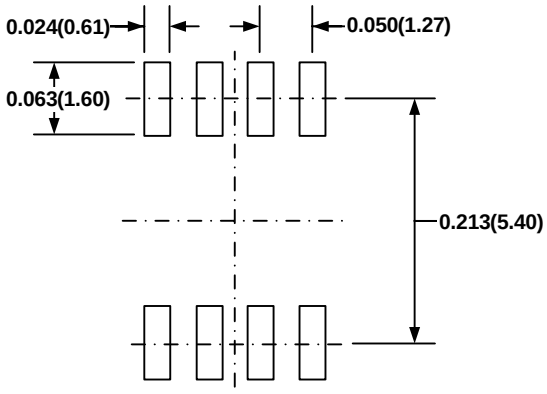
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE INFORMATION *(continued)*

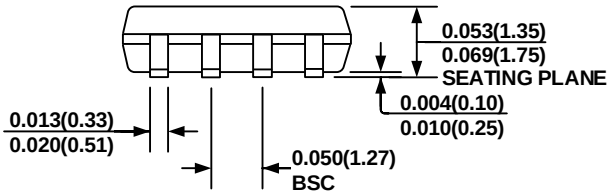
SOIC-8



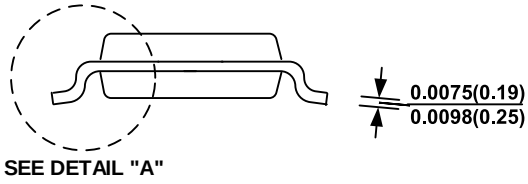
TOP VIEW



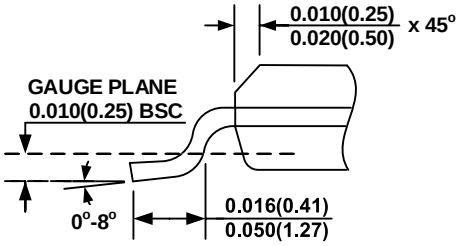
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



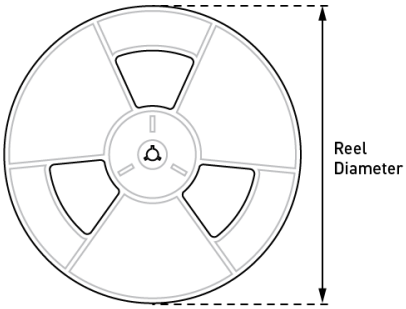
DETAIL "A"

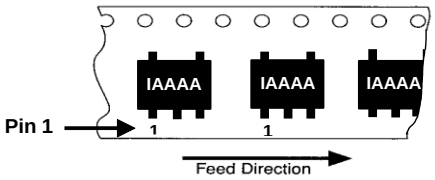
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

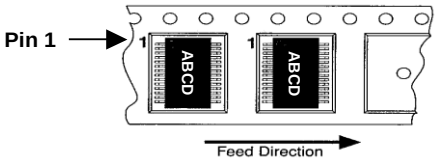
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

CARRIER INFORMATION





TSOT23-5



SOIC-8

Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP171AGJ-Z	TSOT23-5	3000	N/A	7in	8mm	4mm
MP171AGS-Z	SOIC-8	2500	100	13in	12mm	8mm

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.