MP1593

3A, 28V, 385kHz Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP1593 is a step-down regulator with an internal Power MOSFET. It achieves 3A of continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. An adjustable soft-start reduces the stress on the input source at startup. In shutdown mode the regulator draws 20μA of supply current.

The MP1593 requires a minimum number of readily available external components, providing a compact solution.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV1593DN-00A	2.1"X x 1.3"Y x 0.4"Z

FEATURES

- 3A Output Current
- Programmable Soft-Start
- 100mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20μA Shutdown Mode
- Fixed 385kHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75V to 28V Operating Input Range
- Output Adjustable from 1.22V
- Under-Voltage Lockout
- Available in 8-Pin SOIC Package

APPLICATIONS

- Distributed Power Systems
- Battery Chargers
- Pre-Regulator for Linear Regulators
- Flat Panel TVs
- Set-Top Boxes
- Cigarette Lighter Powered Devices
- DVD/PVR Devices

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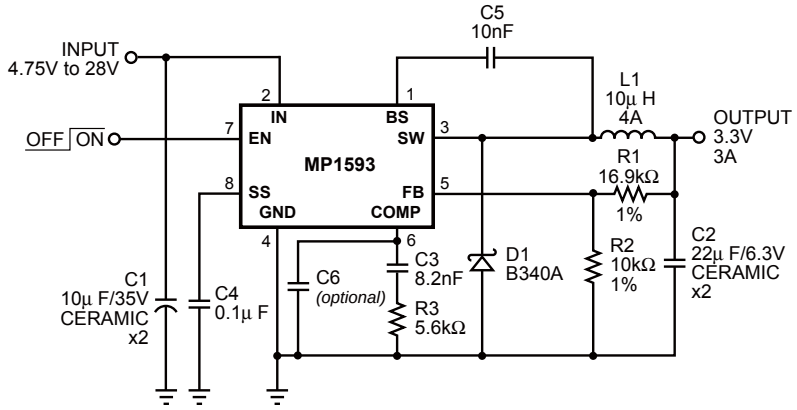
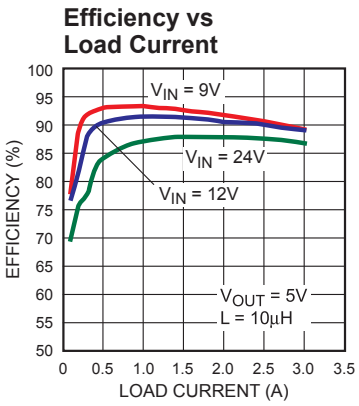
TYPICAL APPLICATION





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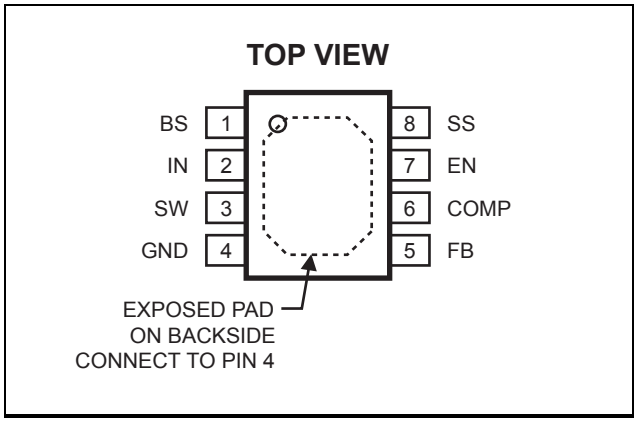
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP1593DN	SOIC8E	MP1593DN	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP1593DN–Z).
For RoHS Compliant packaging, add suffix –LF (e.g. MP1593DN–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} .....-0.3V to +30V
Switch Voltage V_{SW} .....-0.5V to V_{IN} + 0.3V
Boost Voltage V_{BS} .....V_{SW} – 0.3V to V_{SW} + 6V
All Other Pins .....-0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
.....2.5W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} .....4.75V to 28V
Operating Junct. Temp (T_J).....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
SOIC8E (Exposed Pad)	50	10	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown Supply Current		V_{EN} = 0V		20	30	μA
Supply Current		V_{EN} =3V, V_{FB} = 1.4V		1.0	1.2	mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 28V V_{COMP} < 2V	1.194	1.222	1.250	V
Error Amplifier Voltage Gain	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ±10μA	500	800	1120	μA/V
High-Side Switch On-Resistance	$R_{DS(ON)1}$			100	140	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)2}$			10		Ω
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V		0	10	μA
Current Limit			4.8	6.2	7.6	A
Current Sense to COMP Transconductance	G_{CS}			5.4		A/V
Oscillation Frequency	f_{OSC1}		335	385	435	kHz
Short Circuit Oscillation Frequency	f_{OSC2}	V_{FB} = 0V	25	45	60	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 1.0V		90		%
Minimum Duty Cycle	D_{MIN}	V_{FB} = 1.5V			0	%
EN Rising Threshold			2.05	2.5	2.95	V
EN Threshold Hysteresis				150		mV
Enable Pull Up Current		V_{EN} = 0V	1.0	1.7	2.5	μA
Under-Voltage Lockout Threshold		V_{IN} Rising	3.75	4.05	4.35	V
Under-Voltage Lockout Threshold Hysteresis				210		mV
Soft-Start Period		C_{SS} = 0.1μF		10		ms
Thermal Shutdown				160		°C

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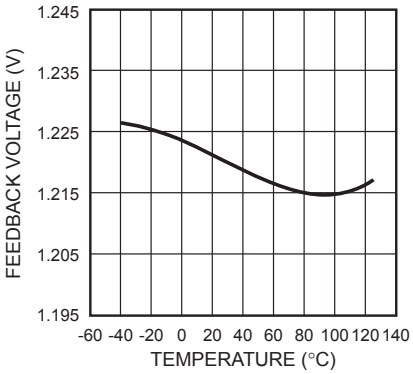
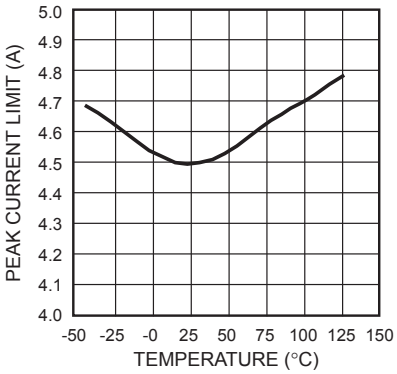
TYPICAL PERFORMANCE CHARACTERISTICS

Refer to Typical Application Schematic on Page 1

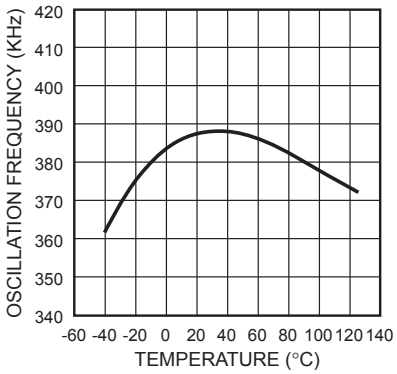
Feedback Voltage vs Temperature



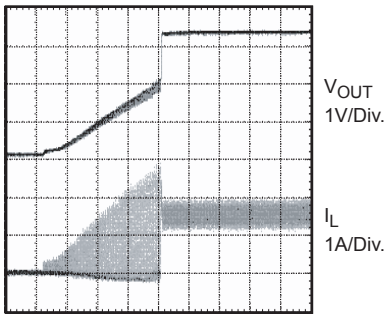
Peak Current Limit vs Temperature



Oscillation Frequency vs Temperature

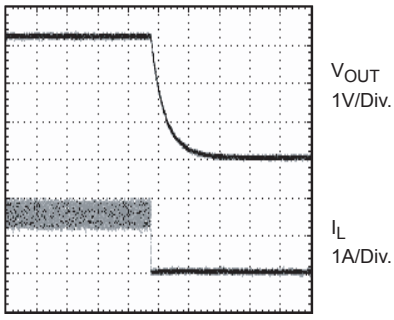


Soft-Start Waveforms



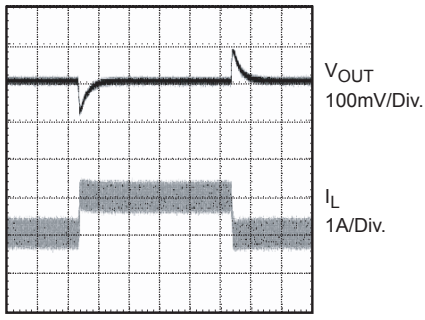
V_{IN} = 12V, V_{OUT} = 3.3V, R_{LOAD} = 2Ω

Turn Off Waveforms



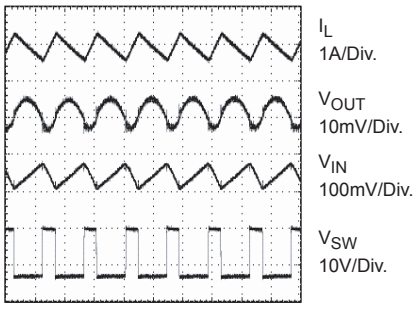
V_{IN} = 12V, V_{OUT} = 3.3V, R_{LOAD} = 2Ω

Load Transient Waveforms



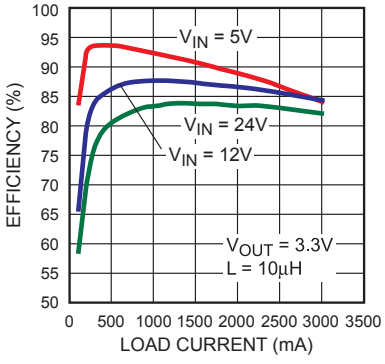
V_{IN} = 12V, V_{OUT} = 3.3V, 1A - 2A STEP

Switching Waveforms

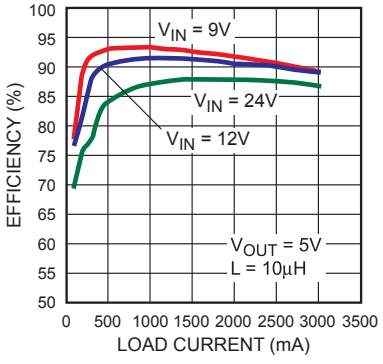


V_{IN} = 12V, V_{OUT} = 3.3V, R_{LOAD} = 2Ω

Efficiency vs Load Current



Efficiency vs Load Current



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PIN FUNCTIONS

Pin #	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 10nF or greater capacitor from SW to BS to power the high-side switch.
2	IN	Power Input. IN supplies power to the IC. Drive IN with a 4.75V to 28V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor.*
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground. Note: Connect the exposed pad to Pin 4.
5	FB	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider from the output voltage to ground. The feedback threshold is 1.222V. See *Setting the Output Voltage.*
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required. See *Compensation.*
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. An Under-Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from V_{IN} to GND. For complete low current shutdown the EN pin voltage needs to be less than 1.5V. For automatic startup leave EN disconnected.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 10ms. To disable the soft-start feature, leave SS disconnected.

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OPERATION

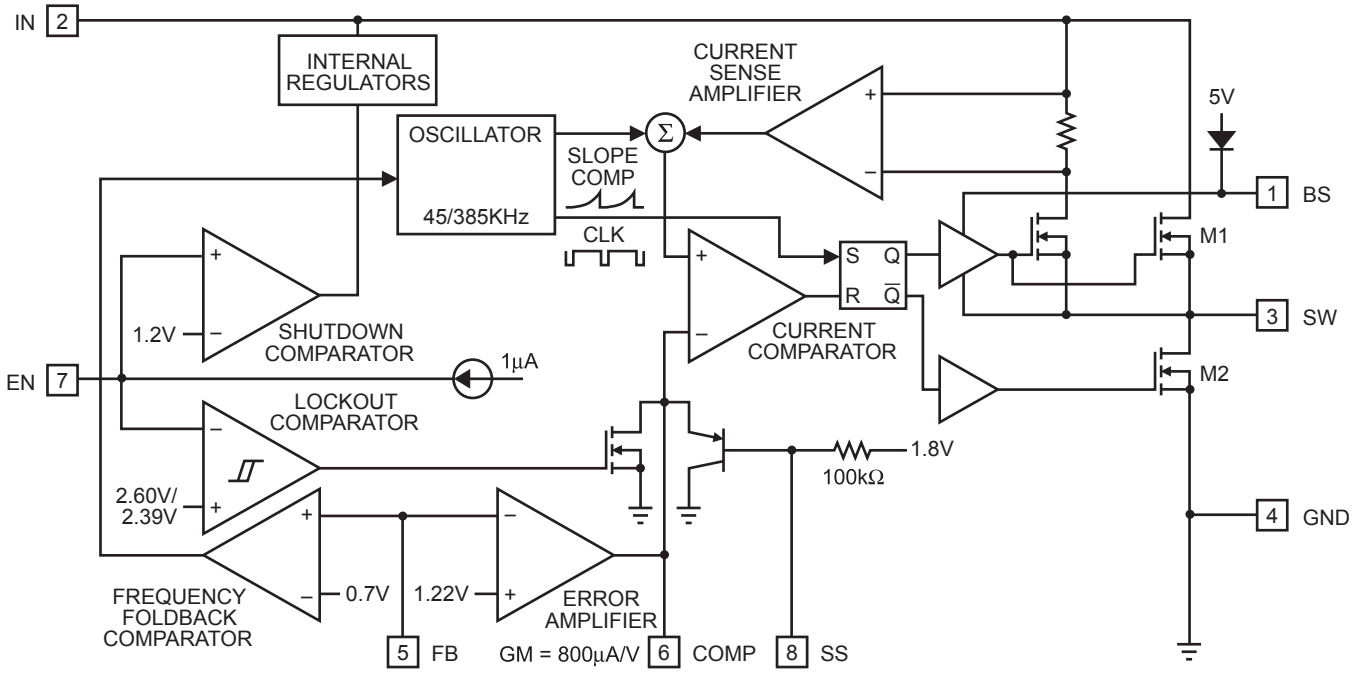

Figure 1—Functional Block Diagram

The MP1593 is a current-mode step-down regulator. It regulates input voltages from 4.75V to 28V down to an output voltage as low as 1.22V, and is able to supply up to 3A of continuous load current.

The MP1593 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal error amplifier. The output current of the transconductance error amplifier is presented at COMP where a network compensates the regulation control system. The voltage at COMP is compared to the internally measured switch current to control the output voltage.

The converter uses an internal N-Channel MOSFET switch to step-down the input voltage to the regulated output voltage. Since the MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS drives the gate. The capacitor is internally charged when SW is low.

An internal 10Ω switch from SW to GND is used to insure that SW is pulled to GND when it is low to fully charge the BS capacitor.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to the FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Thus the output voltage is:

$$V_{OUT} = 1.22 \times \frac{R1+R2}{R2}$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using that value, R1 is determined by:

$$R1 = 8.18 \times (V_{OUT} - 1.22)(k\Omega)$$

For a 3.3V output voltage, R2 is 10kΩ and R1 is 17kΩ.

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, larger value inductors will have larger physical size, higher series resistance and/or lower saturation current. A good standard for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{IN} is the input voltage, f_S is the switching frequency and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Table 1 lists a number of suitable inductors from various manufacturers. The choice of which inductor to use mainly depends on the price vs. size requirements and any EMI requirement.

Table 1—Inductor Selection Guide

Vendor/ Model	Core Type	Core Material	Package Dimensions (mm)		
			W	L	H
Sumida					
CR75	Open	Ferrite	7.0	7.8	5.5
CDH74	Open	Ferrite	7.3	8.0	5.2
CDRH5D28	Shielded	Ferrite	5.5	5.7	5.5
CDRH5D28	Shielded	Ferrite	5.5	5.7	5.5
CDRH6D28	Shielded	Ferrite	6.7	6.7	3.0
CDRH104R	Shielded	Ferrite	10.1	10.0	3.0
Toko					
D53LC Type A	Shielded	Ferrite	5.0	5.0	3.0
D75C	Shielded	Ferrite	7.6	7.6	5.1
D104C	Shielded	Ferrite	10.0	10.0	4.3
D10FL	Open	Ferrite	9.7	1.5	4.0
Coilcraft					
DO3308	Open	Ferrite	9.4	13.0	3.0
DO3316	Open	Ferrite	9.4	13.0	5.1

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Output Rectifier Diode

The output rectifier diode supplies current to the inductor when the high-side switch is off. Use a Schottky diode to reduce losses due to diode forward voltage and recovery times.

Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current. Table 2 lists example Schottky diodes and manufacturers.

Table 2—Diode Selection Guide

Diode	Voltage/Current Rating	Manufacture
SK33	30V, 3A	Diodes Inc.
SK34	40V, 3A	Diodes Inc.
B330	30V, 3A	Diodes Inc.
B340	40V, 3A	Diodes Inc.
MBRS330	30V, 3A	On Semiconductor
MBRS340	40V, 3A	On Semiconductor

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor (i.e. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum or low ESR electrolytic capacitors are recommended.

Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value, C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, which is the main cause of the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP1593 can be optimized for a wide range of capacitance and ESR values.

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Compensation Components

The MP1593 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of error amplifier, while the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case (as shown in Figure 3), a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency (where the feedback loop has unity gain) is important.

Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good standard is to set the crossover frequency to approximately one-tenth of the switching frequency. The switching frequency for the MP1593 is 385KHz, so the desired crossover frequency is around 38KHz.

Table 3 lists the typical values of compensation components for some standard output voltages with various output capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability at given conditions.

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Table 3—Compensation Values for Typical Output Voltage/Capacitor Combinations

V_{OUT}	L	C2	R3	C3	C6
1.8V	4.7μH	100μF Ceramic	5.6kΩ	3.3nF	None
2.5V	4.7-6.8μH	47μF Ceramic	3.9kΩ	5.6nF	None
3.3V	6.8-10μH	22μFx2 Ceramic	5.6kΩ	8.2nF	None
5V	10-15μH	22μFx2 Ceramic	7.5kΩ	10nF	None
12V	15-22μH	22μFx2 Ceramic	10kΩ	3.3nF	None
1.8	4.7μH	100μF SP-CAP	5.6kΩ	3.3nF	100pF
2.5V	4.7-6.8μH	47μF SP-CAP	4.7kΩ	5.6nF	None
3.3V	6.8-10μH	47μF SP-CAP	6.8kΩ	10nF	None
5V	10-15μH	47μF SP CAP	10kΩ	10nF	None
2.5V	4.7-6.8μH	560μF Al. 30mΩ ESR	10kΩ	5.6nF	1.5nF
3.3V	6.8-10μH	560μF Al 30mΩ ESR	10kΩ	8.2nF	1.5nF
5V	10-15μH	470μF Al. 30mΩ ESR	15kΩ	5.6nF	1nF
12V	15-22μH	220μF Al. 30mΩ ESR	15kΩ	4.7nF	390pF

To optimize the compensation components for conditions not listed in Table 3, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency. Determine R3 by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency (which typically has a value no higher than 38KHz).

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, below one forth of the crossover frequency provides sufficient phase margin.

Determine C3 by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

Where R3 is the compensation resistor value.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the 385kHz switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

Where C2 is the output capacitance value, R_{ESR} is the ESR value of the output capacitor and f_S is the switching frequency. If this is the case, then add the second compensation capacitor (C6) to set the pole f_{P3} at the location of the ESR zero. Determine C6 by the equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

Where C2 is the output capacitance value, R_{ESR} is the ESR value of the output capacitor and R3 is the compensation resistor.

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure2 and 3 for references.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and low-side MOSFET/schottky diode.
2) Keep the connection of low-side MOSFET/schottky diode between SW pin and input power ground as short and wide as possible.
3) Bypass ceramic capacitors are suggested to be put close to the V_{IN} and V_{CC} Pin.
4) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

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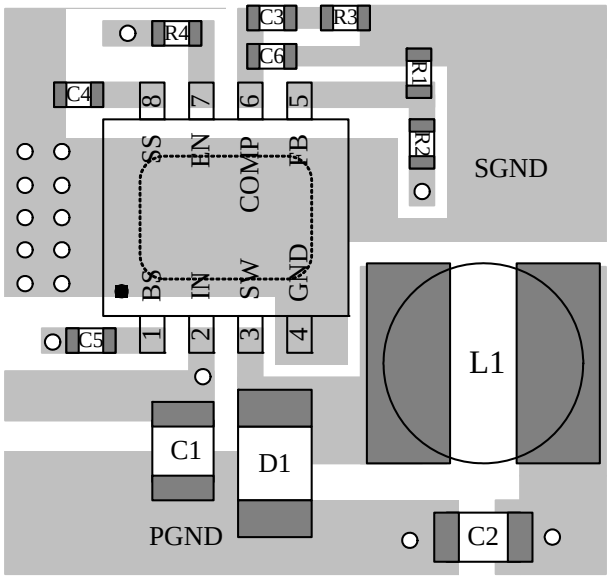
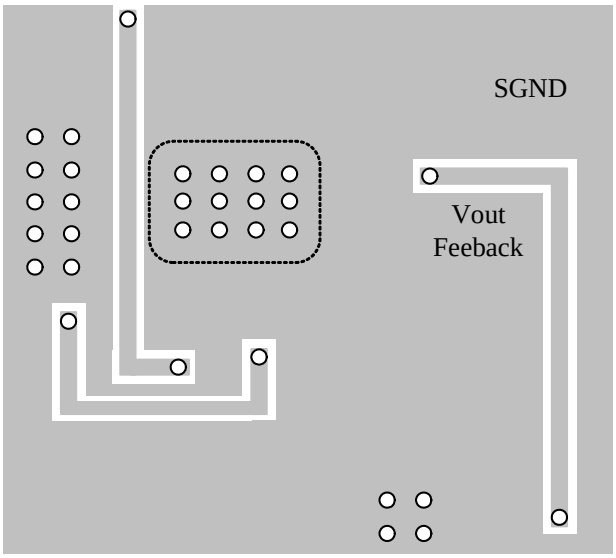
5) Route SW away from sensitive analog areas such as FB.

6) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability. For single layer, do not solder exposed pad of the IC.



TOP Layer



Bottom Layer

Figure 2—PCB Layout (Double Layer)

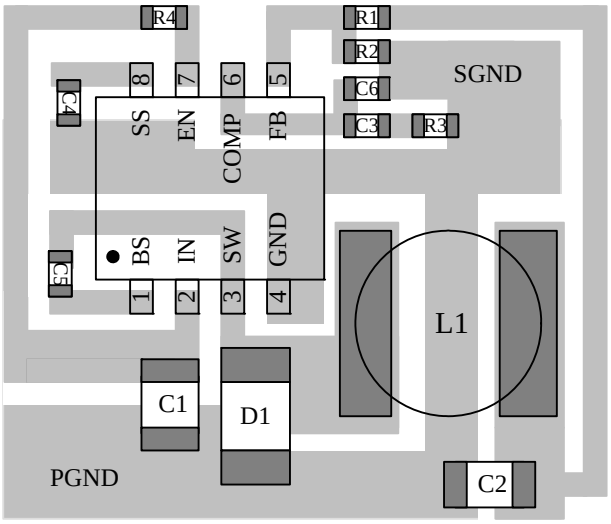


Figure 3—PCB Layout (Single Layer)

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Fig.4

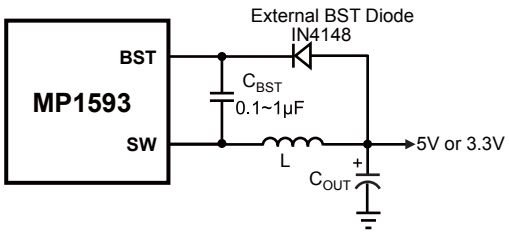


Figure 4—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

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TYPICAL APPLICATION CIRCUITS

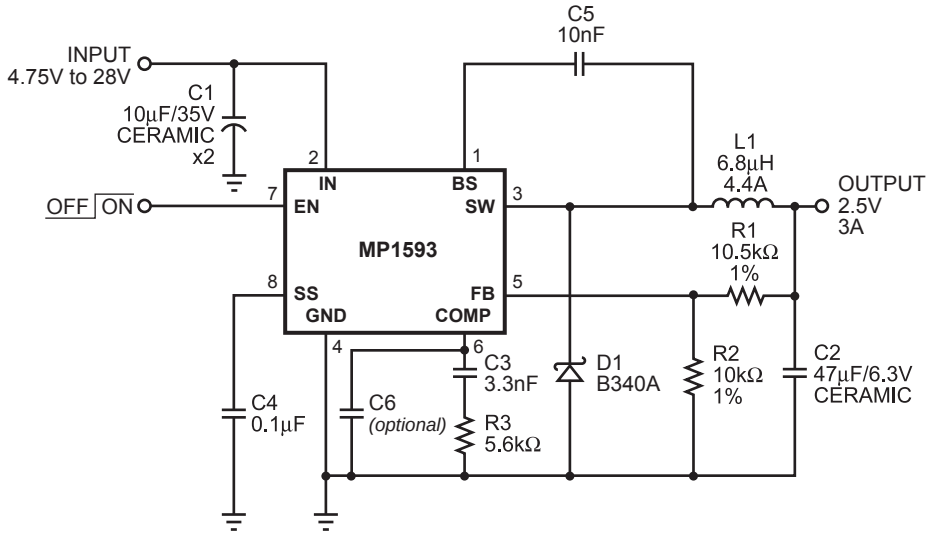

Figure 5—MP1593 with AVX 47µF, 6.3V Ceramic Output Capacitor

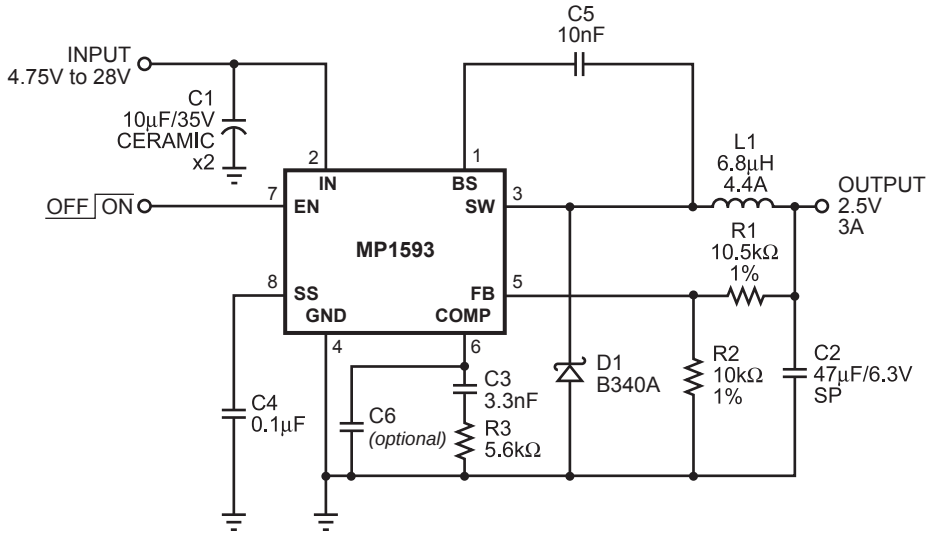

Figure 6—MP1593 with Panasonic 47µF, 6.3V Special Polymer Output Capacitor

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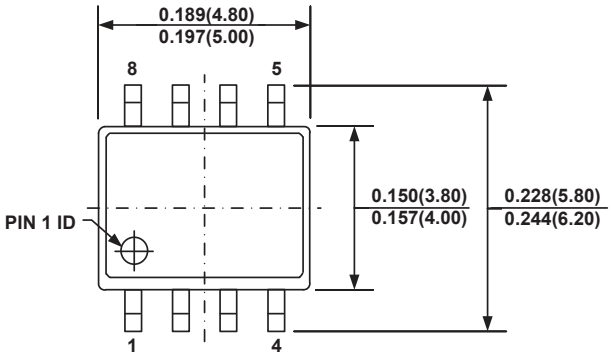
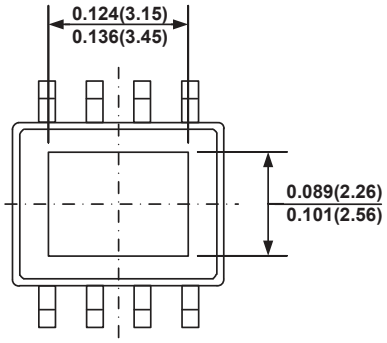
PACKAGE INFORMATION

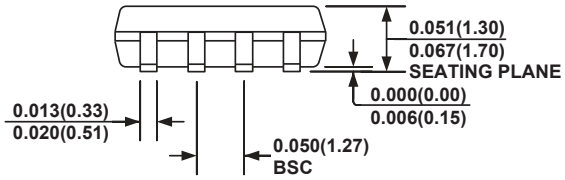
SOIC8E (EXPOSED PAD)



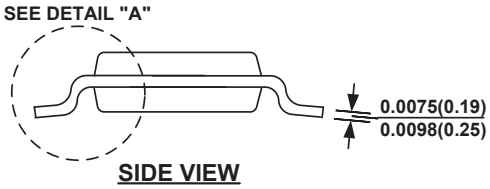
TOP VIEW



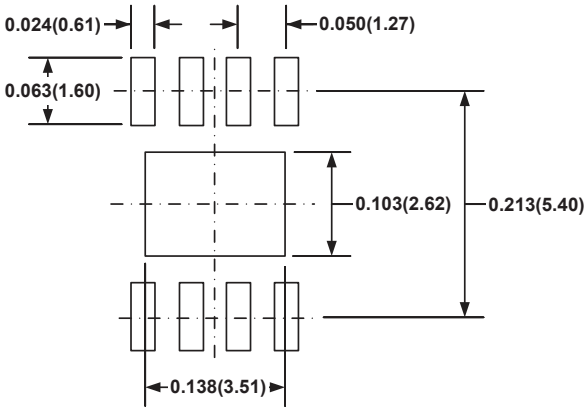
BOTTOM VIEW



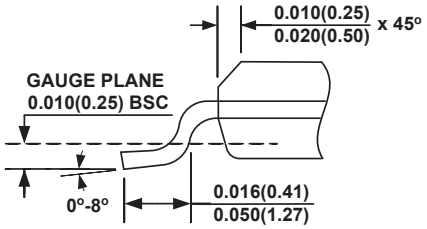
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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