MP158

Small, Energy-Efficient, Off-line Regulator 30mW No-Load Power Consumption

The Future of Analog IC Technology

DESCRIPTION

MP158 is a primary-side regulator that provides accurate constant voltage (CV) regulation without opto-coupler. It supports Buck, Buck-Boost, Boost and Flyback topologies. It has an integrated 500V MOSFET to simplify the structure and reduce costs. These features make it an ideal regulator for off-line low power applications, such as home appliances and standby power.

MP158 is a green-mode-operation regulator. Both the peak current and switching frequency decrease as the load decreases. This feature provides excellent efficiency at light load, thus improving the overall average efficiency.

MP158 features various protections, including thermal shutdown (TSD), VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), and open loop protection.

MP158 is available in small TSOT23-5 package and SOIC8 package.

FEATURES

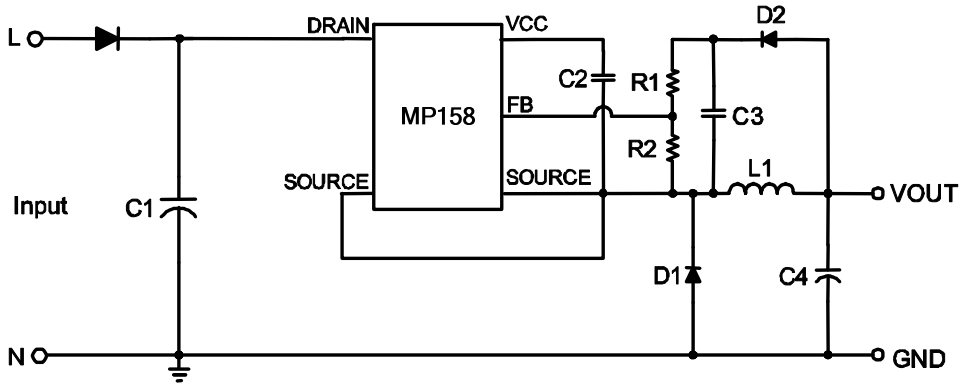
- Primary-side constant voltage (CV) control, supporting Buck, Buck-Boost, Boost and Flyback topologies
- Integrated 500V MOSFET and current source
- <30mW no-load power consumption
- Up to 2W output power
- Maximum DCM output current less than 40mA
- Maximum CCM output current less than 70mA
- Low VCC Operating Current
- Frequency foldback
- Limited maximum frequency
- Peak-current compression
- Internally biased VCC
- Thermal shutdown (auto restart)
- VCC under voltage lockout with hysteresis
- Timer based over-load protection.
- Short-circuit protection
- Open-loop protection

APPLICATIONS

- Home appliances, white goods and consumer electronics
- Industrial controls
- Standby power

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are Registered Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP158GJ	TSOT23-5	*See Below*
MP158GS	SOIC-8	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP158GJ–Z);

TOP MARKING

|AKHY

AKH: product code of MP158GJ;
Y: year code;

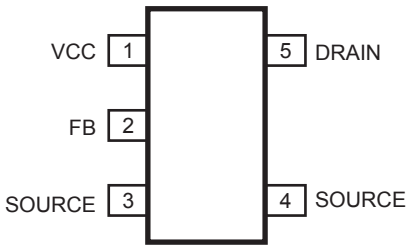
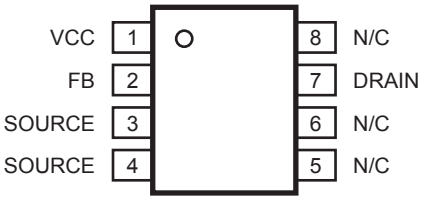
TOP MARKING

MP158
LLLLLLLL
MPSYWW

MP158: part number:
LLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
TSOT23-5	SOIC-8

ABSOLUTE MAXIMUM RATINGS (1)

Drain to source ..... -0.3V to 500V
All other pins..... -0.3V to 6.5V
Continuous Power Dissipation ... (T_A = +25°C)(2)
TSOT23-5.....1W
SOIC8.....1W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-60°C to +150°C
ESD Capability Human Body Mode 3.5kV
ESD Charged Device Model
TSOT23-5.....1.75kV
SOIC8.....2.0kV

Recommended Operating Conditions (3)

Operating Junction Temp. (T_J). -40°C to +125°C
Operating VCC range ..... 5.3V to 5.6V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-5	100	55	°C/W
SOIC-8	96	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowance continuous power dissipation at any ambient temperature is calculated by PD(MAX)=(TJ(MAX)-TA)/θ_{JA}. Exceeding the maximum allowance power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

VCC = 5.8V, T_J=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-up Current Source and Internal MOSFET (Drain Pin)						
Internal regulator supply current	$I_{regulator}$	VCC=4V;V_{Drain}=100V	2.2	3.5	4.8	mA
Drain pin leakage current	I_{Leak}	V_{Drain}=400V		10	15	μA
Breakdown Voltage	$V_{(BR)DSS}$		500			V
ON resistance	R_{on}			20		Ω
Supply Voltage Management (VCC Pin)						
VCC level (increasing) where the internal regulator stops	VCC_{OFF}		5.3	5.6	5.95	V
VCC level (decreasing) where the internal regulator turns on	VCC_{ON}		5.1	5.3	5.7	V
VCC regulator on and off hysteresis			110	250		mV
VCC level (decreasing) where the IC stops	VCC_{stop}		3	3.4	3.7	V
VCC level (decreasing) where the protection phase ends	VCC_{pro}		2	2.4	2.8	V
Internal IC consumption	I_{CC}	VCC=5.5V, f_s=50kHz, D=47%			600	μA
Internal IC consumption (No switching)	I_{CC}	VCC=5.5V			165	uA
Internal IC consumption, latch-off phase	$I_{CCLATCH}$	VCC=5.3V		16		μA
Internal Current Sense						
Peak current limit	I_{Limit}	T_J=25°C	83	101	125	mA
Leading-edge blanking	τ_{LEB1}			350		ns
SCP threshold	I_{SCP}	T_J=25°C	150	220	290	mA
Leading-edge blanking for SCP(1)	τ_{LEB2}			180		ns
Feedback Input (FB Pin)						
Minimum off time	τ_{minoff}		7.4	9.4	11.7	μs
Maximum on time	τ_{maxon}		7.9	10.4	13.1	μs
Primary MOSFET feedback turn-on threshold	V_{FB}		2.45	2.55	2.65	V
OLP feedback trigger threshold	$V_{FB\ OLP}$		1.6	1.7	1.85	V
OLP delay time	τ_{OLP}	f_s=50kHz		120		ms
Open-loop detection	V_{OLD}			60		mV
Thermal Shutdown						
Thermal shutdown threshold(1)				150		°C
Thermal shutdown recovery hysteresis(1)				30		°C

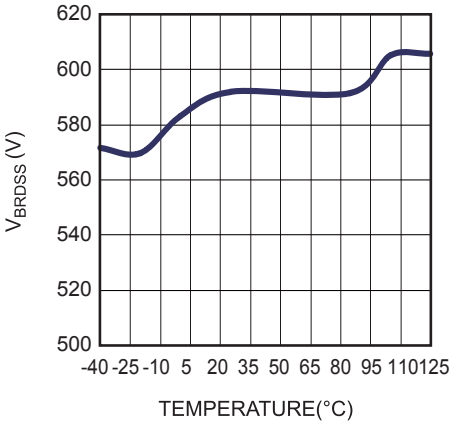
Notes:

1) This parameter is guaranteed by design.

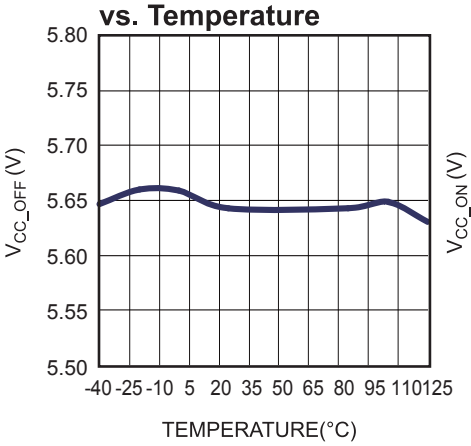
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

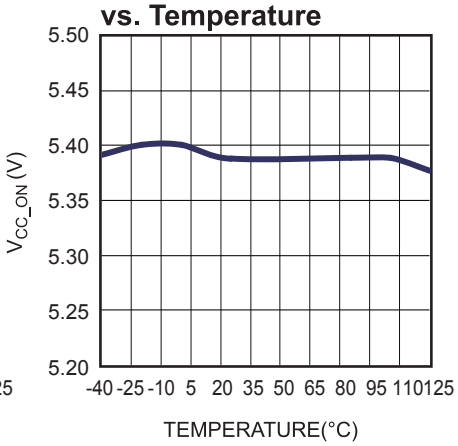
Breakdwon Voltage vs. Temperature



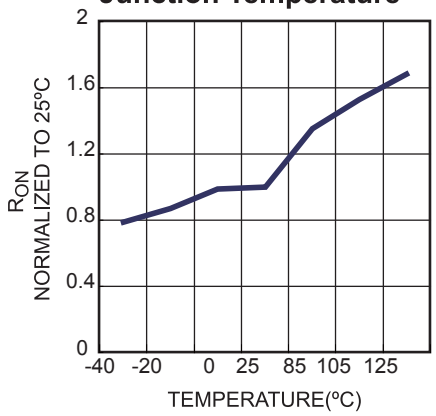
V_{CC} Increasing Level at which the Internal Regulator Stops vs. Temperature



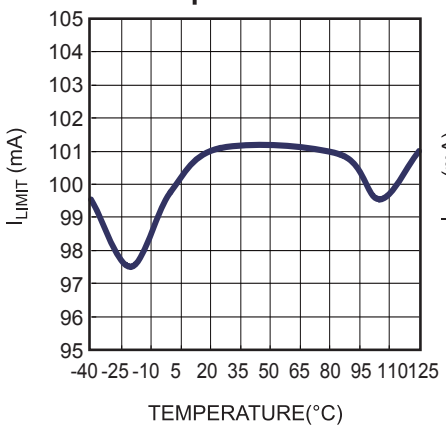
V_{CC} Increasing Level at which the Internal Regulator Turns On vs. Temperature



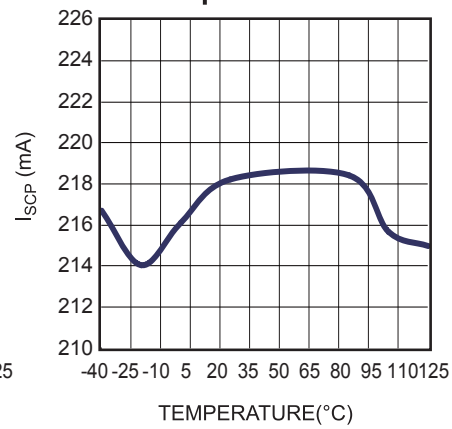
On-State Resistance vs. Junction Temperature



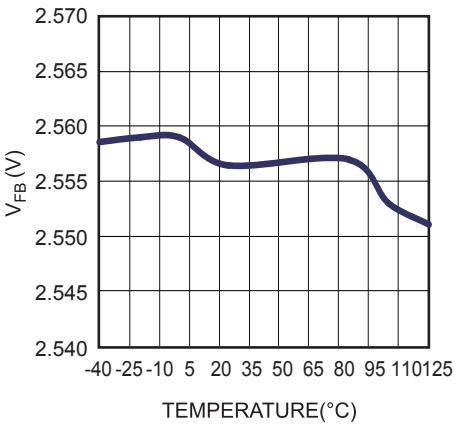
Peak Current Limit vs. Temperature



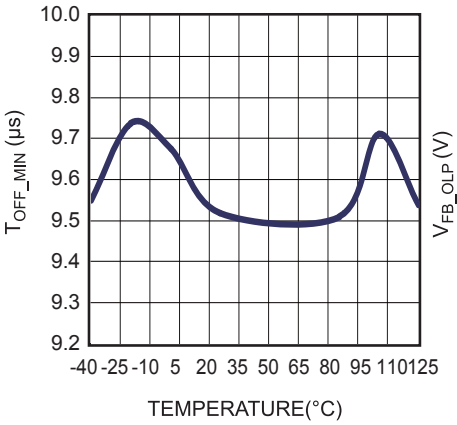
SCP Point vs. Temperature



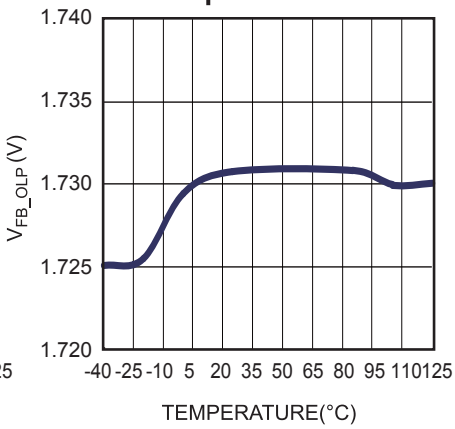
Feadback Voltage vs. Temperature



Minimum Off Time vs. Temperature



Over Load Protection Triggering Thershold vs. Temperature

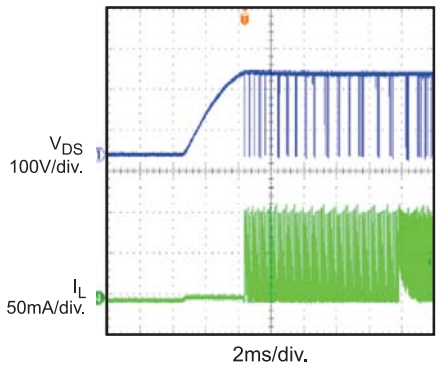


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

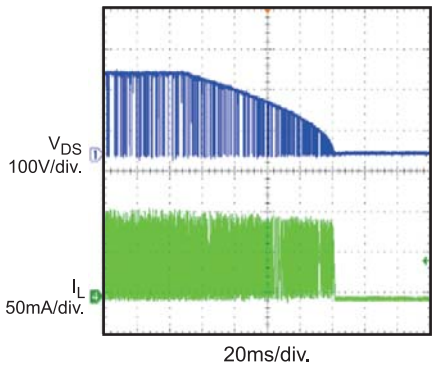
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 145VAC, V_{OUT} = 4V, I_{OUT} = 50mA, L = 1mH, C_{OUT} = 10µF, T_A = +25°C, unless otherwise noted.

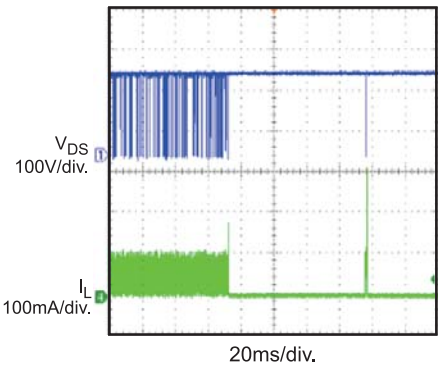
Input Power Start Up



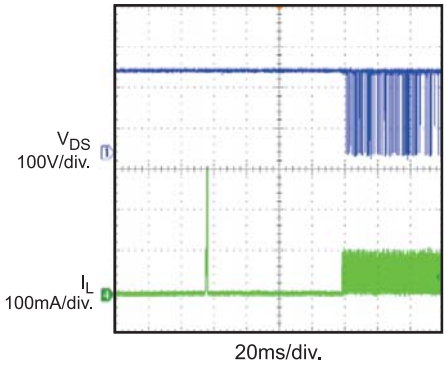
Input Power Shut Down



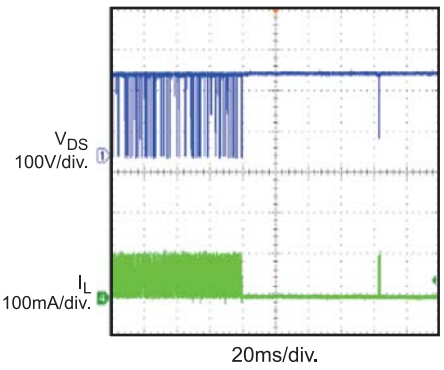
SCP Entry



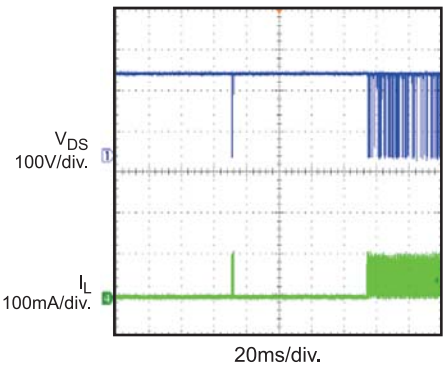
SCP Recovery



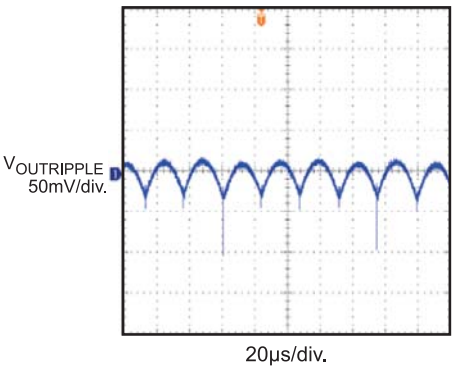
Open Loop Entry



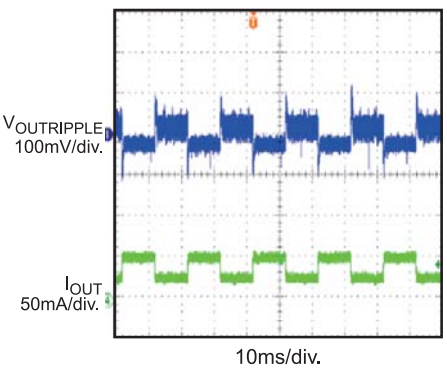
Open Loop Recovery



Output Voltage Ripple



Load Transient



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin # TSOT23-5	Pin # SOIC-8	Name	Description
1	1	VCC	Control circuit power supply.
2	2	FB	Regulator feedback.
3,4	3,4	SOURCE	Internal power MOSFET source. Ground reference for VCC and FB pins.
5	7	DRAIN	Internal power MOSFET drain. High-voltage current source input.
	5,6,8	N/C	Not connected.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

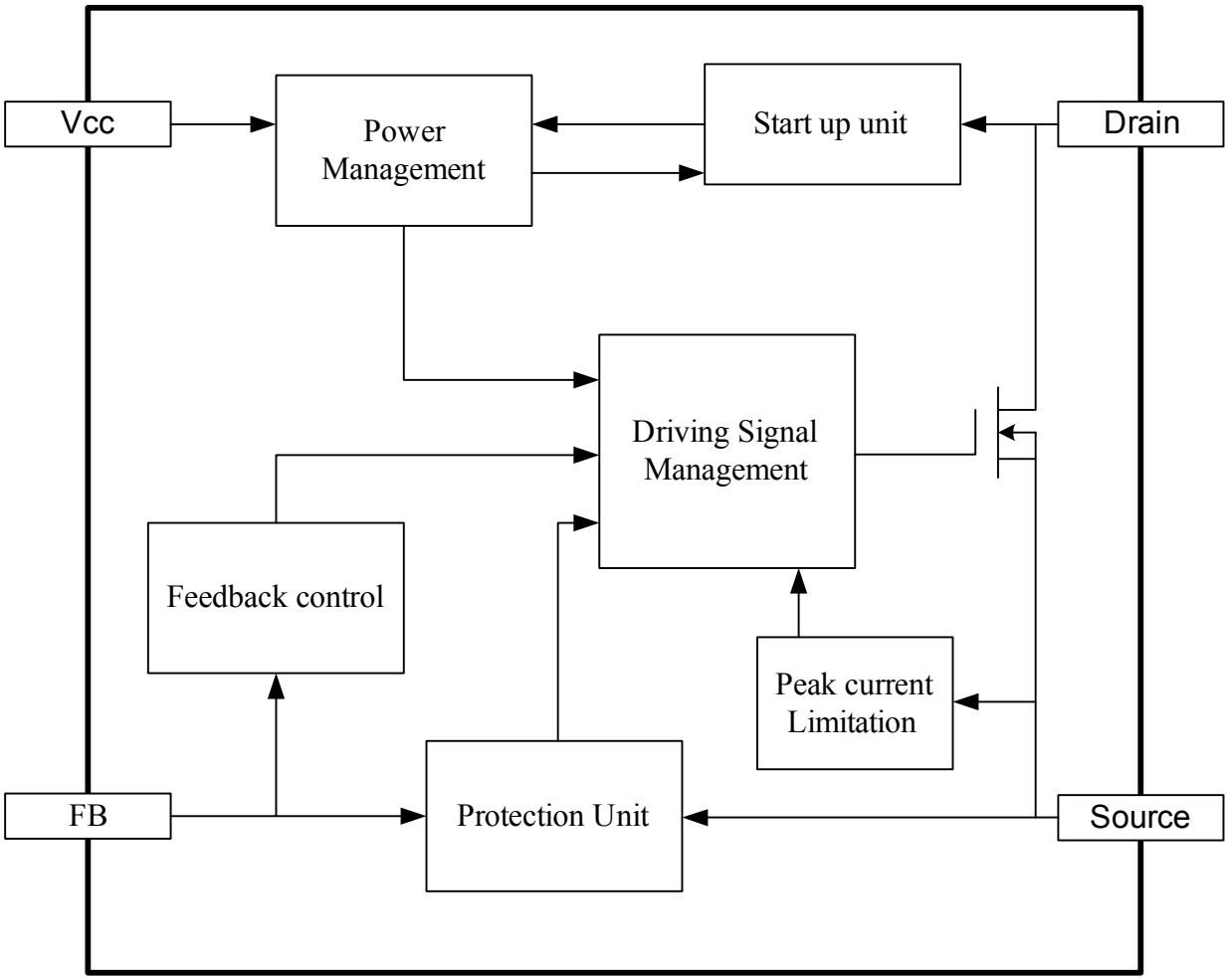


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

OPERATION

MP158 is a green-mode-operation regulator: the peak current and the switching frequency both decrease with a decreasing load. As a result, it offers excellent light-load efficiency, and improves average efficiency. The typical application diagram shows the regulator operates with minimum external components. It incorporates multiple features as described in the following sections.

Start-Up and Under-Voltage Lockout

The internal high-voltage regulator self-supplies the IC from Drain pin. When VCC voltage reaches 5.6V, the IC starts switching and the internal high voltage regulator turns off. The internal high-voltage regulator turns on to charge the external VCC capacitor when the VCC voltage falls below 5.3V. A small capacitor (in the low μF range) can maintain the VCC voltage and thus lower the capacitor cost.

The IC stops operation when VCC voltage drops blow 3.4V.

Under fault conditions—such as OLP, SCP, and OTP—the IC stops switching and an internal current source (~16μA) discharges the VCC capacitor. The internal high-voltage regulator will not charge the VCC capacitor until the VCC voltage drops below 2.4V. The restart time can be estimated using the following equation,

$$\tau_{restart} = C_{VCC} \times \frac{V_{CC} - 2.4V}{16\mu A} + C_{VCC} \times \frac{5.6V - 2.4V}{3.5mA}$$

Figure 2 shows the typical waveforms with VCC under-voltage lockout.

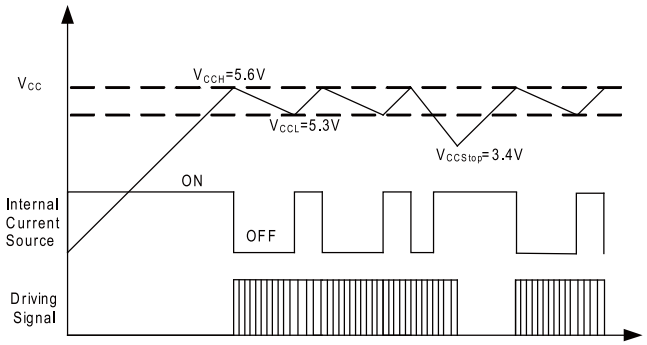


Figure 2: VCC Under-Voltage Lockout

Soft-Start

The IC stops operation when VCC voltage drops blow 3.4V and starts operation when VCC charges to 5.6V. Every time when the chip starts operation there is a Soft-Start period. The soft-start prevents the inductor current from overshooting by limiting the minimum off time.

MP158 adopts a 2 phase minimum off-time limit soft-start. Each soft-start phase retains 128 switching cycles. During soft-start, off-time limit gradually shortens from 72μs to 22.5μs and finally to the 9μs normal operation off-time limit (see Figure 3).

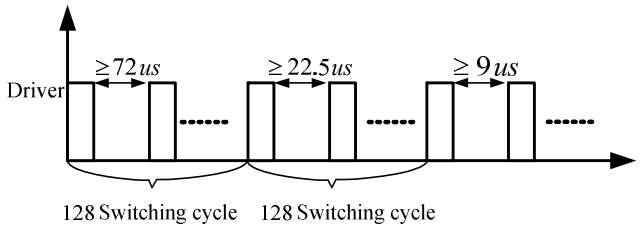


Figure 3: $\tau_{min\,off}$ at Start-Up

Constant Voltage Operation

MP158 acts as a fully-integrated regulator when used in the Buck topology, as shown in the typical application on page1.

It regulates the output voltage by monitoring the sampling capacitor.

At the beginning of each cycle, the integrated MOSFET turns on while the feedback voltage drops below the 2.55V reference voltage, which indicates insufficient output voltage. The peak current limitation determines the ON period. After the ON period elapses, the integrated MOSFET turns off. Sampling capacitor (C3) voltage is charged to the output voltage when the freewheeling diode (D1) turns on. In this way, the sampling capacitor (C3) samples and holds the output voltage for output regulation. The sampling capacitor (C3) voltage decreases when the L1 inductor current falls below the output current. When the feedback voltage falls below the 2.55V reference voltage, a new switching cycle begins. Figure 4 shows this operation under CCM in detail.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

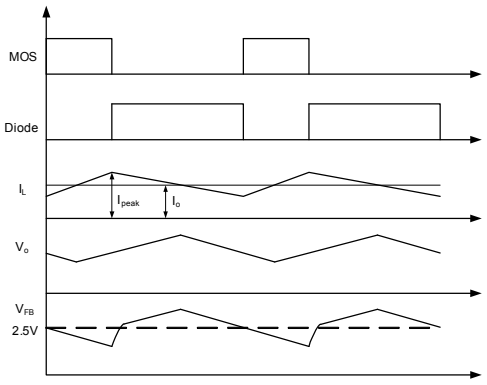


Figure 4: V_{FB} vs. V_O

Use the following equation to determine the output voltage:

$$Vo = 2.55V \times \frac{R1+R2}{R2}$$

Frequency Foldback and Peak Current Compression

The MP158 remains highly efficient under light-load condition by reducing the switching frequency and peak current automatically.

Under light-load or no-load conditions, the output voltage drops very slowly, which increases the MOSFET off time. Thus the switching frequency decreases as the load decreases.

Determine the switching frequency as:

$$f_s = \frac{(V_{in}-V_o)}{2L(I_{peak}-I_o)} \cdot \frac{V_o}{V_{in}}, \text{ for CCM}$$

$$f_s = \frac{2(V_{in}-V_O)}{LI^2_{peak}} \cdot \frac{I_o V_o}{V_{in}}, \text{ for DCM}$$

At the same time, the peak current limit decreases as the off-time increases. In standby mode, the frequency and the peak current are both minimized, allowing for a smaller dummy load. As a result, peak-current compression helps further reduce no-load consumption. Peak current limit can be estimated from the following equation (τ_{off} is the MOSFET's off time):

$$I_{Peak} = 101mA - (1mA/\mu s) \times (\tau_{off} - 9\mu s)$$

EA Compensation

MP158 has internal error amplifier and compensation loop. It samples the feedback voltage 6μs after the MOSFET turns off, and regulates the output based on the 2.55V reference voltage.

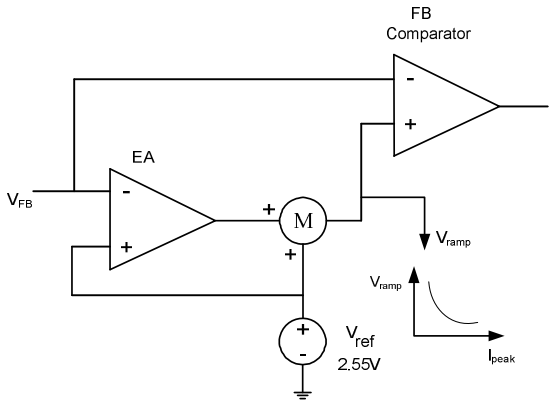


Figure 5: EA and Ramp Compensation

Ramp Compensation

An internal ramp compensation circuit improves the load regulation. As shown in Figure 5, an exponential signal added to pull down the reference voltage of the feedback comparator. The ramp compensation is a function of the load conditions: the compensation is about the 1mV/μs under full-load conditions compensation increases exponentially as the peak current decreases.

Over-Load Protection (OLP)

Maximum output power of MP158 is limited by maximum switching frequency and peak current limit. If the load current is too large, output voltage drops, so that the FB voltage drops.

When the FB voltage drops below 1.7V, it is considered as an error flag and timer starts. If the timer reaches 120ms (f_s=50kHz), OLP occurs. This timer duration avoids triggering OLP when the power supply starts up or load transition. The power supply should start up in less than 120ms (f_s=50kHz). The OLP delay time is calculated as per the following equation:

$$\tau_{Delay} \approx 120ms \times \frac{50kHz}{fs}$$

Short-Circuit Protection (SCP)

The MP158 monitors the peak current, and shuts down when the peak current rises above SCP threshold through short-circuit protection. The

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

power supply resumes operation with the removal of the fault.

Thermal Shutdown (OTP)

To prevent any thermal induced damage, the MP158 shuts down when the junction temperature exceeds 150°C. During the thermal shutdown (OTP), the VCC capacitor is discharged to 2.4V, and then the internal high voltage regulator re-charges. MP158 recovers when junction temperature drops below 120°C

Open-Loop Detection

If V_{FB} is less than 60mV, the IC stops switching and a re-start cycle begins. During Soft-Start, the open loop detection is blanked.

Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit avoids premature switching pulse termination due to turn on sipke. Turn on spike caused by parasitic capacitance and reverse recovery of freewheeling diode. During the blanking time, the current comparator is disabled and can not turn off the external MOSFET. Figure Figure 6 shows the leading-edge blanking.

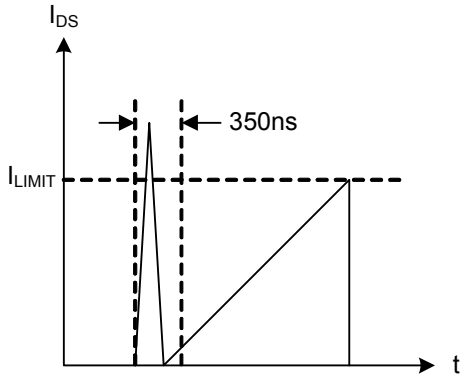
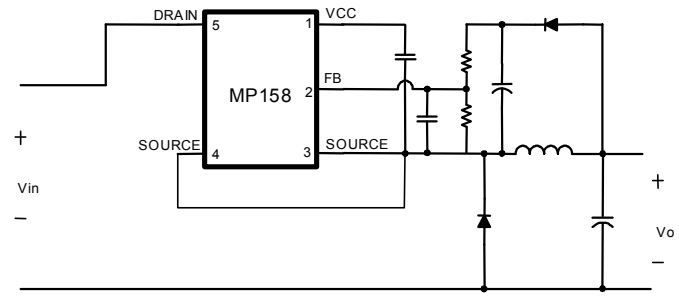
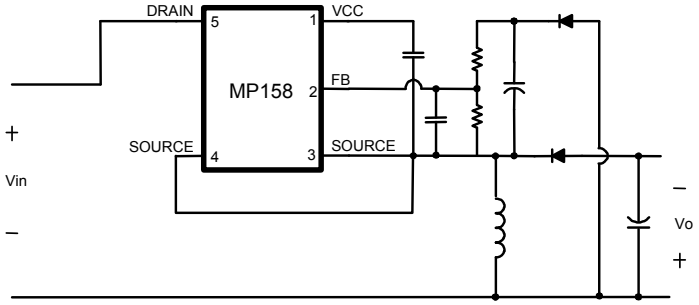
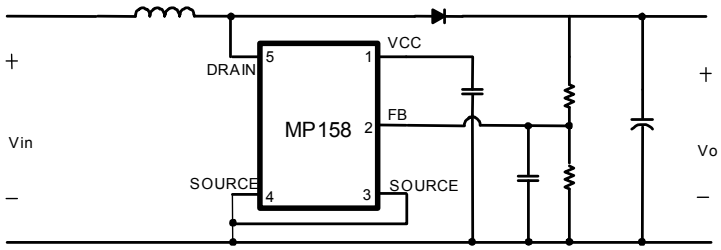
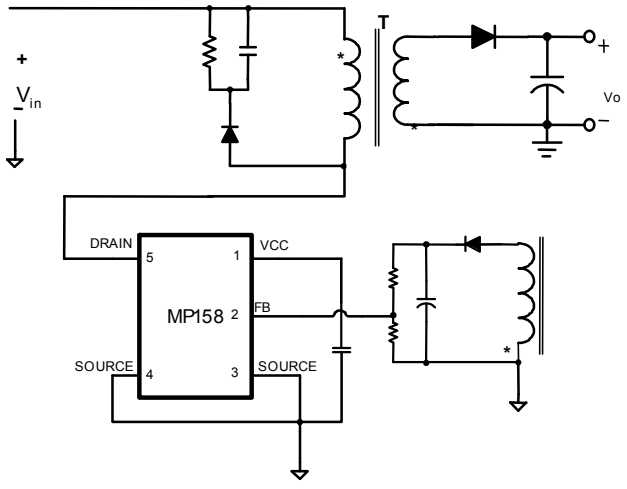


Figure 6: Leading-Edge Blanking

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

APPLICATION INFORMATION

Table 1. Common Topologies Using MP158

Topology	Circuit Schematic	Features
High-Side Buck		**1. No-isolation,** **2. Positive output** **3. Low cost** **4. Direct feedback**
High-Side Buck-Boost		**1. No-isolation,** **2. Negative output** **3. Low cost** **4. Direct feedback**
Boost		**1. No-isolation,** **2. Positive output** **3. Low cost** **4. Direct feedback**
Flyback		**1. Isolation,** **2. Positive output** **3. Low cost** **4. Indirect feedback**

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

Topology Options

MP158 can be used in common topologies, such as Buck, Buck-Boost, Boost and Flyback, as illustrated in table 1.

Component Selection

Input Capacitor

The input capacitor supplies the DC input voltage for the converter. Figure 7 shows the typical DC bus voltage waveform of a half-wave rectifier.

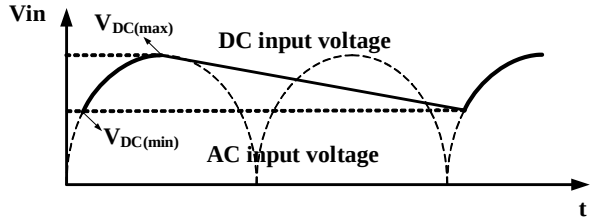


Figure 7: Input Voltage Waveform

Typically, a half-wave rectifier requires an input capacitor rated at 3uF/W for the universal input condition. When using a full-wave rectifier, input capacitor is chosen as 1.5~2uF/W for the universal input condition. A minimum DC voltage below 70V should be usually avoided, since it may cause thermal issue.

Inductor

The MP158 has a minimum off-time limit that determines the maximum power output. The maximum power increases as the inductor increases. Using a very small inductor may cause failure at full load, but a larger inductor means a higher OLP load. It is recommended to select an inductor with the minimum value that can supply the rated power. Estimate the maximum power with:

$$P_{omax} = V_o(I_{peak} - \frac{V_o \tau_{minoff}}{2L}), \text{ for CCM}$$

$$P_{omax} = \frac{1}{2} L I_{peak}^2 \cdot \frac{1}{\tau_{minoff}}, \text{ for DCM}$$

For mass production, tolerance on the parameters, such as peak current limitation, minimal off time, should be taken into consideration.

To reduce costs, use a standard off-the-shelf inductor no less than the calculated value.

Freewheeling Diode

The diode should be selected based on maximum input voltage and peak current.

The freewheeling diode's reverse recovery can affect efficiency and circuit operation under CCM, so use an ultra fast diode such as the EGC10JH.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Estimate the output voltage ripple as:

$$V_{CCM_ripple} = \frac{\Delta i}{8 f_s C_o} + \Delta i \cdot R_{ESR}, \text{ for CCM}$$

$$V_{DCM_ripple} = \frac{I_o}{f_s C_o} \cdot \left(\frac{I_{pk} - I_o}{I_{pk}} \right)^2 + I_{pk} \cdot R_{ESR}, \text{ for DCM}$$

It is recommended to use ceramic, tantalum or low ESR electrolytic capacitors to reduce the output voltage ripple.

Feedback Resistors

The resistor divider determines the output voltage. Appropriate R1 and R2 values should be chosen to maintain V_{FB} at 2.55V. R2 is typically 5kΩ to 10kΩ, avoid large R2 value.

Feedback Capacitor

The feedback capacitor provides a sample and hold function. Small capacitors result in poor regulation at light loads, and large capacitors affect the circuit operation. Roughly estimate an optimal capacitor value using the following equation:

$$\frac{1}{2} \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o} \le C_{FB} \le \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o}$$

Dummy Load

A dummy load is required to maintain the load regulation. This ensures sufficient inductor energy to charge the sample and hold capacitor to detect the output voltage. Normally a 2mA dummy load is needed and can be adjusted according to the regulated voltage. The dummy load reduces the efficiency and increases the no-load consumption.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

So, when reducing dummy load to achieve 30mW no load requirement, no load regulation will get worse.

Use a zener to reduce no-load consumption if no-load regulation is not a concern.

Auxiliary VCC Supply

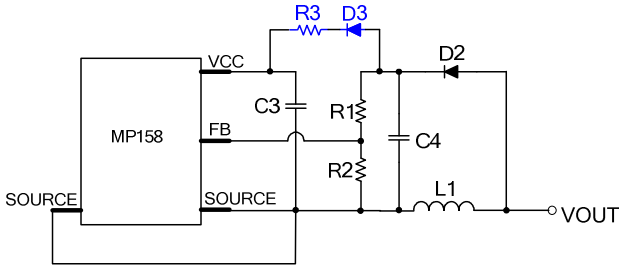


Figure 8: Auxiliary V_{CC} Supply Circuit

For V_O above 7V applications, MP158 can achieve the 30mW no-load power requirement. In order to do this, chip requires an external VCC supply to reduce overall power consumption.

This auxiliary VCC supply is derived from the resistor connected between C3 and C4. C4 should be set larger than recommendation above. D3 is used in case that VCC interfere with FB, R3 is determined per the formula below.

$$R \approx \frac{V_o - 5.8V}{I_S}$$

Where I_S is the VCC consumption under no load condition. R should be adjusted to meet the actual I_S, because it varies in different application. In a particular configuration, I_S is measured as about 180uA.

Surge Performance

Select an appropriate input capacitor value to obtain a good surge performance. Figure 9 shows the half-wave rectifier. Table 2 shows the capacitance required under normal condition for different surge voltages. In this test, FR1 is 20Ω/2W fused resistor and L1 is 1mH.

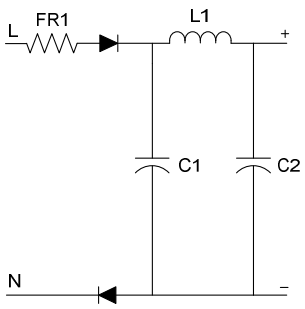


Figure 9: Half-Wave Rectifier

Table 2: Recommended Capacitance

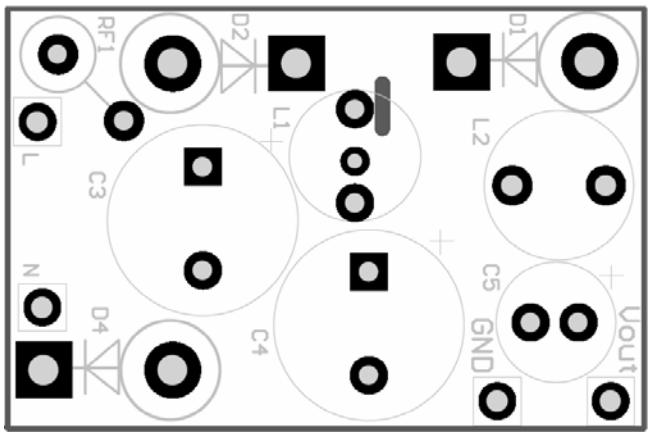
Surge voltage	500V	1000V	2000V
C1	1μF	10μF	22μF
C2	1μF	4.7μF	10μF

Layout Guide

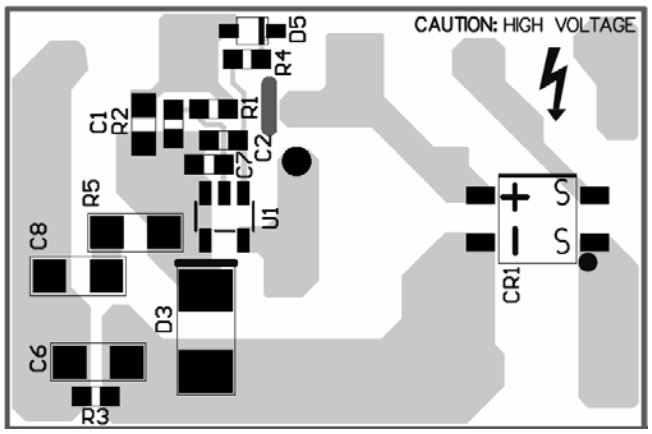
PCB layout is very important for reliable operation, good EMI and thermal performance. Please follow these guidelines to optimize performance.

1) Minimize the loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.
2) Place the power inductor far away from the input filter while keeping the loop area to the inductor to a minimum, see example below.
3) Place a capacitor valued at several hundred pF between the FB pin and source as close the IC as possible.
4) Connect exposed pads or larger copper area with the DRAIN pin to improve thermal performance.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.



Top



Bottom Layer

Design Example

Below is a design example following the application guidelines for the specifications:

Table 3: Design Example

V_{IN}	35VAC to 145VAC
V_{OUT}	4V
I_{OUT}	50mA

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

Figure 10 shows a typical application example of a 4V, 50mA non-isolated power supply using MP158.

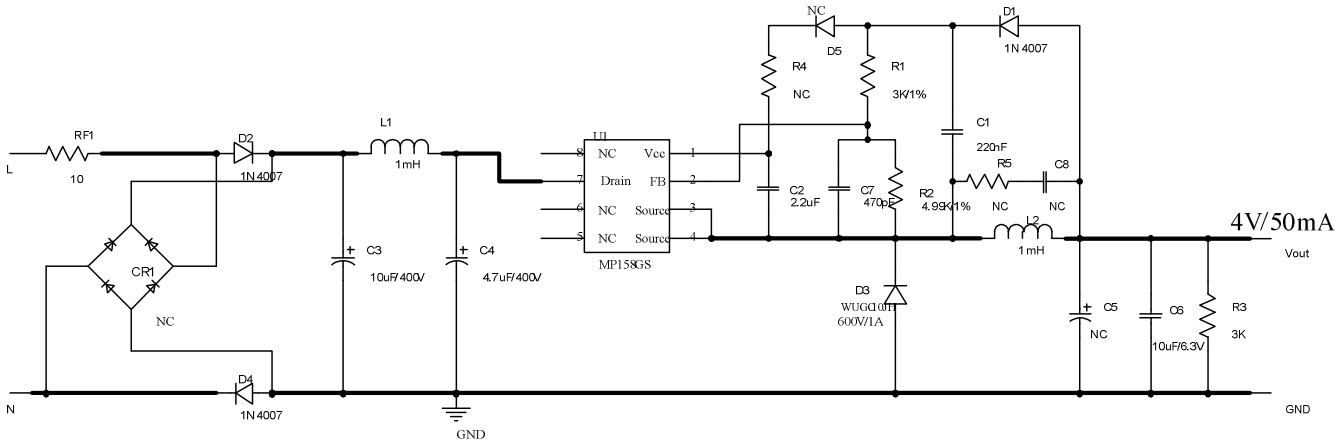
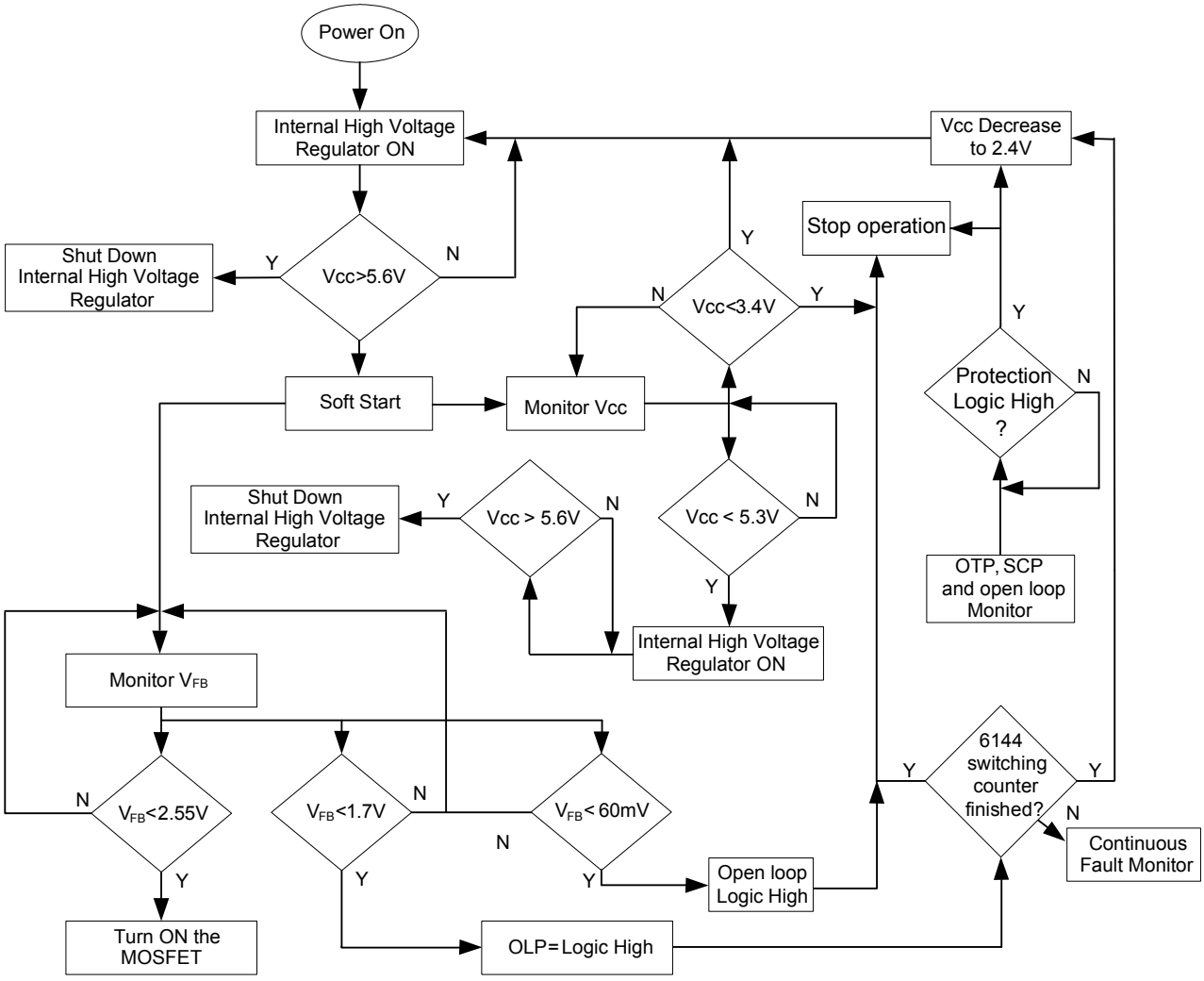


Figure 10: Typical Application at 4V, 50mA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

FLOW CHART



UVLO, SCP, OLP, OTP and Open loop protections are auto restart

Figure 11: Control Flow Chart

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

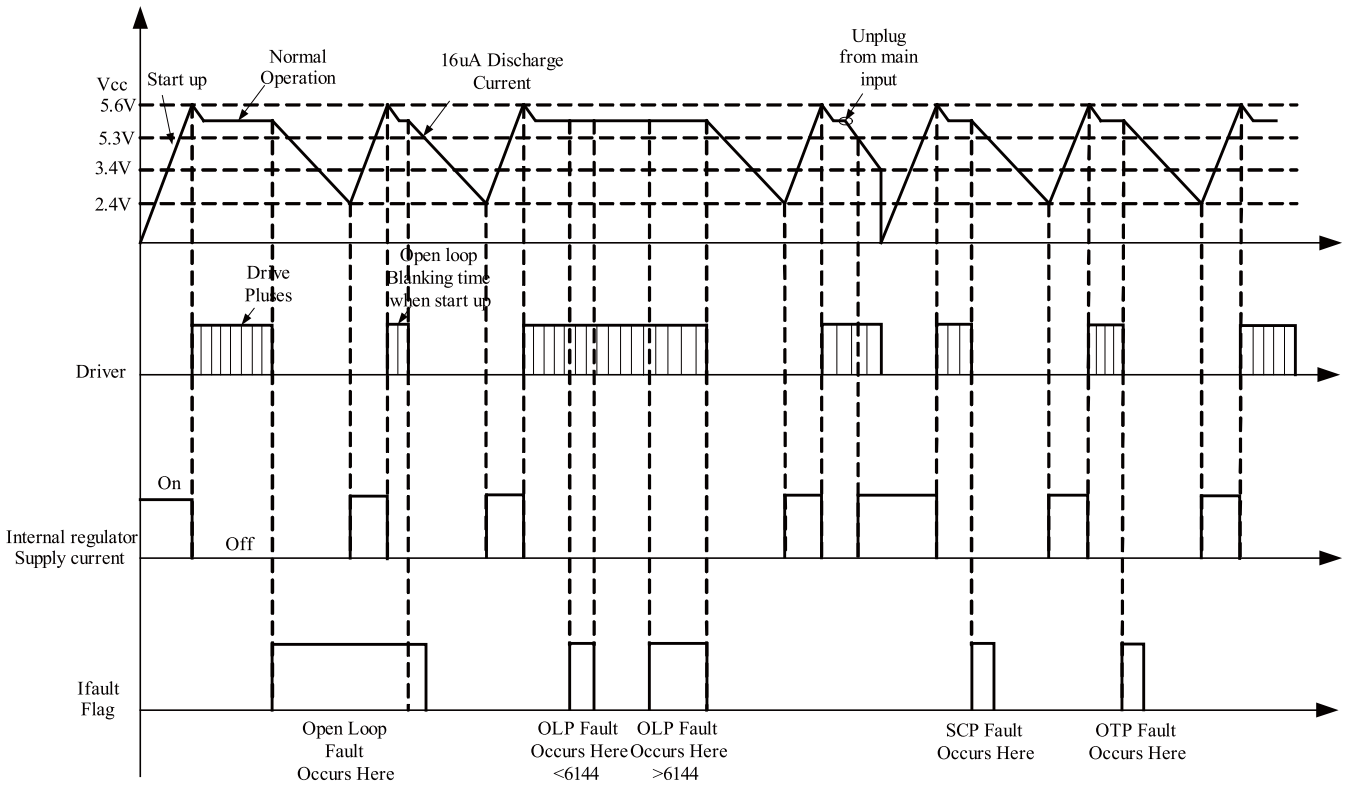
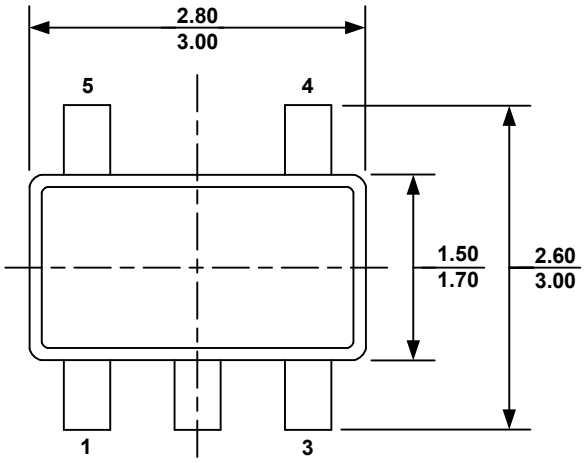


Figure 12: Signal Evolution in the Presence of a Fault

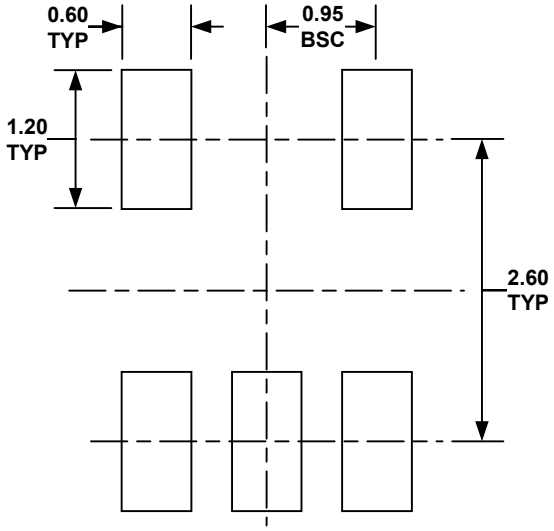
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

PACKAGE INFORMATION

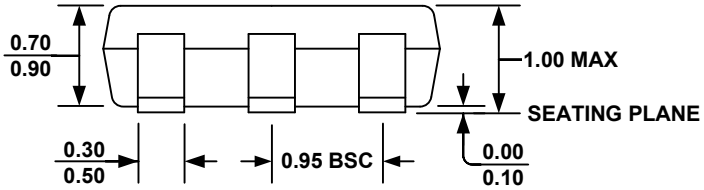
TSOT23-5



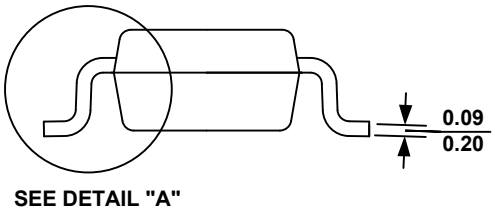
TOP VIEW



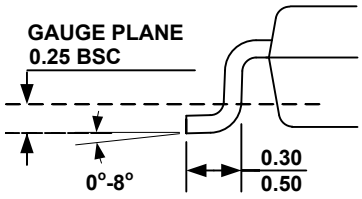
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

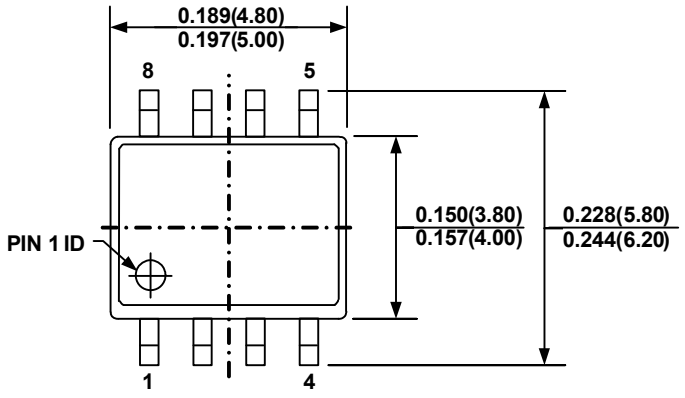
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

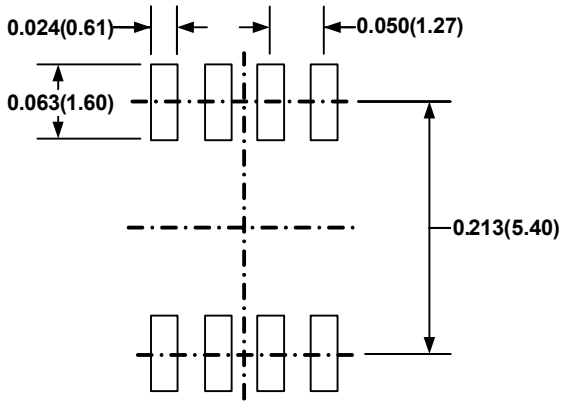
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

PACKAGE INFORMATION

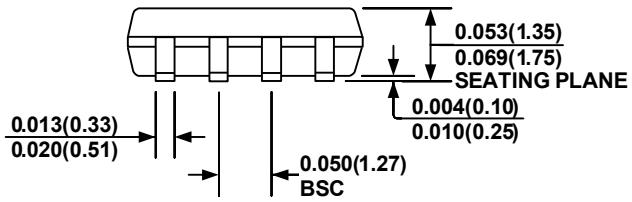
SOIC-8



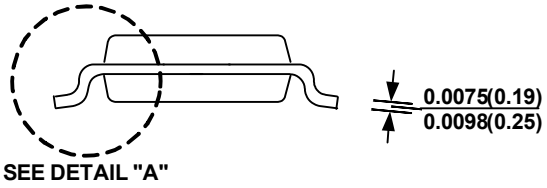
TOP VIEW



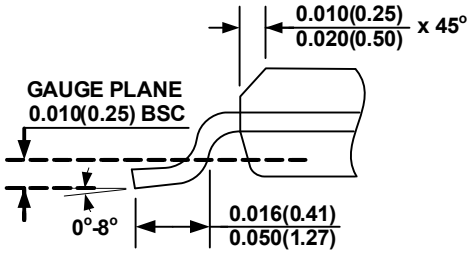
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS012, VARIATION AA.
6) DRAWING IS NOT TO SCALE

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.